MS440GX Motherboard
Technical Product Specification

June 1998

Order Number 710790-001

The MS440GX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the MS440GX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the MS440GX Motherboard Technical Product Specification	June 1998

This product specification applies only to standard MS440GX motherboards with BIOS identifier 4M4SG0x0.86E.

Changes to this specification will be published in the MS440GX Motherboard Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the MS440GX motherboard. It describes the standard motherboard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the motherboard and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically not intended for general audiences.

What this Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	Features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes
6	A listing of where to find information about specifications supported by the motherboard

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

A note calls attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions which, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn is the relative coordinates of its location on the motherboard, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. There is only one such connector at that location.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.

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1 Motherboard Description

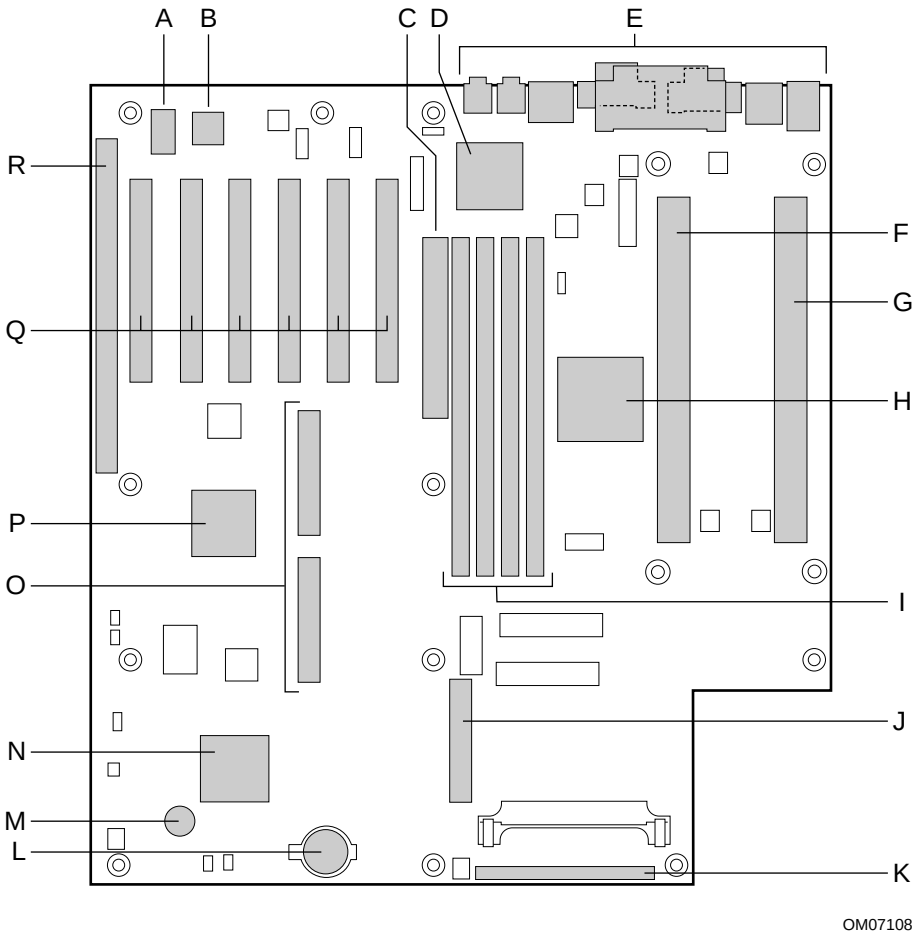
This chapter describes the board's hardware features. The contents of the chapter include:

1.1 Overview

The MS440GX motherboard's features are summarized below.

Form factor	Custom ATX (12 inches by 13 inches)
Processor(s)	• Two Slot 2 connectors • Support for one or two Pentium® II Xeon™ processors • 100 MHz host bus speed • 512 KB or 1 MB of L2 cache support on each processor
Chipset	Intel® 82440GX, consisting of: • 82443GX PCI/AGP controller (PAC) • 82371EB PCI ISA IDE Xcelerator (PIIX4E)
Memory	• Four dual inline memory module (DIMM) sockets • Support for up to 2 GB of 100 MHz SDRAM • Support for ECC DIMMs only
I/O Control	National Semiconductor PC97307 I/O controller
Peripheral Interfaces	• Two serial ports • Two Universal Serial Bus (USB) ports • One parallel port • Two IDE interfaces with Ultra DMA support • One diskette drive interface
Video	One AGP slot
Audio	• Crystal Semiconductor CS4235 audio codec • Crystal Semiconductor CS9236 wavetable synthesizer
LAN	Intel® 82558 10/100 Mbps PCI LAN controller
Hardware Monitor	• Microprocessor system hardware monitor (Analog Devices ADM9240 or equivalent) • Wired for Management (WfM) 1.1a compliant (see Section 6.2 for compliance level)
Expansion capabilities	• Five PCI slots • One shared slot for either a PCI or an ISA add-in card
BIOS	• Intel® E28F004BXT80 4 Mbit flash memory • Support for SMBIOS, ACPI, APM, and Plug and Play (see Section 6.2 for specification compliance levels)

Figure 1 shows the major components of the motherboard.



A	Intel® E28F004BXT80 4 Mbit flash memory	J	Diskette drive connector
B	Crystal Semiconductor CS4235 audio codec	K	Front panel connector
C	AGP connector	L	Battery
D	82558 PCI LAN controller	M	Piezoelectric speaker
E	Back panel connectors	N	National Semiconductor PC97307 I/O controller
F	Boot processor slot (P0)	O	IDE connectors
G	Application processor slot (P1)	P	82371EB PIIX4E
H	82443GX PAC	Q	PCI bus add-in card connectors
I	DIMM sockets	R	ISA bus add-in card connector

Figure 1. Motherboard Components

1.2 Processor

The motherboard supports:

- One or two Pentium II Xeon processors
- 400- or 450-MHz processor speeds
- 100-MHz host bus speed
- L2 caches of 512 KB or 1 MB

The processor's VID pins automatically program the voltage regulator(s) on the motherboard to the required processor voltage.

1.2.1 Processor Packaging

The processor is packaged in a single edge contact cartridge (S.E.C.C.). The S.E.C.C. includes the processor core, second-level cache, thermal plate, and back cover.

The processor connects to the motherboard through the Slot 2 connector, a 330-pin edge connector. When mounted in a Slot 2 connector, the processor is secured by a retention mechanism attached to the motherboard.

1.2.2 Second Level Cache

The 512 KB or 1 MB ECC second-level cache is located on the substrate of the S.E.C.C.. All onboard system memory is cacheable.

1.2.3 Processor Options

The following processor configuration options can be used:

- A single 400-MHz processor installed in the boot processor slot (P0) and a terminator card installed in the application processor slot (P1). P0 is the Slot 2 connector closest to the middle of the board. See page 11 for the location of the processor slots.
- Dual 400-MHz processors. When using two processors, a voltage regulator module (VRM) must be installed. See page 37 for the location of the VRM connector.
- A single 450-MHz processor installed in the boot processor slot (P0) and a terminator card installed in the application processor slot (P1). See page 11 for the location of the processor slots.
- Dual 450-MHz processors. When using two processors, a VRM must be installed. See page 37 for the location of the VRM connector.

Use configure mode to set the processor speed if necessary (see Section 1.11). If you are installing two processors, the following values must be identical for both processors:

- Processor speed
- L2 cache size
- Operating voltages

CAUTION

If the processor operating voltages for either VCC core or VCC L2 do not match, the computer will not boot.

1.3 System Memory

The motherboard has four DIMM sockets. Minimum memory size is 32 MB; maximum memory size is 2 GB. The BIOS automatically detects memory type, size, and speed. See page 11 for the location of the DIMM sockets. The DIMM socket closest to the boot processor slot is Bank 0; the DIMM socket closest to the AGP slot is Bank 3.

The motherboard supports the following memory features:

- PC100 compliant 168-pin DIMMs with gold-plated contacts (see Section 6.2 for information about this specification)
- 3.3 V unbuffered or registered (not mixed) 100-MHz ECC SDRAM DIMMs only
- Single- or double-sided DIMMs in the sizes listed in Table 1

Table 1. Supported DIMM Sizes

DIMM Size	Configuration
16 MB	2 Mbit x 72
32 MB	4 Mbit x 72
64 MB	8 Mbit x 72
128 MB	16 Mbit x 72
256 MB	32 Mbit x 72
512 MB	128 Mbit x 72

Memory can be installed in one, two, three, or four sockets and populated in any order. Memory size can vary between sockets.

1.4 Chipset

The Intel® 440GX AGPset includes a Host-PCI bridge integrated with both an optimized DRAM controller and an AGP interface. The I/O subsystem of the 440GX is based on the PIIX4E, which is a highly integrated PCI-ISA/IDE Accelerator Bridge. This chipset consists of the Intel 82443GX PAC and the Intel 82371EB PIIX4E bridge chip.

1.4.1 Intel® 82443GX PAC

The PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, the AGP, and main memory. The PAC features:

- Processor interface control
  - — Support for processor host bus frequencies of 100 MHz only
  - — 32-bit addressing
  - — Desktop Optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for:
  - — +3.3 V only DIMM DRAM configurations
  - — Up to four double sided DIMMs
  - — 100-MHz PC100-compatible Synchronous DRAM
  - — DIMM serial presence detect via SMBus interface
  - — 2-, 4-, 8-, 16-, 32-, 64-, and 128-Mbit DRAM devices
  - — SDRAM 64-bit data interface with ECC support
  - — Symmetrical and asymmetrical DRAM addressing
- AGP Interface
  - — Complies with the AGP specification Rev 1.0 (see Section 6.2 for specification information)
  - — Support for +3.3 V AGP 1X and AGP 2X devices
  - — Synchronous coupling to the host-bus frequency
- PCI bus interface
  - — Complies with the PCI 33 MHz interface (see Section 6.2 for specification information)
  - — Asynchronous coupling to the host-bus frequency
  - — PCI parity generation support
  - — Data streaming support from PCI-to-DRAM
  - — Support for six PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - — Support for concurrent host, AGP, and PCI transactions to main memory
- Data buffering
  - — DRAM write buffer with read-around-write capability
  - — Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1/AGP-to-DRAM read buffers
  - — AGP dedicated inbound/outbound FIFOs (AGP 2X), used for temporary data storage
- Power management functions
  - — Support for system suspend/resume (DRAM and power-on suspend)
  - — Compliant with ACPI power management
- SMBus support for desktop management functions
- Support for system management mode (SMM)

1.4.2 Intel® 82371EB PIIX4E

The PIIX4E is a multifunction PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub function, and enhanced power management. The PIIX4E features:

- Multifunction PCI-to-ISA bridge
  - Support for the PCI bus at 33 MHz
  - Complies with the PCI specification (see Section 6.2 for specification information)
  - Full ISA bus support
- USB controller
  - Two USB ports (see Section 6.2 for specification information)
  - Support for legacy keyboard and mouse
  - Support for universal host controller interface (UHCI) Design Guide interface (see Section 6.2 for specification information)
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers up to 33 MB/sec
  - Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
  - Fast type-F DMA for reduced PCI bus usage
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for Wake-on-Modem, Wake on LAN† technology, and Wake on PME
  - Support for ACPI (see Section 6.2 for specification information)
  - System wakes from ACPI sleep state with keyboard activity
- Real-Time Clock
  - 256-byte battery-backed CMOS RAM
  - Includes date alarm
- 16-bit counters/timers based on 82C54
- Support for one- and two-way symmetric multiprocessing (SMP) Pentium II Xeon processor configurations

1.4.3 Intel® 82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC)

The Intel® 82093AA IOAPIC provides interrupt management and incorporates both static and dynamic symmetric interrupt distribution across all processors in a multiprocessor system. The 82093AA IOAPIC features 24 interrupts as follows:

- 13 ISA interrupts
- Four PCI interrupts
- One Interrupt/SMI# rerouting
- Two motherboard interrupts
- One interrupt used for INTR input
- Three general purpose interrupts
- SCI BIOS supported steering

1.4.4 USB

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The motherboard fully supports the universal host controller interface (UHCI) and uses UHCI-compatible software drivers. See Section 6.2 for information about the USB specification.

1.4.5 IDE Support

The motherboard has two independent bus-mastering IDE interfaces. These interfaces support PIO Mode 3, PIO Mode 4, ATAPI devices (e.g., CD-ROM), and Ultra DMA synchronous-DMA mode transfers. The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

The motherboard supports LS-120 diskette technology through its IDE interfaces. LS-120 diskette technology enables users to store 120 MB of data on a single, 3.5-inch removable diskette. LS-120 technology is backward compatible (both read and write) with 1.44 MB and 720 KB DOS-formatted diskettes and is supported by Windows† 98 and Windows NT† operating systems.

The motherboard allows connection of an LS-120 compatible drive and a standard 3.5-inch diskette drive. If an LS-120 drive is connected to an IDE connector and configured as the A drive and a standard 3.5-inch diskette drive is configured as a B drive, the standard diskette drive must be connected to the diskette drive cable's "A" connector (the connector at the end of the cable). The LS-120 drive can be configured as a boot device, if selected in the BIOS setup utility.

1.4.6 Real-Time Clock, CMOS RAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS RAM in two banks that are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

An external coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 5 V applied.

1.5 I/O Controller

The PC97307 I/O controller from National Semiconductor is an ISA Plug and Play compatible (see Section 6.2), multifunction I/O device that provides the following features:

- Serial ports
  - Two 16450/16550A-software compatible UARTs
  - Internal send/receive 16-byte FIFO buffer
  - Four internal 8-bit DMA options for the UART with SIR support (USI)
- Multimode bidirectional parallel port
  - Standard mode: IBM and Centronics compatible
  - Enhanced parallel port (EPP) mode with BIOS and driver support
  - High-speed extended capabilities port (ECP) mode
- Diskette drive controller
  - DP8473 and N82077 compatible
  - 16-byte FIFO buffer
  - PS/2† diagnostic-register support
  - High-performance digital data separator (DDS)
  - PC-AT†, PS/2, and 3-mode diskette drive-mode support
- 8042A-compatible keyboard and mouse controller
- Support for IrDA† and Consumer infrared compliant infrared interface

By default, the I/O controller interfaces are automatically configured during boot up. The I/O controller can also be manually configured in the Setup program.

1.5.1 Serial Ports

The two 9-pin D-Sub serial port connectors on the back panel are compatible with 16450 and 16550A UARTs.

1.5.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the Setup program, the parallel port can be configured for the following:

- Compatible (standard mode)
- Bidirectional (PS/2 compatible)
- Extended Parallel Port (EPP)
- Enhanced Capabilities Port (ECP)

1.5.3 Diskette Drive Controller

The diskette drive controller is software compatible with the DP8473 and N82077 diskette drive controllers and supports both PC-AT and PS/2 modes. In the Setup program, the diskette drive interface can be configured to support up to two diskette drives for the following capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.5.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The 5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed.

⟹ NOTE

The mouse and keyboard can be plugged into either of the PS/2 connectors. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI Megakey keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power on/reset. A power on/reset password can be specified in Setup.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-On Self Test (POST).

1.6 AGP Support

AGP is a high-performance interconnect for graphic-intensive applications, such as 3D applications. AGP is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP provides these performance features:

- Pipelined-memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for near 100 percent bus efficiency
- AC timing for 133 MHz data transfer rates (AGP 2X), allowing data throughput of 533 MB/sec

An AGP add-in card connector is provided on the motherboard. See page 28 for more information on the AGP connector. See Section 6.2 for more information about the AGP specification.

1.7 Audio Subsystem

The onboard audio subsystem features the Crystal CS4235, an audio codec with an integrated FM synthesizer. The audio subsystem provides all the digital audio and analog mixing functions needed for recording and playing sound on personal computers. Together, these components feature the following:

- Stereo analog-to-digital and digital-to-analog converters
- Analog mixing, anti-aliasing, and reconstruction filters
- Line and microphone level inputs
- ADPCM, A-law, or μlaw digital audio compression/decompression
- Full digital control of all mixer and volume control functions
- High-quality, 16-bit, MPC-II compliant audio
- Full duplex operation
- AdLib†, Sound Blaster Pro† 2.0, Windows Sound System, and MPU-401 support
- Full DOS games compatibility
- MIDI/Game port support
- OPL3 compatible FM synthesizer
- BIOS Setup-based enable/disable

The audio subsystem requires up to two DMA channels and one IRQ. Table 2 shows the IRQ, DMA channel, and base I/O address options. These options are automatically chosen by the Plug and Play interface, so there are no default settings.

Table 2. Audio Subsystem Resources

Resource	IRQ (Options)	DMA Channel (Options)	I/O Address (Options)
Sound Blaster (DMA playback, DMA / IRQ shared with Windows Sound System capture)	5 (best choice) 7 9 (best choice) 11	0 (best choice) 3	210-21Fh 220-22Fh (best choice) 230-234h 240-24Fh 250-25Fh 260-26Fh
Windows Sound System (DMA playback)	7 9 (best choice) 11	0 1 (best choice) 3	534-537h (best choice) 608-60Bh
MPU-401 (IRQ shared with Sound Blaster)	5 (best choice) 7 9 (best choice) 11		300-301h 330-331h (best choice) 332-333h 334-335h
MIDI			200-207h
FM Synthesis			388-38Dh
CS4235 Control			FF0-FFFh

1.7.1 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 6.1). Audio driver support is provided for the Microsoft Windows NT 4.0, and Microsoft Windows 98 operating systems.

1.7.2 Audio Connectors

The audio connectors include the following:

- Back panel connectors: Line In, Line Out, Mic In (see page 24 for more information)
- CD-ROM audio (ATAPI)
- Telephony (ATAPI-style)

1.7.2.1 CD-ROM Audio

A 1 x 4-pin ATAPI-style connector is available for connecting an internal CD-ROM drive to the audio mixer. See page 33 for the location and pinout of the connector.

1.7.2.2 Telephony

A 1 x 4-pin ATAPI-style connector is available for connecting the monaural audio signals of an internal telephony device, such as a modem, to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, modems, and answering machines. See page 33 for the location and pinout of the connector.

1.8 Hardware Monitor Subsystem

The hardware monitor subsystem provides low-cost instrumentation capabilities. The features of the hardware monitor subsystem include:

- Management Level 4 functionality
- Microprocessor System Hardware Monitor (Analog Devices ADM9240, Dallas Semiconductor DS1780, National Semiconductor LM81, or equivalent)
  - — Integrated temperature and voltage monitoring to detect levels above or below acceptable values (+12 V, -12 V, +5 V, +3.3 V, and +2.5 V). When suggested ratings for temperature, fan speed, or voltage are exceeded, an interrupt is activated.
  - — Two fan speed sensors
  - — Access through the SMBus
- Remote reset capabilities from a remote peer or server through Intel® LANDesk® 3.3 (or later) Client Manager and service layers
- Headers for front and rear chassis intrusion connectors (see page 43)

See Section 6.2 for information about the management extension hardware specification.

1.9 Intel® EtherExpress™ PRO/100 PCI LAN Subsystem

The Intel® EtherExpress™ PRO/100 Wired for Management (WfM) PCI LAN subsystem is an Ethernet† LAN interface that provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32-bit direct bus mastering on the PCI bus
- Shared memory structure in the host memory that copies data directly to/from host memory
- 10Base-T and 100Base-TX capability using a single RJ-45 connector
- IEEE 802.3µ Auto-Negotiation for the fastest available connection

1.9.1 Intel® 82558 LAN Controller

The Intel 82558 LAN Controller provides the following functions:

- CSMA/CD Protocol Engine
- PCI bus interface (Rev 2.1 compliant)
- DMA engine for movement of commands, status, and network data across the PCI bus
- Integrated physical layer interface, including:
  - — Complete functionality necessary for the 10Base-T and 100Base-TX interfaces; when in 10 Mbit/sec mode, the interface drives the cable directly
  - — A complete set of MII management registers for control and status reporting
  - — 802.3µ Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices
- Integrated power management features, including:
  - — Support for ACPI
  - — Support for Wake on LAN technology
- Digitally controlled adaptive equalizations and transmission

1.9.2 Alert On LAN Component

The Alert on LAN component is a companion device to the Intel 82558 LAN controller. Together, these devices provide a management interface between a remote management console (or management server) and a client system monitoring instrumentation. When an alert input is asserted, the Alert on LAN component transmits Ethernet packets to the 82558 through an 8-bit dedicated data path. Examples of events that can trigger alert messages to a management server include:

- Chassis intrusion
- System BIOS hang (transmits POST error code)
- LAN leash (transmits an alert that the LAN cable was disconnected)
- Temperature out of specification

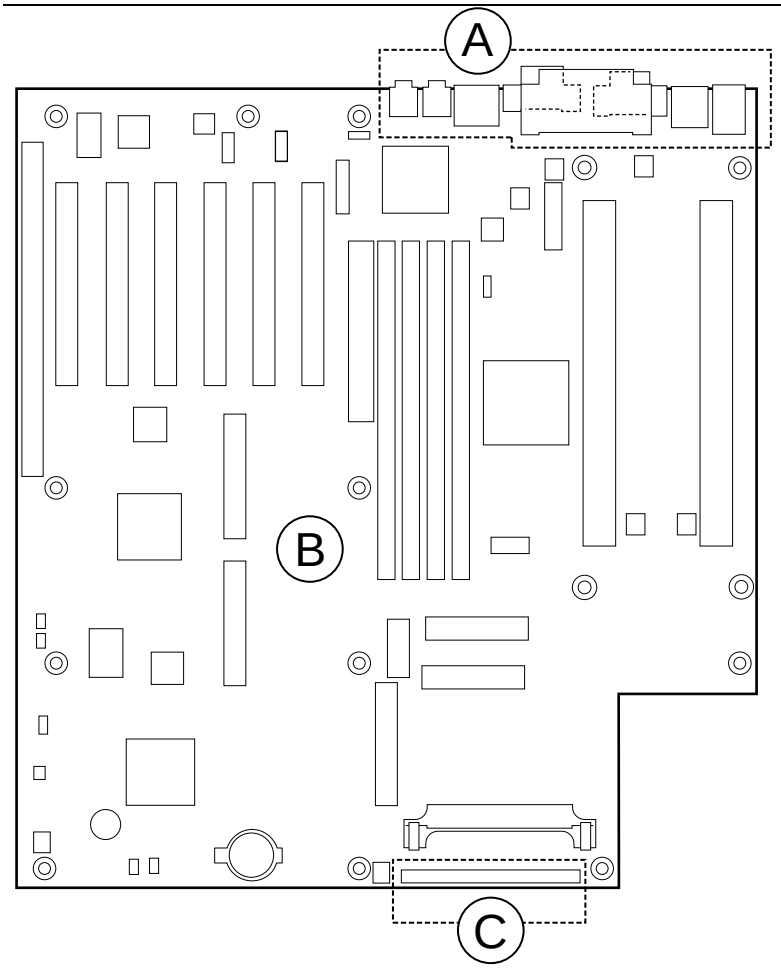
For more information on the Alert on LAN component and its network management capabilities, contact your local Intel sales office.

1.9.3 LAN Subsystem Software

The EtherExpress PRO/100 WfM PCI LAN software available for the board includes setup and diagnostic software (SETUP.EXE), a readme file viewer (README.EXE), and drivers. The LAN software is available from Intel's World Wide Web site (see Section 6.1).

1.10 Connectors

This section describes the board's connectors. The connectors are divided into three groups, as shown in Figure 2.



A. Back panel connectors (see page 24)

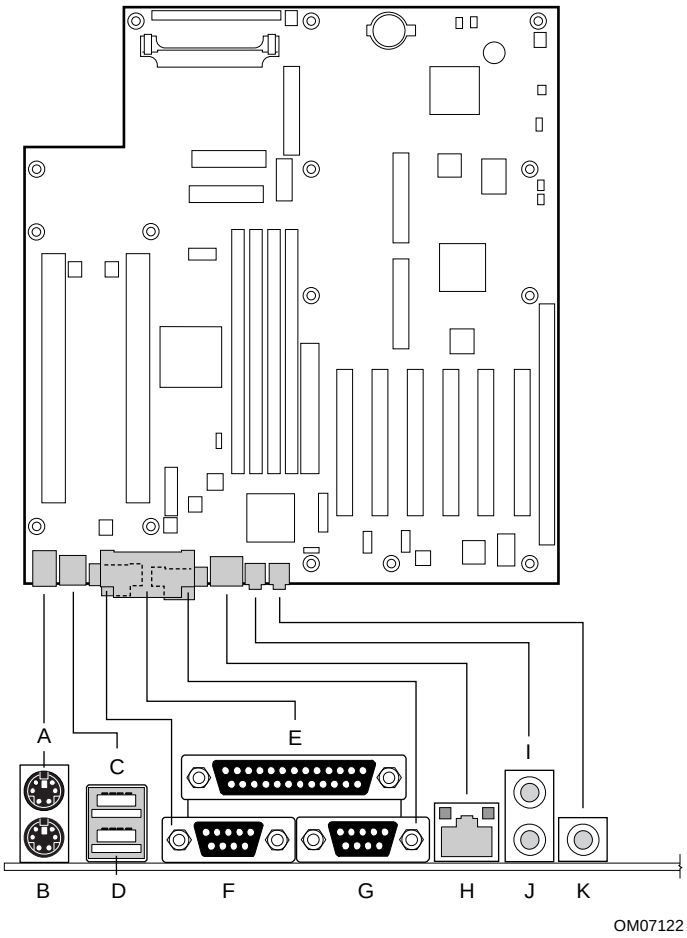
B. Midboard connectors (see page 27)

C. Front panel connectors (see page 45)

Figure 2. Connector Groups

1.10.1 Back Panel Connectors

Figure 3 shows the location of the back panel connectors. Tables 3 through 10 list the pinouts of the back panel connectors.



A	PS/2 Keyboard or Mouse	G	Serial Port B
B	PS/2 Keyboard or Mouse	H	LAN
C	USB Port 1	I	Audio Line Input
D	USB Port 0	J	Audio Line Output
E	Parallel Port	K	Microphone Input
F	Serial Port A		

Figure 3. Back Panel Connectors

Table 3. PS/2 Keyboard/Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 4. USB Connectors

Pin	Signal Name
1	Power (fused)
2	USBP0- [USBP1-]
3	USBP0+ [USBP1+]
4	Ground

Signal names in brackets ([ ]) are for USB port 1

Table 5. Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

Table 6. Serial Port Connectors

Pin	Signal Name	Pin	Signal Name
1	DCD	6	DSR#
2	Serial In#	7	RTS#
3	Serial Out#	8	CTS#
4	DTR#	9	RI#
5	Ground		

Table 7. LAN Connector

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	No connect
5	No connect
6	RX-
7	No connect
8	No connect

Table 8. Audio Line In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left In
Ring	Audio Right In

Table 9. Audio Line Out Connector

Pin	Signal Name
Sleeve	Ground
Tip	Audio Left Out
Ring	Audio Right Out

Table 10. Audio Mic In Connector

Pin	Signal Name
Sleeve	Ground
Tip	Mono In
Ring	Electret Bias Voltage

1.10.2 Midboard Connectors

The midboard connectors are divided into the following functional groups:

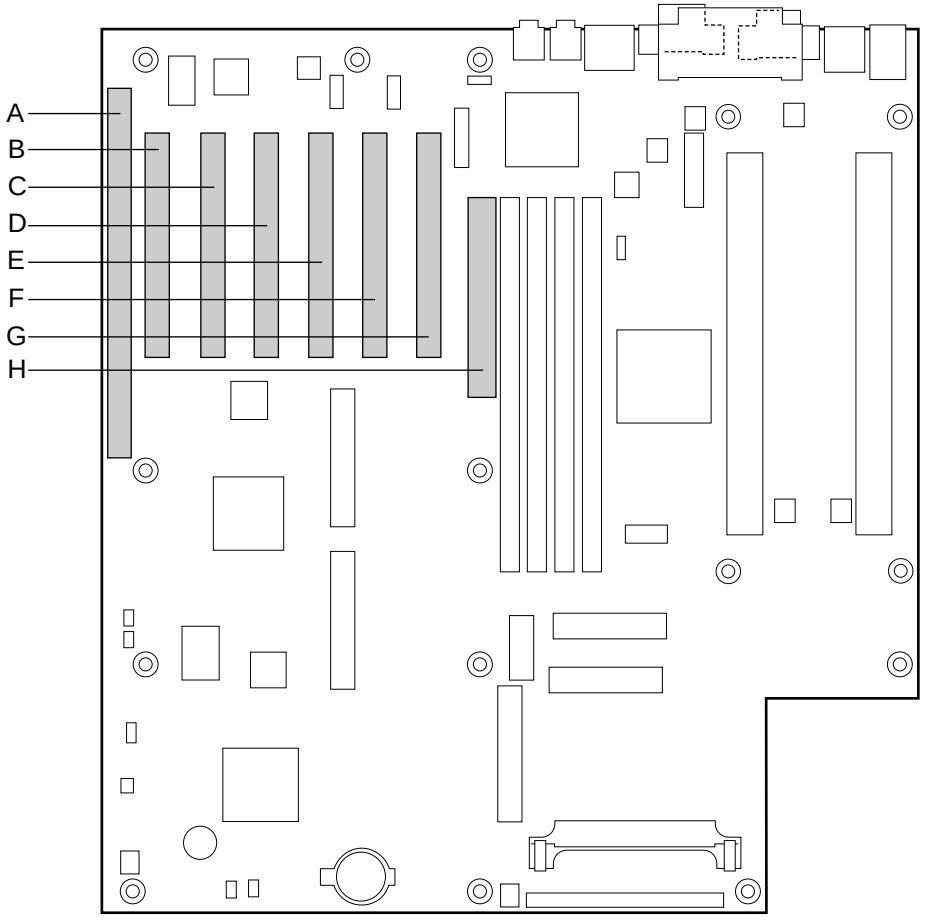
- Add-in card connectors (see page 28)
  - ISA
  - PCI
  - AGP
- Audio (see page 33)
  - ATAPI-style Telephony
  - ATAPI-style CD-ROM
  - MIDI/Joystick
  - External Speaker
- Fans (see page 35)
  - Processor heatsink fans (4)
  - Front chassis fans (2)
  - Rear chassis fan (1)
- Power (see page 37)
  - Power connector
  - Primary power supply
  - Secondary power supply
  - VRM
- Peripheral Interfaces (see page 40)
  - Diskette
  - SCSI LED
  - IDE
- Security and Hardware Management (see page 43)
  - Front Intrude
  - Rear Intrude
  - Wake on LAN
  - Wake on Modem

1.10.2.1 Add-in Card Connectors

When the board is installed in a chassis, there are a maximum of seven available slots for installing add-in cards as follows:

- One shared slot for an ISA or a PCI add-in card.
- Five dedicated PCI slots
- One AGP slot

All of the PCI bus connectors are bus master capable. Figure 4 shows the add-in card connectors. Tables 11 through 13 list the pinouts of the add-in card connectors.



A	ISA bus connector (slot shared with PCI bus connector 6)	E	PCI bus connector 3
B	PCI bus connector 6 (shared with ISA bus connector)	F	PCI bus connector 2
C	PCI bus connector 5	G	PCI bus connector 1
D	PCI bus connector 4	H	AGP connector

Figure 4. Add-in Card Connectors

Table 11. ISA Bus Connector

Pin	Signal Name	Pin	Signal Name
B1	Ground	A1	IOCHK# (IOCHCK#)
B2	RESET (RESDRV)	A2	SD7
B3	+5 V	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	SRDY# (NOWS#)	A8	SD1
B9	+12 V	A9	SD0
B10	Ground	A10	IOCHRDY (CHRDY)
B11	SMEMW# (SMWTC#)	A11	AEN
B12	SMEMR# (SMRDC#)	A12	SA19
B13	IOW# (IOWC#)	A13	SA18
B14	IOR# (IORC#)	A14	SA17
B15	DACK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
Key		Key	
D1	MEMCS16# (M16#)	C1	SBHE#
D2	IOCS16# (IO16#)	C2	LA23
D3	IRQ10	C3	LA22

Note: Items in parentheses are alternate versions of signal names.

continued

Table 11. ISA Bus Connector (continued)

Pin	Signal Name	Pin	Signal Name
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR# (MRDC#)
D10	DACK5#	C10	MEMW# (MWTC#)
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	Master16# (MASTER#)	C17	SD14
D18	Ground	C18	SD15

Note: Items in parentheses are alternate versions of signal names.

Table 12. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+5 V (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	PRSNT1#	A40	SDONE	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	SBO#	B41	+3.3 V
A11	Reserved	B11	PRSNT2#	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	Reserved	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

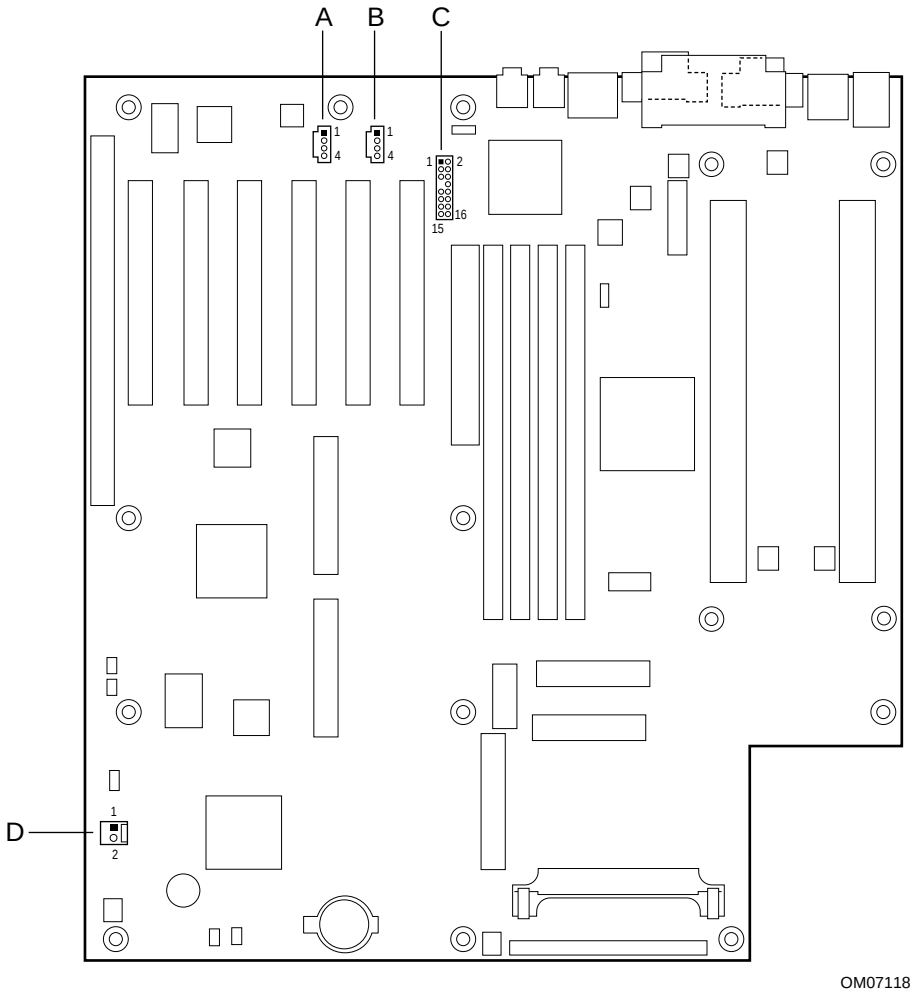
* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

Table 13. AGP Connector

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12V	B1	No Connect	A34	Vcc3.3	B34	Vcc3.3
A2	No Connect	B2	Vcc	A35	AGP_AD22	B35	AGP_AD21
A3	Reserved	B3	Vcc	A36	AGP_AD20	B36	AGP_AD19
A4	No Connect	B4	No Connect	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AGP_AD18	B38	AGP_AD17
A6	INTA#	B6	INTB#	A39	AGP_AD16	B39	AGP_CBE2#
A7	RST#	B7	HCLK_AGP	A40	Vcc3.3	B40	Vcc3.3
A8	AGP_GNT1#	B8	AGP_REQ1	A41	AGP_FRAME#	B41	AGP_IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	Reserved
A10	AGP_ST1	B10	AGP_ST0	A43	Ground	B43	Ground
A11	Reserved	B11	AGP_ST2	A44	Reserved	B44	Reserved
A12	AGP_PIPE#	B12	AGP_RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	AGP_TRDY#	B46	AGP_DEVSEL#
A14	No Connect	B14	No Connect	A47	AGP_STOP#	B47	Vcc3.3
A15	SBA1	B15	SBA0	A48	No Connect	B48	AGP_PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	AGP_PAR	B50	AGP_SERR#
A18	Reserved	B18	SB_STB	A51	AGP_AD15	B51	AGP_CBE1#
A19	Ground	B19	Ground	A52	Vcc3.3	B52	Vcc3.3
A20	SBA5	B20	SBA4	A53	AGP_AD13	B53	AGP_AD14
A21	SBA7	B21	SBA6	A54	AGP_AD11	B54	AGP_AD12
A22	Key	B22	Key	A55	Ground	B55	Ground
A23	Key	B23	Key	A56	AGP_AD9	B56	AGP_AD10
A24	Key	B24	Key	A57	AGP_CBE0#	B57	AGP_AD8
A25	Key	B25	Key	A58	Vcc3.3	B58	Vcc3.3
A26	AGP_AD30	B26	AGP_AD31	A59	Reserved	B59	AD_STB0
A27	AGP_AD28	B27	AGP_AD29	A60	AGP_AD6	B60	AGP_AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AGP_AD26	B29	AGP_AD27	A62	AGP_AD4	B62	AGP_AD5
A30	AGP_AD24	B30	AGP_AD25	A63	AGP_AD2	B63	AGP_AD3
A31	Ground	B31	Ground	A64	Vcc3.3	B64	Vcc3.3
A32	Reserved	B32	AD_STB1	A65	AGP_AD0	B65	AGP_AD1
A33	AGP_CBE3#	B33	AGP_AD23	A66	No Connect	B66	No Connect

1.10.2.2 Audio Connectors

Figure 5 shows the locations of the audio connectors. Tables 14 through 17 list the pinouts of the audio connectors.



A ATAPI CD-ROM
B ATAPI-style telephony
C MIDI/Joystick
D External speaker

Figure 5. Audio Connectors

Table 14. ATAPI-Style Telephony Connector

Pin	Signal Name
1	MONO_IN (from external device)
2	Ground
3	Ground
4	TEL_MICIN

Table 15. ATAPI CD Audio Connector

Pin	Signal Name
1	Left CD In
2	Ground
3	Ground
4	Right CD In

Table 16. MIDI/Joystick Connector

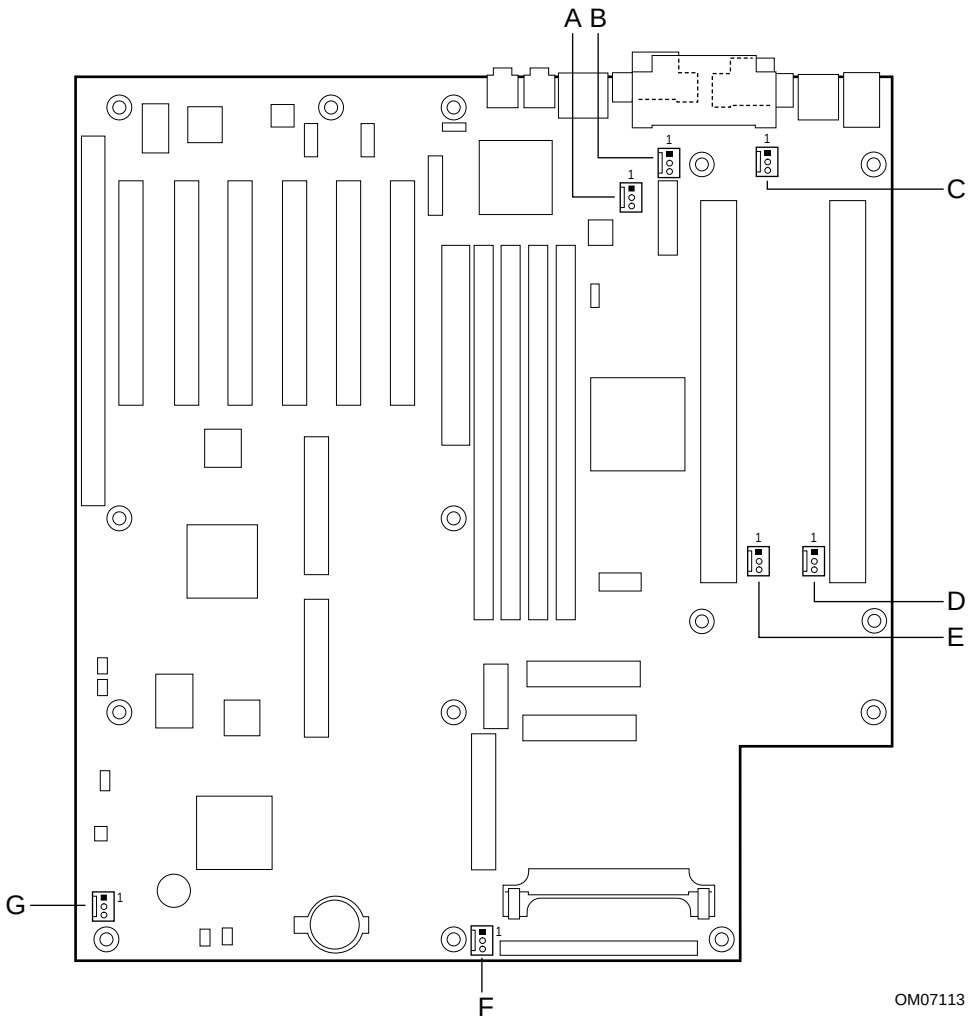
Pin	Signal Name	Pin	Signal Name
1	+5 V (fused)	9	Ground
2	+5 V (fused)	10	JBCY
3	JAB1	11	JACY
4	JBB1	12	JBB2
5	JACX	13	JAB2
6	JBCX	14	MIDI-IN
7	No connect	15	+5 V (fused)
8	MIDI-OUT	16	MIDI-PRESENT GP#

Table 17. External Speaker Connector

Pin	Signal Name
1	+5 V
2	BUZZER_A

1.10.2.3 Fan Connectors

There are seven fan connectors: four are used for processor heatsink fans and three are for chassis fans. Figure 6 shows the location of the fan connectors. Table 18 lists the pinout of the fan connectors.



A	Rear chassis fan	E	Processor heatsink fan
B	Processor heatsink fan	F	Front chassis fan 1
C	Processor heatsink fan	G	Front chassis fan 2
D	Processor heatsink fan		

Figure 6. Fan Connectors

The maximum current ratings for the fan connectors are as follows:

- Rear chassis fan (600 mA)
- Processor heatsink fans (150 mA each)
- Front chassis fan 1 (500 mA)
- Front chassis fan 2 (300 mA)

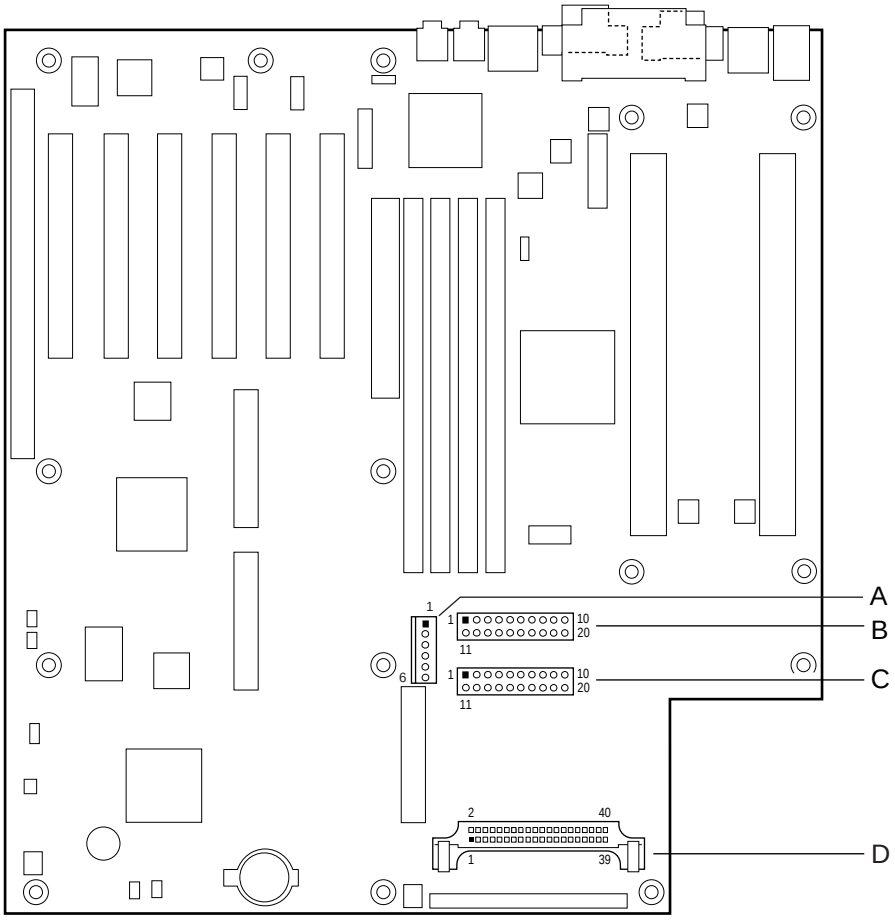
Table 18. Fan Connectors

Pin	Signal Name
1	FAN_ENABLE
2	+12 V
3	TACH_OUT

1.10.2.4 Power Connectors

There are three power supply connectors and one connector for a VRM. Figure 7 shows the power connectors. Tables 19 through 21 list the pinouts of the power connectors.

The primary and secondary power supply connectors are identical; either may be used with the 6-pin power connector for system configurations requiring less than 300 W. If the system power requirements exceed 300 W, a power supply with two 20-pin connectors and a 6-pin connector can be used, or dual power supplies can be used. VRMs used with this board must be compatible with the *VRM 8.3 DC-DC Converter Design Guidelines* document.



A Power connector
B Secondary power supply connector
C Primary power supply connector
D VRM connector

Figure 7. Power Connectors

When used with a power supply that supports remote power on/off, the motherboard can turn off the system power through software control.

Table 19. Primary and Secondary Power Supply Connectors

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PW_ON# (power supply remote on/off control)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	-5 V
9	+5 VSB	19	+5 V
10	+12 V	20	+5 V

Table 20. Power Connector

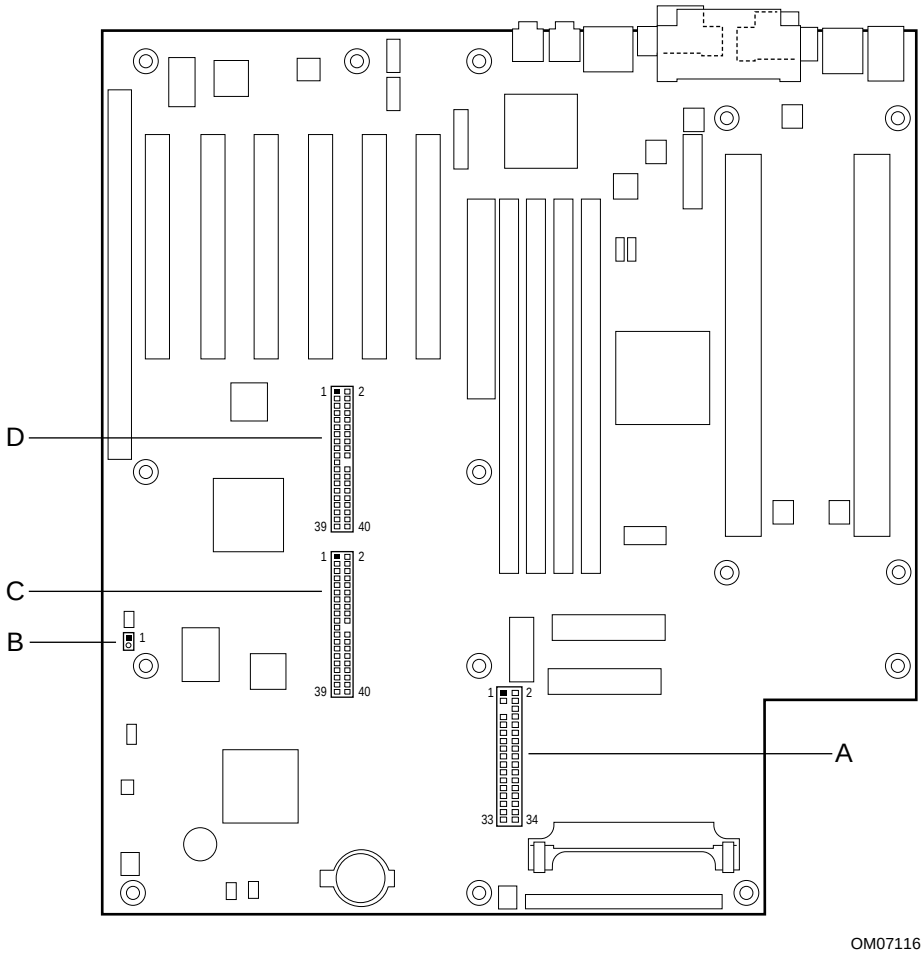
Pin	Signal Name
1	Ground
2	Ground
3	Ground
4	+3.3 V
5	+3.3 V
6	+5 V (Keyed)

Table 21. VRM Connector

Pin	Signal Name	Pin	Signal Name
1	5VIN	21	VSS
2	5VIN	22	VCC
3	5VIN	23	VCC
4	5VIN	24	VSS
5	5VIN	25	VSS
6	5VIN	26	VCC
7	12VIN	27	VCC
8	12VIN	28	VSS
9	12VIN	29	VSS
10	SENSE	30	VCC
11	No connect	31	VCC
12	OUTEN	32	VSS
13	VID0	33	VSS
14	VID1	34	VCC
15	VID2	35	VCC
16	VID3	36	VSS
17	VID4	37	VSS
18	PWRGOOD	38	VCC
19	VCC	39	VCC
20	VSS	40	VSS

1.10.2.5 Peripheral Interface Connectors

Figure 8 shows the location of the peripheral interface connectors. Tables 22 through 24 list the pinouts of the peripheral interface connectors.



A Diskette Drive
B SCSI LED
C Secondary IDE
D Primary IDE

Figure 8. Peripheral Interface Connectors

Table 22. SCSI LED Connector

Pin	Signal Name
1	SCSI_LED#
2	Ground

Table 23. Diskette Drive Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	TP_FLOPPY
5	Key	6	DRATE0
7	Ground	8	FDINDX# (Index)
9	N.C.	10	FDM00# (Motor Enable A)
11	Ground	12	FDDS1# (Drive Select B)
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	FDM01# (Motor Enable B)
17	MSEN1	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	WGATE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	MSEN0	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

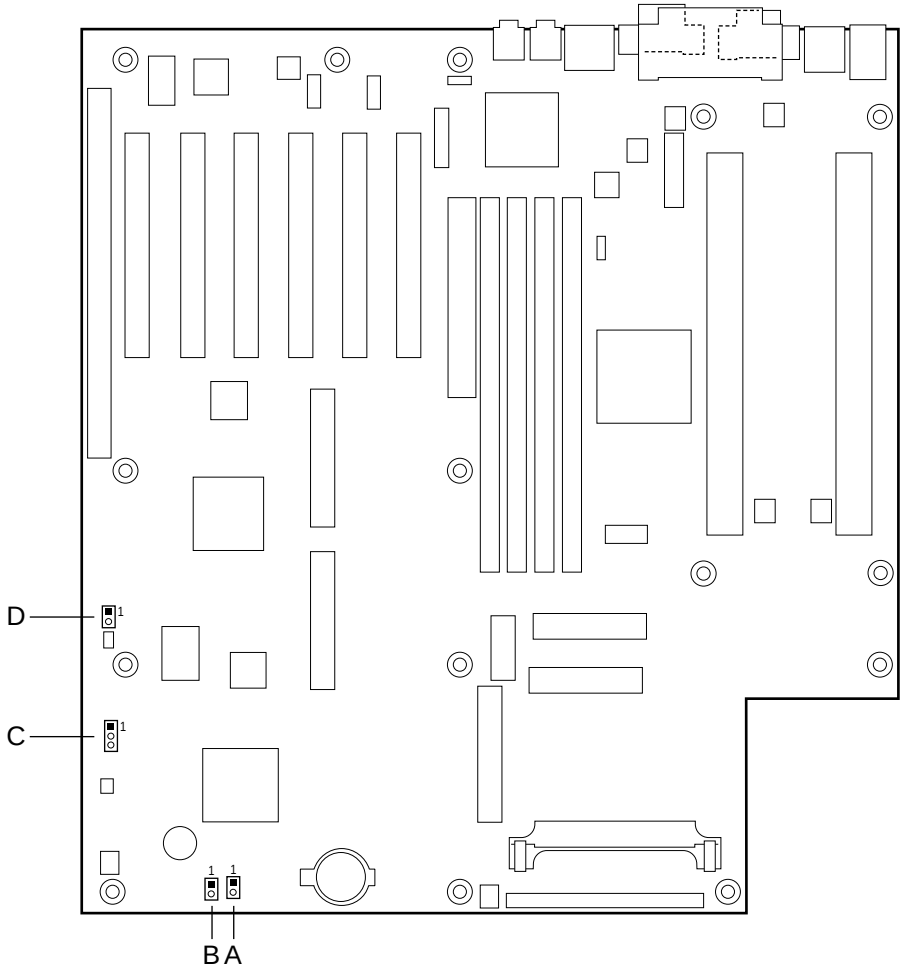
Table 24. IDE Connectors

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Ground
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	Address 1	34	Reserved
35	Address 0	36	Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

NOTE: Signal names in brackets ([ ]) are for the secondary IDE connector.

1.10.2.6 Security and Hardware Management Connectors

Figure 9 shows the security and hardware management connectors. Tables 25 through 27 list the pinouts of the security and hardware management connectors.



A Rear Chassis Intrusion
B Front Chassis Intrusion
C Wake on LAN technology connector
D Wake on Modem

Figure 9. Security and Hardware Management Connectors

Table 25. Front and Rear Chassis Intrusion Connectors

Pin	Signal Name
1	TAMPER_DETECT#
2	Ground

Table 26. Wake on LAN Technology Connector

Pin	Signal Name
1	AUX5
2	Ground
3	WOL_PIN3

Table 27. Wake-on-Modem Connector

Pin	Signal Name
1	Ground
2	MODEMRING #

1.10.2.6.1 Chassis Intrusion Connectors

The hardware monitor subsystem supports a chassis security feature that detects if the chassis cover is removed. When the chassis cover is removed, a signal is sent to the hardware monitor component. The chassis intrusion circuit is powered by either the chassis' power supply (when the computer is connected to AC power) or the battery (when the computer is not connected to AC power). The security feature uses mechanical switches on the chassis that are attached to the 1 x 2-pin chassis intrusion connectors. The switch contacts are open for normal computer operation. As a result, a normally-open switch should be used for chassis intrusion. When the chassis cover is removed, the switch contacts close and the circuit to ground is completed.

1.10.2.6.2 Wake on LAN Technology Connector

This connector supports the Wake on LAN technology feature. Attach this connector to a network interface card (NIC) that supports Wake on LAN technology. The NIC monitors network traffic. When the NIC detects a Magic Packet†, it asserts a signal through the Wake on LAN technology connector to wake up the computer. This signal can wake up the computer only when the power cord is still plugged into the socket and the computer is turned off. Wake on LAN can be enabled through the BIOS Setup program.

To enable Wake on LAN for an add-in NIC, disable the onboard LAN subsystem by moving the LAN enable/disable jumper to the disable position. See page 49 for more information on the LAN enable/disable jumper block.

NOTE

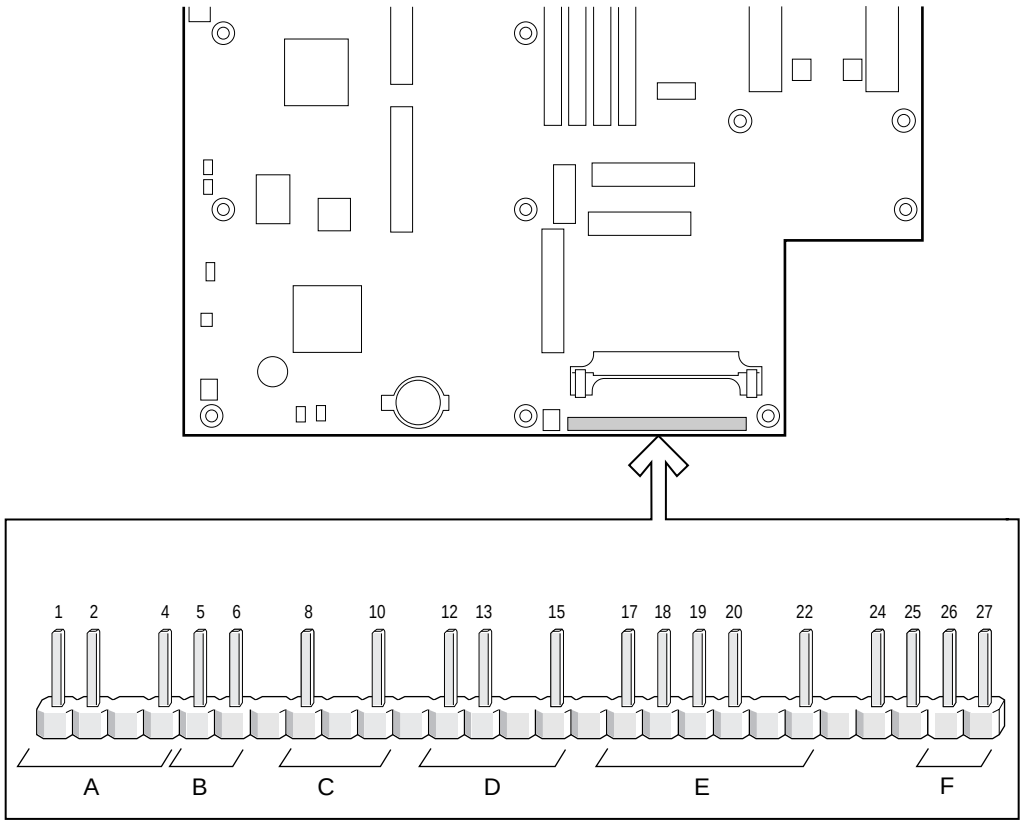
The computer's power supply must provide sufficient +5 VSB current to the NIC; without enough +5 VSB current, the Wake on LAN feature will not function and the motherboard may not boot. Check the NIC's documentation for its +5 VSB current requirements. See page 52 for information on the board's power requirements.

1.10.2.6.3 Wake on Modem

The Wake-on-Modem feature allows the computer to wake from Sleep mode when a call is received on a telephony device, such as a modem. The first incoming call will power up the motherboard, but a second call must be made to access the computer.

1.10.3 Front Panel Connectors

Figure 10 shows the location of the front panel connectors.



A	Speaker	D	Hard drive activity LED
B	Reset switch	E	Infrared port
C	Power/sleep LED	F	Power switch

Figure 10. Front Panel Connectors

Table 28. Front Panel Connectors

Connector	Pin	Signal Name
Speaker	1	BUZZER_B1
	2	BUZZER_A2
	3	Key
	4	+5 V
Reset Switch	5	FP_RESET#
	6	Ground
None	7	Key
Power/Sleep LED	8	YEL_BLNK#
	9	Key
	10	GREEN/YELLOW_INV
None	11	Key
Hard Drive Activity LED	12	+5 V
	13	DASDACTIVE#
	14	Key
	15	+5 V
None	16	Key
Infrared Port	17	IRLS1
	18	IRTX
	19	Ground
	20	IRRX
	21	Key
	22	+5 V
None	23	Key
	24	+5 V
	25	N.C.
Power Switch	26	Ground
	27	SWITCH

1.10.3.1 Speaker

The onboard piezoelectric speaker is enabled by a jumper on pins 1-2 of the front panel connector. The onboard speaker can be disabled by removing the jumper, and an offboard speaker can be connected in its place across pins 1 and 4. The speaker (onboard or offboard) provides error beep code information during the POST in the event that the computer cannot use the video interface. The speaker is not connected to the audio subsystem and does not receive output from the audio subsystem.

1.10.3.2 Reset Switch

These pins can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the motherboard resets and runs the POST.

1.10.3.3 Power/Sleep LED

These pins can be connected to a multicolor LED that lights when the computer is powered on or in sleep mode. The possible states for this LED are:

LED State	Indication
Off	Power off
Green	Power on
Yellow	Sleep

1.10.3.4 Hard Drive Activity LED

These pins can be connected to an LED to provide a visual indicator that data is being read from or written to an IDE or SCSI hard drive, as well as add-in cards that provide an activity signal. For the LED to function properly, the IDE drive must be connected to the onboard IDE controller. This LED will also show activity for devices connected to the hard drive LED header.

1.10.3.5 Infrared Port

Serial Port 2 can be configured to support an IrDA module connected to the front panel infrared connector. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptop computers, PDAs, and printers using application software.

1.10.3.6 Power Switch

These pins can be connected to a front panel power switch. Because of debounce circuitry on the motherboard, the switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. At least two seconds must pass before the power supply will recognize another on/off signal.

⚠ CAUTION

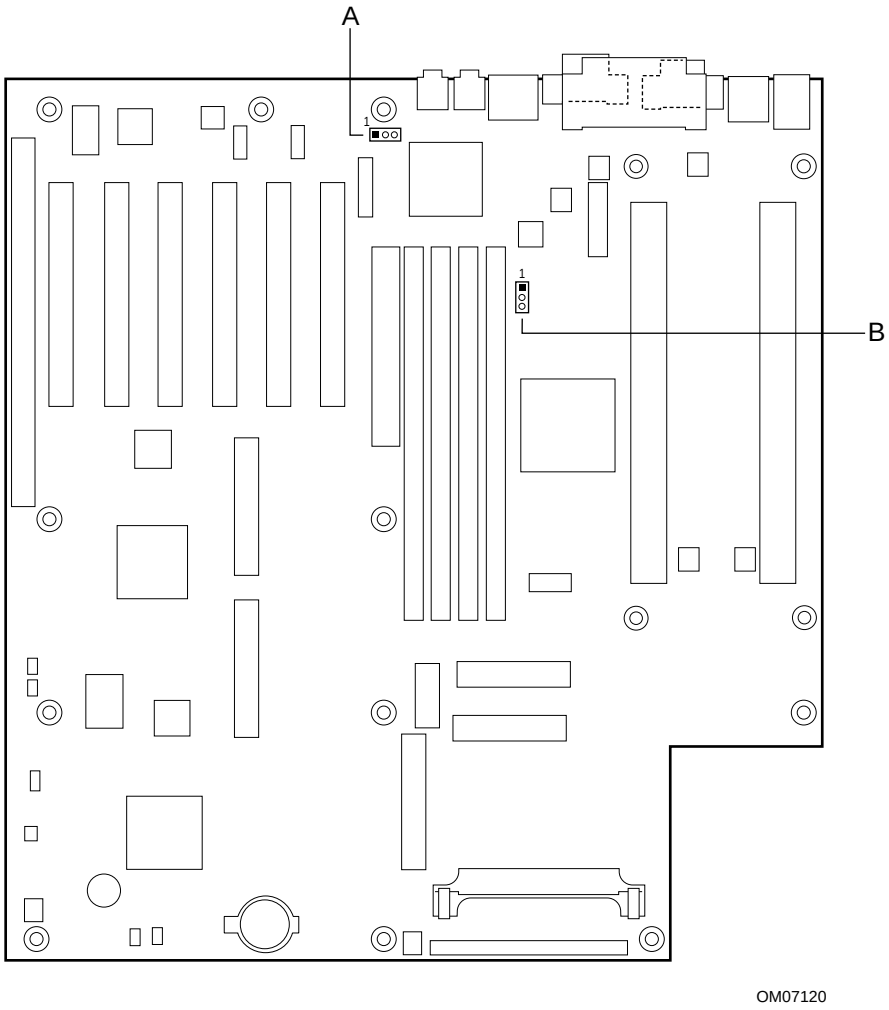
If you need to turn off the computer during POST, hold the power switch in for four seconds; otherwise the computer will not switch off.

1.11 Jumper Settings

CAUTION

Do not move jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumpers.

Figure 11 shows the location of the configuration jumper blocks.



A LAN enable/disable jumper block
B BIOS Setup configuration jumper block

Figure 11. Configuration Jumper Blocks

1.11.1 LAN Enable/Disable Jumper Block

The table below describes the settings of the LAN enable/disable jumper block. To enable the Wake on LAN feature for an add-in network interface card, disable the onboard LAN subsystem by moving the jumper to the disable position.

Table 29. LAN Enable/Disable Jumper Settings

Mode	Jumper Setting	Description
Enable	1-2	Enables the onboard LAN subsystem. (**Default**)
Disable	2-3	Disables the onboard LAN subsystem, which allows for the use of an add-in network interface card.

1.11.2 BIOS Setup Configuration Jumper Block

The table below describes the settings of the BIOS Setup configuration jumper block.

Table 30. BIOS Setup Configuration Jumper Settings

Mode	Jumper Setting	Description
Normal	1-2	The BIOS uses current configuration information and passwords for booting. (**Default**)
Configure	2-3	After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	Off (jumper removed)	The BIOS attempts to recover the BIOS from a diskette. A recovery diskette is required.

1.12 Mechanical Considerations

1.12.1 Custom Form Factor

The motherboard is designed to fit into a custom ATX form-factor chassis. Figure 12 shows the board mounting hole locations. The mounting holes closest to the Slot 2 connectors are used for mounting the processor retention mechanism to the board and chassis.

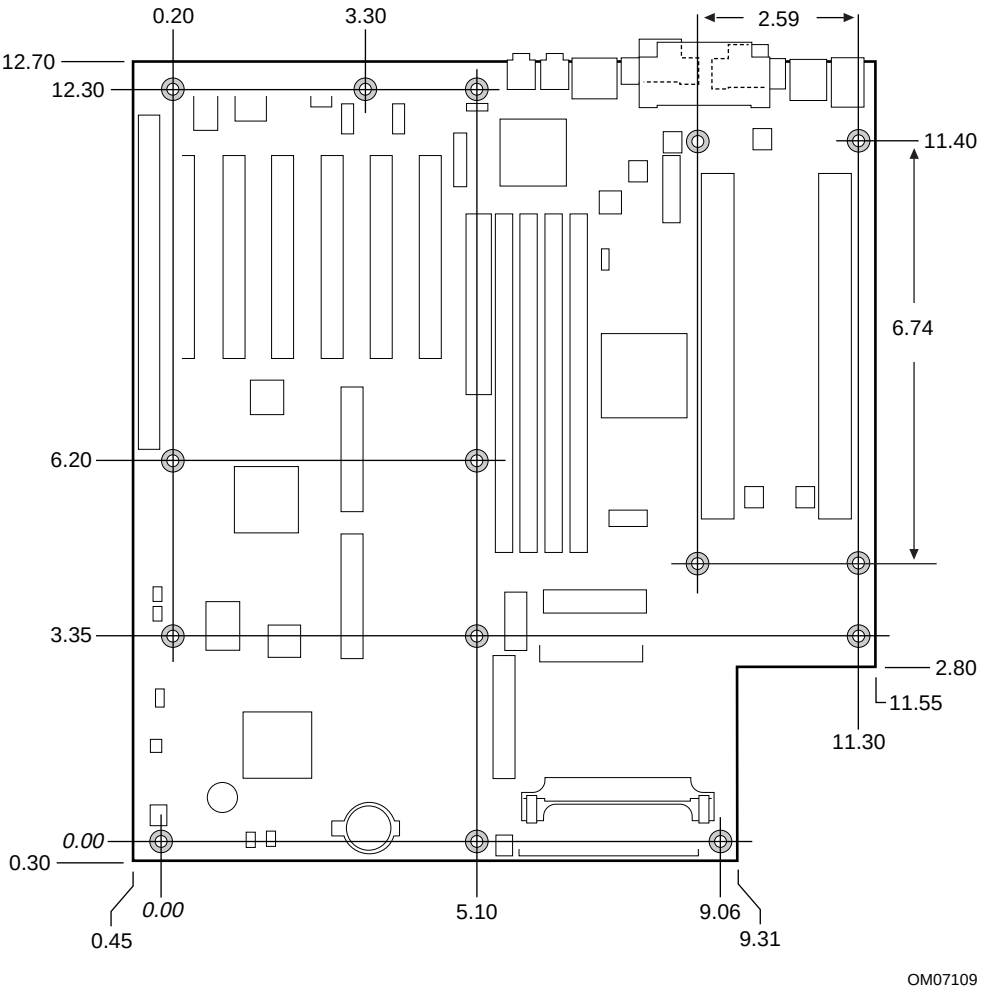


Figure 12. Motherboard Dimensions

1.12.2 I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements. Systems based on this motherboard need the back panel I/O shield to pass EMI compliance verification. Figure 13 shows the critical dimensions of a chassis-independent I/O shield.

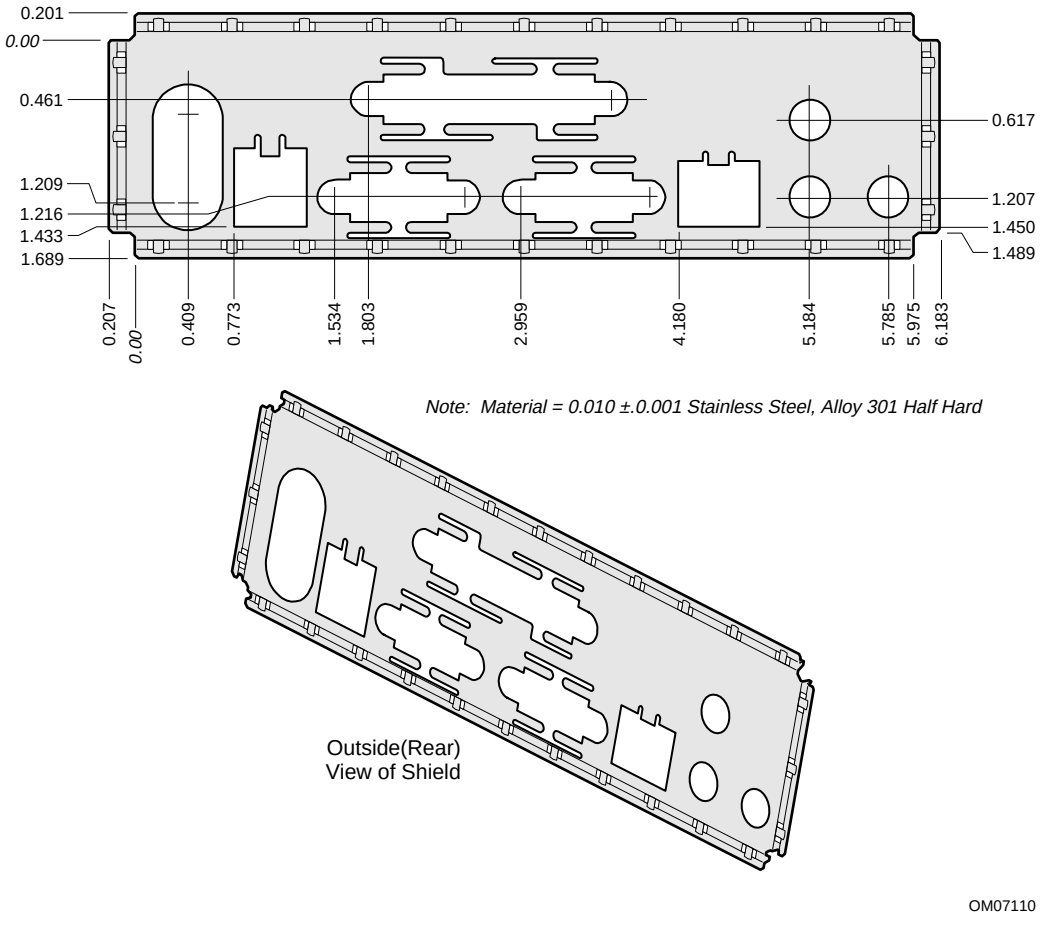


Figure 13. Back Panel I/O Shield Dimensions (ATX Chassis-Independent)

1.13 Electrical Considerations

1.13.1 Power Consumption

Table 31 lists the power specifications for a computer that contains a motherboard with two 400 MHz Pentium II Xeon processors, 128 MB SDRAM, a 3.5-inch diskette drive, a Western Digital Caviar 3320 3.3 GB Ultra ATA hard drive, a Hitachi CBR 8330 IDE CD-ROM, and a Diamond Viper 330 AGP graphics card. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 desktop mode are measured at 1280 x 1024 x 256 colors and 70 Hz refresh rate. AC watts are measured with a typical 300 W power supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 31. Power Usage

Mode	Watts (AC) Out of 110 VAC Wall Outlet
Windows 98 desktop	60
Windows NT 4.0 desktop	92

1.13.2 Power Supply Considerations

For typical configurations, the motherboard is designed to operate with at least a 300 W power supply. A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must comply with the following recommendations found in the *Intel Workstation Product Division 300 W Power Supply Design Guide*:

- The potential relation between 3.3 V DC and +5 V DC power rails
- The current capability of the +5 VSB line
- All timing parameters

See Section 6.2 for information on obtaining the power supply design guide. The power supply used with this motherboard should have these characteristics:

- Current ratings of:
  - 28.0 A on the 3.3 V DC power rail
  - 30.0 A on the 5 V DC power rail
  - 8.0 A on the +12 V DC power rail
  - 0.1 A on the -5 V DC power rail
  - 0.4 A on the -12 V DC power rail
  - 0.72 A on the +5 VSB power rail (1 A recommend)
- 3.3 VDC and +5 VDC maximum continuous output power of 220 W
- Total power output of 300 W

NOTE

Power supplies used with the MS440GX motherboard must meet UL SELV requirements and meet the 240 VA energy limit.

Table 32 lists the DC voltage tolerances and estimated current requirements for the motherboard. The values listed are for the motherboard and RAM only; they do not include PCI or AGP add-in cards.

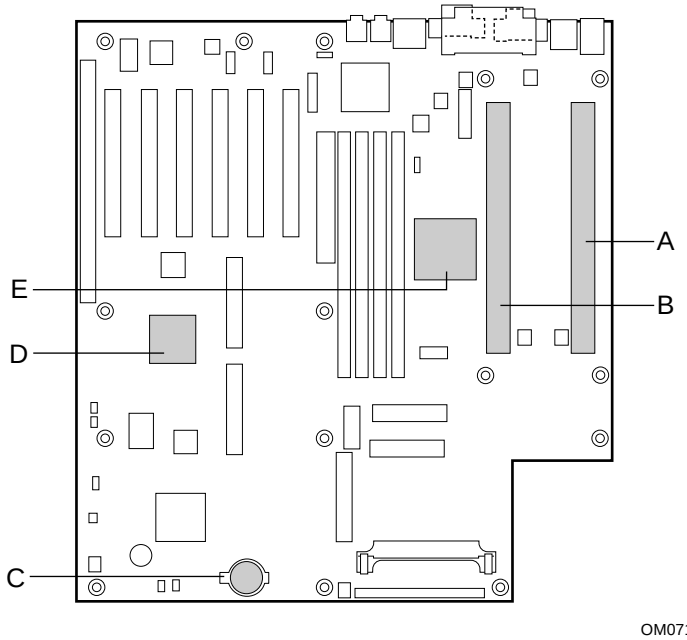
Table 32. DC Voltage Tolerances and Estimated Current Requirements

DC Voltage	Acceptable Tolerance	Estimated current with a 400-MHz processor, 512 KB cache, and 2 GB of RAM	Estimated current with a 450-MHz processor, 512 KB cache, and 2 GB of RAM
+3.3 V	± 5%	20 A	20 A
+5 V	± 5%	14 A	16 A
+5 VSB (standby)	± 5%	0.72 A	0.72 A
-5 V	± 10%	0.0 A	0.0 A
+12 V	± 5%	2.8 A	3.1 A
-12 V	± 10%	0.0 A	0.0 A

1.14 Thermal Considerations

Figure 14 shows the locations of the thermally-sensitive components.

Table 33 lists the maximum component case temperatures for motherboard components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.



A	Slot 2 (Application Processor)
B	Slot 2 (Boot Processor)
C	Battery Case
D	82371EB PIIX4E
E	82443GX PAC

Figure 14. Thermally Sensitive Components

⚠ CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C might cause components to exceed their maximum case temperature. For information about the maximum operating temperature, see the environmental specifications in Section 1.15. When determining system compliance, considerations should be given for maximum rated ambient temperatures.

Table 33. Thermal Considerations for Components

Component	Maximum Temperature
Pentium II Xeon processor	75 °C (thermal plate)
Intel 82443GX PAC	105 °C (case)
Intel 82371EB PIIX4E	85 °C (case)
Lithium battery	70 °C (case)
PWB substrate	105 °C

1.15 Environmental Specifications

Table 34. Environmental Specifications

Parameter	Specification		
Temperature			
Nonoperating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 G trapezoidal waveform		
	Velocity change of 170 inches/sec		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz : 0.02g² Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)		
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz		

1.16 Reliability Information

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991.

The MTBF prediction can be used when estimating repair rates and spare parts requirements.

MTBF data is calculated from predicted data @ 55 °C.

The MTBF prediction for the motherboard is 129,574 hours.

1.17 Regulatory Compliance

This motherboard complies with the following safety and EMC regulations when correctly installed in a compatible host system.

Table 35. Safety Regulations

Regulation	Title
UL 1950 - CSA 950-95, 3rd edition, Dated 07-28-95	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

Table 36. EMC Regulations

Regulation	Title
FCC Class A	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)

1.17.1 Product Certification Markings

This motherboard has the following product certification markings:

- European CE Marking: Consists of a marking on the board and/or the shipping container.
- UL Recognition Mark: Consists of the UL File No. E186194 and a stylized backward UR on component side of the board and the PB No. on the solder side of the board. Board material flammability is 94V-1 or -0.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of the board.

2 Resource Mapping

This chapter provides detailed technical information about onboard resources, presented in table format. The contents of the chapter include:

NOTE

For more detailed information about the resources used for onboard audio, see Section 1.7.

2.1 Memory Map

Table 37. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 2097152 K	100000 - 7FFFFFFF	2047 MB	Extended memory (SDRAM)
928 K - 1024 K	E8000 - FFFFF	96 KB	System BIOS
800 K - 928 K	C8000 - E7FFF	128 KB	Available high DOS memory (open to ISA and PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.2 DMA Channels

Table 38. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Audio
1	8 or 16 bits	Audio / parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP)/audio
4		Reserved - cascade channel
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.3 I/O Map

Table 39. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4E - DMA 1
0020 - 0021	2 bytes	PIIX4E - interrupt controller 1
002E - 002F	2 bytes	I/O controller configuration registers
0040 - 0043	4 bytes	PIIX4E - Counter/Timer 1
0048 - 004B	4 bytes	PIIX4E- Counter/Timer 2
0060	1 byte	Keyboard Controller Byte - Reset IRQ
0061	1 byte	PIIX4E - NMI, Speaker Control
0064	1 byte	Keyboard controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX4E - enable NMI
0070, bits 6:0	7 bits	PIIX4E - real time clock, address
0071	1 byte	PIIX4E - real time clock, data
0078	1 byte	Reserved - motherboard configuration
0079	1 byte	Reserved - motherboard configuration
0080 - 008F	16 bytes	PIIX4E - DMA page registers
00A0 - 00A1	2 bytes	PIIX4E - interrupt controller 2
00B2 - 00B3	2 bytes	APM control
00C0 - 00DE	31 bytes	PIIX4E - DMA 2
00F0	1 byte	Reset numeric error
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0200 - 0207	8 bytes	Audio / game port
0220 - 022F	16 bytes	Audio (Sound Blaster compatible)
0240 - 024F	16 bytes	Audio (Sound Blaster compatible)
0278 - 027F	8 bytes	LPT2
0290 - 0297	8 bytes	Hardware monitor
02E8 - 02EF	8 bytes	COM4/Video (8514A)
02F8 - 02FF	8 bytes	COM2
0300 - 0301	2 bytes	MPU-401 (MIDI)
0330 - 0331	2 bytes	MPU-401 (MIDI)
0332 - 0333	2 bytes	MPU-401 (MIDI)
0334 - 0335	2 bytes	MPU-401 (MIDI)
0376	1 byte	Secondary IDE channel command port
0377	1 byte	Floppy channel 2 command
0377, bit 7	1 bit	Floppy disk change, channel 2
0377, bits 6:0	7 bits	Secondary IDE channel status port

continued

Table 39. I/O Map (continued)

Address (hex)	Size	Description
0378 - 037F	8 bytes	LPT1
0388- 038D	6 bytes	AdLib (FM synthesizer)
03B4 - 03B5	2 bytes	Video (VGA†)
03BA	1 byte	Video (VGA)
03BC - 03BF	4 bytes	LPT3
03C0 - 03CA	11 bytes	Video (VGA)
03CC	1 byte	Video (VGA)
03CE - 03CF	2 bytes	Video (VGA)
03D4 - 03D5	2 bytes	Video (VGA)
03DA	1 byte	Video (VGA)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Floppy channel 1 command
03F7, bit 7	1 bit	Floppy disk change channel 1
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0530 - 0537	8 bytes	Windows Sound System
0604 - 060B	8 bytes	Windows Sound System
LPTn + 400h	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB*	4 bytes	PCI configuration address register
0CF9**	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
0E80 - 0E87	8 bytes	Windows Sound System
0F40- 0F47	8 bytes	Windows Sound System
0FF0 - 0FF7	8 bytes	CS4235 audio control
FF00 - FF07	8 bytes	IDE bus master register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers
007C, bits 5:4	2 bits	Chassis fan RPM sense selection

* DWORD access only

** Byte access only

2.4 Interrupts

Table 40. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option) / audio / user available / shared
6	Diskette drive
7	LPT1* / shared
8	Real time clock
9	Windows Sound System* / shared
10	LAN / shared
11	User available / shared
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.5 PCI Configuration Space Map

Table 41. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82443GX PAC
01	00	00	Intel 82443GX PCI-to-PCI bridge (for AGP)
00	0C	00	Intel 82371EB PIIX4E PCI/ISA bridge
00	0C	01	Intel 82371EB PIIX4E IDE bus master
00	0C	02	Intel 82371EB PIIX4E USB
00	0C	03	Intel 82371EB PIIX4E power management
00	02	00	Intel 82558 PCI LAN controller
00	0D	00 *	PCI expansion slot 1
00	0E	00 *	PCI expansion slot 2
00	0F	00 *	PCI expansion slot 3
00	10	00 *	PCI expansion slot 4
00	11	00 *	PCI expansion slot 5
00	12	00 *	PCI expansion slot 6

* Function numbers depend on the add-in card used. (Typical card = 00)

2.6 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and, therefore, share the same interrupt. Table 42 lists the PIRQ signals and shows how the signals are connected to the PCI expansion slots and to onboard PCI interrupt sources.

Table 42. PCI Interrupt Routing Map

PIIX4E PIRQ Signal	PCI Slot 1	PCI Slot 2	PCI Slot 3	PCI Slot 4	PCI Slot 5	PCI Slot 6	AGP	PCI LAN	Power Management
PIRQA	INTA	INTD	INTC	INTB	INTA	INTD	INTA		X
PIRQB	INTB	INTA	INTD	INTC	INTB	INTA	INTB		
PIRQC	INTC	INTB	INTA	INTD	INTC	INTB		X	
PIRQD	INTD	INTC	INTB	INTA	INTD	INTC			

For example, assume an add-in card has one interrupt (group INTA) and is plugged into the second PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQB signal, which is not connected to any onboard interrupt sources. If there are no other add-in cards, this card does not share its interrupt with any other devices.

Now, however, plug a second add-in card that has two interrupts (group INTA and INTB) into the first PCI slot. INTA in the first slot is connected to signal PIRQA and INTB is connected to signal PIRQB. Therefore, the second device on the two-function add-in card in the first slot will share its interrupt with the single-function card in the second slot.

NOTE

The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 12, 14, or 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. In the presence of an SMP operating system, the IOAPIC is used instead of the PIIX4E to distribute interrupts.

3 Overview of BIOS Features

This chapter describes the features supported by BIOS Setup program. The contents of the chapter include:

The motherboard uses an Intel/Phoenix BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the Setup program, Power-On Self Test (POST), Advanced Power Management (APM), the PCI auto-configuration utility, and Windows 98-ready Plug and Play code.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and the revision code. The initial production BIOS is identified as 4M4SG0X0.86E.

3.1 BIOS Upgrades

The BIOS can be upgraded from a diskette using the Intel Flash Memory Update utility that is available from Intel. This utility does BIOS upgrades as follows:

- Updates the flash BIOS from a file on a disk
- Updates the language section of the BIOS
- Makes sure that the upgrade BIOS matches the target system to prevent accidentally installing a BIOS for a different type of system.

BIOS upgrades and the update utility are available from Intel through the Intel World Wide Web site. See Section 6.1 for information about this site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

3.2 BIOS Flash Memory Organization

The Intel E28F004BXT80 4-Mbit flash component is organized as 512 KB x 8 bits and is divided into areas as described in Table 43. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

Table 43. Flash Memory Organization

Address (Hex)	Size	Description
FFFFC000 - FFFFFFFF	16 KB	Boot Block
FFFFA000 - FFFFBFFF	8 KB	Vital Product Data (VPD) Extended System Configuration Data (ESCD) (DMI configuration data / Plug and Play data)
FFFF9000 - FFFF9FFF	4 KB	Used by BIOS (e.g., for Event Logging)
FFFF8000 - FFFF8FFF	4 KB	OEM logo or Scan Flash Area
FFF80000 - FFFF7FFF	480 KB	Main BIOS Block

3.3 Plug and Play: PCI Autoconfiguration

The BIOS can be set to automatically configure PCI devices and Plug and Play devices. PCI devices may be onboard or add-in cards. Plug and Play devices are ISA add-in cards built to meet the Plug and Play specification. Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system. When a user turns on the system after adding a PCI or Plug and Play card, the BIOS can automatically configure interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is dependent upon a number of factors including type and number of add-in cards, slot selection, and operating system. Any change to the hardware or system software configuration can cause a change to the interrupt configuration of existing devices. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device. Autoconfiguration information is stored in the extended system configuration data (ESCD) format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2. Copies of the specifications can be obtained from the Intel World Wide Web site (see Section 6.1).

3.4 PCI IDE Support

If Auto is selected as a primary or secondary IDE device (see Section 4.3) in Setup, the BIOS automatically sets up the two local-bus IDE connectors with independent I/O channel support. The IDE interface supports PIO Mode 3, PIO Mode 4, and Ultra DMA hard drives and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and LS-120 diskette drives (see Section 6.2 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them so as to optimize capacity and performance. To take advantage of the high-capacity storage devices, hard drives are automatically configured for logical block addressing (LBA) and to PIO Mode 3, PIO Mode 4, or Ultra DMA depending on the capability of the drive. To override the autoconfiguration options, use the specific IDE device options in Setup. The ATAPI specification recommends that ATAPI devices be configured as shown in Table 44.

Table 44. Recommendations for Configuring an ATAPI Device

	Primary Cable		Secondary Cable	
Configuration	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE system with only one cable	ATA	ATAPI		
Enhanced IDE with CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

3.5 ISA Plug and Play

If Plug & Play O/S (see Section 4.3) is selected in Setup, the BIOS autoconfigures only ISA Plug and Play and PCI cards that are required for booting (IPL devices). If Plug & Play O/S is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA and PCI cards.

NOTE

With Plug & Play O/S selected in Setup, PCI or PnP add-in cards that are not required for booting will not be available unless they are initialized and assigned resources by the operating system or other program.

3.6 ISA Legacy Devices

Since ISA legacy devices are not autoconfigurable, the resources for them must be reserved. Resources can be reserved in the Setup program or with an ISA configuration utility. The ISA configuration utility can be downloaded from the Intel World Wide Web site (see Section 6.1).

3.7 Desktop Management Interface (DMI)

DMI is an interface for managing computers in an enterprise environment. The main component of DMI is the management information format (MIF) database, which contains information about the computing system and its components. Using DMI, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel LANDesk Client Manager to use DMI. The BIOS stores and reports the following DMI information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

OEMs can use a utility that programs flash memory so the BIOS can report on system and chassis information. This utility is available through Intel sales offices. See Section 6.1 for information about contacting a local Intel sales office. See Section 6.2 for information about the latest DMI specification.

DMI does not work directly under non-Plug and Play operating systems (e.g., Windows NT 4.0). However, the BIOS supports a DMI table interface for such operating systems. Using this support, a DMI service-level application running on a non-Plug and Play operating systems can access the DMI BIOS information.

3.8 APM

The BIOS supports APM and standby mode. See Section 6.2 for the version of the APM specification that is supported. The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in Setup
- From the operating system, such as the Suspend menu item in Windows 98

In standby mode, the motherboard reduces power consumption by using SMM capabilities, spinning down hard drives, and reducing power to or turning off VESA† DPMS-compliant monitors. Power-management mode can be enabled or disabled in Setup (see Section 4.5).

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 98 supports the power-management features upon detecting that APM is enabled in the BIOS.

3.9 Advanced Configuration and Power Interface (ACPI)

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. ACPI requires an ACPI-aware operating system. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM functionality normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 46)
- Support for a front panel power and sleep mode switch. Table 45 describes the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system

Table 45. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off	Less than four seconds	Power on
On	Less than four seconds	Soft off/Suspend
On	More than four seconds	Fail safe power off
Sleep	Less than four seconds	Wake up

3.9.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

3.9.2 Wake Up Devices and Events

The table below describes which devices or specific events can wake the computer from specific states. Sleeping states S4BIOS and S5 are the same for the wake up events.

Table 46. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S4BIOS, S5
RTC alarm	S1, S4BIOS, S5
LAN	S1, S4BIOS, S5
Modem	S1, S4BIOS, S5
IR command	S1
USB	S1
PS/2 keyboard	S1
PS/2 mouse	S1
Sleep button	S1

3.9.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure motherboard devices that do not have other hardware standards for enumeration and configuration. PCI devices on the motherboard, for example, are not enumerated by ACPI.

3.9.4 BIOS Support

The BIOS supports both APM and ACPI. If the board is used with an ACPI-aware operating, the BIOS provides ACPI support. Otherwise, it defaults to APM support.

3.10 Language Support

Five languages are available: American English, German, Italian, French, and Spanish. The default language is American English, which is present unless another language is programmed into the BIOS using the flash memory update utility. See Section 3.1 for information about the BIOS update utility.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.11 Boot Options

In the Setup program, the user can choose to boot from a diskette drive, hard drive, CD-ROM, or the network. The default setting is for the diskette drive to be the primary boot device and the hard drive to be the secondary boot device. By default the third and fourth devices are disabled.

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. See Section 6.2 for information about the El Torito specification. Under the Boot menu in the Setup program, CD-ROM is listed as a boot device. Boot devices are defined in priority order.

The network can be selected as a boot device. This selection allows booting from a network add-in card with a remote boot ROM installed. The LANDesk Service Agent can be used to perform service boots if the network is equipped with a suitable LANDesk Configuration Manager server.

3.12 OEM Logo or Scan Area

A 4 KB flash-memory user area at memory location FFFF8000h-FFFF8FFFh is for displaying a custom OEM logo during POST. A utility is available from Intel to assist with installing a logo into the flash memory. Contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

3.13 USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place. By default, USB legacy support is disabled. USB legacy support is only intended to be used in accessing BIOS Setup and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in Setup).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized. After the operating system loads the USB drivers, the USB devices are recognized.

To install an operating system that supports USB, enable USB Legacy support in BIOS Setup and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers configured, USB legacy support is no longer used. USB Legacy Support can be left enabled in BIOS Setup if needed.

Notes on using USB legacy support:

- If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice. For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non USB operating system.
- USB legacy support is for keyboards and mice only. Hubs and other USB devices are not supported.

3.14 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. An administrator password and a user password can be set for the Setup program and for booting the computer, with the following restrictions:

- The administrator password gives unrestricted access to view and change all the Setup options in the Setup program. This is administrator mode.
- The user password gives restricted access to view and change Setup options in the Setup program. This is user mode.
- If only the administrator password is set, pressing the <Enter> key at the password prompt of the Setup program allows the user restricted access to Setup.
- If both the administrator and user passwords are set, users can enter either the administrator password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the administrator password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 47 shows the effects of setting the administrator password and user password. This table is for reference only and is not displayed on the screen.

Table 47. Administrator and User Password Functions

Password Set	Administrator Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Administrator only	Can change all options	Can change a limited number of options	Administrator Password	Administrator	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Administrator and user set	Can change all options	Can change a limited number of options	Administrator Password Enter Password	Administrator or user	Administrator or user

* If no password is set, any user can change all Setup options.

See Section 4.4 for information about setting user and administrator passwords.

3.15 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the recovery mode (see Section 1.11.2, beginning on page 49).

To create a BIOS recovery diskette, a bootable diskette must be created and the recovery files copied to it. The recovery files are available from Intel, contact Intel customer support for further information. See Section 6.1 for information on contacting Intel customer support.

NOTE

If the computer is configured to boot from an LS-120 diskette (see Section 4.6), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

4 BIOS Setup Program

This chapter provides a detailed description of the BIOS Setup program's screens. The contents of this chapter include:

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 48 shows the menus available from the menu bar at the top of the Setup screen.

Table 48. Setup Menu Bar

Setup Menu Screen	Description
Maintenance	Specifies the processor speed and clears the Setup passwords. This menu is only available in configure mode. Refer to Section 1.11, beginning on page 48 for information about configure mode.
Main	Allocates resources for hardware components.
Advanced	Specifies advanced features available through the chipset.
Security	Specifies passwords and security features.
Power	Specifies power management features.
Boot	Specifies boot options and power supply controls.
Exit	Saves or discards changes to the Setup program options.

Table 49 shows the function keys available for menu screens.

Table 49. Setup Function Keys

Setup Key	Description
<F1> or <Alt-H>	Brings up a help screen for the current item.
<Esc>	Exits the menu.
<←> or <→>	Selects a different menu screen.
<↑> or <↓>	Moves cursor up or down.
<Home> or <End>	Moves cursor to top or bottom of the window.
<PgUp> or <PgDn>	Moves cursor to top or bottom of the window.
<F5> or <->	Selects the previous value for a field.
<F6> or <+> or <Space>	Selects the next value for a field.
<F9>	Load the default configuration values for the current menu.
<F10>	Save the current values and exit Setup.
<Enter>	Executes command or selects the submenu.
<+> or <->	Moves a device or class of devices up or down in the boot order.

4.1 Maintenance Menu

This menu is for setting the processor speed and clearing the Setup passwords. Setup only displays this menu in configure mode. See Section 1.11, beginning on page 48 for information about entering configure mode.

Table 50. Maintenance Menu

Feature	Options	Description
Processor Speed	• 300 MHz • 350 MHz • 400 MHz • 450 MHz • 500 MHz	Specifies the processor speed in megahertz.
Clear All Passwords	No options	Clears the user and administrator passwords.

4.2 Main Menu

This menu reports processor and memory information and is for configuring the system date, system time, floppy options, and IDE devices.

Table 51. Main Menu

Feature	Options	Description
Processor 0 Type	No options	Displays processor type.
Processor 1 Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
Cache RAM	No options	Displays size of second-level cache.
System Memory	No options	Displays the total amount of RAM on the motherboard.
Memory Bank 0 Memory Bank 1 Memory Bank 2 Memory Bank 3	No options	Specifies size and type of DIMMs installed in the respective banks.
Language	English (US)	Selects the language used by the BIOS.
ECC Configuration	• **Non-ECC (default)** • ECC	Specifies the ECC memory configuration.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.
Primary IDE Slave, submenu	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master, submenu	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave, submenu	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.3 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

Table 52. Advanced Menu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if a Plug and Play operating system is being used. No lets the BIOS configure all devices and steers SCI to INT20 of the IOAPIC. Yes lets the operating system configure Plug and Play devices and steers SCI to INT9 of the IOAPIC. Not required with a Plug and Play operating system.
Reset Configuration Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• **Auto (default)** • On • Off	Specifies the power on state of the Numlock feature on the numeric keypad of the keyboard.
Fan Monitoring	• **Fan 4 - J8L1 (default)** • Fan 3 - J8M1 and J13A1 • Fan 2 - J2L1 and J14G1 • Fan 1 - J2K1 and J3J1	Sets which fan header is monitored.
Power LED Type	• **Single Color (default)** • Dual Color	Set this option based on what type of LED is used for a power LED in your chassis. A single color LED is typically green or off. A dual color LED can be green, yellow, or off. A single color LED will blink during Suspend, whereas a dual color LED will turn yellow.
Peripheral Configuration, submenu	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration, submenu	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Floppy Options, submenu	No options	When selected, displays the Floppy Options submenu.
DMI Event Logging, submenu	No options	Configures DMI Events Logging. When selected, displays the DMI Events Logging submenu.
Video Configuration, submenu	No options	Configures video features. When selected, displays the Video Configuration submenu.

4.3.1 Peripheral Configuration Submenu

This submenu is for configuring the computer peripherals.

Table 53. Peripheral Configuration Submenu

Feature	Options	Description
Serial port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. Auto assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Serial port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. Auto assigns the first free COM port, normally COM2, the address 2F8h, and the interrupt IRQ3. An * (asterisk) displayed next to an address indicates a conflict with another device. If either serial port address is set, that address will not appear in the list of options for the other serial port.
Mode	• **Normal (default)** • IrDA • ASK-IR	Selects the mode for serial port B.
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. Auto assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • Bi-directional • EPP • **ECP (default)**	Selects the mode for the parallel port. Output Only operates in AT† -compatible mode. Bi-directional operates in bidirectional PS/2-compatible mode. EPP is Extended Parallel Port mode, a high-speed bidirectional mode. ECP is Enhanced Capabilities Port mode, a high-speed bidirectional mode.
Audio	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN	• Disabled • **Enabled (default)**	Enables or disables the LAN.
Embedded PXE Support	• Disabled • **Enabled (default)**	Enables or disables the embedded PXE support.
Legacy USB Support	• **Disabled (default)** • Enabled	Enables or disables support for legacy universal serial bus.

4.3.2 IDE Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

Table 54. IDE Configuration Submenus

Feature	Options	Description
IDE controller	• Disabled • Primary • Secondary • **Both (default)**	Configures the IDE controller. Both specifies both the primary and secondary the primary and secondary channel are used.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk pre-delay value.
Type	• None • ATAPI Removable • CD-ROM • IDE Removable • Other ATAPI • User • **Auto (default)**	Specifies the IDE configuration mode for IDE devices. IDE Removable allows the cylinders, heads, and sectors fields to be changed. Auto automatically fills in the values for the cylinders, heads, and sectors fields.
Cylinders	1 to *XXXX*	Specifies number of disk cylinders.
Heads	1 to 16	Specifies number of disk heads.
Sectors	1 to 64	Specifies number of disk sectors.
Maximum Capacity	No options	Reports the maximum capacity for the hard disk. Value calculated from number of cylinders, heads, and sectors.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard drive to memory. Check the hard drive's specifications for optimum setting.

continued

Table 54. IDE Configuration Submenu (continued)

Feature	Options	Description
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables logical block addressing (LBA) in place of the Cylinders, Heads, and Sectors fields. ⚠ **CAUTION** *Changing the LBA Mode Control after a hard drive has been formatted can corrupt data on the drive.*
Transfer Mode	• Standard • Fast PIO 1 • Fast PIO 2 • Fast PIO 3 • Fast PIO 4 • **FPIO 3 / DMA 1 (default)** • FPIO 4 / DMA 2	Specifies method for transferring data between the hard drive and system memory.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2	Specifies the ultra DMA mode for the hard drive.

4.3.3 Floppy Options Submenu

This submenu is for configuring diskette drives.

Table 55. Floppy Options Submenu

Feature	Options	Description
Floppy disk controller	• Disabled • **Enabled (default)**	Configures the diskette drive controller.
Diskette A:	• Disabled • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • **1.44/1.25 MB, 3½″ (default)** • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive A.
Diskette B:	• **Disabled (default)** • 360 KB, 5¼″ • 1.2 MB, 5¼″ • 720 KB, 3½″ • 1.44/1.25 MB, 3½″ • 2.88 MB, 3½″	Specifies the capacity and physical size of diskette drive B.
Floppy Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protect for the diskette drive(s).

4.3.4 DMI Event Logging Submenu

This submenu is for configuring the DMI event logging features.

Table 56. DMI Event Logging Submenu

Feature	Options	Description
Event log capacity	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View DMI event log	No options	Enables viewing of DMI event log.
Clear all DMI event logs	• **No (default)** • Yes	Clears the DMI Event Log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of DMI events.
ECC Event Logging	• Disabled • **Enabled (default)**	Enables logging of ECC events.
Mark DMI events as read	No options	Marks all DMI events as read.

4.3.5 Video Configuration Submenu

This submenu is for configuring video features.

Table 57. Video Configuration Submenu

Feature	Options	Description
Palette Snooping	• **Disabled (default)** • Enabled	Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card.

4.4 Security Menu

This menu is for setting passwords and security features.

Table 58. Security Menu

Feature	Options	Description
User Password Is	No options	Reports if there is a user password set.
Administrator Password Is	No options	Reports if there is an administrator password set.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Set Administrative Password	Password can be up to seven alphanumeric characters.	Specifies the administrator password.
Clear User Password	No options	Pressing <Enter> clears the user password.
User Setup Access	• None • **View Only (default)** • Limited Access • Full	Enables or disables user access to the Setup program.
Unattended Start	• **Disabled (default)** • Enabled	Enables the unattended start feature. When enabled, the computer boots, but the keyboard is locked. The user must enter a password to unlock the computer or boot from a diskette.

4.5 Power Menu

This menu is for setting power management features.

Table 59. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Inactivity Timer	• **Off (default)** • 1 Minute • 5 Minutes • 10 Minutes • 20 Minutes • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby and suspend modes.
VESA Video Power Down	• Disabled • **Enabled (default)**	Enables power management for video during standby and suspend modes.
Fan Always On	• No (default) • Yes	“Yes” forces the fan to remain on when the system is in a power-managed state.

4.6 Boot Menu

This menu is for setting the boot features and the boot sequence.

Table 60. Boot Menu

Feature	Options	Description
Quick Boot Mode	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stay Off • **Last State (default)** • Power On	Specifies how the computer responds following a power failure. Stay Off keeps power off until power button pressed. Last State restores previous power state before a power failure. Power On restores power without restoring previous power state.
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.
On Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off.
On PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PCI power management enable event when the power is off.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device Fifth Boot Device	• Removable devices • Hard Drive • ATAPI CD-ROM Drive • Network boot • LANDesk Service Agent	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering.
Hard Drive, submenu	No options	Lists available hard drives. When selected, displays the Hard Drive submenu.
Removable Devices, submenu	No options	Lists available removable devices. When selected, displays the Removable Devices submenu.

4.6.1 Hard Drive Submenu

This submenu is for configuring the boot sequence for hard drives.

Table 61. Hard Drive Submenu

Options	Description
• Installed hard drive • Bootable ISA Cards	Specifies the boot sequence for the hard drives attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.6.2 Removable Devices Submenu

This submenu is for configuring the boot sequence for removable devices.

Table 62. Removable Devices Submenu

Options	Description
• Legacy Floppy Drives	Specifies the boot sequence for the removable devices attached to the computer. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <+> to move the device up the list or <-> to move the device down the list. The operating system assigns a drive letter to each device in the order listed. Changing the order of the devices changes the drive lettering.

4.7 Exit Menu

This menu is for exiting the Setup program, saving changes, and loading and saving defaults.

Table 63. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS RAM.
Exit Discarding Changes	Exits without saving any changes made in Setup.
Load Setup Defaults	Loads the default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

This chapter lists the BIOS error messages, POST codes, and beep codes. The contents of this chapter include:

5.1 BIOS Error Messages

Table 64. BIOS Error Messages

Error Message	Explanation
Diskette drive A error or Diskette drive B error	Drive A or B is present but fails the POST diskette tests. Check that the drive is defined with the proper diskette type in Setup and that the diskette drive is installed correctly.
Extended RAM Failed at offset: *nnnn*	Extended memory not working or not configured properly at offset *nnnn*.
Failing Bits: *nnnn*	The number *nnnn* is a map of the bits at the RAM address (System, Extended, or Shadow memory) that failed the memory test. Each 1 in the map indicates a failed bit.
Fixed Disk 0 Failure or Fixed Disk 1 Failure or Fixed Disk Controller Failure	Fixed disk is not working or not configured properly. Check to see if fixed disk is installed properly. Run Setup be sure the fixed-disk type is correctly identified.
Incorrect Drive A type - run SETUP	Type of diskette drive for drive A not correctly identified in Setup.
Incorrect Drive B type - run SETUP	Type of diskette drive for drive B not correctly identified in Setup.
Invalid NVRAM media type	Problem with NVRAM (CMOS) access.
Keyboard controller error	The keyboard controller failed test. Try replacing the keyboard.
Keyboard error	Keyboard not working.
Keyboard error *nn*	BIOS discovered a stuck key and displays the scan code *nn* for the stuck key.
Keyboard locked - Unlock key switch	Unlock the system to proceed.
Monitor type does not match CMOS - Run SETUP	Monitor type not correctly identified in Setup.
Operating system not found	Operating system cannot be located on either drive A or drive C. Enter Setup and see if fixed disk and drive A are properly identified.
Parity Check 1	Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.

continued

Table 64. BIOS Error Messages (continued)

Error Message	Explanation
Parity Check 2	Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.
Press <F1> to resume, <F2> to Setup	Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change any settings.
Real time clock error	Real-time clock fails BIOS test. May require motherboard repair.
Shadow RAM Failed at offset: *nnnn*	Shadow RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System battery is dead - Replace and run SETUP	The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.
System cache error - Cache disabled	RAM cache failed the BIOS test. BIOS disabled the cache.
System CMOS checksum bad - run SETUP	System CMOS RAM has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. Run Setup and reconfigure the system either by getting the default values and/or making your own selections.
System RAM Failed at offset: *nnnn*	System RAM failed at offset *nnnn* of the 64 KB block at which the error was detected.
System timer error	The timer test failed. Requires repair of system motherboard.

Nnnn = hexadecimal numbers

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following table provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 65. Port 80h Codes

Code	Description of POST Operation
02h	Verify real mode
03h	Disable non-maskable interrupt (NMI)
04h	Get processor type
06h	Initialize system hardware
08h	Initialize chipset with initial POST values
09h	Set IN POST flag
0Ah	Initialize CPU registers
0Bh	Enable CPU cache
0Ch	Initialize caches to initial POST values
0Eh	Initialize I/O component
0Fh	Initialize the local bus IDE
10h	Initialize power management
11h	Load alternate registers with initial POST *valuesnew*
12h	Restore CPU control word during warm boot
13h	Initialize PCI bus mastering devices
14h	Initialize keyboard controller
16h	BIOS ROM checksum
17h	Initialize cache before memory autosize
18h	8254 timer initialization
1Ah	8237 DMA controller initialization
1Ch	Reset programmable interrupt controller
20h	Test DRAM refresh
22h	Test keyboard controller
24h	Set ES segment register to 4 GB
26h	Enable A20 line
28h	Autosize DRAM
29h	Initialize POST memory manager

continued

Table 65. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
2Ah	Clear 512 KB base RAM
2Ch	RAM failure on address line *nnnn*
2Eh	RAM failure on data bits *nnnn* of low byte of memory bus
2Fh	Enable cache before system BIOS shadow
30h	RAM failure on data bits *nnnn* of high byte of memory bus
32h	Test CPU bus-clock frequency
33h	Initialize POST dispatch manager
34h	Test CMOS RAM
35h	Initialize alternate chipset registers
36h	Warm start shut down
37h	Reinitialize the chipset (MB only)
38h	Shadow system BIOS ROM
39h	Reinitialize the cache (MB only)
3Ah	Autosize cache
3Ch	Configure advanced chipset registers
3Dh	Load alternate registers with CMOS *valuesnew*
40h	Set Initial CPU speed new
42h	Initialize interrupt vectors
44h	Initialize BIOS interrupts
45h	POST device initialization
46h	Check ROM copyright notice
47h	Initialize manager for PCI option ROMs
48h	Check video configuration against CMOS RAM data
49h	Initialize PCI bus and devices
4Ah	Initialize all video adapters in system
4Bh	Display QuietBoot screen
4Ch	Shadow video BIOS ROM
4Eh	Display BIOS copyright notice
50h	Display CPU type and speed
51h	Initialize EISA motherboard
52h	Test keyboard
54h	Set key click if enabled
56h	Enable keyboard
58h	Test for unexpected interrupts
59h	Initialize POST display service
5Ah	Display prompt “Press F2 to enter SETUP”
5Bh	Disable CPU cache

continued

Table 65. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
5Ch	Test RAM between 512 and 640 KB
60h	Test extended memory
62h	Test extended memory address lines
64h	Jump to UserPatch1
66h	Configure advanced cache registers
67h	Initialize multiprocessor APIC
68h	Enable external and processor caches
69h	Setup System Management Mode (SMM) area
6Ah	Display external L2 cache size
6Ch	Display shadow-area message
6Eh	Display possible high address for UMB recovery
70h	Display error messages
72h	Check for configuration errors
74h	Test real-time clock
76h	Check for keyboard errors
7Ah	Test for key lock on
7Ch	Set up hardware interrupt vectors
7Eh	Initialize coprocessor if present
80h	Disable onboard Super I/O ports and IRQs
81h	Late POST device initialization
82h	Detect and install external RS232 ports
83h	Configure non-MCD IDE controllers
84h	Detect and install external parallel ports
85h	Initialize PC-compatible PnP ISA devices
86h	Re-initialize onboard I/O ports
87h	Configure motherboard configurable devices
88h	Initialize BIOS Data Area
89h	Enable Non-Maskable Interrupts (NMIs)
8Ah	Initialize extended BIOS data area
8Bh	Test and initialize PS/2 mouse
8Ch	Initialize diskette drive controller
8Fh	Determine number of ATA drives
90h	Initialize hard-disk controllers
91h	Initialize local-bus hard-disk controllers
92h	Jump to UserPatch2
93h	Build MPTABLE for multiprocessor boards
94h	Disable A20 address line
95h	Install CD-ROM for boot

continued

Table 65. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
96h	Clear huge ES segment register
97h	Fix up multiprocessor table
98h	Search for option ROMs
99h	Check for SMART Drive
9Ah	Shadow option ROMs
9Ch	Set up power management
9Eh	Enable hardware interrupts
9Fh	Determine number of ATA and SCSI drives
A0h	Set time of day
A2h	Check key lock
A4h	Initialize typematic rate
A8h	Erase F2 prompt
Aah	Scan for F2 key stroke
Ach	Enter SETUP
Aeh	Clear IN POST flag
B0h	Check for errors
B2h	POST done - prepare to boot operating system
B4h	One short beep before boot
B5h	Terminate QuietBoot
B6h	Check password (optional)
B8h	Clear global descriptor table
B9h	Clean up all graphics
Bah	Initialize DMI parameters
BBh	Initialize PnP Option ROMs
BCh	Clear parity checkers
BDh	Display MultiBoot menu
Beh	Clear screen (optional)
BFh	Check virus and backup reminders
C0h	Try to boot with INT 19
C1h	Initialize POST Error Manager (PEM)
C2h	Initialize error logging
C3h	Initialize error display function
C4h	Initialize system error handler

continued

Table 65. Port 80h Codes (continued)

Code	Description of POST Operation (The following are for boot block in flash memory)
E0h	Initialize the chipset
E1h	Initialize the bridge
E2h	Initialize the processor
E3h	Initialize system timer
E4h	Initialize system I/O
E5h	Check force recovery boot
E6h	Checksum BIOS ROM
E7h	Go to BIOS
E8h	Set huge segment
E9h	Initialize multiprocessor
Eah	Initialize OEM special code
Ebh	Initialize PIC and DMA
Ech	Initialize memory type
Edh	Initialize memory size
Eeh	Shadow boot block
Efh	System memory test
F0h	Initialize interrupt vectors
F1h	Initialize runtime clock
F2h	Initialize video
F3h	Initialize beeper
F4h	Initialize boot
F5h	Clear huge segment
F6h	Boot to mini-DOS
F7h	Boot to full DOS

nnnn = hexadecimal numbers

5.3 BIOS Beep Codes

Beep codes represent a terminal error. If the BIOS detects a terminal error condition, it outputs an error beep code, halts the POST, and attempts to display a port 80h code on the POST card's LED display.

Table 66. Beep Codes

Beeps	80h Code	Description
1	B4h	One short beep before boot
1-2	98h	Search for option ROMs
1-2-2-3	16h	BIOS ROM checksum
1-3-1-1	20h	Test DRAM refresh
1-3-1-3	22h	Test keyboard controller
1-3-4-1	2Ch	RAM failure on address line *nnnn*
1-3-4-3	2Eh	RAM failure on data bits *nnnn* of low byte of memory bus
1-4-1-1	30h	RAM failure on data bits *nnnn* of high byte of memory bus
2-1-2-3	46h	Check ROM copyright notice
2-2-3-1	58h	Test for unexpected interrupts

nnnn = hexadecimal numbers

6 Specifications and Customer Support

6.1 Online Support

Find information about Intel boards under “Product Info” or “Customer Support” at this World Wide Web site:

http://www.intel.com/

6.2 Specifications

The motherboard complies with the following specifications:

Table 67. Compliance with Specifications

Specification	Description	Revision Level
AGP	Accelerated Graphics Port Interface Specification	Revision 1.0, July 1996, Intel Corporation. The specification is available through the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February 1996, Intel Corporation, Microsoft Corporation
ACPI	Advanced Power Management BIOS interface specification	Revision 1.0, December 22, 1996 Intel Corporation, Microsoft Corporation, and Toshiba Corporation
ATA-3	Information Technology - AT Attachment-3 Interface	X3T10/2008D Revision 6 ATA Anonymous FTP Site: fission.dt.wdc.com
ATAPI	ATA Packet Interface for CD-COMs	SFF-8020i Revision 2.5 (SFF) Fax Access: (408) 741-1600
ATX	ATX form factor specification	Revision 2.01, February 1997, Intel Corporation. The specification is available at: http://www.intel.com/
DMI	Desktop Management Interface BIOS specification	Version 2.0, October 16, 1995 American Megatrends Inc., Award Software International Inc., Dell Computer Corporation, Intel Corporation, Phoenix Technologies Ltd., SystemSoft Corporation
El Torito	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies Ltd., IBM Corporation. The El Torito specification is available at: http://www.ptltd.com/techs/specs.html
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2], v1.7
Multiprocessor systems	Multiprocessor specification	Version 1.4, May 1997, Intel Corporation

continued

Table 67. Compliance with Specifications (continued)

Specification	Description	Revision Level
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1995, PCI Special Interest Group
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994, Compaq Computer Corporation, Phoenix Technologies Ltd., Intel Corporation
Power Supply	Intel Workstation Product Division 300 W Power Supply Design Guide	Revision 1.0, June 1998, Intel Corporation. The specification is available at: http://www.intel.com/
SDRAM DIMMs	PC SDRAM Specification PC SDRAM Unbuffered DIMM Specification PC SDRAM Registered DIMM Specification PC SDRAM Serial Presence Detect (SPD) Specification	Version 1.51, November 1997, Intel Corporation Revision 1.0, February 1998, Intel Corporation Revision 1.0, February 1998, Intel Corporation Revision 1.2A, December 1997, Intel Corporation
UHCI	Universal Host Controller Interface	Revision 1.1
USB	Universal serial bus specification	Revision 1.0, January 15, 1996, Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, Northern Telecom