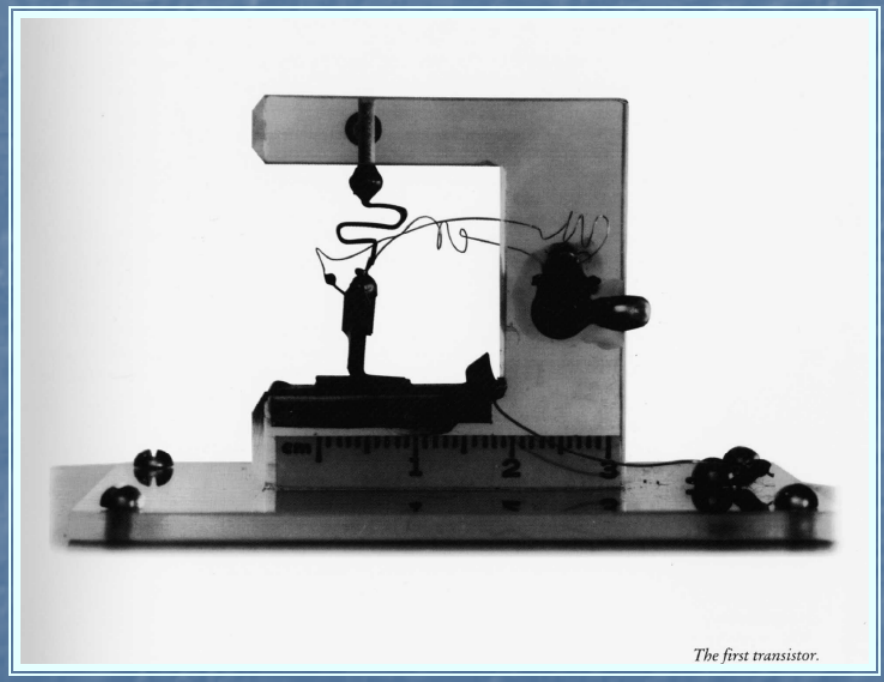
Tops down Nanotechnology breakthrough

12th EMEA Academic Forum
Paula Goldschmidt
Principal Engineer
EMEA Development Manager - TME Director
Budapest/07

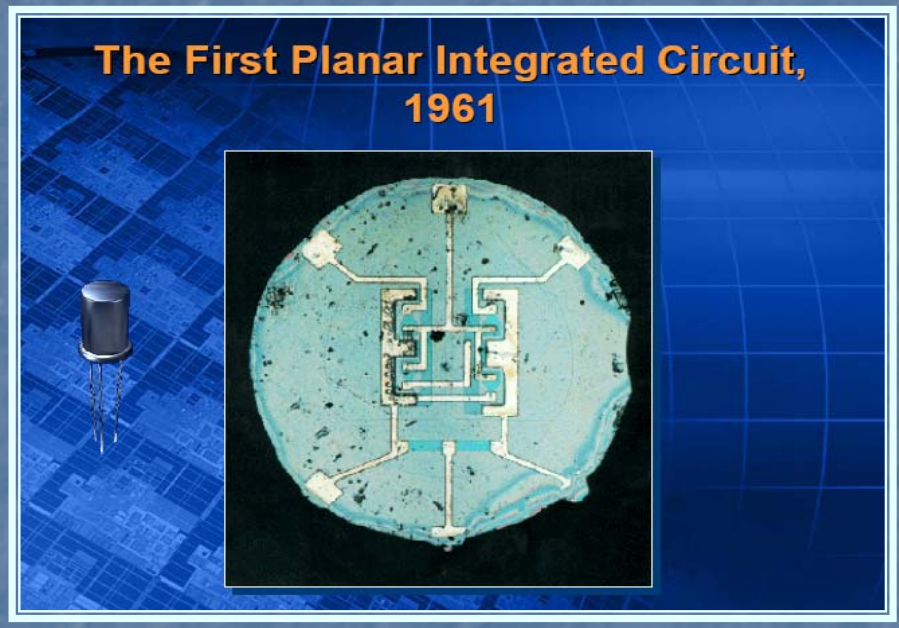
Let's start from the beginning
The bipolar Transistor

- 1947- J. Bardeen and W. Brattain invented and demonstrated the Point-contact transistor
- 1948- W.B. Shockley invented the junction transistor

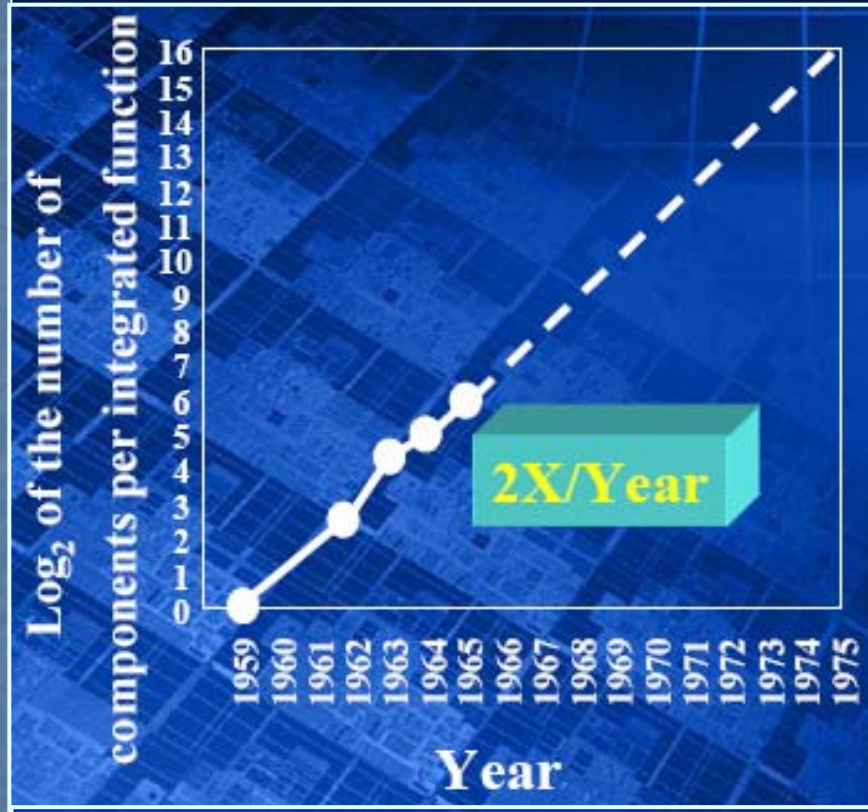


Let's start from the beginning
The integrated circuit

- 1959- Robert Noyce invented the Integrated Circuit by using Aluminum Interconnections patterned by photolithography and defined by chemical etching
- 1959 -Jack Kirby invented the hybrid integrated circuit by using Au wires



1965-First Introduction of Moore's Law



" Dr. Gordon E. Moore is one of the new breed of Electronic Engineers, schooled in the physical sciences rather then in electronics"

Electronics Magazine (35th anniversary), April 19, 1965

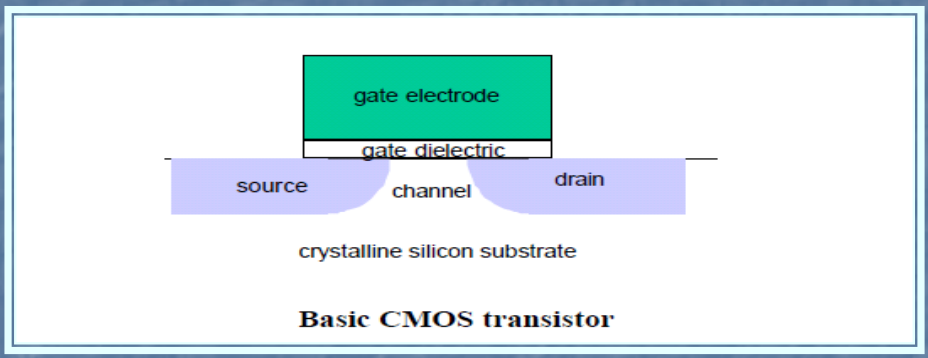
1969- Commercialization of Silicon Gate

IEEE Spectrum October, 1969 28

Silicon-gate technology

Low-cost, large-scale integrated electronics based on metal-oxide-semiconductor design benefits from the application of silicon-gate technology

L. L. Vadasz, A. S. Grove, T. A. Rowe, G. E. Moore *Intel Corporation*



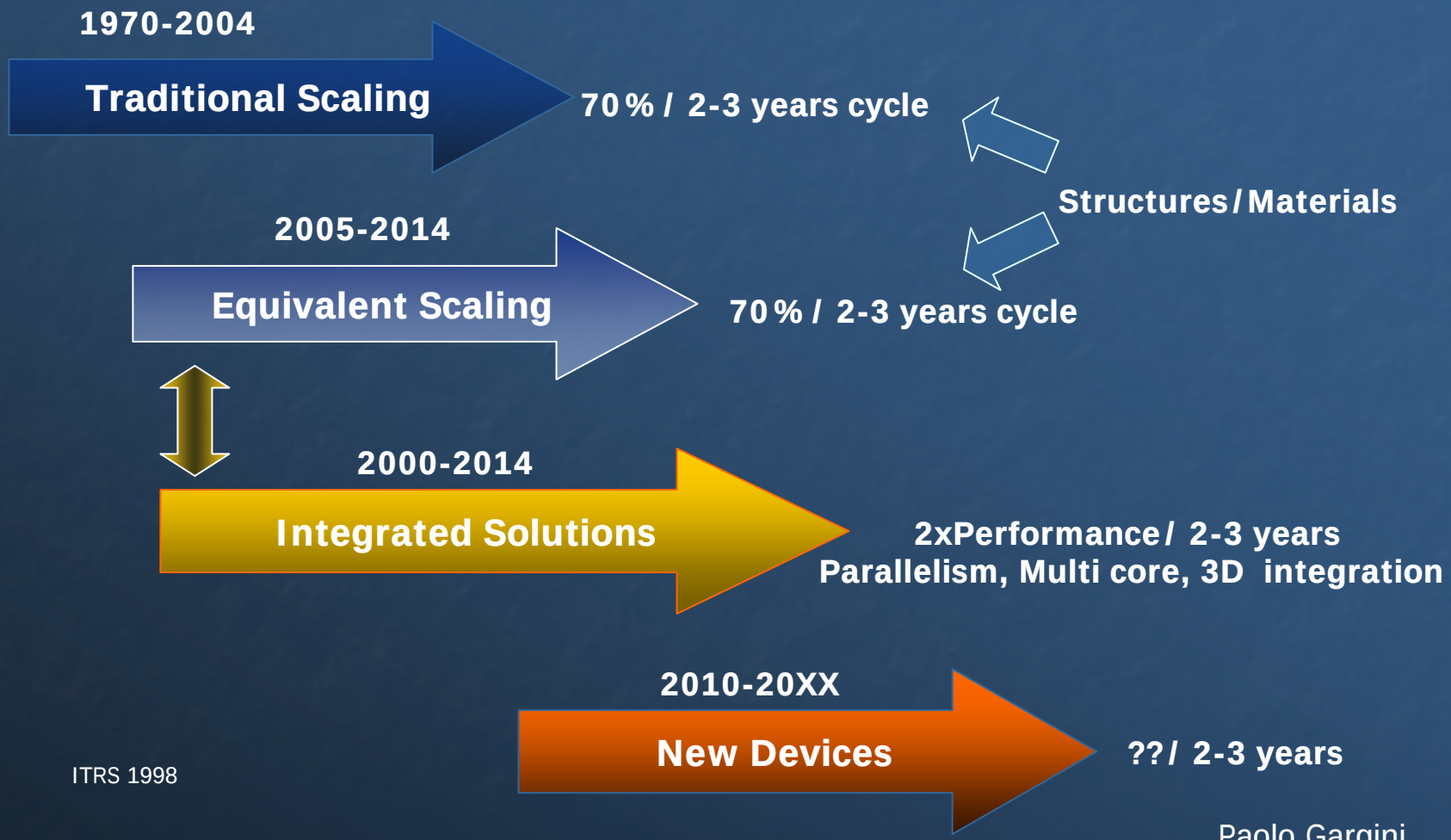
Basic CMOS transistor

Intel was the first company to develop a manufacturable transistor process using silicon gate electrodes instead of aluminum. Although the metal was gone, these transistors were still referred to as MOSFETs.

Commercialization of MOS

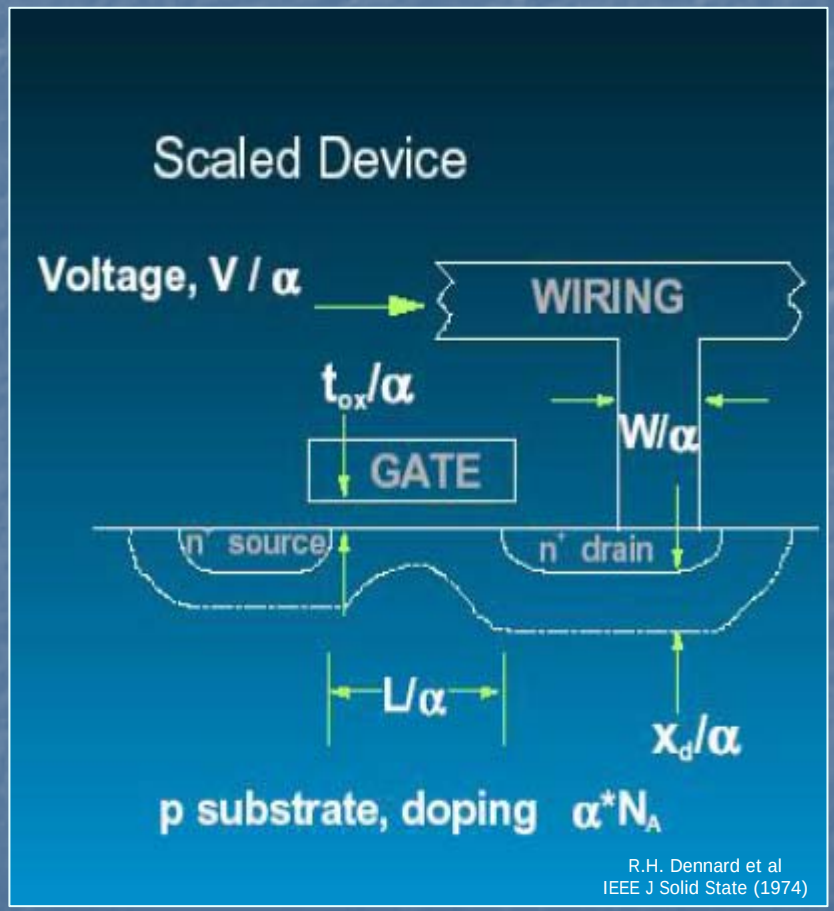
- *1969- 1101, 6T, 256 SRAM produced*
- *1970- 1103, 3T, 1Kbit DRAM produced*
- *1971- 2101/2, 6T, 1Kbit SRAM produced*
- *1971- 4004 MPU produced*
- *1972- 2104, 1T, 4Kbit DRAM produced*

Future Directions



Paolo Gargini
Intel Fellow

MOS Transistors
Traditional Scaling



R.H. Dennard et al
IEEE J Solid State (1974)

Parameters

SCALING:

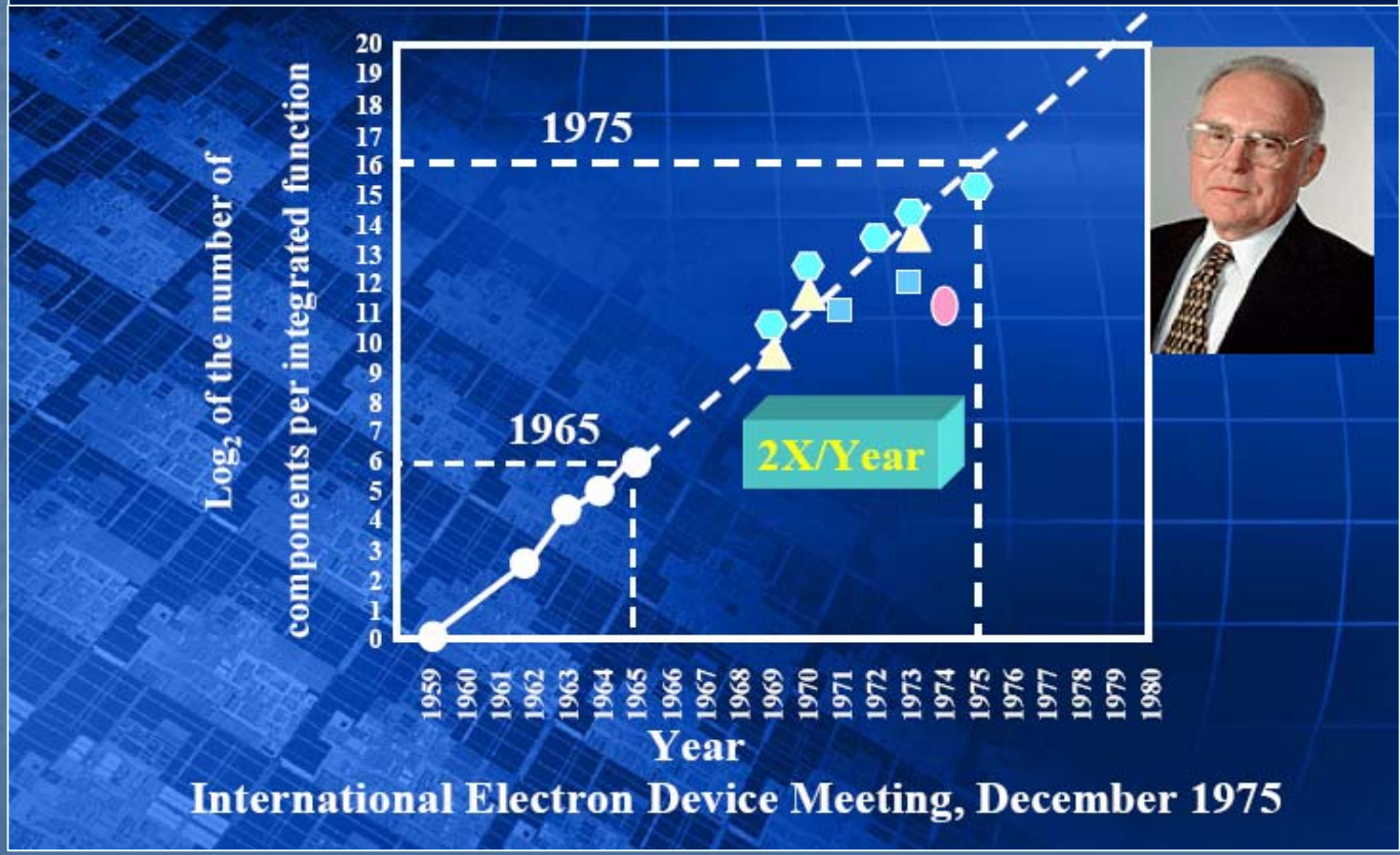
Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

RESULTS:

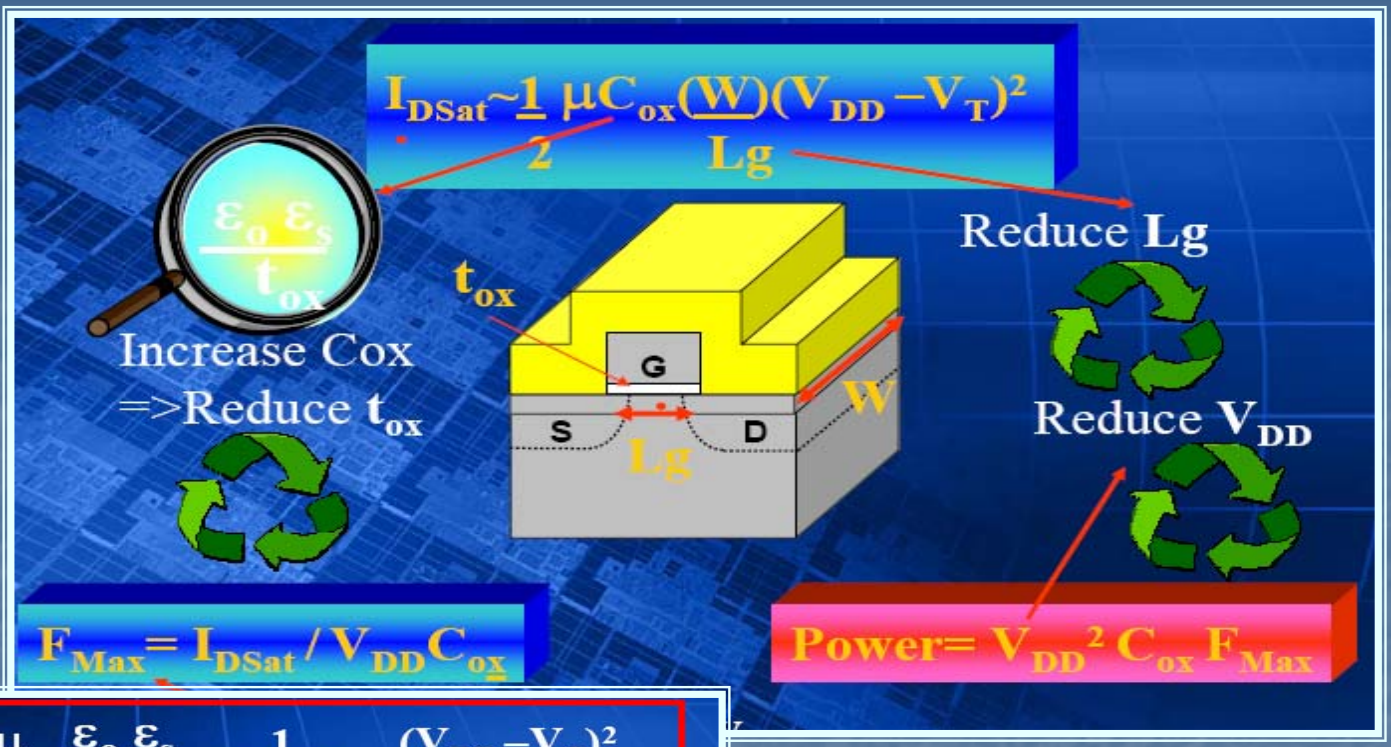
Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Lower Power/ckt:	$\sim 1/\alpha^2$
Power Density:	~Constant

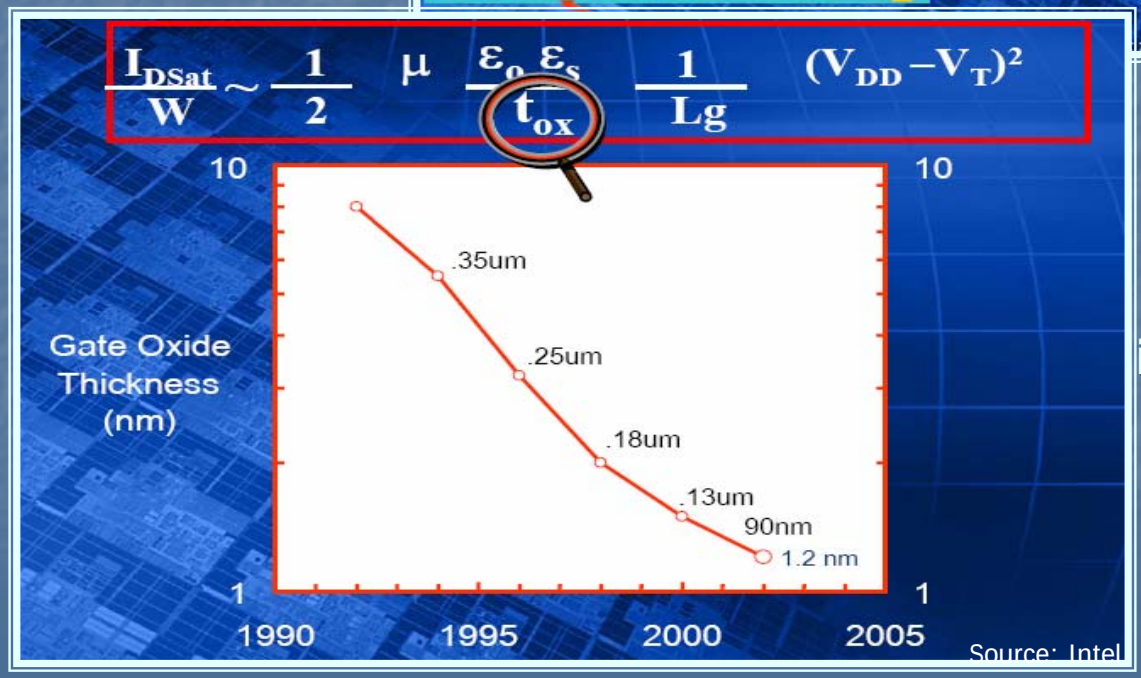
(Source: R. Isaac, 2001)

1975-Second Update of Moore's Law



Traditional Scaling Transistors Trade off

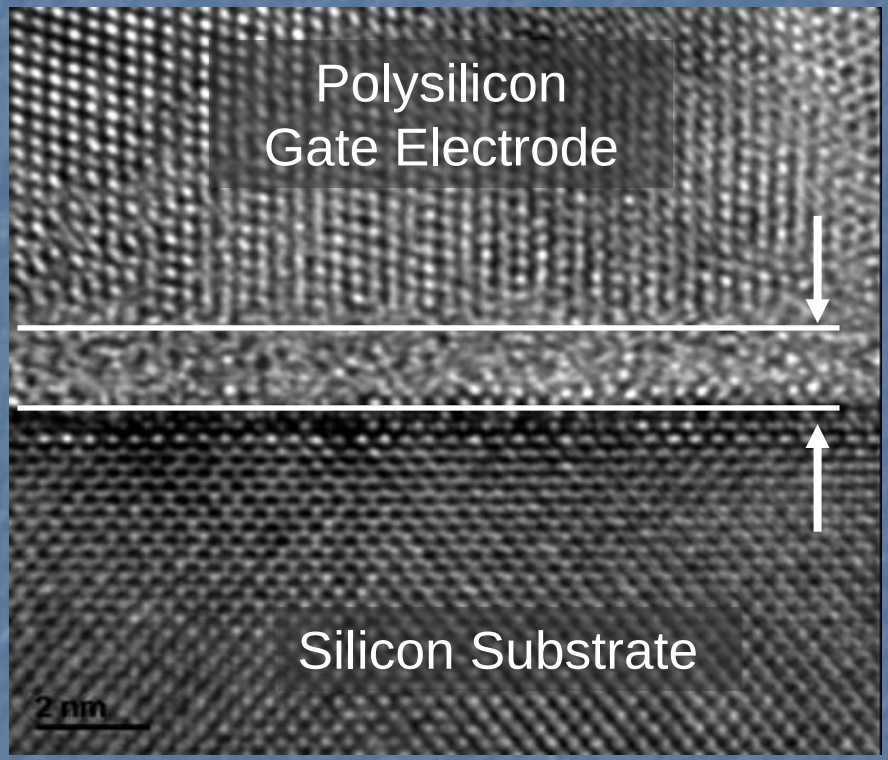




Thinner gate oxide increases transistor performance

90-65 nm Generation Gate Oxide

Nanoelectronics is here!

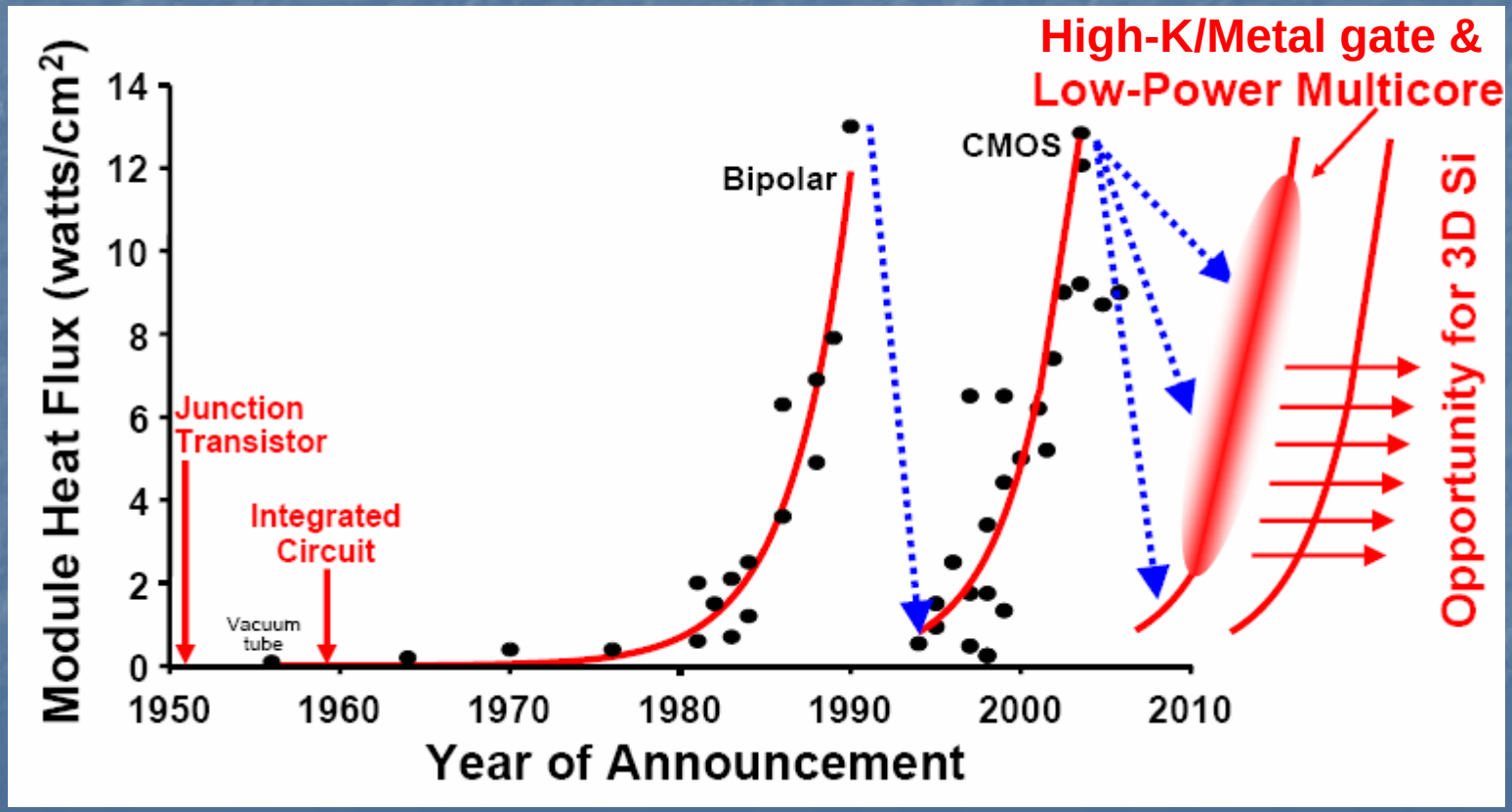


1.2 nm SiO_2

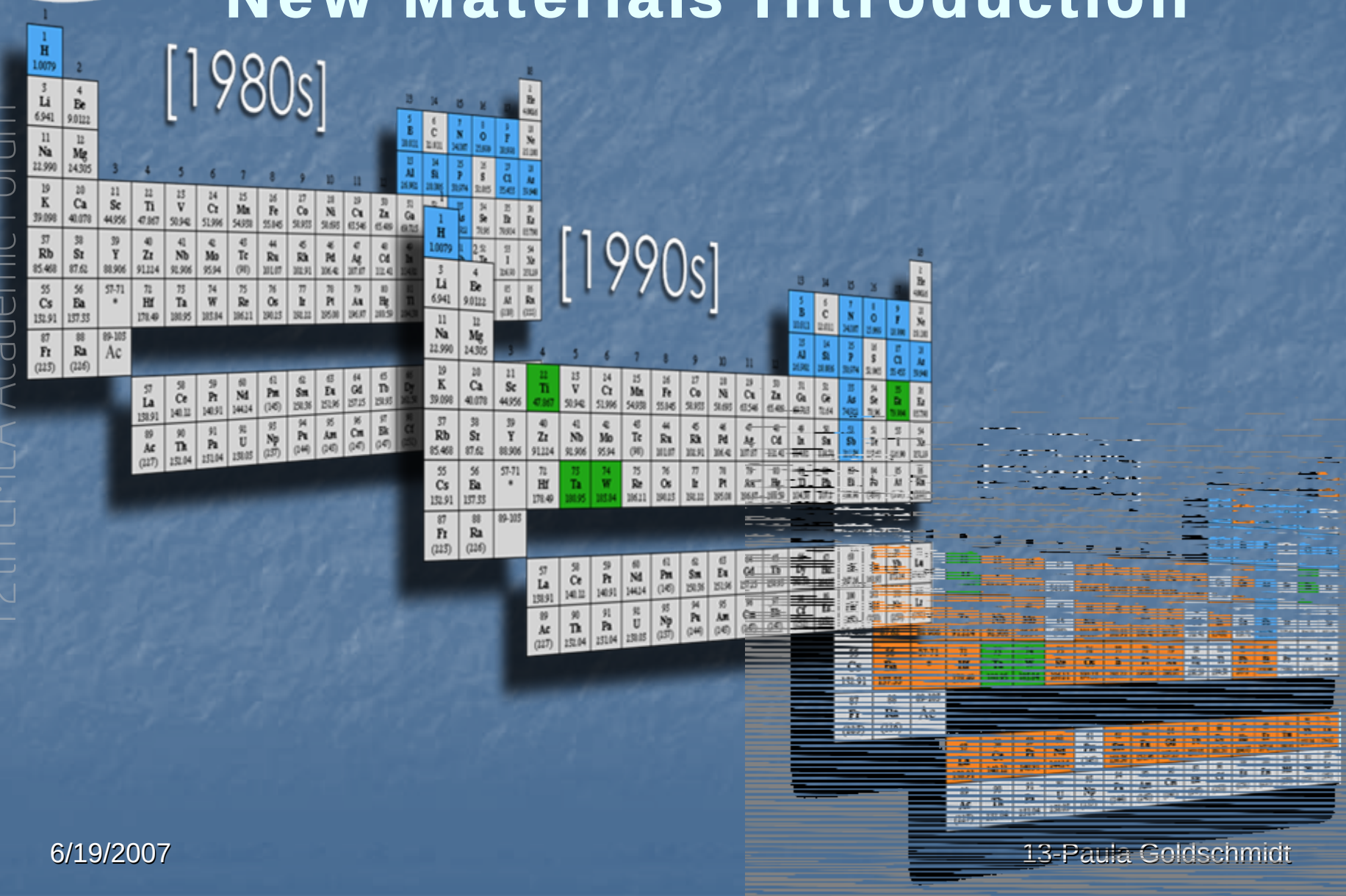
Gate oxide is less than 4-5 atomic layers thick

Literally: *"We are running out of atoms"*

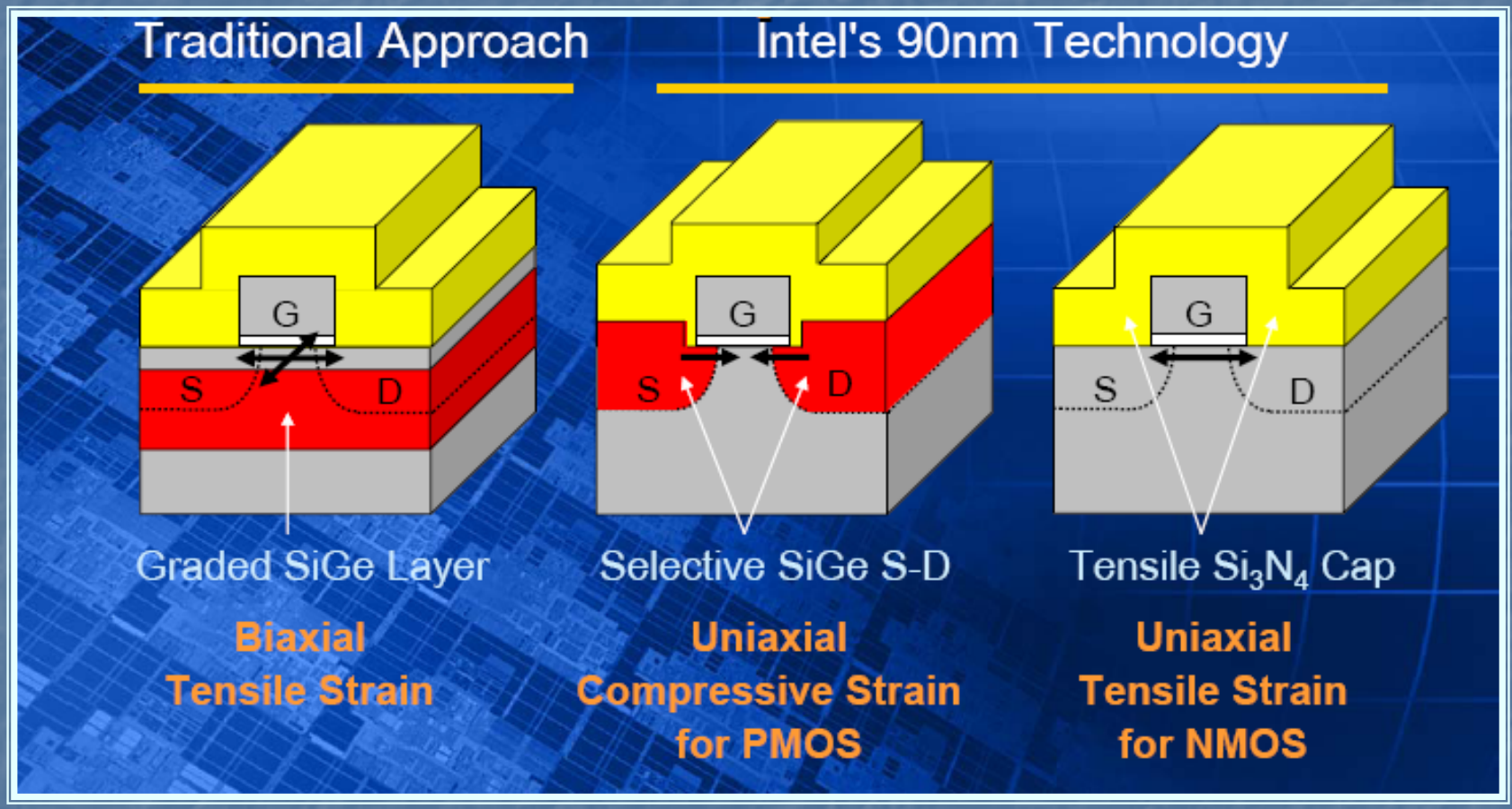
Integrated Solutions
Performance improvement through Power Reduction and Higher Density



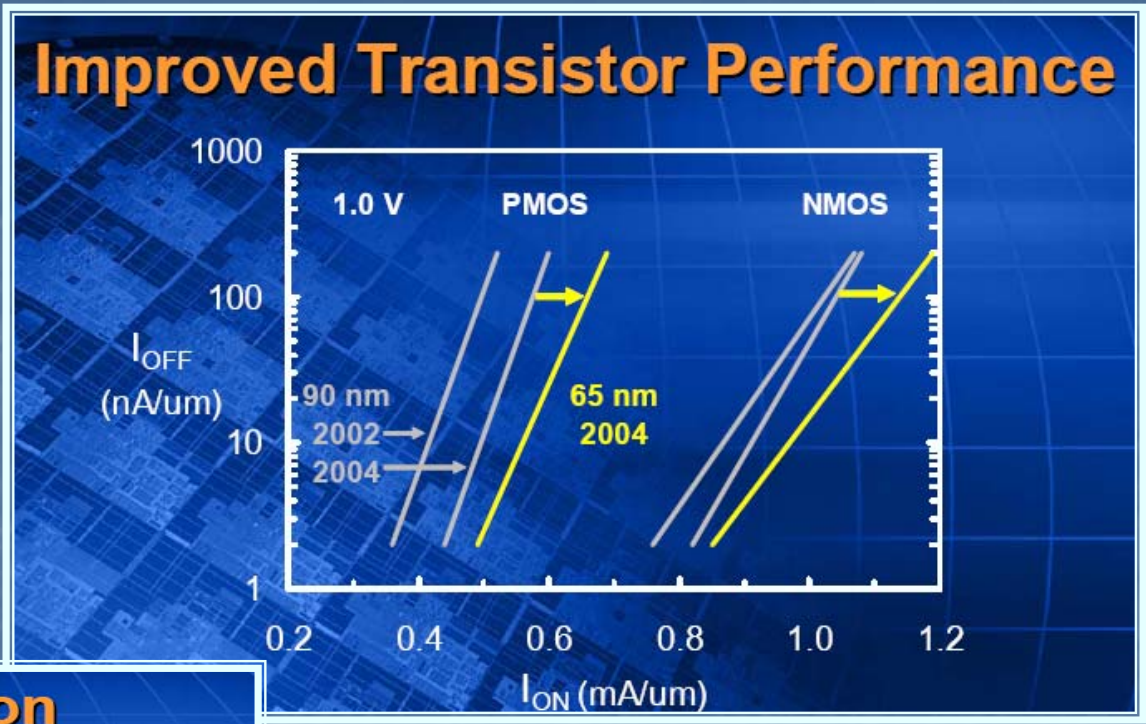
Equivalent Scaling
New Materials Introduction



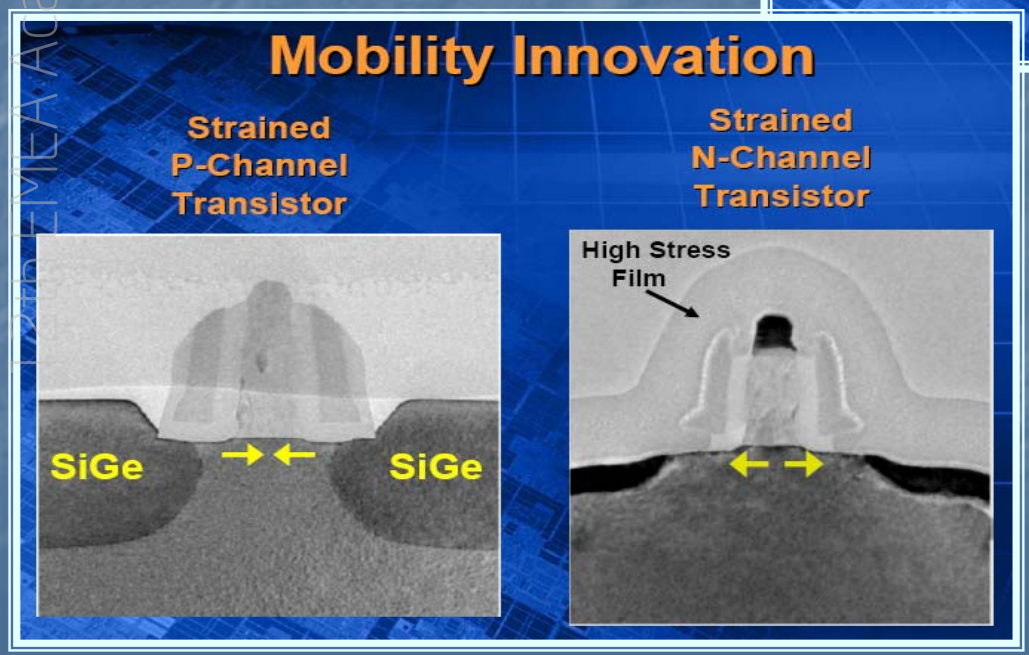
Equivalent Scaling
Transistors Strain Techniques



Strained Si

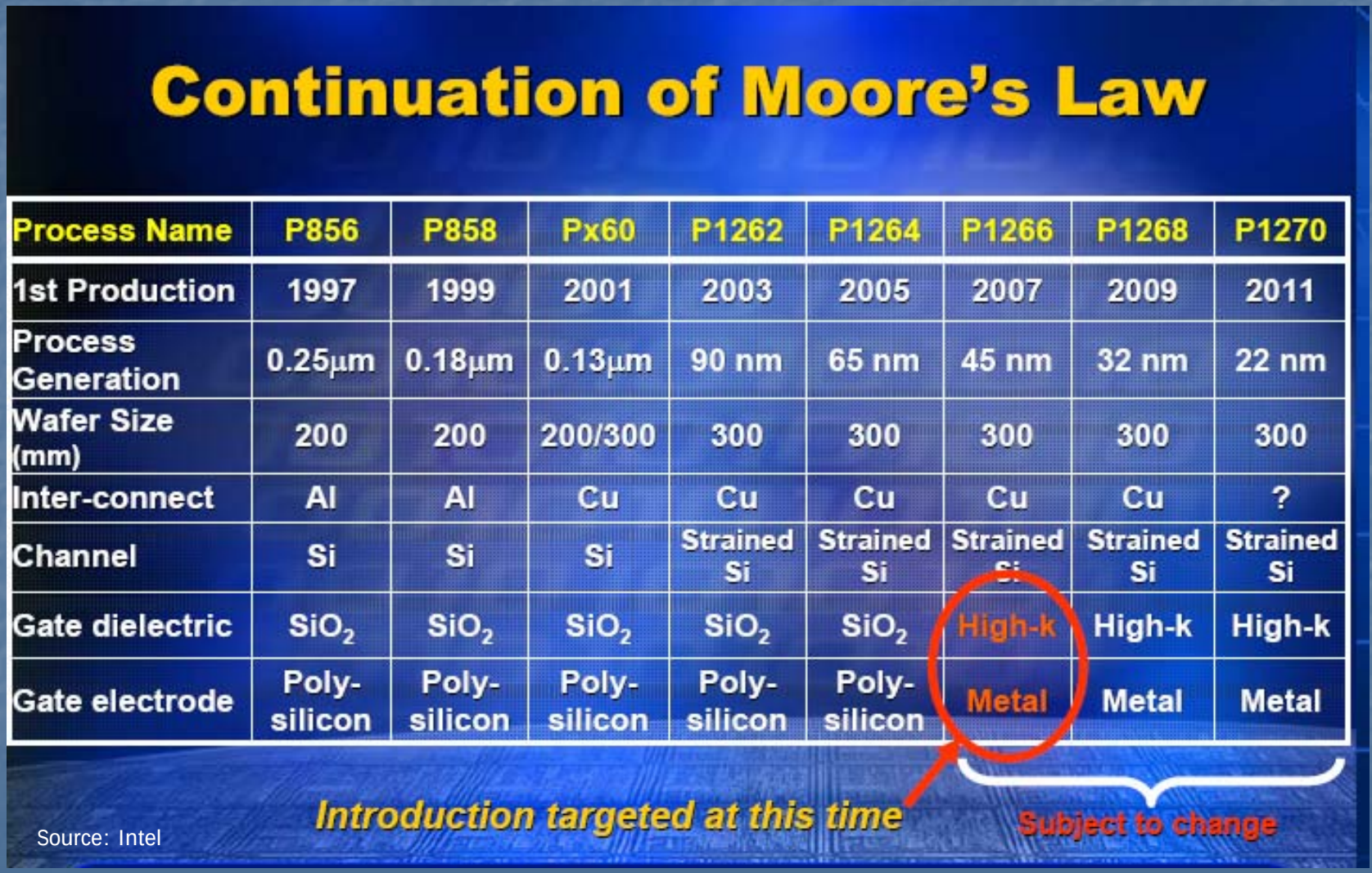


65nm transistors drive current increased in 10-15%

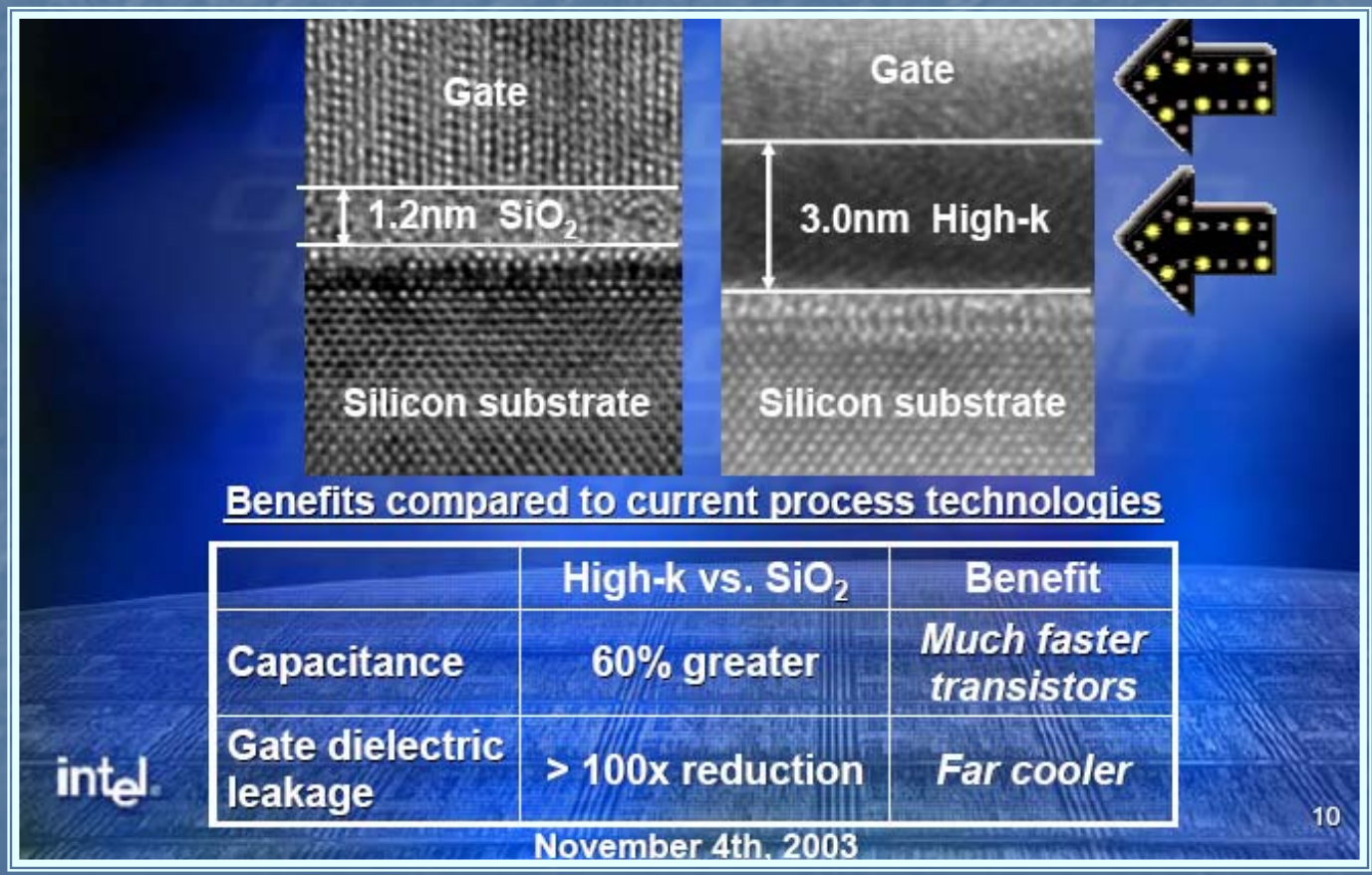


Source Intel

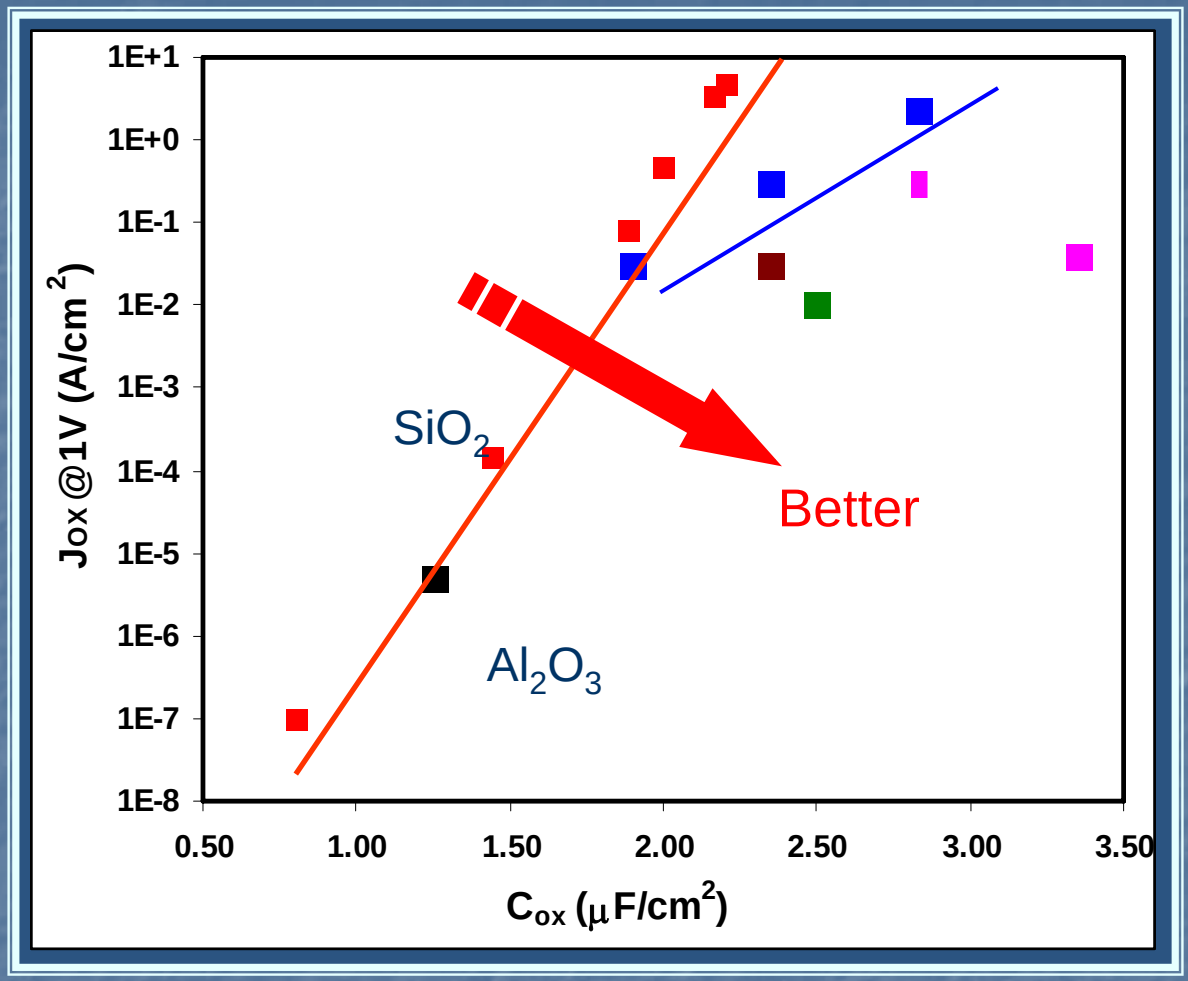
Intel found the solution for High-k & Metal Gate Combination



Equivalent Scaling
High-K Dielectric decreases leakage substantially



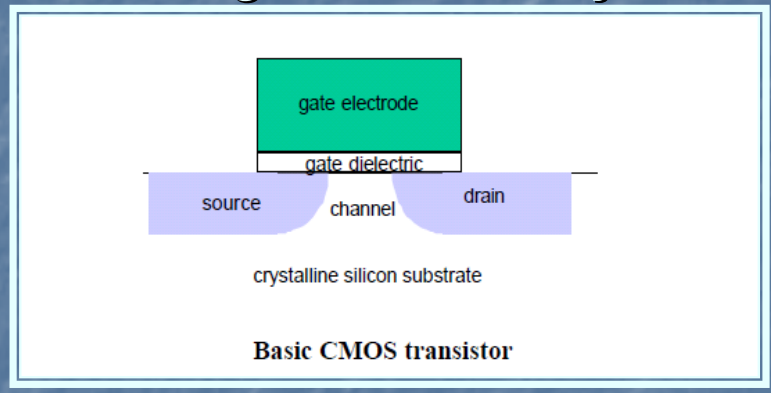
High-k Gate Dielectric Materials



High-k dielectrics provide higher capacitance and reduced leakage

High-K Dielectric Gate Stack and Metal gate Materials

Biggest Breakthrough since Poly Gate introduction



Basic CMOS transistor

- In the aim of replacing SiO2 as Gate insulator High –K material were introduced in gate stacks
- **Hafnium-based dielectrics** as the most promising option of several potential materials. High dielectric constant (K) allows thicker insulation layer (to reduce leakage) while maintaining same capacitance
- But High-K material interacts with Poly-Si, and required a capping layer between them that reduce overall capacitance due to its low-K or **Changing the gate electrode to metal** (now in a self-aligned fashion) also provided added transistor performance improvements.

After 40 year Intel announced: Dramatically new materials used for transistor construction

The technical breakthrough:

- **Two key transistor structures changed**:
  - **The switch's insulating walls**
  - **The gate**
- **A hafnium-based material** was selected to change **the gate dielectric silicon oxide**
- A new combination of **metal materials for the transistor gate electrode**. .
- New 45nm transistors, operates with **very low current leakage and record high performance**.

An Intel engineer holding a 300mm wafer with 45nm shuttle test chips.

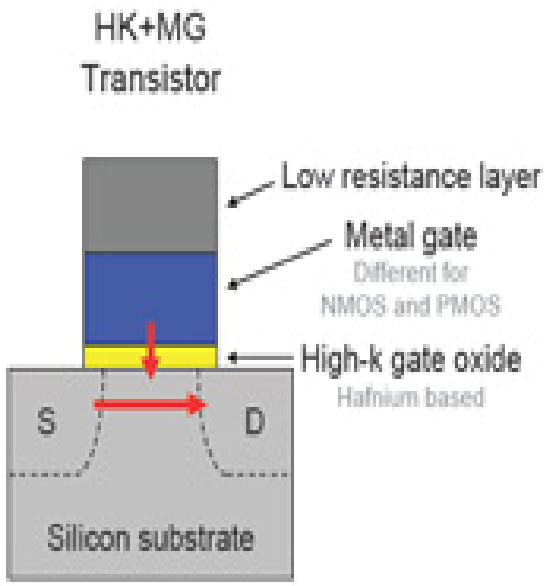
45nm Transistors
How do they work

High-k + Metal Gate Transistors

Metal Gate
- Increases the gate field effect

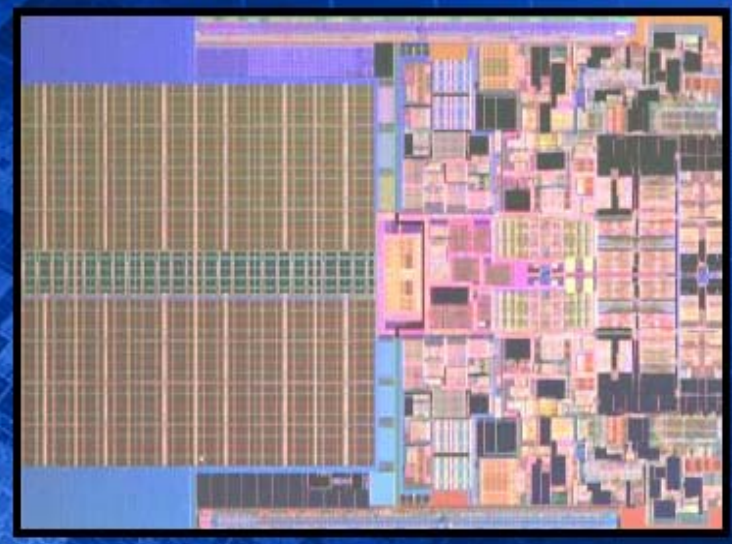
High-k Dielectric
- Increases the gate field effect
- Allows use of thicker dielectric layer to reduce gate leakage

HK + MG Combined
- Drive current increased >20% (>20% higher performance)
- Or source-drain leakage reduced >5x
- Gate oxide leakage reduced >10x



Caption: schematic of High-k and metal gate

Penryn Die Photo

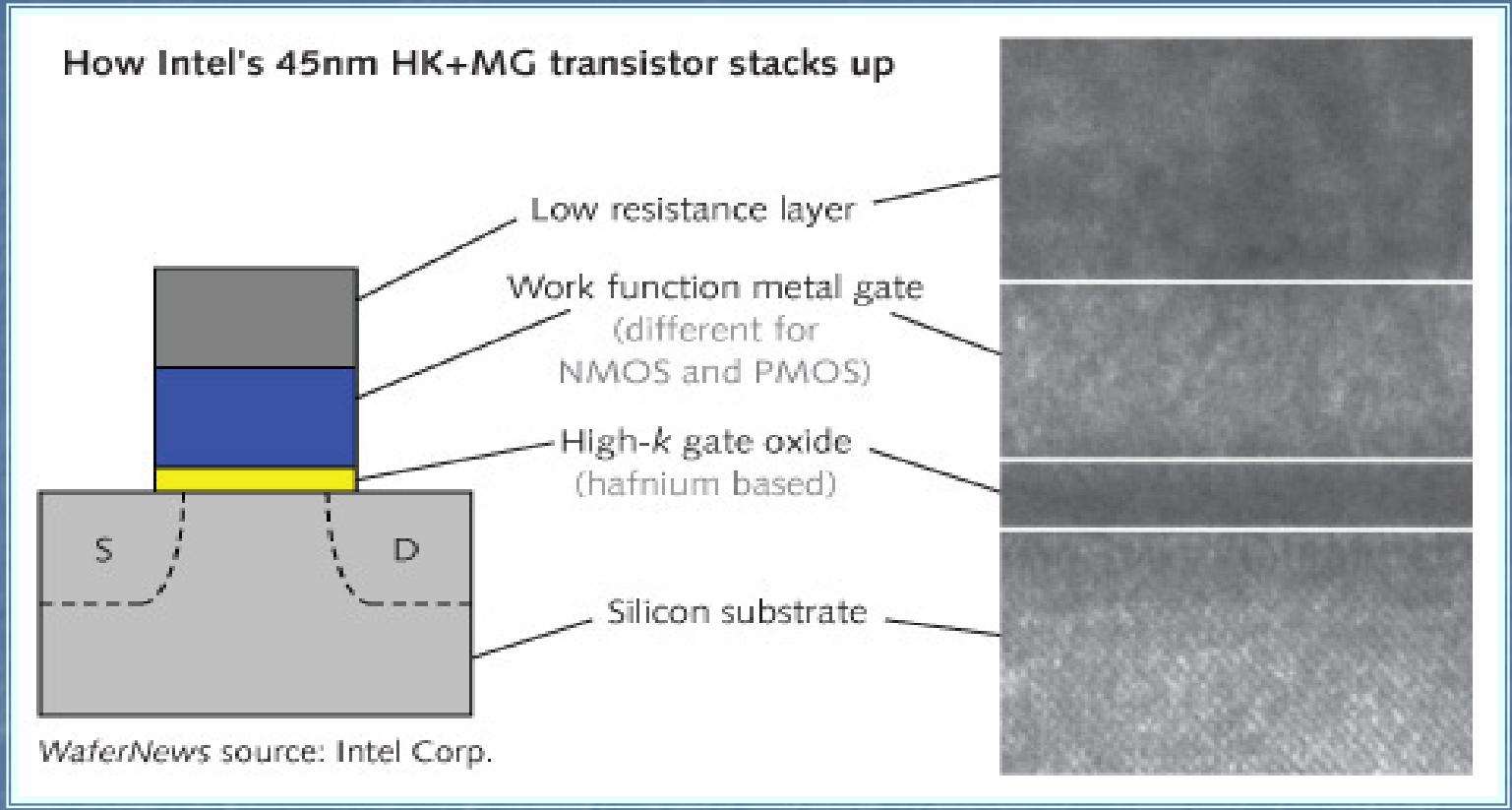


45 nm next generation Intel® Core™2 family processor

410 million transistors for dual core, 820 million for quad core

World's first working 45 nm CPU

Gate leakage reduction



The reduction in gate leakage results from the fact that the gate oxide thickness can be increased using this hafnium-based high-*k* dielectric, which is produced by atomic layer deposition (ALD)

45nm Manufacturing Capabilities

Fab 32 in Arizona. Ramping 45nm in the second half of 2007.

Fab 28 in Israel. Ramping 45nm in the first half of 2008

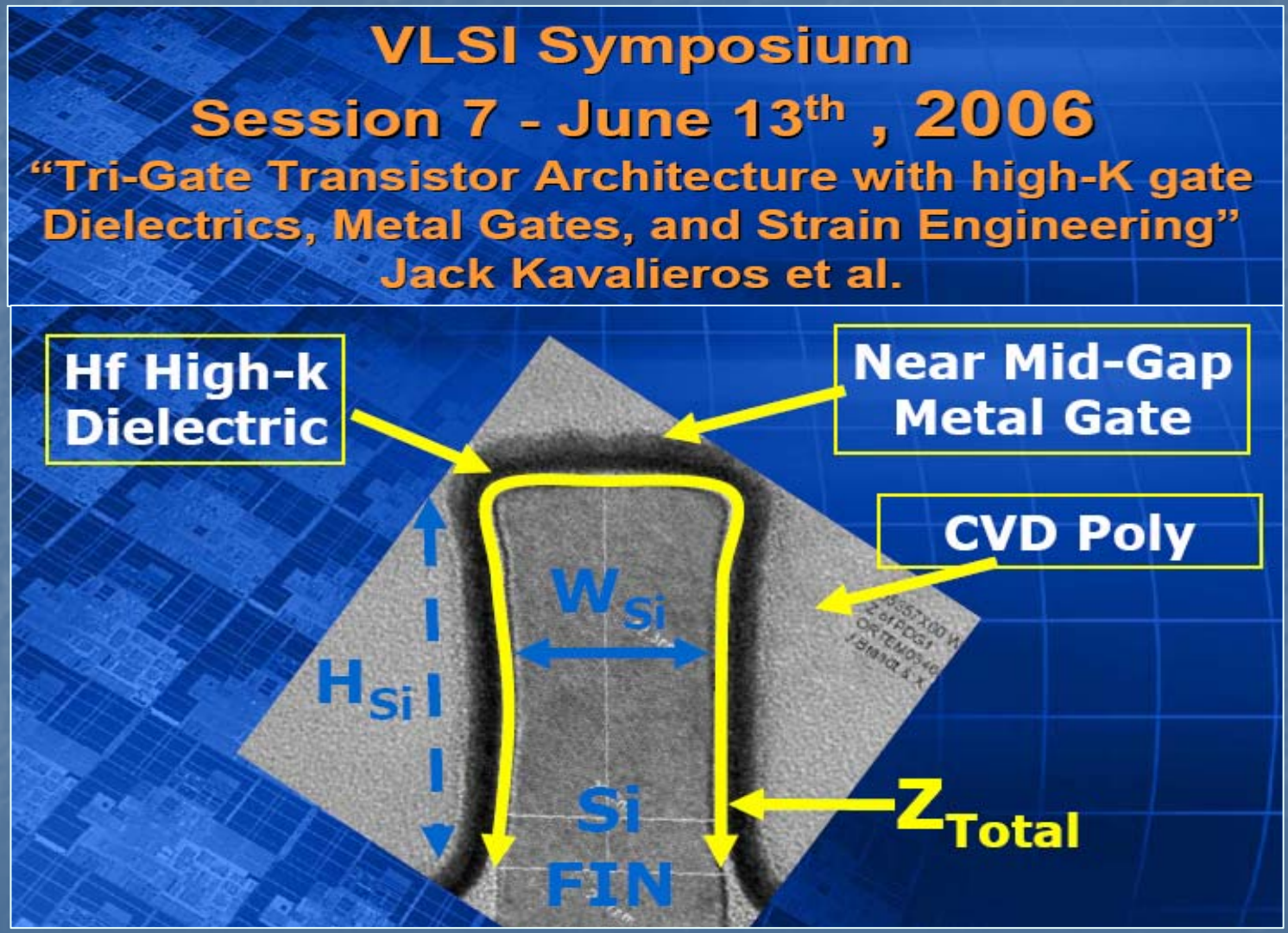
D1D in Oregon. Ramping 45nm in the second half of 2007.

The new 45nm transistors will power the next-generation Intel® Core™2 Duo, Intel Core 2 Quad, and Intel Xeon families of multi-core processors. Intel has five early-version products up and running, both dual-core and quad-core parts—the first of fifteen 45nm processor products that Intel is planning

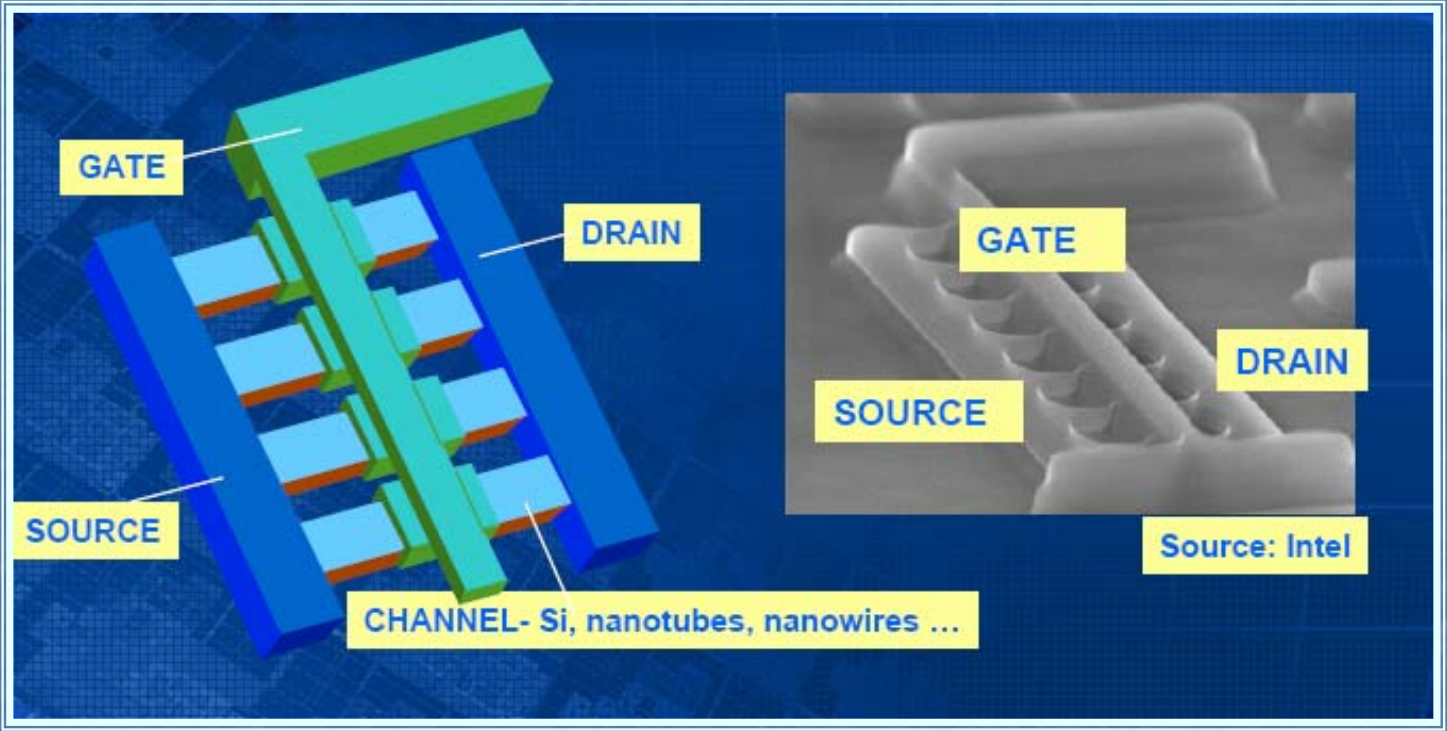
New 45nm technology offers superior performance

The collaboration of many groups across Intel and Suppliers was needed to make this happen.

New structures for the future



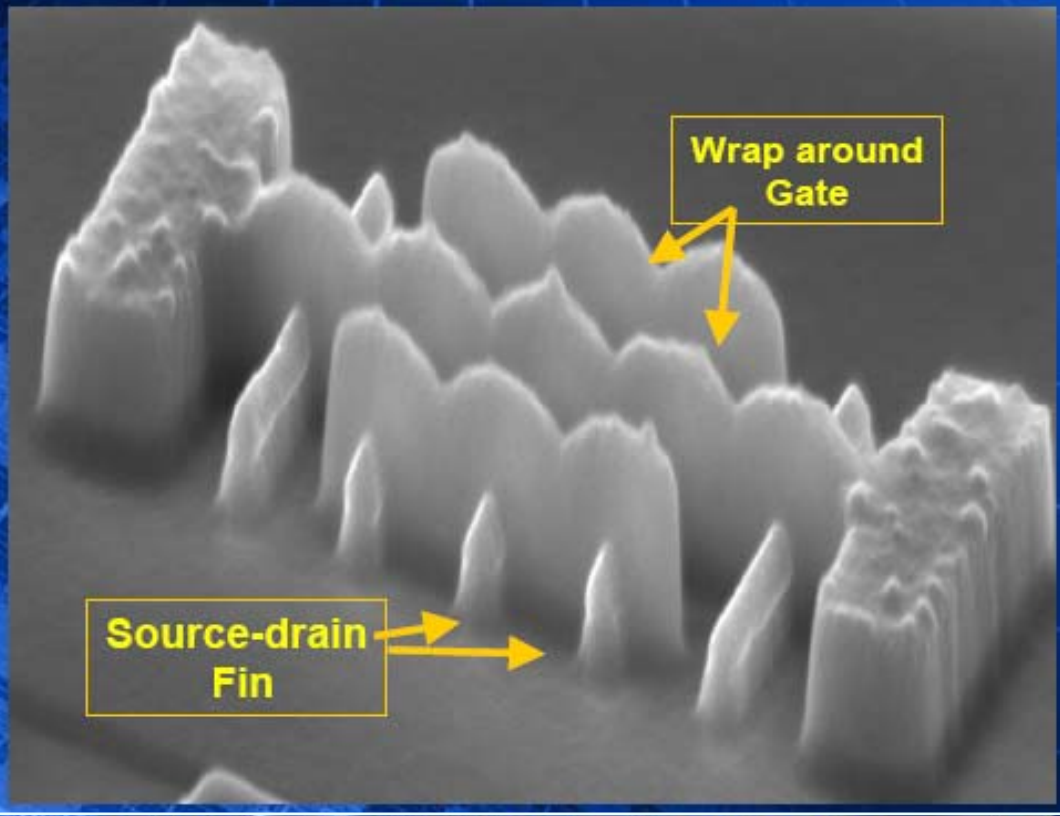
Tri-gate Transistor
“A template for the Future”



Technical Details presented at:
Robert Chau - ISSDN Conference, Japan, Sept. 17, 2002

VLSI Symposium, 6-2006

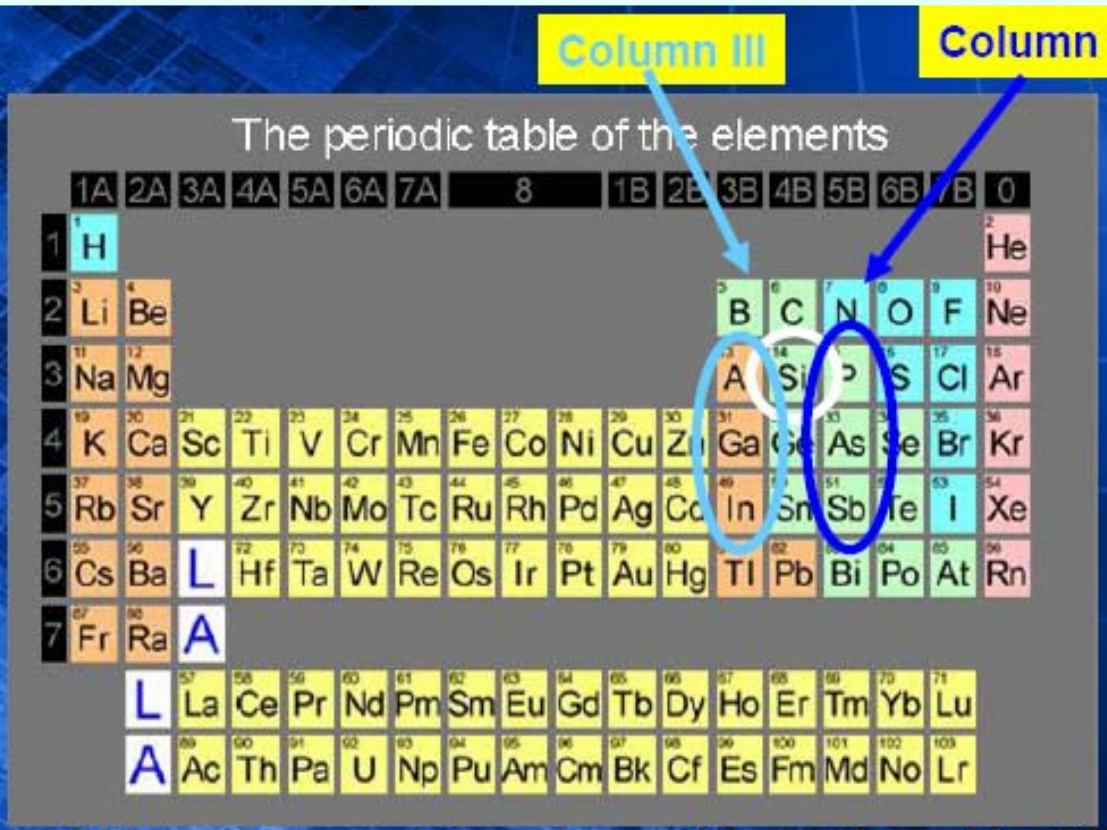
The Key is Optimizing the Integration



1. Tri-gate gives better off current and therefore less wasted power
2. High k – metal gate gives both higher speed and less wasted power
3. Strained Si produces higher speed and less wasted power

The sum of all these pieces is once again world leading transistors

Beyond Si
III-V Materials compounds



Si = Silicon
Al = Aluminum
Ga= Gallium
In = Indium
P = Phosphorous
As = Arsenic
Sb = Antimony

- Silicon in transistor channel is replaced by "III-V compound semiconductor"
- Result is much higher electron mobility, meaning significant performance and power improvements

S. Datta

Beyond Si
Increase Electron Mobility

Increased mobility in the transistor channel leads to higher performance and less energy consumption

$$I_{DSAT} \propto \frac{W}{L} \cdot \mu \cdot C_{OX}$$

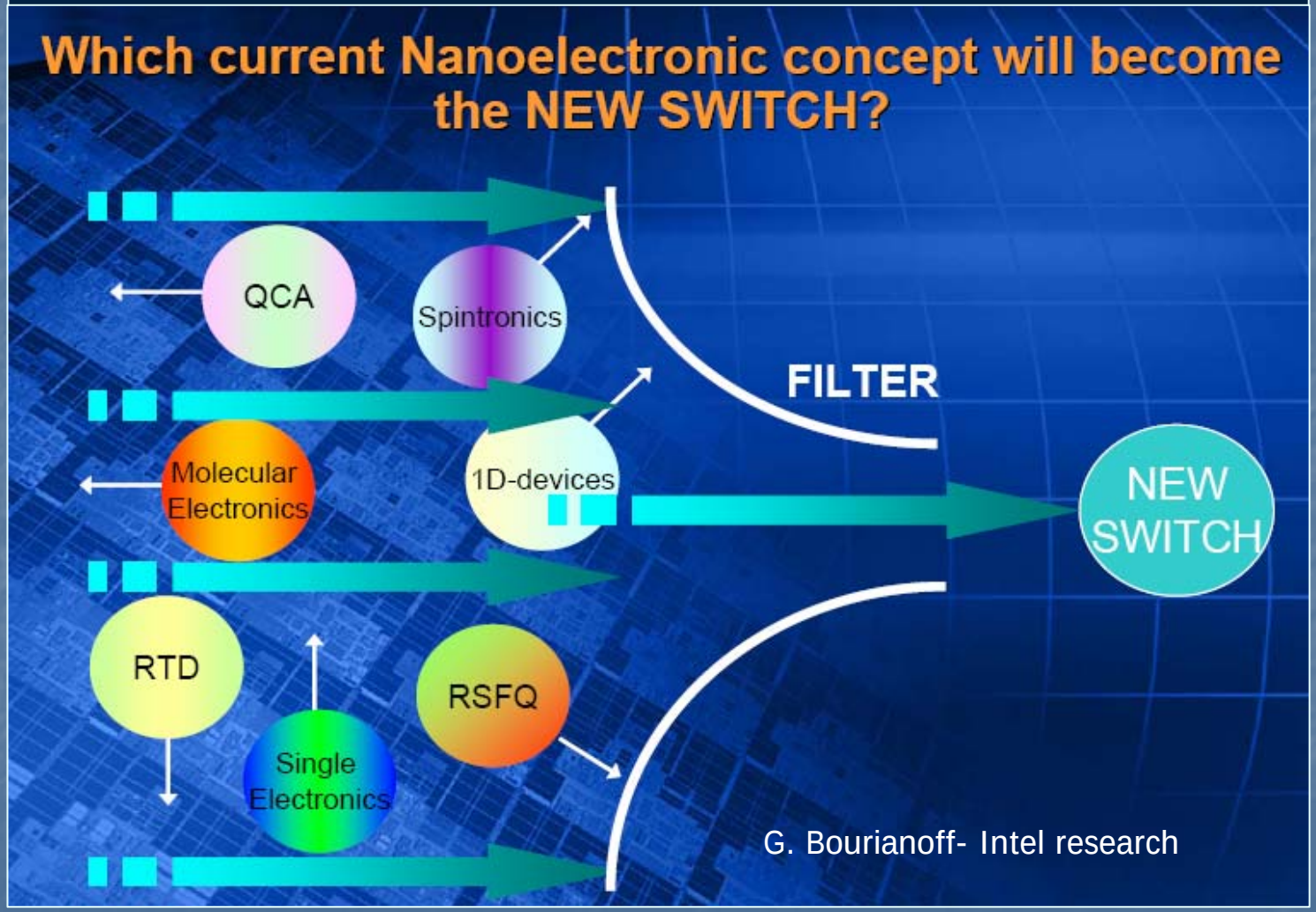
Relative mobility

	Compound Semiconductors		
Si	GaAs	InAs	InSb
1	8	33	50

Compound semiconductors have higher electron mobility than Si; InSb (indium antimonide) is highest of all

S. Datta

Beyond CMOS


Which current Nanoelectronic concept will become the NEW SWITCH?
QCA
Spintronics
FILTER
Molecular Electronics
1D-devices
NEW SWITCH
RTD
RSFQ
Single Electronics
G. Bourianoff- Intel research

Research directions in beyond CMOS computing

Device	Switching energy ev	Status	Comments	Reference
65 nm planar CMOS	2500	production	NMOS	Chau et.al. Proceedins of the IEDM 2005
10 nm planar CMOS	1.8	prototype	NMOS	Chau et.al. Proceedins of the IEDM 2005
single electron/ 2 quantum wells	25 X 10^{-3}	Theory	Room Temperature, BER = 1, 1.5 nm barrier	Zhirnov et. al Proceedings of the IEEE Nov 2003
SPIN				
Mn atoms on Cu	5 X 10^{-3}	Experimental results	3 atom linear chain, single atom spin flip, Low temperature,	Hirjibehdin et.al, Science Vol 312, 19 May 2006
permaloy nano magnets	1	Experimental results	130nmX70nm bistable oval shaped structures, room temp	Porod et.al, Science Vol 311, 13 Jan 2006
Electron spin in Quantum well	1 X 10^{-3}	Theory	Room Temp, B field of 4.5 T, g =200 material	Nikonov et.al., http://arxiv.org/abs/cond-mat/0605298
Dynamic switching	1.3 X 10^{-6}	Theory	Room Temp, B field of 4.5 T, g =200 material	Nikonov et.al http://arxiv.org/abs/cond-mat/0605298

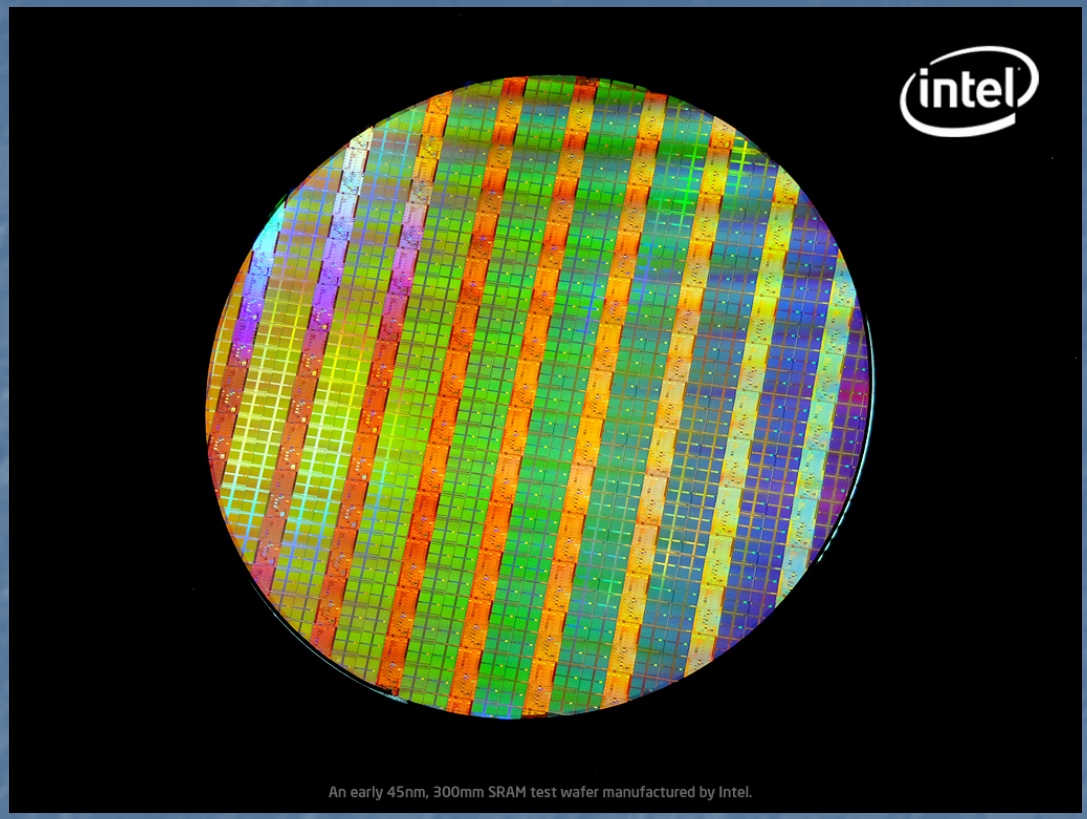
George I. Bourianoff, Paolo A. Gargini and Dimitry E. Nikonov

Summary and Future opportunities

- Intel 45nm Technology is in place
- It took 40 years to introduce a meaningful change in the transistor structure
- Science incubation may require 30-50 years
- Technology definition and initial commercialization can take 10-15 years
- New state variables are being investigated to extend Moore's low beyond 2020
- While "running out of atoms", the Tops down technology development will need to move to a Bottoms up technology.
- Bottoms up industry collaborations should start now to ensure readiness for HVM on time
- Intel operates a Technology Collaboration Program in Europe, and will be glad to listen about future opportunities

- For more information contact:
  - Paula.Goldschmidt@Intel.com
    EMEA Development Manager

45nm SRAM Intel 300mm wafer



Thanks for your attention