IC materials for next decade

450mm challenges and opportunities

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Outline

- Objectives
- The environment
- The evolving world of silicon
- Metallization
- Challenges and opportunities
- Summary

Objective

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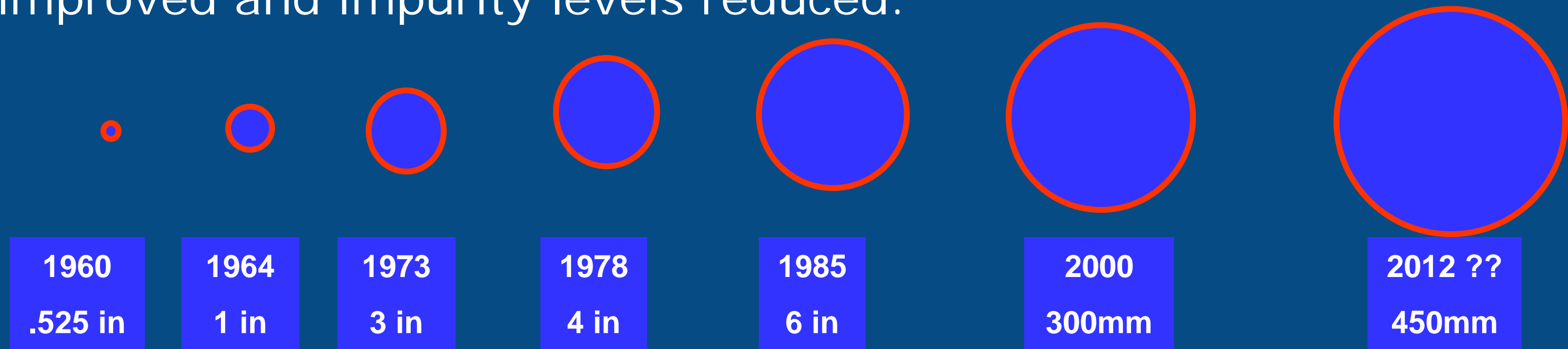
- To present some of the challenges created by the IC manufacturing transition to 450mm wafers for the silicon and metallization.
- To review the academia role and opportunities as driving force for solving engineering challenges created by the wafer size increase.

Our Environment

- Diligently following Moore's Law, introducing a new process technology every two years, scaling linear dimensions by ~30% at each generation
- Increased chip manufacturing complexity
- Expended research and development
- Continuing cost control efforts
- Increasing environmental regulations

Silicon Evolving Environment

- Silicon is the building block of integrated circuits. As the devices become more complex, the line dimensions shrink, the number of transistors growth exponentially and their total area is increased the requirements from silicon materials are evolving. Wafers size is increased, crystal imperfections are eliminated, surface quality is improved and impurity levels reduced.



Wafer Size Progression

- With tougher requirements and specialized demand we see consolidation of supply.
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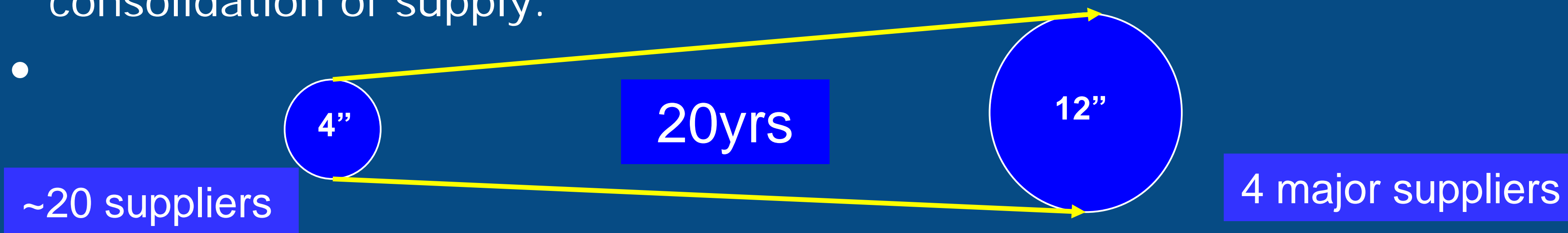

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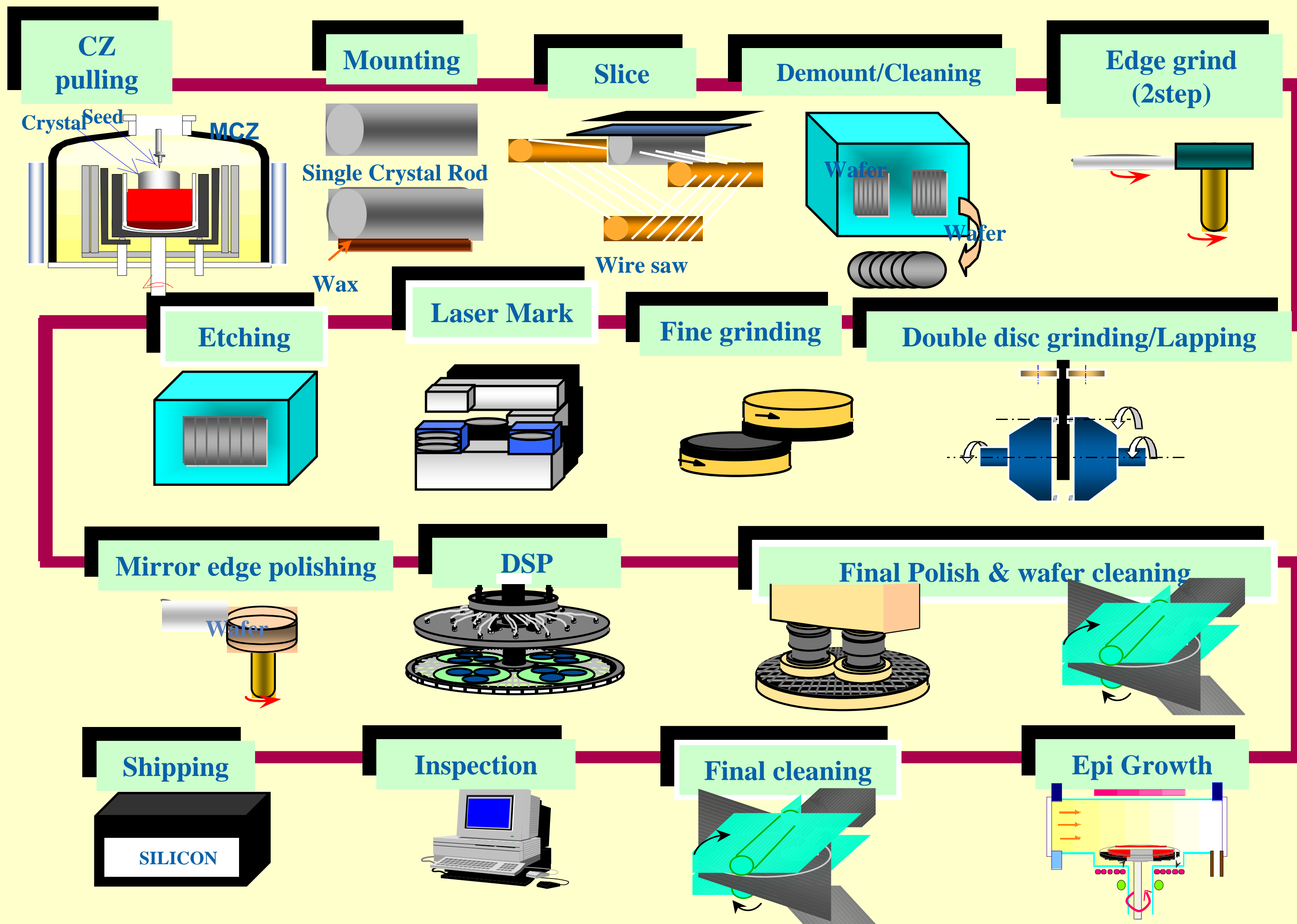
Typical 300mm Epi Si Manufacturing Process Flow



Courtesy of KEM

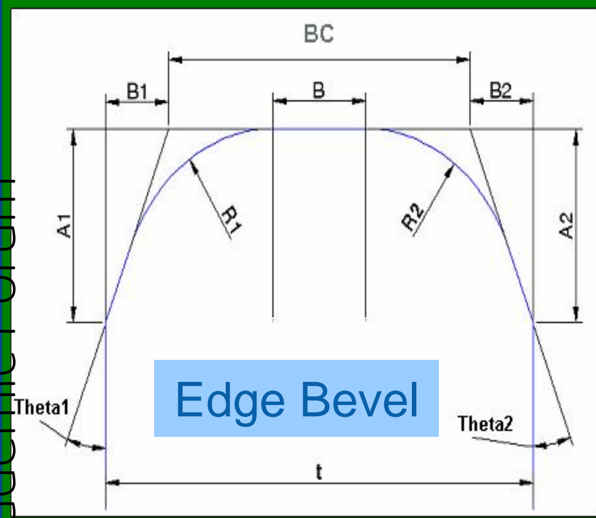
Past Challenges

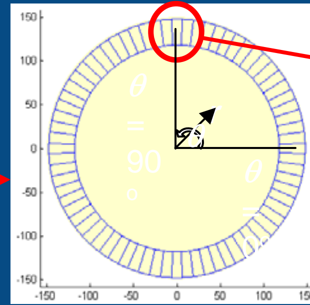
- HVM IC requires high quality silicon crystal. The silicon supplier technical efforts have been focused in the past on improving the crystal grow process:
  - crystallographic defect free crystals
  - reducing dopant elements variability
  - controlling oxygen concentration
- Defect engineering – harnessing thermal cycles and crystal defects to improve yield
- Epitaxial (Epi) film introduction enabled new opportunities in resistivity control and improved crystal quality.

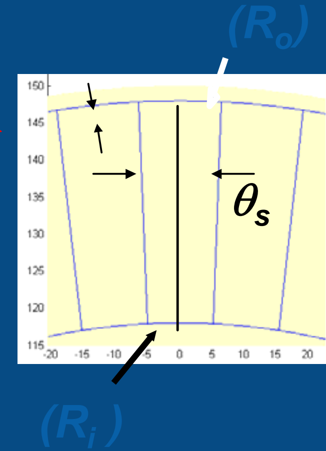
Present "State of the Art"

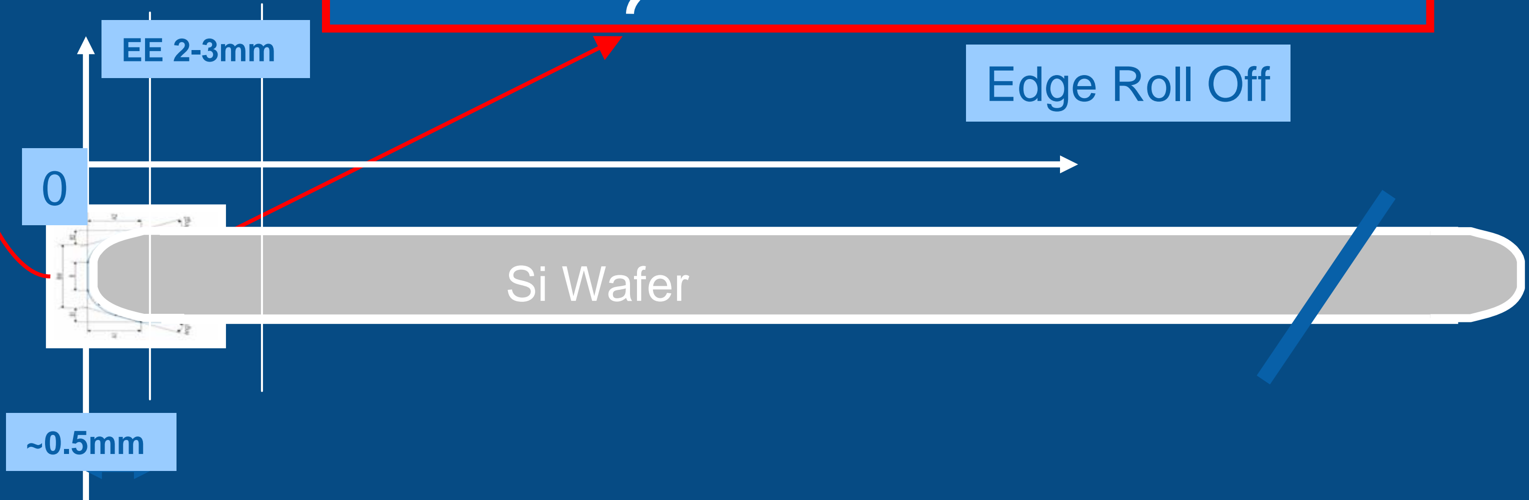
- 300mm ϕ DSP wafers are the wafers of choice for advanced IC manufacturing.
- CZ process is well understood, crystal quality is good and crystallographic issues seem to be well under control.
- Today the technical focus has shifted to mechanical aspects of wafer fabrication, driven by tight process requirements. There is a strong interaction between the wafer geometry and the IC process, and wafer topography, edge shape and edge roll-off have been identified as parameters affecting the yield.

Edge Description









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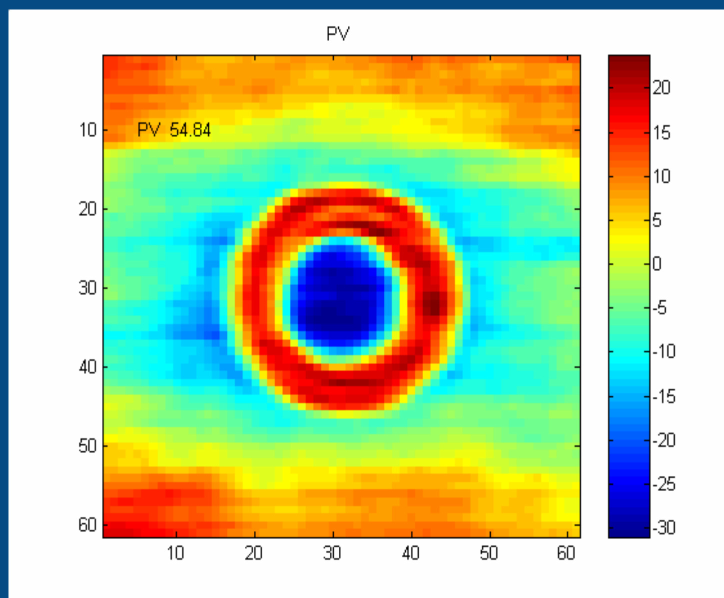
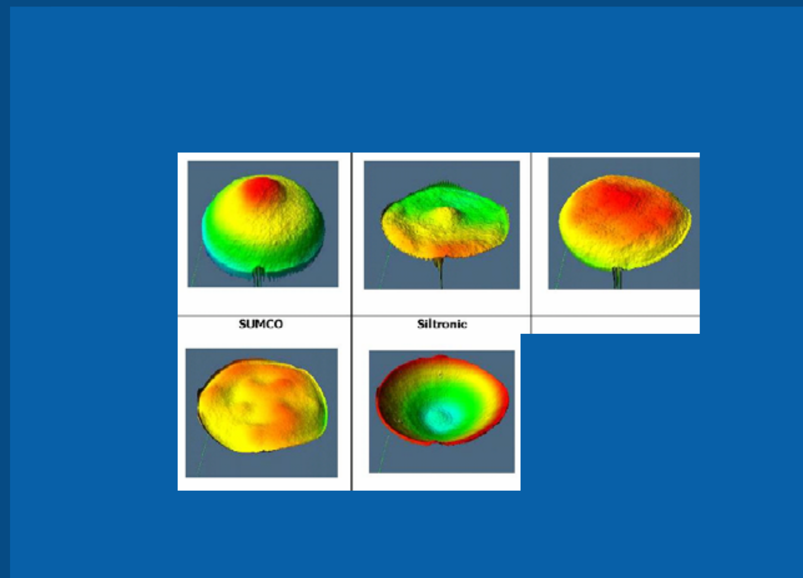
Wafer Geometry

Wafer topography and wafer shape have been shown to modulate manufacturing defects and yield.



A 54 nm PV thick ring detected at NT screening prevented a potential problem for litho



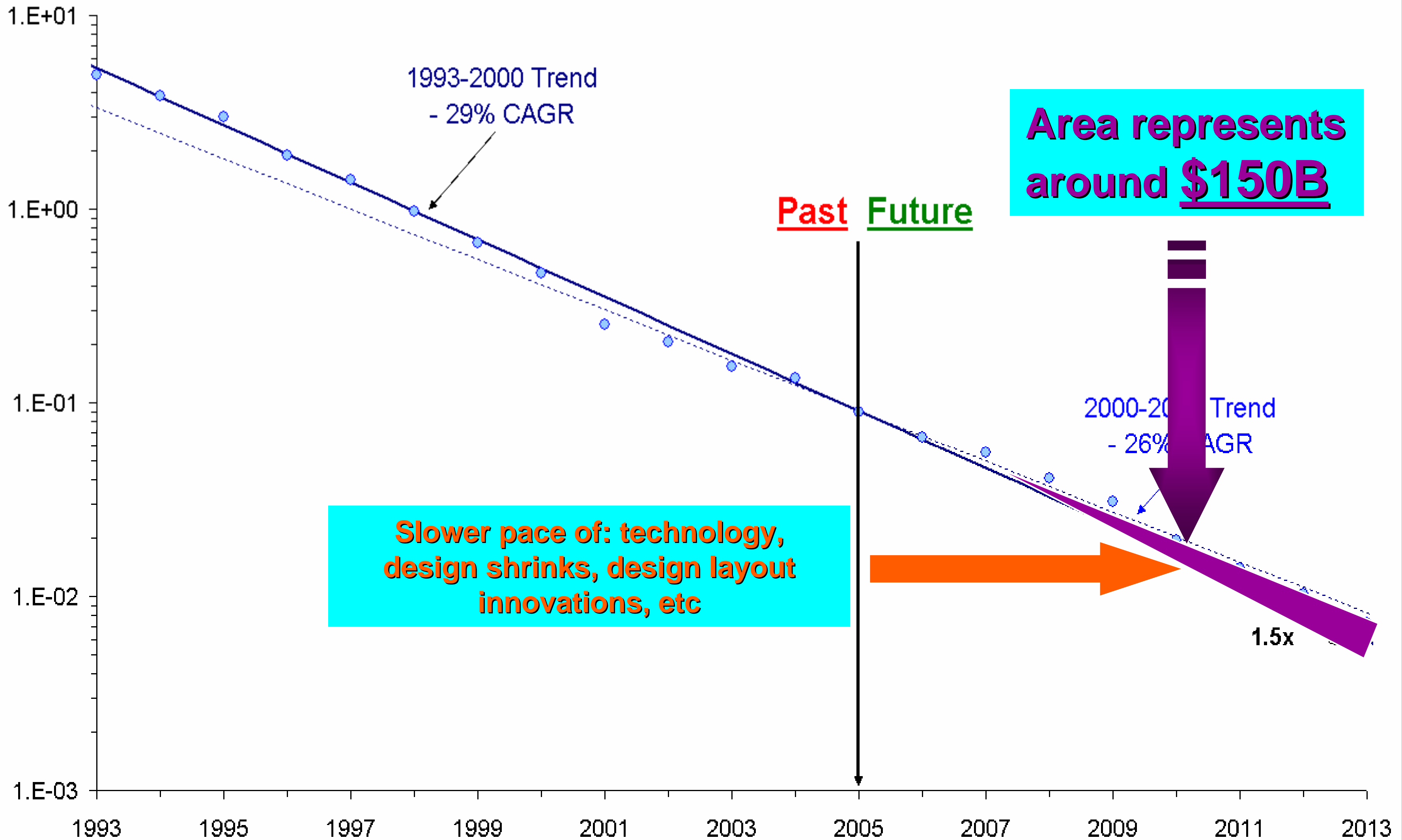
3D global shape images of typical 300mm wafers manufactured by different suppliers

What To Expect Next

- Tougher geometry requirements:
  - ERO specified
  - Edge profile well defined
  - Flatness tightened
- New types of wafers driven by designers effort to use the crystal properties as a leverage to enhance mobility and improve device performance.
  - FD-SOI
  - Change in crystal orientation
  - Hybrid wafers with new elements like: III-V and CNT (ITRS ERM)
- Next wafer size, ϕ450mm, driven by the economy of scaling.

  The transistor size shrinks and their density increases driving the cost reduction predicted by Moore Law, however the device area and the wafer cost increases with every new generation. To keep on the Moore Law curve a wafer size scaling is required every 4-5 generations.

ISMI Industry Economic Modeling - Productivity Trends



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ISMI Wafer Diameter Scenarios

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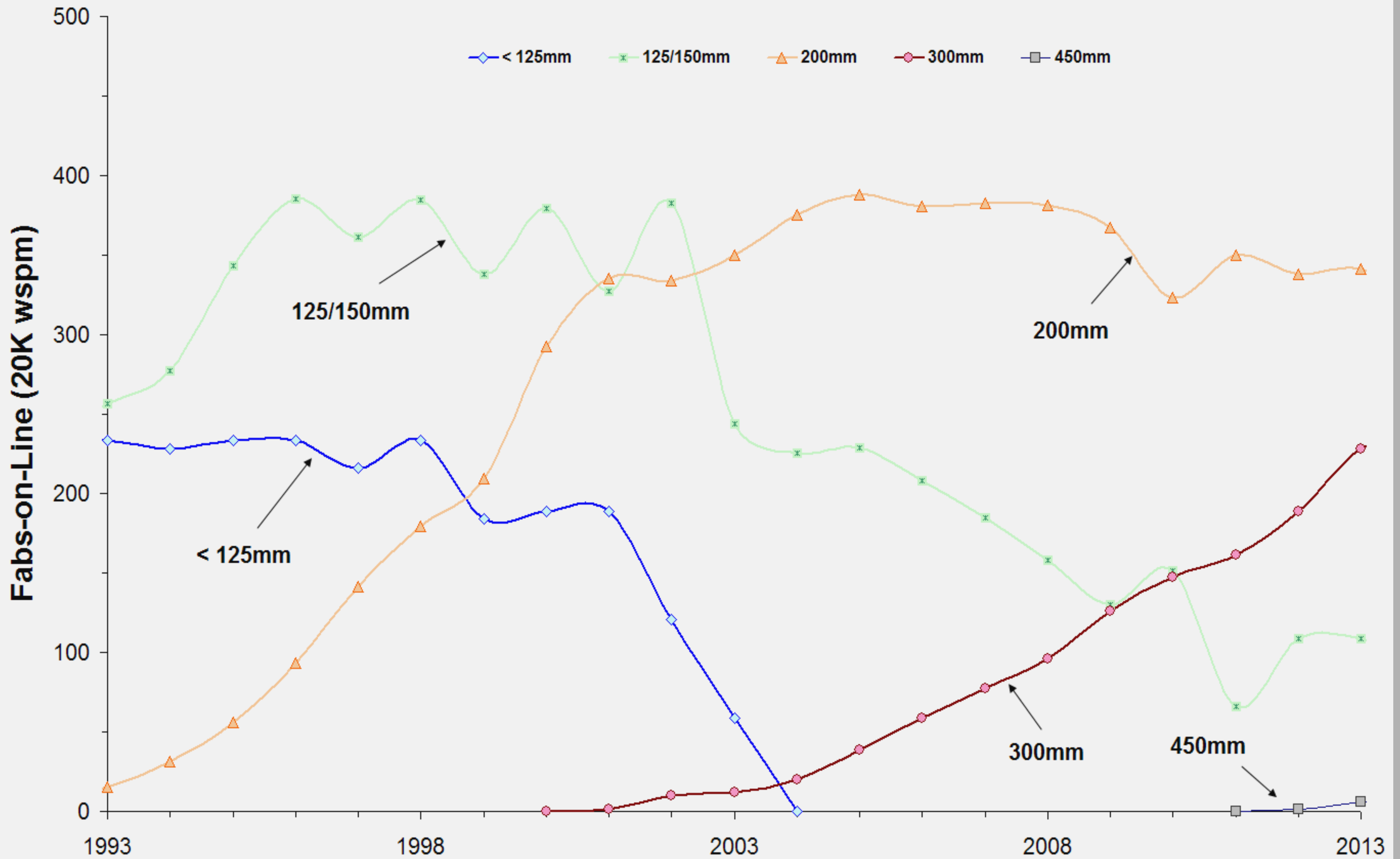


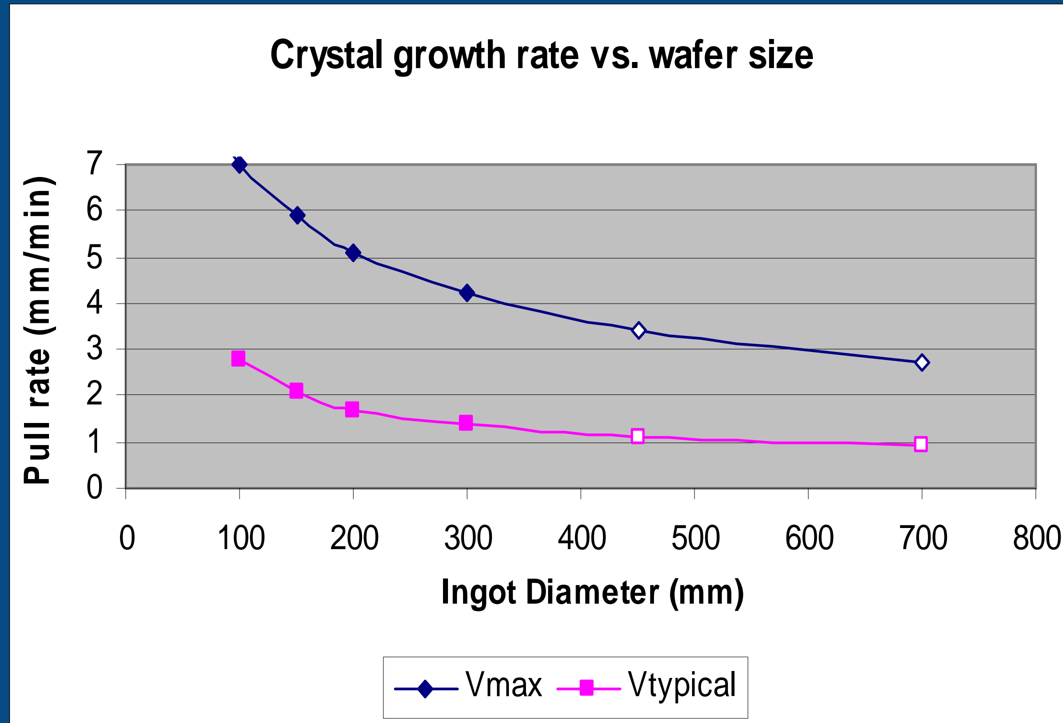
Large Diameter Silicon Wafers - Technical Challenges

- Crystal growth development will be the most demanding technically:
  - pull rate will be ~20% slower
  - time to grow the same length crystal almost double
  - the charge, compared to 300mm, ~2.4x bigger
  - crystal yield, for the same length crystal, lower

Crystal Growth Rate.

- $V_{max} = \left(L\rho \right) 2\sigma\varepsilon K_m T_m^{5} / 3R)^{1/2}$
  $\alpha \; R^{-1/2}$

  ε = emissivity
  ρ = density
  σ = Boltzmann const.
  L = latent heat of fusion
  T_m = Melting point temp.
  K_m = thermal conductivity



When the ingot diameter is increased by 50% the pull rate is reduce by ~20%.

- Typical pulling rate is ~25%-35% of V_{max}.

For the same crystal length, crystal pull time for a 450mm ingot is expected to be almost double that of 300mm.

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Yield vs Wafer Size

450mm crystal is expected to yield lower than 300mm ingot.
A 450mm crystal with a 95% yield has to be ~3m long and weight ~1300kg. A more realistic situation is of a 1.5 meter long crystal requiring a 700-800kg charge.

Yield vs. wafer size

Crystal yield (%)

100%
95%
90%
85%

0
100
200
300
400
500

Wafer size (mm)

1 m long
1.5 m long
GRC
3 m long

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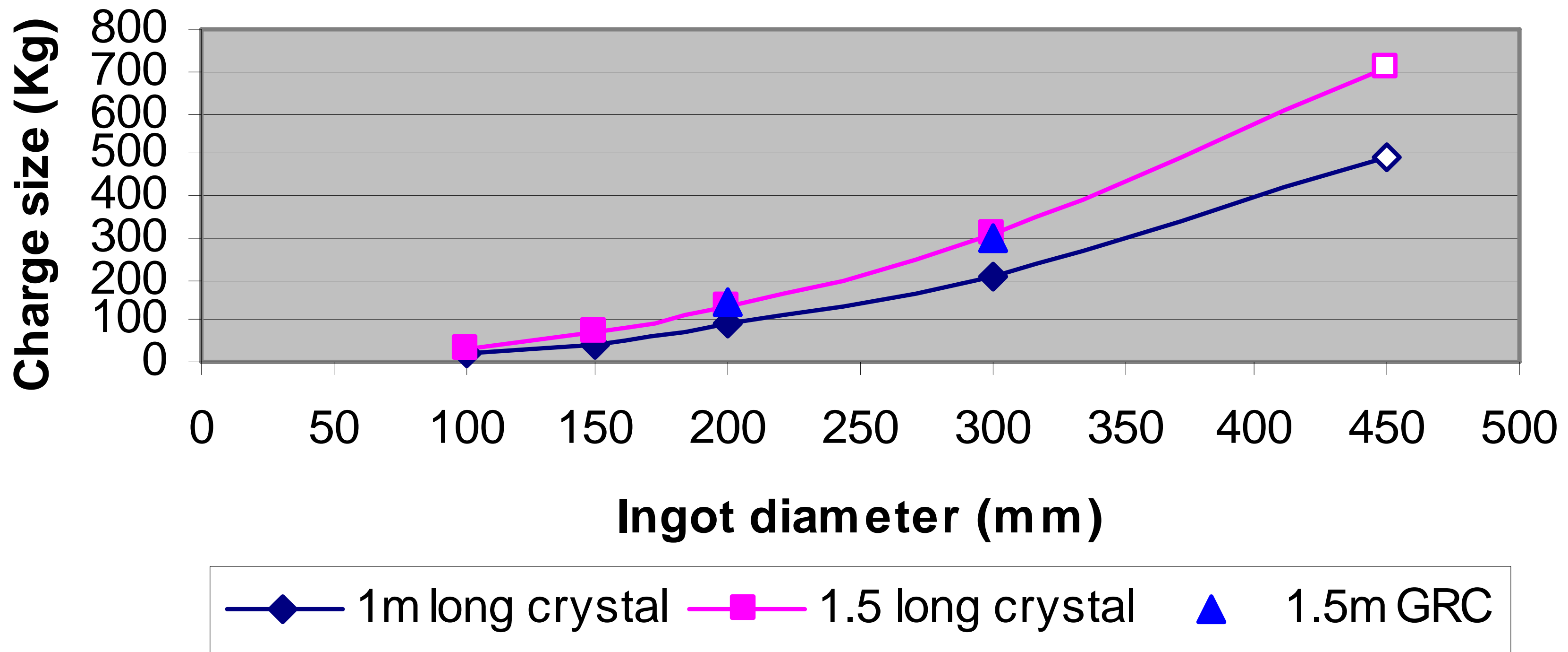
Charge Size vs. Wafer Size



450mm size will require a polysilicon charge ~2.4x larger than 300mm to grow the same crystal length.

Technical Challenges (II)

- Crystal pulling equipment design optimization for the bigger size:
  - Safety
  - Bigger and heavier crucibles
  - Larger hot zones
  - Larger melt convection
  - Heat shielding
- Ingot slicing development:
  - Wafer shape control
  - Manufacturability
- Wafer shaping processes (grind, polish, CMP) development with equal or better capability than 300mm over a 2X+ increase in surface area.
- Metrology capability

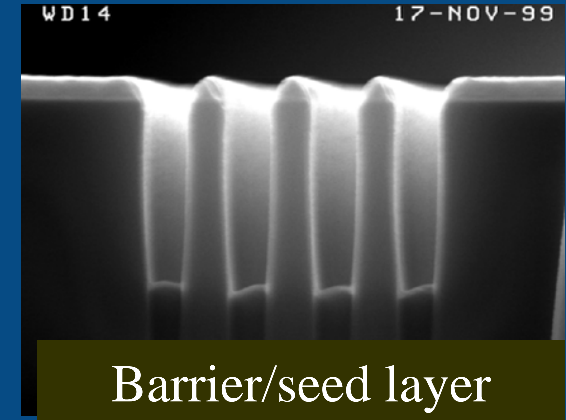
The biggest challenge for the suppliers is to be ready to intercept the ITRS specs required by the technology node present at the time of 450mm wafer insertion.

Metallization Environment

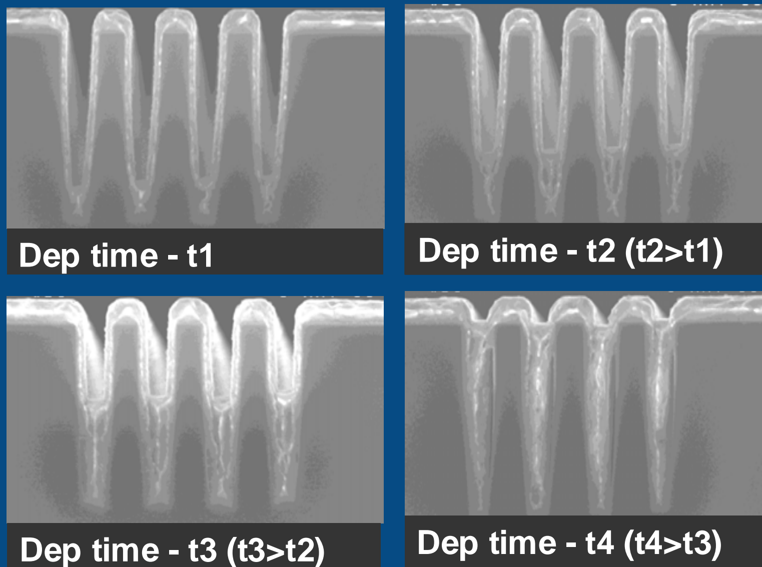
- Interconnects became the dominating timing delay factor.
- The metallization environment is following the same trends as the transistor scaling - increased complexity, thinner more closely packed metal lines with increased number of metal levels.
- Cu dual damascene is the current the state-of- the-art technology.
- Al alloys replacement by Cu, with ~40% reduction in resistivity and improved reliability, enabled the prolonging of the current wiring technology lifetime by about a decade.
- The metallization is an integral part of the process. It is impacted by lithography, patterning, CMP, cleaning and thermal treatment and is strongly affecting the low k integration.

Typical Cu Metallization Process

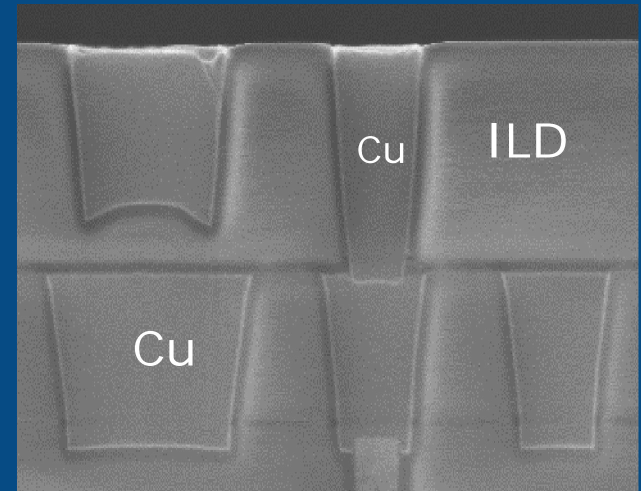
- Ta/TaN diffusion barrier sputtering.
- Cu seed sputtering.
- Dual damascene Cu electroplating
- CMP



Barrier/seed layer



Superfill behavior of Cu electroplating



Dual damascene Cu

Metallization Scaling

- Current wiring technology is approaching end of life for the lower metal layers. Cu resistivity does not scale linearly. It increases due to line-edge and line-width roughness, grain boundaries and impurities scattering
- Novel interconnect approaches are considered for the lower metal layers, with CNT and Optical interconnects being the leading candidates.

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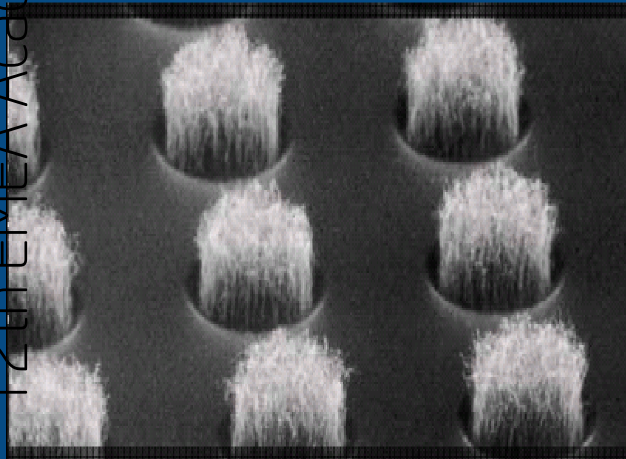
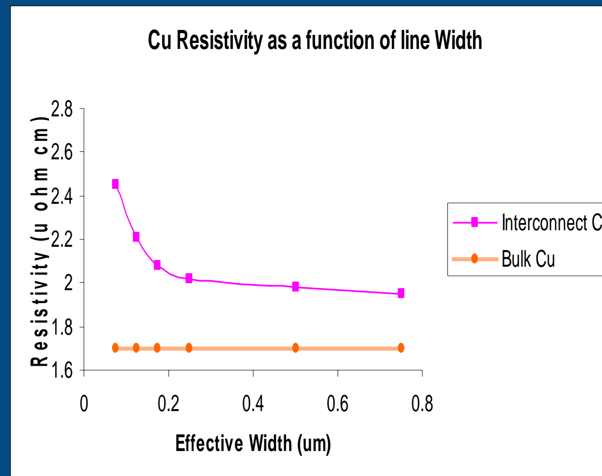
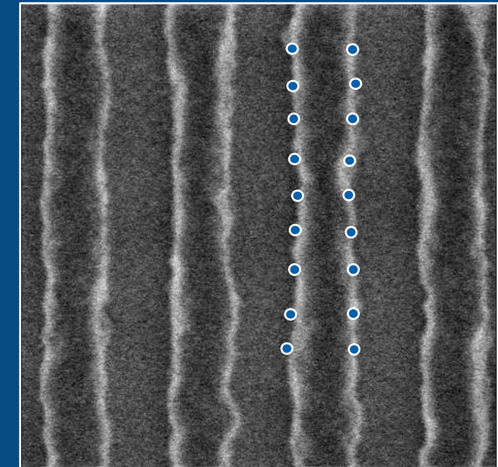


CNT vias. Courtesy of Y Awano (Fujitsu) ITRS ERM meeting 2007





Line-Edge and Linewidth Roughness
Courtesy of A. Ymaguchi (Hitachi) ITRS spring 07

Metallization Scaling (II)

- Current Cu metallization process will continue to be the preferred solution for the higher metal layers, however the continued dimension scaling and the bigger wafer size are expected to increase the process complexity:
  - The Cu seed integrity will become much more difficult to control.
  - The wafer size increase and the barrier and seed thickness reduction will create large center to edge potential gradients on the wafer
  - Line dimensions shrinkage will dramatically reduce the volume available for plating

Challenges and Opportunities

- The transition to 450mm diameter wafers will encounter a lot of engineering challenges. No fundamental physical "hard stoppers" are expected however academic work has the opportunity to play a major contribution through innovative ideas and basic studies.
- Following is a very short, tentative review of potential areas requiring support and open to innovative approach:

  - crystal pulling
  - wafer geometry
  - metallization
  - CMP

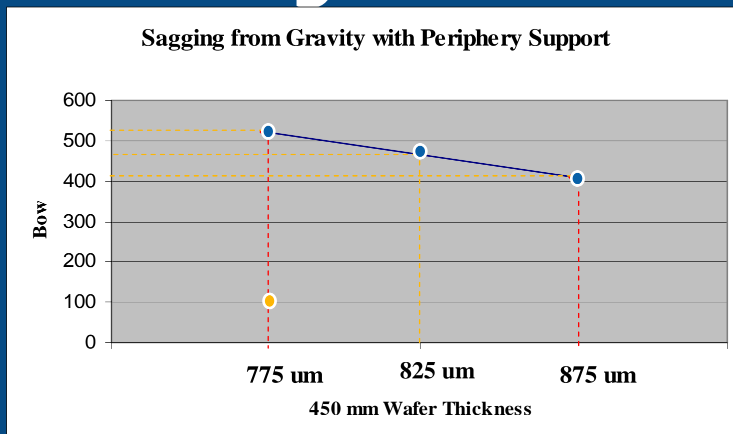
Crystal Pulling

- Modeling to optimize the time, crystal perfection and doping elements distribution.
- Crystal support to prevent dislocation generation at the neck
- Crucible material to support the heavy silicon melt for the duration of the crystal growth.
- Alternative solution - a continuous crystal growth process

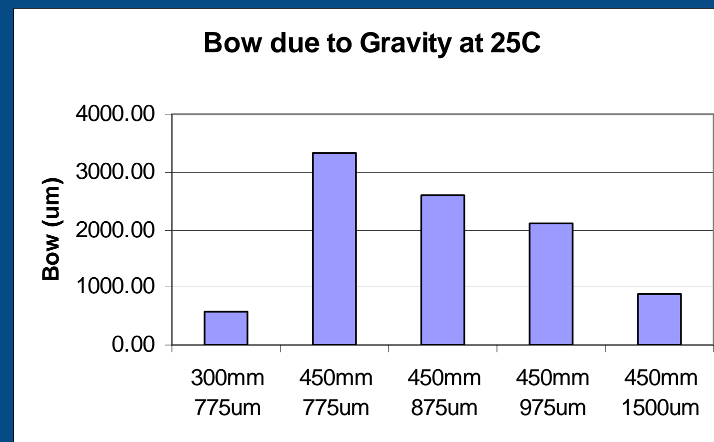
Wafer Manufacturing

- Wafer thickness have to be optimized.
  - IC process simulation predict wafer thickness of 825μm, with wafer stress being ~3X higher than that of 300mm wafers and bow from gravity impacted mainly by wafer support.
  - No modeling for wafer manufacturing and handling is available
- The current challenges affecting the wafer geometry are expected to be amplified by the tighter requirements and by the larger area of the wafer. ERO will be especially affected:
  - As shown in previous studies the maximum stress position during silicon wafer CMP was moving toward the center when the diameter was increased.
  - Larger wafer bow will impact polishing pressure at the wafer edge.
  - Pad temperature increases with the increased wafer size, pad modulus decreases generating a significant increase in the COF.

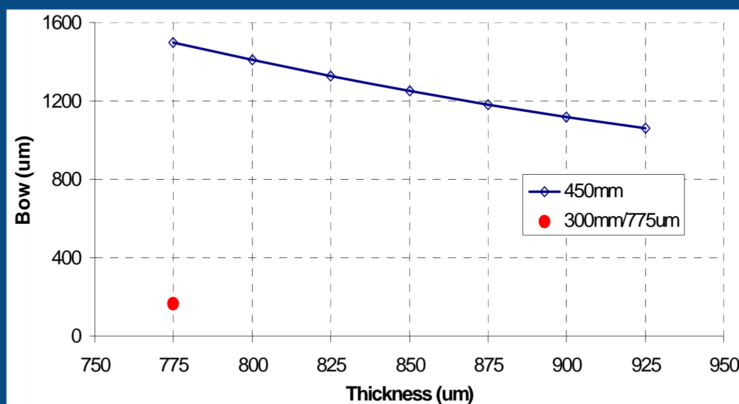
Gravity Bow vs. Wafer Thickness



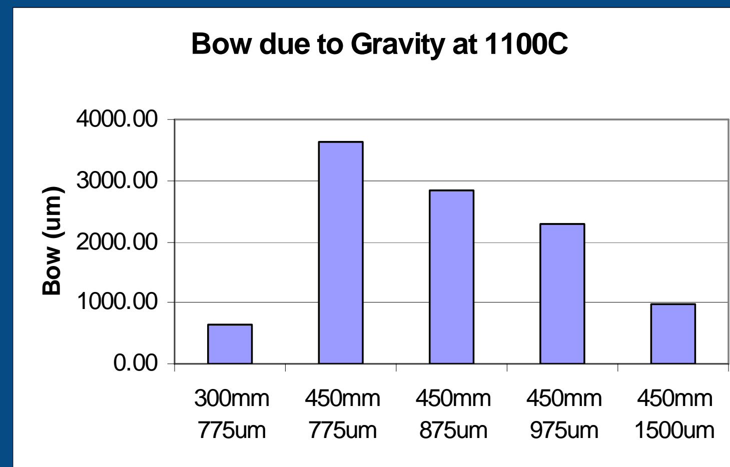
Room temperature
Full periphery support



Room temperature
3-point support

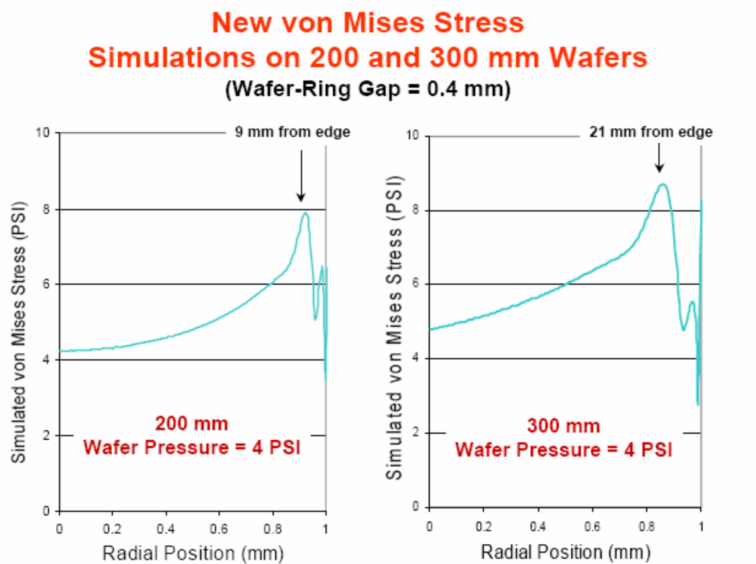


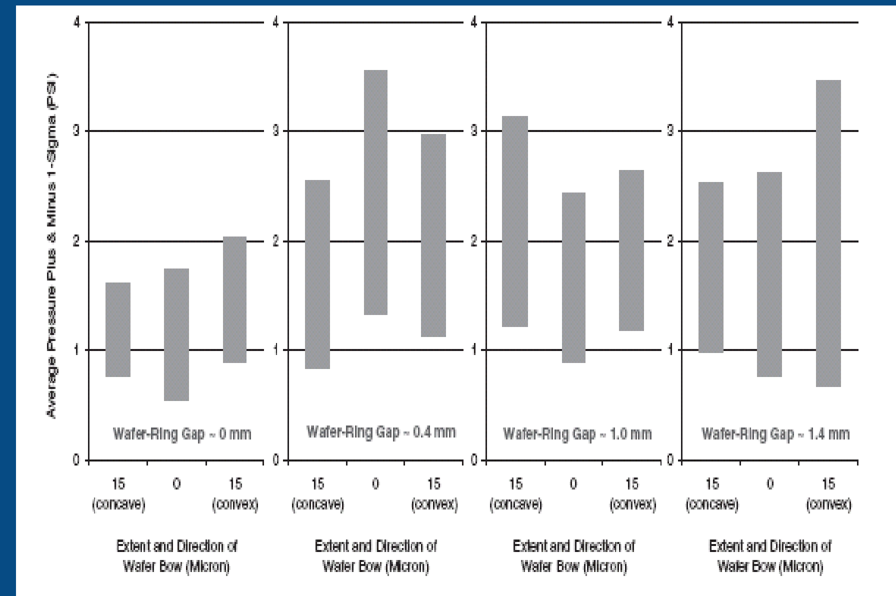
Room temperature
FOSB support



1100^0c 3-point support

Silicon Wafers CMP

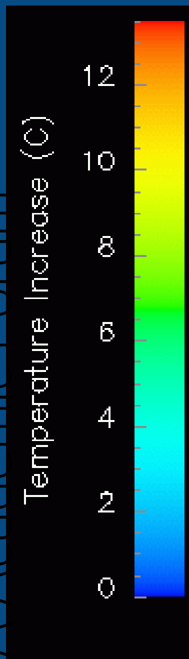


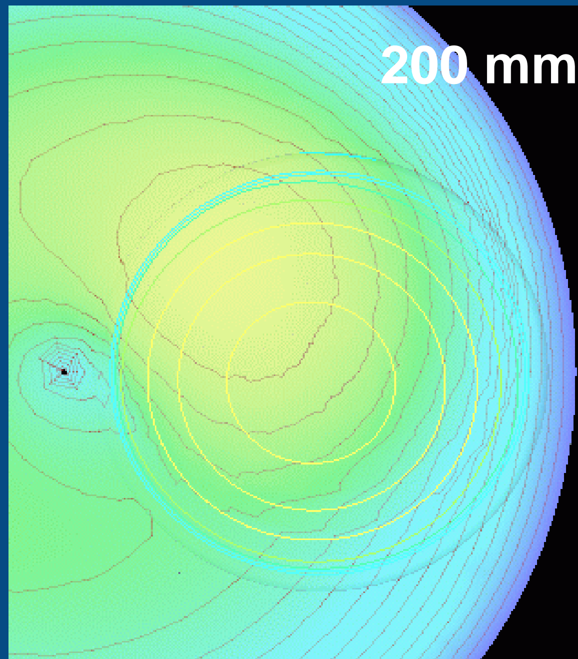


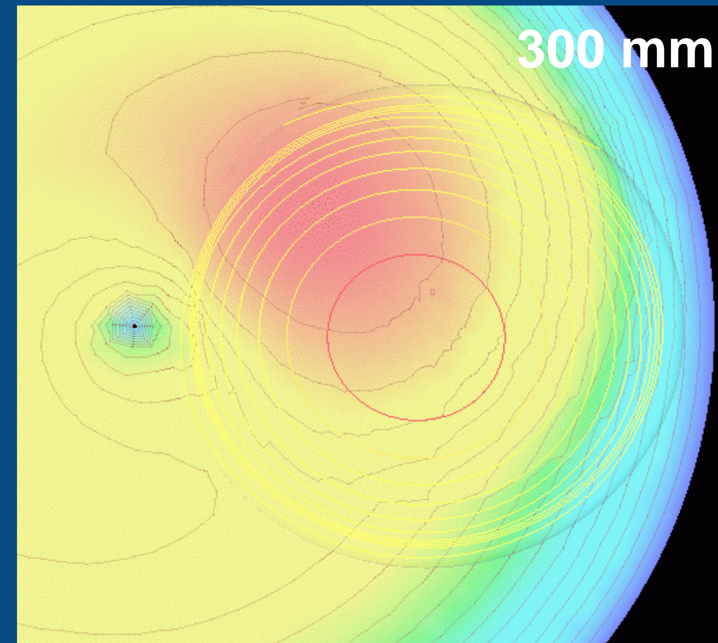
- J. Sorooshian et al, JSPE Planarization
- and CMP meeting San Francisco (July 2002)

- J. Sorooshian et al, Jpn. J. Appl. Phys., 42(2003), 6363

Pad Temperature Effect







A. Philipossian, CMPMIC 2007

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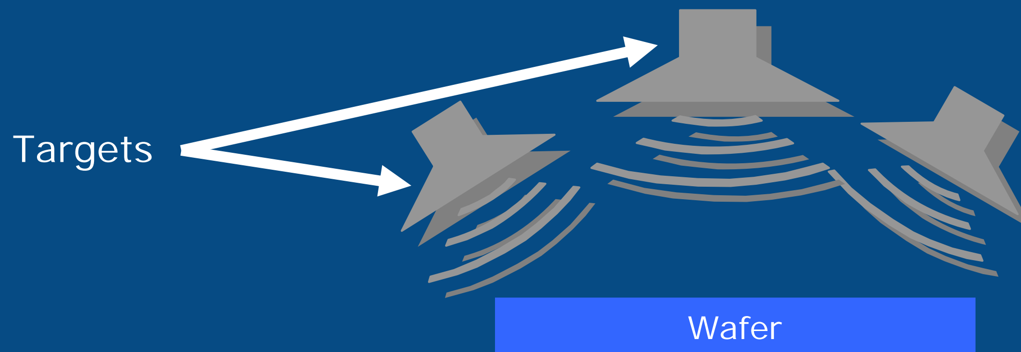
Pad temperature increase leads to a proportionate decrease in its modulus - E
10°C increase in T, leads to ~ 15% drop in E
A decrease in pad modulus (E) can result in a significantly higher COF.
COF α $E^{-0.36}$
A higher coefficient of friction in turn further increases the pad temperature during the process

Metallization

- Sputtering – in need for innovation:

  If the scaling-up trend used in the 200 to 300mm transition will continue for the 450mm wafers, we will be working in the next generation with monstrous targets (Ta targets weighting ~100 Kg). A different, innovative approach is required; for example good modeling and understanding of sputtering profiles may enable the same metal coverage by a number of small, well position targets.

- Electroless plating
  - A potential solution to overcome the large potential gradients on the wafer
  - A seed repair solution



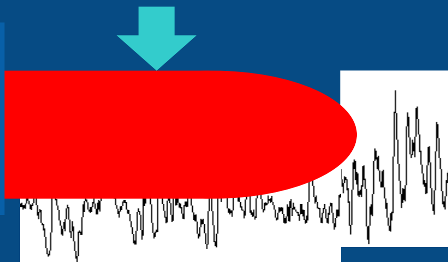
CMP

- Cu CMP is expected to be the most affected by changes in wafer geometry and by the larger wafer size.
  - There is a strong correlation between wafer edge shape and COF, ~25% difference when polishing Cu films on round bevel or square bevel edged wafers.
  - Cu Removal Rate is a function of both chemical and mechanical attributes of the CMP process. Wafer size scaling from 200mm wafers to 300mm wafers indicated frictional, thermal and kinetic changes of CMP process attributes. This trend is expected to continue to the 450mm wafers.

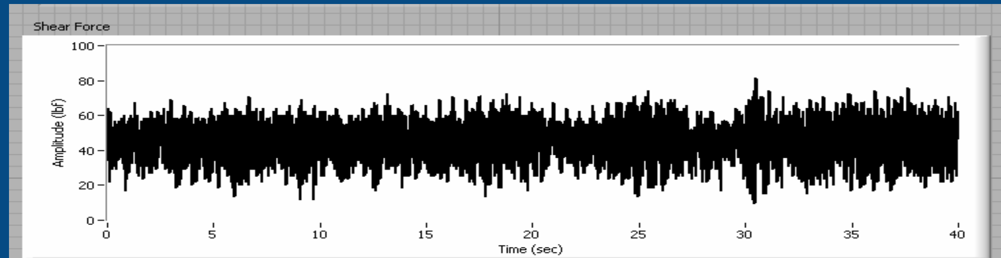
    The reaction temperature (i.e. true wafer surface temperature) increases significantly as wafer size is increased due to the higher pad temperature and higher COF. Wafer surface reaction temperature increase leads to a higher chemical reaction rate for larger size wafers. This not only increases removal rate, but it also shifts the balance between chemical and mechanical actions.

Copper CMP – Edge Shape Effect

2 PSI ; 1.2 m/s ; Fujimi PL-7102 ; R&H IC1000

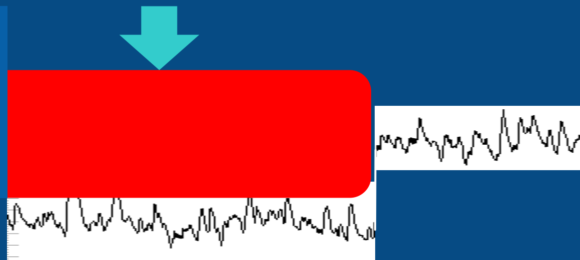


Wafer with Round Bevel

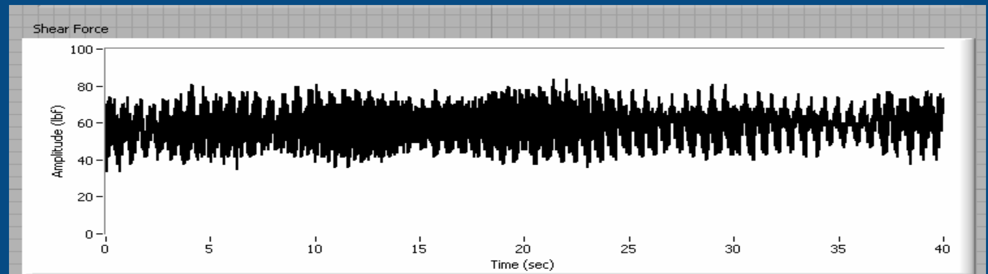


Variance of Shear Force = 84.641 lb_f^2

COF = 0.461



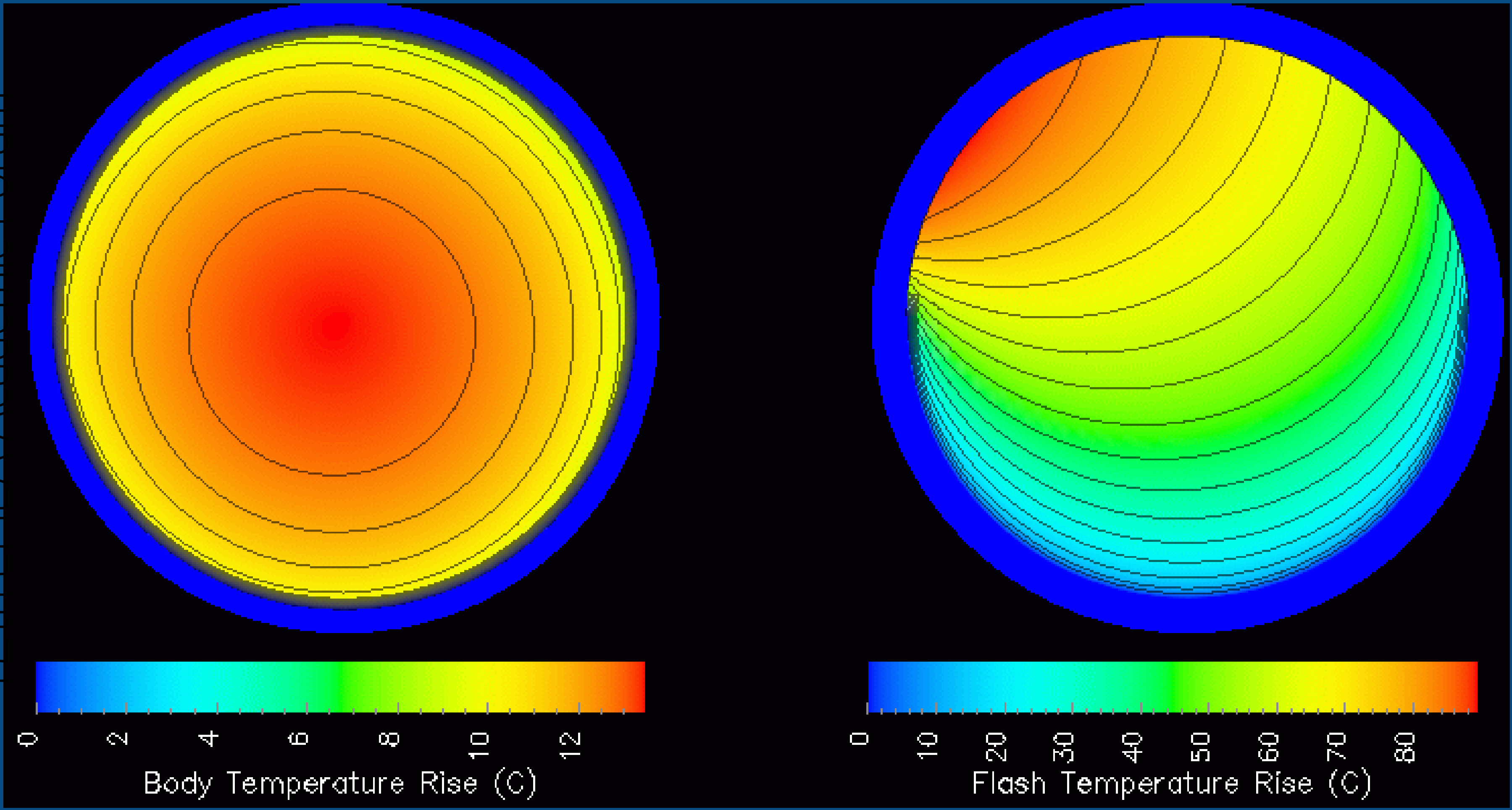
Wafer with Square Bevel



Variance of Shear Force = 72.096 lb_f^2

COF = 0.586

Pad Contact vs. Body Temperature
300 mm



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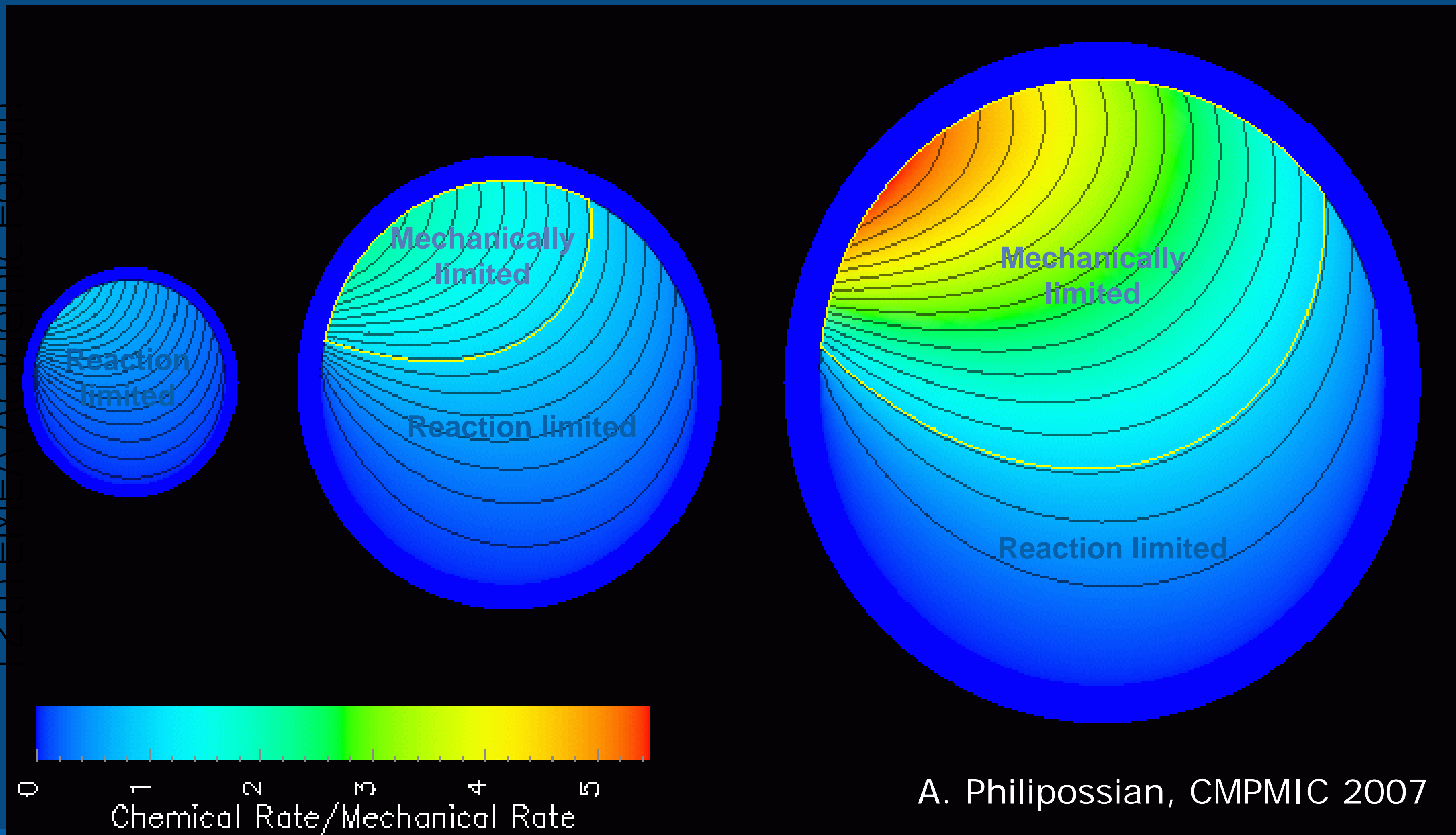
Copper CMP Processes
Chemical and Mechanical Rate



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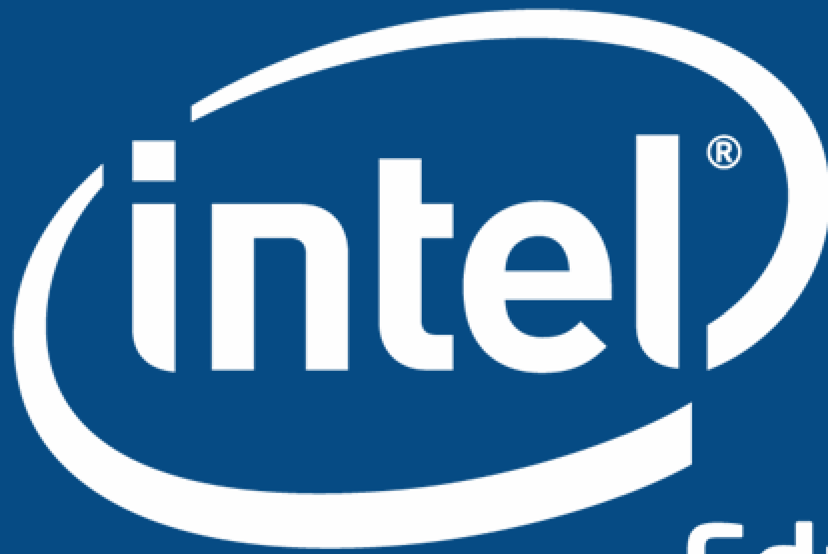
Summary

- Moving to 450mm diameter silicon wafers at the beginning of the next decade will be a challenging transition. The 450mm wafer insertion will have to intercept the spec requirements of the technology node present at the time of the introduction.
- No fundamental physical “hard stoppers” are expected however academic work has the opportunity to play a major contribution through innovative ideas and basic studies.
- The academia has always been a leader in modeling, basic process studies and characterization method development. Work on the next generation wafers is in progress and you are invited to join it. Some areas of the large diameter wafers requiring innovative solutions have been reviewed, however this is just “the tip of the iceberg” and the field is open to novel ideas.



Education