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FORUM

Technical Overview of the 45nm Next Generation Intel® Core™ Microarchitecture (Penryn)

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June 13, 2007

Based on Stephen Fischer's 4/2006 Intel Developer Forum (IDF) talk


2007
15 17:38

IDC – Israel Development Center

Located on Israel's Mediterranean coast, Haifa is the home of Intel's Israel Development Center (IDC).

IDC was established in 1974, and is Intel's first development center outside the US. The center is a multi-disciplinary team, with close to 2000 employees.

Many of Intel's leading products were developed and originated at IDC.

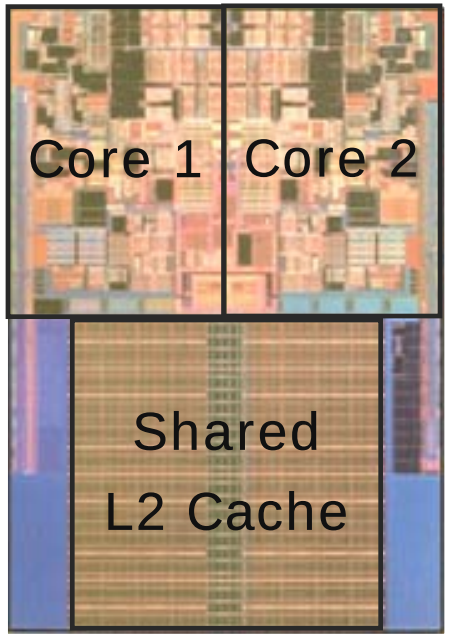
IDC's employees are currently working on Intel's future microprocessors, CAD tools, advanced networking components and software technologies.

Agenda

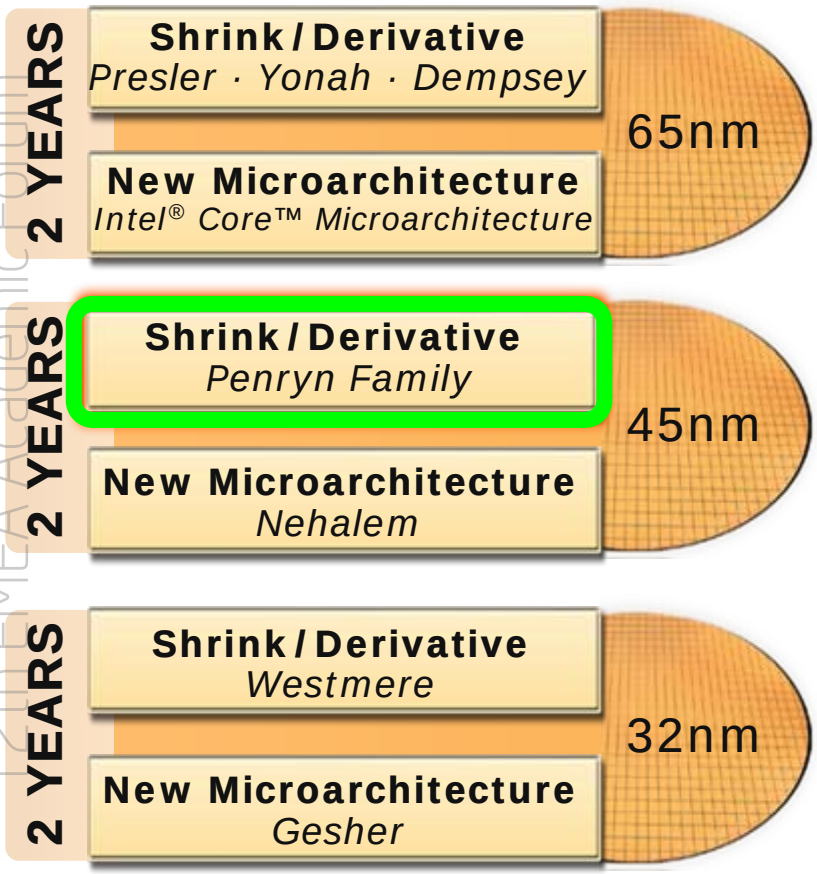
- Penryn Family Design Goals
- Processor Architecture Basics
- Intel® Core™ Microarchitecture Refresh
- Intel 45nm High-K Silicon Technology
- Enhancing the Intel® Core™ Microarchitecture
  - Microarchitecture Enhancements
  - New Intel® SSE4 Instructions
  - Power Management Enhancements
- Summary

Terminology

- Architecture/microarchitecture
  - Intel® Core™ Microarchitecture ➔ “Merom”
  - Enhanced Intel® Core™ Microarchitecture ➔ Penryn
- Products
  - Intel® Core™ 2 Dou processor (65nm) ➔ Merom/Conroe/Woodcrest
  - <no name> (45nm) ➔ Penryn
- Penryn is
  - Next generation based on “Merom” arch/microarch
  - It will have both dual core and quad core versions
  - The Dual core shares L2 cache



Penryn Family Design Goals



Extend leadership in performance and energy efficiency

- Increase performance per given clock cycle
- Increase processor frequencies
- Further gains in energy efficiency

Deliver lead product for 45nm High K + metal gate process technology

Deliver optimized processors across each segment and power envelope

- Mobile, desktop, workstation, and server segments

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Processor Architecture Basics

Delivered Performance = Frequency * Instructions Per Cycle (IPC)

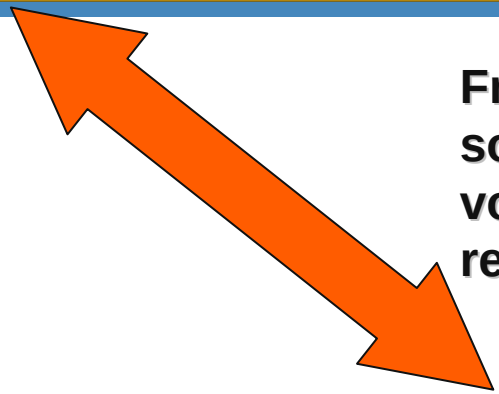
Goal is higher performance and lower power

Power = $C_{dynamic} \times V^2 \times$ Frequency

$C_{dynamic}$ is roughly a product of area and activity
*"how many bits" * "how much do they toggle"*

Processor Architecture Basics

Delivered Performance = Frequency * Instructions Per Cycle (IPC)



Frequency is proportional to voltage, so frequency reduction coupled with voltage reduction results in cubic reduction in power.

Power = $C_{dynamic} \times V^2 \times$ Frequency

Processor Architecture Basics

Delivered Performance = Frequency * Instructions Per Cycle (IPC)

Higher IPC usually results in wider data paths and/or more speculation : directly increasing C dynamic

Power = $C_{dynamic} \times V^2 \times$ Frequency

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Intel® Core™ Microarchitecture Refresh

Intel® Wide Dynamic Execution

4 instructions per clock cycle vs. 3;
14 Stage Pipe, Micro and Macro Fusion, Enhanced ALUs

Intel® Advanced Smart Cache

Each core pair can access shared L2 cache;

Intel® Smart Memory Access

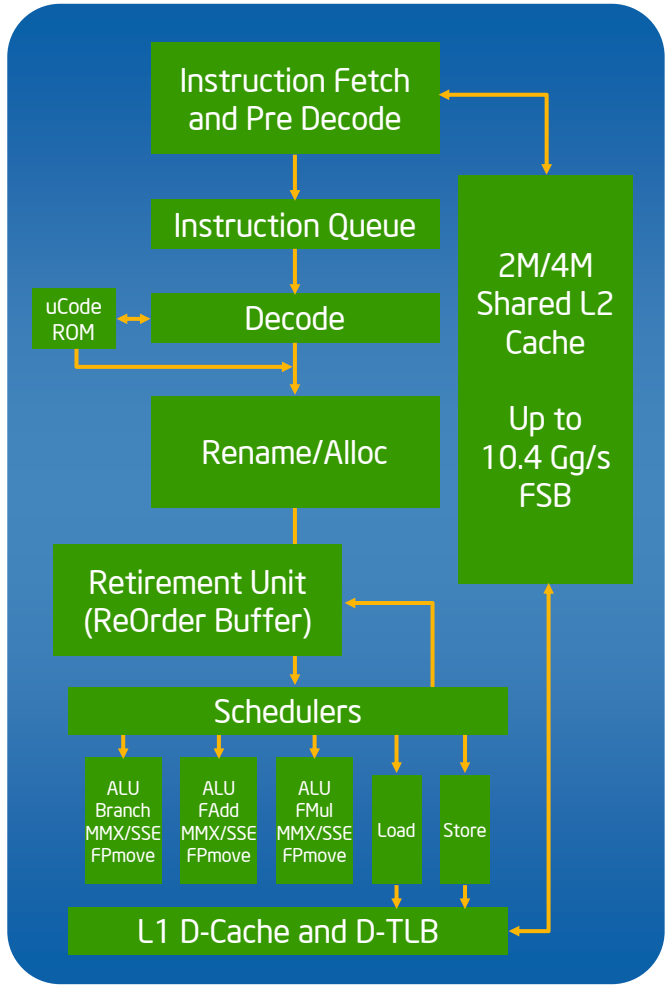
HW based Mem Disambiguation: "Load" can pass "Store";
Improved Prefetchers: Hiding latency to memory subsystem

Intel® Advanced Digital Media Boost

128 bit Single cycle SSE

Intel® Intelligent Power Capability

Ultra fine grain power control;
Split bus for varying data width;
Platform level power management



'Each Core'

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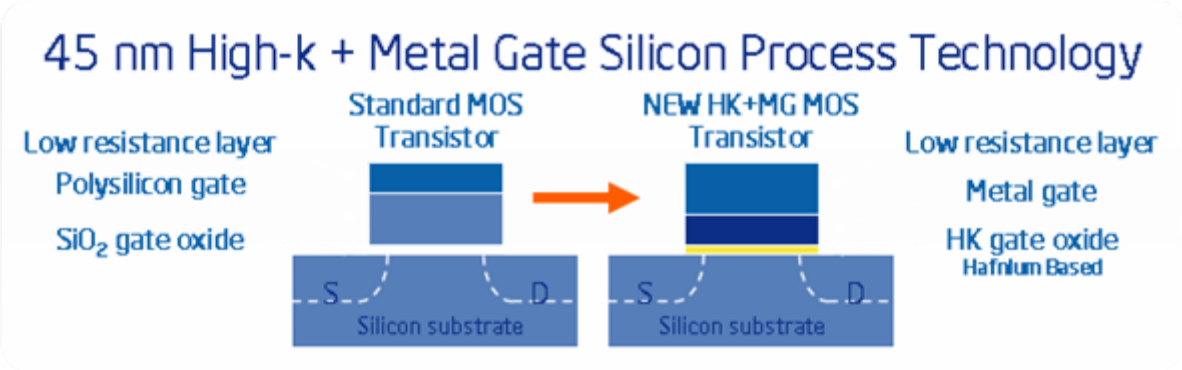
Next Generation Intel 45 nm High-k Process Technology



- ~2x larger transistor budget provides freedom to add new features and higher performance with cost effective die sizes
- >20% faster transistor switching speed delivers higher core speeds and increased instructions per second
- Lower leakage current reduces power consumption or enables more capability and performance within a given power envelope compared to 65nm processors

High-k example: Hafnium oxide (HfO2) k >20

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Enhanced Intel® Core™ Microarchitecture

Intel Core Microarchitecture	New with the Penryn Family
Intel® Wide Dynamic Execution	Fast Radix-16 Divider Faster OS Primitive Support Enhanced Intel Virtualization Technology
Intel® Advanced Smart Cache	Larger Caches: up to 12MB 24 Way Set Associativity
Intel® Smart Memory Access	Split Load Cache Enhancement Improved Store Forwarding Higher bus speeds
Intel® Adv Digital Media Boost	Intel SSE4 instructions Super Shuffle Engine
Intel® Intelligent Power Capability	Deep Power Down Technology Enhanced Intel Dynamic Acceleration Tech

Increased Performance and Energy Efficiency Across Applications

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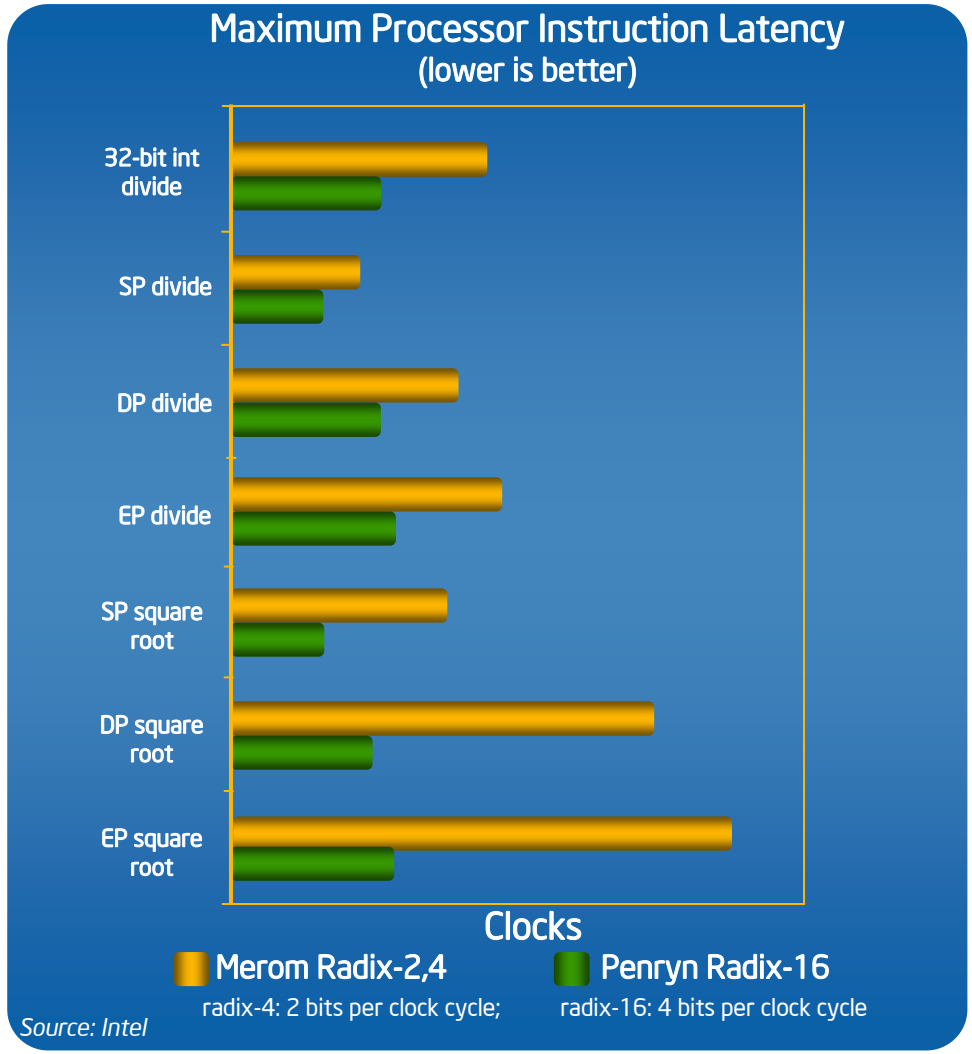
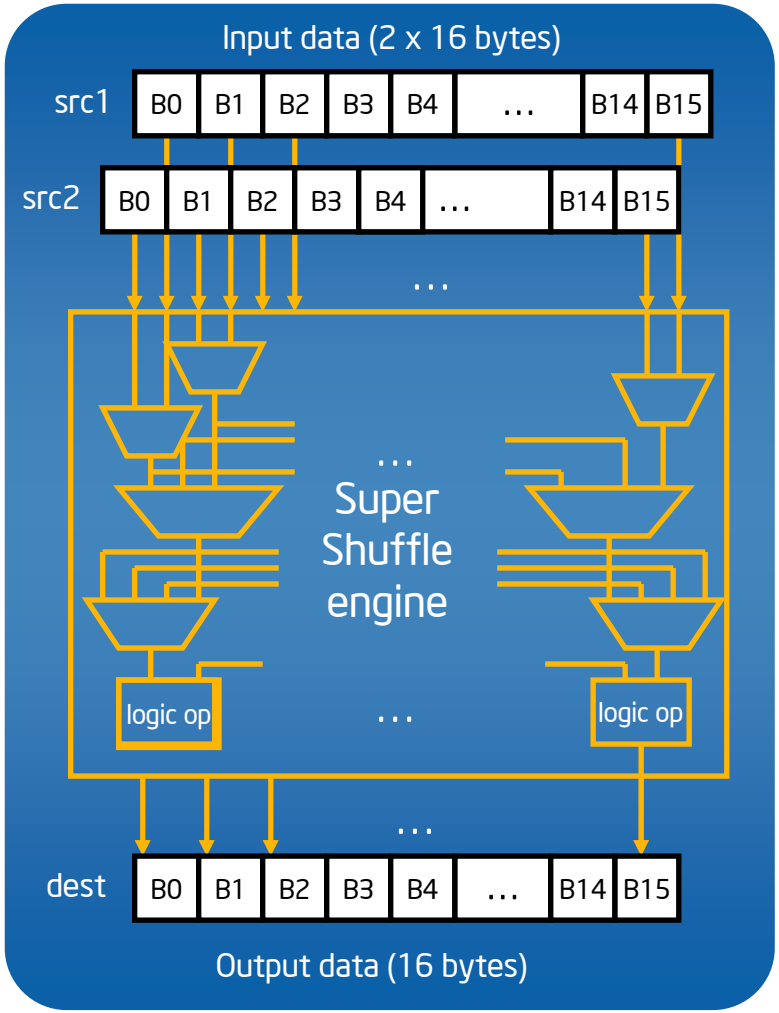
Fast Radix-16 Divider

- Leading edge divider performance
- 4 bits processed per cycle vs. 2 bits per cycle
- Innovative radix-16 based architecture
  - Utilized for both floating-point and integer operations
  - Optimized square root
- Early-out algorithm for both integer and FP data allows lower latency
  - 6 cycle minimum



On Avg: Doubles the Divide Execution Speed

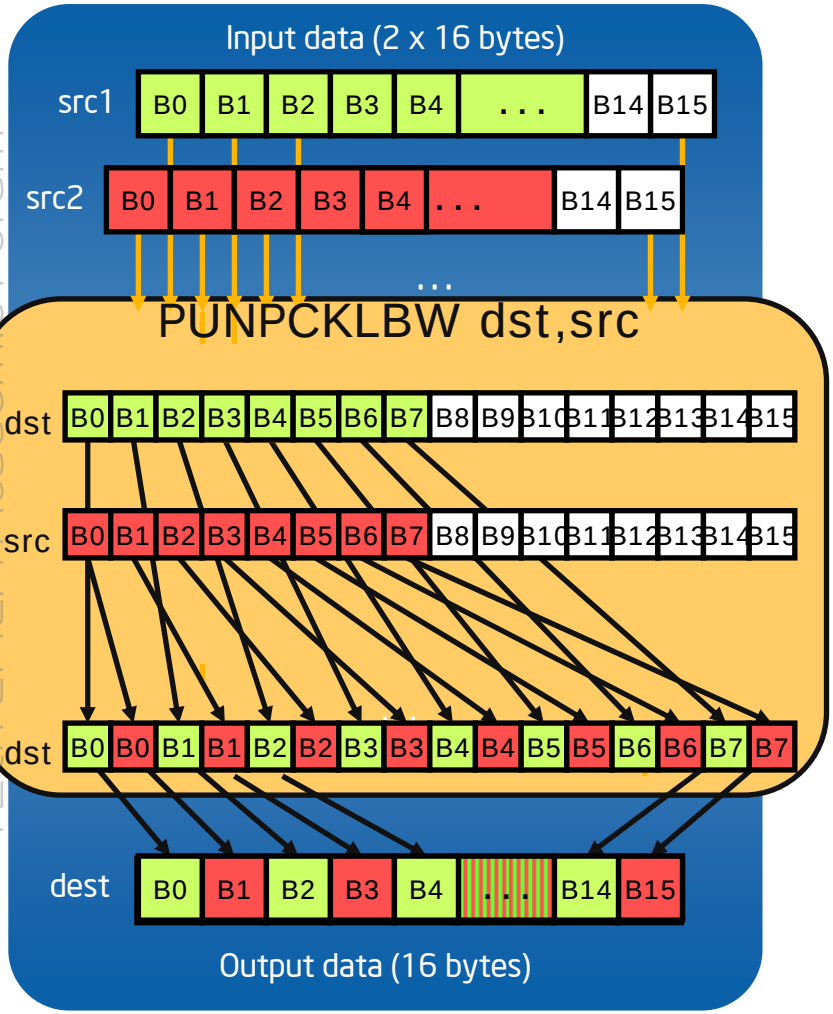
Super Shuffle Engine



- Shuffle operations required for SSE data formatting operations
  - Unpacking
  - Packing
  - Align concatenated sources
  - Wide shifts
  - Insertion and extraction
  - Setup for horizontal arithmetic functions
- Penryn super shuffle engine performs 128 bit operation in single cycle
- No software changes required

Doubles shuffle speed

Super Shuffle Engine



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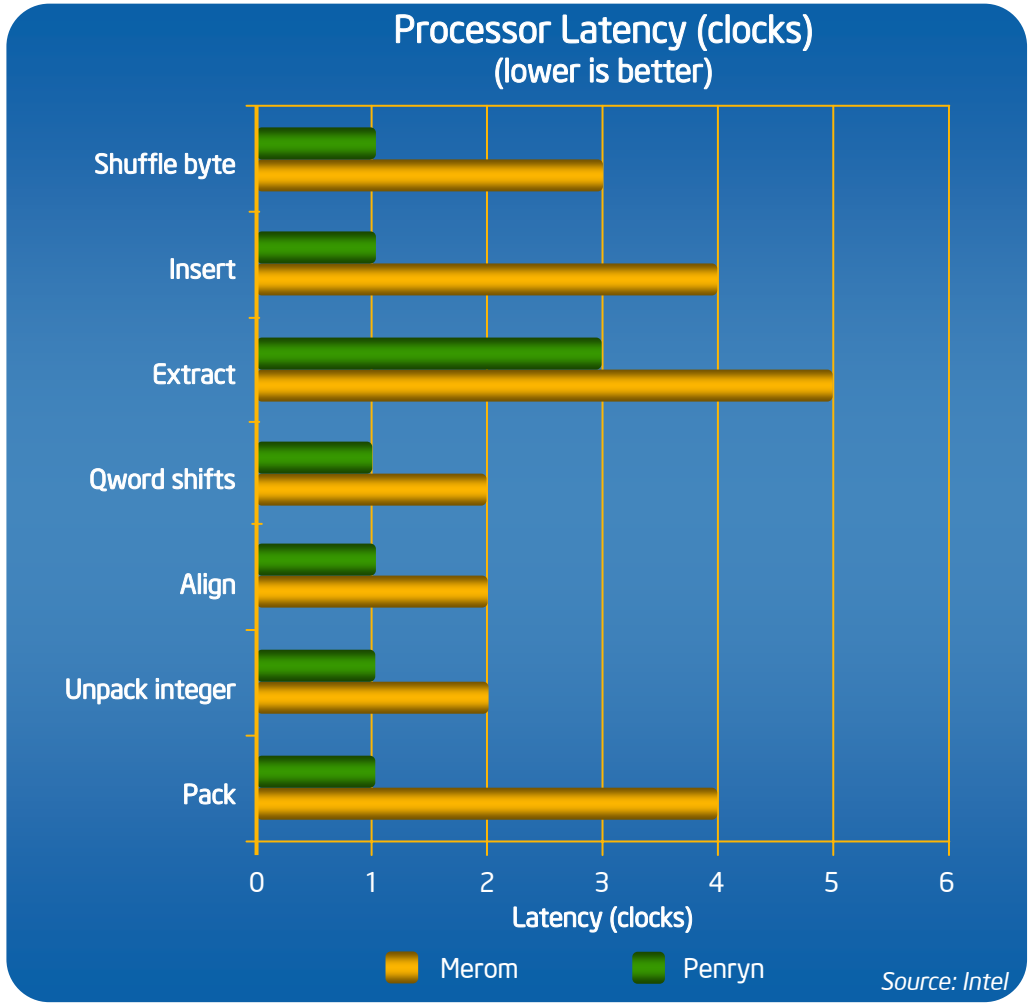
Doubles shuffle speed

Super Shuffle Engine

- Doubles the speed for most byte, word, and dword granular SSE data shuffle operations
- Also key capability for performance effective enabling of new SSE4 functionality
  - Blends
  - Dot product
  - Multiple sum-of-abs differences

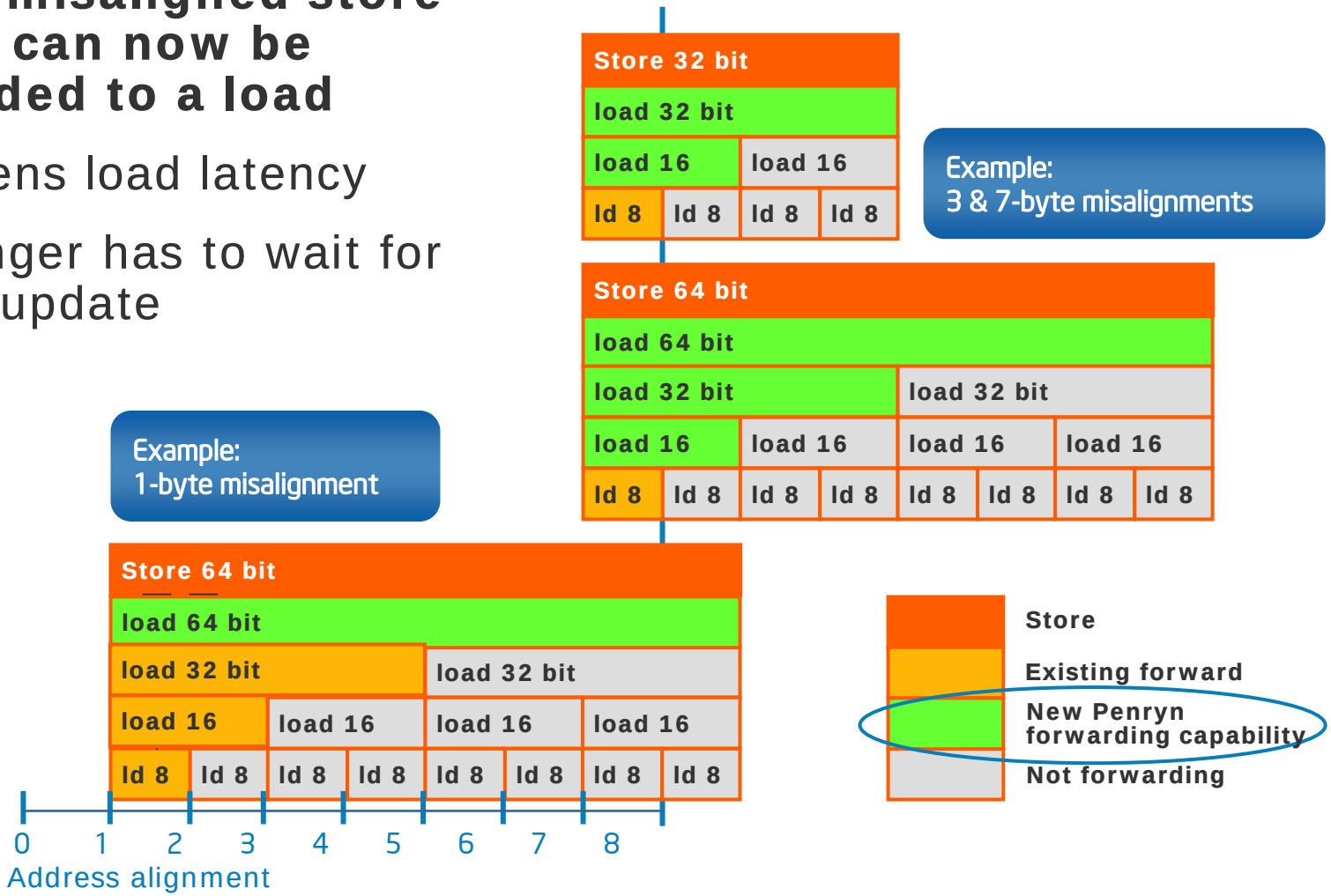


2X Faster SSE Shuffle Instruction Execution

Store Forwarding: Misaligned Store

8-byte misaligned store results can now be forwarded to a load

- Shortens load latency
- No longer has to wait for cache update



Improved OS Synchronization Primitive Performance

- Faster locked instruction performance
  - Key primitive for multiple thread synchronization
    - > Faster locks enable more concurrency between threads
  - Up to **55-80%** faster

- Faster interrupt masking control
  - Execution time critical to OS for shared resource control
  - Uarch improvements to eliminate pipeline stalls in the common case
  - CLI/STI instrs as much as **2X** faster

Example spin lock sequence:

Used for controlling access to shared resources (i.e. I/O, kernel state)

Applicable for MT/MP OS env

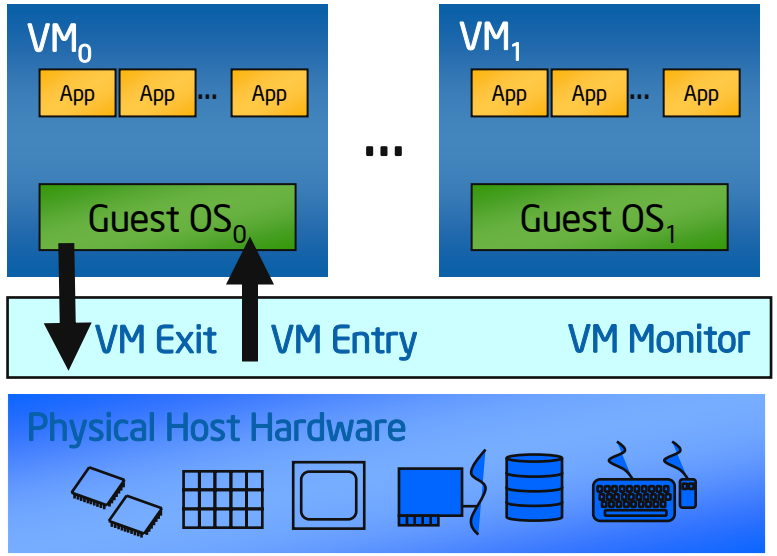
```
spin_lock:
  lock dec [edi]    ;atomic decrement
  jns lock_acquired  ;exit if lock was 1
spin:
  pause             ;otherwise loop until
  cmp [edi], 0      ; lock is released
  jle spin
  jmp spin_lock     ;try to reacquire lock
lock_acquired:
  ret
```

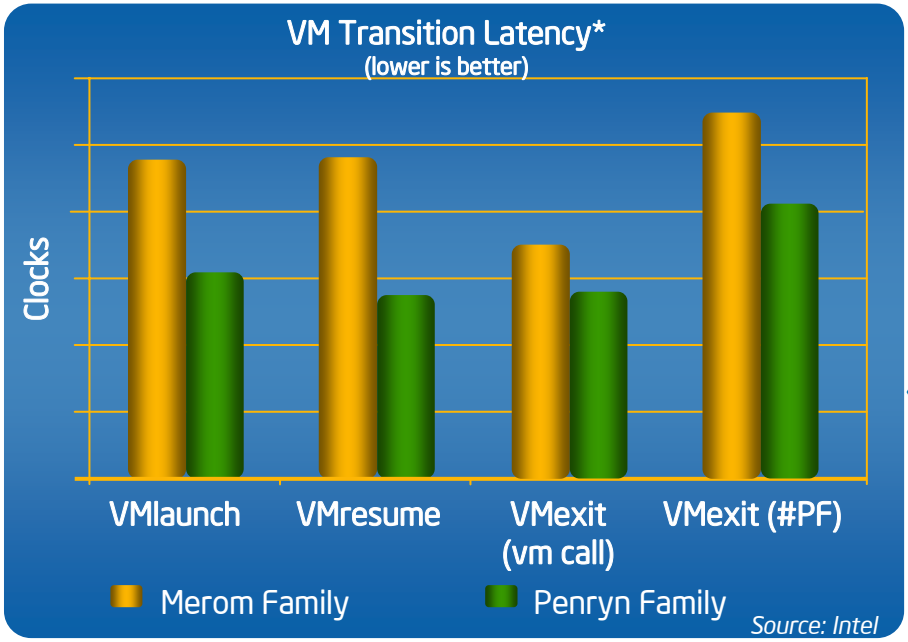
- Faster access of Time Stamp Counter
  - RDTSC instr as much as **3X** faster
  - Key functionality for database servers, OS time-of-day services frequent in transaction processing

Improves Server Performance Scalability

Virtualization Performance Improvements

- Intel® Virtualization technology addresses today's IT concerns
  - Data center consolidation
  - Dynamic load balancing
  - Disaster recovery





Penryn improves VT-x instruction context switch times by ~25-75%

* Comparisons based on RTL simulations via micro-kernel workloads with cache hits

Improved Caches

- Up to 50% Larger Level 2 Cache

- 24-Way Set Associativity – Helps maximize utilization of the larger L2 Cache
  - Compared to 16-way associativity on previous generation

Minimizes Latency on Commonly Used Data

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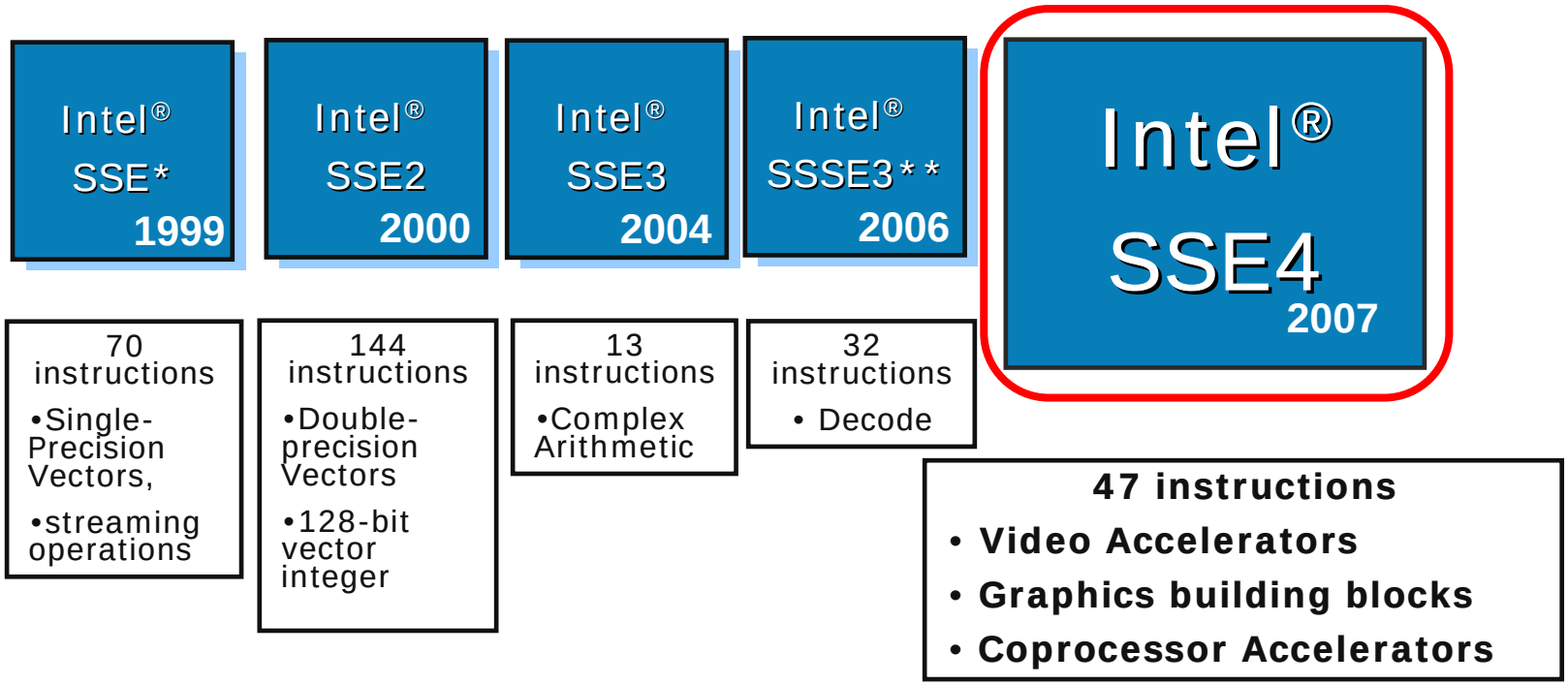
SSE4 History



Enhanced Intel® Core™ Microarchitecture (Penryn) supports 47 new instructions

This continues a trend set by SSE, SSE2, SSE3, and SSSE3

These extensions are a result of continuous customer feedback over the years!

* *Streaming SIMD Extension*

** *SSSE3: Supplemental Streaming SIMD Extension 3*

New Intel® SSE4 Instructions

Components

Video Accelerators– 2X faster **

14 instructions accelerate 4x4 SAD, Subpixel Filtering, and Search

Graphics Building Blocks –

32 Common Graphics Primitives generalized for compiler auto-vectorization

Streaming Load –

up to 9X faster***

access to device memory

Applications

- Video
  - Authoring - up to 1.4X faster *
  - Encoding
  - Search
- Portable Video Devices
- Imaging
  - e.g. Photo processing
- Graphics
- Gaming and Physics
- 3D content creation
- Off-chip Accelerators

SSE4 –Continuing a History of ISA Innovation

* Demonstrated in IDF 2007

** Gains of 2-3X on block SAD (Sum of Absolute Difference). As demonstrated in the "Motion Estimation with Intel® SSE4" whitepaper

*** Compared to existing loads to WC memory, measured using 45nm Hi-k Intel dual core desktop processor 1333 FSB, and software published in the "Using SSE4 Streaming Load" Whitepaper

Penryn SSE4 Instruction summary

Instruction Category	Instructions	Benefits
Packed DWORD Multiplies	PMULLD, PMULDQ	Improved automated compiler vectorization
Floating Point Dot Product	DPPS, DPPD	3D content creation, gaming, support for languages such as CG and HLSL
Multi-packed sum of absolute diffs & min pos	MPSADBW, PHMINPOSUW	Video processing
Packed Blending	BLENDPS, BLENDPD, BLENDVPS, BLENDVPD, PBLENDVB, PBLENDDW	Compiler vectorization and applications such as video processing, multi-media and gaming
Packed Integer Min and Max	PMINSB, PMAXSB, PMINUW, PMAXUW, PMINUD, PMAXUD, PMINDS, PMAXSD	Compiler vectorization and applications such as video processing, multi-media and gaming
Floating Point Round	ROUNDPS, ROUNDSS, ROUNDPD, ROUNDSD	Image processing, graphics, video processing, 2D/3D applications, multimedia, and gaming.
Register Insertion/Extraction	INSERTPS, PINSRB, PINSRD, PINSRQ, EXTRACTPS, PEXTRB, PEXTRD, PEXTRW, PEXTRQ	Compiler vectorization and applications such as video processing, multi-media and gaming
Packed Format Conversion	PMOVSXBW, PMOVZXBW, PMOVSXBD, PMOVZXBD, PMOVSXBQ, PMOVZXBQ, PMOVSXWD, PMOVZXWD, PMOVSXWQ, PMOVZXWQ, PMOVSXDQ, PMOVZXDQ	Compiler vectorization and applications such as video processing, multi-media and gaming
Streaming load	MOVNTDQA	Video processing, imaging, data sharing apps with GPU
Packed Test & Set	PTEST	Compiler vectorization and applications such as video processing, multi-media and gaming
Packed Compare for Equal	PCMPEQQ	Compiler vectorization and applications such as video processing, multi-media and gaming
Pack DWORD to Unsigned WORD	PACKUSDW	Compiler vectorization and applications such as video processing, multi-media and gaming

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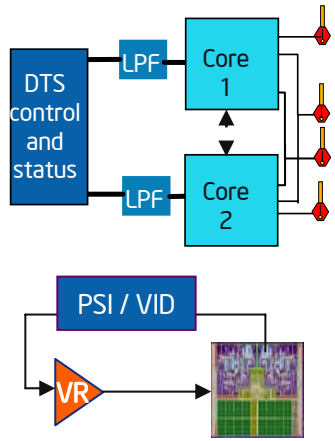
Power Management Enhancements

- **Penryn builds on the power and thermal architecture capabilities in the Core™ microarchitecture**
  - C-states: Processor idle condition low power states
  - P-states: Performance states
  - Thermal monitoring capability
  - Digital thermometer access
  - Intelligent voltage regulator management
  - Fine grained power management applied across the microarchitecture

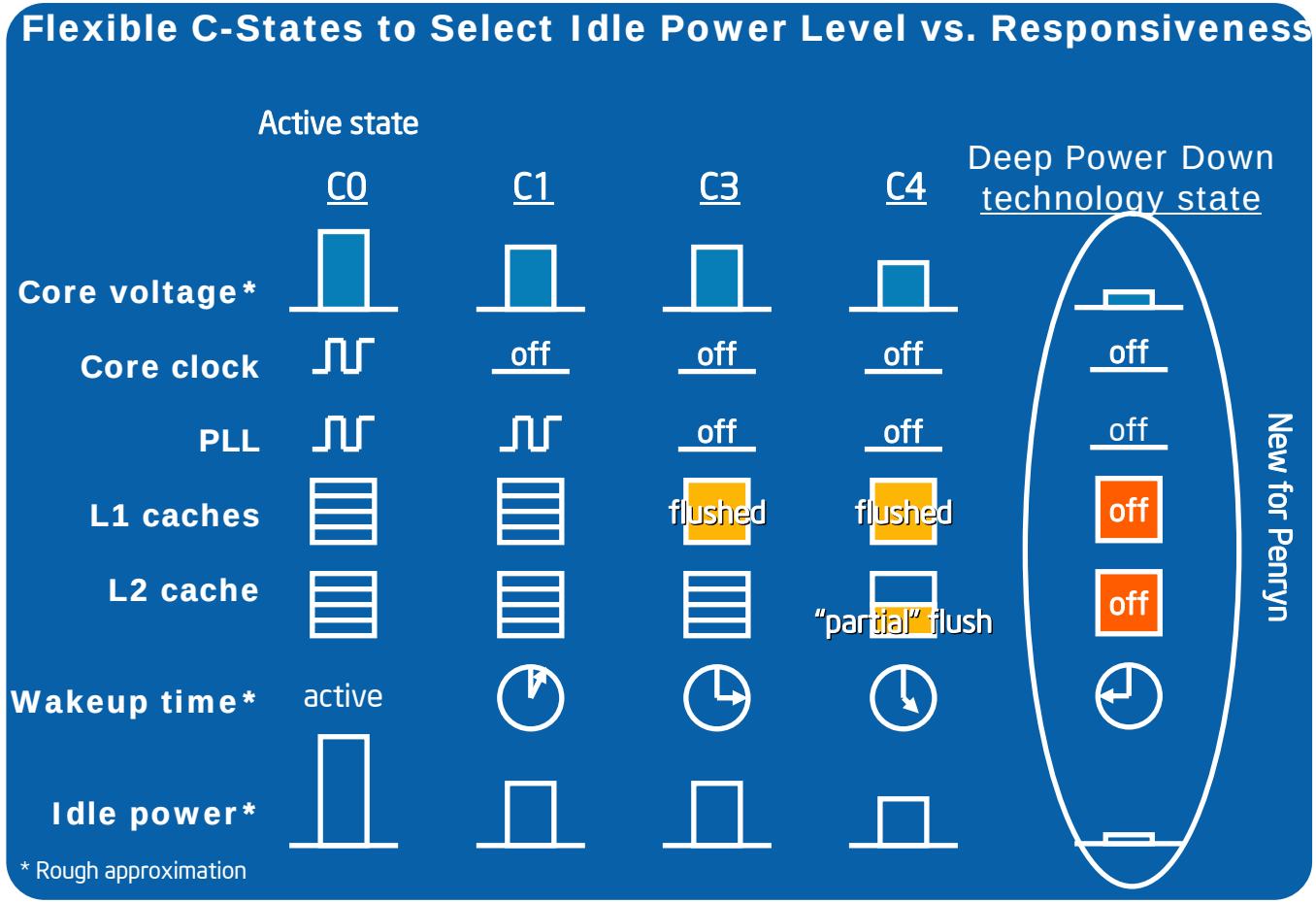


- **Key New Mobile Power / Thermal Features in Penryn:**
  - Deep Power Down technology:
    A radically new and innovative idle power management state
  - Enhanced dynamic acceleration technology:
    A deterministic and platform power-friendly performance boost using power headroom of idled core

Deep Power Down Technology

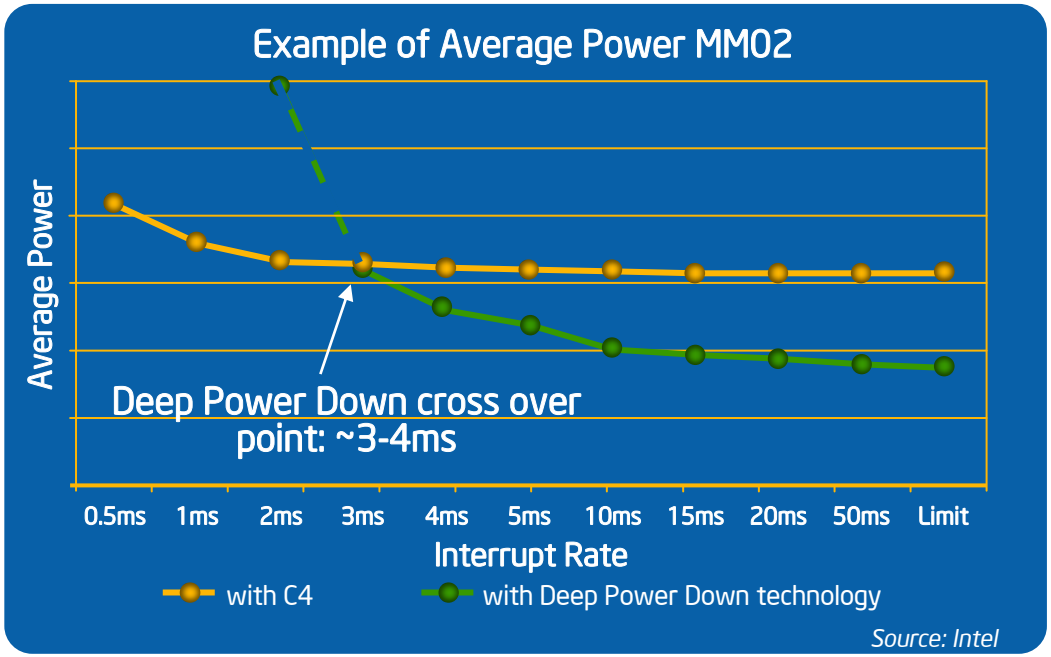
Available on Mobile Penryn Family Processors

- New Power Management State
- Significantly reduces processor power consumed in idle mode
- Further Extends Battery Life



Interrupt Rate Sensitivity of Average Power

- Deep Power Down technology delivers greatest benefit at reduced interrupt rates



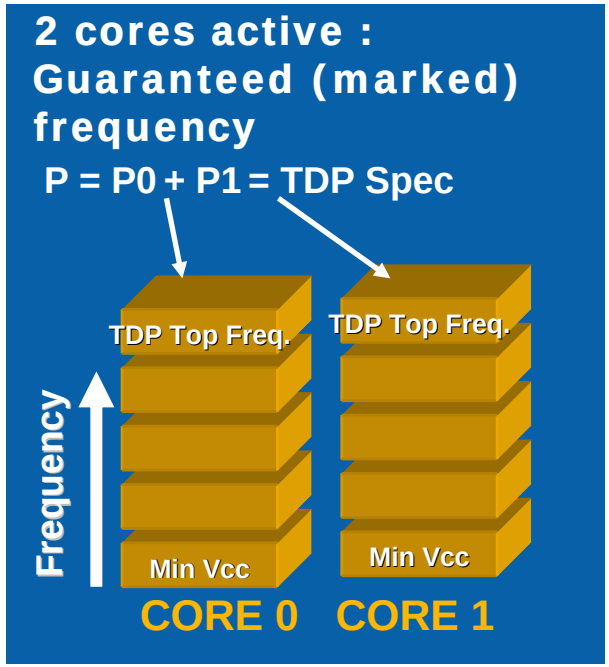
Penryn supports intelligent heuristics to recognize when:

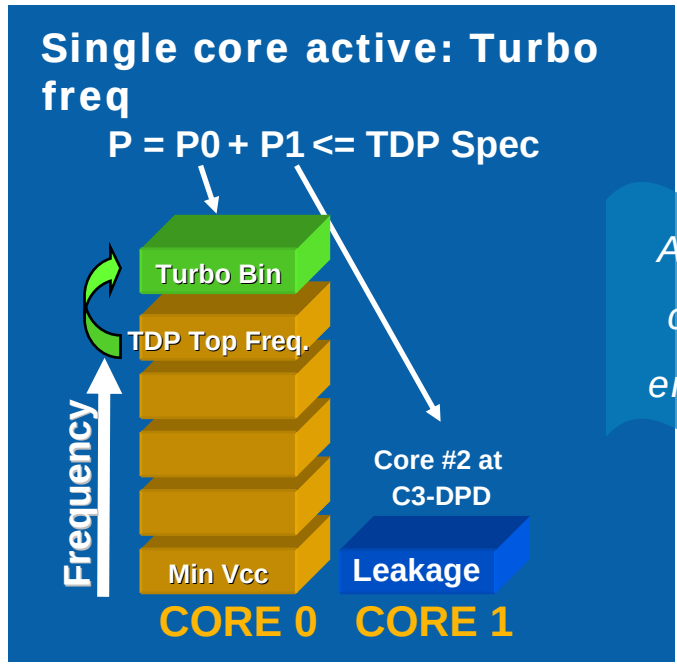
- Deep Power Down energy cost > idle period savings
- Demotes OS Deep power down requests to C4

Auto demote capability

Enhanced Dynamic Acceleration Technology

- **Concept:** In multi-core CPUs, use the power headroom of idle core to boost performance of the non-idle core
- **How it works:**
  - Enhanced Dynamic Acceleration technology available when one core enters an idle power C-state
  - Potential frequency boost on other core for single threaded apps
  - Processor still stays within the specified thermal design power (TDP) for any thermally significant amount of time

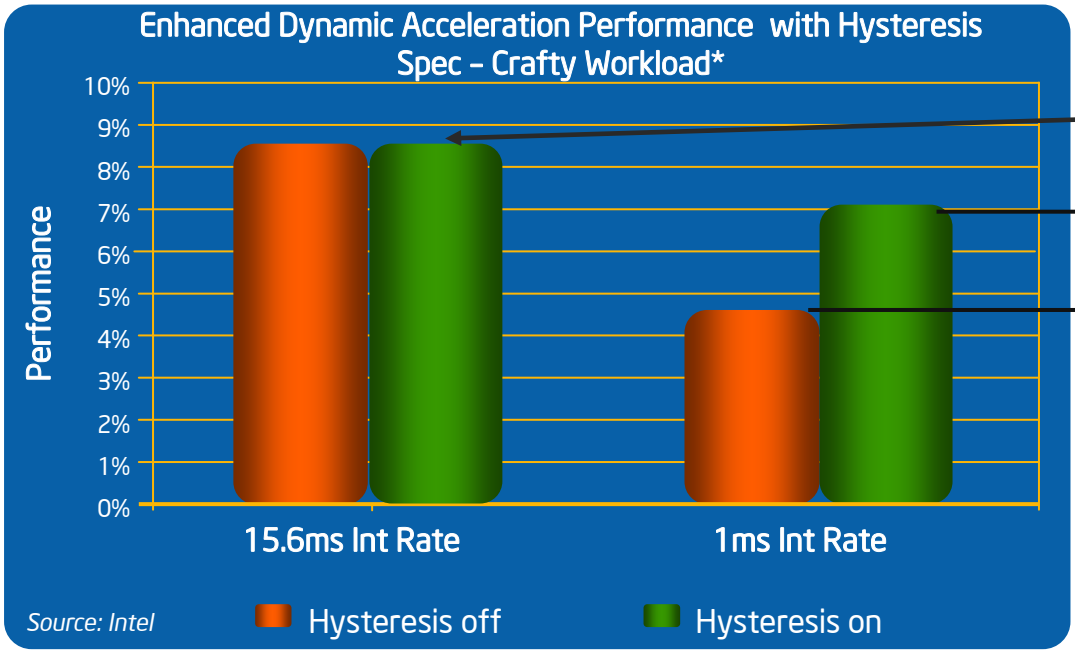




Applicable in power constrained mobile environments

Enhanced Dynamic Acceleration Technology Performance

- Delivers greatest benefit when 2nd core remains in idle mode
- Penryn supports a hysteresis mechanism to allow operation even when 2nd core is awoken for short intervals



No performance degradation at reduced interrupt rates

Hysteresis performance benefit under high timer tick rate environment

* *Measured results from preliminary silicon. 'crafty' is a workload component of ISPEC00 See backup slide for details on system configuration used for this measurement*

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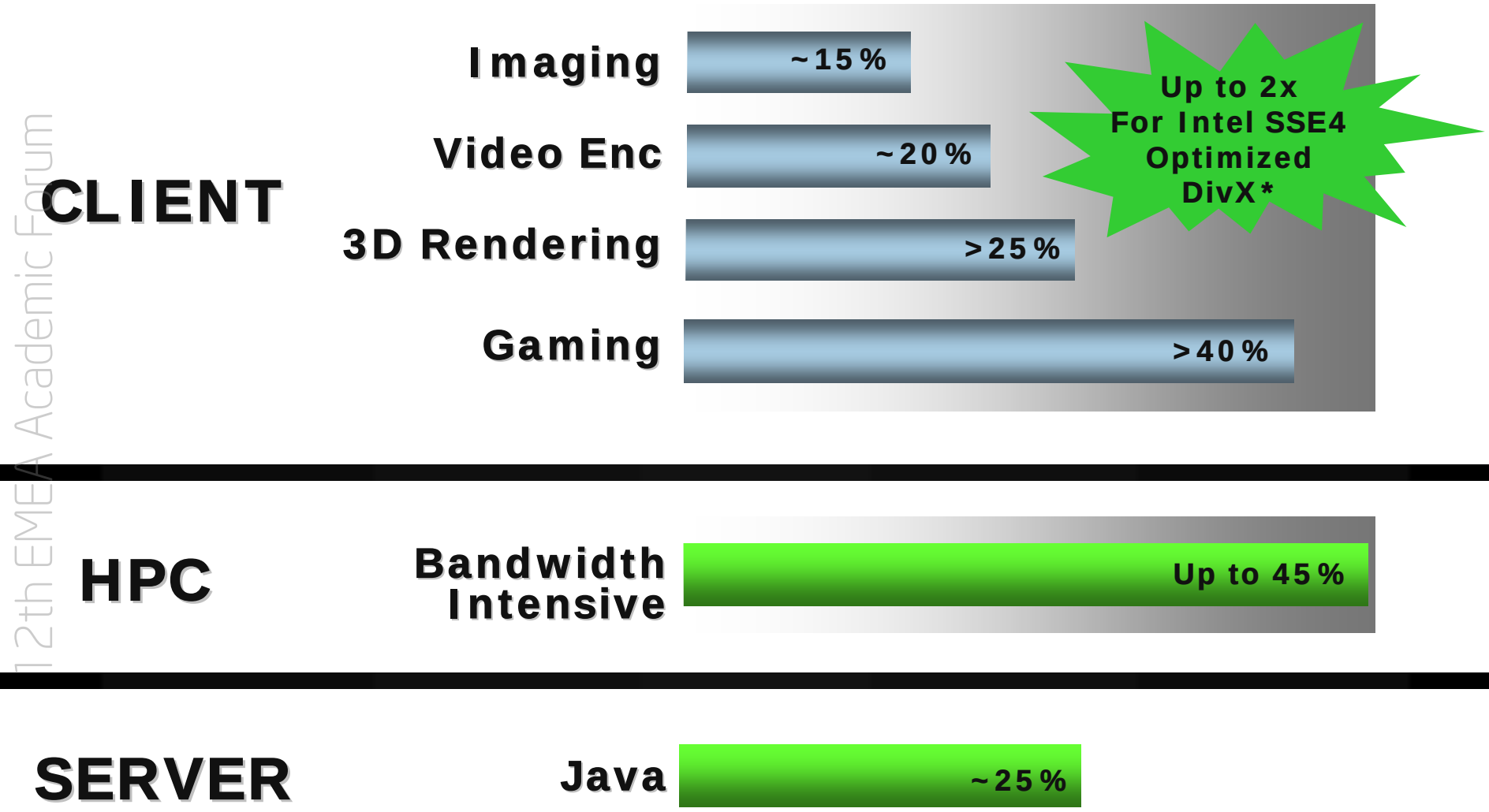
Early Penryn Family Performance Indicators**

45nm Hi-k vs 65nm Intel® Core™ 2 and Xeon™ Processors



** based on early silicon – results on production silicon may vary

45nm Next Generation Intel® Core™ and Xeon Family processors (Penryn)

- Intel's leading 45 nm High-k silicon process coupled with enhanced Intel Core Microarchitecture
- Greater performance at given frequency and higher frequencies
- Greater energy efficiency
- Optimized configurations for server, workstation, desktop, and mobile

On Track for 2H'07 Production

Additional sources of information on this topic:

- More web based info:
  - Intel® Core™ Microarchitecture: http://www.intel.com/technology/architecture/coremicro/index.htm
  - Intel® SSE4 Instructions: http://download.intel.com/technology/architecture/new-instructions-paper.pdf
  - 45 nm Process Technology & High-k gate dielectrics http://www.intel.com/technology/silicon/45nm_technology.htm http://en.wikipedia.org/wiki/High-k
  - Penryn http://www.intel.com/technology/magazine/45nm/coremicroarchitecture-0507.htm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Backup

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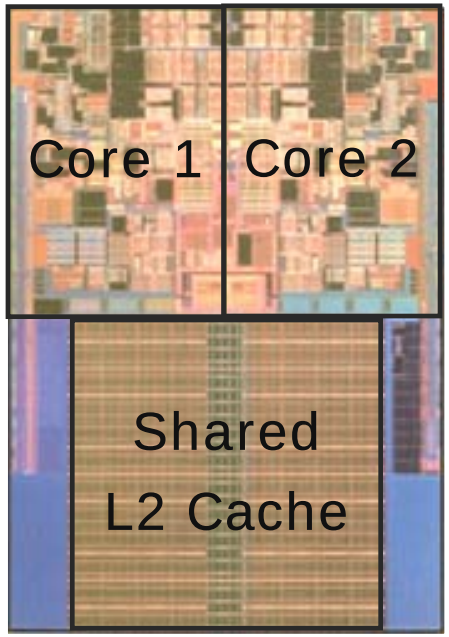


System configuration data used for Enhanced Dynamic Acceleration Technology measurements

- Mobile Penryn pre-production processor
- Mobile pre-production chipset
- Windows* XP* SP2
- Max Battery CPU setting

Appendix A: Performance Configurations

Client

- Pre-production 45nm Hi-k Intel Core 2 quad core processor (12MB L2, 3.33GHz, 1333MHz FSB) compared to Intel® Core™ 2 Extreme processor QX6800 (8MB L2, 2.93GHz, 1066MHz FSB)
- Applications: Half-Life* 2 build 2707, Cinbench* R9.5, MainConcept* H.264 Encoder v2.1, Photoshop* CS2

Server

- Based on Intel internal measurement/projection on a Server Side Java benchmark. March 2007. Pre-production 45nm Hi-k Intel® Xeon™ processor is compared to current generation Quad-Core Intel® Xeon® processor X5355 on the Bensley Server platform

HPC

- Based on Intel internal measurement on bandwidth intensive floating point benchmarks. March 2007. New generation Stoakley platform with Pre-production 45nm Hi-k Intel® Xeon™ processor with 1600 MHz FSB is compared to current generation Quad-Core Intel® Xeon® processor X5355 based Bensley platform

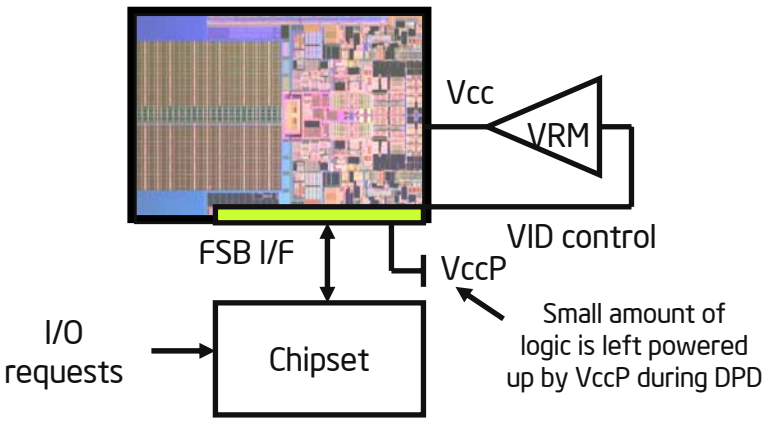
Client Performance Results

- *Source: Intel. Configuration: Preproduction 45nm Hi-k Intel® quad core processor (3.33 GHz/1333/12MB quad-core) and Intel® Core™ 2 Extreme processor QX6800 (2.93 GHz/1066/8MB) on modified Intel D975XBX2 Rev. 505; with Dual channel (2x1GB) DDRII 800 5-5-5-15 ASUS EN8800GTX GeForce GTX graphics, 300GB NCQ SATA. Windows* Vista* 32 bit build 6000.*
- *Performance tests and ratings are measured using specific systems and/or components and reflect approximate performance of Intel products as measured by those tests. Any difference in system hardware, software, or configuration may affect actual performance. Buyers should consult other sources of information to evaluate system or component performance they are considering purchasing. For information on performance tests and performance of Intel products, visit http://www.intel.com/performance/resources/limits.htm*

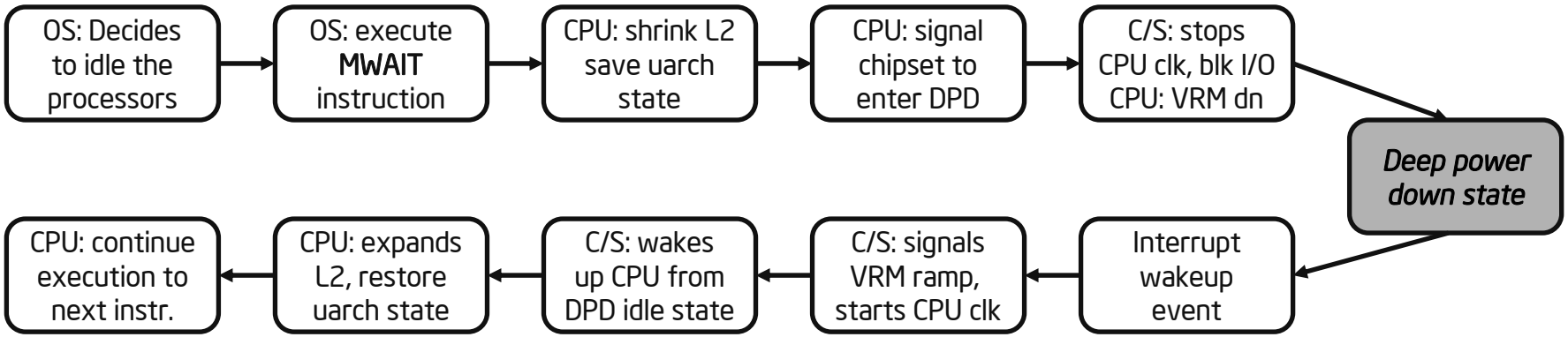
	Intel® Core™2 Extreme processor QX6800 (8MB L2, 2.93 GHz, 1066 FSB)	45nm Hi-k Intel® quad core processor (12MB L2, 3.33 GHz, 1333 FSB)	Percent Faster
DivX* 6.6 Alpha with VirtualDub 1.7.1 (time in seconds – lower is better)	38	18	211%
Half-Life* 2 build 2707 (frames per second - higher is better)	151	213	41%
Cinebench* R9.5 (score - higher is better)	1549	1935	25%
MainConcept* H.264 Encoder v2.1 (time in seconds - lower is better)	88.0	73.4	20%
Photoshop* CS2 (time in seconds - lower is better)	105	91.0	15%

*** based on early silicon – results on production silicon may vary**

Deep Power Down Technology *in Action*



- S/W instruction initiates processor Deep Power Down (DPD) technology action
- Handshake with chipset initiates shutdown and wakeup sequencing
  - Clock control, interrupt, and DMA traffic blocking



Autonomous Power Down Capability for Longer Battery Life