Tunnel FET: the next energy efficient switch?

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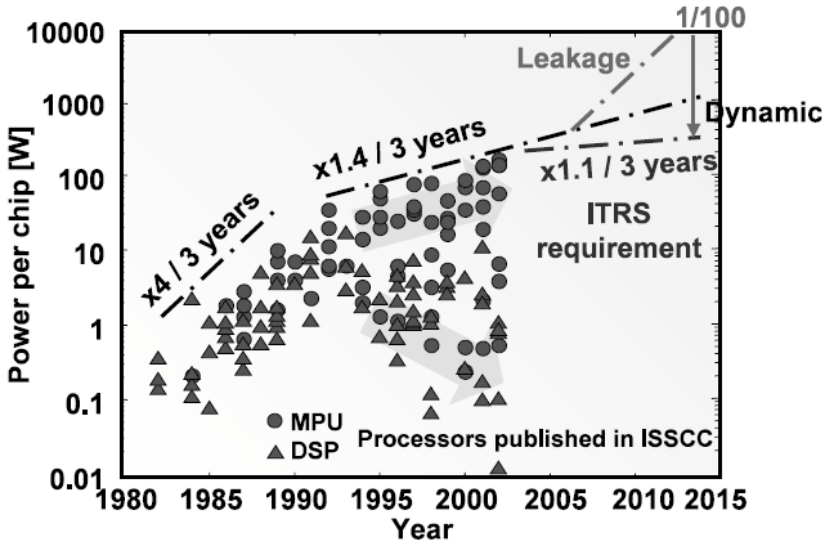
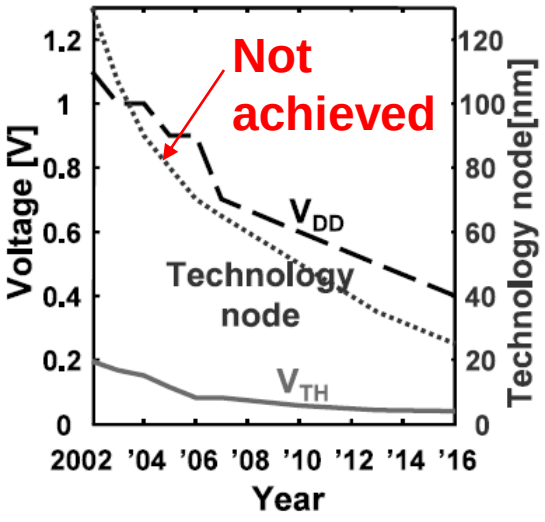
Outline

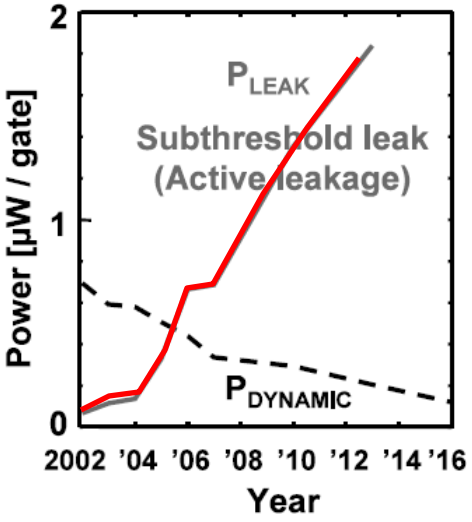
- **Power challenge and energy efficient switch**
- **Sub-thermal swing switches**
- **Complementary Tunnel FETs**
  - Physics, optimization, scaling
  - Model and temperature (in)dependence
  - All-silicon, Ge & III-V heterostructure, Carbon
  - Circuit benefits
- **Conclusions**

The power challenge

- Power per chip continues increasing.
- Leakage power dominates in advanced technology nodes.
- V_T scaling saturated by 60mV/dec physical limit.
- Voltage scaling slowed, 90nm=1.2V, 45nm=1V, 22nm=0.8V

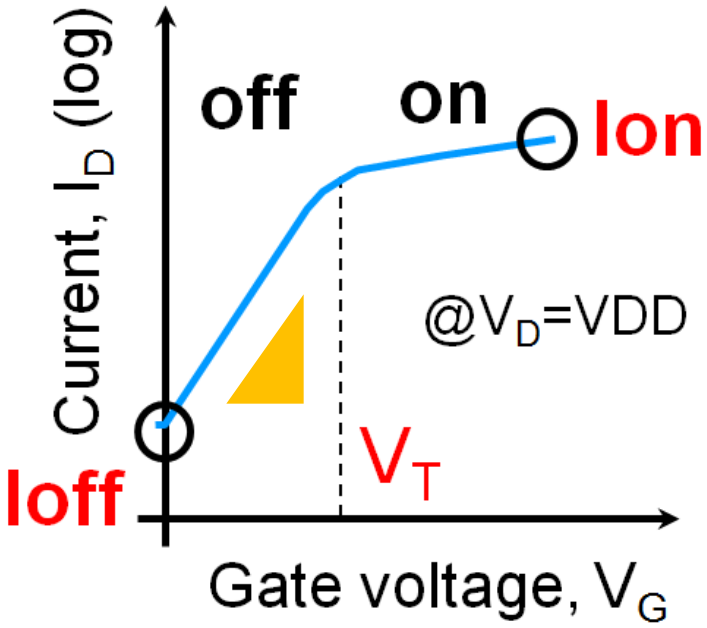


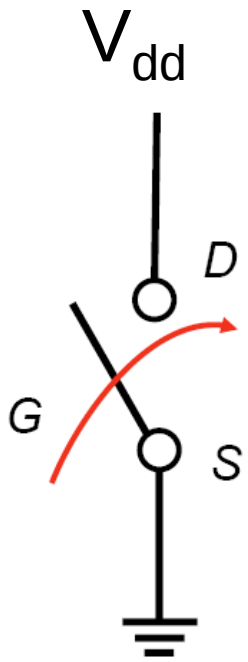




T. Sakurai, IEICE Trans. Electron., Vol.E87-C, April 2004, pp. 429-436.

MOSFET & subthreshold swing

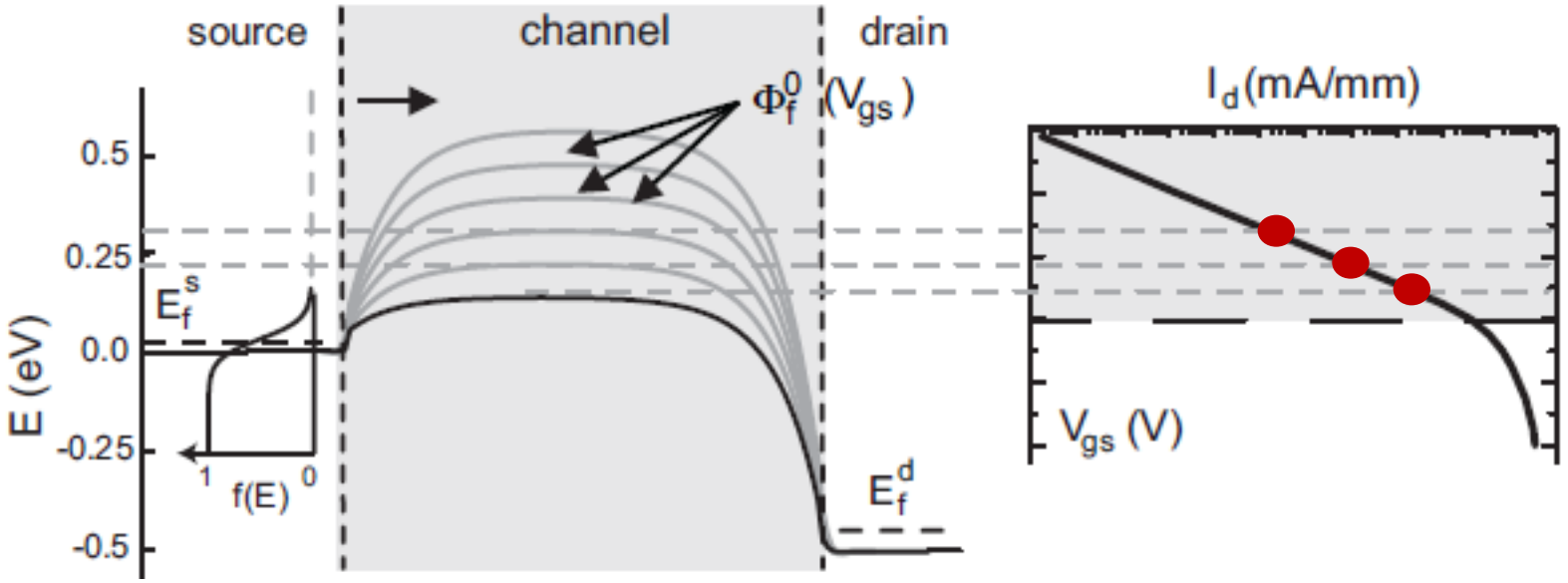




$$S_{avg} = (V_T - V_{Goff}) / \log(I_T / I_{off}) \approx V_{dd} / \log(I_{on} / I_{off})$$

(mV/decade)

60mV/decade limit at RT

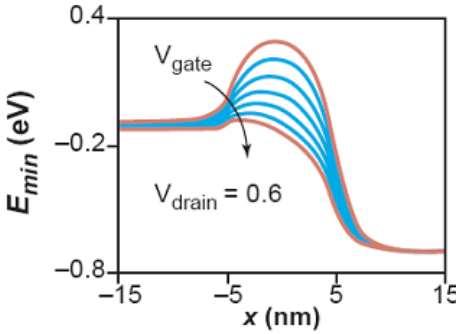


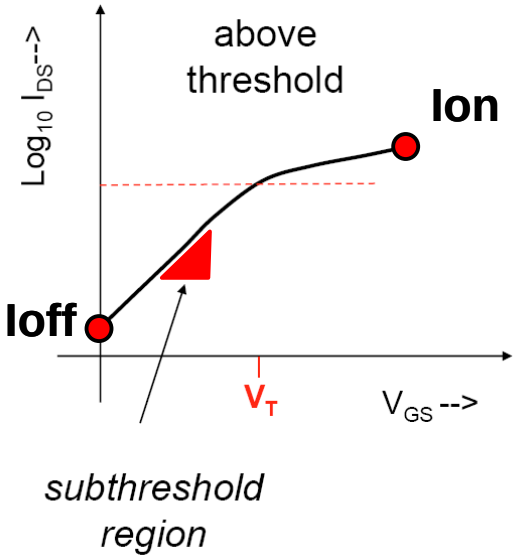
Conduction band profile in transport direction in a long channel MOSFET.

• The gate voltage moves the conduction band downwards, so that a larger fraction of the exponential tail of the source Fermi distribution can contribute to the current.

•This gives rise to the exponential increase of the current.

History: diffusion current and S





subthreshold region

- carrier injection by lowering the barrier
- subthreshold current is a diffusion current

$$I_D = q\frac{W}{L}\left(\frac{n_i^2}{N_A}\right)\frac{(k_BT/q)^2}{E_S}\mu_{eff}e^{qV_{GS}/mk_BT}\left(1-e^{-qV_{DS}/k_BT}\right)\text{A}$$

$$m = 1 + C_D / C_{OX}$$

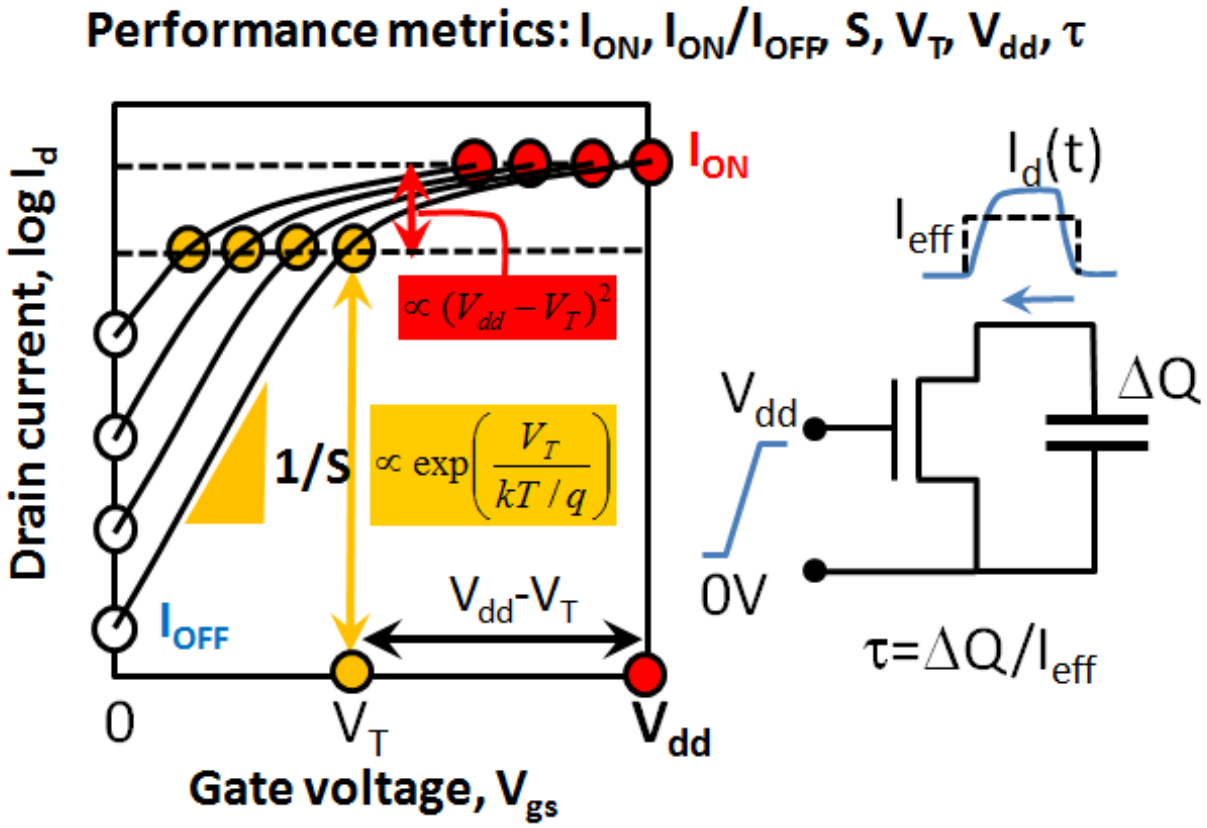
$$S = \frac{dV_g}{d(\log_{10} I_d)} = \ln 10 \frac{kT}{q}(1+\frac{C_{dep}}{C_{ox}}+\frac{C_{ss}}{C_{ox}})$$

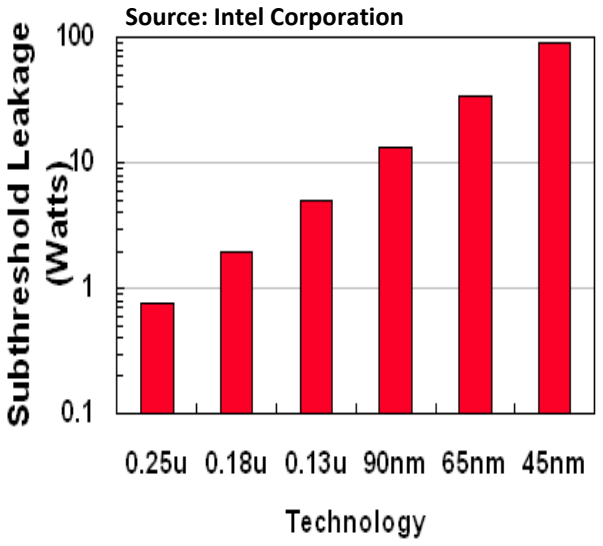
$$\rightarrow \frac{kT}{q}\ln 10 = 60mV/decade \quad @\,RT$$

R. Van Overstraeten,G.J. Declerck, P.A. Muls,
IEEE Transactions on Electron Devices, Volume 22, May 1975.

Leakage power and thermal swing

Reducing threshold voltage **by 60mV**
increases the leakage current (power) **by ~10 times**





Energy efficiency, V_{dd} scaling and S

$$E_{total} = E_{dynamic} + E_{leakage} = \alpha L_d C V_{dd}^2 + L_d I_{off} V_{dd} \tau_{delay} \approx$$

$$\approx \alpha L_d C V_{dd}^2 + L_d C V_{dd}^2 \frac{I_{off}}{I_{on}} =$$

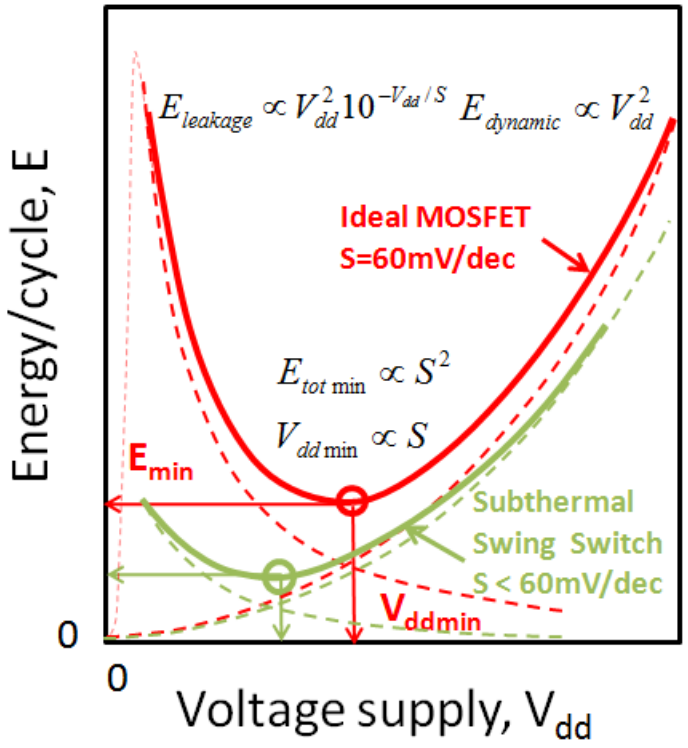
$$= L_d C V_{dd}^2 (\alpha + \frac{I_{off}}{I_{on}}) \approx L_d C V_{dd}^2 (\alpha + 10^{-V_{dd}/S})$$

$$P = \alpha L_D C V_{dd}^2 f + I_{off} V_{dd} \approx K C V_{dd}^3 + I_{off} V_{dd}$$

a technology that would enable a voltage scaling by a factor of 5 (from 1 V to 0.2 V) with a negligible leakage power (with ultra-low I_{off} due to a small S, as the TFET) **could offer a power dissipation reduction of 125x.**

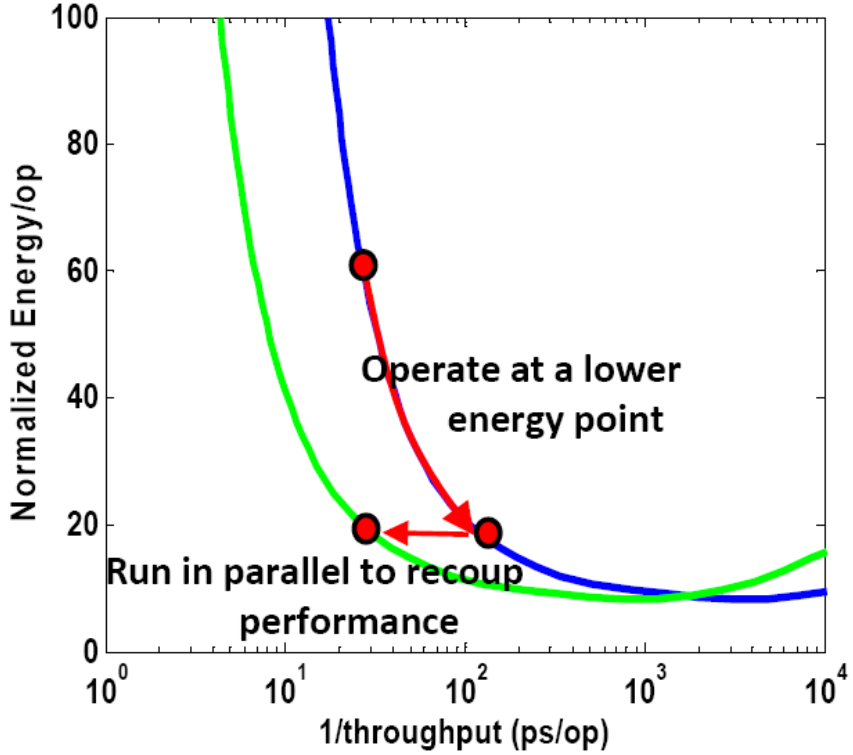
Small S and/or parallelism to the rescue

CMOS has a fundamental lower limit in energy per operation due to subthreshold leakage: (V_{ddmin}, E_{min})



Source: A.M. Ionescu, H. Riel, to appear.

Parallelism (multi-core) is a key technique to improve system performance under a power budget



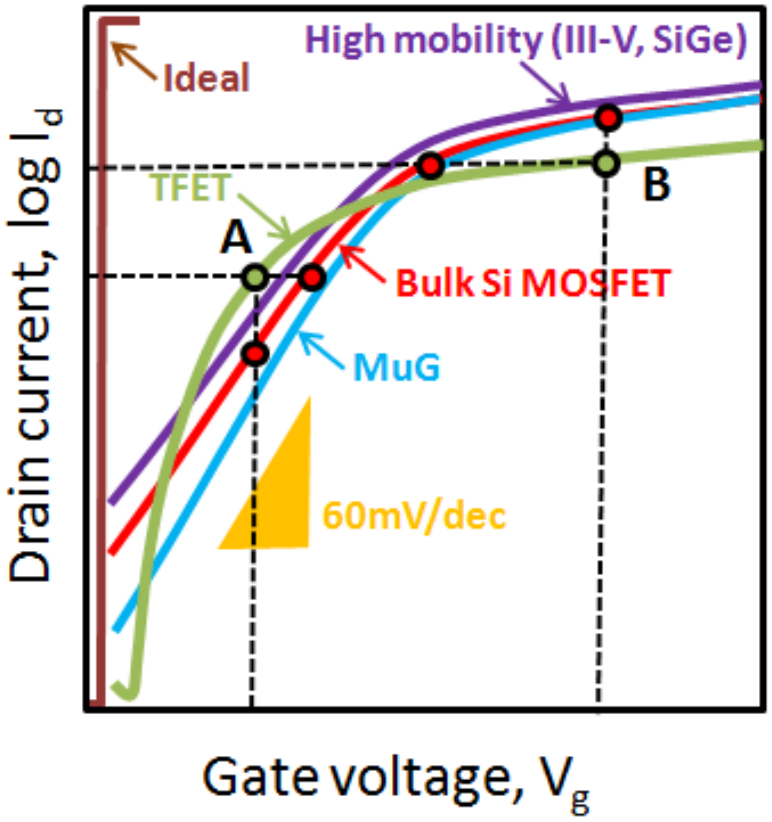
Source: T.J. King, UC Berkeley.

Strategy for the energy efficient switch

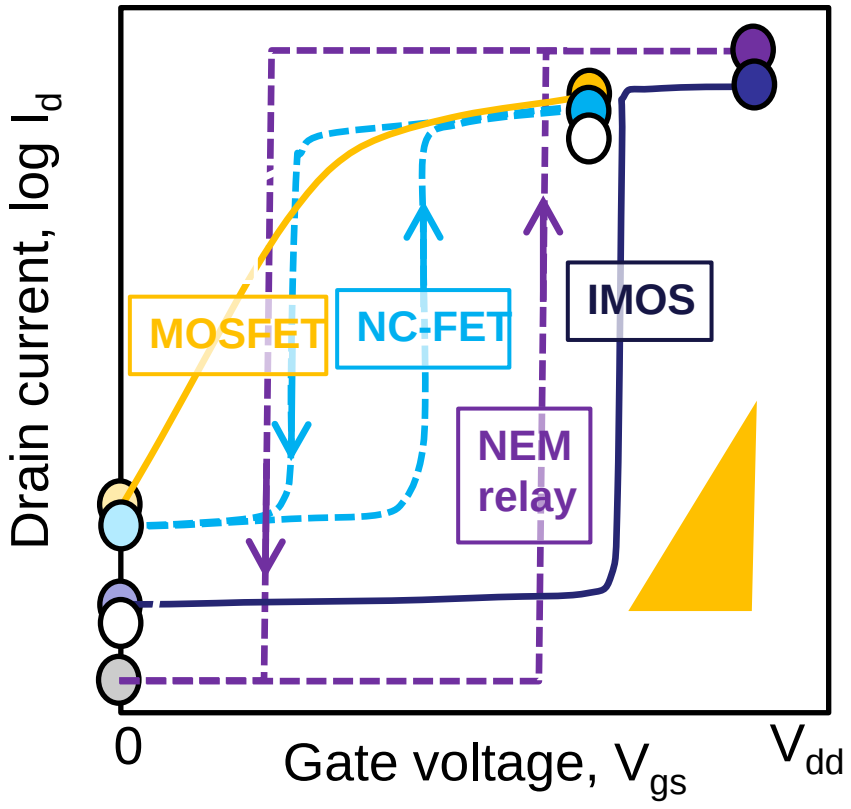
- **Improving the MOSFET switch: evolutive, additive technology boosters.**
  - Channel engineering to reduce the V_{dd}-V_t (Ge, III-V, graphene, etc).
  - Nanowire and nanotube FETs for improved electrostatic (subthreshold leakage) control.
- **Reduce the V_T and V_{dd} by a novel small swing switch.**

Small swing switches

Tunnel FET vs. future FET



Small swing switches



Tunnel FET is the most promising small swing switch for V_{dd} scaling.

Principles for SS < 60mV/decade

$$S = \frac{\partial V_g}{\partial(\log I_d)} = \frac{\partial V_g}{\partial \psi_S} \frac{\partial \psi_S}{\partial(\log I_d)} = (1 + \frac{C_s}{C_{ins}}) \frac{kT}{q} \ln 10$$

$\underbrace{\qquad}_{m}$ $\underbrace{1 4 2 4 3}_{n}$

m less than 1

- NEM relay or NEMFET
- negative capacitance (NC) FET)

n less than (kT/q)ln10

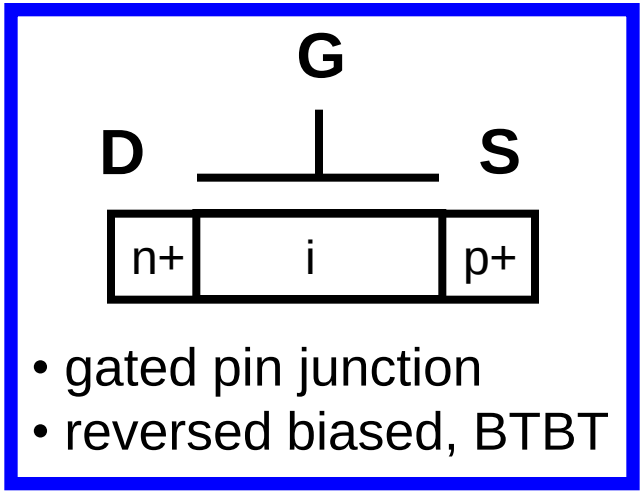
- Tunnel FETs
- Impact Ionization MOS

Tunnel FET: principle

Band-To-Band-Tunneling (BTBT)

Off-state

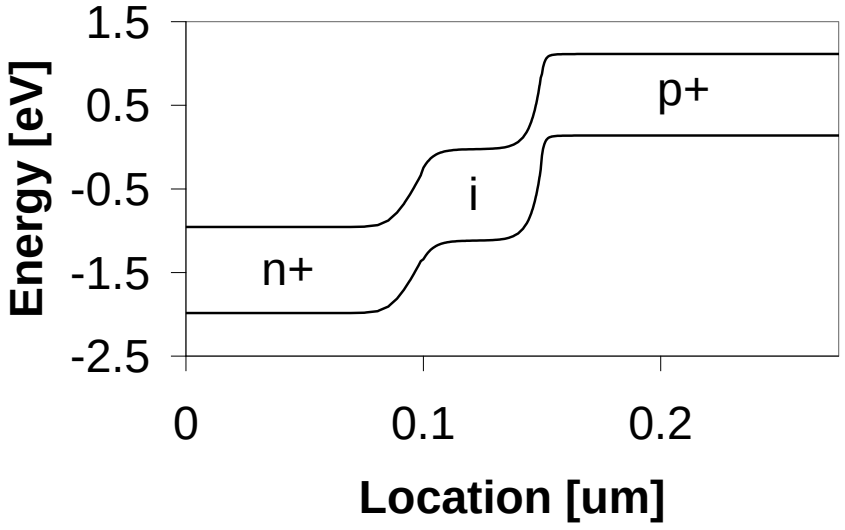
- V_d = positive
- V_g = 0
- **no current flows**

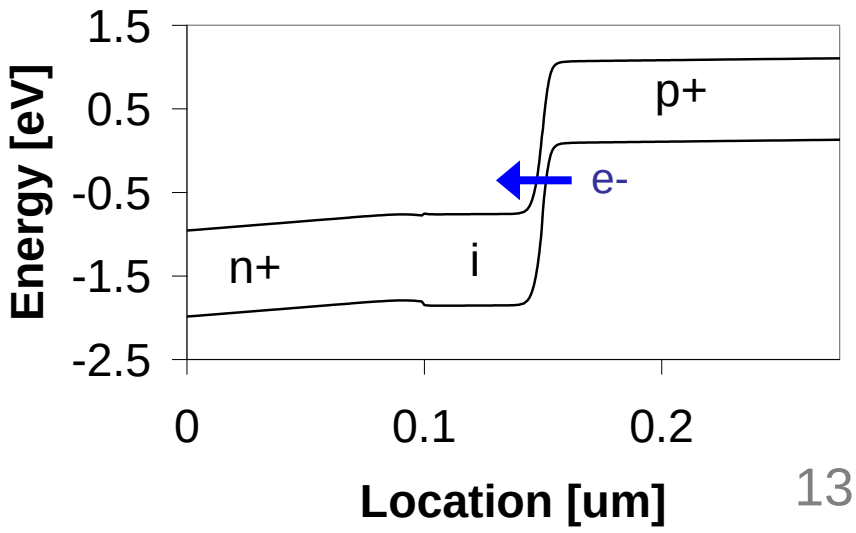


- gated pin junction
- reversed biased, BTBT

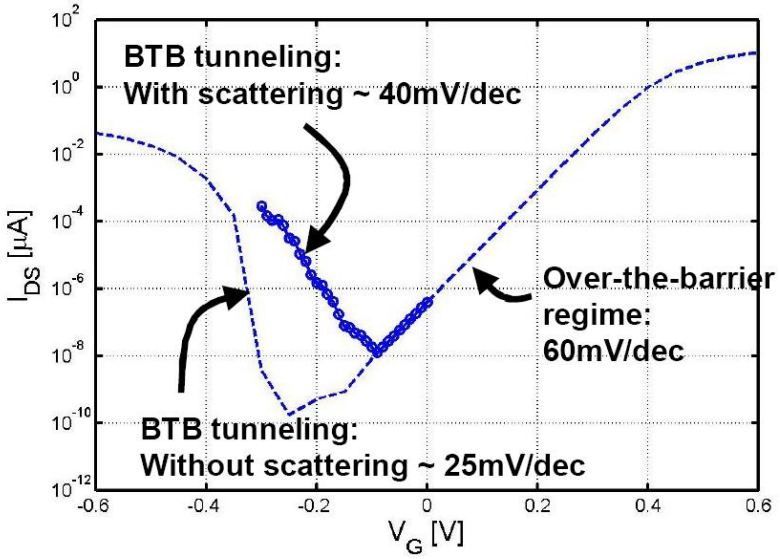
On-state

- V_d = positive
- V_g = positive
- **barrier thin, current flows**



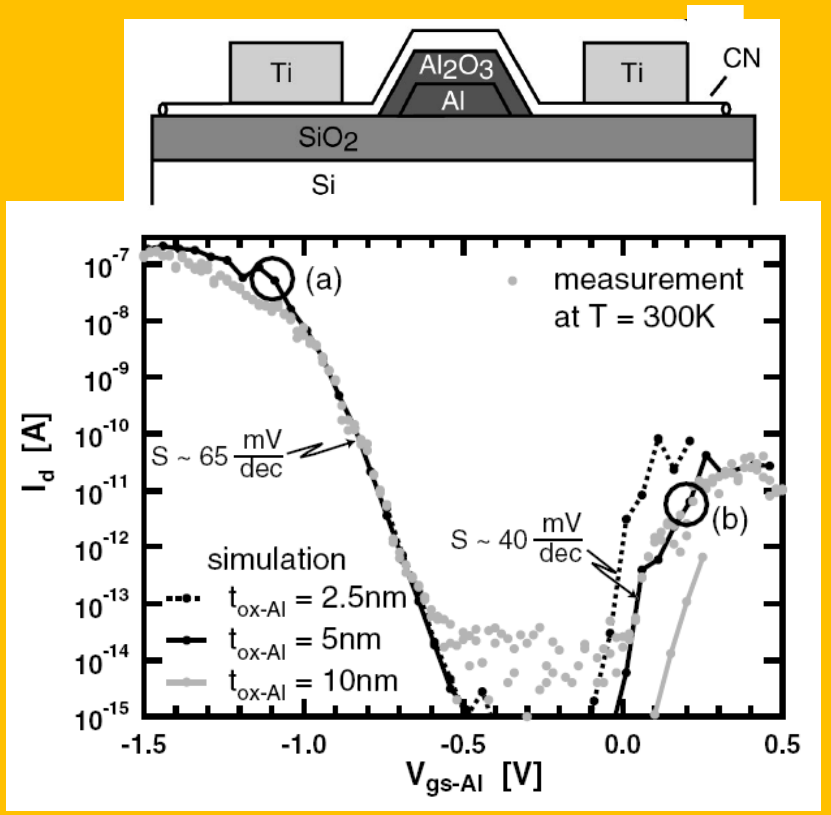


First experimental demonstration: 40mV/dec in CNT tunnel FETs



• dissipative quantum transport simulations of CNT FETs using the non-equilibrium Green's function (NEGF) formalism.

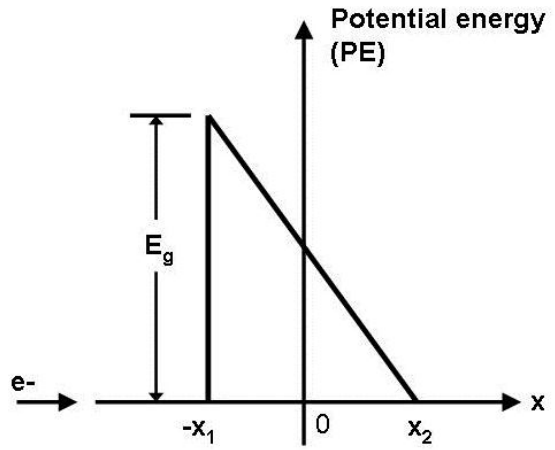
M. Lundstrom



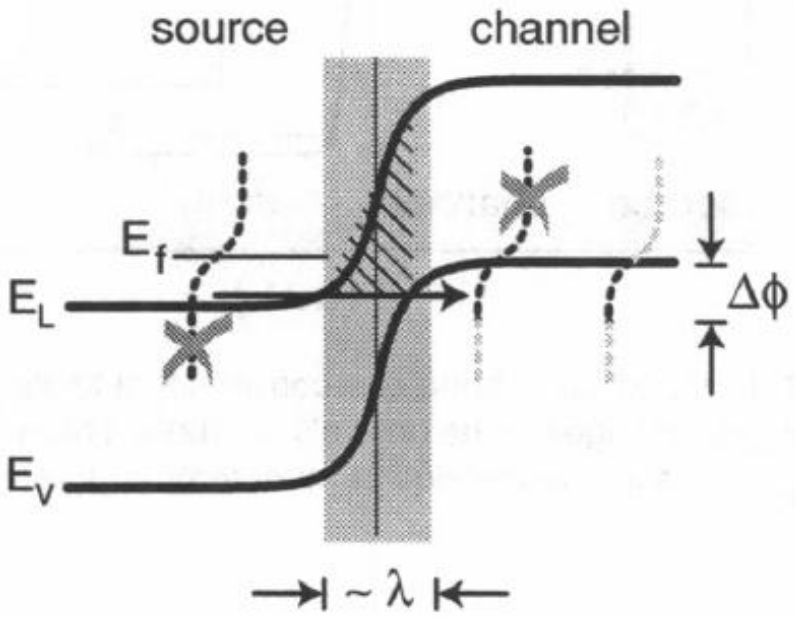
On-current: ~1μA/tube

J. Appenzeller, J. Knoch, Phys. Rev. Lett. 93, (2004).

Physics: tunneling rate



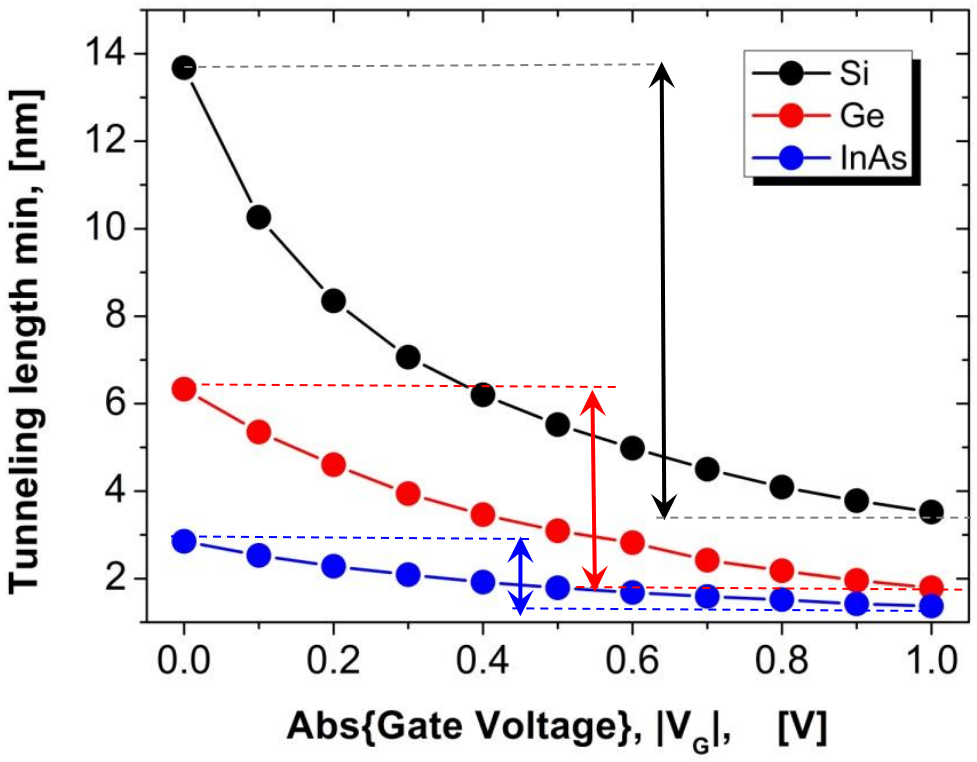
$$I_{BTB} \propto T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{1.5}}{3\eta(\Delta\Phi + E_g)}\right)$$



Parameter	Means of improvement
m*	Small effective tunnel mass, SiGe, III-V, CNT
E_G	Source in SiGe, III-V heterostructures, strain CNT
λ	3D geometry (wrap gate), high-k gate dielectric, thin gate dielectric

Source: H. Riel, IBM Zurich.

Min tunneling screening length, λ

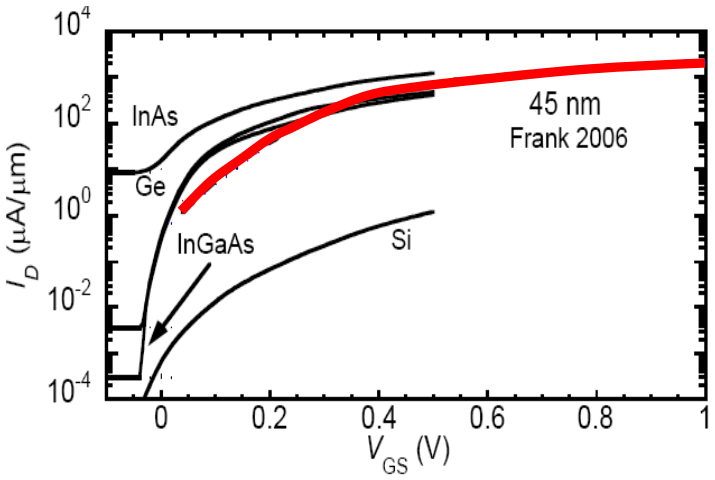


Major characteristics dictated by the tunneling junction and gate control on λ

- bandgap
- gate dielectric (thickness, permittivity)
- silicon film thickness (UTB, NW)
- fringing fields

20nm Tunnel FET versus CMOS

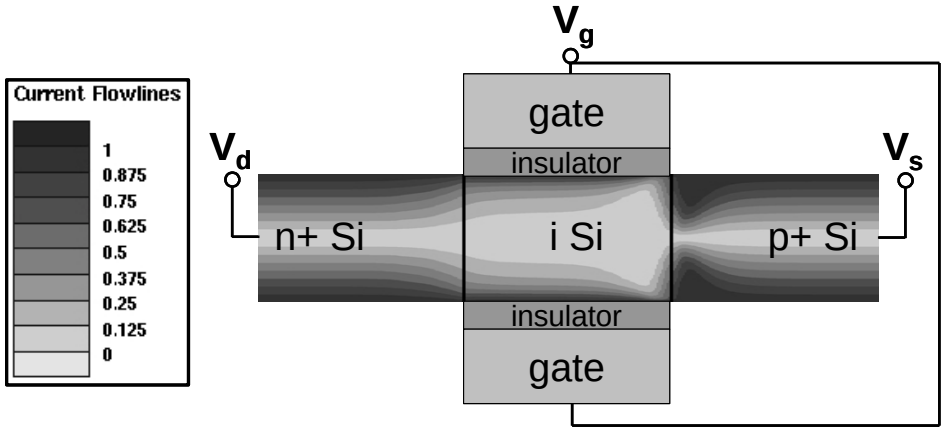
Parameter	MOSFET[a]			Tunnel transistor		Unit
	2007	2010	2013[b]	Si	Ge	
Gate length L_G	*25*	*18*	*13*	20	20 nm	
Gate width $W \sim 10L_G$	250	180	130	200	200	nm
Equivalent oxide thickness EOT	*1.1*	*0.65*	*0.5*	1	1	nm
Supply voltage V_{DD}	0.5	0.5	0.5	0.5	0.5	V
On current I_{ON}	428	701	1053	1.2	440	μA/μm
Off current I_{OFF}	0.29	2.02	1.88	2.7E-06	0.0036	μA/μm
Oxide capacitance density $C_{OX} \sim \varepsilon / t_{OX}$	31.4	53.1	69.1	34.5	34.5	fF/μm^2
Gate capacitance $C_G \sim C_{OX}L_G$	0.78	0.96	0.90	0.69	0.69	fF/μm
Intrinsic speed $_T \sim C_G V_{DD}/I_{ON}$	0.92	0.68	0.43	288	0.78	ps
Leakeage $P_{leak} \sim n\, I_{leak}\, V_{DD}$	7.25	50.50	47.00	6.8E-05	0.09	μW/μm
Dynamic $P_{dyn} \sim 1/2nI_{ON}V_{DD}\,\alpha$	107	175	263	0.300	110	μW/μm
Total $P \sim P_{leak} + P_{dyn}$	114	226	310	0.300	110	μW/μm
Leakeage $E_{leak} \sim (nI_{leak})\, V_{DD}\, (n\tau)$	332	1722	1002	1	4	aJ/μm
Dynamic $E_{dyn} \sim 1/2\, (nC_G)V_{DD}{}^2\alpha$	98	120	112	86	86	aJ/μm
Total $E \sim E_{leak} + E_{dyn}$	430	1842	1114	87	90	aJ/μm



Q. Zhang, A. Seabaugh, DRC 2008.

- all-silicon Tunnel FET: low performance (low Ion)
- heterostructures: source bandgap engineering.

All-Si Double Gate Tunnel FET with high-k dielectric



Parameter	Before	After optimization
Gate dielectric ε	3.9	25
Junction width	47 nm / 5 decades	12 nm / 5 decades
Body thickness	50 nm	10 nm
Source doping	$8x10^{19}$ atoms/cm^3	$1.5x10^{20}$ atoms/cm^3
Gates	Single	Double
Oxide alignment	Over all	Over intrinsic
Device/gate length	90 nm	30 nm

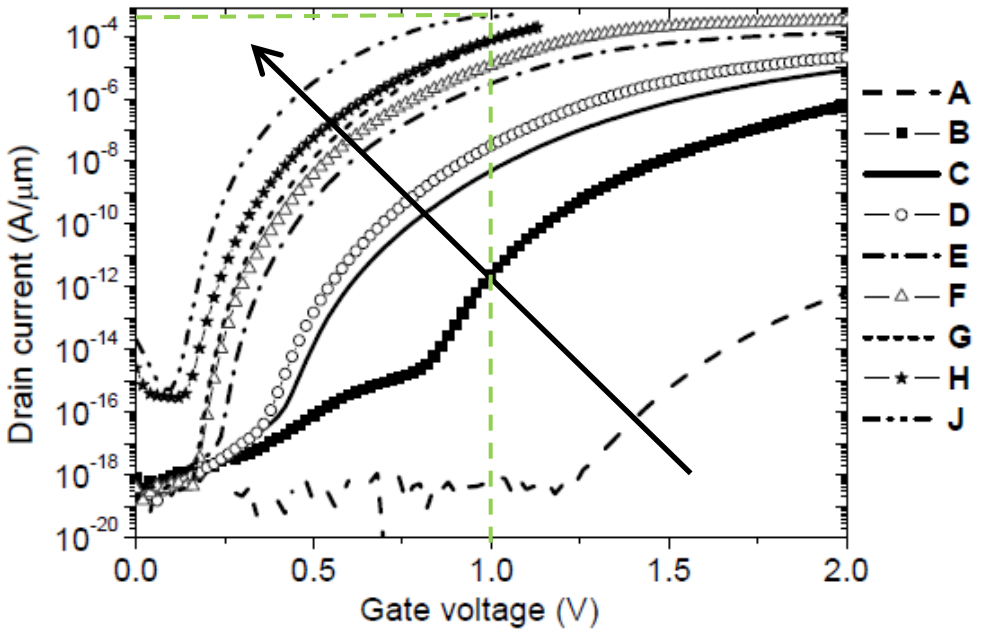
K. Boucart and A.M. Ionescu, IEEE TED 2007.

Sub-1V all-silicon tunnel FET

Additive technology boosters (simulation)

$I_{on} > 100\mu A/\mu m$ @ 1V

$I_{on}/I_{off} > 10^{10}$



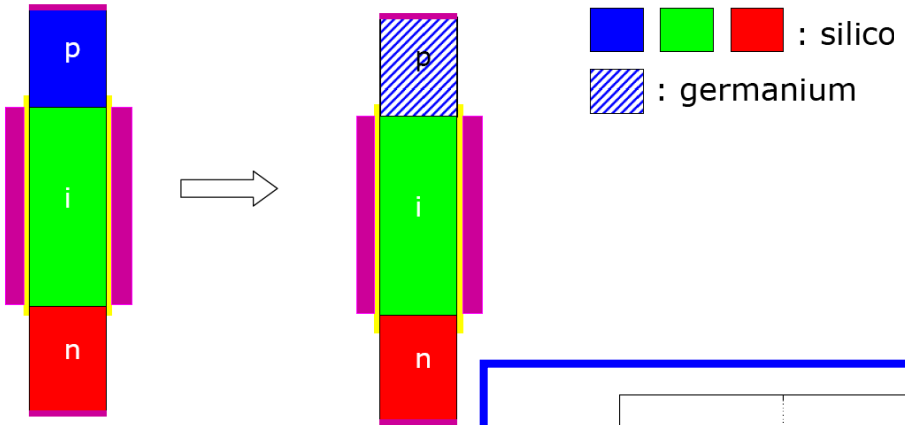
'A': base device
'B': Like A with high-k dielectric.
'C': Like B with narrower junction.
'D': Like 'C' with thinner body.
E: Like 'D' with higher source doping.
'F': Like E with double gate.
'G': Like 'F' with oxide over intrinsic region.
'H': Like 'G' with shorter length.
'J': Like 'H' with bandgap E_g = 0.8 eV at the tunnel junction.

K. Boucart, W. Riess, A.M. Ionescu, ESSDERC 2009.

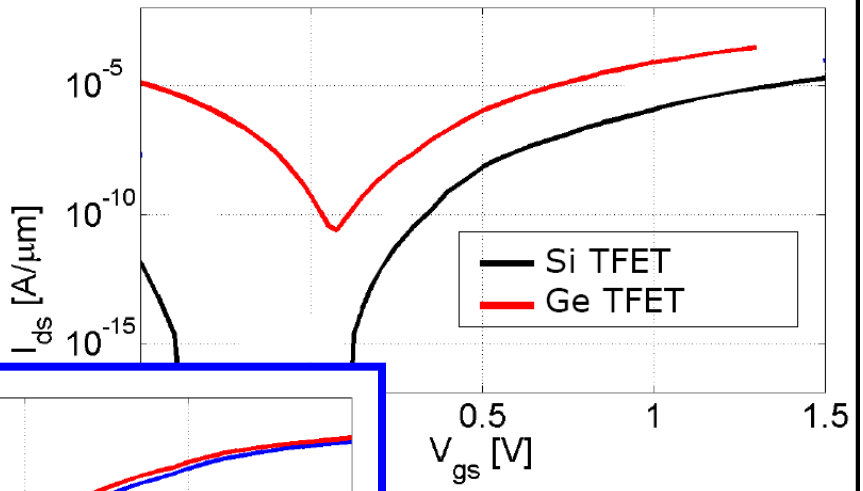
Ge/SiGe-source vertical NW Tunnel FET

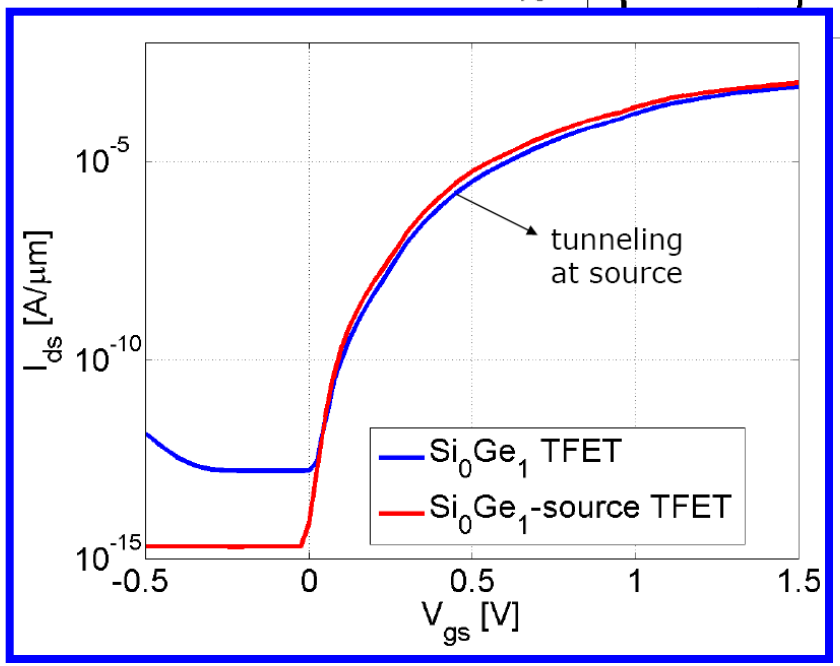
all-Si TFET

Ge-source TFET



• Smaller bandgap → improved tunneling but Ioff high

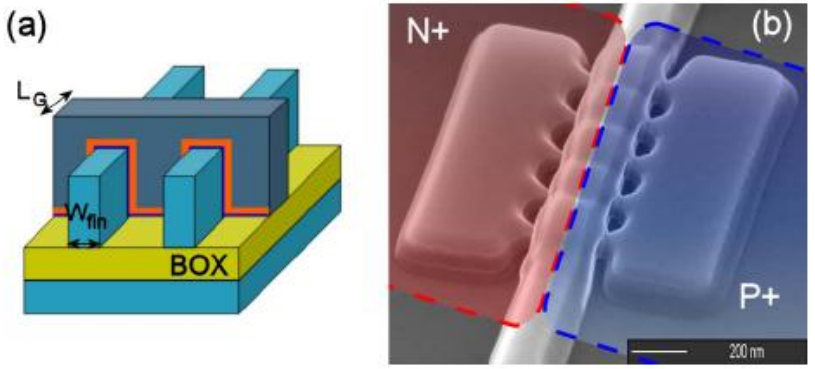


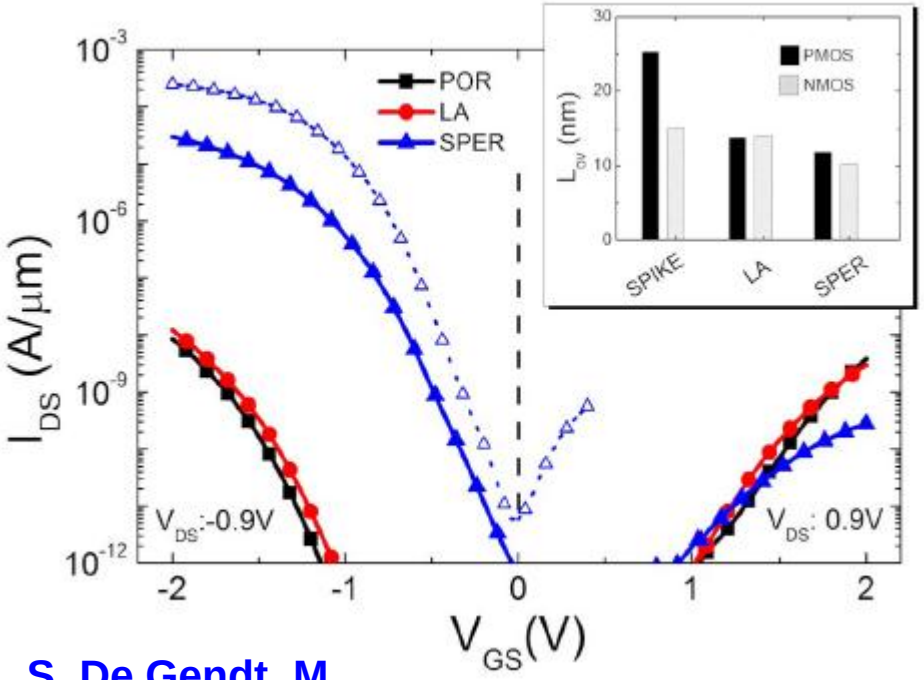


A. Verhulst, Node workshop, Zurich, 2009.

All-Si Multiple-Gate Tunnel FET

- Ion=46μA/μm and I_{OFF} of 5pA/μm at V_{DD}=-1.2V demonstrated for narrow fin Tunnel FETs by IMEC.
- Implant optimization study carried out: spike anneal ('**SPIKE'**), sub-ms laser anneal ('**LA'**) and low temperature anneal for Solid Phase Epitaxy Regrowth ('**SPER'**).

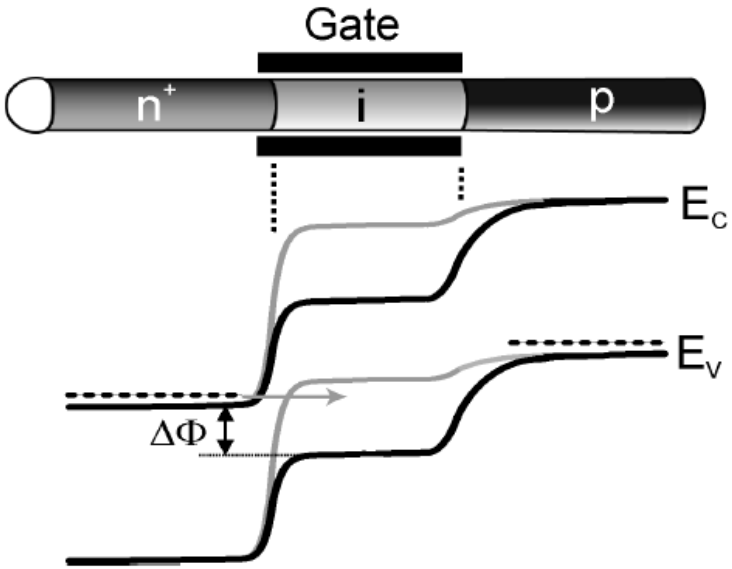




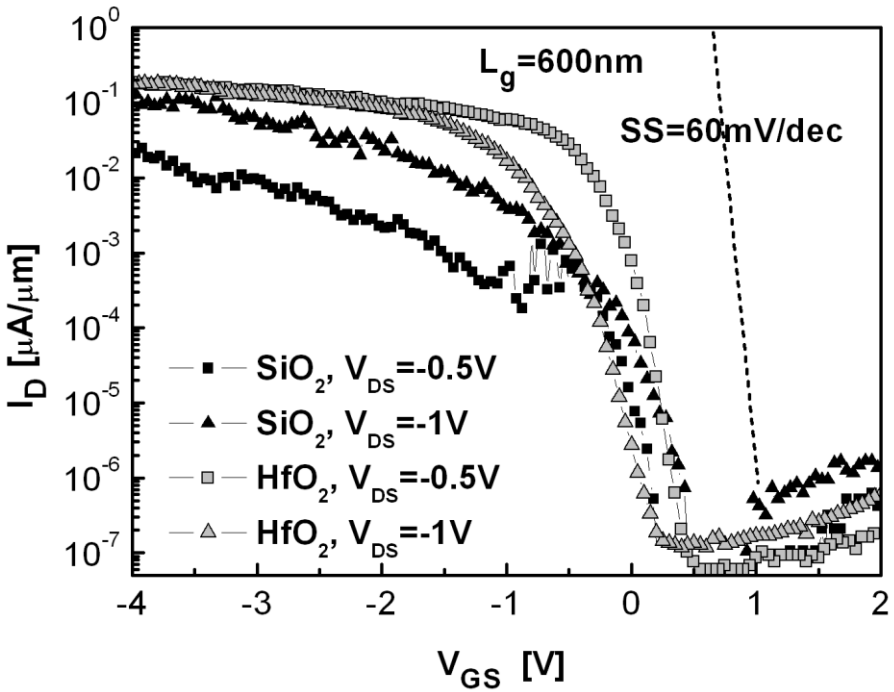
D. Leonelli, A. Vandooren, R. Rooyackers, S. De Gendt, M. M. Heyns, G. Groeseneken, ESSDERC 2010.

Bottom-up NW Tunnel FETs

VLS grown Si NWs tunnel FETs with different gate stacks (SiO_2 and HfO_2); the use of a high-k gate dielectric markedly improves the TFET performance in terms of average slope and on-current.



Ion~0.3uA/um, I_{on}/I_{off} ~10^5

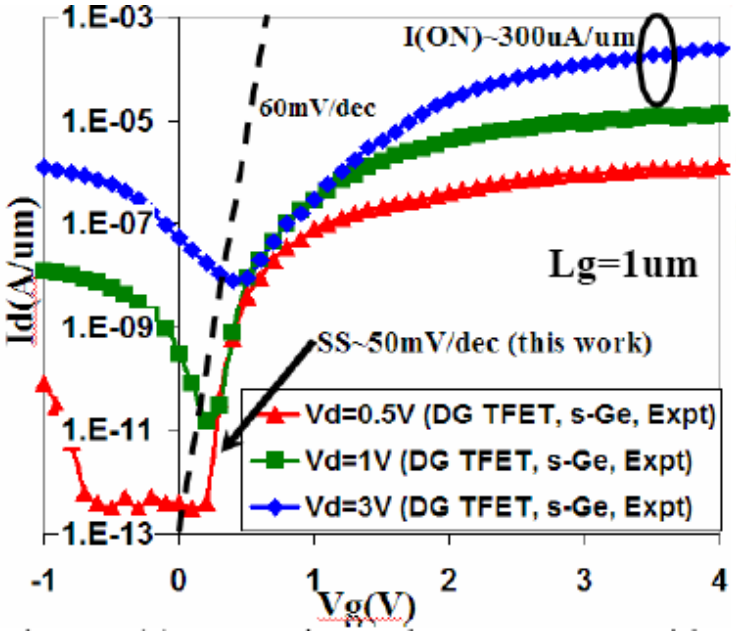


K. Moselund et al, ESSDERC 2009, DRC 2008, TED 2011.

Experimental Ge-source Tunnel FETs

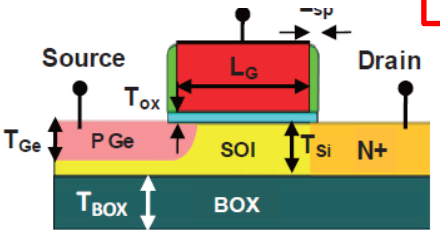
Ion/Ioff ~3.10^6 @ Vdd=0.5V

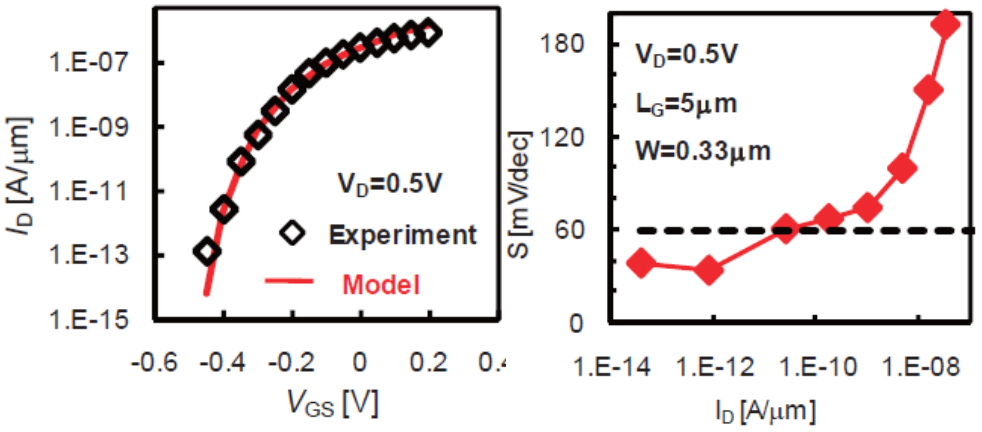
Ion ~ 300μA/μm @ Vd=3V
Ion ~ 10μA/μm @ Vd=1V
Ion ~ 0.2μA/μm @ Vd=0.5V
S=50mV/dec



T. Krishnamohan et al, IEDM 2008.

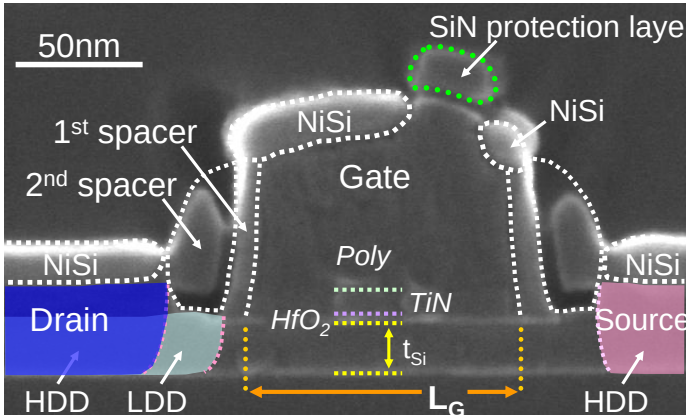
	Ref. [4]	Ref. [7]	Ref. [8]	This Work
Structure	Si TFET	SiGe TFET	s-Ge TFET	Ge TFET
T_{ox}(nm)	2(SiO_2)	3(HfO_2)	20(LTO)	3(SiO_2)
L_G(nm)	70	100	1000	5000
@ V_D (V)	1	1.2	0.5	0.5
I_{ON}(μA/μm)	12.1	0.009	0.001	0.42
I_{OFF}(pA/μm)	5400	8	0.3	0.12
I_{ON}/I_{OFF} for V_{DD}=0.5V	6E3	3E3	4E4	3E6



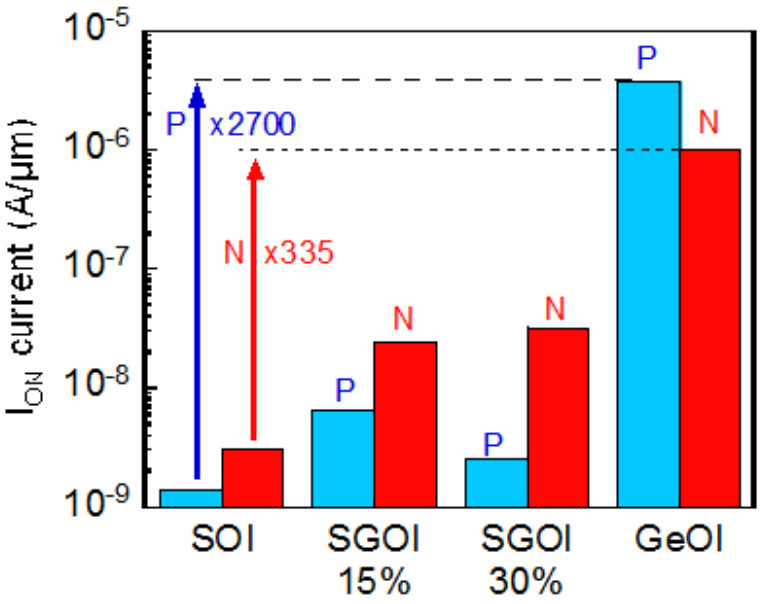


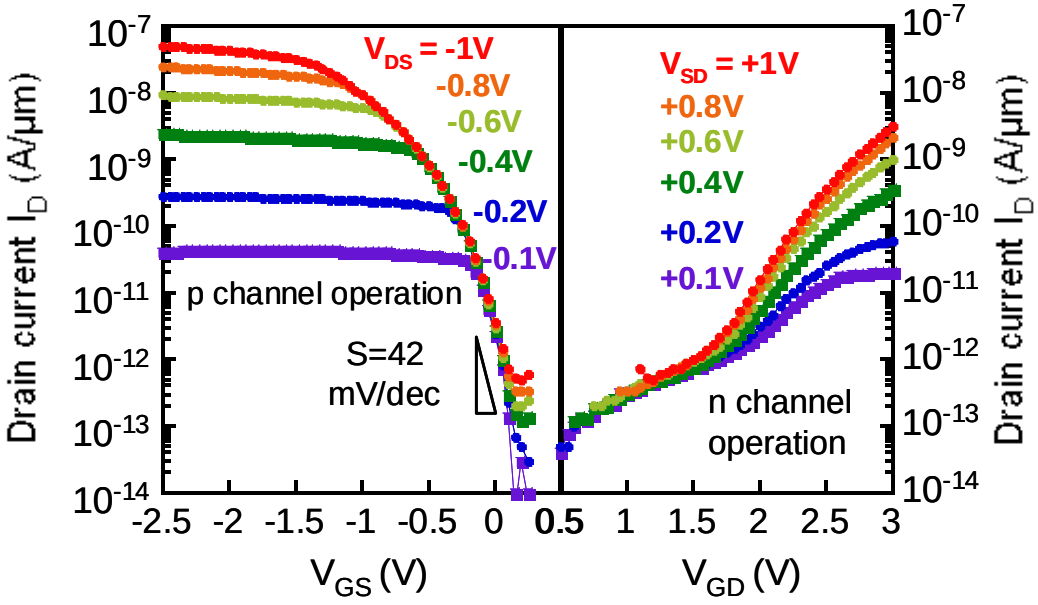
S. Kim, H. Kam, C. Hu and T.-J. King Liu, VLSI 2009.

SOI, SGOI, GeOI tunnel FETs



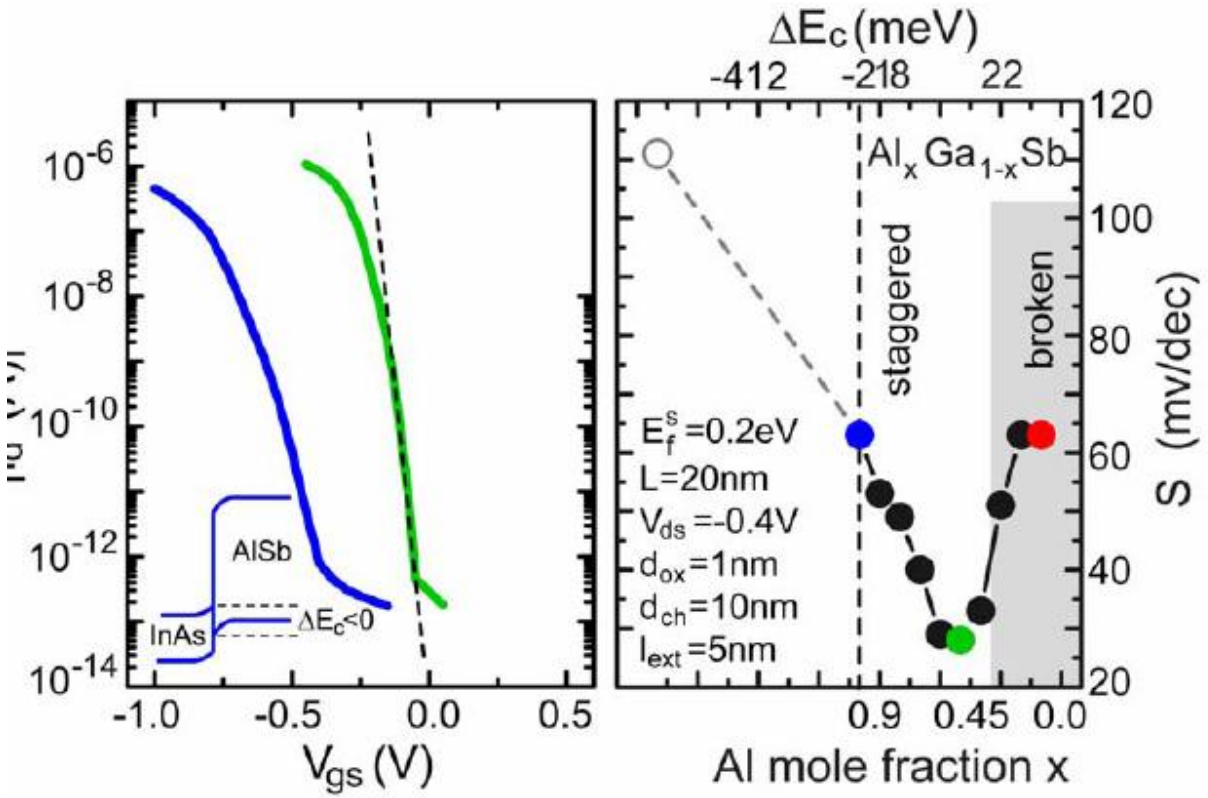
Technology boosters + contact engineering.
Various types of substrates studied.



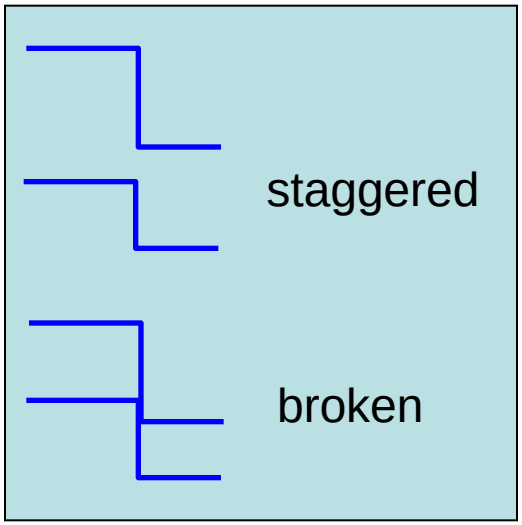


Courtesy of Cyrille Le Royer: CEA-LETI @ IEDM 2008 & ULIS 2010.

Heterojunction Tunnel FETs: staggered vs. broken band line-up



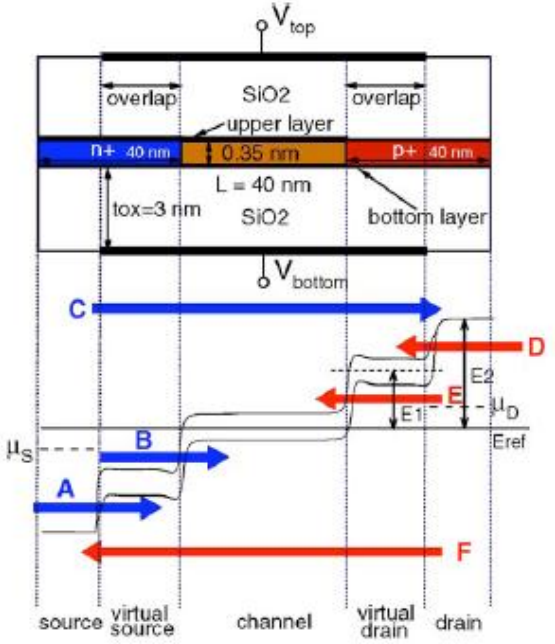
- High on state performance predicted
- minimal S value in the case of staggered band line-up



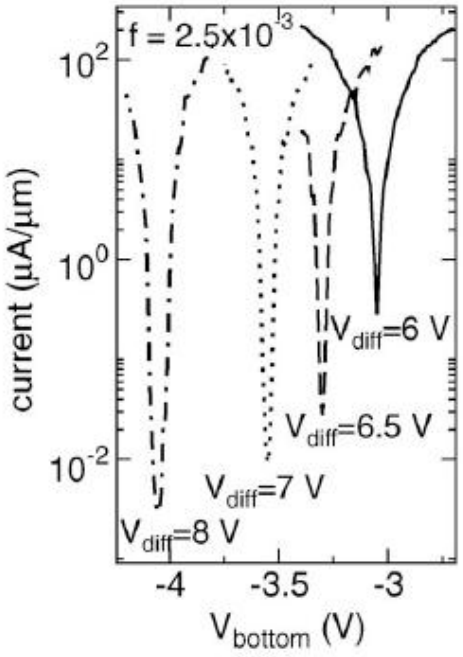
J. Knoch, Proc. 2009 Internat. Symp. VLSI-TSA, 45 (2009).

Graphene Tunnel FET

- **Ultralow-Voltage Bilayer Graphene Tunnel FET with electrostatically tuned bandgap** for Vd=0.1V,
- Solution of the coupled Poisson and Schrödinger equations in three dimensions, within the nonequilibrium Green's function formalism on a Tight Binding Hamiltonian.
- low quantum capacitance of bilayer graphene allows the BG-TFET to have most of the advantages of 1-D TFETs



(a)



(b)

I_{on}/I_{off} RATIOS, E_{gap} COMPUTED IN THE MIDDLE OF THE CHANNEL $\mathcal{E}$, THE ELECTRIC FIELD IN THE MIDDLE OF THE CHANNEL, AND SUBTHRESHOLD SWING S FOR DIFFERENT V_{diff}

V_{diff} (V)	I_{on}/I_{off}	E_{gap} (eV)	$\mathcal{E}$ (MV/cm)	S (mV/dec)
6	147	0.24	9.45	21
6.5	885	0.25	10.23	13
7	2822	0.260	11.02	12
8	4888	0.274	12.59	14

G. Fiori and G. Iannaccone, IEEE EDL, 2009.

Tunnel FET: basic modeling

$$I = AV_{eff}\xi \cdot \exp(-\frac{B}{\xi})$$

$$S = (d\log I_d / dV_{gs})^{-1}$$

$$= \ln 10(\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{gs}} + \frac{\xi + B}{\xi^2}\frac{d\xi}{dV_{gs}})^{-1}$$

$$S = \frac{V_{GS}^2}{2V_G + B_{Kane}E_g^{3/2}/D}$$

$$S\Big|_{V_G \to 0} \to 0$$

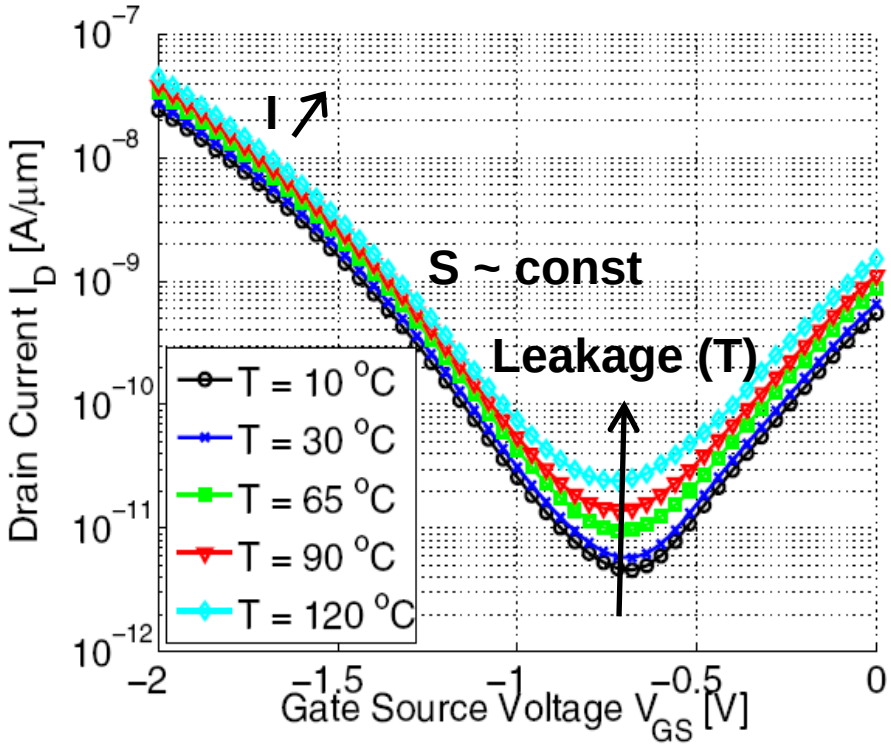
- S is gate bias dependent: lowest @ lowest V_G
- B_{Kane} depends on effective mass
- D depends on tox, L, Vds, dopings

Recent model advancements by IBM and IMEC.

Unique temperature stability

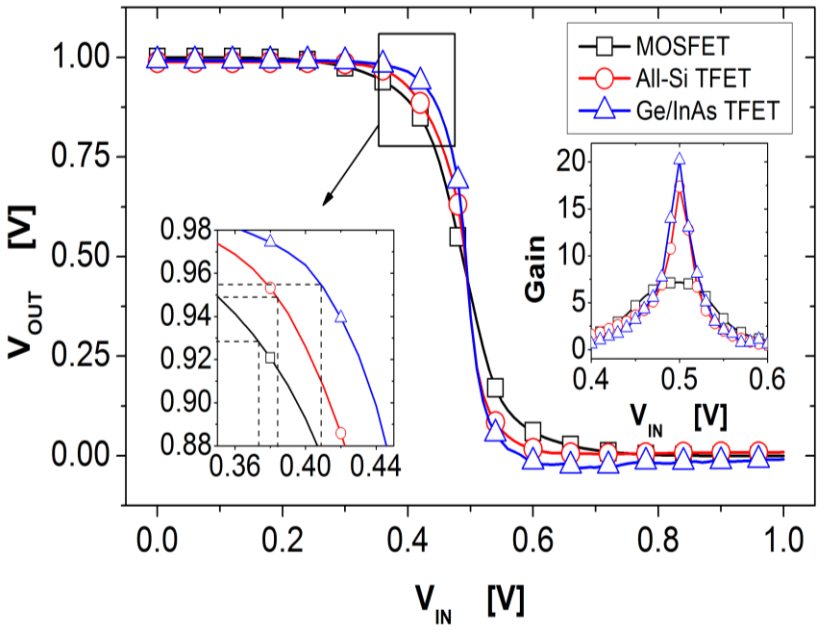
- the S of TFET is weakly dependent on the temperature via the semiconductor band gap, E_G.
- the leakage floor of TFETs determined by Shockley–Read–Hall GR current exponentially increases with temperature
- Correct Tunnel FET behavior can be experimentally checked by the temperature insensitivity of the subthreshold swing.
- Interesting for analog applications with high temperature stability.

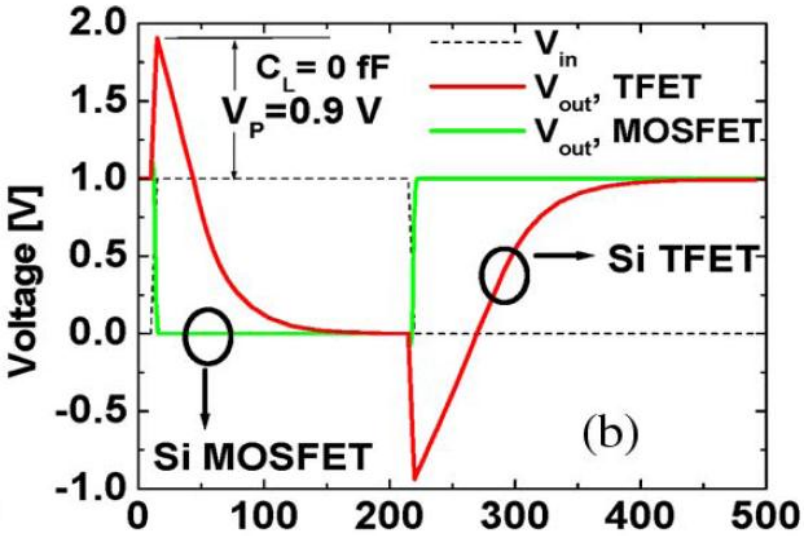
$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta}$$



Complementary Tunnel FET inverter versus CMOS

- 50nm all-Si and 50nm Ge/InAs C-TFET inverters have **better noise margins, more abrupt transition and higher gain** than 65 nm CMOS
- Problem: **slower transient than CMOS and overshoot peaks** due to critical Millet effect (in a Tunnel FET the gate capacitance Cgg is dominated by the Cgd under all bias conditions, which is in strong contrast to a MOSFET). This effect is reduced in heterostructure C-TFET.





Energy and performance: Tunnel FETs versus FinFET & PD SOI

- **Tunnet FET offer better energy efficiency for applications up to 1GHz.**

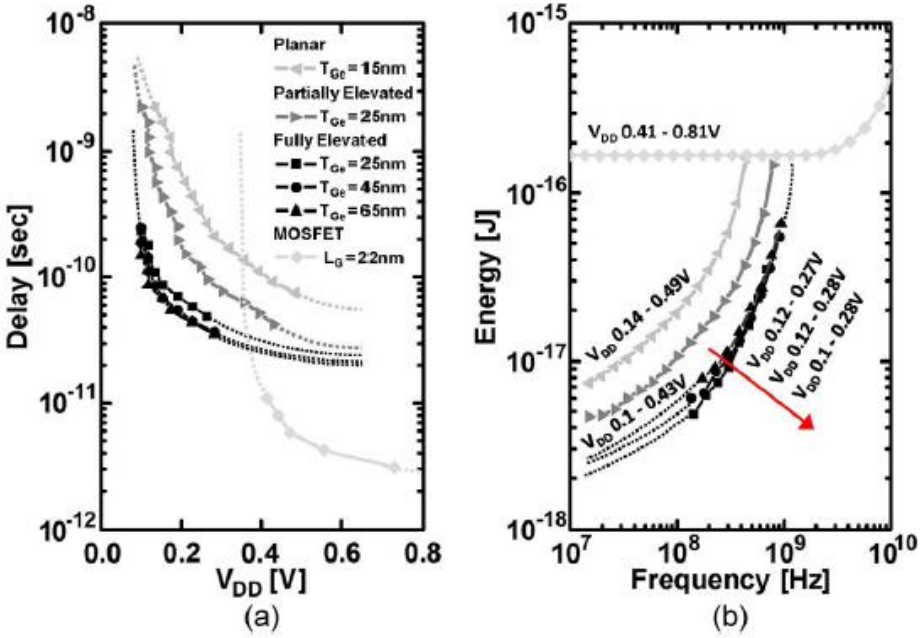
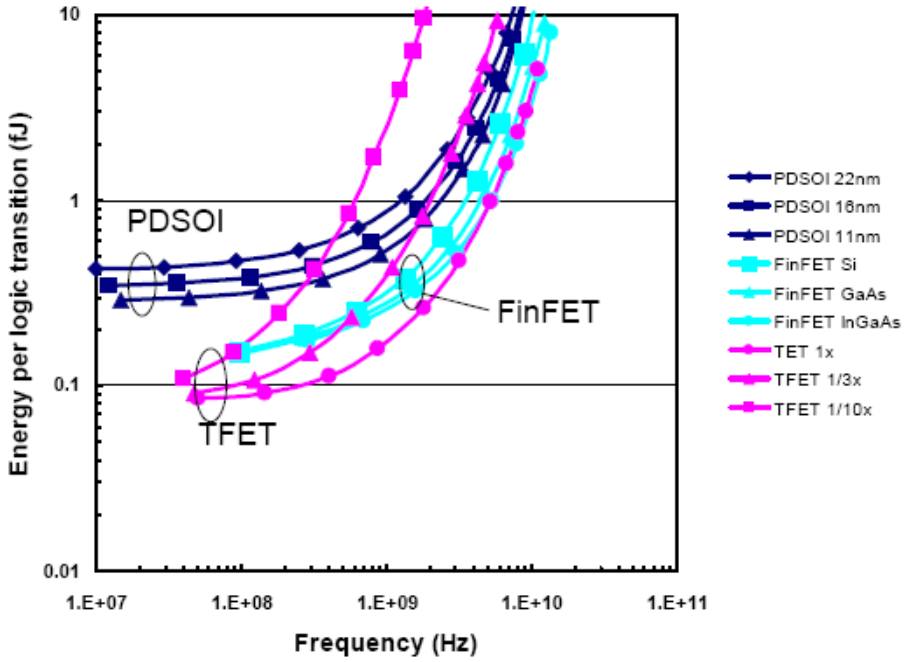


Fig. 4. Simulated (a) minimum-energy delay versus V_{DD} and (b) energy/cycle versus frequency of the TFETs versus MOSFET for a 30-stage FO1 inverter chain (activity factor = 0.01). Projections are indicated by the dotted lines.

Ge-source TFET

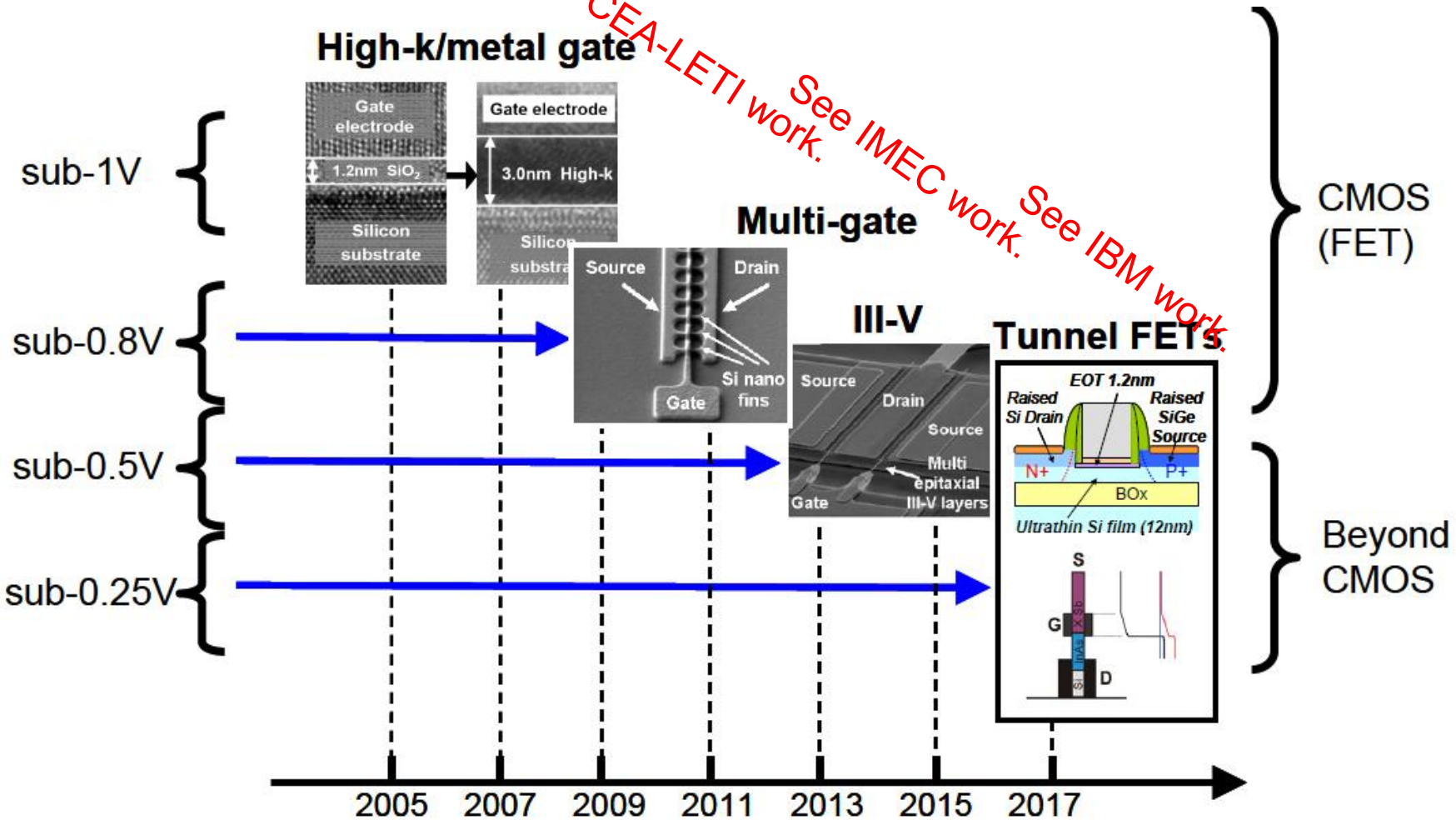
Source: S.Kim, C. Hu, T.-J. King Liu, IEEE EDL, Oct 2010.



TFET with Ion 1x, 1/3x, 1/10x

Source: D.J. Frank, IBM, Node Workshop, Zurich, 2009.

Possible roadmap



Conclusions (1)

- Opportunities:
  - **Tunnel FET stands as the most promising steep slope switch candidate to reduce the supply voltage below 0.5 V and offer significant power dissipation savings.**
  - Because of their low I_{off}, they appear suited for low power and low standby power logic applications operating at moderate frequency (hundreds of MHz).
  - Other promising applications of TFETs: ultra-low power specialized analog integrated circuits with improved temperature stability and low-power SRAM.
  - hybrid CMOS complementary TFET design, with TFETs as an add-on ultra low power device option on advanced CMOS platforms.

Conclusions (2)

- Challenges and perspectives:
  - **achieve high Ion without degrading Ioff, combined with a subthreshold swing of less than 60 mV/decade over more than four decades of drain current.**
  - Additive combination of specific technology boosters.
  - Carbon materials (graphene and carbon nanotubes) are well-suited for high-performance Tunnel FETs due to their ultra-thin body thickness and their one-dimensional transport characteristics but face enormous challenges for experimental implementation.
  - **Heterostructure Tunnel FETs offer the best performance compromise for complementary logic through advanced band engineering, using Ge- and InAs-sources on silicon platforms for n- and p-type Tunnel FETs in ultra-thin films or nanowires.**

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Backup: C-Tunnel FET