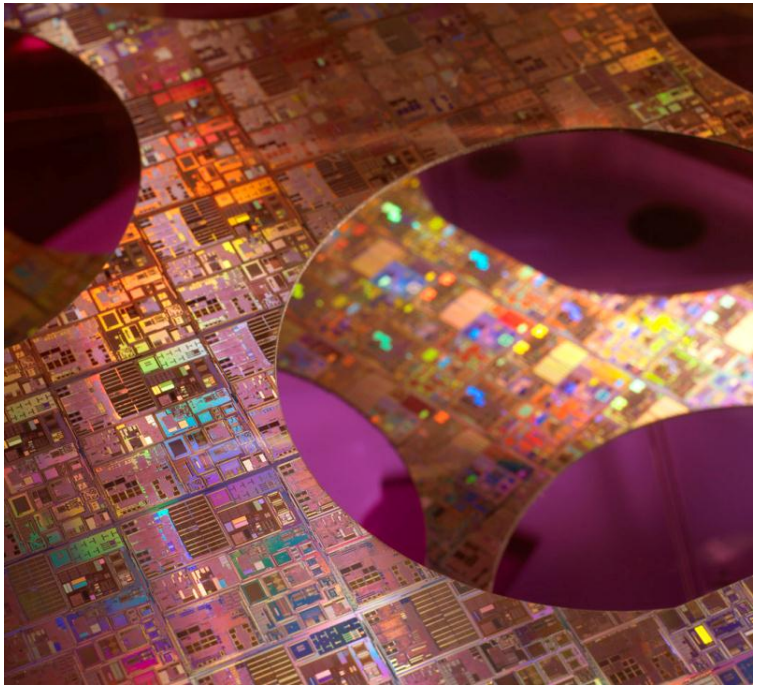
New computing paradigms:

How magnetism can help CMOS microelectronics?



B.Dieny

SPINTEC, CEA/Grenoble, France

OUTLINE

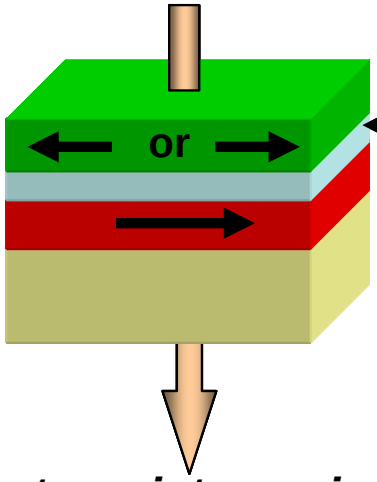
- Spin-electronics
- Progresses on STT-MRAM and Thermally Assisted MRAM
- “Logic-in-memory” architectures, “normally-off-electronics”, expected benefits
- A few words on alternative approaches:
  - Analogic computing (neuromorphic architecture)
  - Quantum computing and emerging approaches
  - RSFQ

TUNNEL MAGNETORESISTANCE

Tunnel magnetoresistance at RT in magnetic tunnel junctions:

Julliere (1975) mais seulement à basse T
Moodera et al, PRL (1995);
Myazaki et al, JMMM(1995).

TMR~40-70%

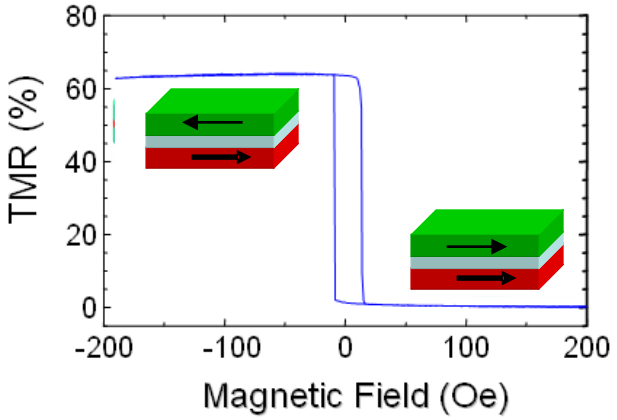


Free layer: CoFe 4 nm

Al_2O_3 barrier 1.5nm

Reference layer :CoFe 3nm

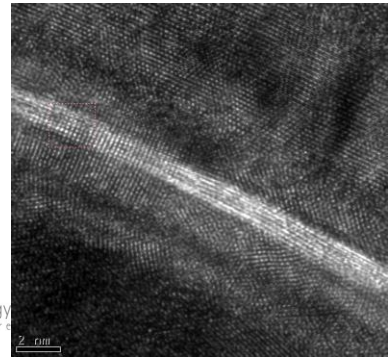
IrMn 7nm



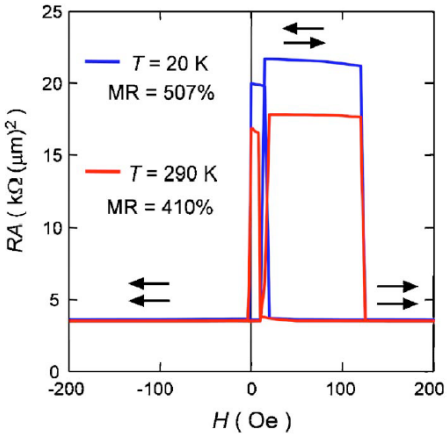
Giant tunnel magnetoresistance in crystalline MgO based MTJ

Parkin et al, Nature Mat. (2004);
Yuasa et al, Nature Mat. (2004).

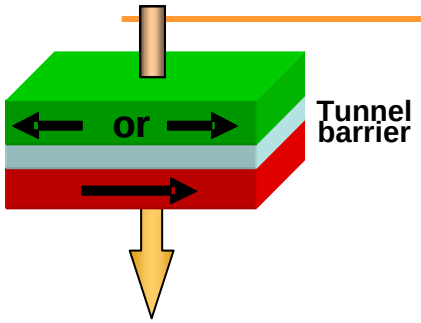
TMR~200-500%



Au cap 50 nm
Ir-Mn 10 nm
Fe(001) 10 nm
Co(001) 0.57 nm
MgO(001) 2.2 nm
Co(001) 0.57 nm
Fe(001) 100 nm
MgO(001) 20 nm
MgO(001) sub.

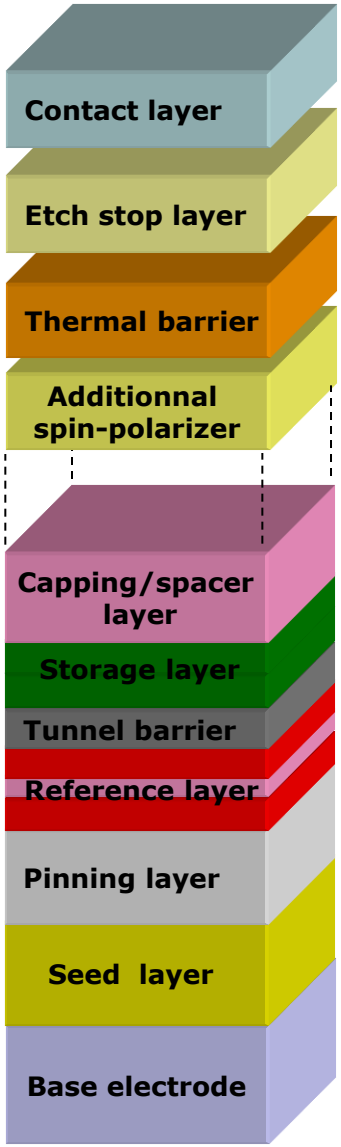


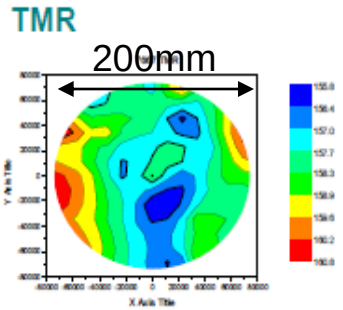
MRAM BUILDING BLOCK : THE MTJ



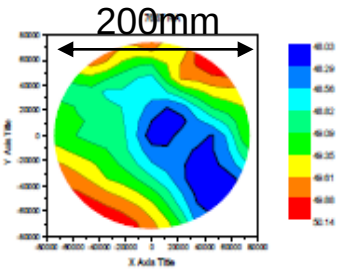
$$TMR = \frac{R_{\uparrow\downarrow} - R_{\uparrow\uparrow}}{R_{\uparrow\uparrow}}$$

~150-200%
(up to 500% with MgO)

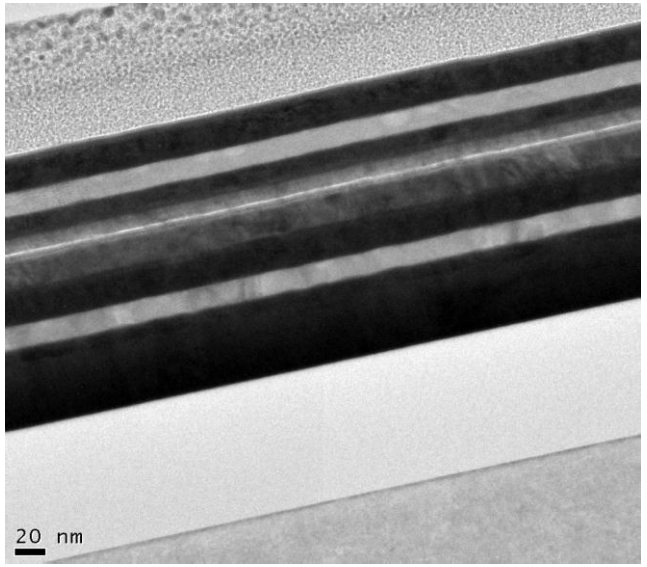




158.2%
1.0% (1sigma)



49.1 Ohm µm²
1.3% (1sigma)



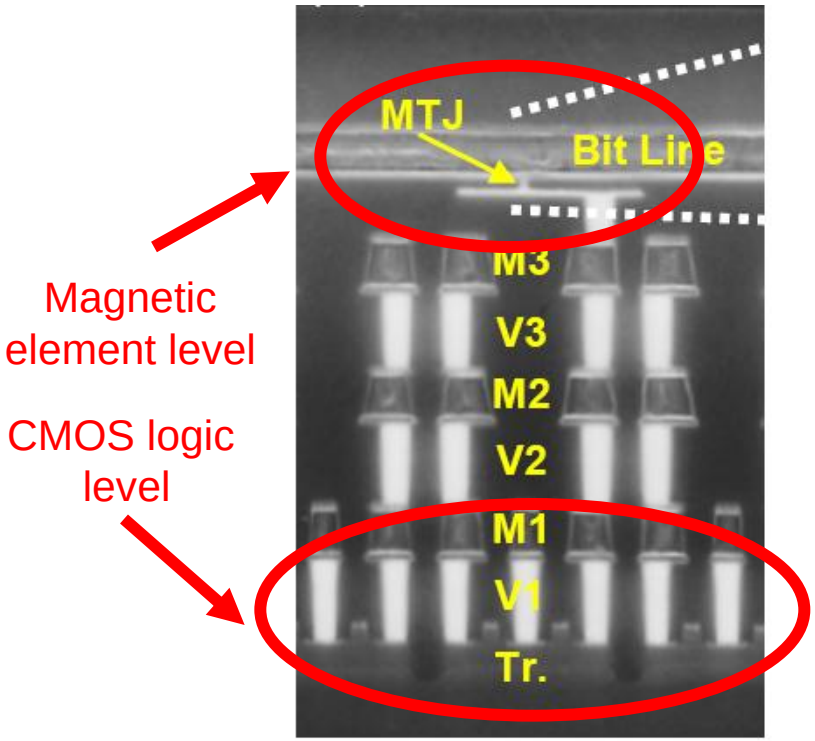
Contact to select transistor + diffusion barrier

Complex but mastered for volume manufacturing
(1 millions heads / day since 7+ years !)

PROCESS MATURITY

MRAM process « easy » to implement

- Resistance compatible with CMOS (cell R ~ kΩ)
- MTJ used as a variable resistance driven by field or current/voltage (STT)
- Above IC technology ('end-of-back-end' process)
- Front-end contamination under control (cf. SVTC, Tower, TSMC, …)
- Low-T BE process (250° C) compatible with Cu interconnect process
- Easy / cheap to embed (3 add-masks, no trade-off with logic process)



MRAM process well established
Fear for contamination (slowly) vanishing
Several fabs now enabled with 200/300mm lines

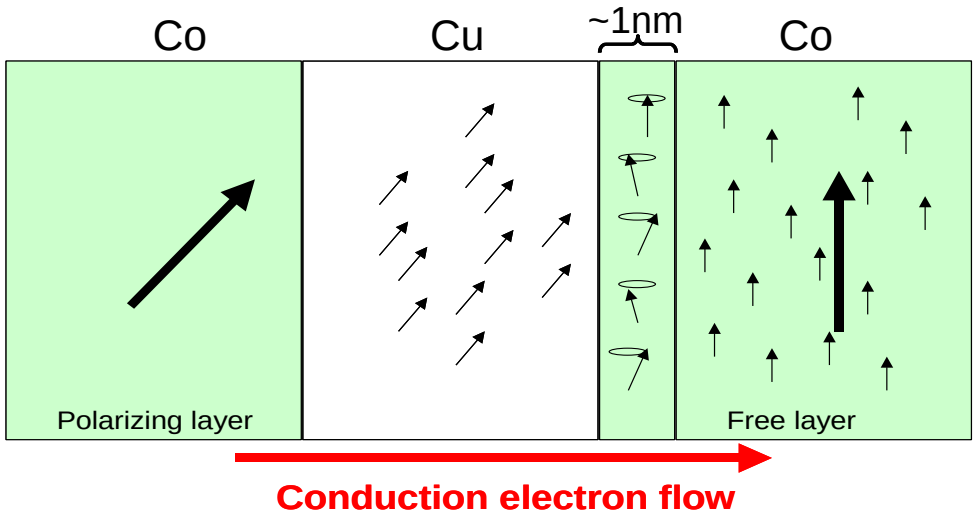
tsmc SAMSUNG freescale semiconductor TOWERJAZZ hynix

SPIN TRANSFER

Predicted by Slonczewski (JMMM.159, L1(1996)) and Berger (Phys.Rev.B54, 9359 (1996)),

Tunnel magnetoresistance:
A magnetization is used to control an electrical current

Spin transfer is the reciprocal effect:
A spin polarized current can act on a magnetization



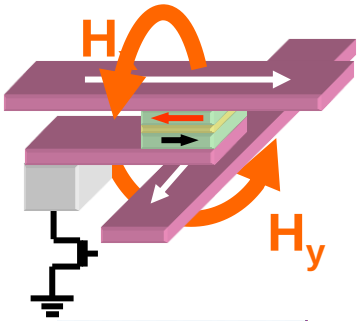
M.D.Stiles et al, Phys.Rev.B.66, 014407 (2002)

Spin-transfer: Magnetic torque exerted by the spin polarized current on the local magnetization due to exchange interactions between the spin of the conduction electrons and the spin of the electrons responsible for the local magnetization

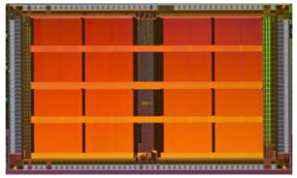
⇒ **New way to manipulate the magnetization of magnetic nanostructures**

THERE ARE MANY MRAM !

Field-only « Toggle »



EVERSPIN TECHNOLOGIES



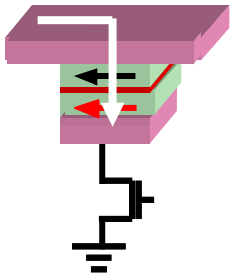
Freescale 4Mb (2006)

Established technology
1.5M units shipped
4.5M forecasted in 2011
Infinite endurance

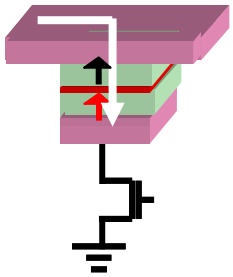
Scalable down to 65nm
(Write power increase, electromigration issues)

Spin Transfer Torque « STT » or « SPRAM »

Planar



Perpendicular

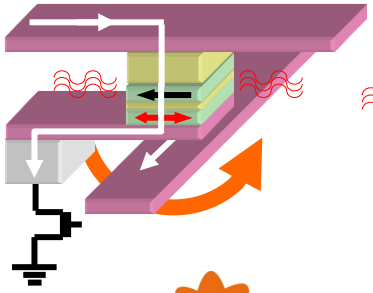


hynix SAMSUNG TOSHIBA HITACHI Inspire the Next
NEC GRANDIS AvalancheTechnology
Headway Technologies FUJITSU RENESAS QUALCOMM

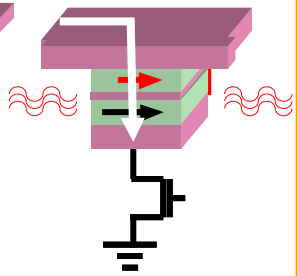
Lowest write current
(<100µA, scales with shrink)
Minimal cell / array size
(~15F², soon not Xtor limited)
Low sensitivity to field disturb
Concern with thermal stability
(retention at small feature size<25nm)

Thermally Assisted « TAS » or « TAMRAM »

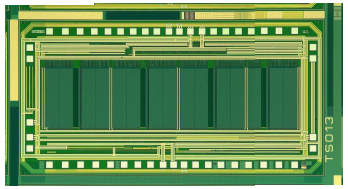
Field-TAS



STT-TAS



CROCUS Technology
Blossoming future



1Mb Field-TAS (2011)

Fully scalable
(stability / retention to <20nm)
Multibit possible

STT MRAM demonstrators

4Kbit
SONY
2005

A Novel Nonvolatile Memory with Spin Torque Transfer Magnetization Switching: Spin-RAM

M. Hosomi, H. Yamagishi*, T. Yamamoto, K. Bessho, Y. Higo, K. Yamane, H. Yamada*,
M. Shoji*, H. Hachino**, C. Fukumoto**, H. Nagao**, and H. Kano
Solid State Memories Research Laboratory, Information Technologies Laboratories, Sony Corporation
*Semiconductor Technology Development Group, Semiconductor Solution Network Company, Sony Corporation
**Memory Design Section 3, LSI Library Design Department, System LSI Products Division 1, Sony Semiconductor Kyushu Corporation
4-14-1, Asahi, Atsugi, Kanagawa 243-0014, Japan
Phone: +81-46-230-5662, FAX: +81-46-230-5730, E-mail: Masanori.Hosomi@jp.sony.com

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 1, JANUARY 2008

2Mbit
Tohoku/Hitachi
2008

2 Mb SPRAM (SPin-Transfer Torque RAM) With Bit-by-Bit Bi-Directional Current Write and Parallelizing-Direction Current Read

Takayuki Kawahara, *Fellow, IEEE*, Riichiro Takemura, Katsuya Miura, Jun Hayakawa, Shoji Ikeda, Young Min Lee, Ryutaro Sasaki, Yasushi Goto, Kenchi Ito, Toshiyasu Meguro, Fumihiro Matsukura, Hiromasa Takahashi, Hideyuki Matsuoka, and Hideo Ohno, *Member, IEEE*

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 4, APRIL 2010

32Mbit
Tohoku/Hitachi
2010

A 32-Mb SPRAM With 2T1R Memory Cell, Localized Bi-Directional Write Driver and '1'/'0' Dual-Array Equalized Reference Scheme

Riichiro Takemura, Takayuki Kawahara, *Fellow, IEEE*, Katsuya Miura, Hiroyuki Yamamoto, Jun Hayakawa, Nozomu Matsuzaki, Kazuo Ono, Michihiko Yamanouchi, Kenchi Ito, Hiromasa Takahashi, Shoji Ikeda, Haruhiro Hasegawa, Hideyuki Matsuoka, and Hideo Ohno, *Member, IEEE*

spintec
SPIN IN ELECTRONICS

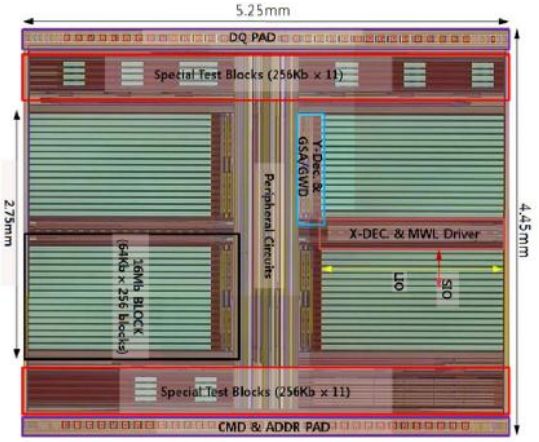
STT MRAM demonstrators

64Mbit
2010
Grandis/
Hynix

Fully integrated 54nm STT-RAM with the smallest bit cell dimension for high density memory application

Suock Chung, K.-M.Rho, S.-D.Kim, H.-J.Suh, D.-J.Kim, H.-J.Kim, S.-H.Lee, J.-H.Park, H.-M.Hwang, S.-M.Hwang, J.-Y.Lee, Y.-B.An, J.-U.Yi, Y.-H.Seo, D.-H.Jung, M.-S.Lee, S.-H.Cho, J.-N.Kim, G.-J.Park, Gyuan Jin, *A.Driskill-Smith, *V.Nikitin, *A.Ong, *X.Tang, Yongki Kim, J.-S.Rho, S.-K.Park, S.-W.Chung, J.-G.Jeong, S.-J.Hong

Hynix Semiconductor Inc., R&D Div., San136-1, Bubal-Eub, Icheon-Si, Gyonggi-Do, 467-701, S.Korea,
* Grandis Inc., 1123 Cadillac Court, Milpitas, CA, 95035, U.S.A.
Tel:+82-31-630-3214; FAX:+82+31+630-8123; Email:suock.chung@hynix.com



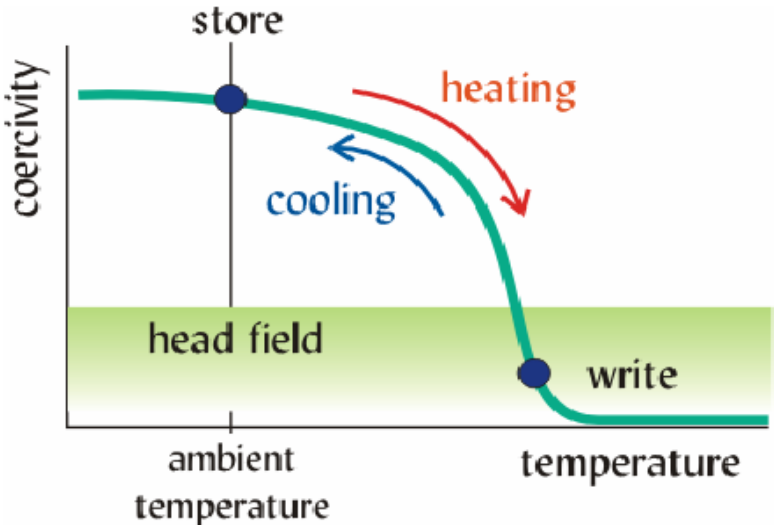
Micrograph of 64Mbit STT-RAM chip.

Table 1 Key features of 64Mbit STT-RAM chip.

Process	54nm CMOS, W SL & BL
Unit cell size	$3.5Fx4F=14F^2$ ($0.188x0.216 = 0.041um^2$)
# of Tr	2Tr / unit cell
MTJ	In-plane ($54x108nm^2$)
Chip density	64Mb (Org 4Mx16)
Chip size	$4.45x5.25mm^2$ (including 11 test blocks)
V_{DD}	1.8V

- Samsung acquired Grandis in July 2011 (Grandis holds a large number of patents on STT MRAM)
- Samsung, Hynix… look for DRAM replacement by p-STT-MRAM by 2015 below 20nm.

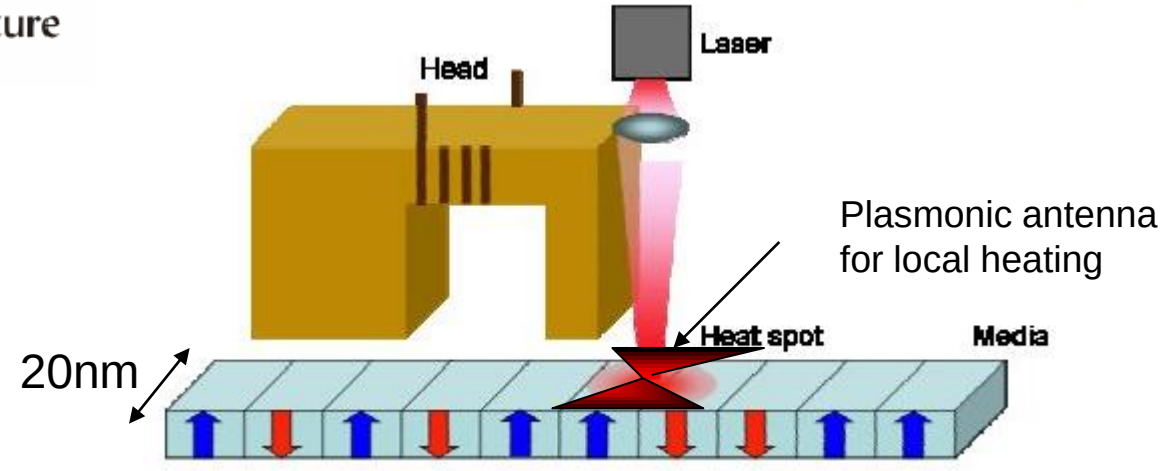
Thermally Assisted switching (TAS)



•Use temperature-dependence of switching ability

- **Write at elevated temperature**
- **Store / read at room temperature**

•Same basic concept as in **Heat Assisted Magnetic Recording.** Allows extending the areal density of stored information (smaller bits) without requiring higher field to write

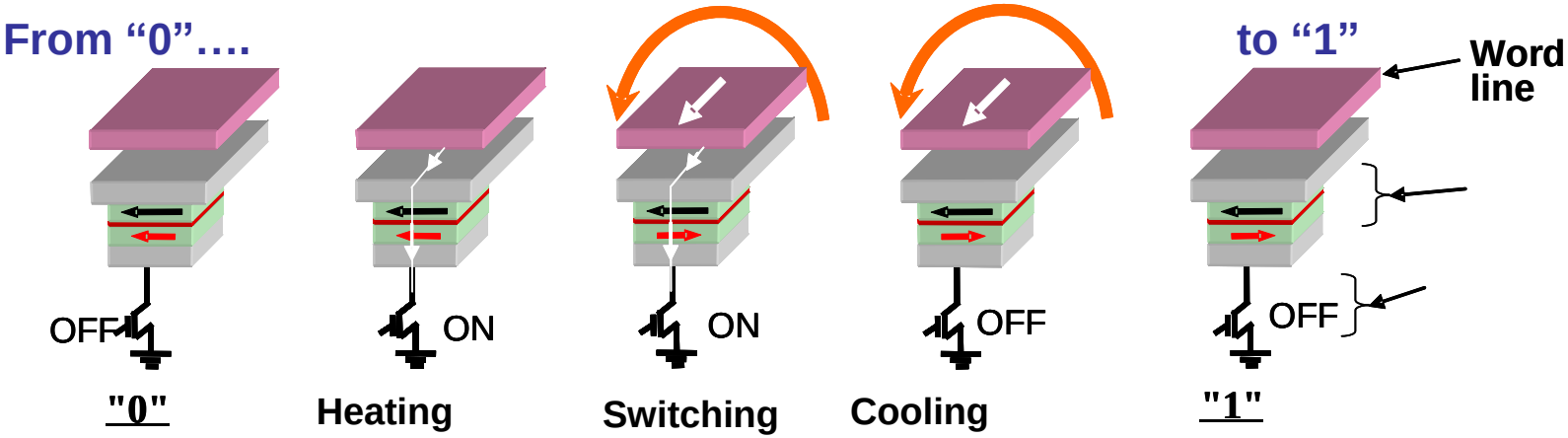


- In MTJ for MRAM, heating produced by Joule dissipation around the tunnel barrier.
- Write temperature~250° C

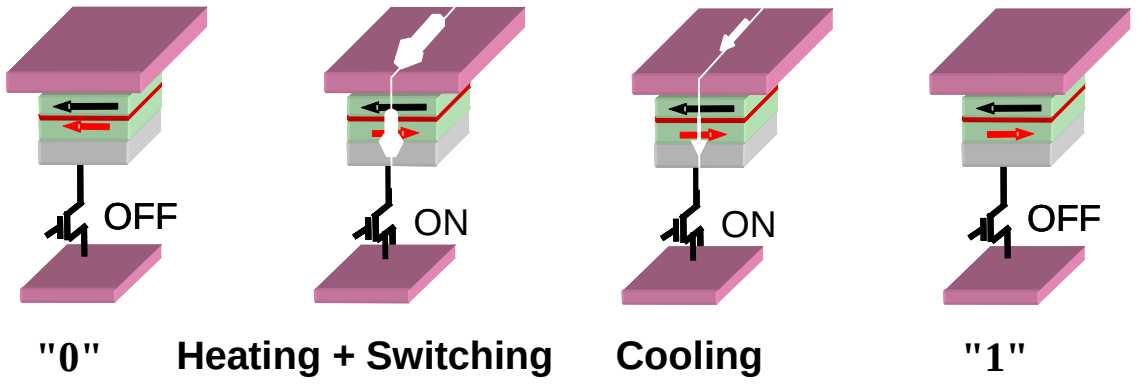
Thermally assisted MRAM

In TA-MRAM: Heating by current flowing through the cell

Heating+ pulse of magnetic field:

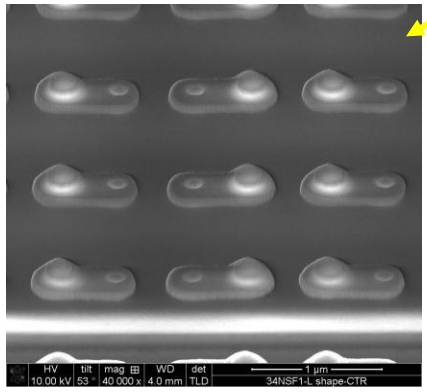


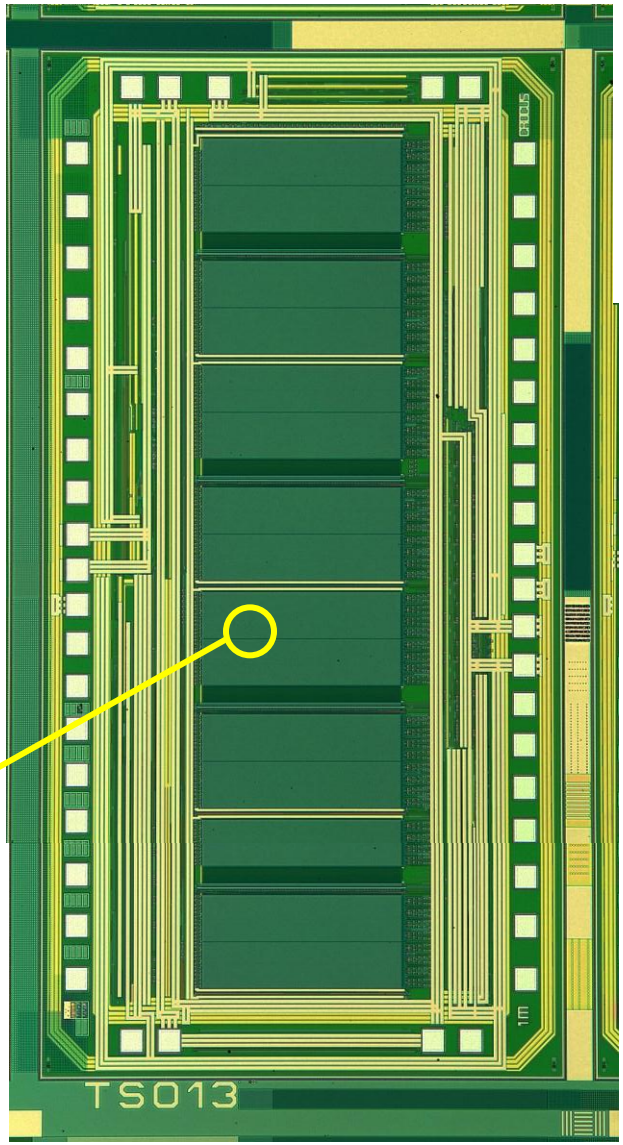
Heating + STT:



CROCUS 1MB PRODUCT (FIELD-TAS)

- Agreement to manufacture Crocus TA-MRAM products on Tower Semiconductors 130nm Cu Fab2
- Both stand-alone and embedded products will be adressed
- Start with 1Mb stand-alone SRAM compatible product, sampling 1H'11
  - 128Kx8 1Mbit MRAM w/ asynchronous SRAM interface
    130nm / 3.3V industry-standard CMOS front-end
    4 metals + magnetics
  - Timings comparable to high speed SRAM
    Read cycle time ~20ns, write cycle time 50ns
  - Low power architecture exclusive to TAS cell operation
    Icc Write ~35mA
  - Commercial T-range (0-85° C)
- Migrating to 4Mb 2H'11
- Potentially going down to
  - ~10F²
  - Icc write ~5mA
  - 10ns R/W cycle

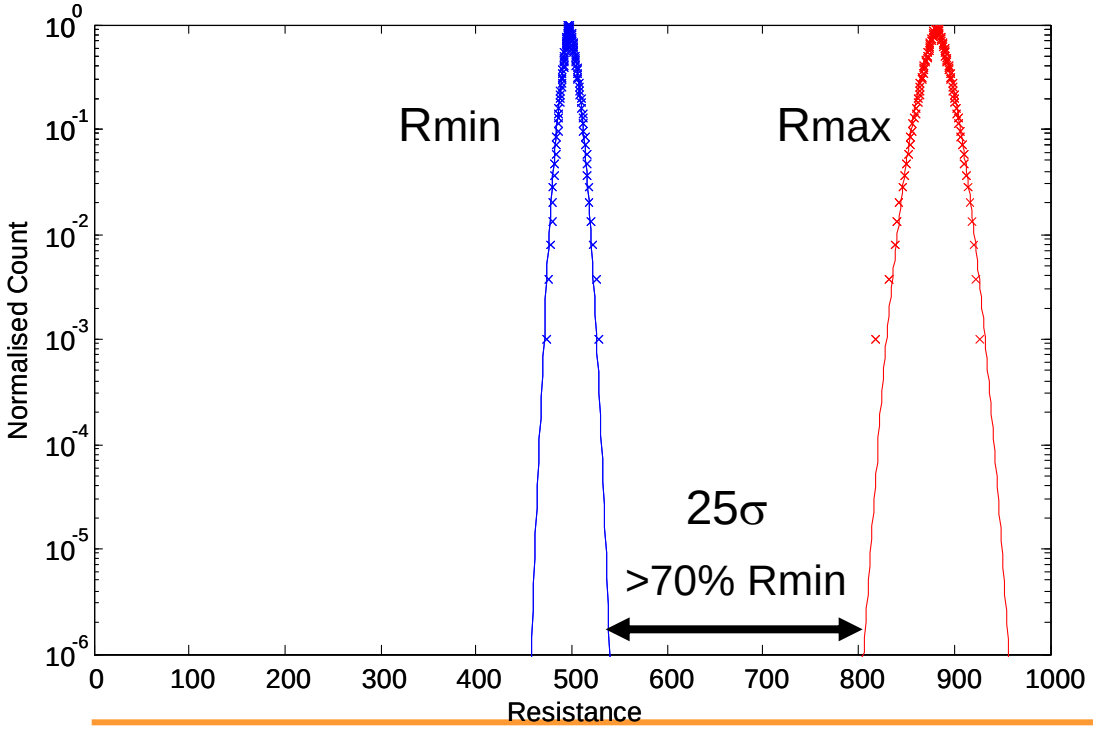




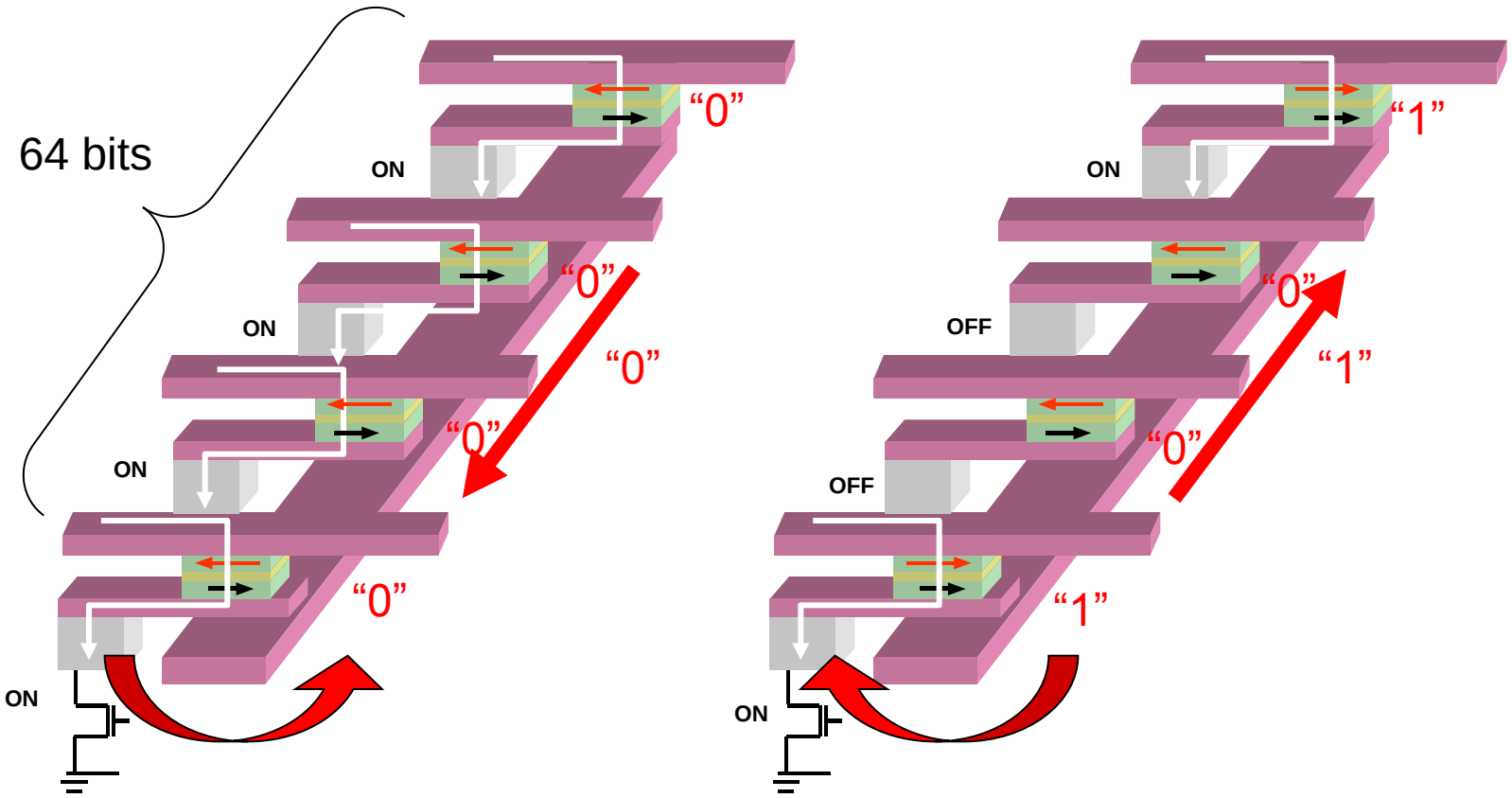
CROCUS 1MB PRODUCT (FIELD-TAS)

- Optimized storage layer materials give:
  - Low programming voltage (<0.9V)
  - 2x lower than breakdown voltage (~1.8V)
  - Clean programming levels

- Resistance distributions after programming:



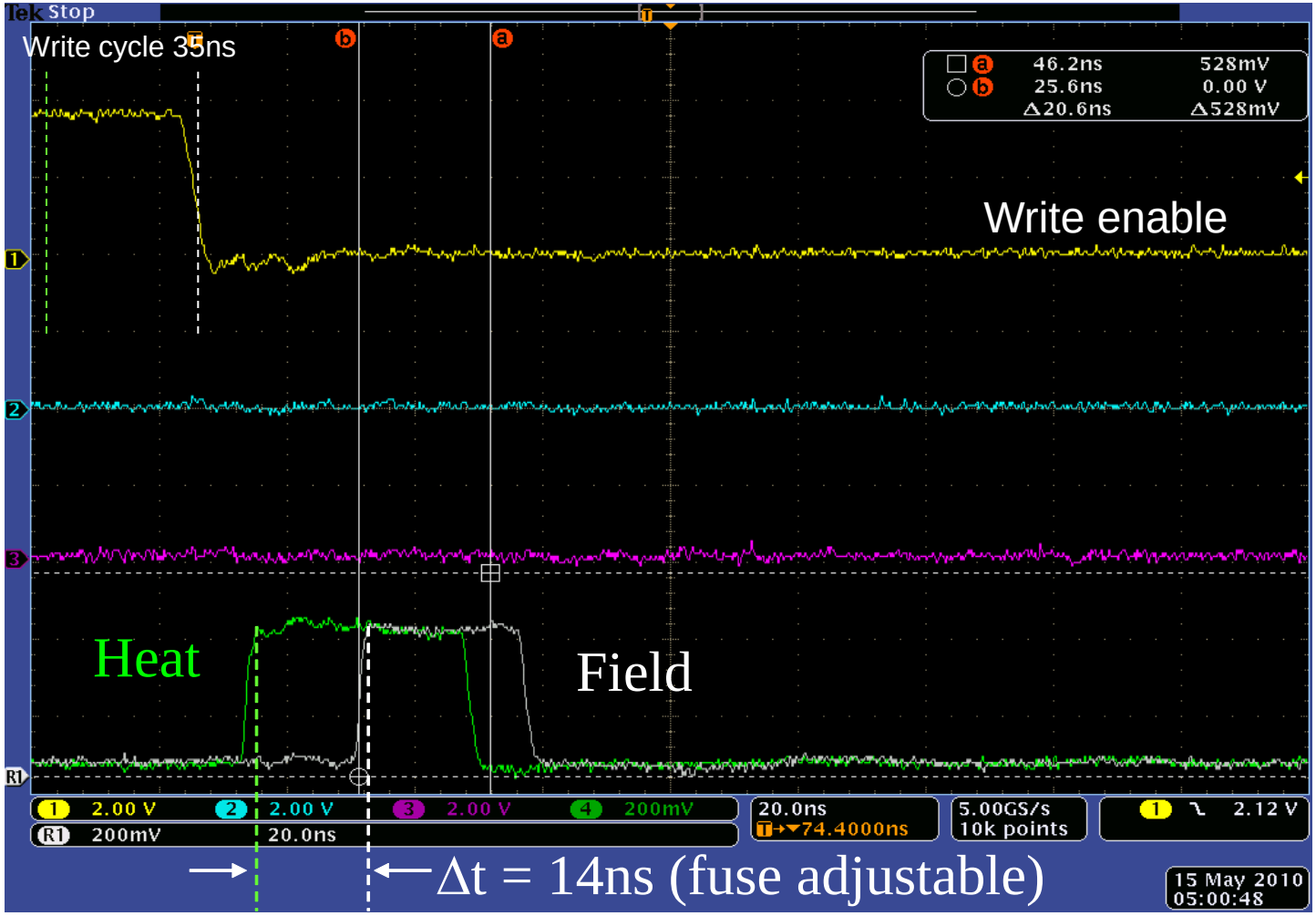
WRITE SEQUENCE (FIELD-TAS)



Only 2 pulses of field required to write 64bits. Required field ~ 5mT

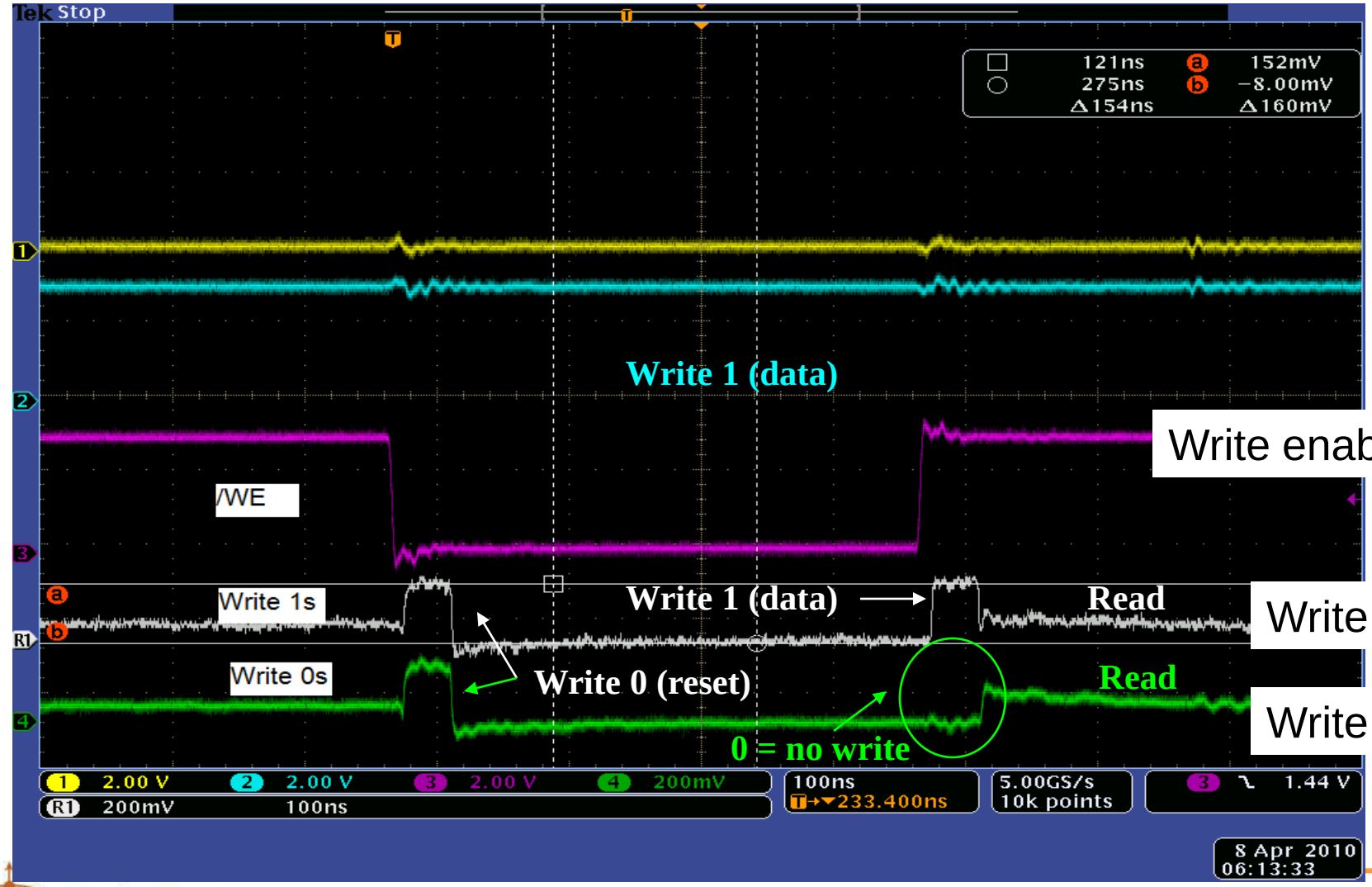
Energy per 10ns field pulse over 64bits=35pJ i.e. 0.55pJ per bit
Energy per 10ns heating pulse = 1pJ per bit, similar to STT writing

WRITE SEQUENCE (FIELD-TAS)



CROCUS 1MB PRODUCT (FIELD-TAS)

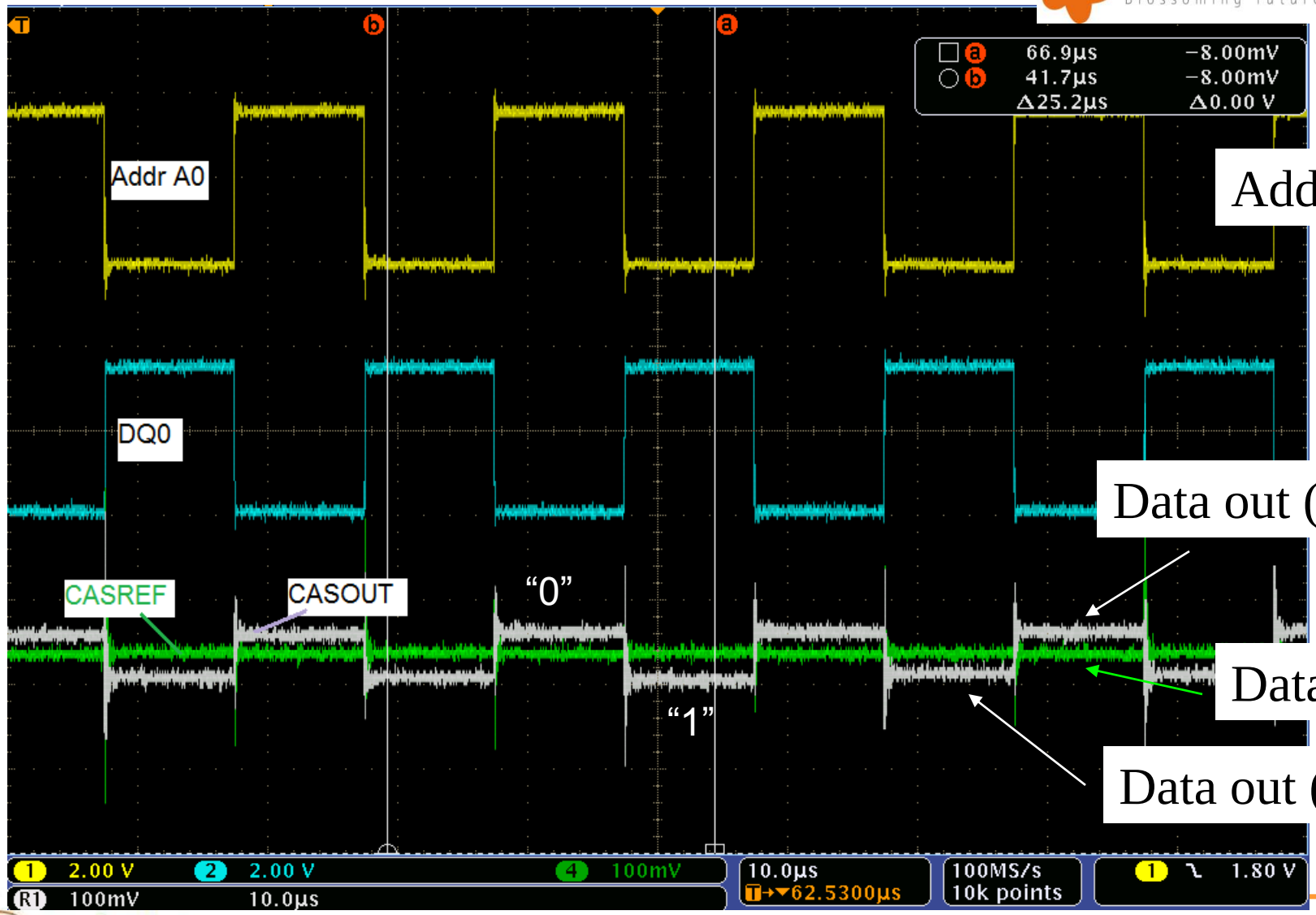
CROCUS Technology
Blossoming future



CROCUS 1MB PRODUCT (FIELD-TAS)

CASREF vs CASOUT (read cycle)-20ns

CROCUS Technology
Blossoming future



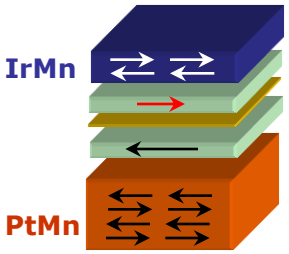
Address

Data out (R_{high})

Data ref

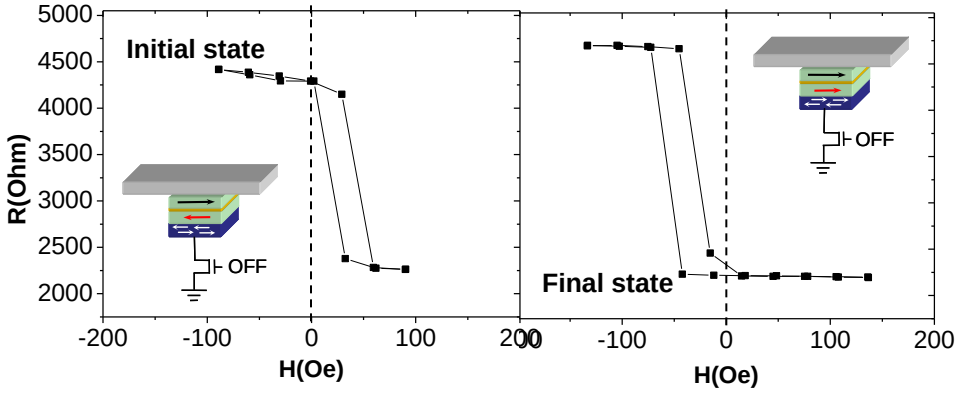
Data out (R_{low})

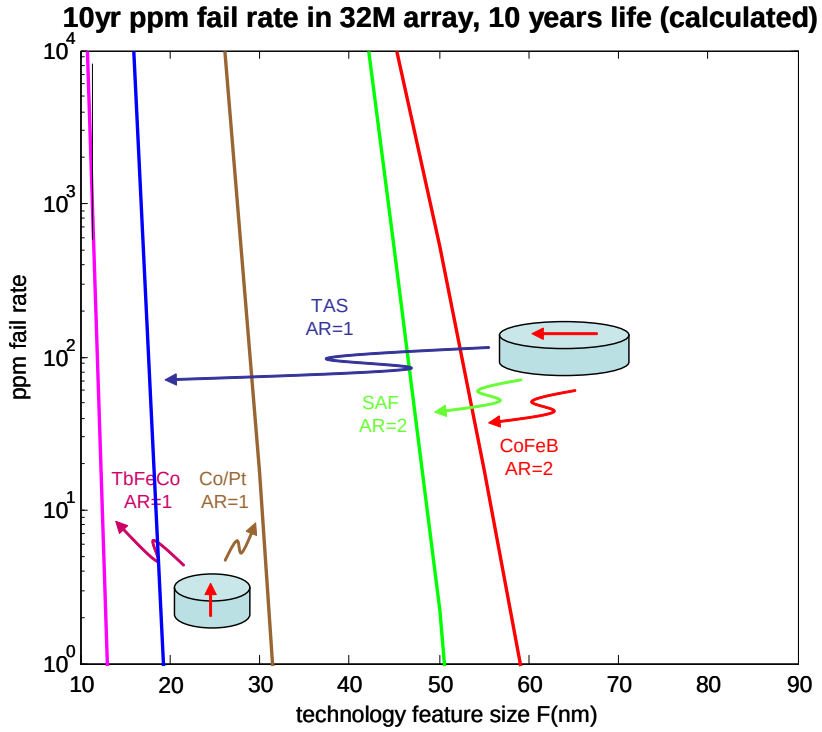
STT + TAS PROOF OF CONCEPT

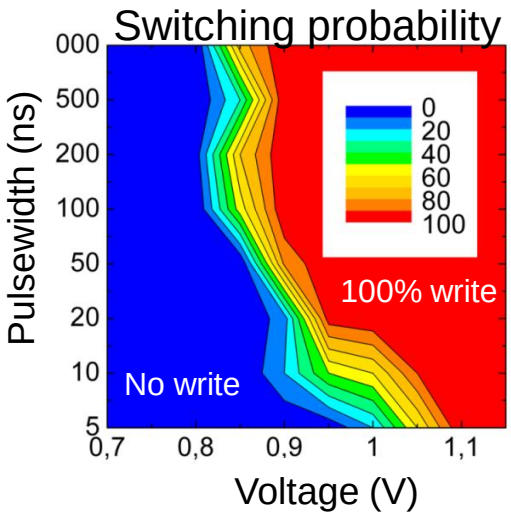


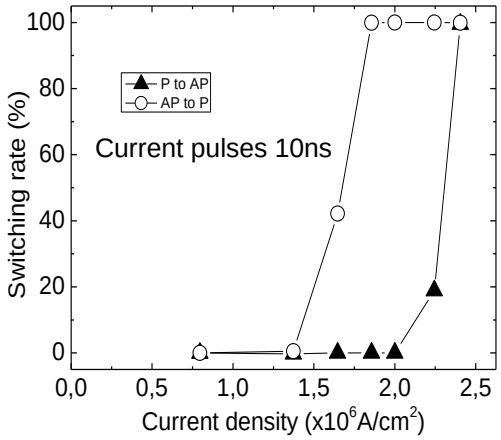
TAS-Field MTJ stack

- ❖RxA from 30Ωμm² to 10Ωμm²
- ❖ TMR up to 130%
- ❖ Cell size 50nm (circular)





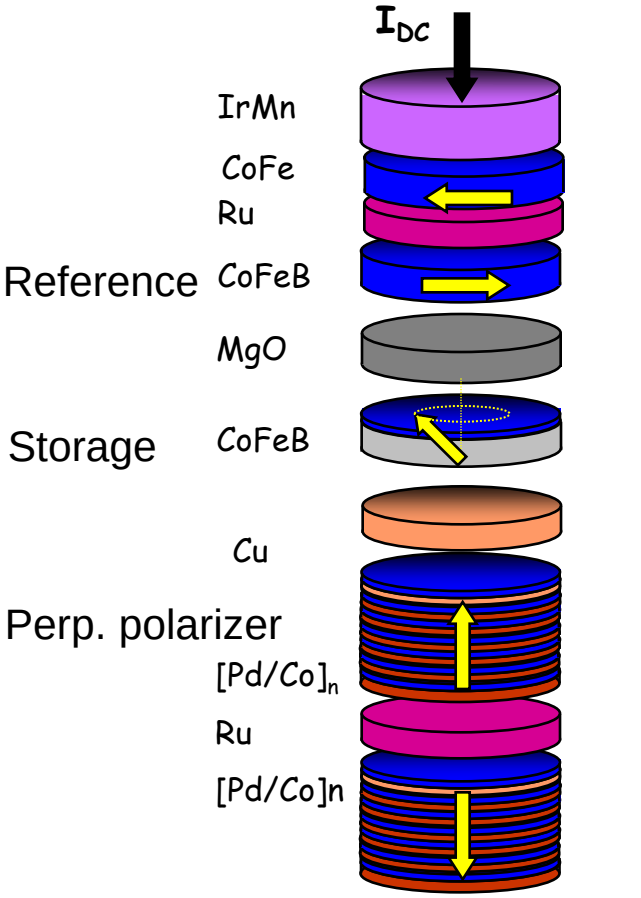




- ❖ Current density @ 10ns **Jc = 2.4 10⁶ A/cm²**
- ❖ **$KV/k_BT > 100$** at 32nm feature size (AR=1)

HOW FAST CAN MRAM BE ?

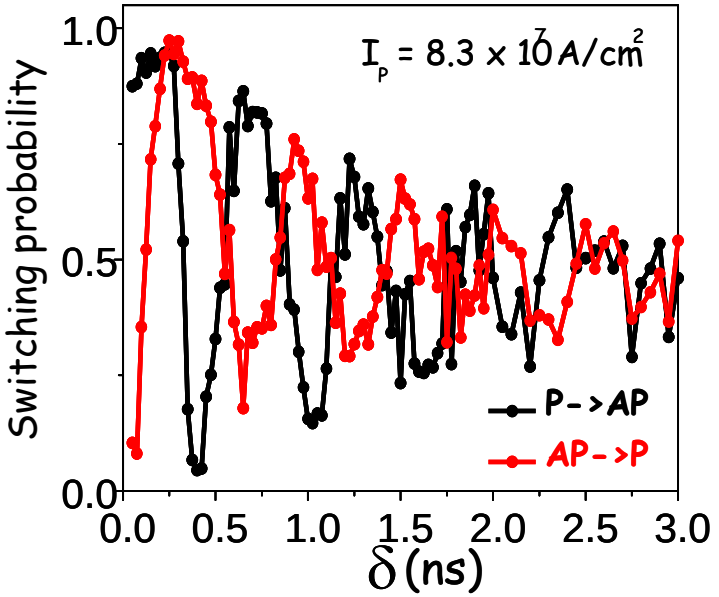
STT Precessional switching



Ellipse 80nm*270nm

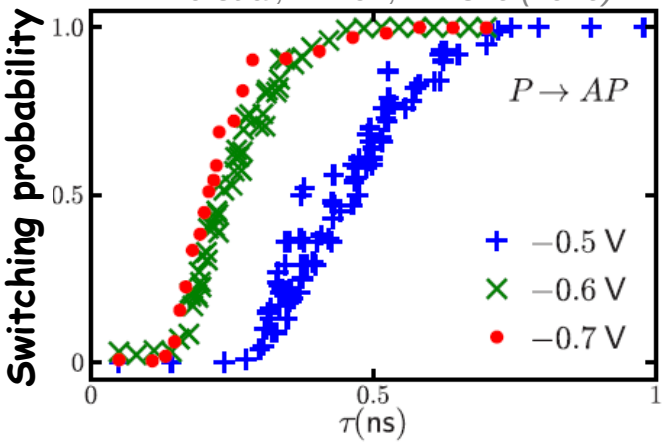
Role of perpendicular polarizer dominant:

C.Papusoi et al, Appl.Phys.Lett. (2009)



Role of planar analyzer dominant:

H.Liu et al, APL97, 242510 (2010)



Hybrid Magnetic/CMOS Integrated Electronics

ERD-ITRS (edition 2007):

"*Nanodevices that implement* ***both logic and memory in the same device*** *would* ***revolutionize*** *circuit and nanoarchitecture implementation*"

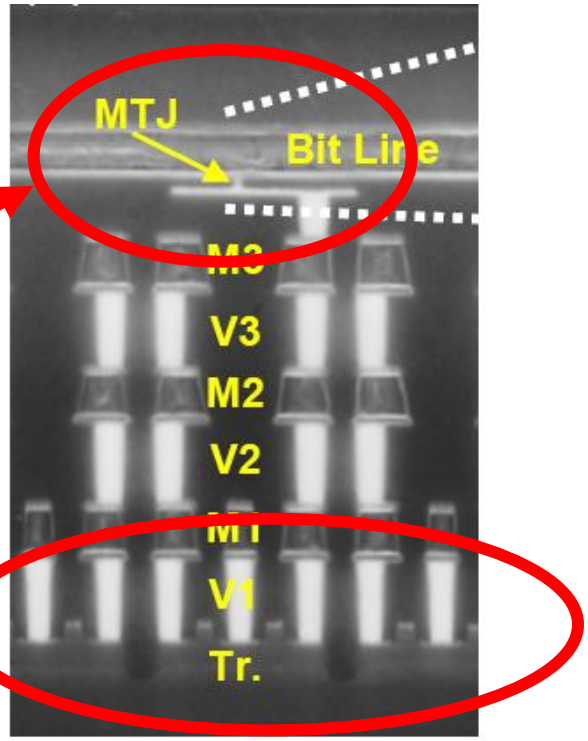
Possible with CMOS/MTJ integration thanks to the unique set of qualities of MTJs:

-Resistance compatible with CMOS (a few kΩ)
-Above IC technology possible
-Cyclability (>10^{16} cycles)
-Switching speed (~200ps-30ns)
-High density possible
-Thermal stability
-Radiation hardness

« Janus logic/memory components »

Non-volatile MTJ memory element

Simple MOSFET or Complex CMOS logic component



Great expectations in terms of energy consumption, speed of communication between memory and logic, footprint.

Problem of power consumption in CMOS-only microelectronics

DRAM, SRAM: volatile. Cannot be switched off without loosing information.

However, increasing leakage current with downsizing (thinner gate oxide)

6 System Driver Chapter 2010 Updates

Power consumption in CMOS electronic circuit per cm²

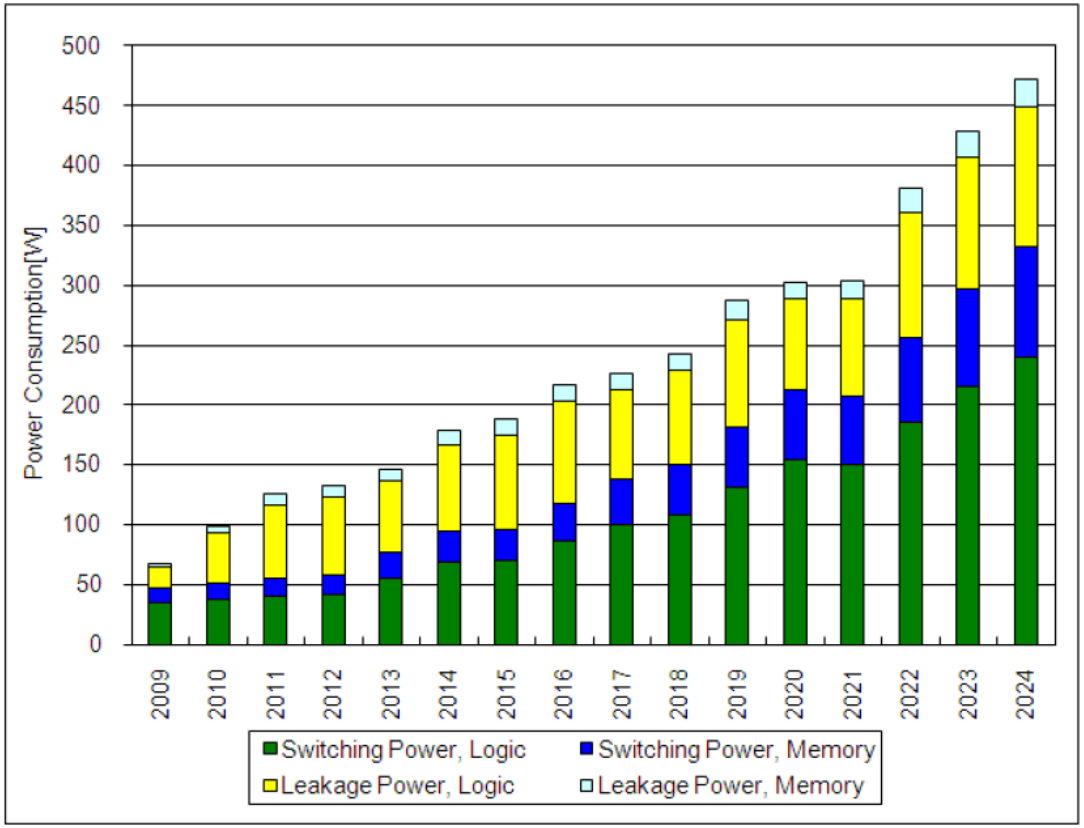


Figure SYSD11 SOC Consumer Stationary Power Consumption Trends—UPDATED

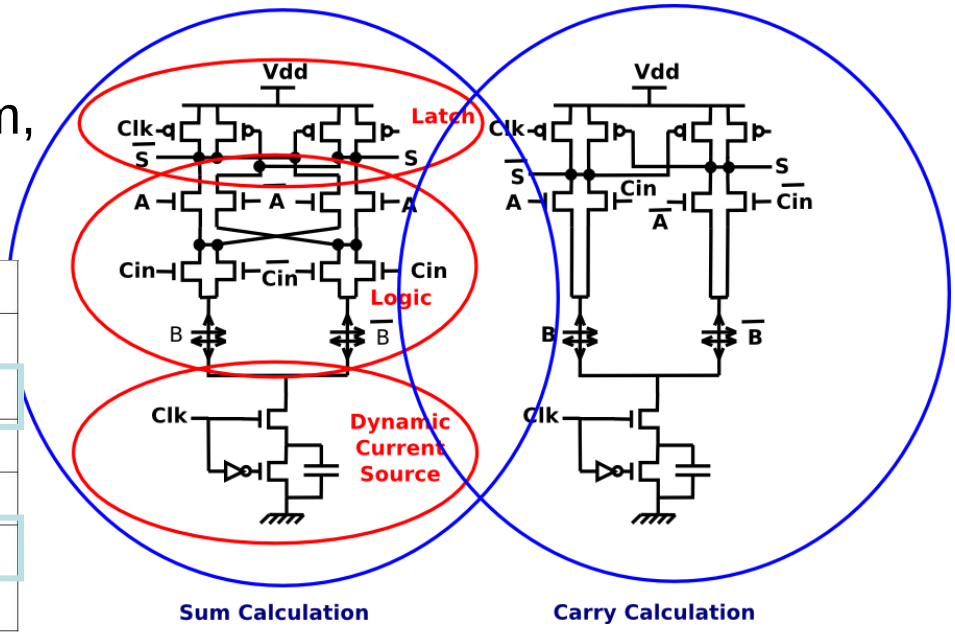
Major benefit in introducing non-volatility in CMOS components in terms of energy savings

Benefit from CMOS/magnetic hybrid architecture: Example of Magnetic non-volatile Full Adder

S.Matsunaga et al, *Applied Physics Express*, vol. 1, 2008.
Hitachi+Tohoku University

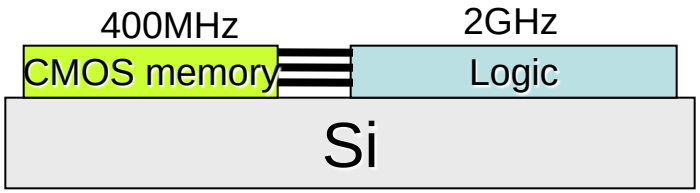
- Based on
  - Dynamic Current Mode Logic
    - Dynamic consumption reduction
    - Footprint reduction
  - MTJs
    - One input is made non-volatile (instant startup, security)
    - Drastic static consumption reduction
    - Footprint reduction
- Demonstrator : CMOS 0.18µm,
- MTJs size: 200X100nm²

	CMOS	Hybrid
Delay	224 ps	219 ps
Dynamic Power	71.1 µW	16.3 µW
Writing Time	2 ns/bit	10 (2) ns/bit
Writing Energy	4 pJ/bit	20.9 (6.8) pJ/bit
Standby Power	0,9 nW	0 nW
Surface	333 µm²	315 µm²

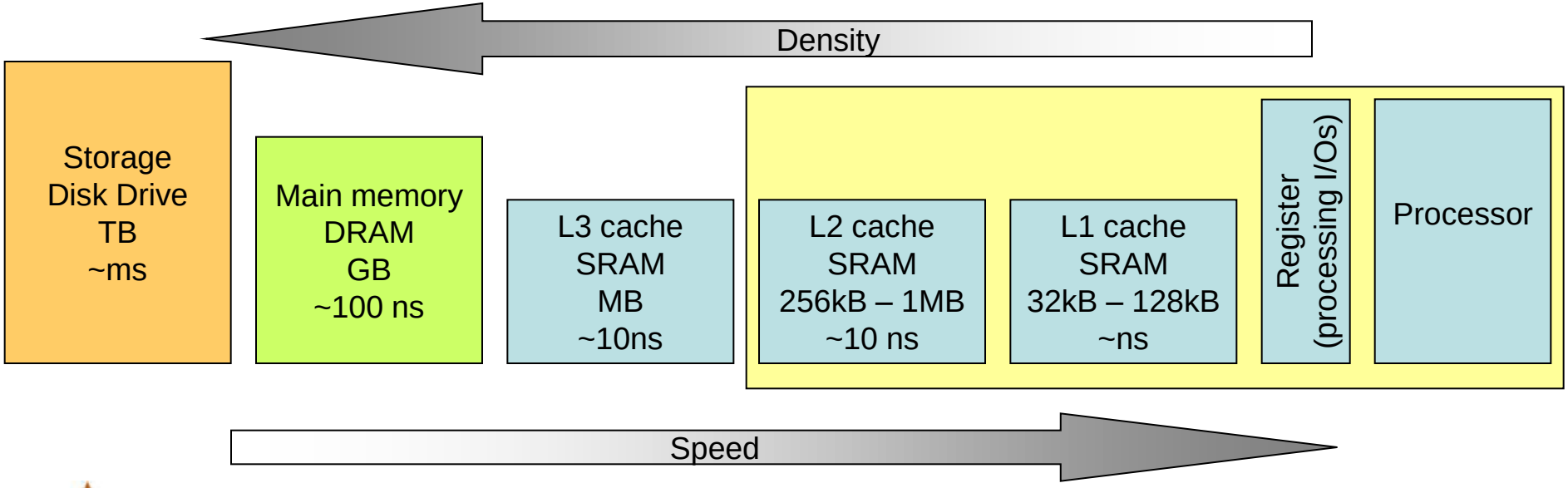


Communication logic ⇔ memory in CMOS-only microelectronics

- Large mismatch between processor speed and memory speed
  - Low Throughput (« VonNeumann bottleneck »)
  - Slow Access time (« Memory wall »)
  - → Processors keep waiting for data !



- Improved by using a memory hierarchy
  - → Cache memory (e.g. post'it)
  - → Complex architecture, high cost in bandwidth & energy

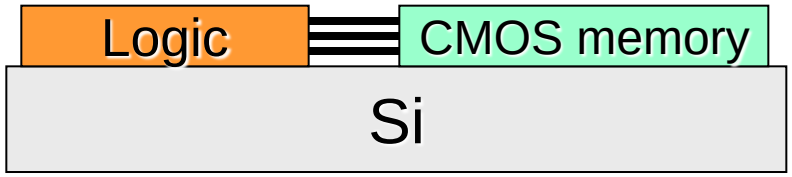


Towards a tighter integration between logic and memory

Same technology as for MRAM

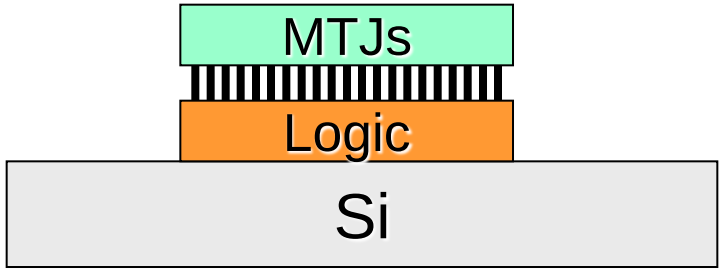
Benefit from "Above IC" technology

With CMOS technology only:



-Slow communication between logic and memory
-few long interconnections
-Large capacitive dynamic losses
-complexity of interconnecting paths
-large footprint on wafer

With hybrid CMOS/magnetic:
"Logic-in memory"



-Non-volatility in logic
-Large static and dynamic energy saving ("normally-off electronics")
-Fast communication between logic and memory
-Numerous short vias
-Simpler interconnection paths
-Smaller footprint on wafer

New paradigm for architecture of complex electronic circuit (microprocessors...)

Which memory technology could be used for logic-in-memory architecture ?

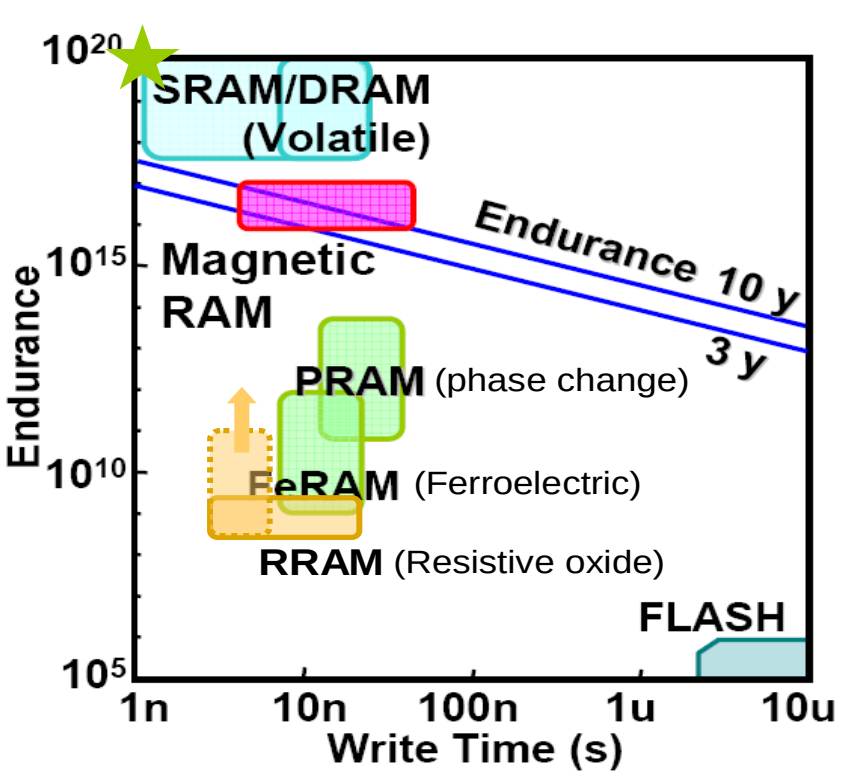
For logic in memory applications, NVM are required with the following characteristics:

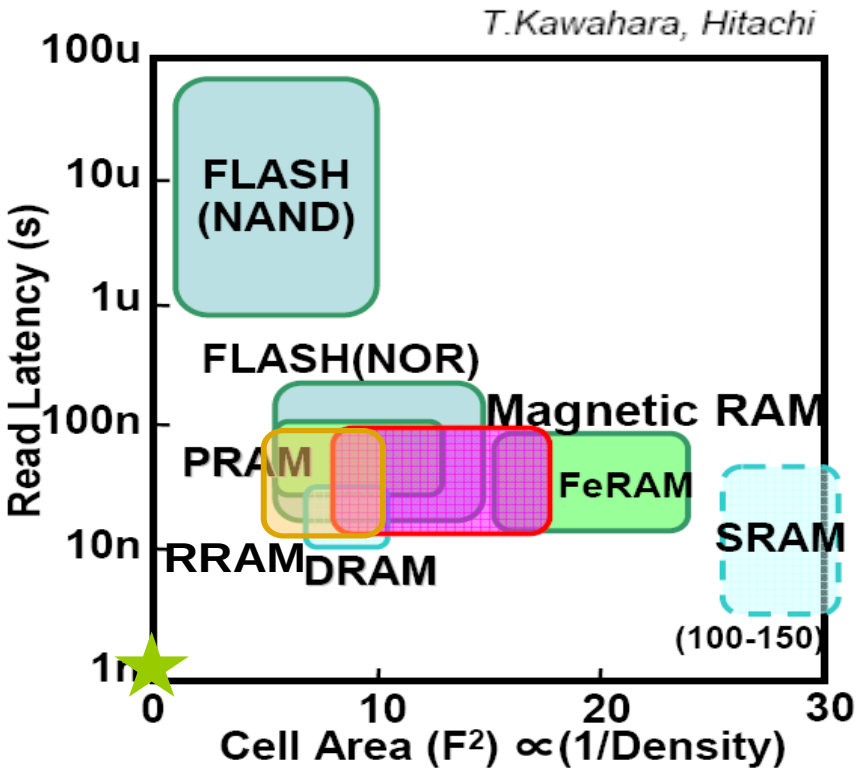
-Can be grown in back-end process (above CMOS)

-Small, dense

-Fast (short write and read cycles, a few ns)

-Infinite endurance (10^{16}cycles)





Although not the best in each category, MRAM is the only memory which scores everywhere + moderate power (no high voltage), radiation-hard, easy to embed

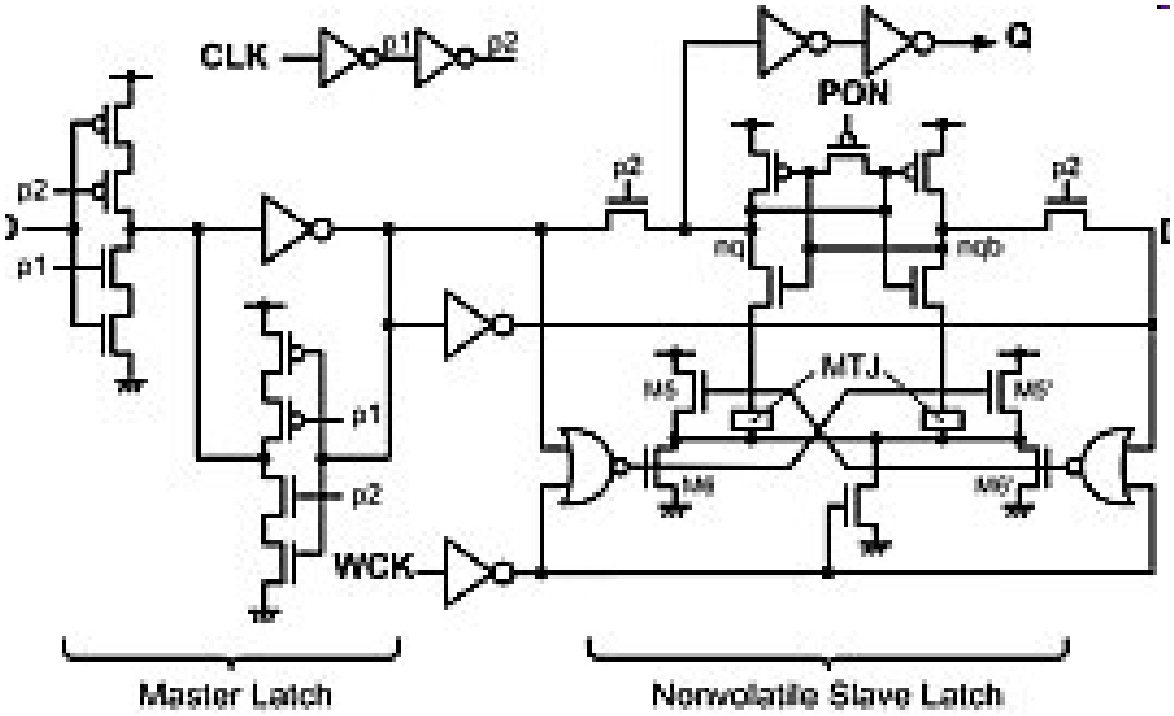
Magnetic non-volatile flip-flop

NEC Empowered by Innovation

Home

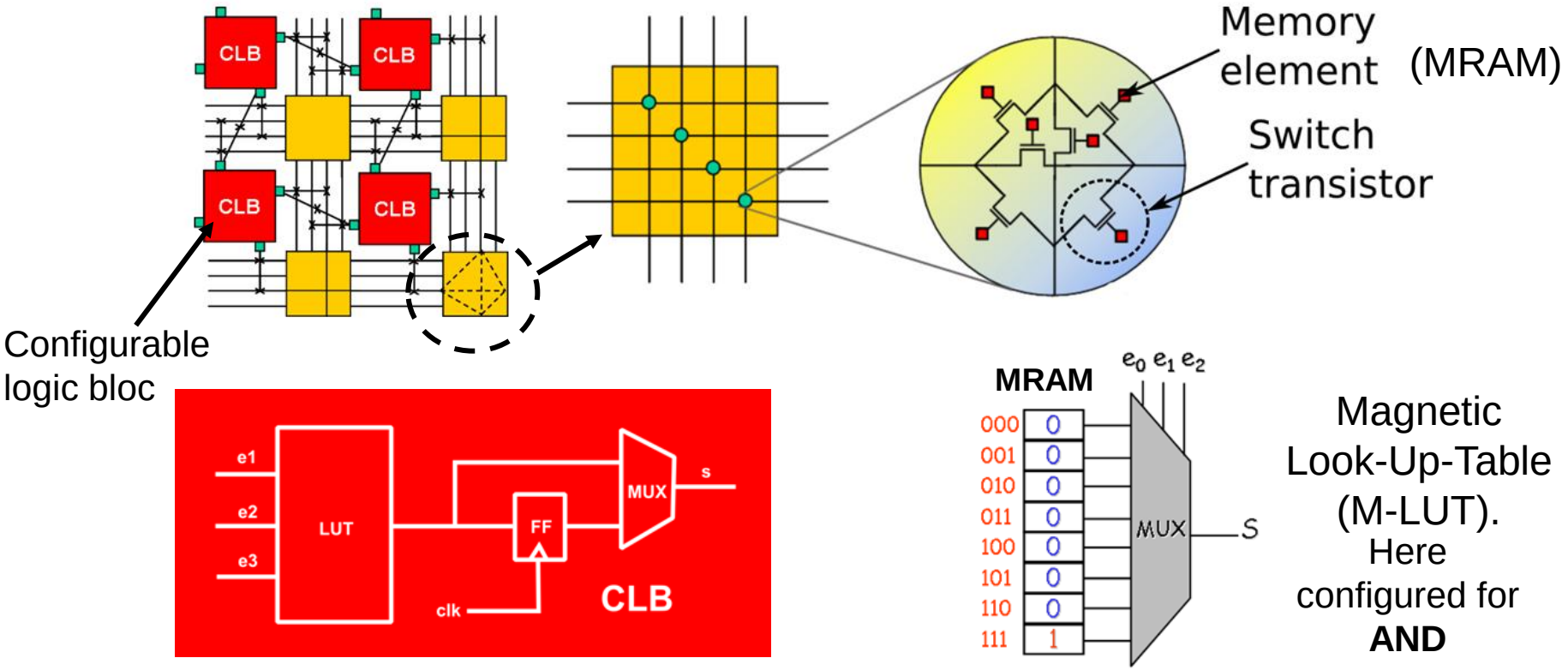
Home > News Room > NEC develops a nonvolatile magnetic flip flop that enables standby-power-free SoCs

NEC develops a nonvolatile magnetic flip flop that enables standby-power-free SoCs



Reconfigurable hybrid CMOS/MTJ logic circuits (M-FPGA)

Reconfigurable: Same hardware can be reconfigured to achieve different functionalities.
Example: Magnetic Field Programmable Gate Arrays (M-FPGA)

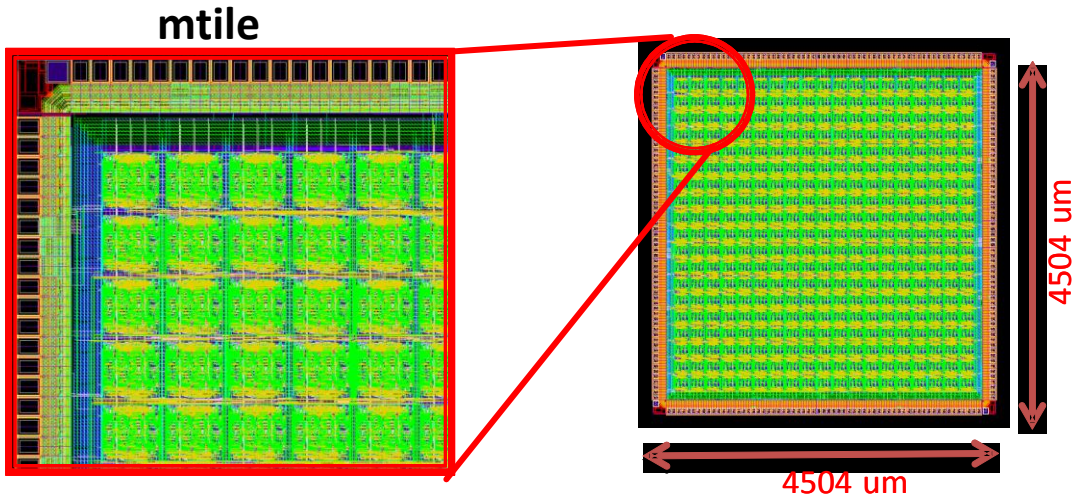


Magnetic Look-Up-Table (M-LUT). Here configured for **AND**

Advantages of hybrid CMOS/MTJ technology: Instant-on start, ultrafast and unlimited reconfiguration, shadowed reconfiguration, reduced power consumption, reduced footprint on wafer.

REPROGRAMABLE MAGNETIC FPGA

# LUT 4	1444
# TILES	361 (19x19)
# Sequential elements	1444
# of MTJs	187 720
# of Transistors	9. 10^6
Silicon Area	21mm^2
MRAM Reconfiguration Tile Energy	9 nJ
MRAM Restoration Tile Energy	25,5 pJ
Clock Frequency	100 MHz
Full configuration time	72us + 93K Clock cycles
Tile reconfiguration	200ns + 260 Clock cycles
# Input/Output	76 Input / 76 Output

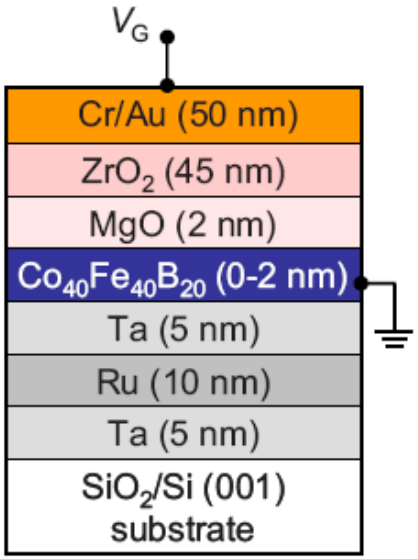


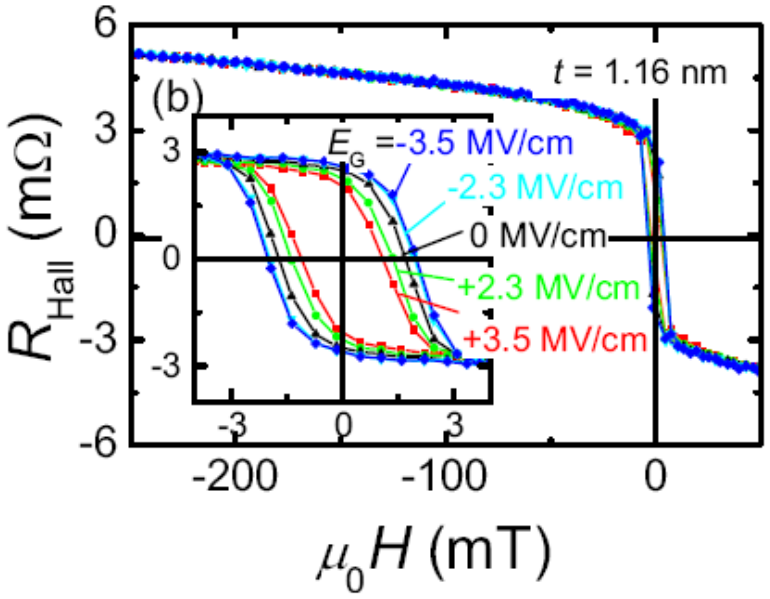
AND FURTHER?

- **Electric field controlled of magnetic properties in MRAM.**

Supposed to reduce power consumption in comparison to current controlled MRAM

Electric-field effects on thickness dependent magnetic anisotropy
of sputtered MgO/Co40Fe40B20/Ta structures,
M. Endo, S. Kanai, S. Ikeda, F. Matsukura, H. Ohno, Appl.Phys.Lett.96, 212503 (2010)





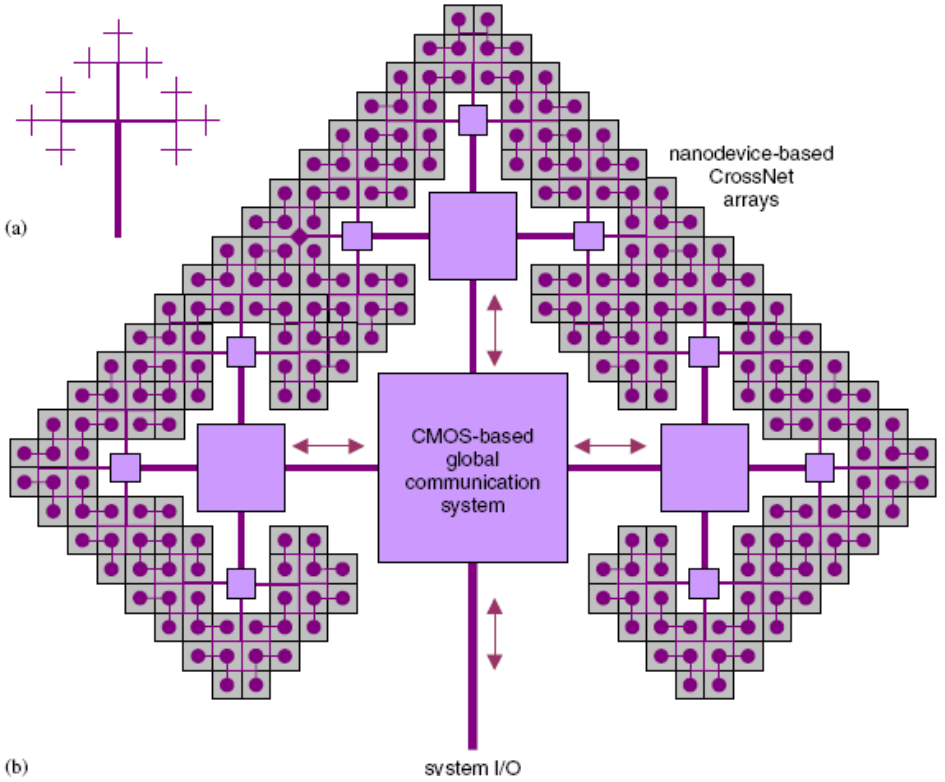
Variation of coercivity with electrical field; reorientation from out-of-plane to in-plane magnetization possible with E.

Benefit on power consumption in comparison to Spin Transfer Torque switching current control) has to be evaluated considering the whole architecture. Here energy $CV^2/2$ to pay.

AND FURTHER?

- **Neuromorphic architecture** (next talk G.Bourianoff).

Totally different architecture mimicking the brain working principle: neurons interconnected by synapses (reprogrammable interconnections with resistance varying according to the history of the current flowing through them) (memristor). Analogic working principle.



Redox RAM may be better adapted for this type of application (as synapses) than MRAM because of their larger ΔR variation (~10 vs ~2) and easier to implement memristor capabilities.
MRAM are best for binary electronics.

Turel, Likharev, Int.J.Circ.th.Appl, 32, 277 (2004)

AND FURTHER?

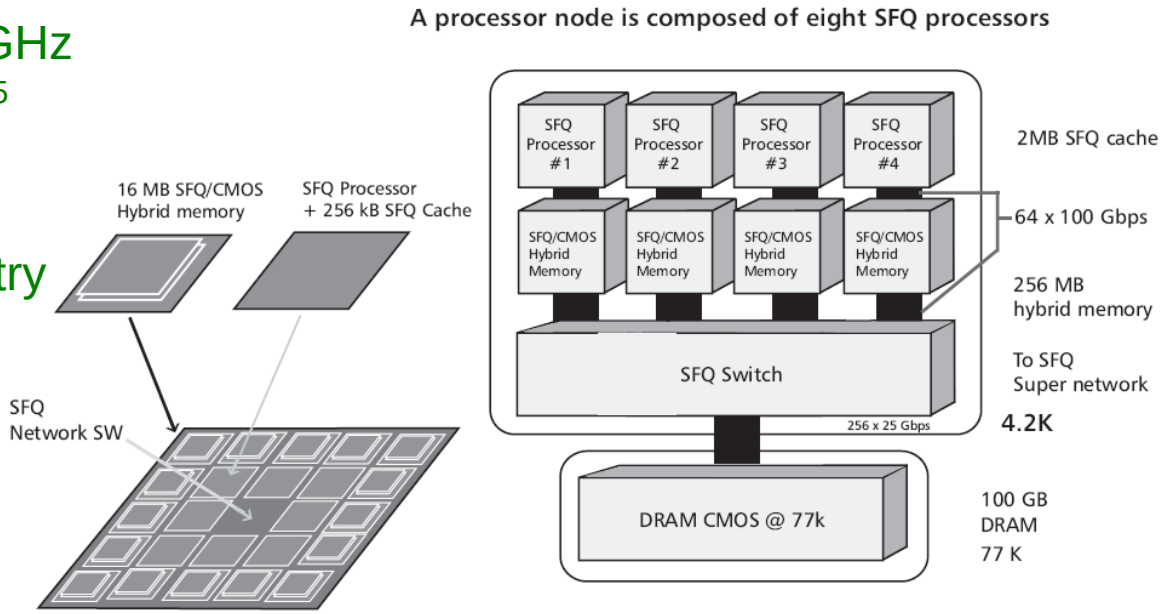
•**<u>Superconducting circuits based on Josephson junctions (RSFQ= Rapid Single Flux Quantum logic)</u>**: May be quite worth for large scale computers or server farms.

•The energy required to cool would be now much lower than the gain in dissipated energy.

•Run at frequency of 100-500GHz

•Power consumption about 10^5 times lower than CMOS semiconductors circuits

•Compatible with CMOS circuitry



SFQ Multi Chip Module

Die size: 10 mm x 10 mm
Module size: 80 mm x 80 mm
Bandwidth between chips: 64-b x 100Gbps

Process	160 KA/cm2 0.25 um Nb process
Processor performance	100 Gflops (Clock frequency: 100 GHz)
Cache size	L1: 256kB, L2: 32 MB (per processor)
Processor/memory bandwidth	800 GB/s (per processor)
Processor node performance	800 Gflops
Power at 4.2k	7.3 W

AND FURTHER?

Quantum computing?

Complex at all levels: Qubits with sufficiently long decorrelation time, algorithms to perform operations, working temperature….

Only very few algorithms have been proposed taking advantage of manipulation of quantum states:
-Peter Shor 1994: factorization,
-Grover 1996: searching a particular string within an unsorted database of N string (time proportional to $N^{1/2}$)
-Cryptography (security provided by manipulation of entangled states).

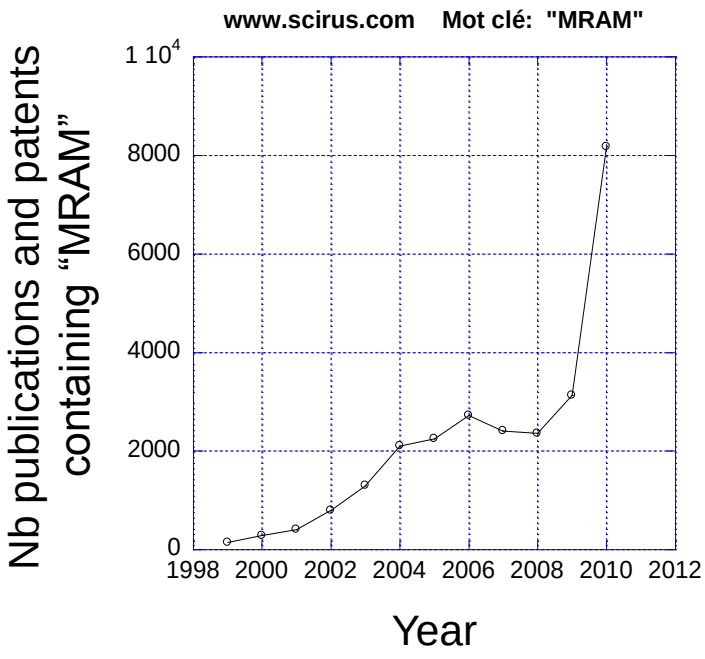
May be useful for very specific applications, particularly secured communications but not for general purpose computing in the next 20years.

CONCLUSION 1

•Raising interest for MRAM in microelectronics industry

•Thermal Assistance (T_{write}~250° C) in MRAM allows to extend the downsize scalability of MRAM written both by field or by STT.

•CMOS/magnetic integration more and more reliable (Everspin products since 2006, magnetic back-end lines at Tower, TSMC, Samsung, Hynix …)



•MRAM physical scalability down to sub-20nm demonstrated with very encouraging performances for cache applications (speed <10ns, density ~8F², cyclability >10^{16},..)

•Magnetic materials and phenomena may look complicate but already a long industrial history (hard disk drives).

CONCLUSION 2

•Boolean logic has still way to go. Introducing non-volatility in logic thanks to embedded non-volatile memory holds great potential in terms of energy savings, speed of applications and security of data (logic-in-memory, normally-off-electronics, security applications)…

•Neuromorphic architectures look very promising (Analogic approach).

•Quantum computing may be useful for very specific applications (secured transmission of data) but no clear route towards general purpose computing.

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RAMAC (ANR 2007)

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NANOINNOV SPIN (2009)

HYMAGINE (ERC2009)

Back slides

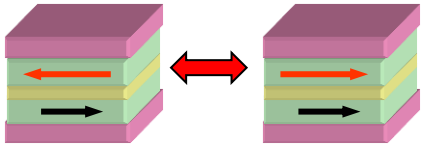
ITRS ERD Roadmap 2010

Assessment of the Potential & Maturity of Selected Emerging Research Memory Technologies
Workshop & ERD/ERM Working Group Meeting (April 6-7, 2010)

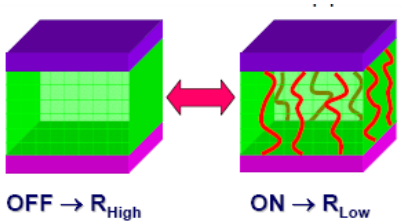
Jim Hutchby & Mike Garner
July 23, 2010

The outcome of this study is the ERD/ERM working groups identified Spin Transfer Torque MRAM and Redox RRAM as emerging memory technologies recommended for accelerated research and development leading to scaling and commercialization of Non-volatile RAM to and beyond the 16nm generation.

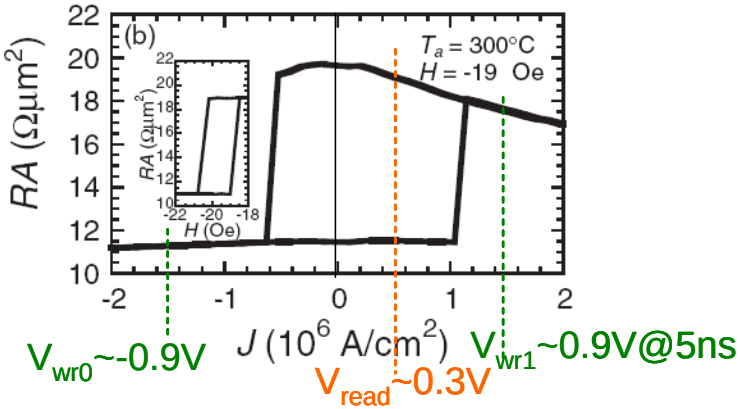
STT-MRAM

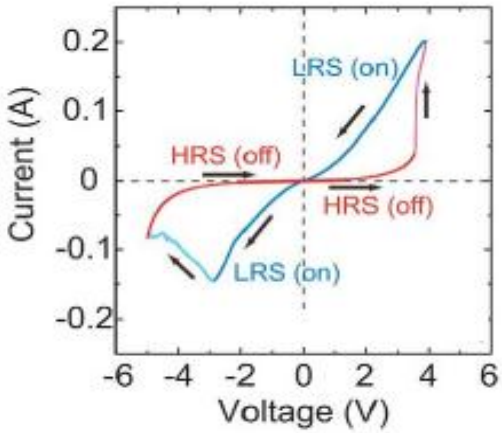


ReRAM



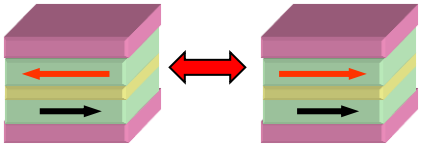
GeAg
Pt/TaOx/Pt

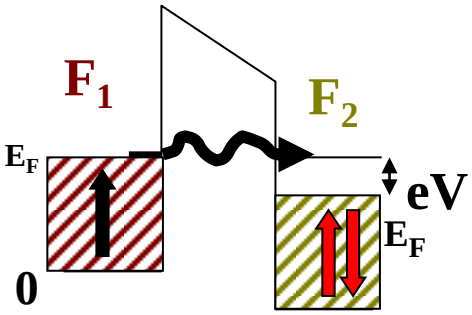




COMPARISON MRAM / ReRAM

STT-MRAM



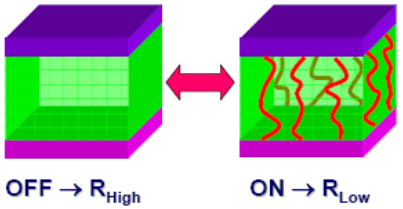


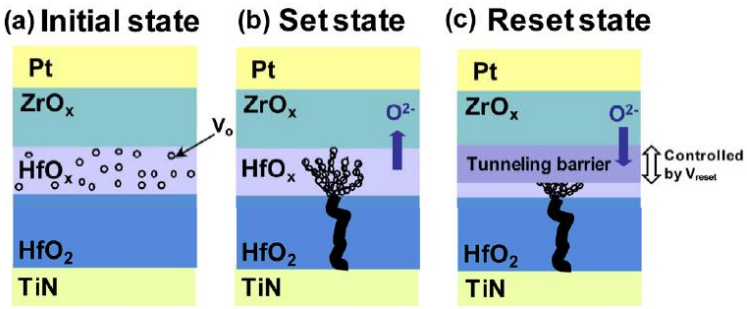
$$R = R_{\min} + \Delta R \frac{(1-\cos\theta)}{2}$$

Spin-dependent quantum mechanical tunneling of electrons (as polarizer/analyzer in optics).
Switching of magnetization described by LLG equation:

$$\frac{dM}{dt} = -\gamma M \times \left(H_{eff} + bI.M_p\right) + \gamma aI.M \times \left(M \times M_p\right) + \alpha M \times \frac{dM}{dt}$$

ReRAM





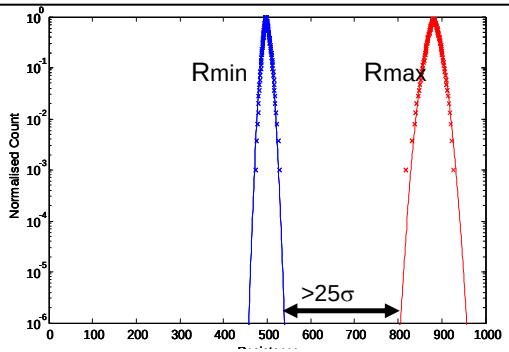
Statistical phenomenon associated with migration of vacancies or metallic ions

J.Lee et al, Gwanju IST, Korea (IEDM2010)

R distributions:

1Mbit chip TA-MRAM

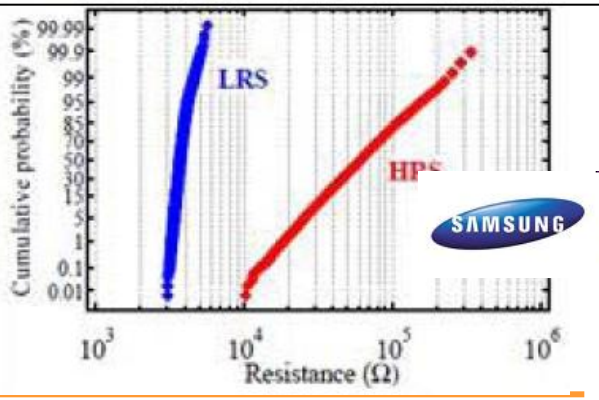
CROCUS Technology
Blossoming future



0 0.5 1

Resistance (kΩ)

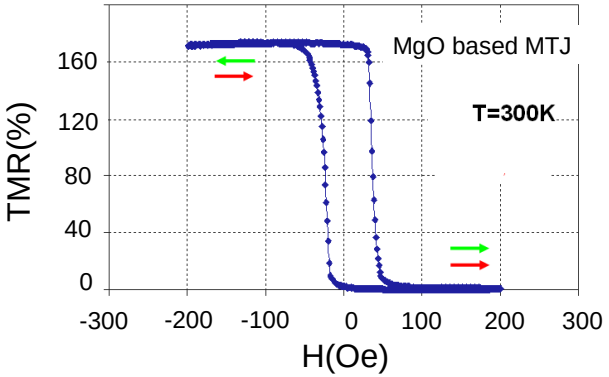
8kbit ReRAM
(K.Kit, SAIT, Samsung IEDM 2010)



COMPARISON MRAM / ReRAM

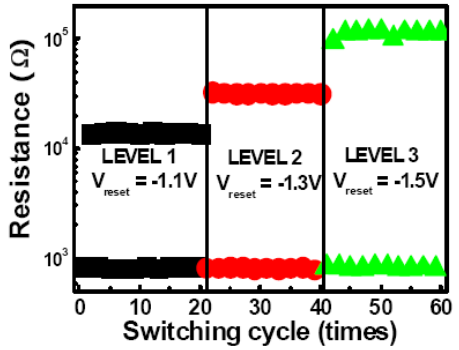
Multilevel capability:

STT-MRAM



- Binary resistance levels
- Multilevel and memristor possible but with much less ΔR amplitude than with ReRAM. Not so easy to implement (R(θ), DW or stacking of several MTJ)

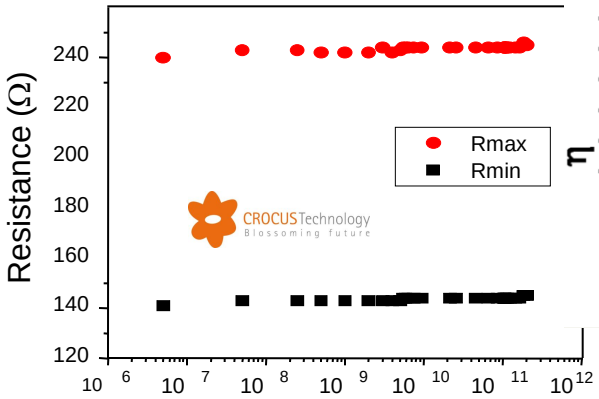
ReRAM

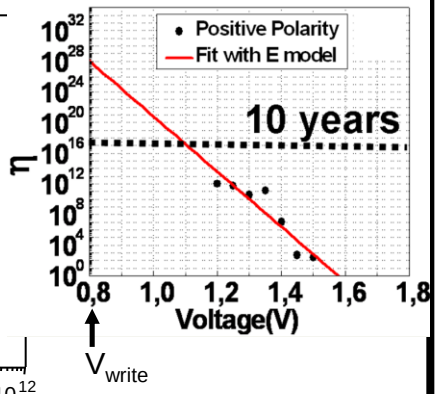


Multilevel capability
Memristor functionality with large ΔR amplitude

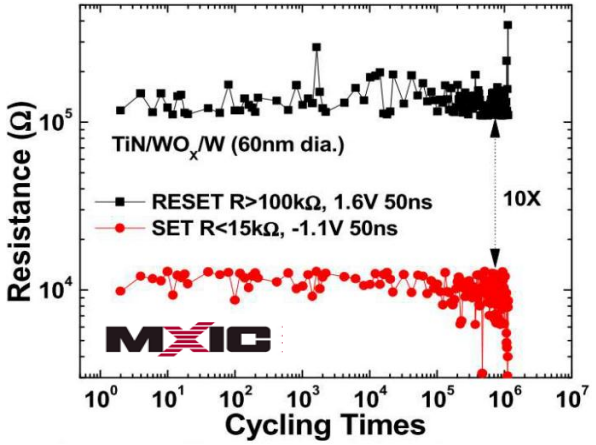
J.Lee et al, Gwanju IST, Korea (IEDM2010)

Cyclability:





>10^{16} cycles



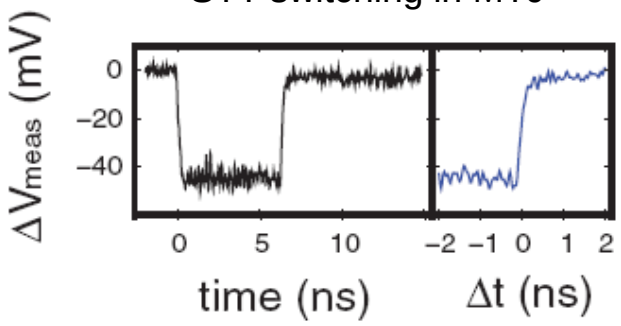
W.C.Chien et al, Macronix, Hsinchu, Taiwan, (IEDM2010)

COMPARISON MRAM / ReRAM

Speed:

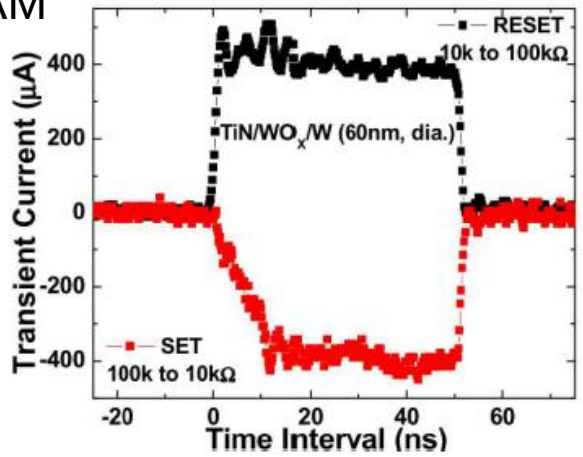
STT-MRAM

STT switching in MTJ



Y.T.Cui et la, PRL104, 097201(2010)

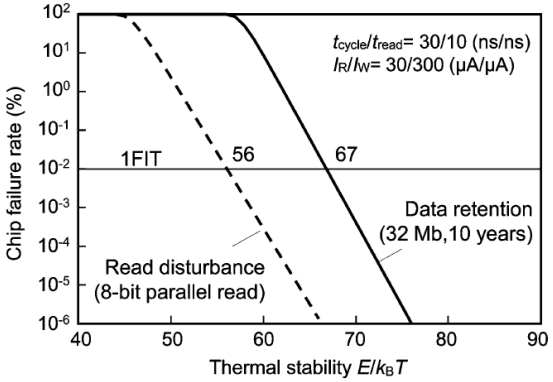
ReRAM



W.C.Chien et al, Macronix, Hsinchu, Taiwan, (IEDM2010)

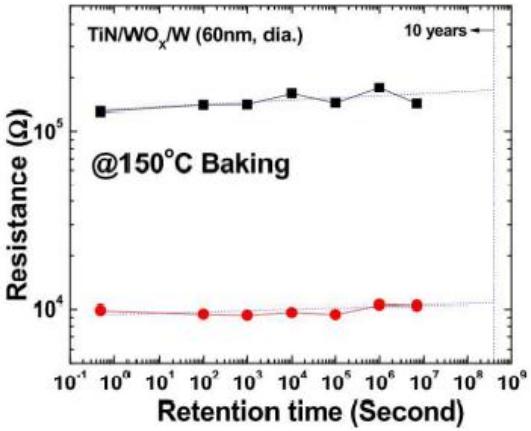
Retention:

$$F_{chip} = 1 - \exp\left[-m\frac{t}{\tau_0}\exp\left(-\frac{E}{k_B T}\left(1-\frac{I_{cell}}{I_{WR}}\right)\right)\right]$$



$E/K_BT>67$

OK with perpendicular MTJ
OK with TAS



W.C.Chien et al, Macronix, Hsinchu, Taiwan, (IEDM2010)

Takemura et al, IEEE Journ of Solid State Circuits, 45, 869 (2010)

COMPARISON MRAM / ReRAM

Possibility of crossbar architecture:

MRAM

(12) **United States Patent**
Tran

(10) **Patent No.: US 6,778,421 B2**
(45) **Date of Patent: Aug. 17, 2004**

(54) **MEMORY DEVICE ARRAY HAVING A PAIR OF MAGNETIC BITS SHARING A COMMON CONDUCTOR LINE**

(75) Inventor: **Lung T. Tran**, Saratoga, CA (US)

(73) Assignee: **Hewlett-Packard Development Company, LP.**, Houston, TX (US)

6,185,122	B1 *	2/2001	Johnson et al.	365/103
6,297,987	B1	10/2001	Johnson et al.	
6,341,084	B2 *	1/2002	Numata et al.	365/158
6,351,406	B1 *	2/2002	Johnson et al.	365/103
6,483,736	B2 *	11/2002	Johnson et al.	365/130
6,577,527	B2 *	6/2003	Freitag et al.	365/158
6,577,529	B1 *	6/2003	Sharma et al.	365/158

* cited by examiner

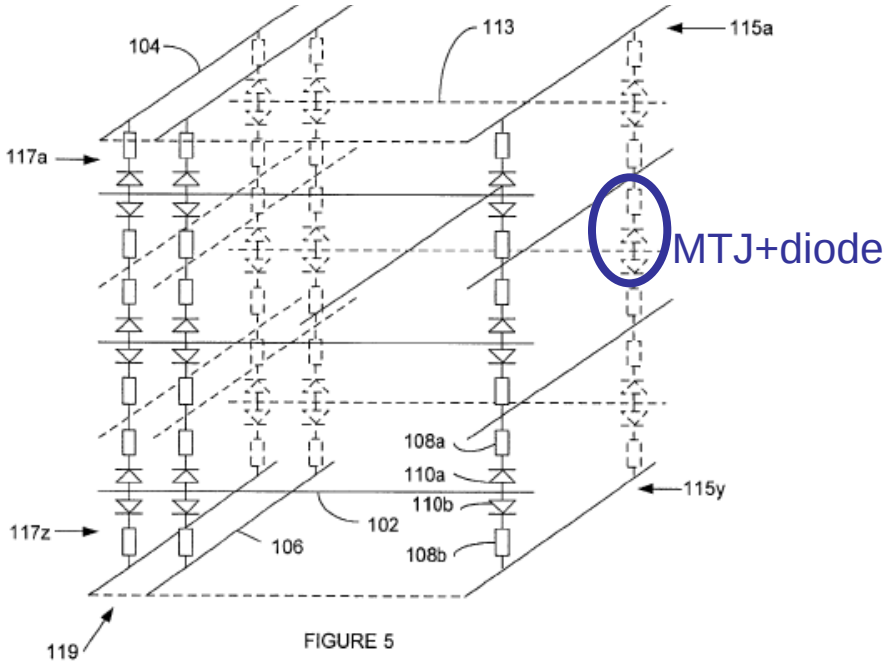
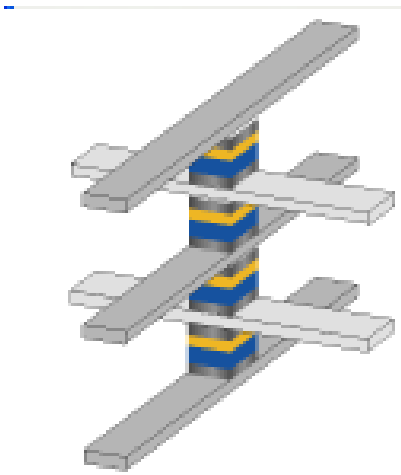


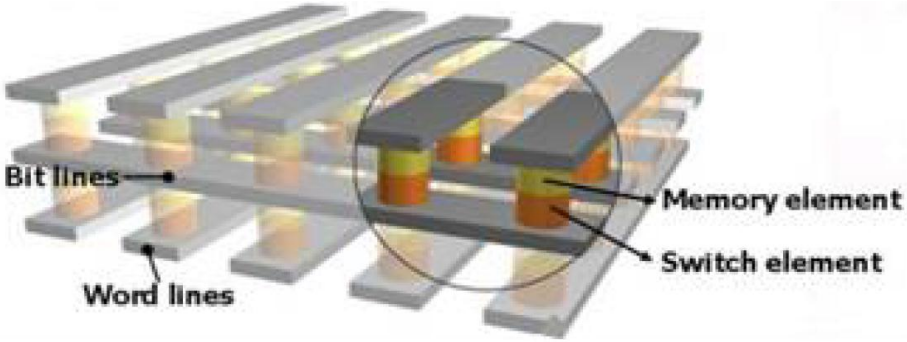
FIGURE 5

Difficulty is the in-stack diode

ReRAM



http://www.unitysemi.com/



M.-J. Lee *et al.*, Samsung, IEDM 2007

Summary of differences
MRAM / ReRAM

MRAM	ReRAM
"Unlimited" cyclability (>10^{16} cycles)	**Cyclability ~ 10^6 cycles, similar to PCRAM**
Narrow distribution of R_{min} / R_{max}	**Larger distribution of R_{min} / R_{max}**
1Mbit: 5kΩ±0.3kΩ 12kΩ±0.8kΩ	**6Kbit: 3-6kΩ / 10kΩ - 300kΩ**
Bilevel resistance **Multilevel possible but not straighforward**	**"Natural" continuous change of R** **Multilevel capability easier to implement**
Moderate ΔR : R_{max}/R_{min} ~2-3	**Large ΔR : R_{max}/R_{min} ~5 - 50**

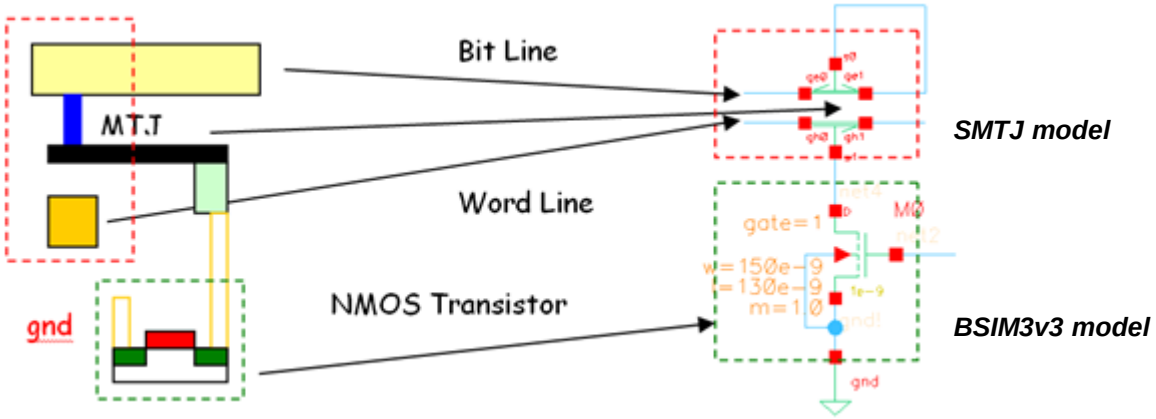
Personal conclusion:

More adapted for <u>binary electronics</u> "0" and "1"	**More adapted for <u>Memristor applications</u> ⇒ Neuromorphic architectures**

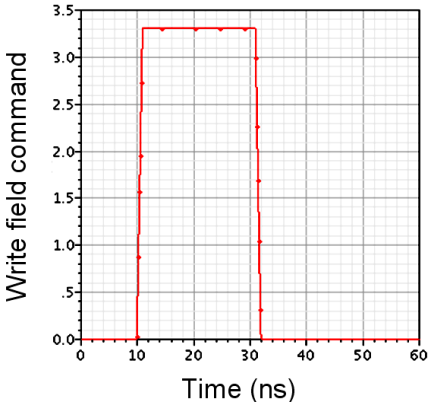
MTJ ELECTRICAL COMPACT MODEL

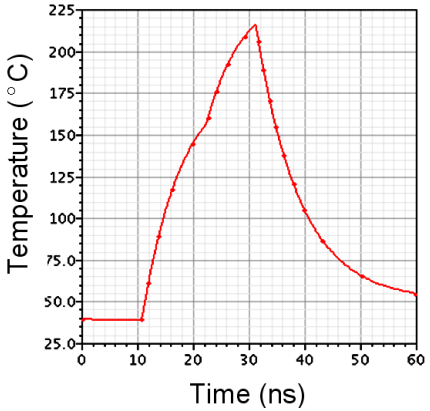
High-Speed compact model → Electrical behavior of MTJ written by field, STT and with/without thermal assistance.

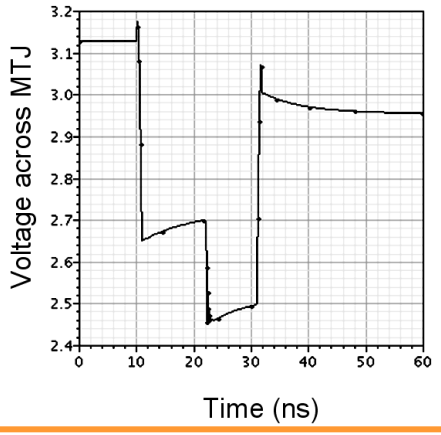
SPECTRE (5.0) compatible (CADENCE platform analog solver).

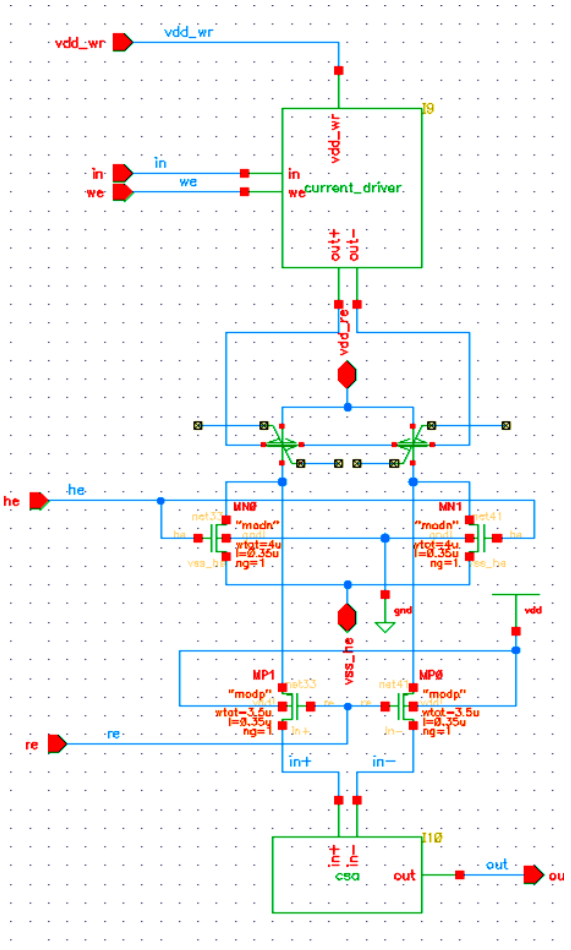


Simulation of a TAS-MRAM



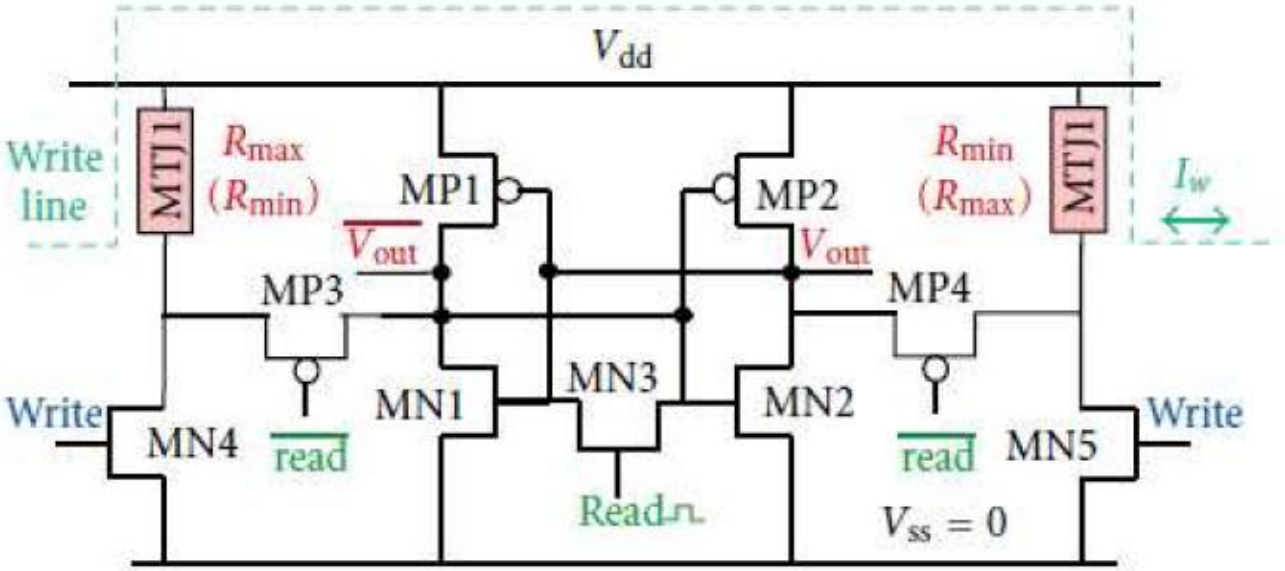






Non-volatile SRAM

R-SRAM ©



Magnetic Flip-flop