Beyond CMOS …
toward new integrated systems?

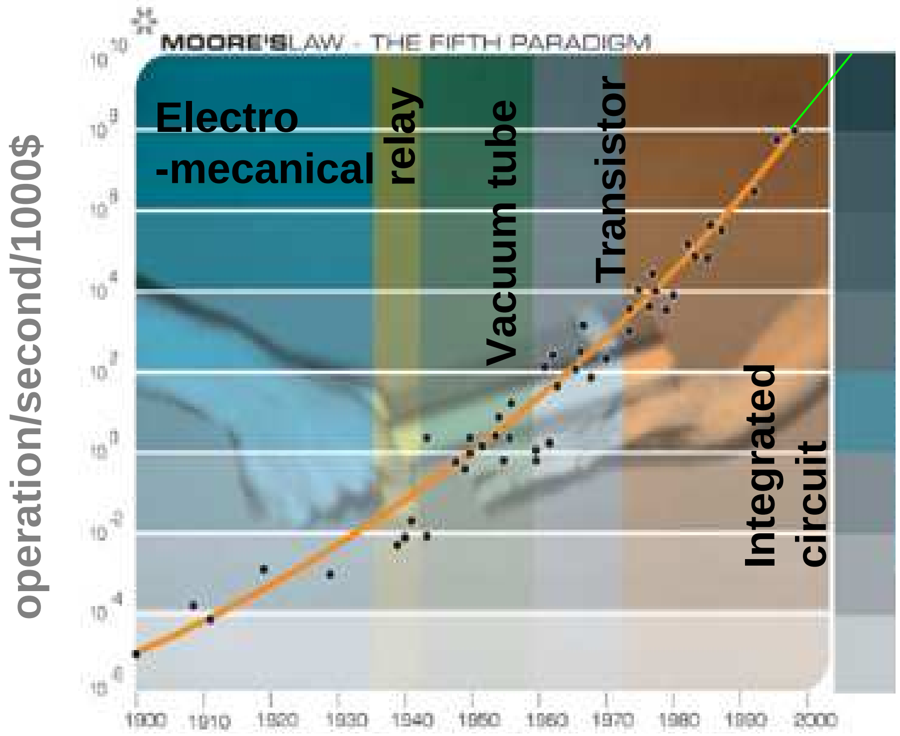
Thomas Ernst

CEA-LETI

Outline

- Introduction
- Why new devices ?
- Need of killer applications
- An example of new application

An history of data computing …



- **increase of operation/second for a given cost**
- **a new device will to answer this question ?**
- **in log time scale, the transition looks disruptive … but …**

From kurzweil

CMOS maturation example

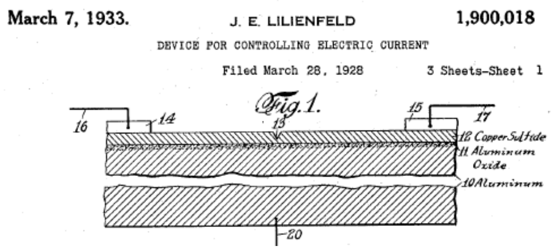
date	Event
1928	Concept invention *Lilienfeld*
1948	1st experimental validation *Shockley-Pearson*
1955	TMOSFET à inversion *Ross et al.*
	Si/SiO_2 *Atalla et al.*
1960	Big switch between Bipolar => MOS (and BICMOS)
1969 -1972	
1980	BOOM CMOS-BiCMOS Information technologies
2007	Si/HfO_2
	III-V, Graphene, nanotubes … ?

40 years

10µm

1µm

10nm



1- CONCEPT

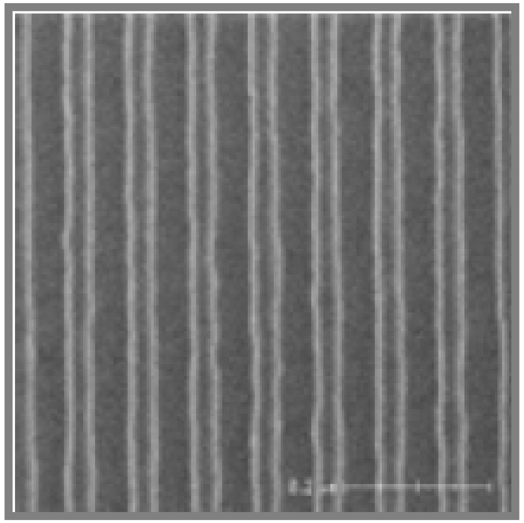
2- VIABLE TECHNOLOGY

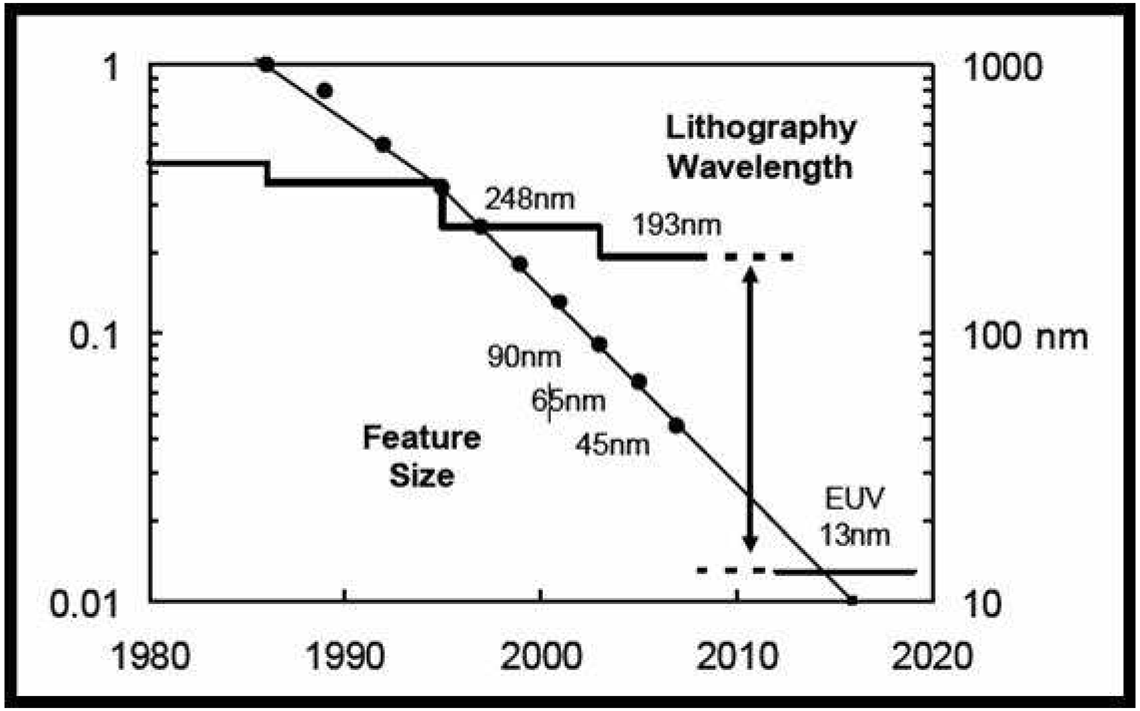
3- MARKET

Scaling limitation today : Lithography

Rayleigh equation

$$d = k_1 \left(\frac{\lambda}{N_A} \right)$$





S. Sivakumar et al., IEDM 2006

Whatever the material or the type of device, lithography should be mature enough…

EUV - ASML production tool

NXE:3300B 1st shipment: H1 2012

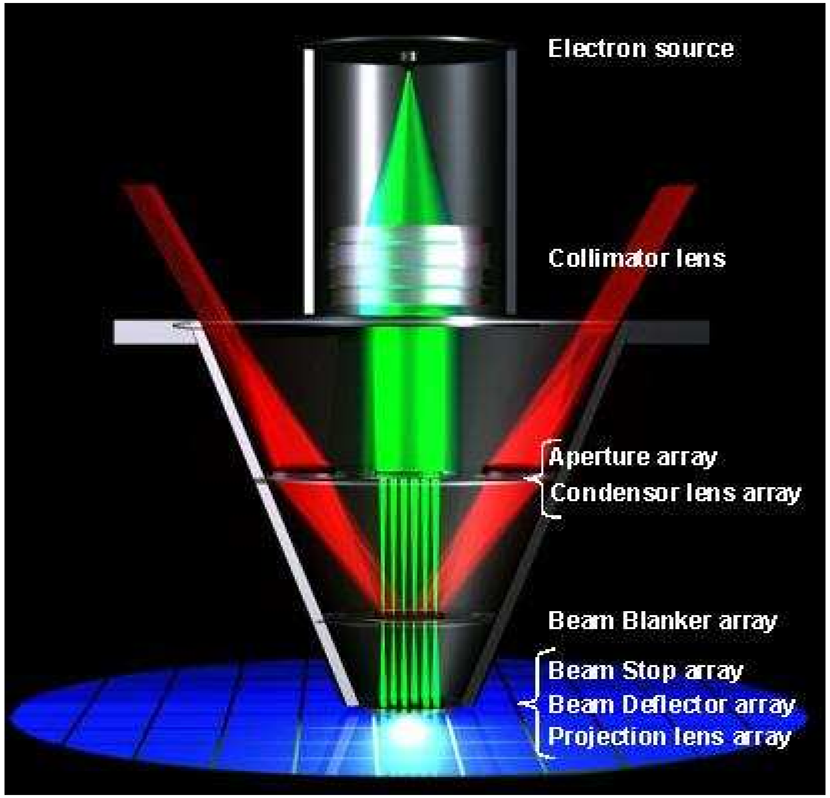
2nd generation of NXE platform, NA raised to 0.33NA

Specifications

- Imaging
  - NA = 0.33
  - σ=0.2-0.9 / OAI
  - Resolution 22 nm
    18/16nm with OAI
- Overlay
  - DCO 3.0nm
  - MMO 5.0nm
- Productivity
  - 125 wph
    15 mJ/cm² resist

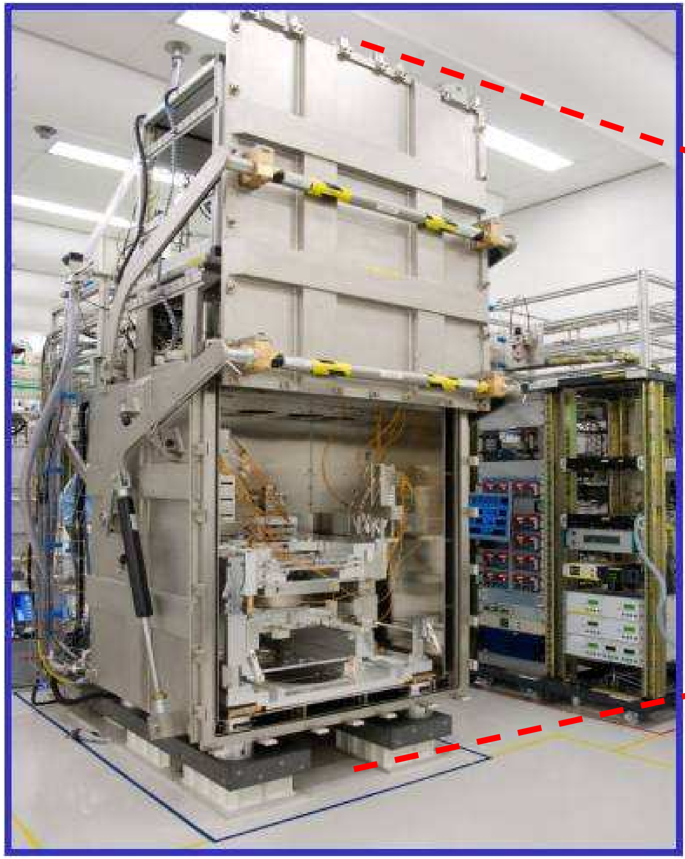
Challenge: Availability of the source?

MAPPER builds a system with 13,000 parallel electron beams for 10 wph



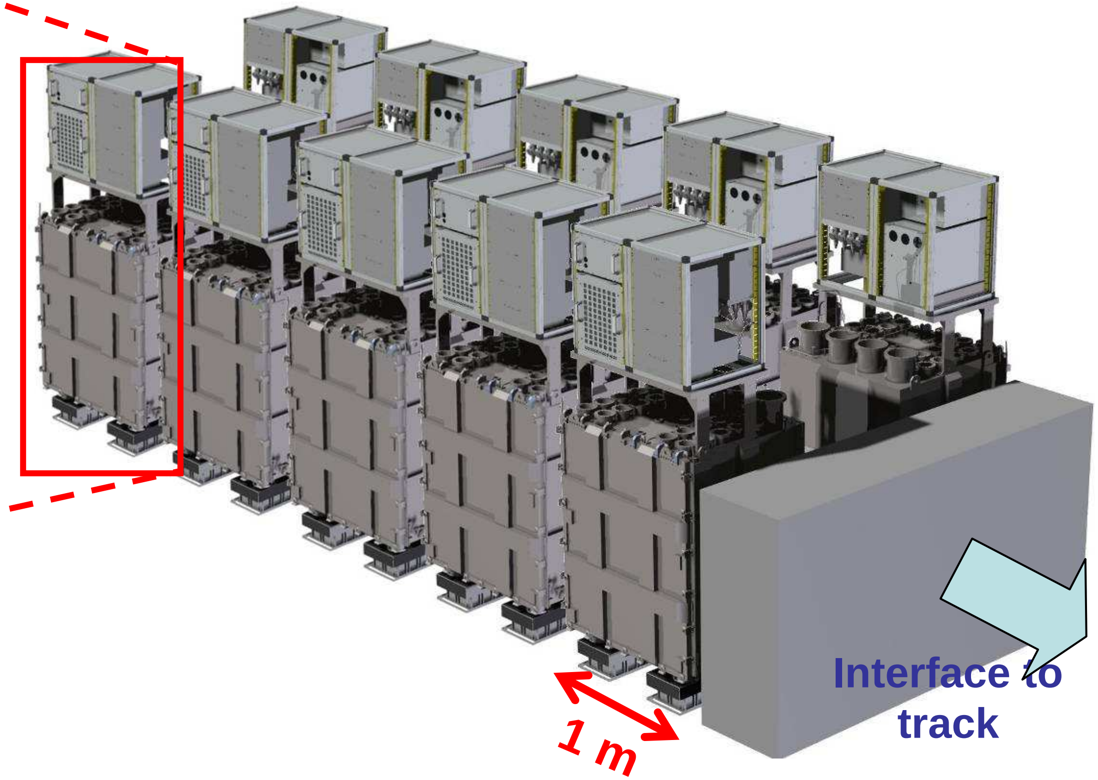
	HVM
#beams and data channels	13,000
Spot size:	25 nm
Beam current:	13 nA
Data rate/channel	70 MHz
Acceleration voltage	5 kV
Nominal dose	30 µC/cm^2
Throughput @ nominal dose	10 wph
Pixel size @ nominal dose	3.5nm
Wafer movement	Scanning

Toward a cluster tool



MAPPER single column tool.
Upgrade to 13,000 beam for 10WPH

Mapper tool cluster for 100 wph



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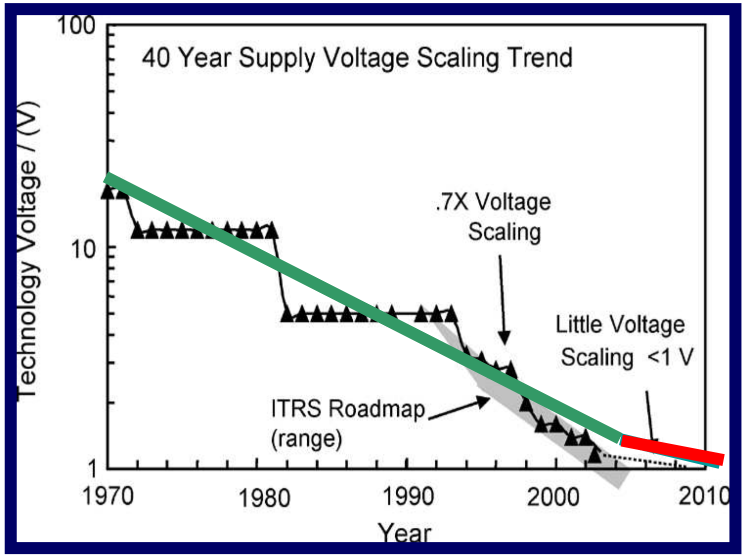
Then, comes the power dissipation limitation



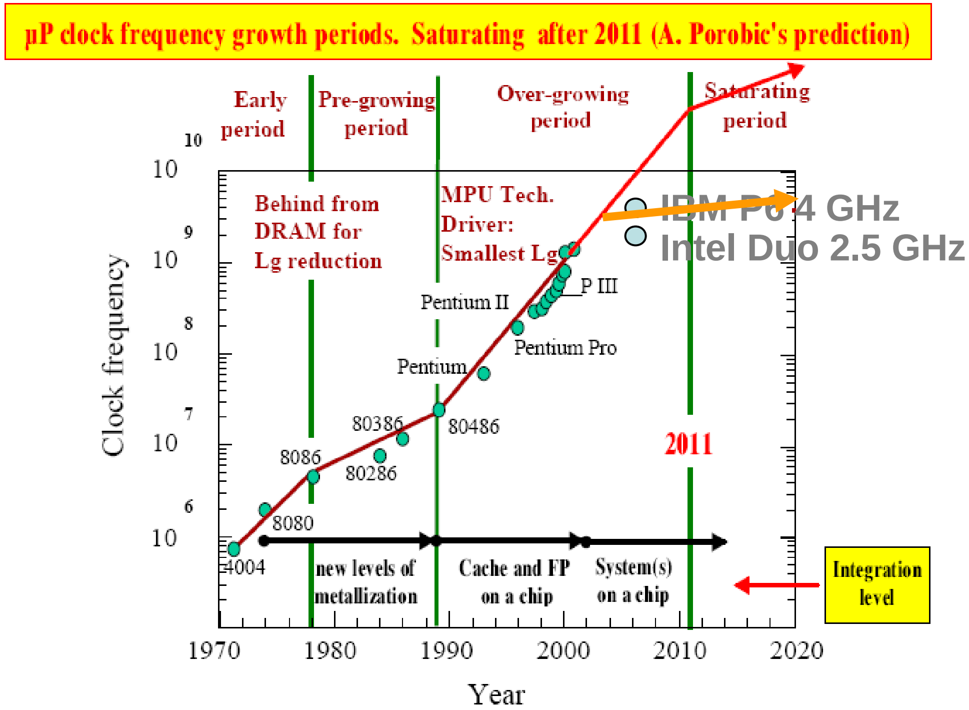
A. Groove, International Electron Devices Meeting 2007

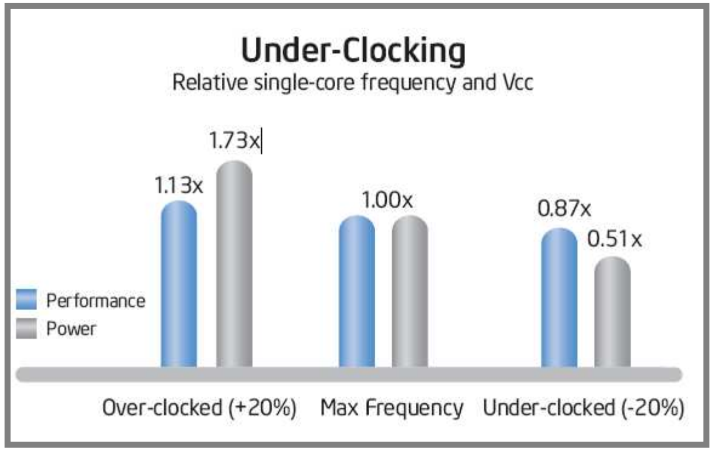
$$P = f\,C\,V_{dd}^{2} + I_{OFF} \cdot V_{dd}$$

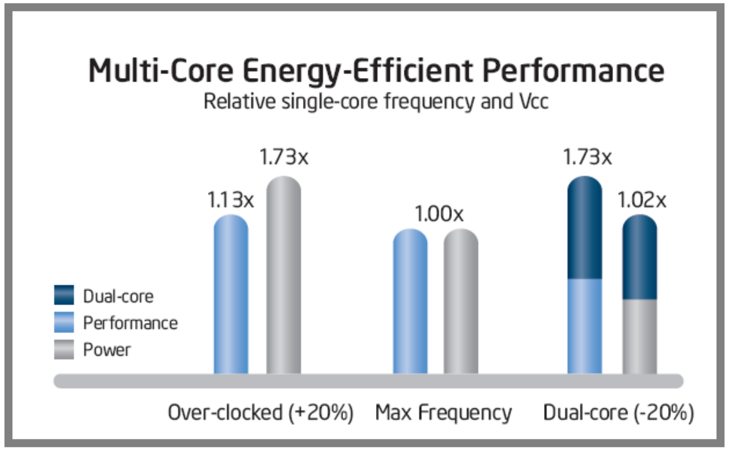
Dynamic Power   Static Power

- New design approaches => limit f, I_{OFF} management, etc…
- New devices architectures: High ION/IOFF or new concepts

Today new design approaches…



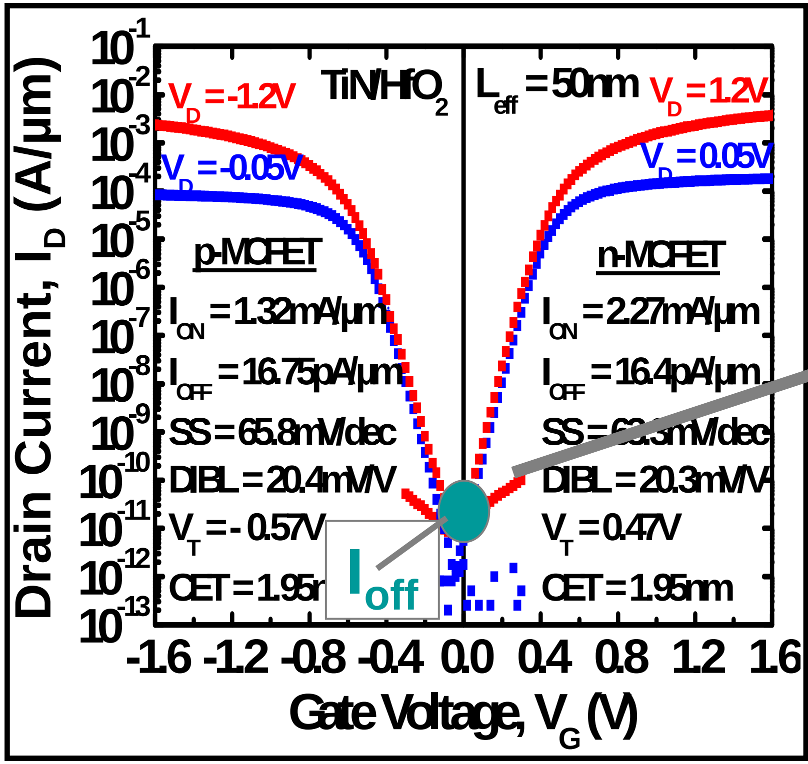


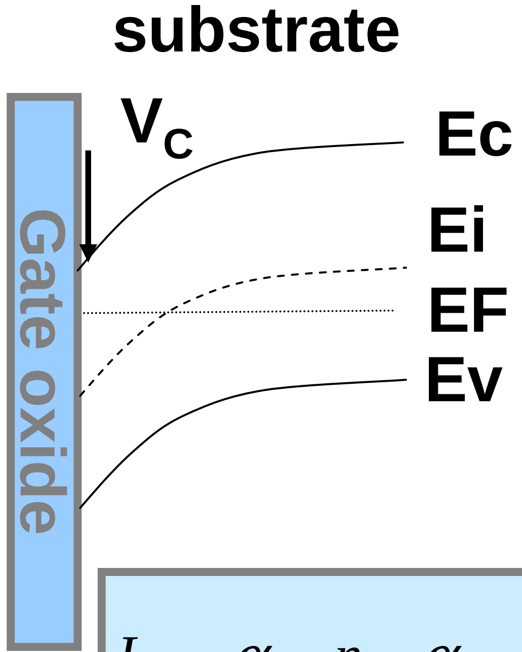


A Porobic, Microsoft

R.M. Ramanathan, Intel

Subthreshold slope limits V_{dd} reduction





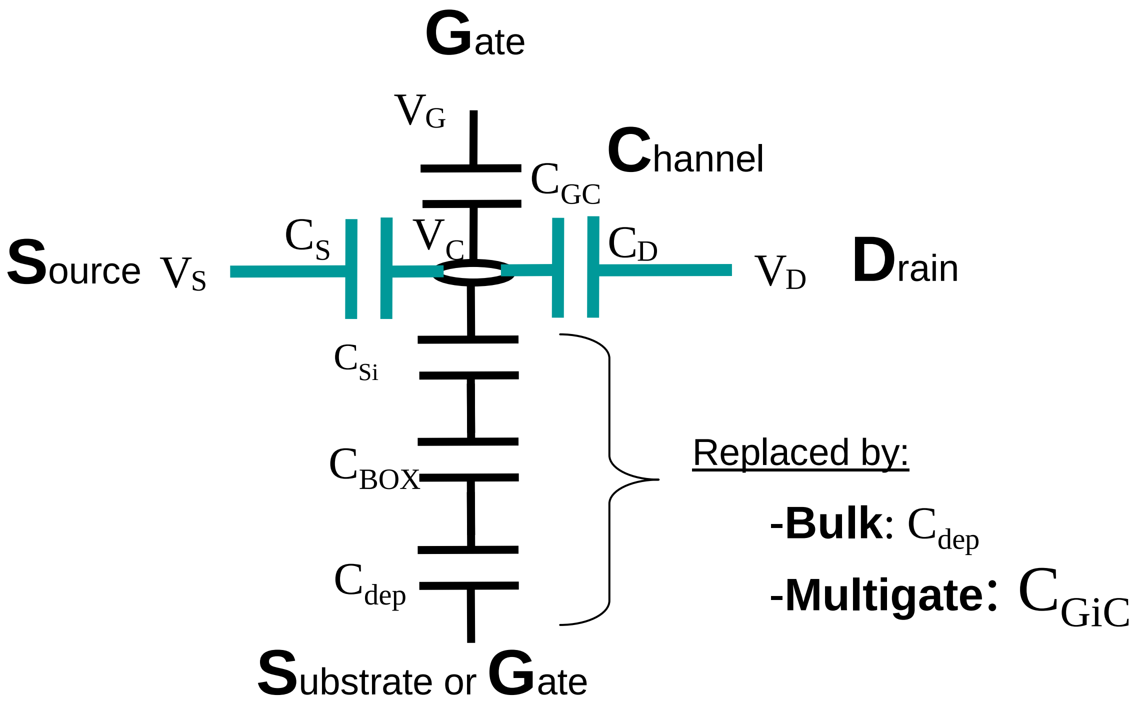
$$I_D \quad \alpha \quad n \quad \alpha \quad n_0 \cdot e^{\frac{q}{kT}V_C}$$

$$Log(n) \quad \alpha \quad \frac{q}{kT.Ln(10)}V_C = \frac{1}{S}V_C$$

New devices may be needed (T-FET, Mechanical….)

S_{min} = 60 mV/decade at room temperature…

Subthrehold slope limited by electrostatics



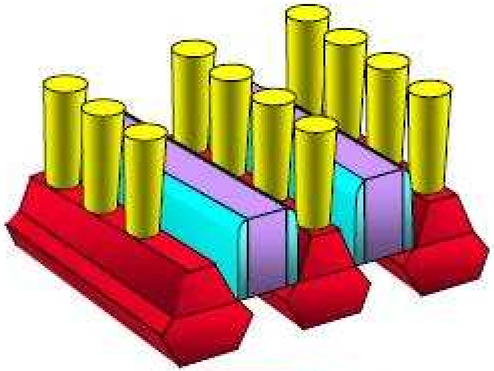
$$A = \frac{dV_C}{dV_G} = \frac{C_{GC}}{C_{tot}} \qquad B = \frac{dV_C}{dV_D} = \frac{C_{DC}}{C_{tot}}$$

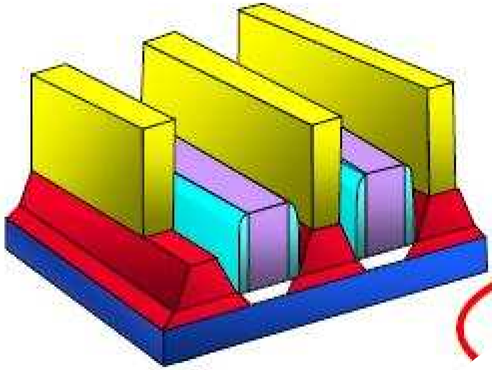
$$C_{tot} = C_{GC} + C_B + C_S + C_D$$

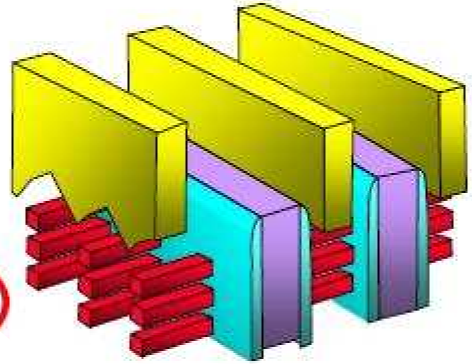
$$S = \frac{kT}{q} \ln 10 \frac{dV_G}{dV_C} = \frac{60mV/dec}{A} \qquad DIBL = -\frac{dV_T}{dV_C}\frac{dV_C}{dV_D} = -\frac{B}{A} = -\frac{C_{DC}}{C_{GC}}$$

Increase C_{GS}/C_{tot} => Multigate (NW?)

Future CMOS ?

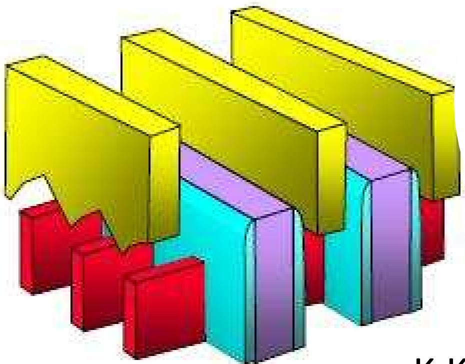


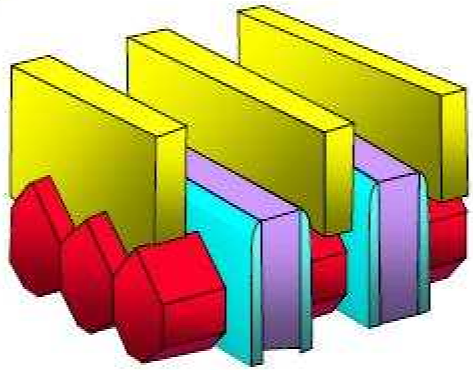




Many possible

thin film architectures....

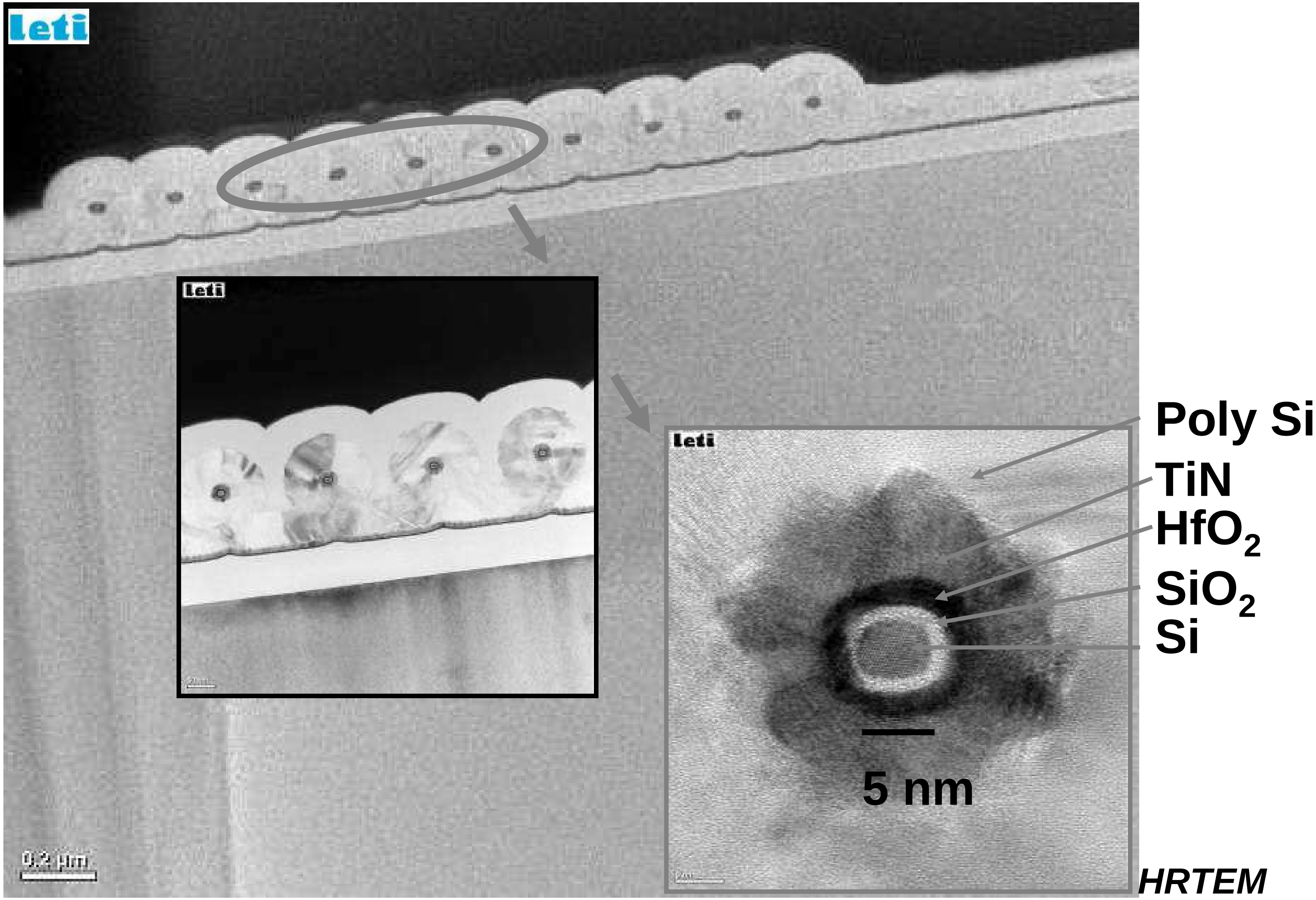




K.Kuhn , Intel, SSDM 2009

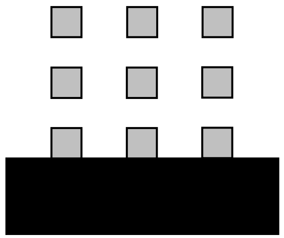
To be coupled with new materials to enhanced ON current III-V, Ge, C

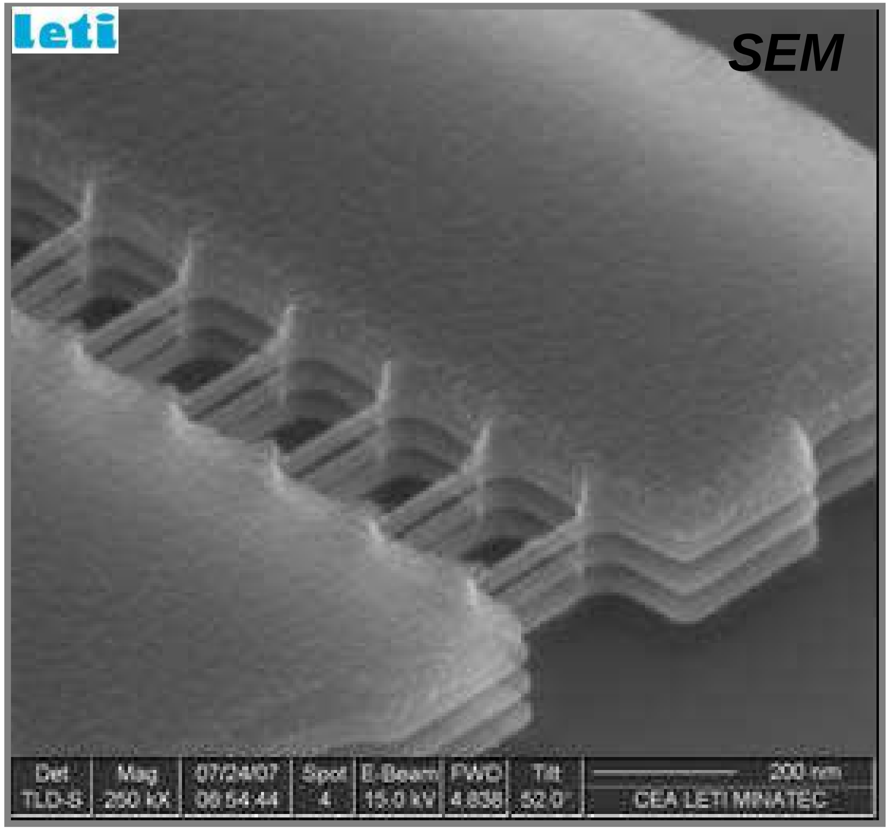
TEM of assembly 5nm nanowires

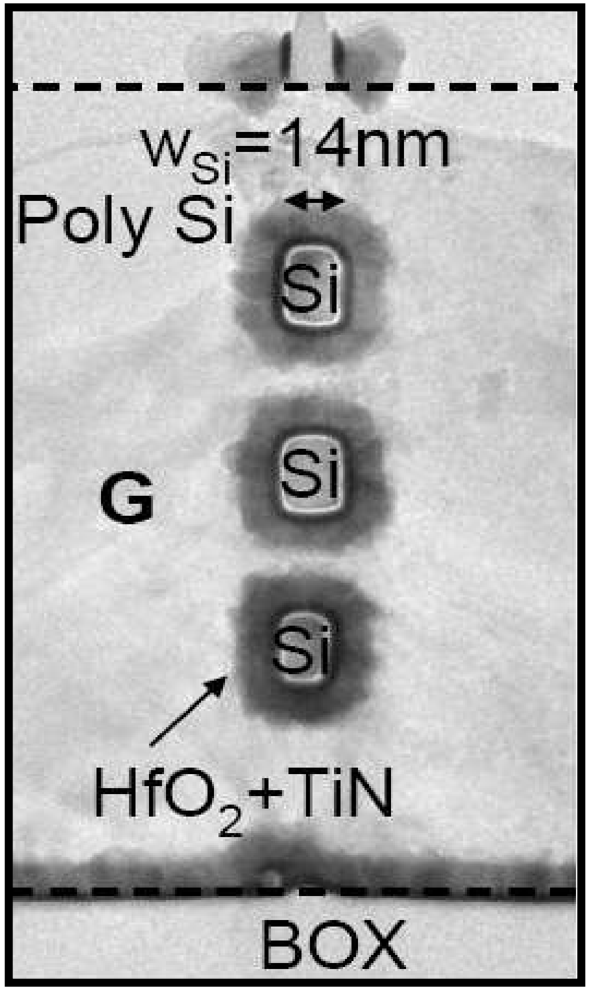


Diameter control of large nanowires assembly

Vertically stacked Nanowires for high current CMOS



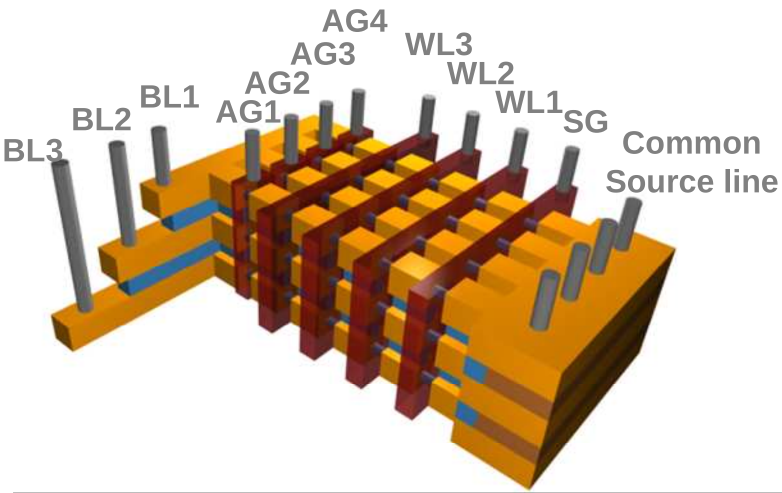


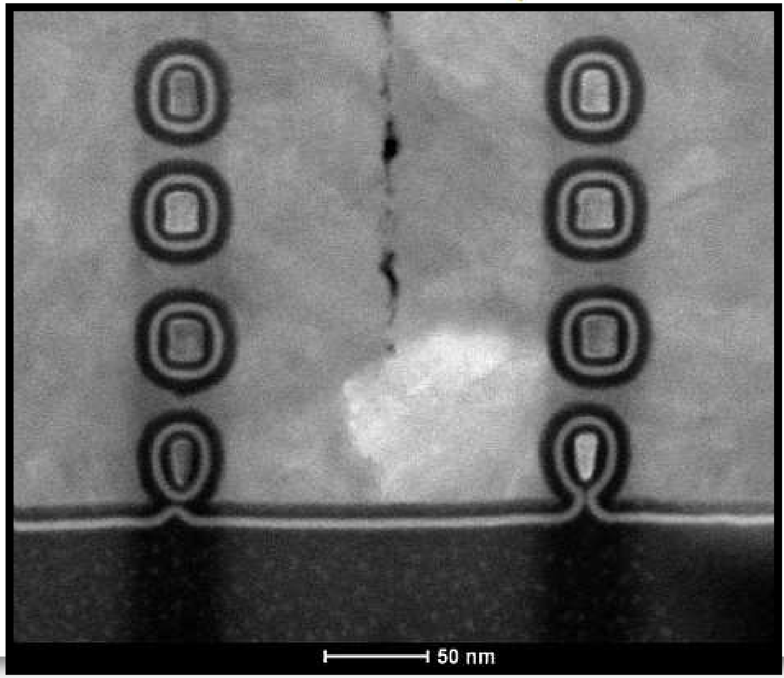


T. Ernst et al., IEDM O6,08

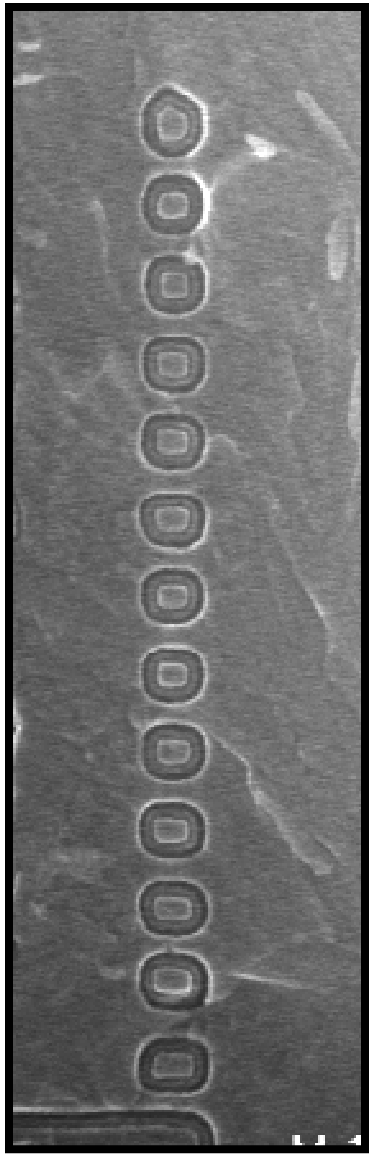
K. Tachi et al IEDM 09,10

Application to 3D Flash …





13 levels !



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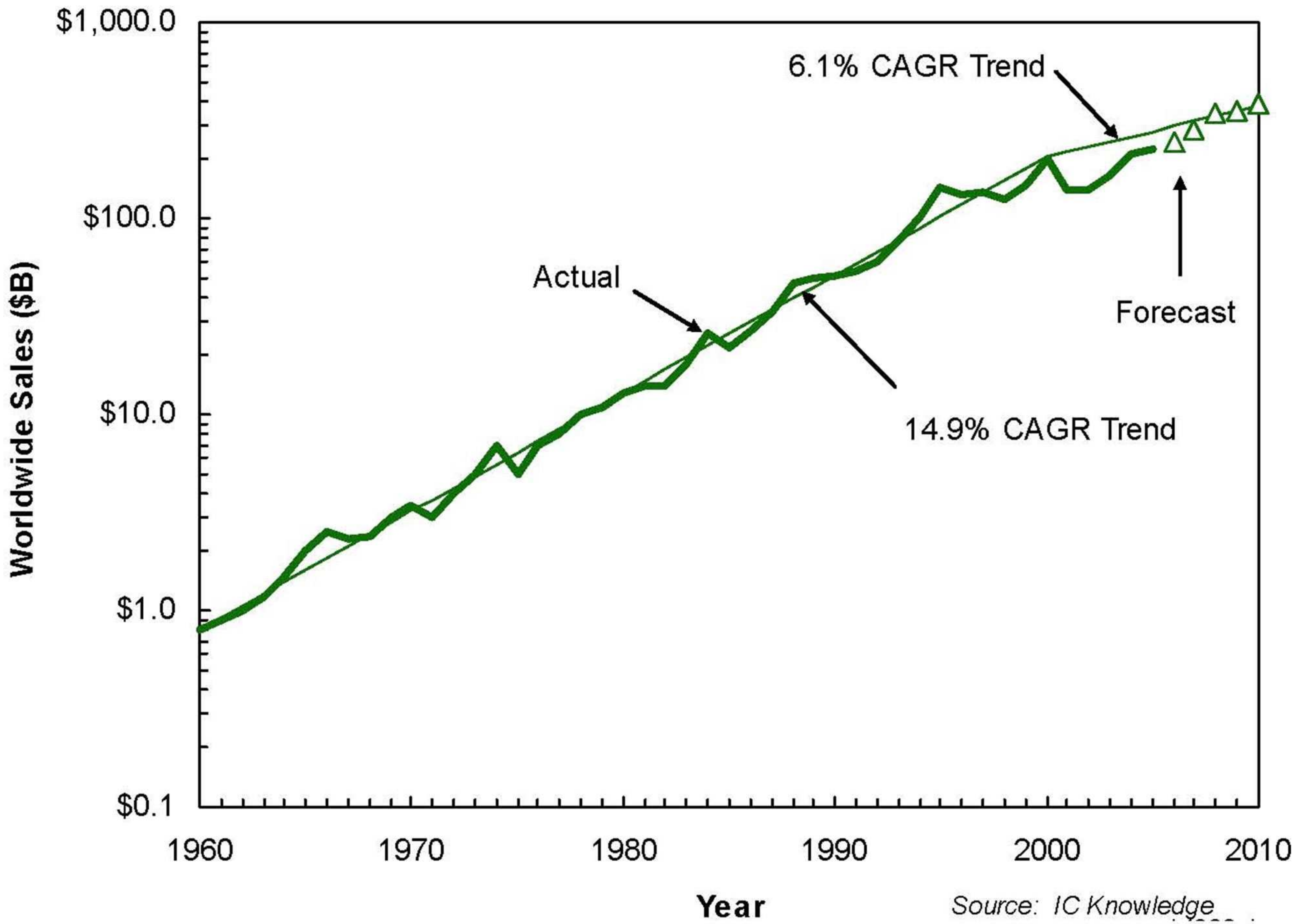
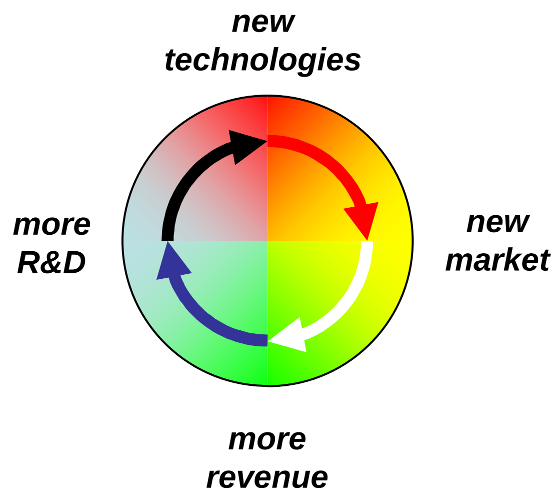
The exponential market growth



… needs « killer applications »

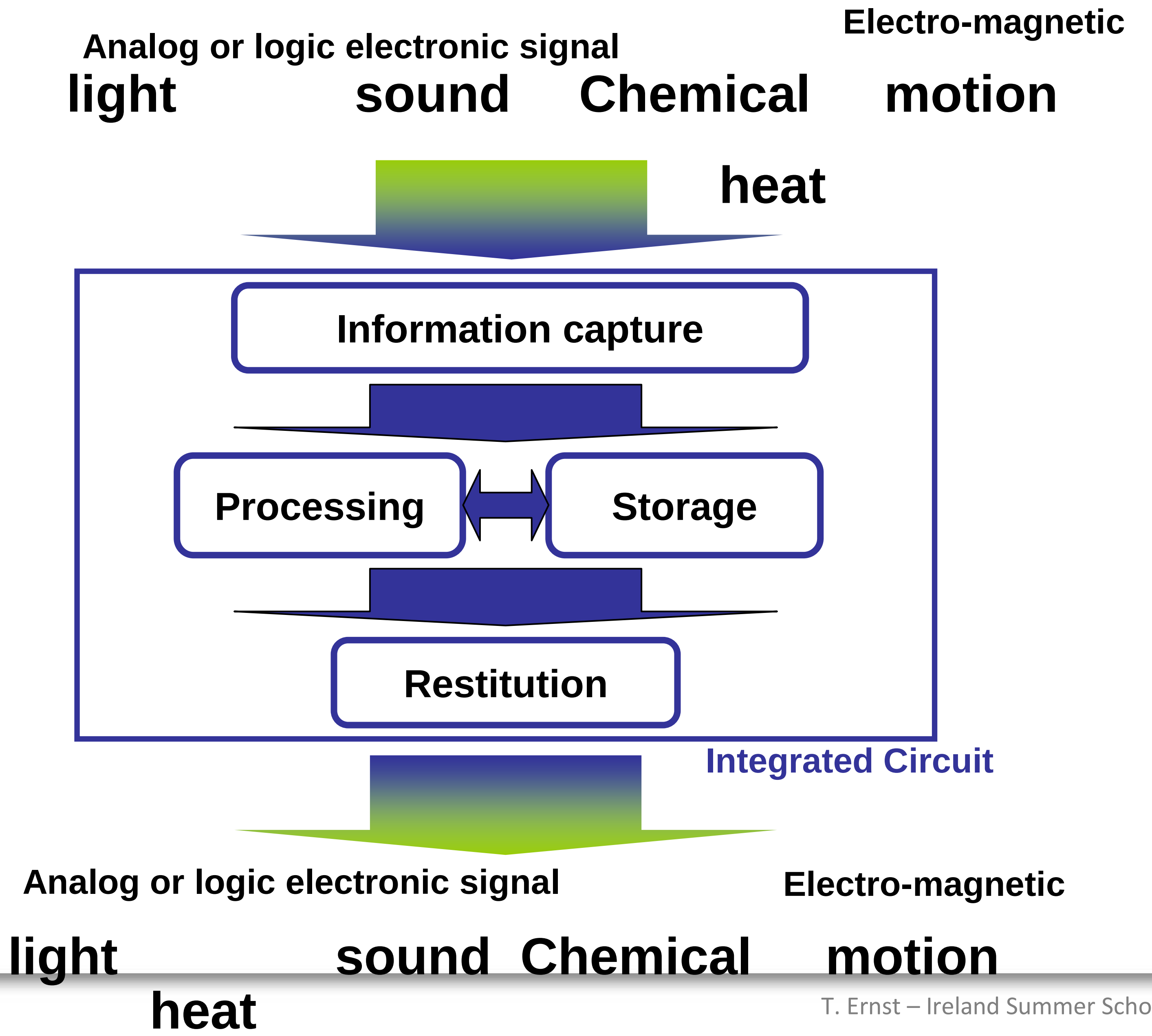
- The conjunction of the cost per function decrease and the emergence of "killer applications" which demanded a large volume of leading edge chip has been the revenue generator for the industry and its sustainability

  - 1980s → Analog for TVs and VCRs
  - 1990s → Digital for PCs
  - 2000s → Analog and Digital for Cell Phones
  - 2010s → Analog and Digital for Mobile Internet
  - 2020s ???



C. Reita, LIA workshop

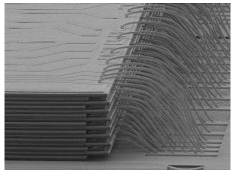
More and more signals in a chip



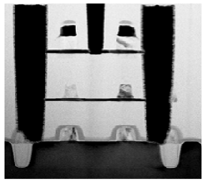
Tomorrow driving applications ?...

Moore

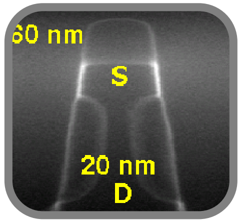
- **90nm**
- **65nm** ***Strained***
- **45nm** ***High-k***
- **32nm**
- **22nm** ***3D Tr***



3D die stacking

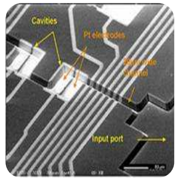


3D circuit

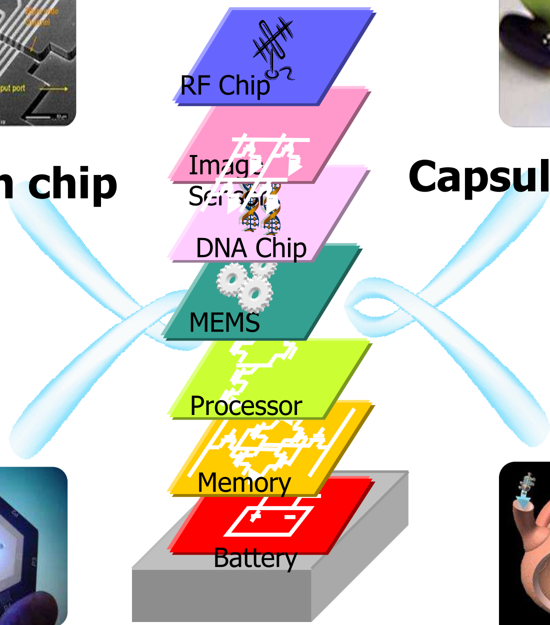


3D transistor

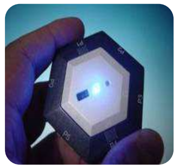
Adapted from Kwon 2007



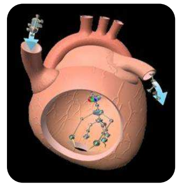
Lab on chip



Capsule endoscope



Integrated sensor



Medicine nano-robot

For devices => Ultra-low power

3D : not only ultradensity but …

- An opportunity for new devices that cannot be implemented in CMOS easily: III-V, new memories, carbon electronics, sensing devices

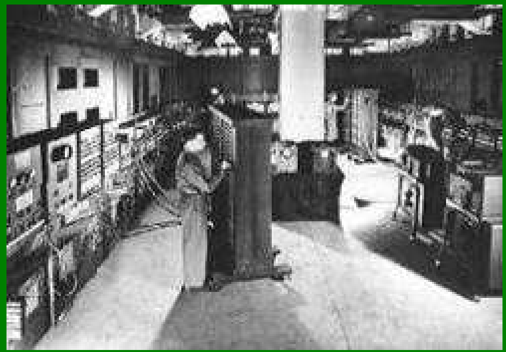
- Specific need for autonomous chips that can boost ultra low voltage devices: thin films, steep slopes …

- Need to develop design methodology at the system level

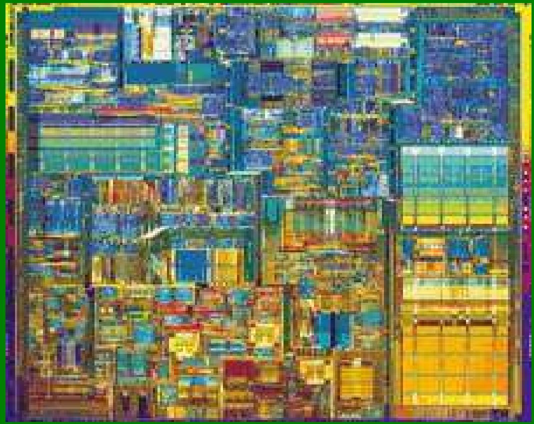
Disruptive devices - which path should we follow ?

The microelectronic revolution… inspired by silicon and VLSI

WW II: Simple machines and manual laborers fill a room.



1955: ENIAC, the first electronic computer, fills a room.



2000s: The integrated circuit has made computation ubiquitous.

- Complex functions integrated - High performances
- Existing manufacturing or design tools, processes, design rules
- Existing micro sensors… (Accelerometers, gyros, imagers, TCD, inkjets etc…)
- A lot of opportunities (assembly, costs, architecture etc…)

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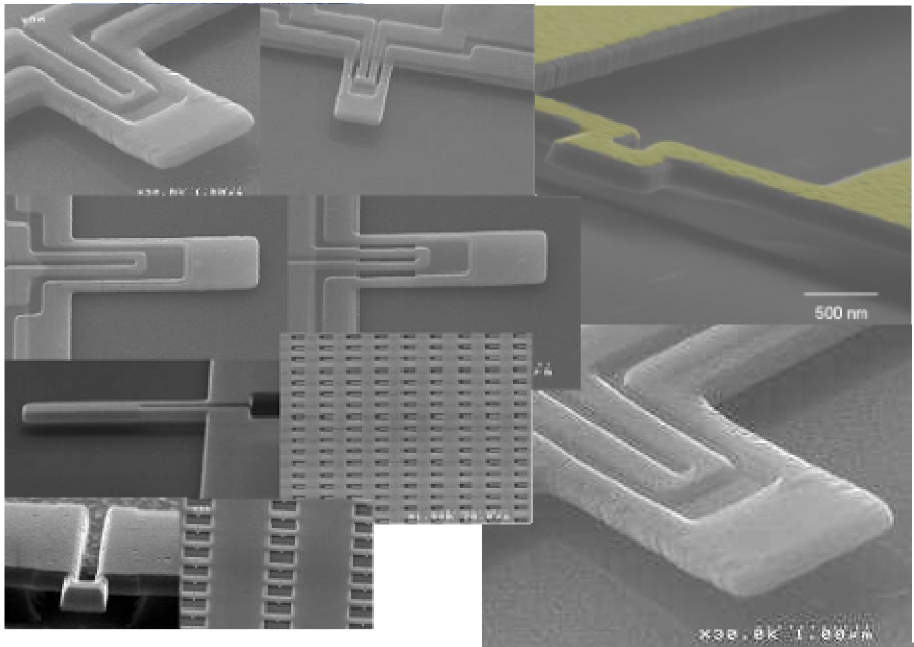
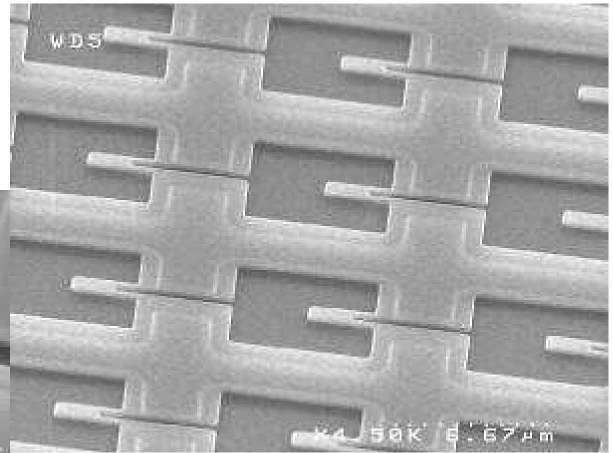
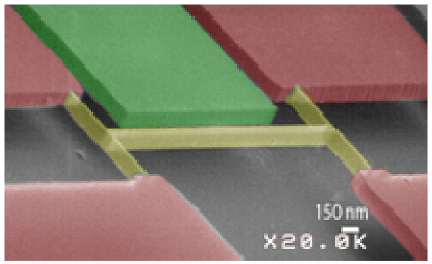
An example: NEMS at VLSI scale





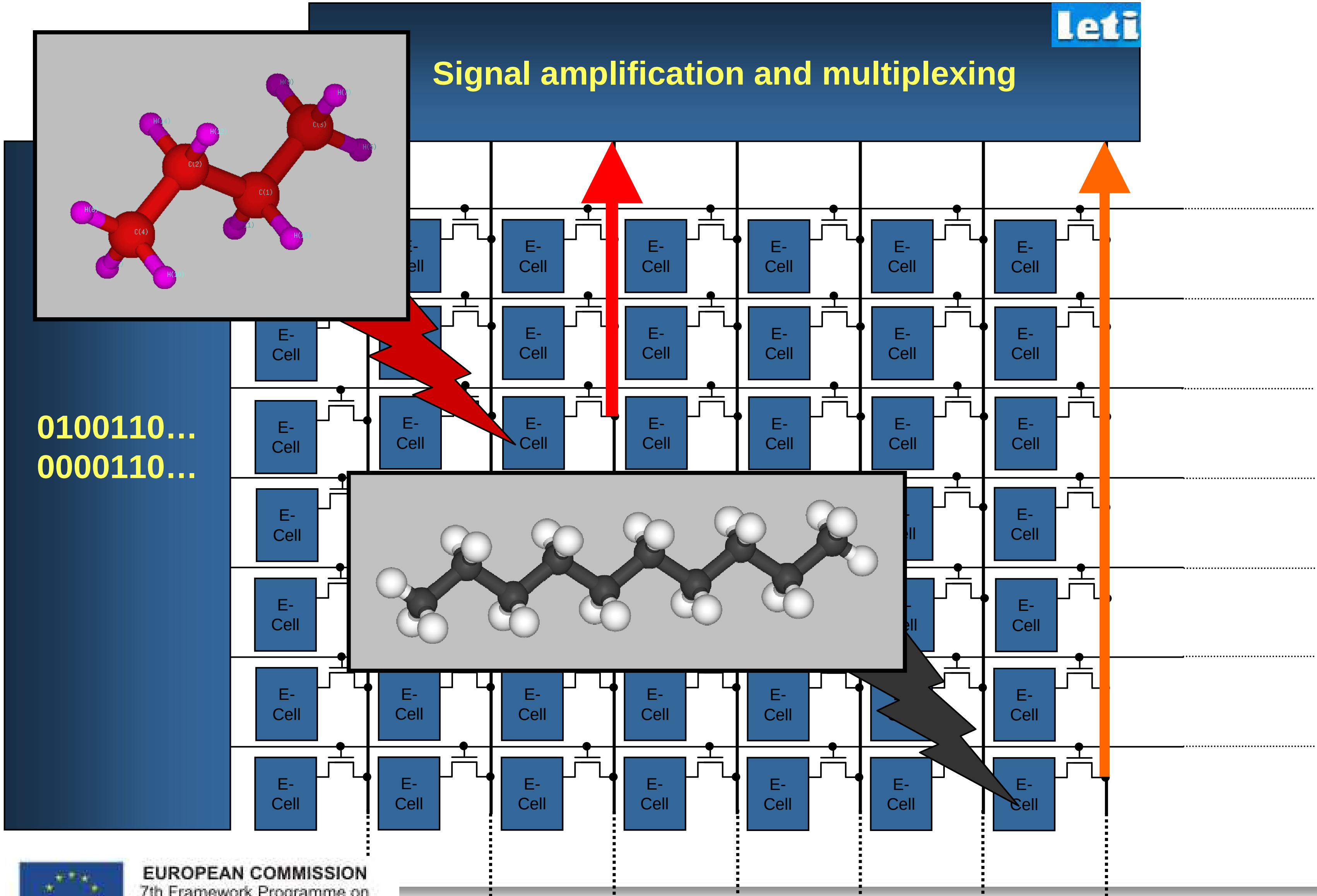


First large arrays of NEMS

~60.000 NEMS / mm²

EUROPEAN COMMISSION
7th Framework Programme on Research, Technological Development and Demonstration

A multi-physics system vision



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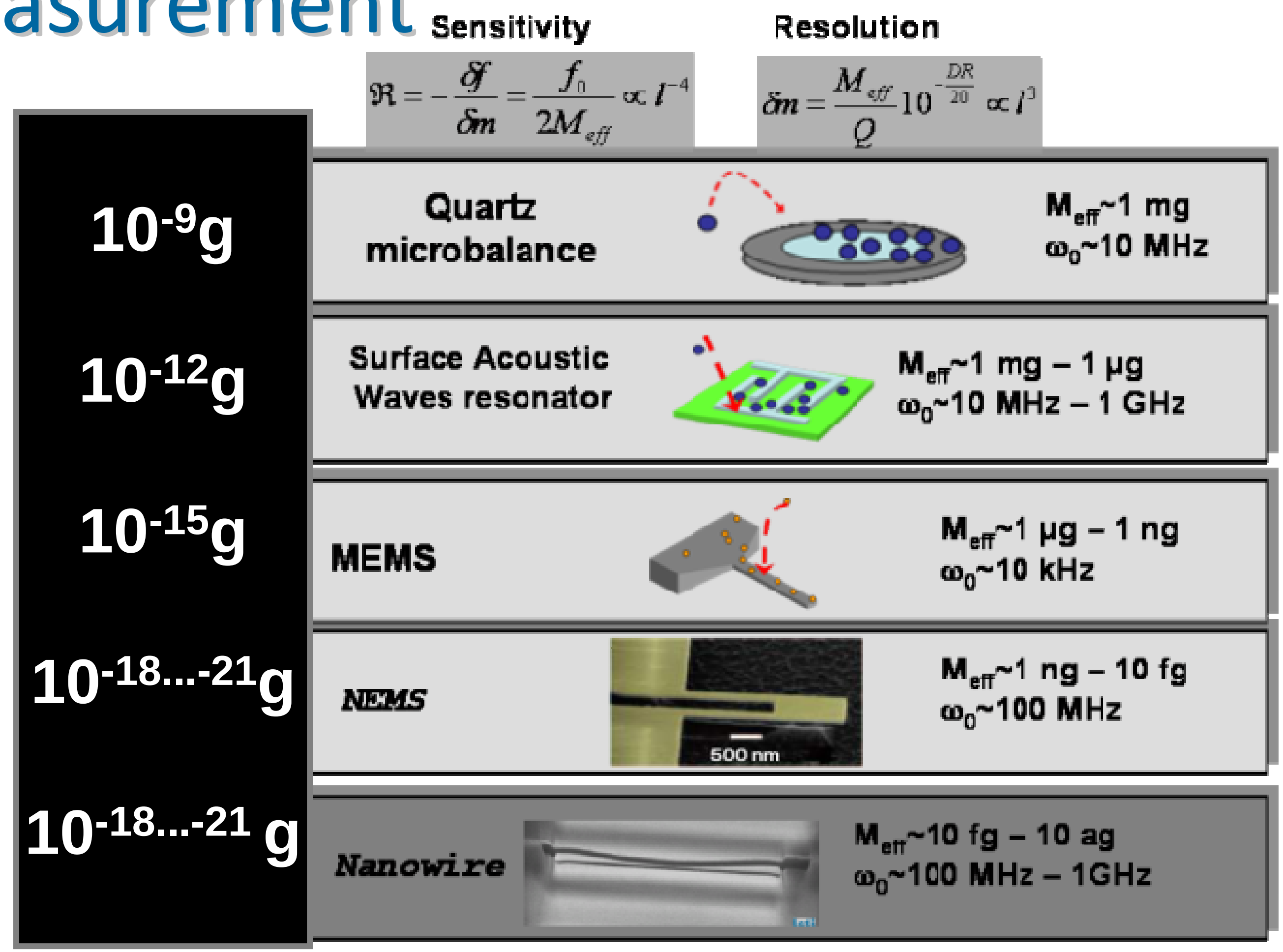
Nanowires for very sensitive mass measurement



T. Ernst et al., IEDM 08

Few molecules sensitivity can be achieved => 1zg

Mass units in biology

Atomic mass unity = 1Da = 1 u ≈ $1.66053886 \times 10^{-27}$kg

1zg = 10^{-21}g = 602 Da ≈ a nucleotides pair (DNA)

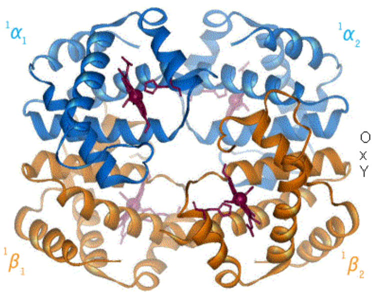
Nanowires

NEMS

A-T — 613.4 Da

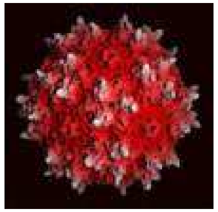
G-C — 616.4 Da

Hemoglobine A molecule — 66.2 kDa

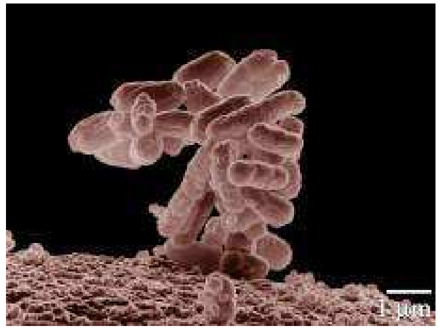


Protein PrP (Prion) — 150 kDa

Parvoviridae viruses: Hepatitis B — 1.1 MDa

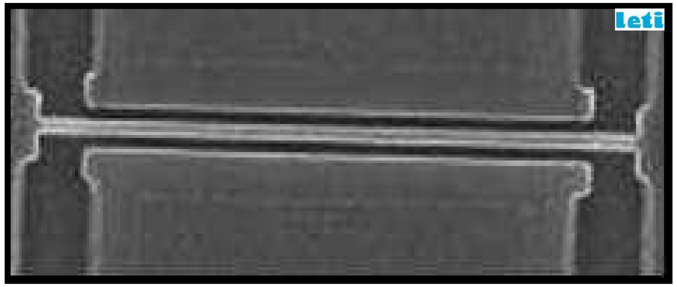


E. Coli bacteria — 4.2×10^{11} Da

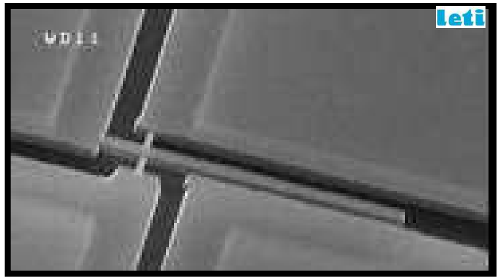


V. Agache et al.

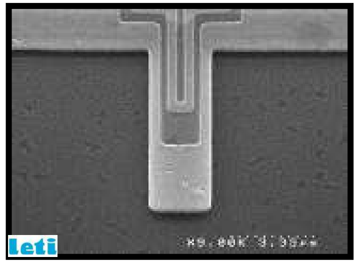
Nanowire used for mass detection



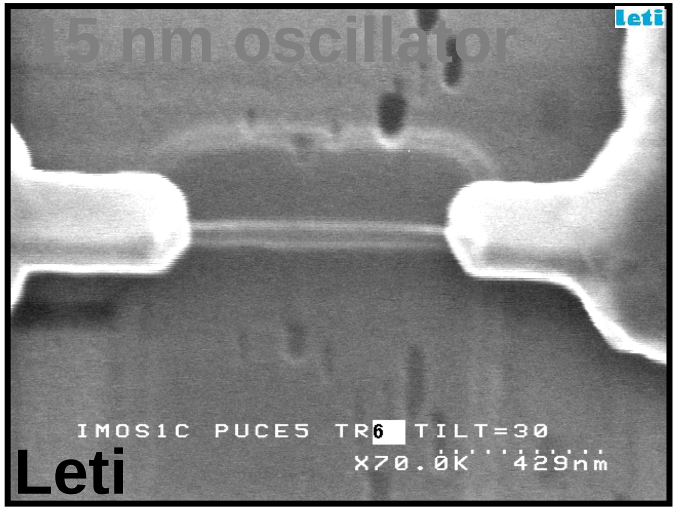
Capacitive actuation & detection

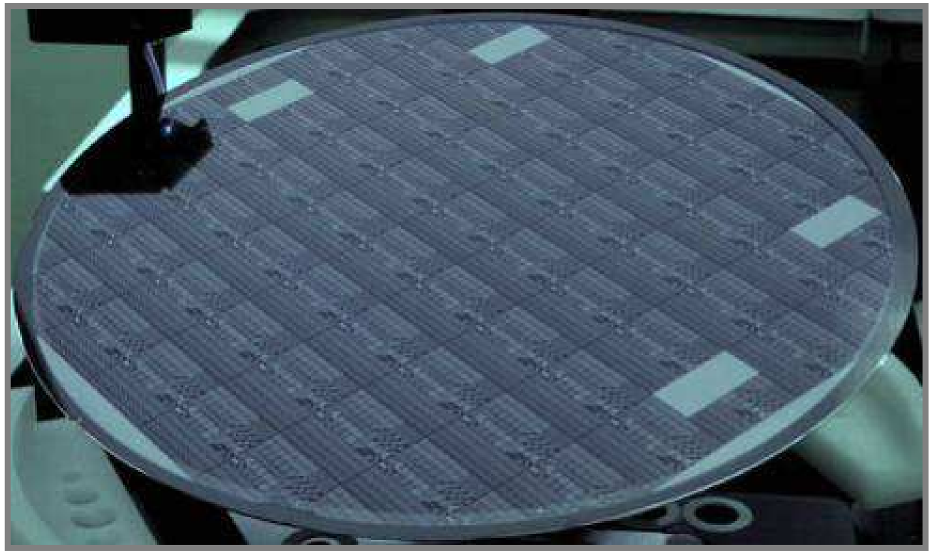


Capacitive actuation & piezo-resistive detection with nanowires



Thermo-elastic actuation & piezo-resistive detection.

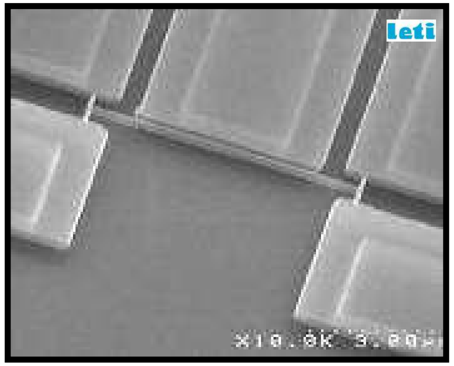


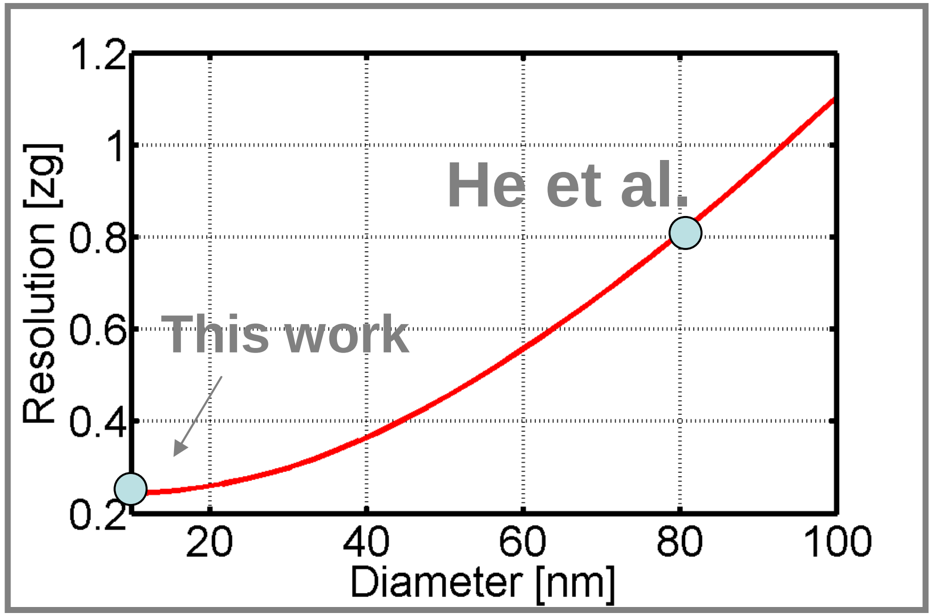


First 200 mm wafers with 3.5 millions NEMS

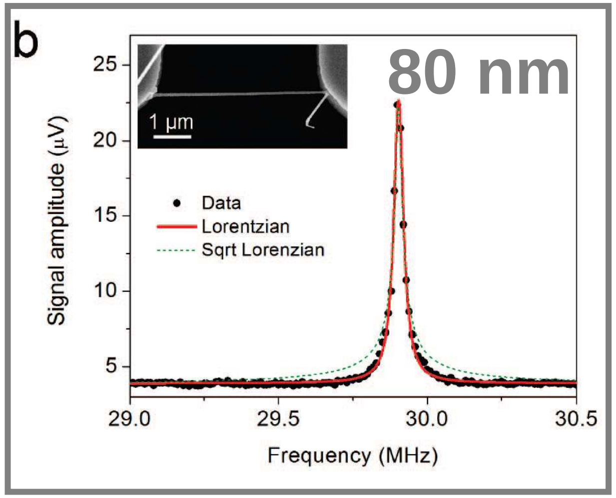
CALTECH & LETI VLSI NEMS Alliance

Mass resolution with nanowire

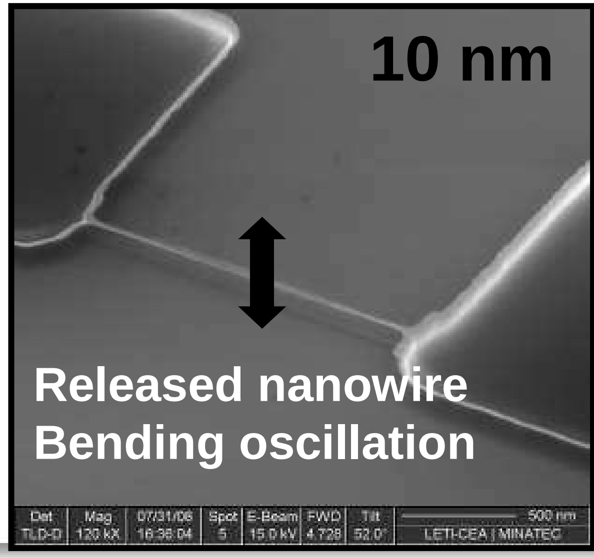




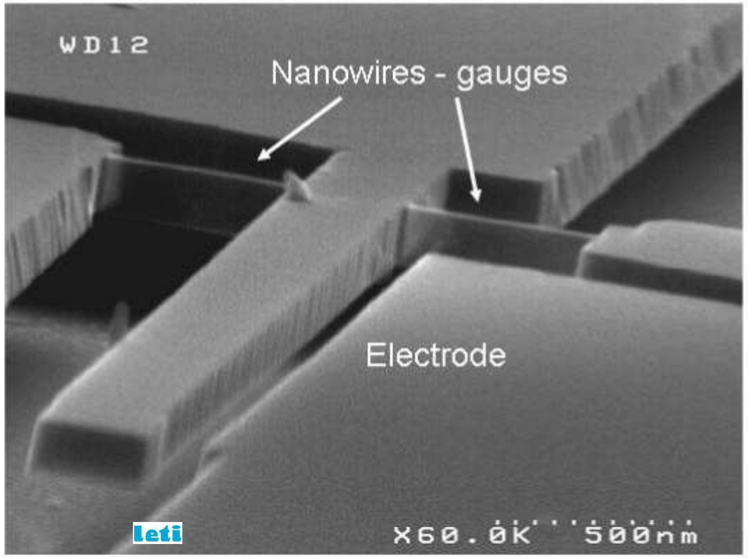
Mass resolution according to the diameter

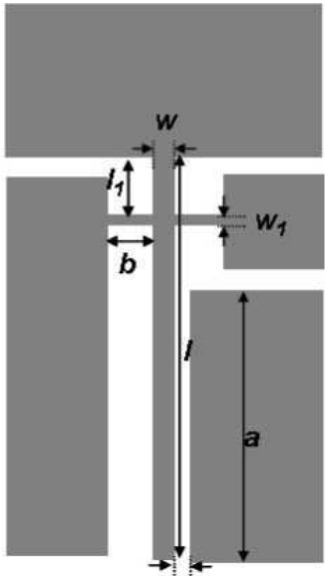


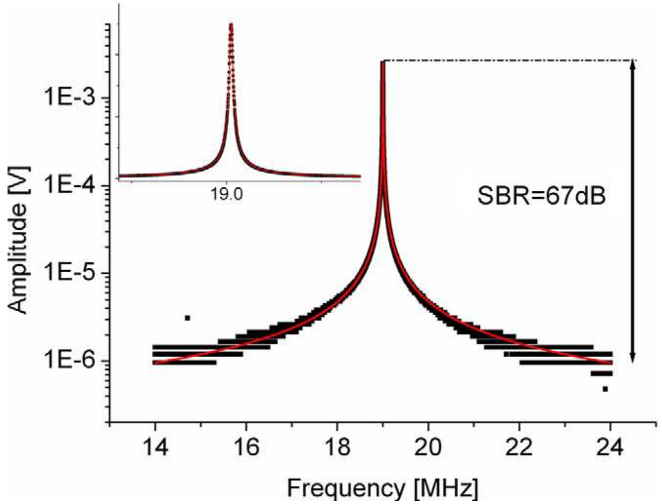
R. He, M. Roukes et al. Nanoletters 12/08



A new design example







E. Mile et al., Nanotechnology 21 (2010) 165504, Leti Patent

Electrostatic actuation

- **Piezzo resistive detection (down mixing scheme)**
- **Excellent Signal to background ratio**

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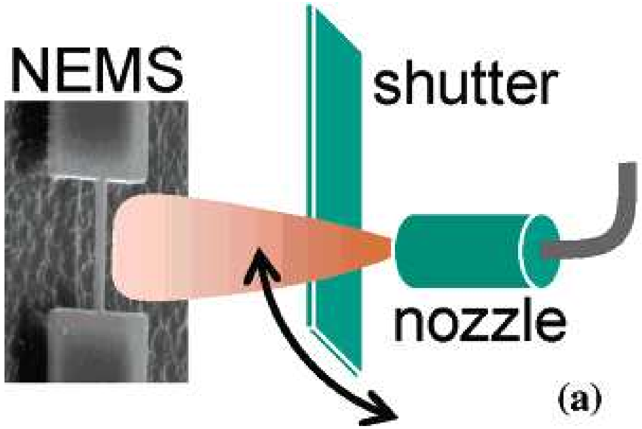
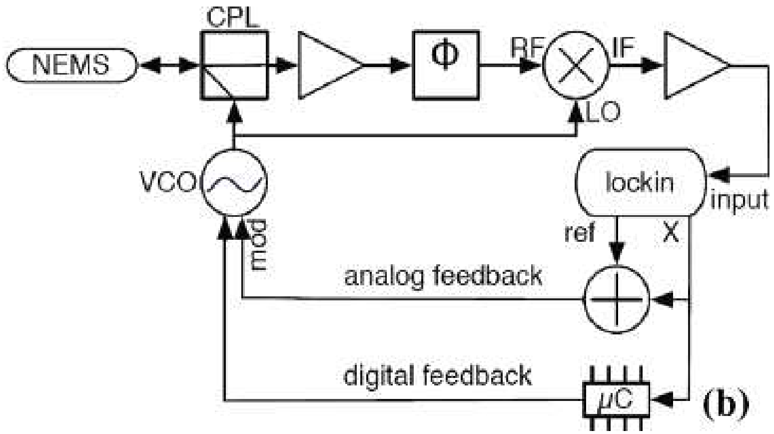
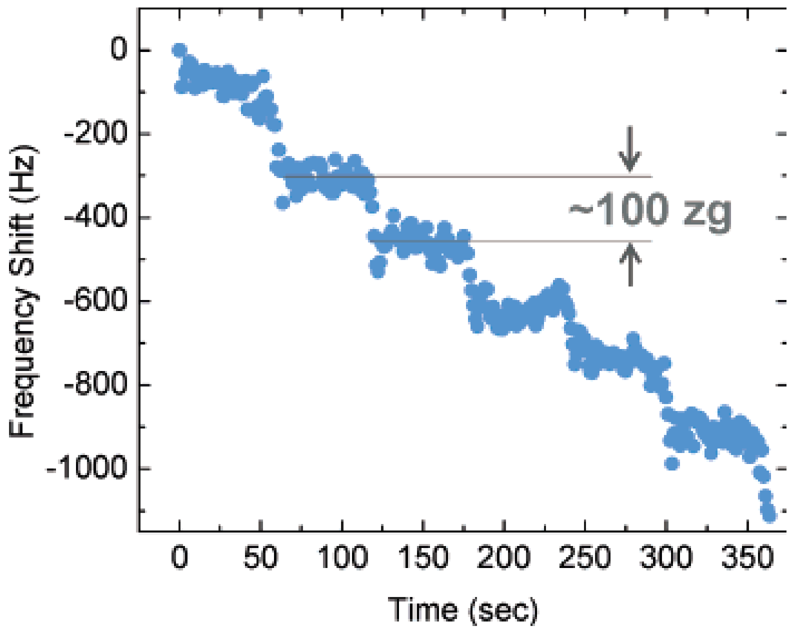
Mass sensing demonstration







best mass resolution corresponds to 7 zg (30 xenon atoms)

Yang et al., Nano Lett., Vol. 6, No. 4, **2006**

Goals

- Bring **in situ** the power of chemical analysis for gas measurements – Bring analyzer to samples
  - To the heart of the industrial processes
  - Into environment of work or of everyday life

- Develop integrated multigas analyzers with less utilities
  - Carrier gas – Air
  - Low power, low volume, low maintenance – ATEX proof
  - No more or Less sample transportation

Goals…

Gas sampling

- Open panel of analytes
- Uncontrolled environment
  - Sample complexity, contaminants, concentration range…

Multigas detection and analysis system
Real time – in situ

Analytical performances comparable to lab tools (sensitivity, number of compounds, robustness)

Quick measurements

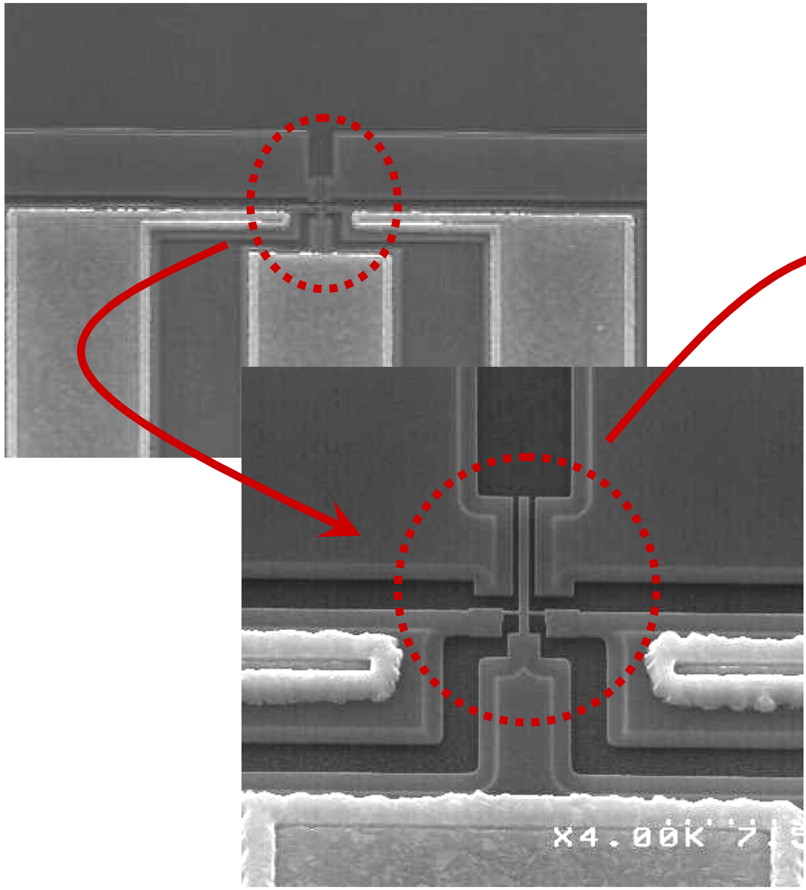
10-100x smaller

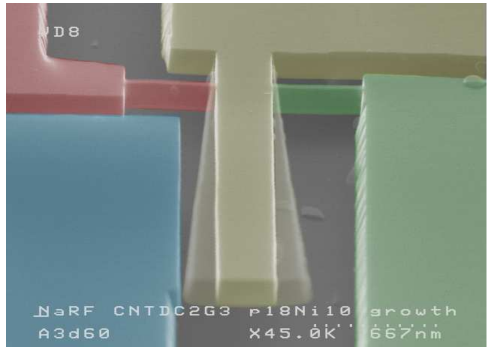
Economy of scale for large volume

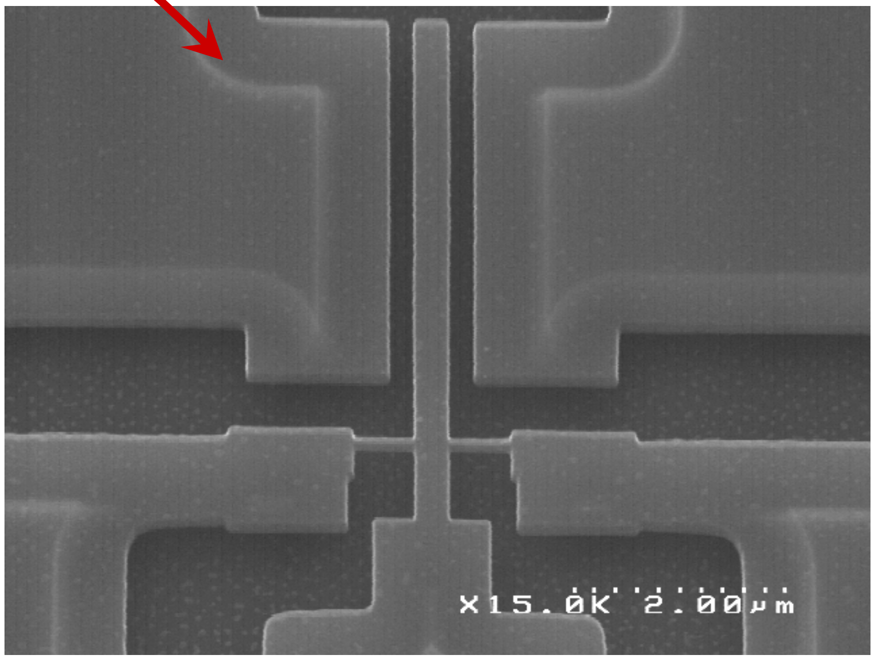
List of different present components with their concentrations [Ci]

- Large detection range (sub-ppm à 100-1000 ppm)

Functional validation of NEMS detector



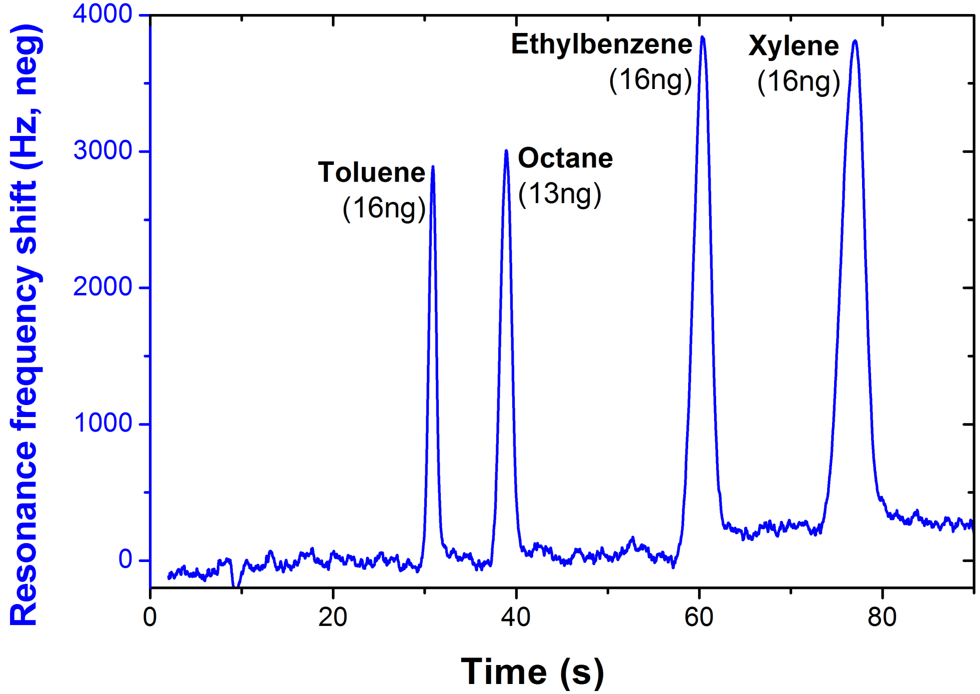




Leti Patent

Gaz recognition

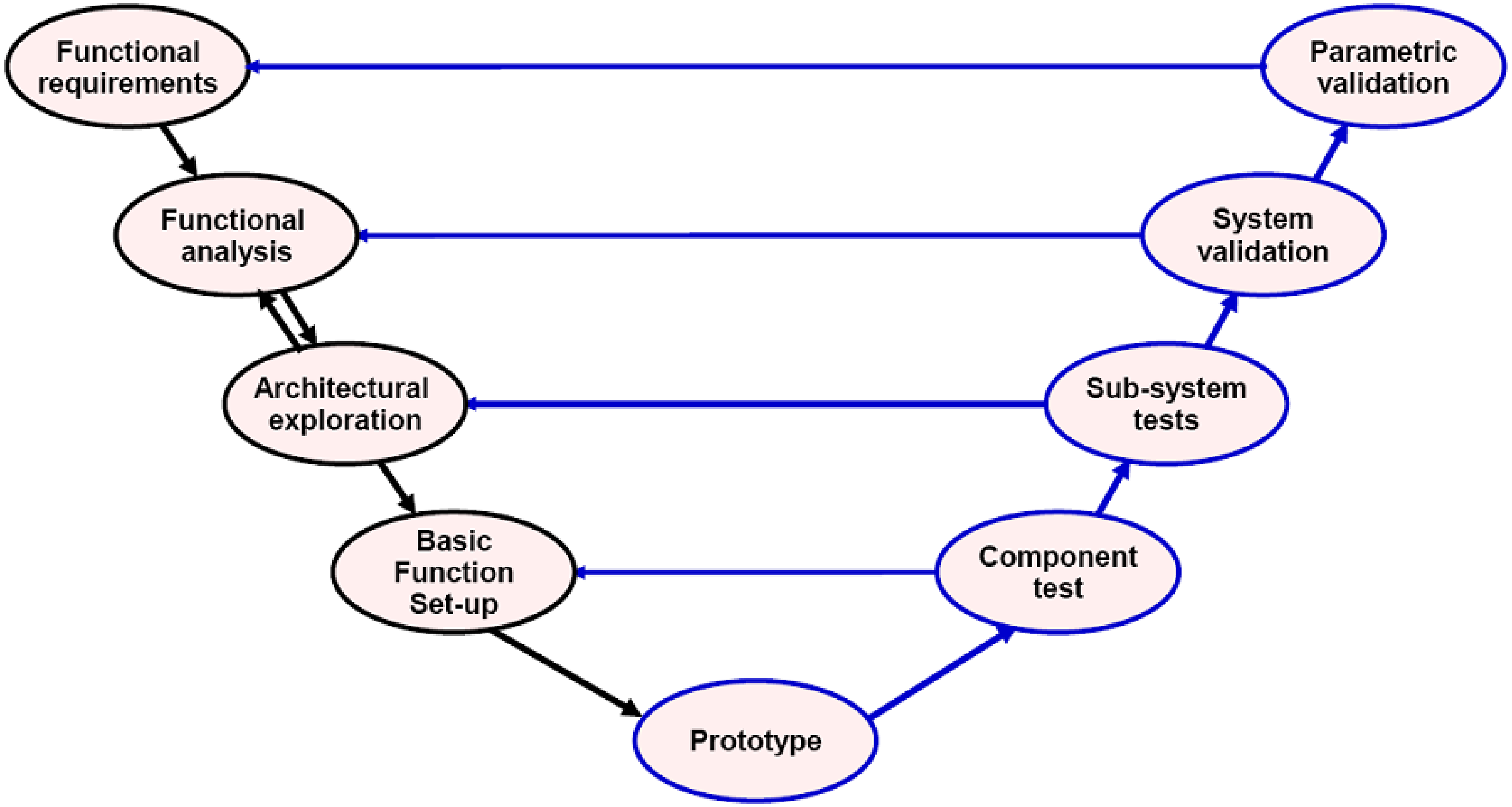
Ref: J. Arcamone et al., IEDM 2011



Partnership:

Apix, startup from LETI and Caltech

Design system methodology: **from** V-shaped cycle



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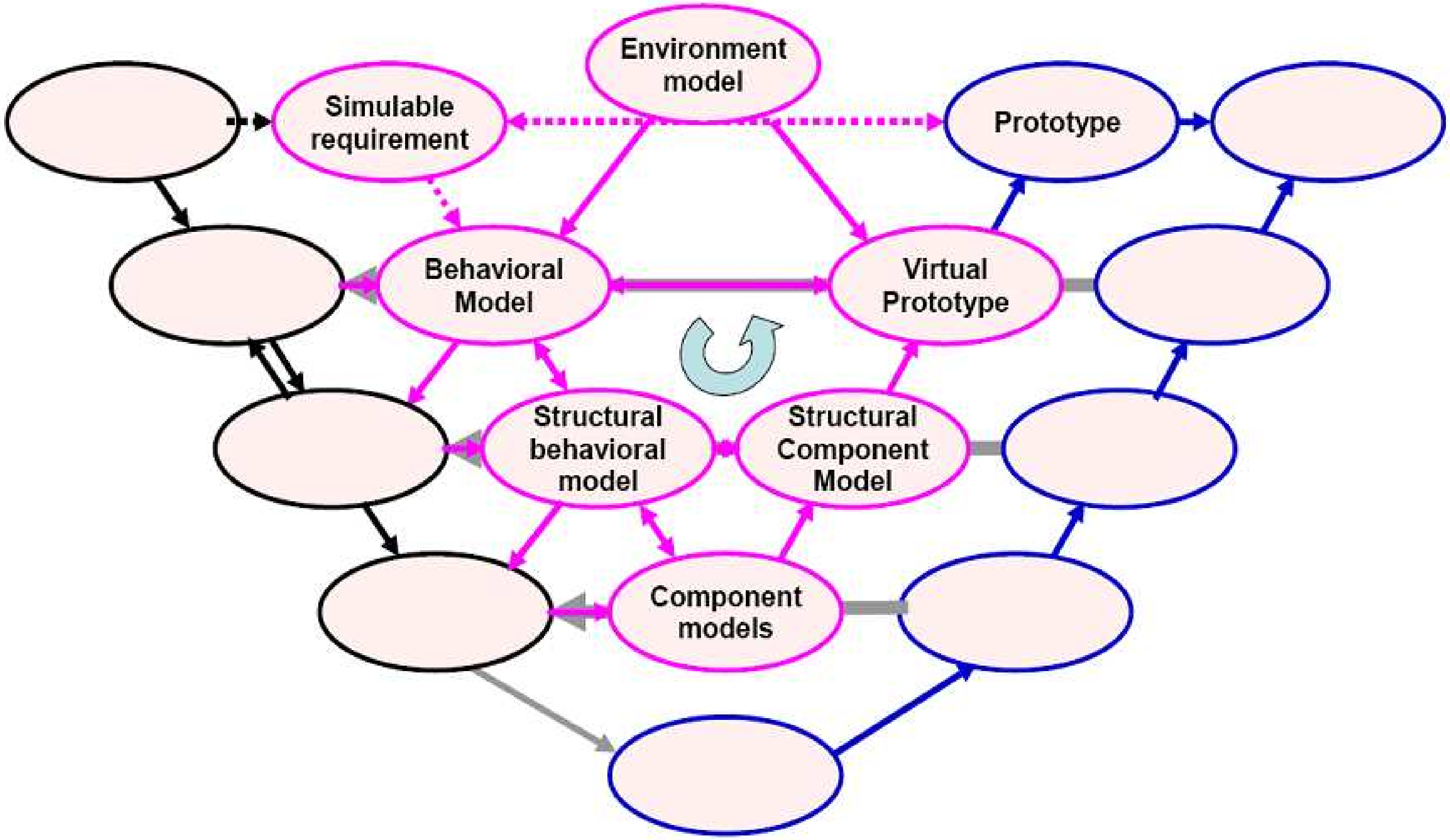
From Y. Hervé et al.

Design methodology: **from** V-shaped cycle **to** FVP **(Functional Virtual Prototyping)**



From Y. Hervé et al.

For any new devices, a sufficient maturity is needed for:

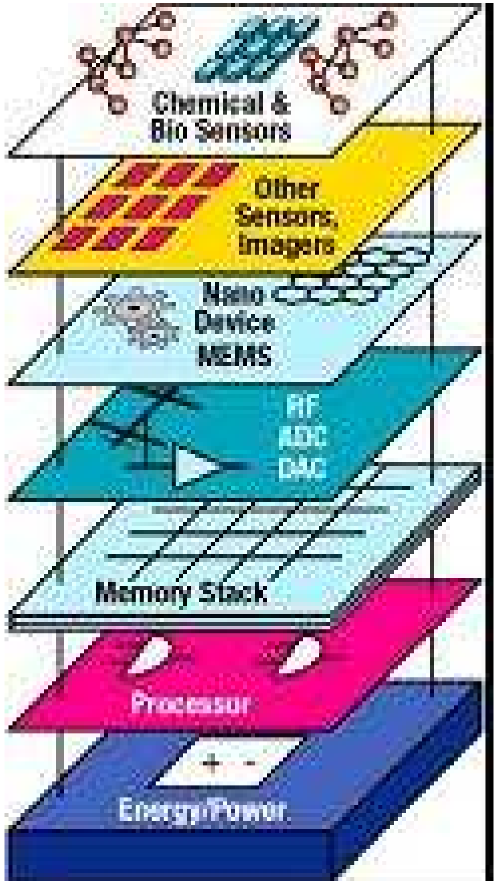
- Compact models
- Introduction in a Design Kit
- Evaluation of performance in the system environment

=> Development of "multiphysics" simulation

& technology platforms

=> NEW devices at VLSI SCALE will need high volume application

New opportunities for emerging devices
Will we replace or complete CMOS ?



Jian-Qiang Lu, *Proceedings of the IEEE* , 2009

- Chemical sensors

- Diodes
- NEMS, MEMS …

- sensors readout circuits
- New passive or active device

- New memories

- New data processind devices
  - high mobility
  - SOI, Nanowire, carbon, TFet, …
  - magnetic devices.

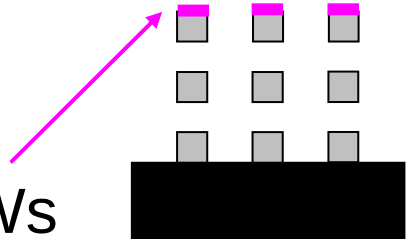
- High capacitances
- Thermoelectric devices
- µ battery or generators

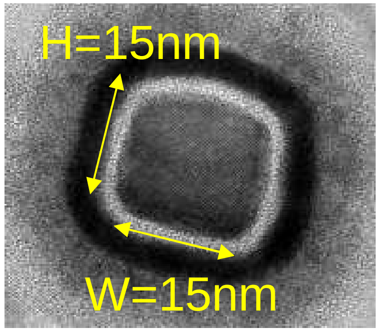
To sum up…

- Sub 22nm CMOS: trigate, SOI, nanowire + new channel materials
- New applications (ultra-low power) may drive revolutionary devices : mechanical, TFET, new memories & associated designs…
- More than Moore & 3D may be an opportunity for new devices
- But standardized (3D) approaches needed => high volume
- System level multiphysics simulation is required integrated several types of devices (in 3D)
- A good feeling of emerging markets & investment capabilities will help…
- The ability to think out of the box is needed !

I_D-V_G characteristics

Normalization : Top view width of NWs



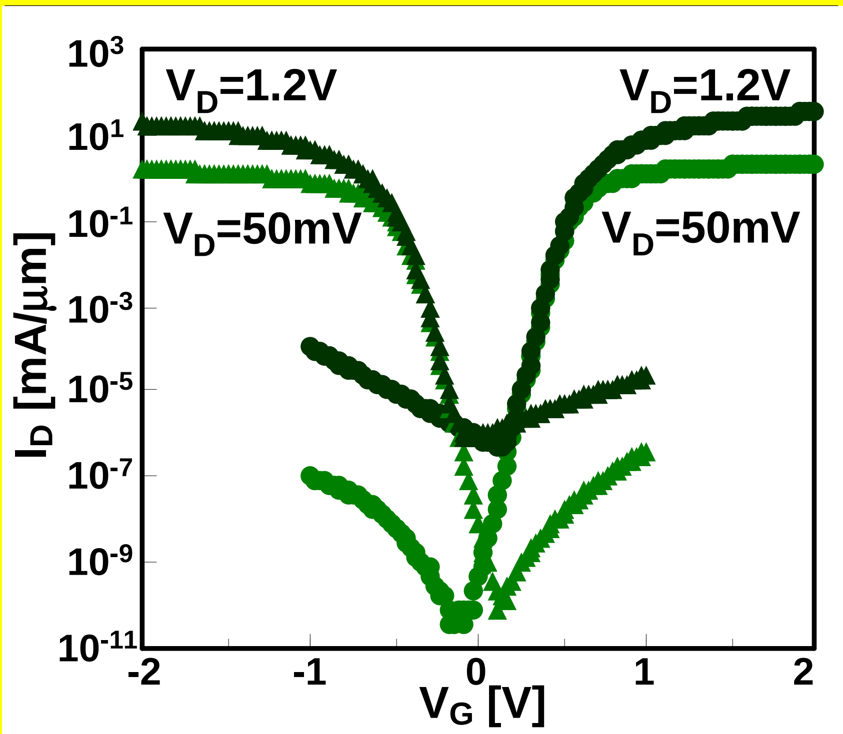


pFET

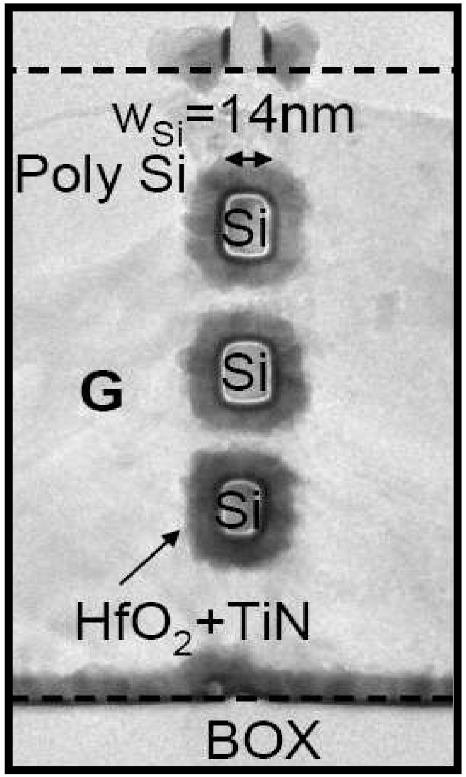
V_T = -0.45V
SS = 62mV/dec
DIBL = 17mV/V
I_{ON} = 3.9mA/µm
I_{OFF} = 0.1nA/µm

nFET

V_T = 0.50V
SS = 62mV/dec
DIBL = 17mV/V
I_{ON} = 5.7mA/µm
I_{OFF} = 0.1nA/µm



L_G=120nm



- High I_{ON} thanks to the vertical stacked NWs

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DE L'INFORMATION

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Thank you for your attention