



Transitioning beyond classical CMOS

Chronicle of a (R)evolution foretold

Marc Heyns

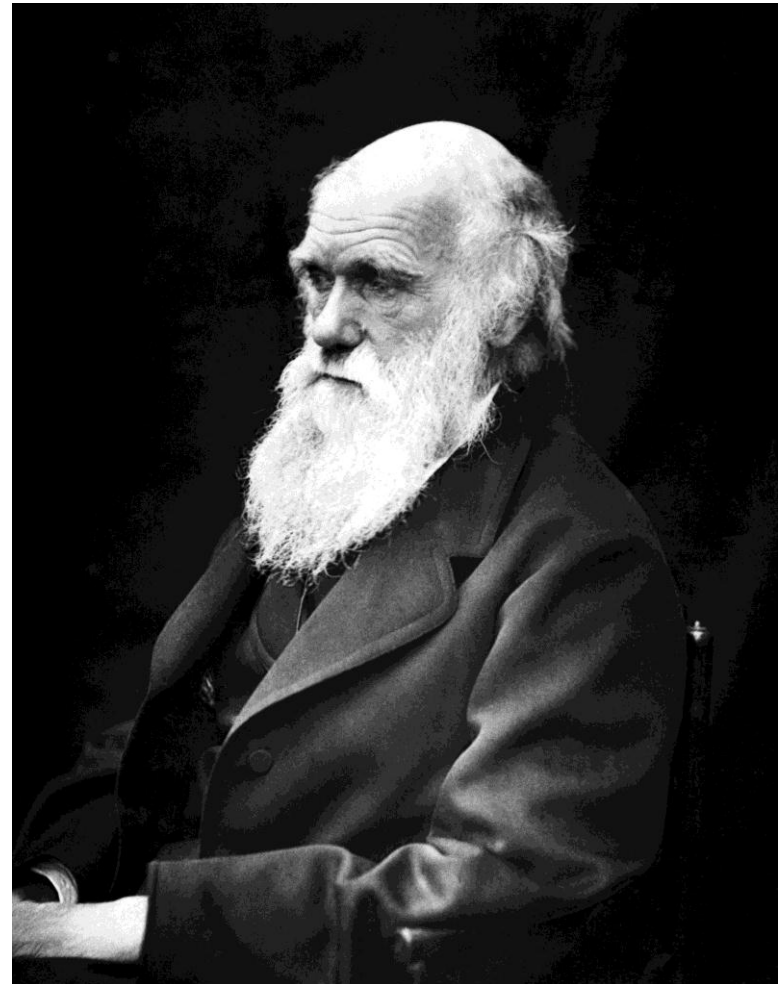
imec, Kapeldreef 75, B-3001 Leuven, Belgium

also at Metallurgy and Materials Engineering Department, K.U. Leuven



Evolution ...

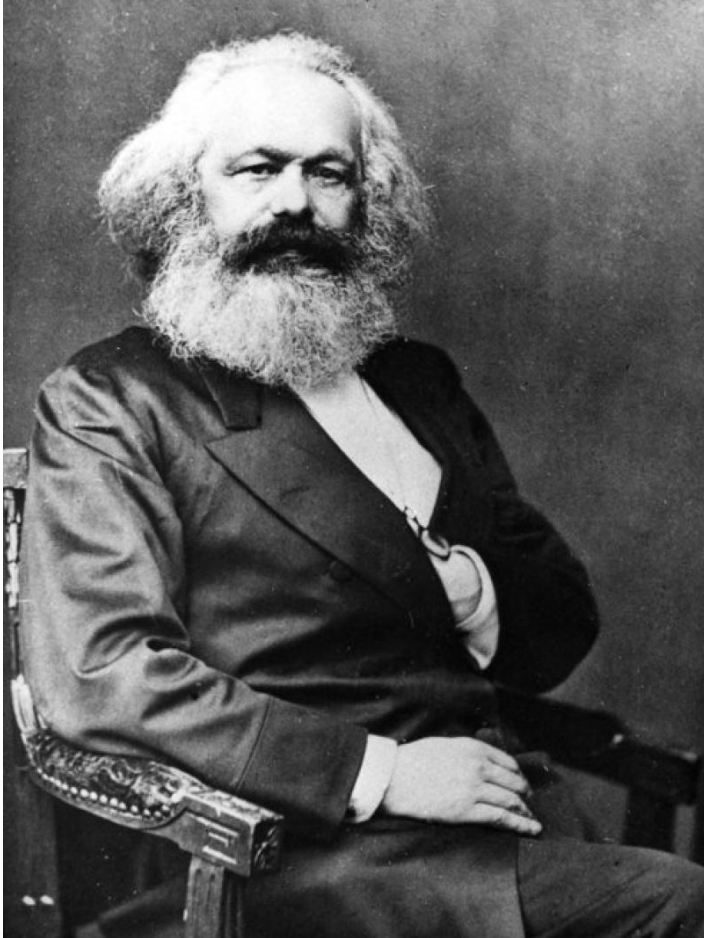
“It is not the strongest of the species that survive nor the most intelligent but the one most responsive to change.”



Charles Robert Darwin
1809 - 1882

On the origin of species (1859)

Or revolution ...



Karl Heinrich Marx
1818 - 1883

“When people speak of ideas that revolutionize society, they do but express the fact that within the old society, the elements of a new one have been created.”

Manifesto of the Communist Party (1848)

Questions to be addressed ...

Will the transition be evolutionary or revolutionary ?

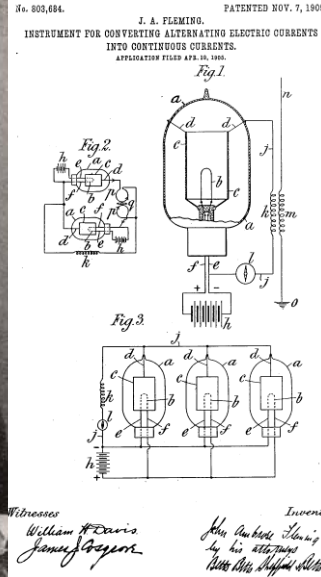
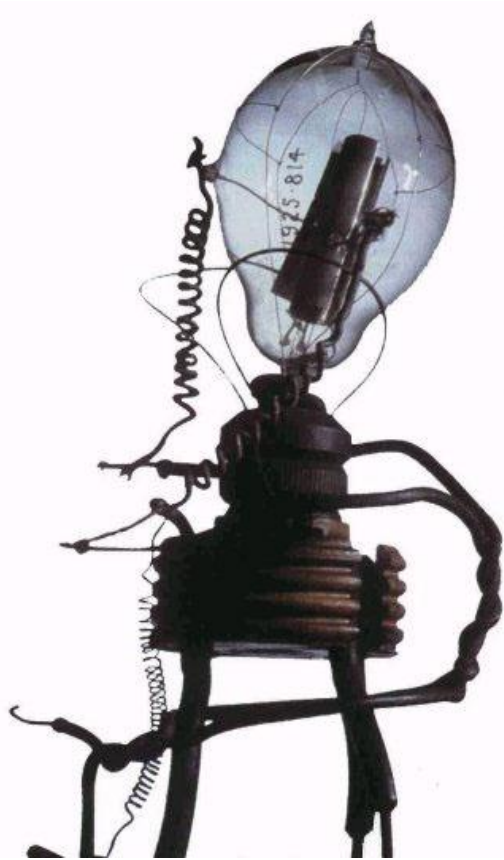
- What will the driving forces be ?
- How can simulation lead the way ?
- Could the transition be 'disruptive' ?
- Who will be the leaders, winners and losers ?



In order to answer these questions we will engage in some time travel....



History of electronics

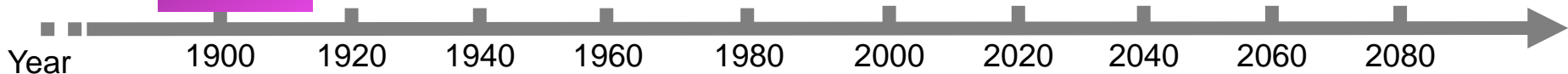


Classical physics

November 16, 1904: Sir John Ambrose Fleming invents and patents the vacuum tube

(the US Supreme Court later invalidated his US Patent claiming prior art).

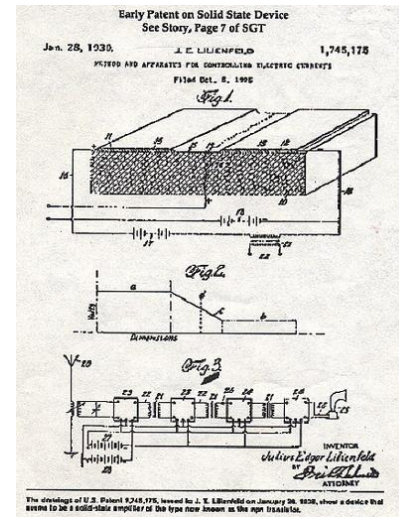
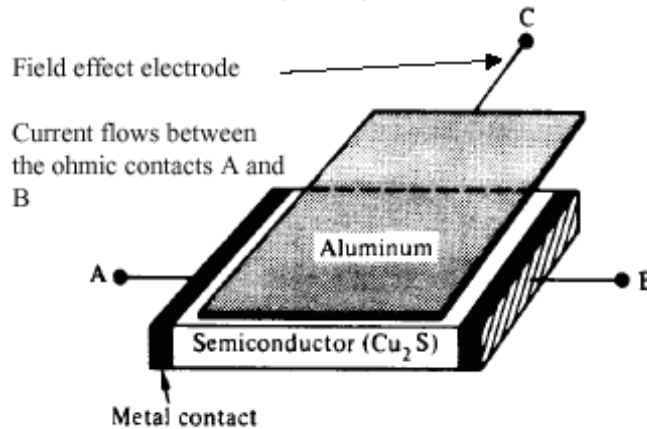
1904



History of electronics



Lilienfeld transistor (1930s)

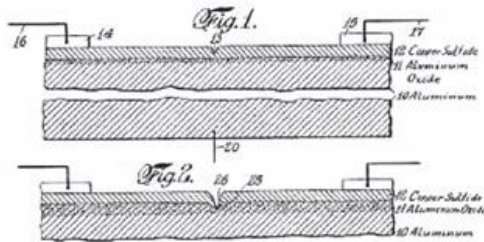


Classical physics

Solid state physics

March 7, 1933. J. E. LILIENFELD 1,900,018

DEVICES FOR CONTROLLING ELECTRIC CURRENT
Filed March 28, 1928 3 Sheets-Sheet 1

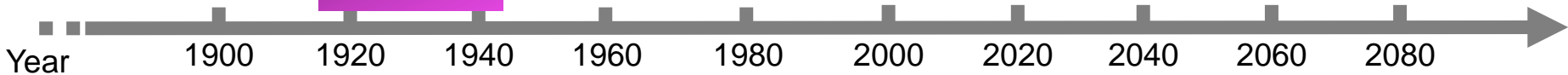


Lilienfeld FET transistor

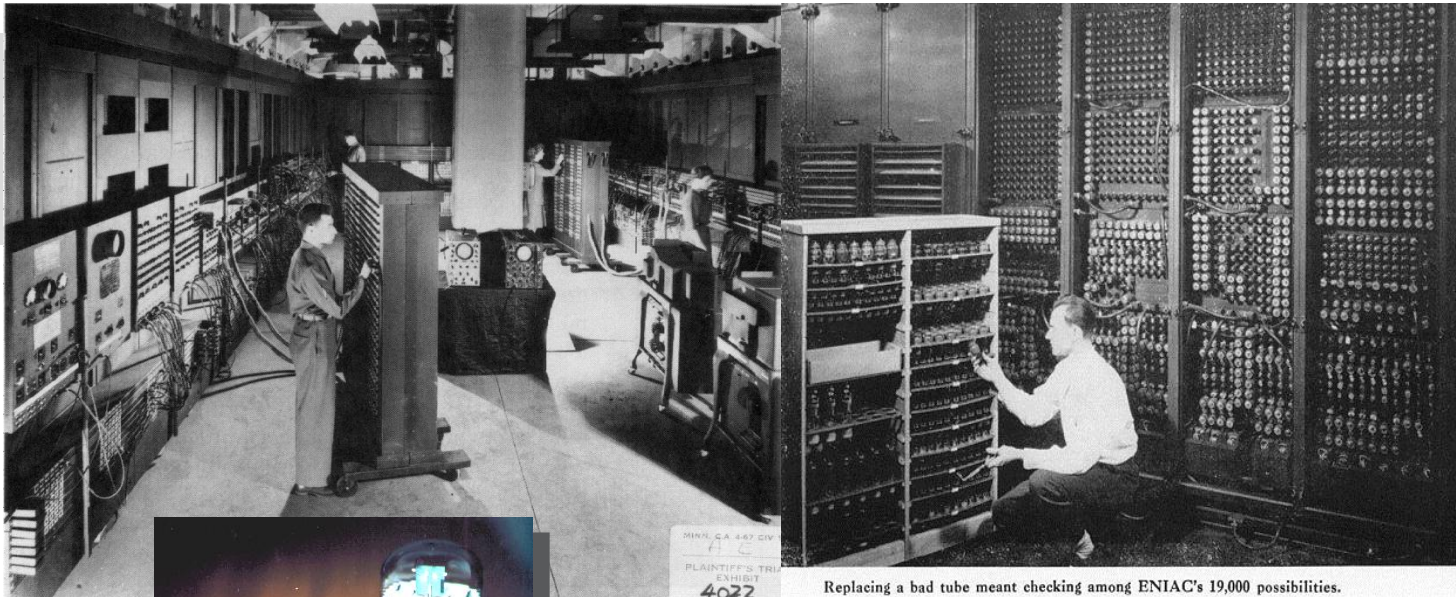
Lilienfeld could not build FET because of excessive surface states at the interface between the oxide and the semiconductor. Charges were so numerous that current flowed with zero bias.

It was only possible to turn OFF the device by driving the carriers deep (now called a “depletion mode” FET). Charges were such that only n-type semiconductors could be used.

1930's



History of electronics



Replacing a bad tube meant checking among ENIAC's 19,000 possibilities.

Classical physics



Solid state physics



ENIAC: the first electronic computer

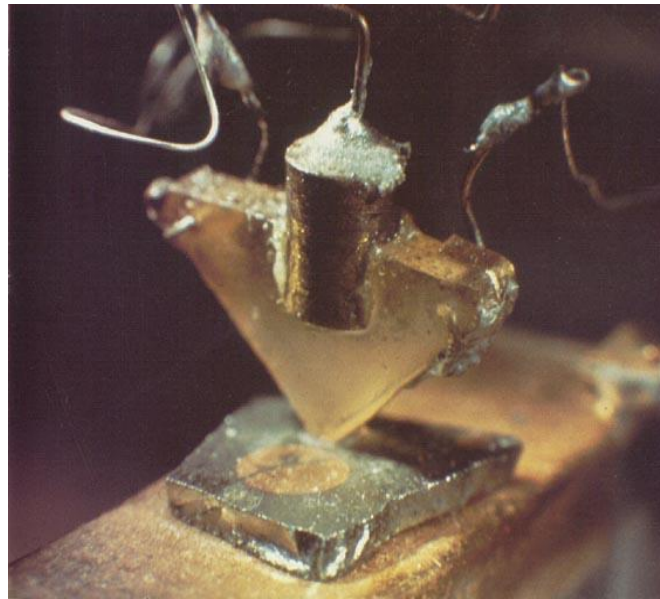
Built by John W. Mauchly (computer architecture) and J. Presper Eckert (circuit engineering), Moore School of Electrical Engineering, University of Pennsylvania. Formed Eckert & Mauchly Computer Co. and built the 2nd computer, "Univac".

1946

Went bankrupt in 1950.



History of electronics



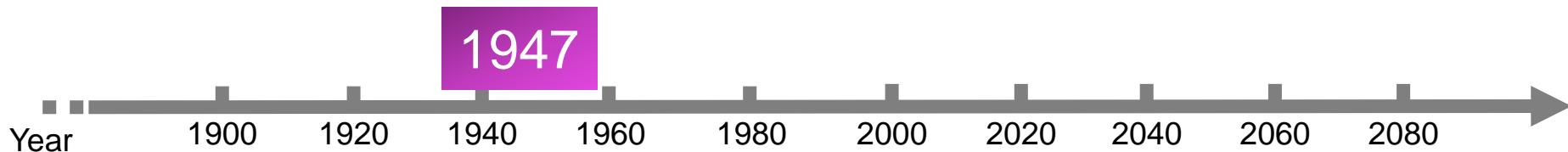
Classical physics



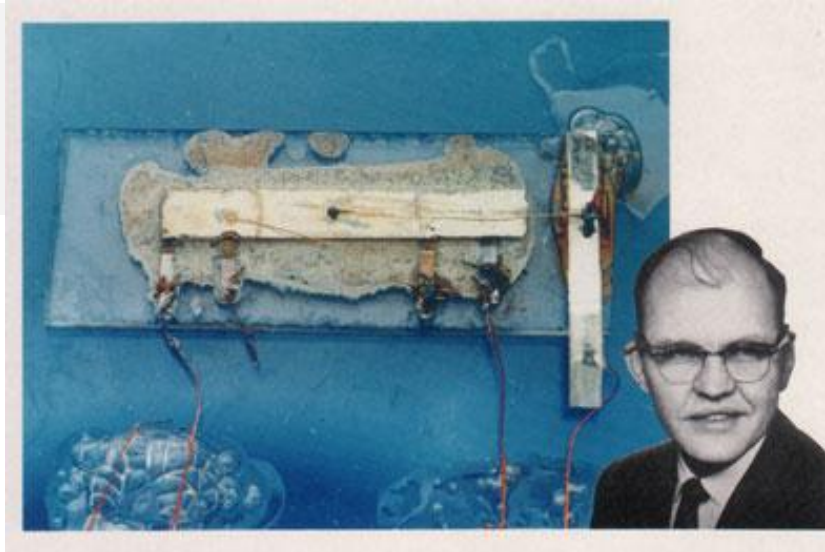
Solid state physics

The first transistor was invented at Bell Laboratories on December 16, 1947 by William Shockley, John Bardeen and Walter Brattain.

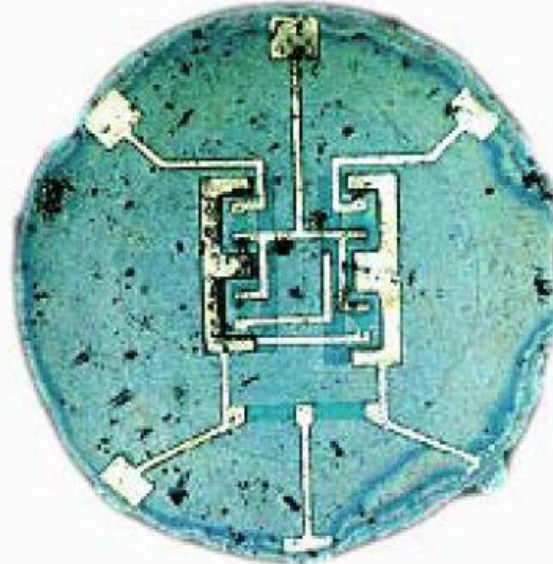
The word "transistor" comes from its ability to regulate and switch current (TRANSfer resISTOR).



History of electronics



Jack Kilby and first Germanium IC



First silicon IC chip made by Robert Noyce of Fairchild in 1961

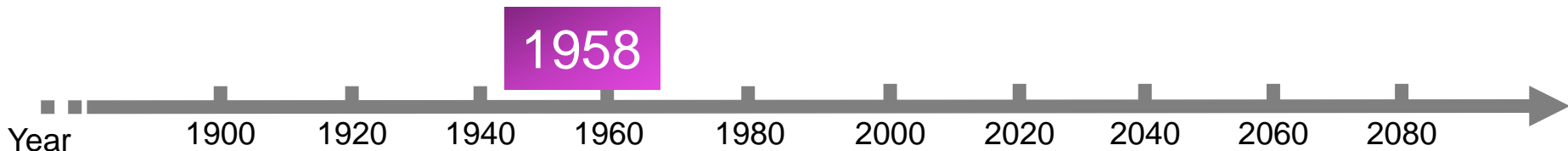
Classical physics



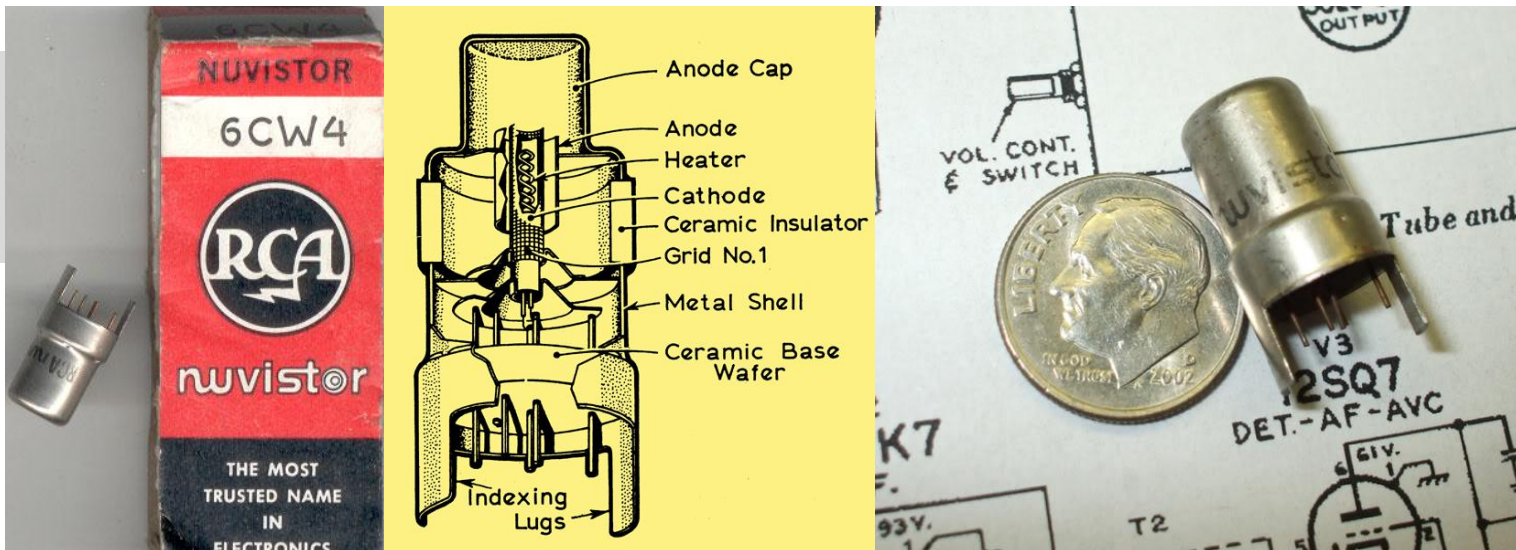
Solid state physics

Invention of the integrated circuit

In 1958 and 1959, Jack Kilby at Texas Instruments and Robert Noyce at Fairchild Camera, came up with a solution to the problem of large numbers of components, and the integrated circuit was developed.



History of electronics



Classical physics

Solid state physics

Nuvistors

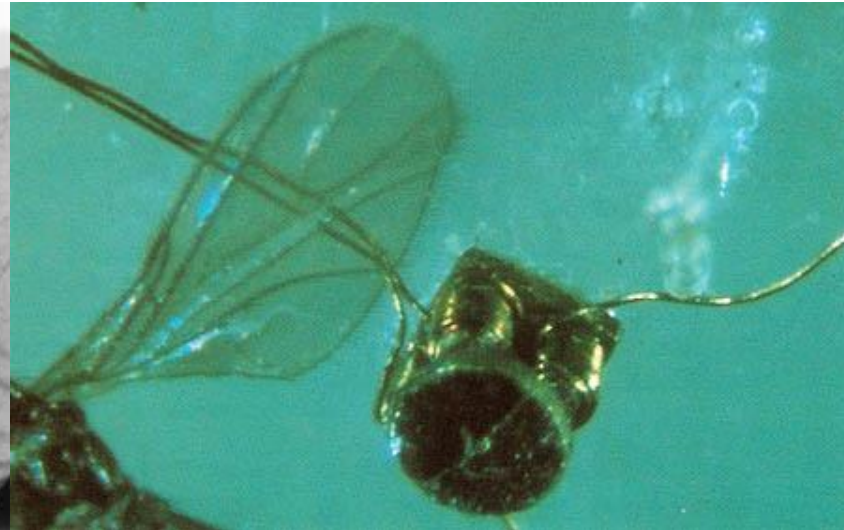
RCA's (1959) introduction of the Nuvistor vacuum tube, heralded one of the attempts of tube manufacturers to hold onto a major portion of the small-signal amplification market.

The Nuvistor is a thimble-sized vacuum tube (enclosed in miniature metal rather than glass) that promised high-reliability, low-noise, and low-power operation.

1959



History of electronics



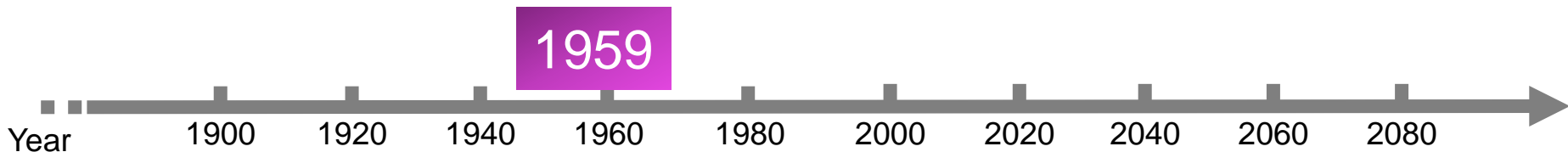
Classical physics



Solid state physics

First nano award

In 1959, when Richard Feynman suggested the possibility of building structures one atom or molecule at a time, the idea seemed fantastic. Feynman offered a \$1,000 prize to the first person who could make a working electric motor that would fit inside a cube that measured $1/64$ of an inch on each side. He guessed it would be a long time before he had to pay up. But just two and a half months later, William McLellan, a physicist at the University of California Institute of Science and Technology, claimed the prize. Working on his lunch breaks with a microscope, toothpick, and watchmaker's lathe, McLellan assembled a motor that met Feynman's requirements.



History of electronics



IBM-PC Model 5100 (1975)



IBM-PC Model 5150 (1981)

Classical physics



Solid state physics

Release of the first IBM PC in 1975

The Model 5100 used a proprietary IBM processor called the PALM (for Put All Logic in Microcode). The 5100 shipped with 16K to 64K of memory, used a tape drive for program storage, and depending on configuration the machine sold for \$8,975 to \$19,975.

1975



History of electronics

Electric Field Effect in Atomically Thin Carbon Films

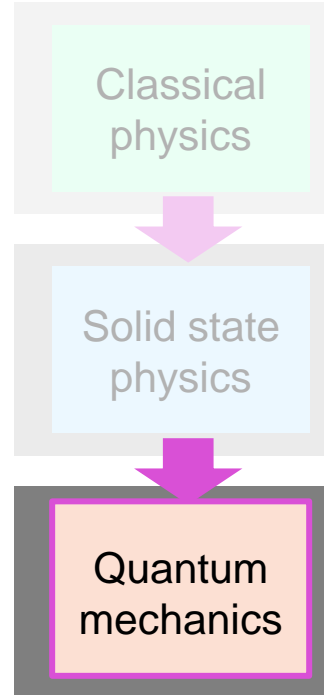
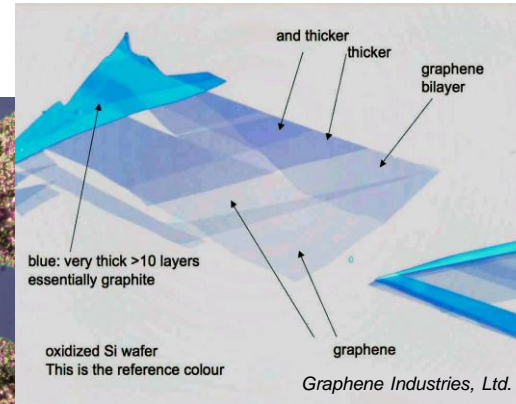
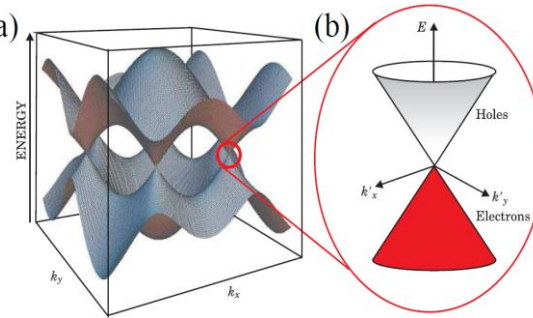
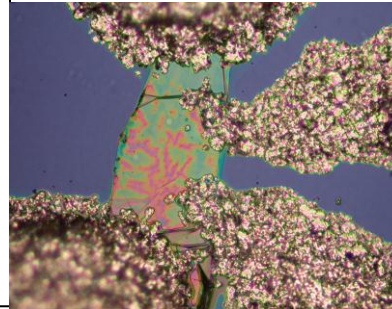
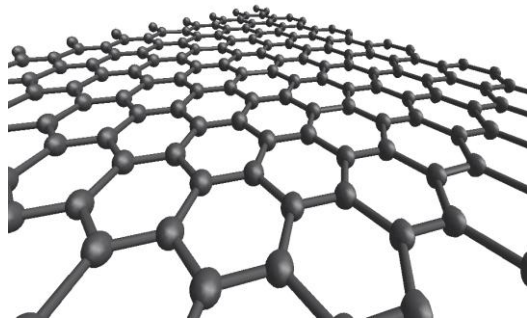
K. S. Novoselov,¹ A. K. Geim,^{1*} S. V. Morozov,² D. Jiang,¹ Y. Zhang,¹ S. V. Dubonos,² I. V. Grigorieva,¹ A. A. Firsov²

We describe monocrystalline graphitic films, which are a few atoms thick but are nonetheless stable under ambient conditions, metallic, and of remarkably high quality. The films are found to be a two-dimensional semimetal with a tiny overlap between valence and conduction bands, and they exhibit a strong ambipolar electric field effect such that electrons and holes in concentrations up to 10^{13} per square centimeter and with room-temperature mobilities of $\sim 10,000$ square centimeters per volt-second can be induced by applying gate voltage.

The Nobel Prize in Physics 2010
Andre Geim, Konstantin Novoselov
The Nobel Prize in Physics 2010
Andre Geim
Konstantin Novoselov



Photo: Sergeom, Wikimedia Commons
Andre Geim
Photo: University of Manchester, UK
Konstantin Novoselov



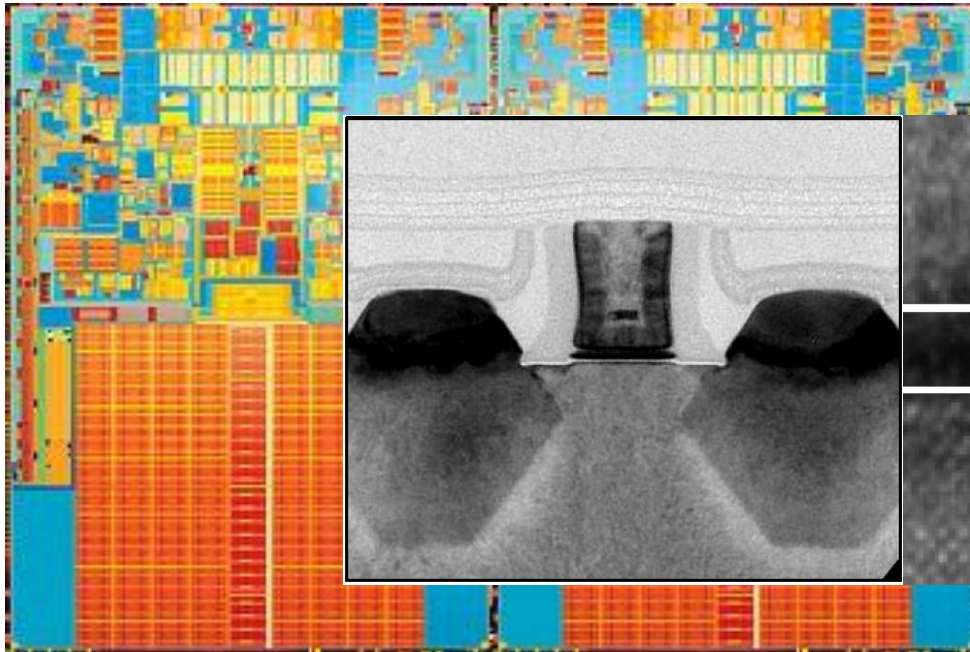
“Discovery” of graphene.....

The Nobel Prize in Physics 2010 was awarded jointly to Andre Geim and Konstantin Novoselov “for groundbreaking experiments regarding the two-dimensional material graphene”

2004



History of electronics



Core 2 Quad processor, $\sim 8 \times 10^8$ transistors

Introduction of high-k/metal gates by INTEL

Intel processors (45 nm technology node) integrate high-*k*/metal gates stacks, allowing improved performances and reduced power consumption.

Classical physics

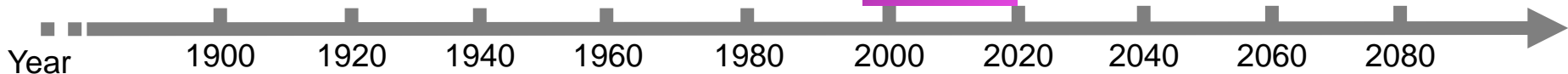


Solid state physics

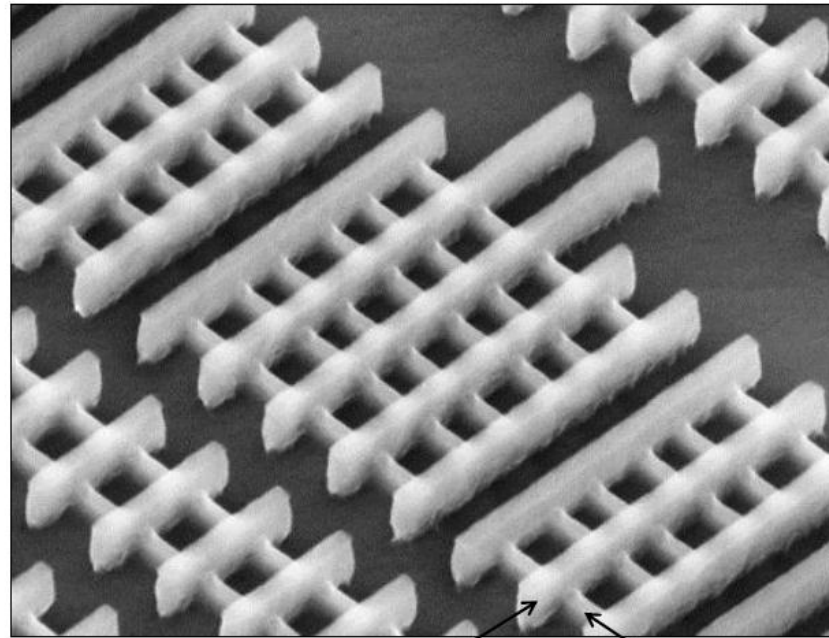
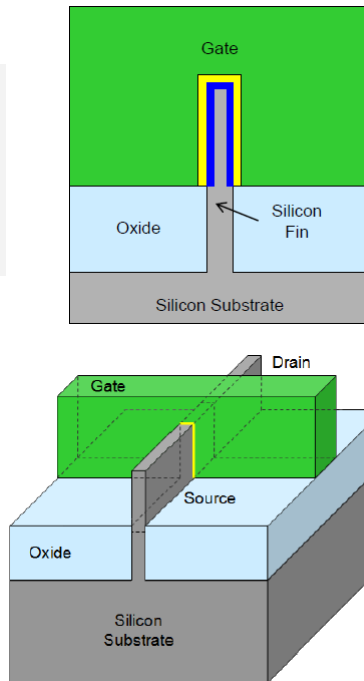


Quantum mechanics

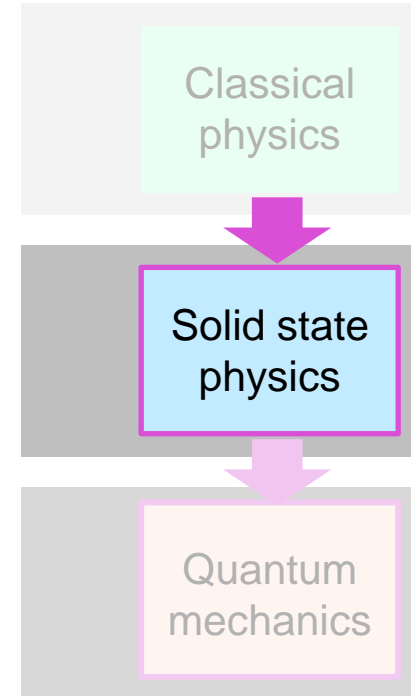
2007



State-of-the art

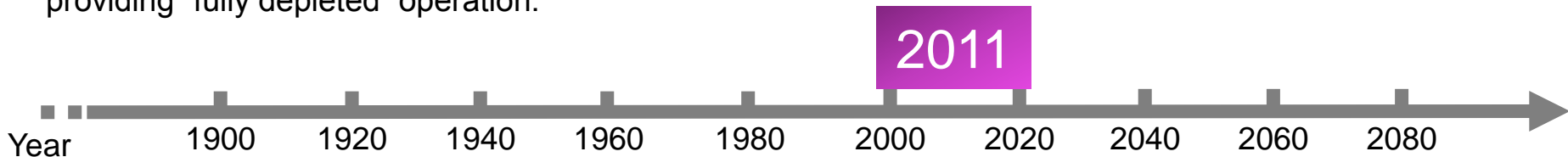


Gates Fins

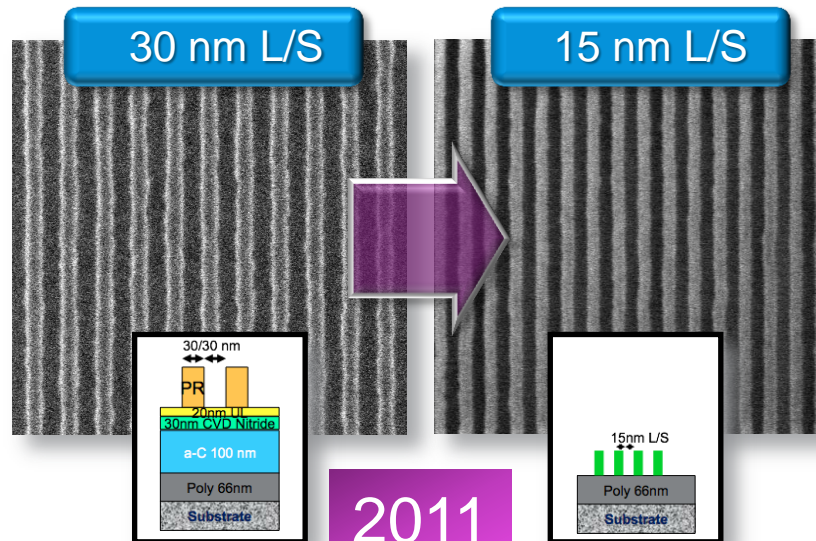
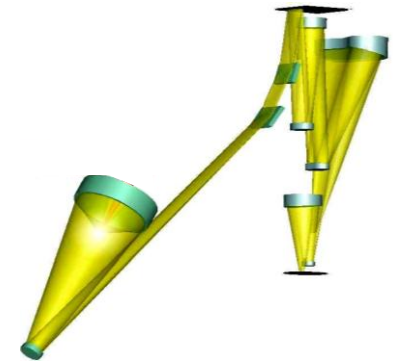
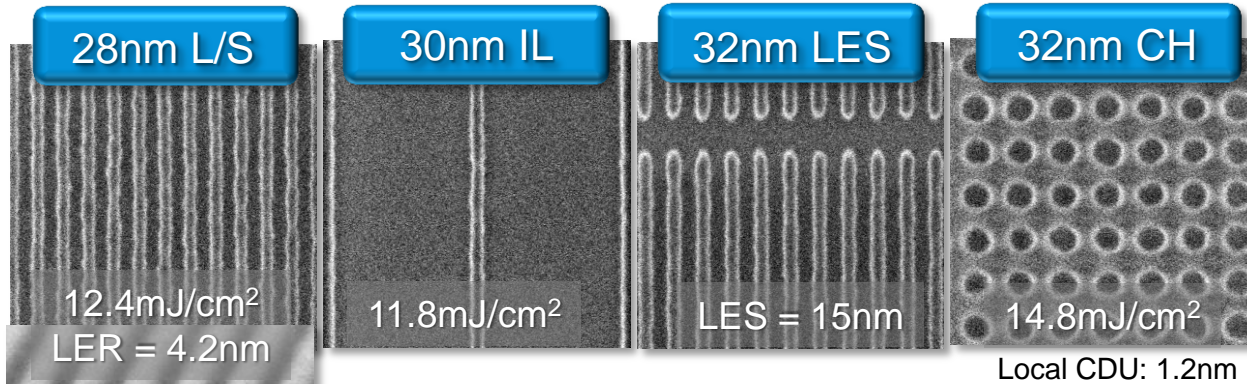


INTEL introduces FinFETs in the 22 nm technology

3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing “fully depleted” operation.



State-of-the art: EUV litho performance



EUV extendability:
self-aligned
double
patterning

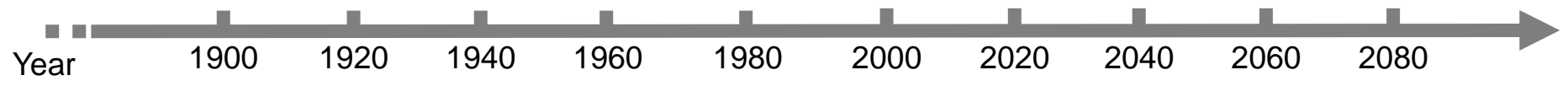




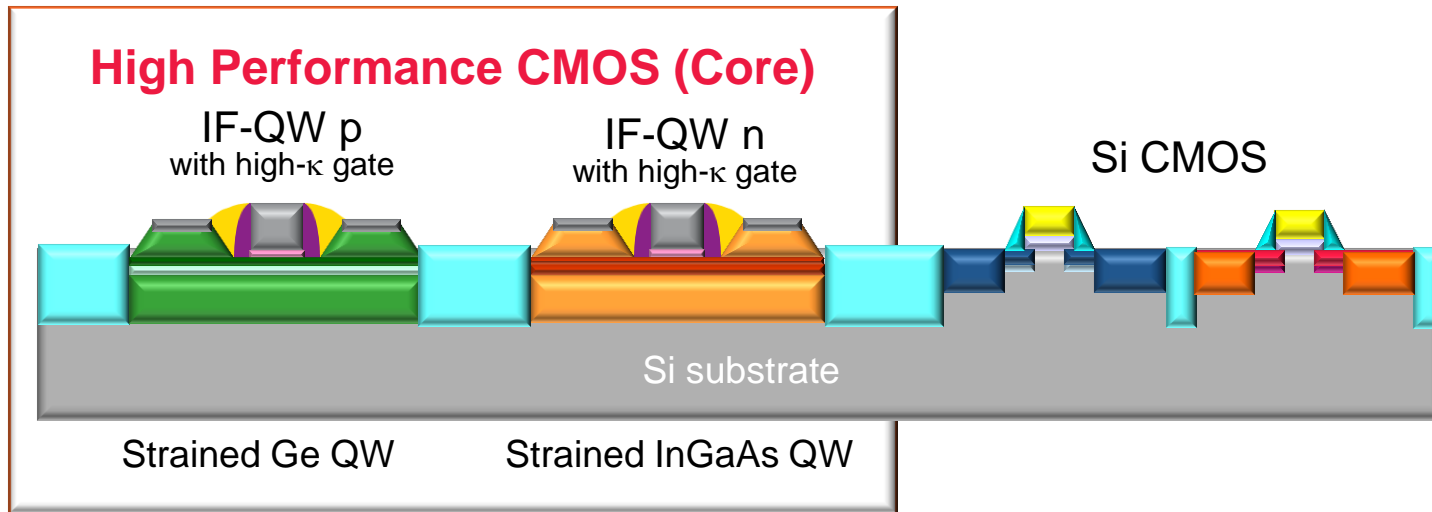
Classical physics

Solid state physics

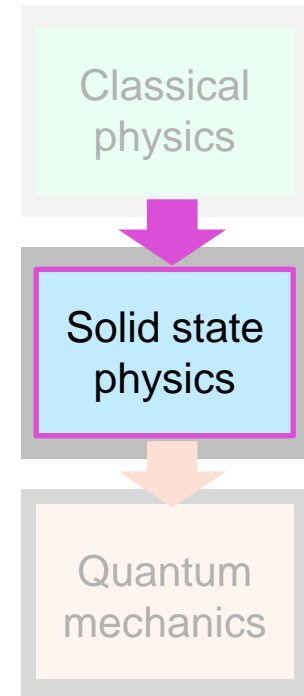
Quantum mechanics



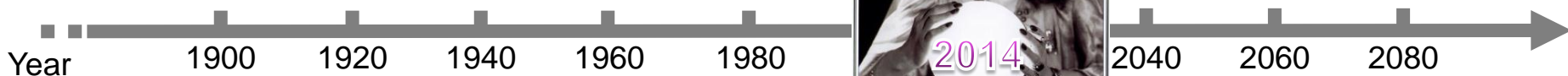
A look into the future.....



1. **Selective growth** of Ge and/or III/V in STI trenches
2. **High- κ gate stack** for low EOT
3. **IF-QW device** with self-aligned **doped raised S/D** for contacts
4. Further **strain engineering** for mobility boost

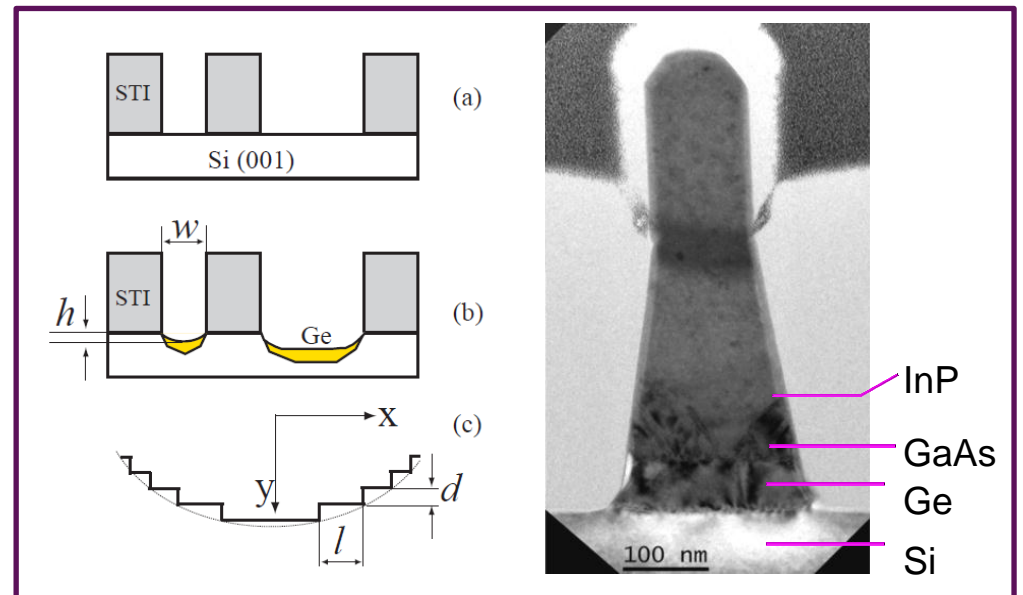
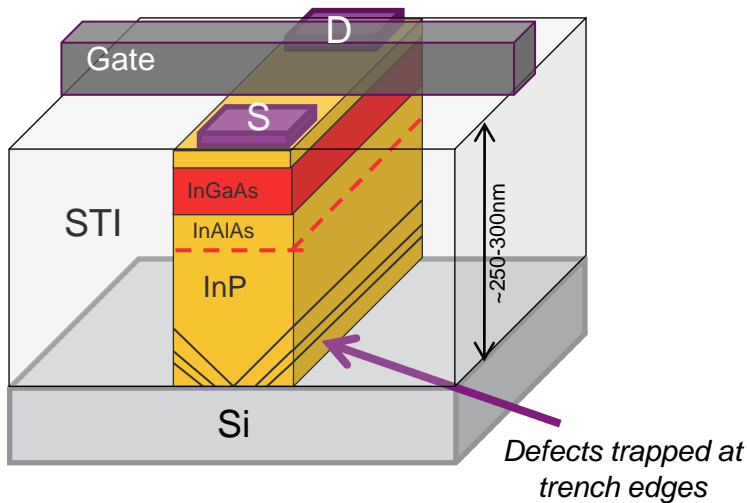
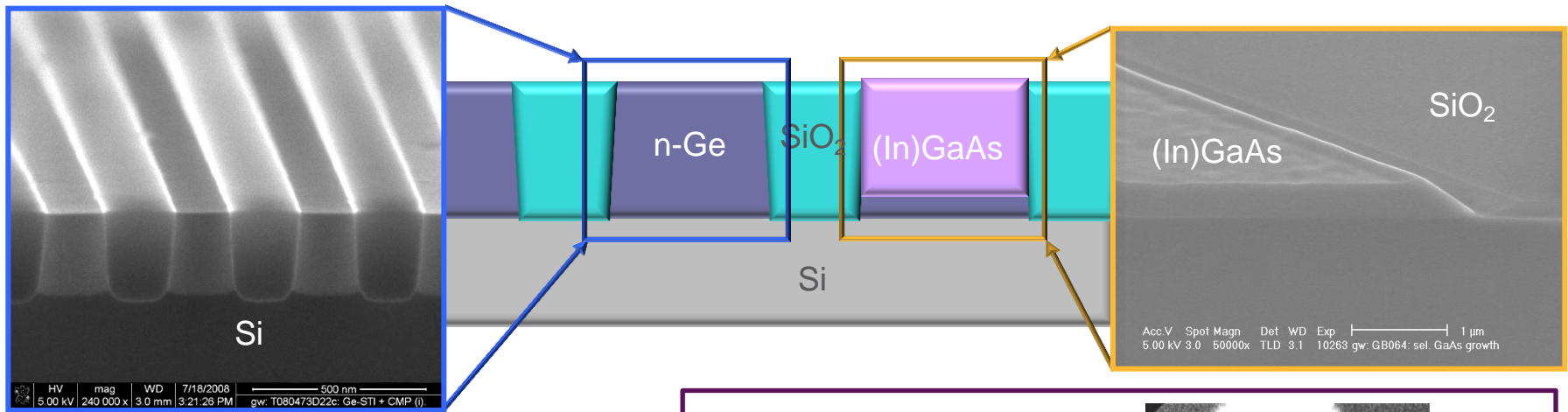


First non-Si based CMOS announced
Ge pMOS and III/V (InGaAs) nMOS



Ge and III/V selective growth on Si wafers

- ▶ Local selective growth after STI allows integration of Ge and III/V materials on Si wafers, also for FinFETs.



Ge and III/V CMOS by wafer bonding

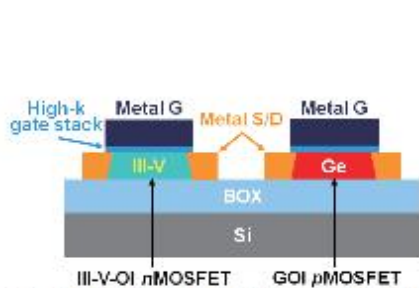


Fig. 1 Ultimate CMOS transistors with III-V nMOSFETs and Ge pMOSFETs on Si substrates with BOX layer.

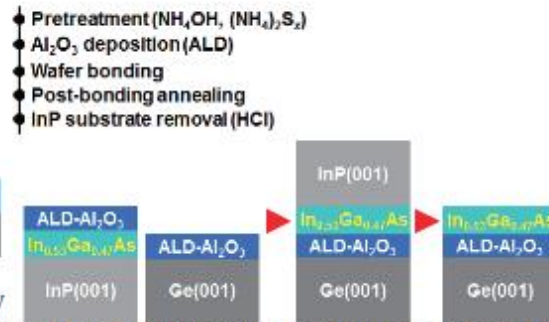


Fig. 2 Process flow for fabricating InGaAs-on-Ge wafers using the ALD- Al_2O_3 DWB technique.

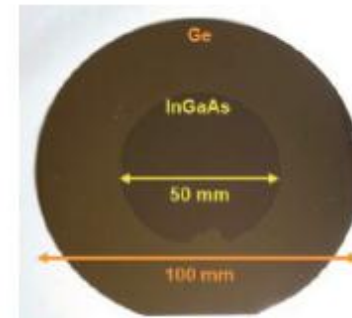


Fig. 3 Photograph of an InGaAs-on-Ge wafer. A 2-inch InGaAs layer integrated on a 4-inch Ge wafer with an Al_2O_3 BOX layer.

- Pretreatment (NH_4OH , $(\text{NH}_4)_2\text{S}_x$)
- Al_2O_3 deposition (ALD)
- Al_2O_3 etching (BHF)
- InGaAs layer isolation (HCl:H₂O₂:H₂O)
- Ta sputtering
- Gate etching (RIE)
- Post metal annealing at 350 °C
- Al_2O_3 etching (BHF)
- Ni sputtering
- Ni-InGaAs and Ni-Ge source/drain formation by annealed in N_2 ambient at 250 °C
- Unreacted Ni selective etching (HCl)

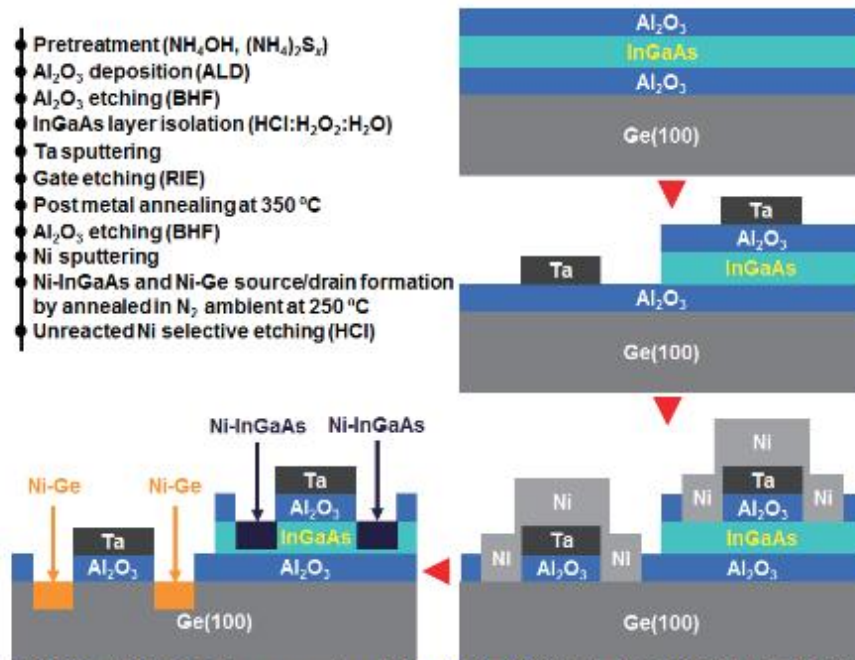


Fig. 4 III-V/Ge CMOS fabrication process flow of InGaAs-OI nMOSFETs and Ge pMOSFETs with Ni-based metal S/D on an InGaAs-on-Ge wafer.

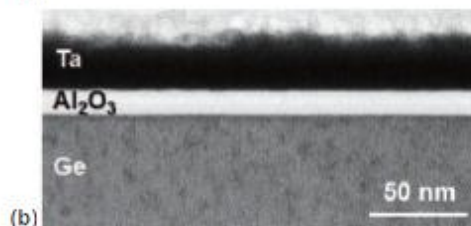
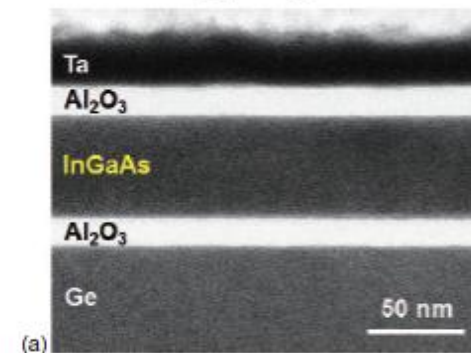
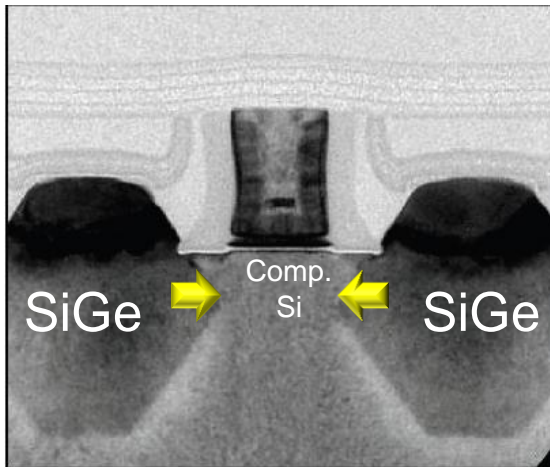


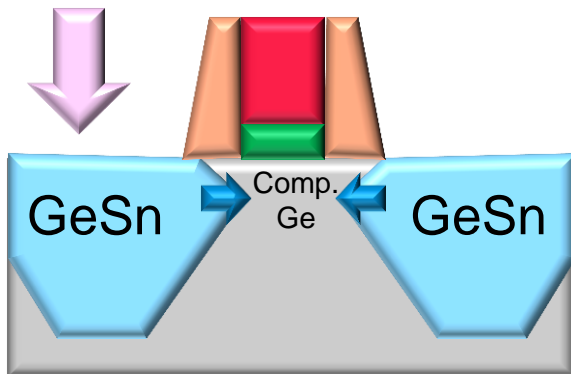
Fig. 5 Cross-sectional TEM image of the MOS interfaces of (a) 50-nm-thick InGaAs-OI nMOSFET and (b) of Ge pMOSFET with Ta/ Al_2O_3 metal-gate/high-k gate-stack.

Introducing strain in Ge devices

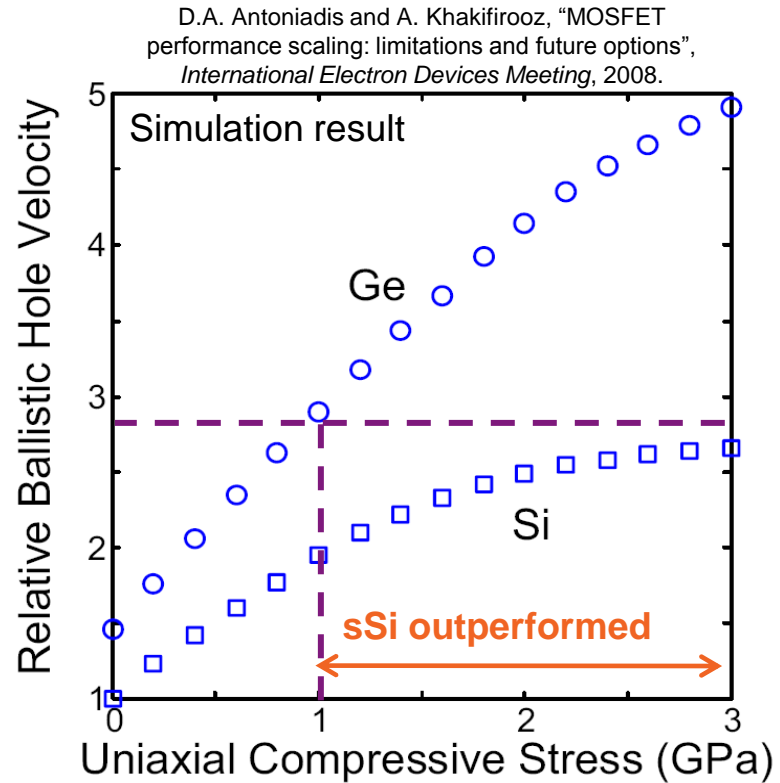
Compressively strained Ge is mandatory to outperform sSi pMOSFETS
 Transfer sSi technologies to compressively strained Ge channels using GeSn



45nm compressive Si pMOSFET from INTEL

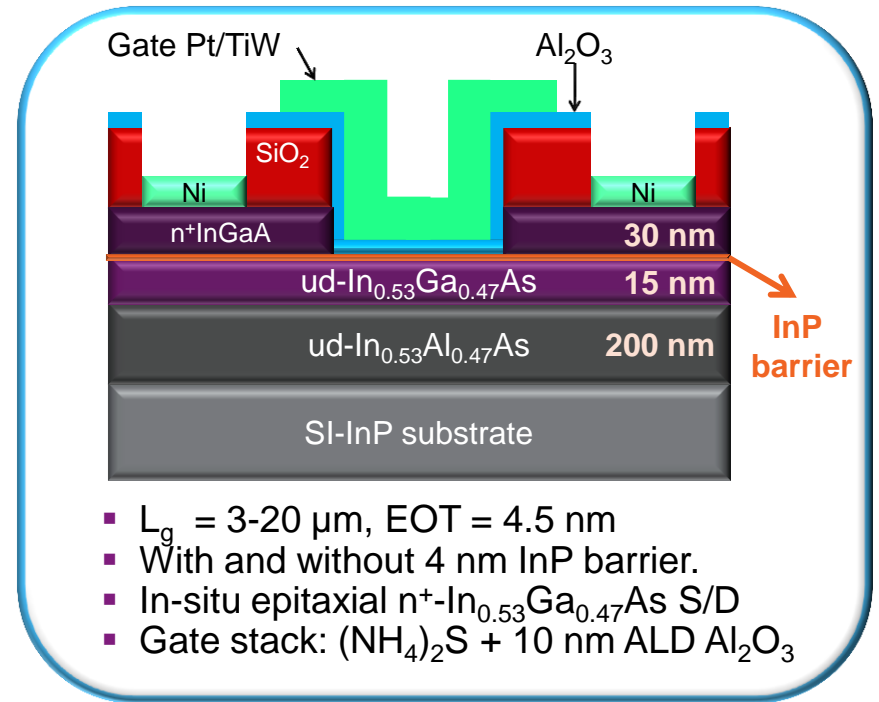
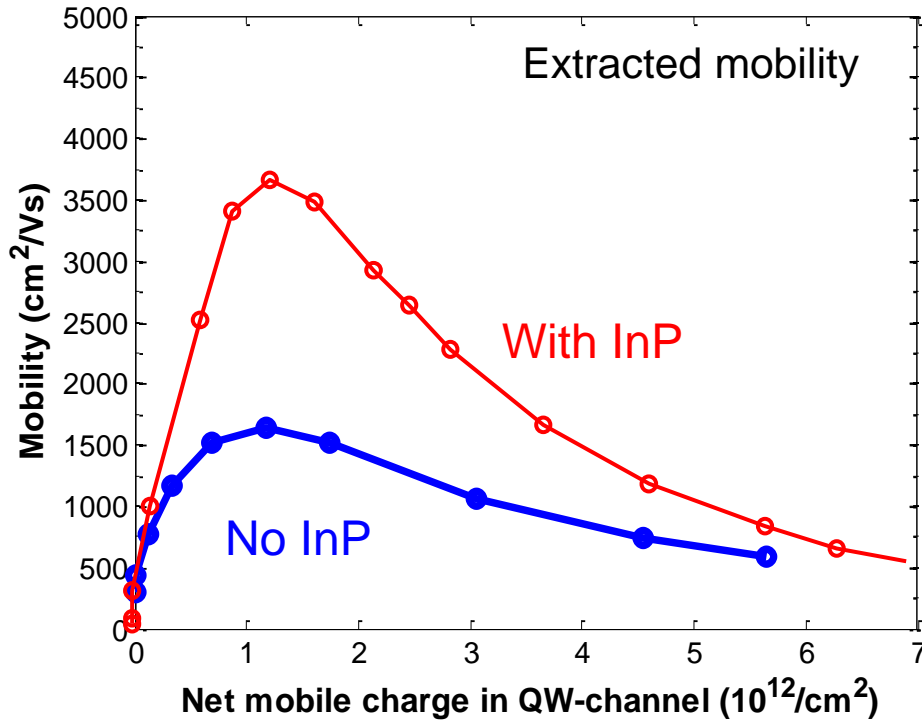


New compressively strained Ge MOSFET architecture

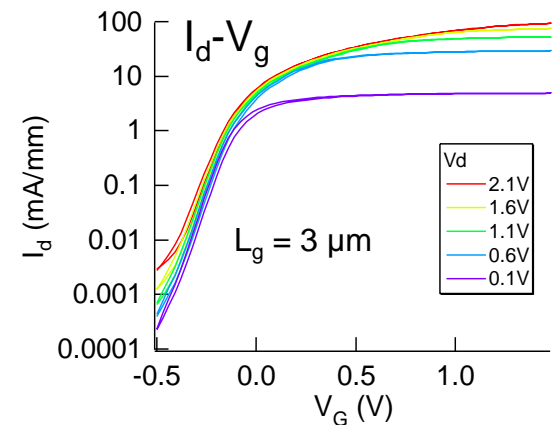


1GPa is requested in Ge channels to outperform sSi hole mobilities

Implant Free Quantum Well (IFQW) device



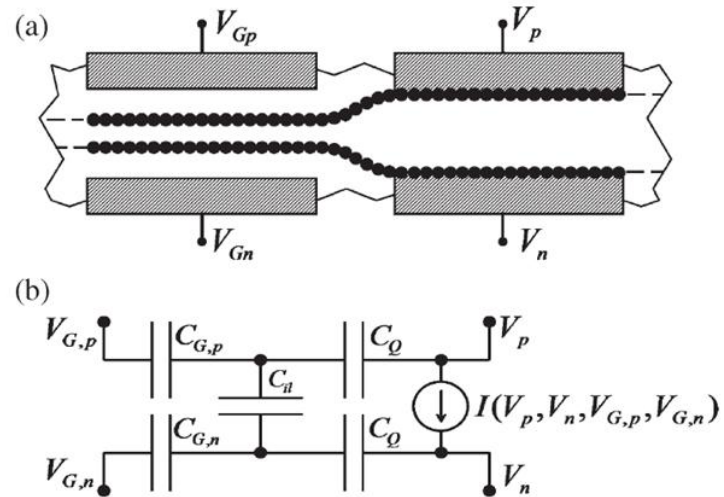
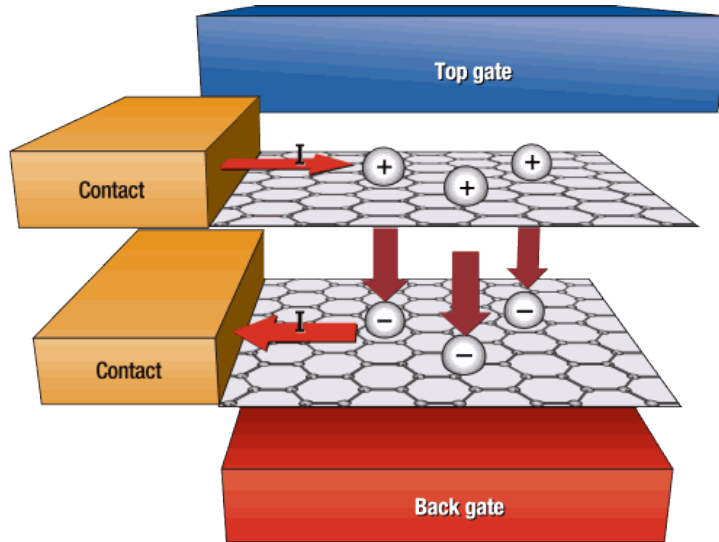
- Good I_{on}/I_{off} ratio of ~10⁵
- Sub-threshold slope ~ 100 mV/dec
- Low hysteresis (if not biased into deep depletion)
- Extrinsic currents limited by R_s of 15 Ω.mm
 - due to 20 μm spacing between S/D metal and gate



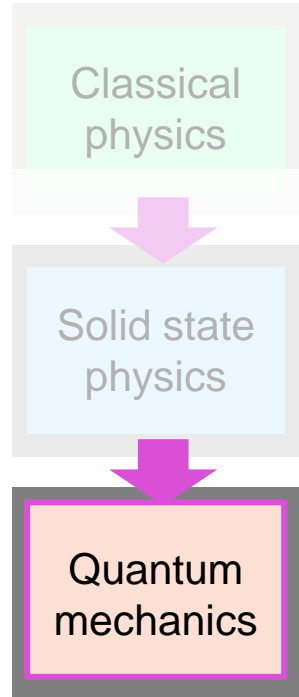
A look into the future.....

Theory predicts that the ground state of a suitable graphene bilayer may be an above-room-temperature Bose-Einstein condensate corresponding to a coherent superposition of excitons.

A logic device based on such a superfluid condensate of excitons is the bilayer pseudospin FET (BiSFET), which controls the presence or absence of the condensate via applied gate voltages.



S.K. Banerjee et al, IEEE ELECTRON DEVICE LETTERS, VOL. 30, NO. 2, 158, FEBRUARY 2009

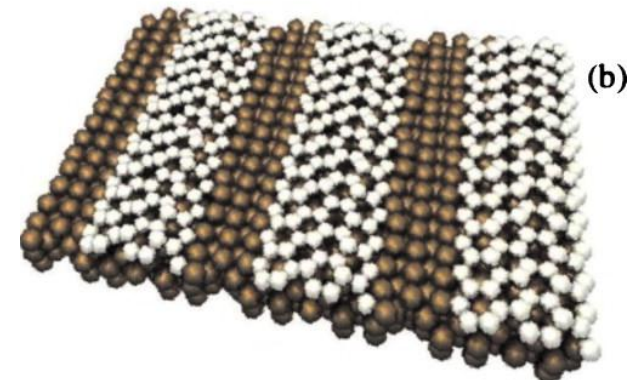
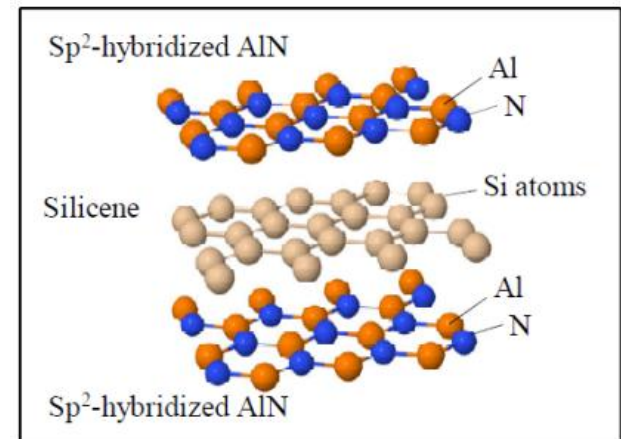
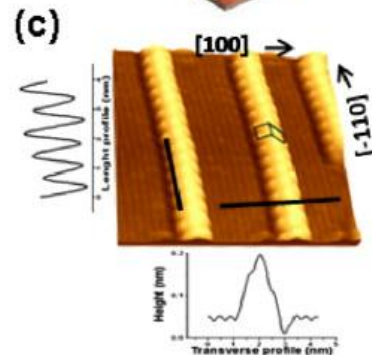
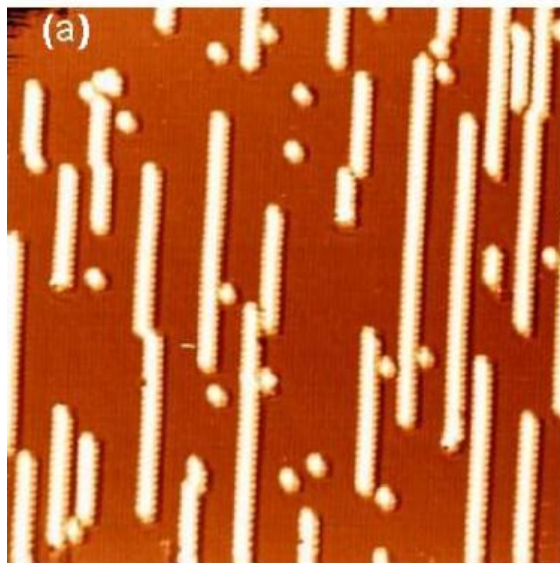


First demonstration of new devices based on 2D materials (i.e. graphene)



Other 2-D materials: Silicene

- ▶ Silicene is the Si equivalent of graphene.
- ▶ Promising results have been obtained on silicene nanoribbon fabrication on Ag surfaces.
- ▶ Can also be made on AlN



STM images of straight, parallel 1D silicon nanostructures grown on a Ag(110) surface. (a) Large view (42×42 nm², filled states); (b) 3D view (12×12 nm², filled states); and (c) detailed view (6.22×6.22 nm², filled states).

Filled-states STM image, 11×10 nm² ($V = -3.3$ V, $I = 1.90$ nA) of the dense array of SiNRs forming a 1D grating with a pitch of ~ 2 nm (a); ball model of the corresponding calculated atomic structure (b).

3D Topological insulators

ARTICLES

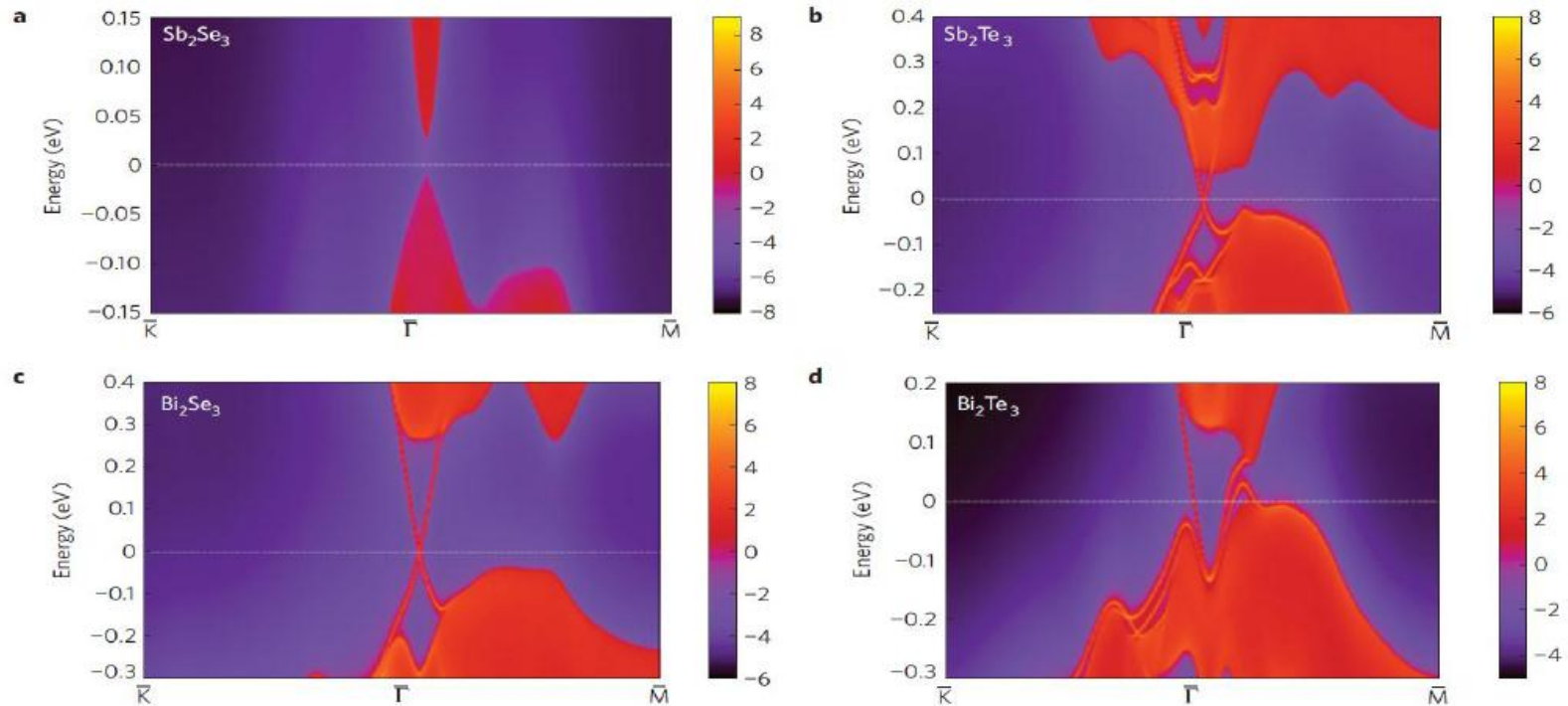
PUBLISHED ONLINE: 10 MAY 2009 | DOI:10.1038/NPHYS1270

nature
physics

Topological insulators in Bi_2Se_3 , Bi_2Te_3 and Sb_2Te_3 with a single Dirac cone on the surface

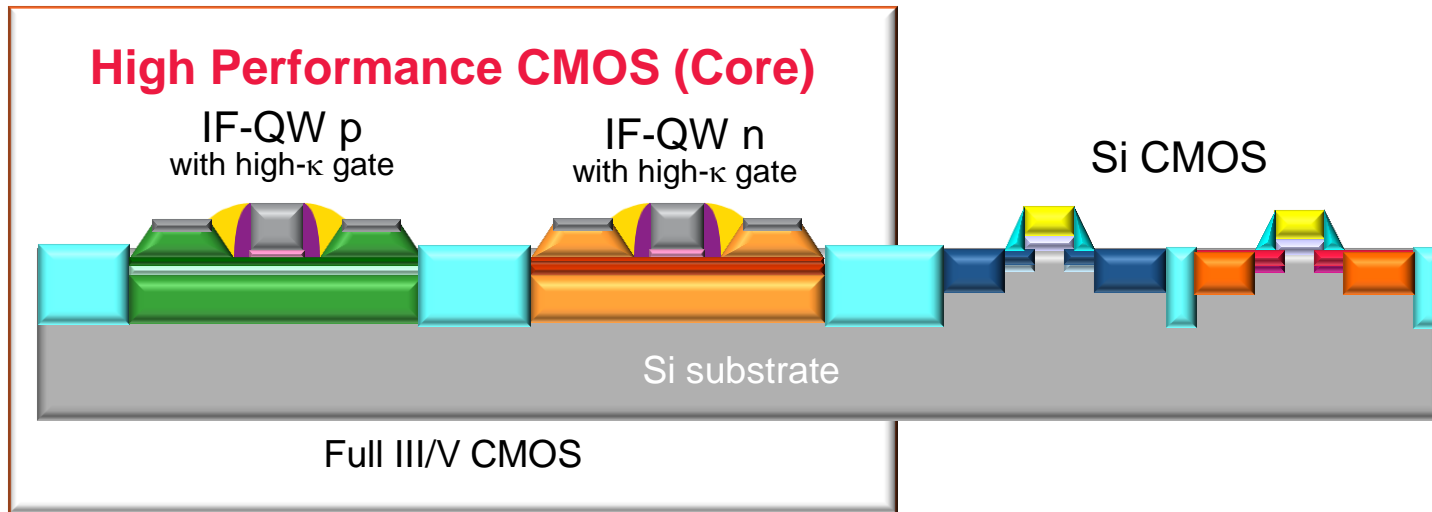
Haijun Zhang¹, Chao-Xing Liu², Xiao-Liang Qi³, Xi Dai¹, Zhong Fang¹ and Shou-Cheng Zhang^{3*}

Energy and momentum dependence of the LDOS



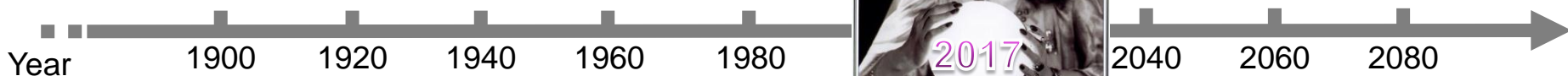
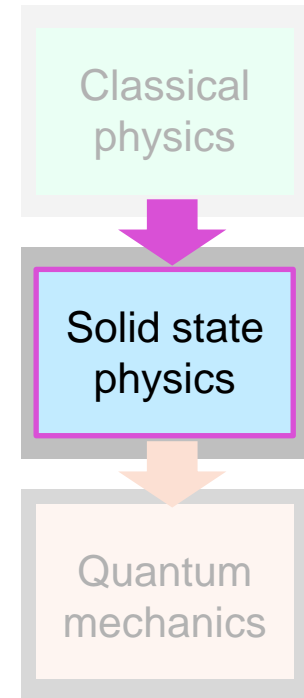
Sb_2Se_3 has no surface state

A look into the future.....



1. **Selective growth** of III/V in STI trenches
2. **High hole mobility materials** for pMOS
3. **IF-QW device**
4. Further **strain engineering** for mobility boost

Full III/V CMOS with reduced supply voltage
(small bandgap materials)



III/V pFET

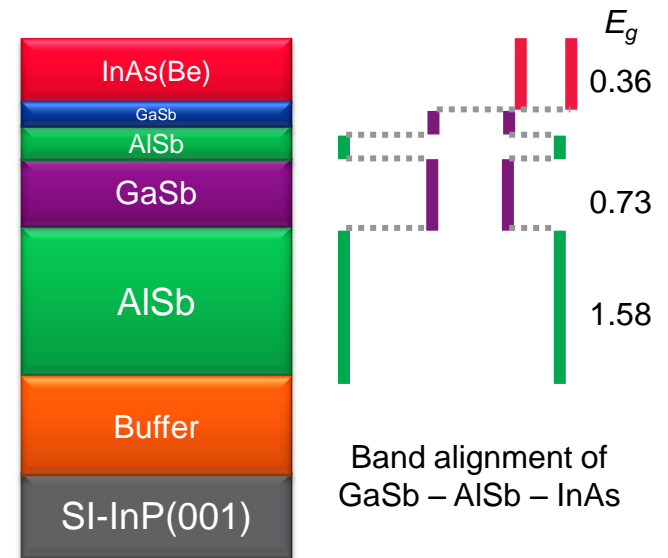
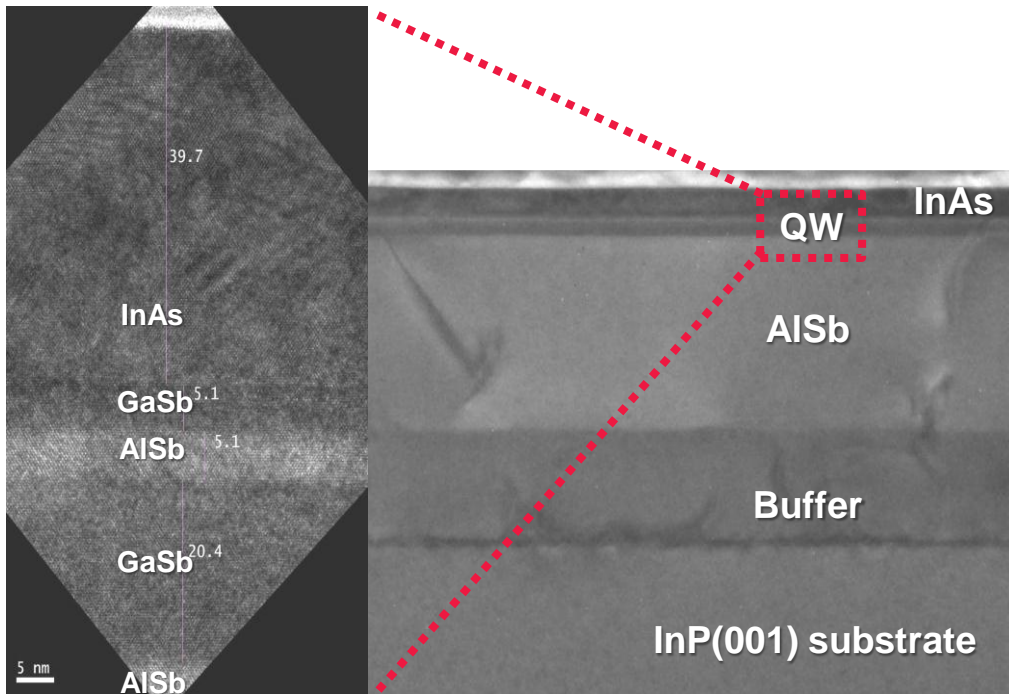
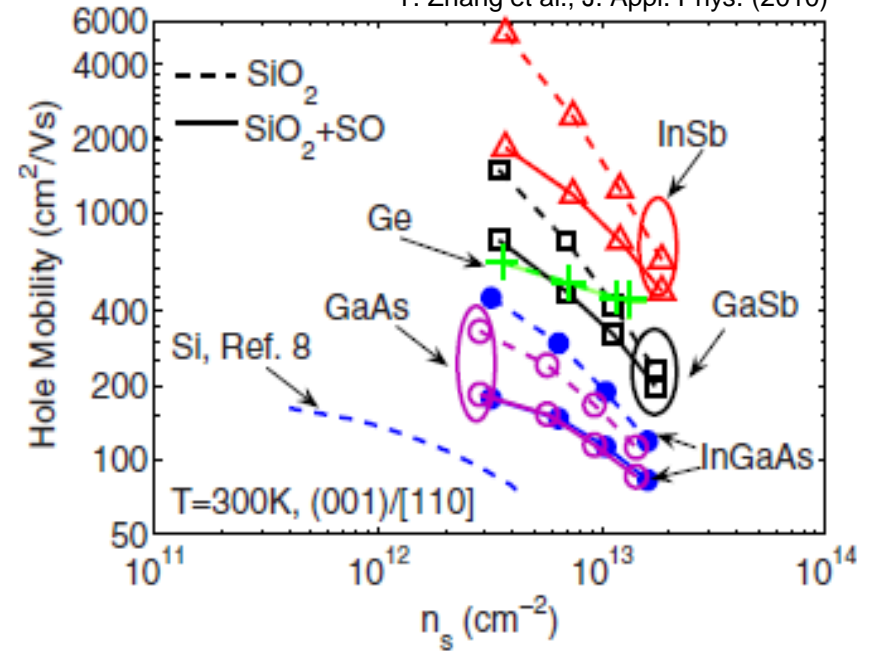
High hole mobility for III-Sb p-channel

InSb followed by GaSb has the largest hole mobility compared to Ge, InGaAs and GaAs

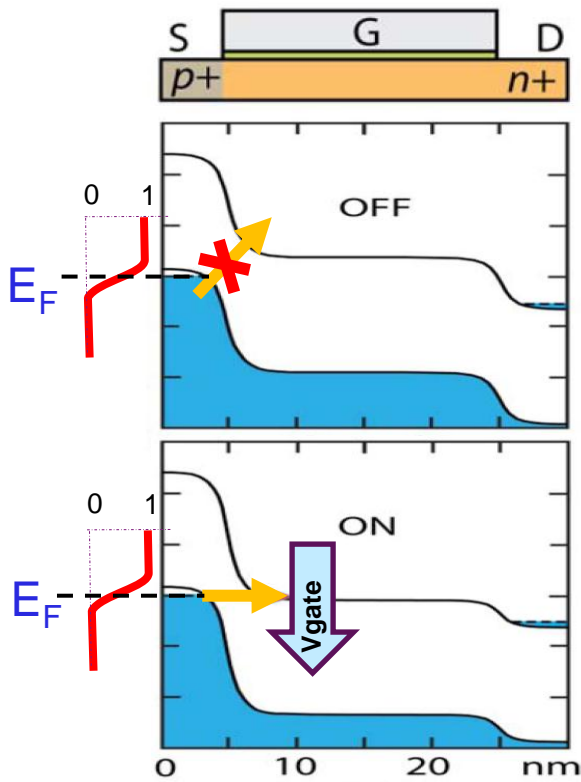
Optimized structural stack quality

The **AISb interfacial layer** plays a key role in the growth of high quality QW stack

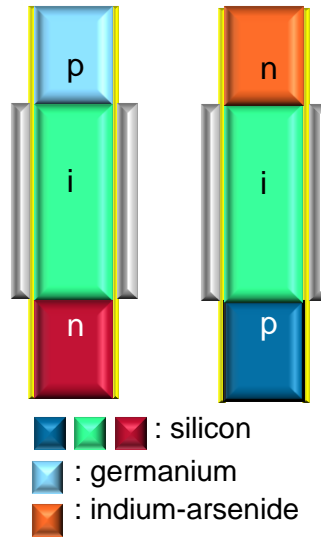
Y. Zhang et al., J. Appl. Phys. (2010)



A look into the future.....

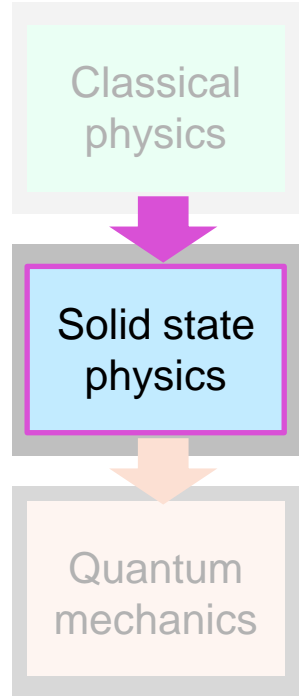
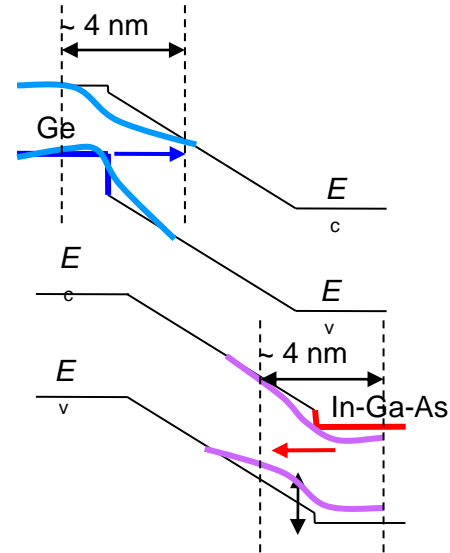


Ge-source n-TFET InAs-source (In_{0.6}Ga_{0.4}As) p-TFET

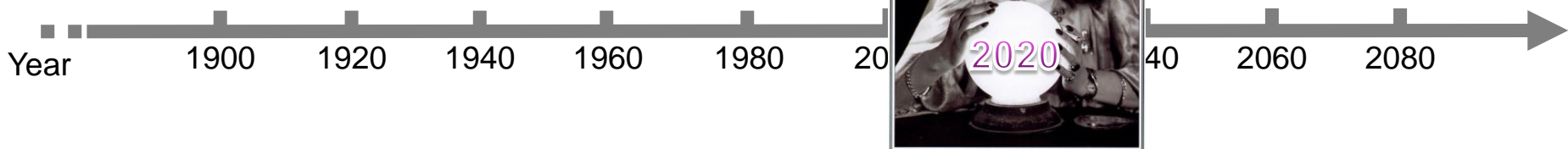


Heterojunction TFET boosts the ON current by increasing the source tunneling efficiency by using low bandgap material in the source

HTFET schematic view

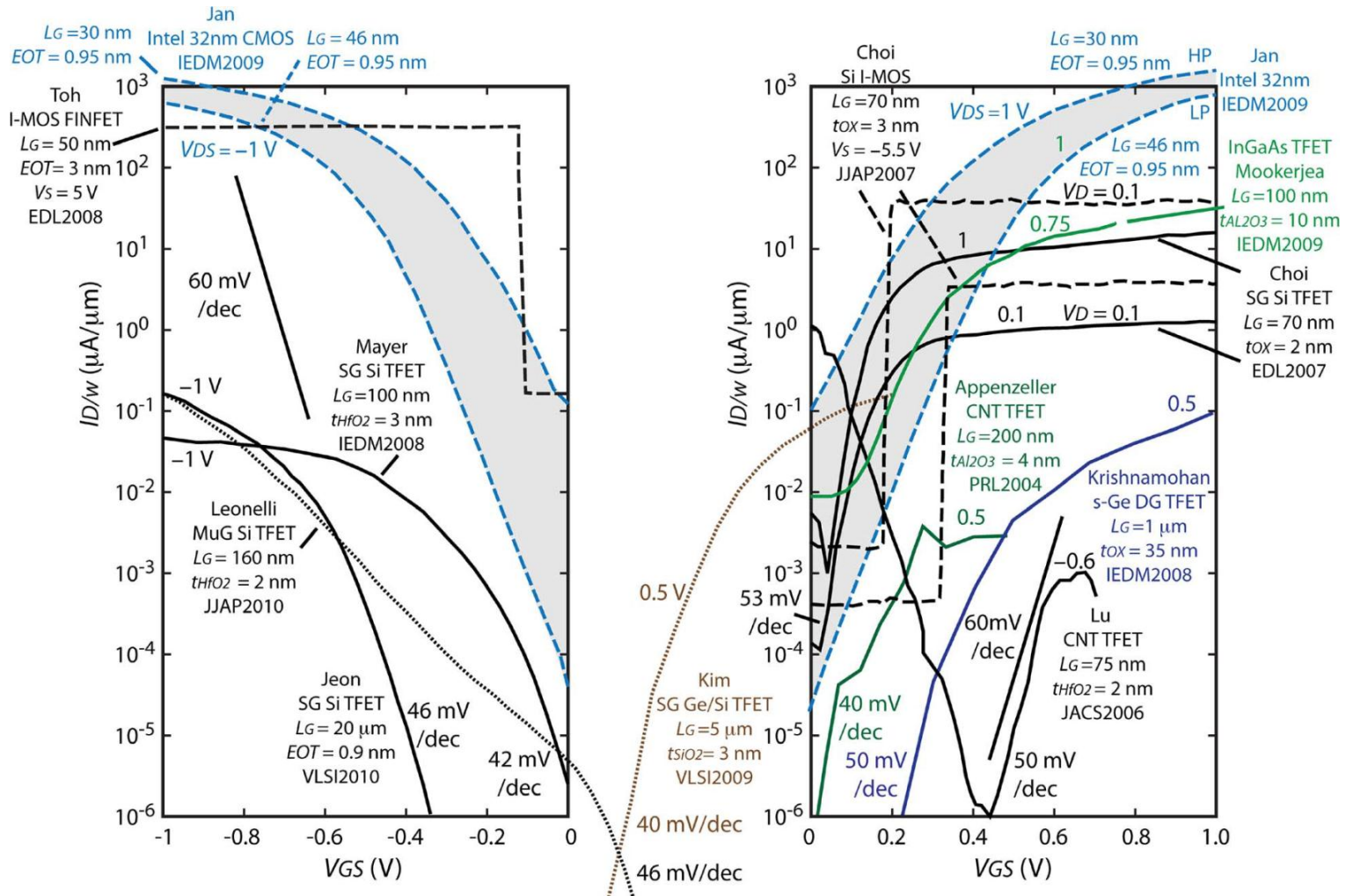


Introduction of steep sub-threshold devices (e.g. TunnelFETs) for power reduction



TunnelFET challenge: ON-current

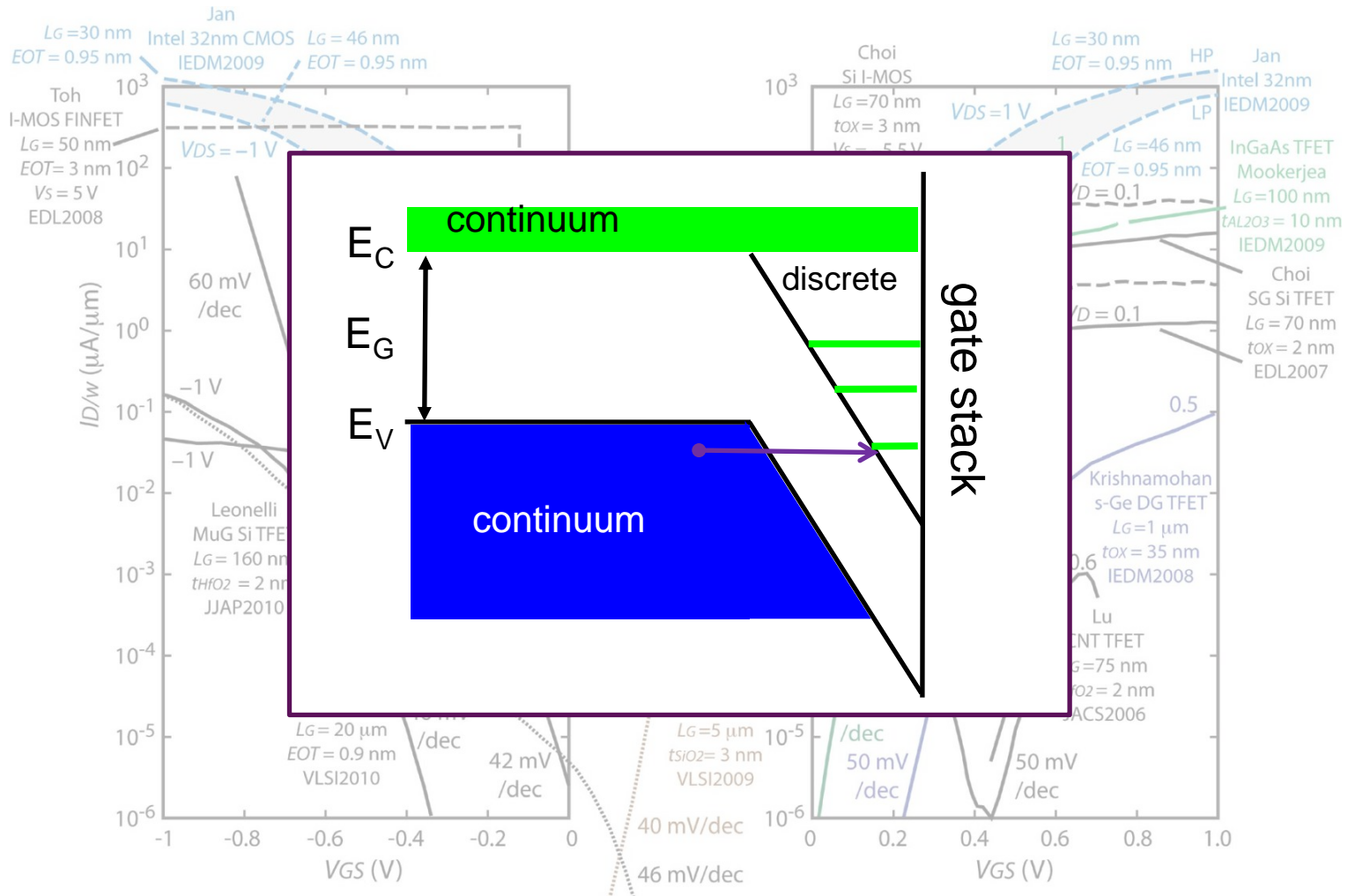
- ▶ ... with $SS < 60$ mV/dec but with (too) low ON current



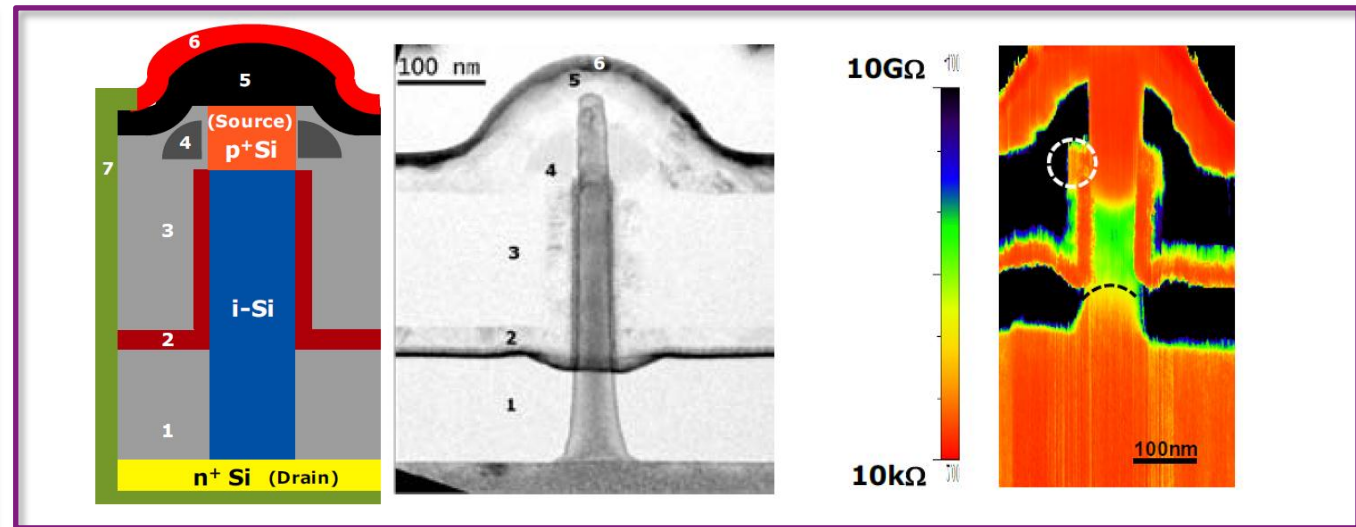
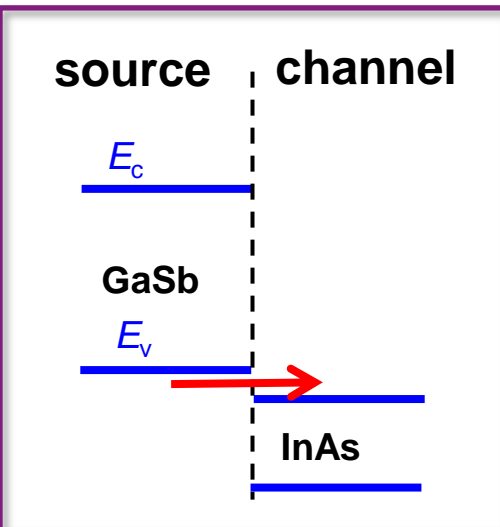
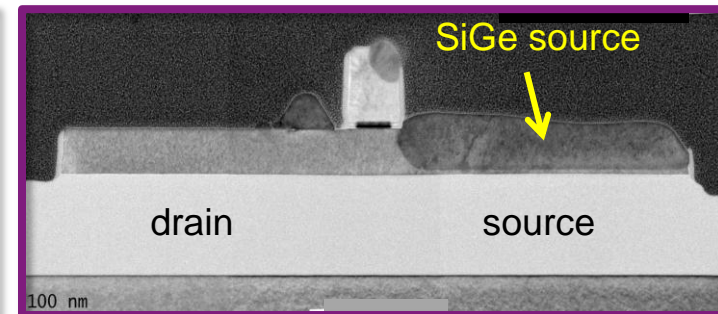
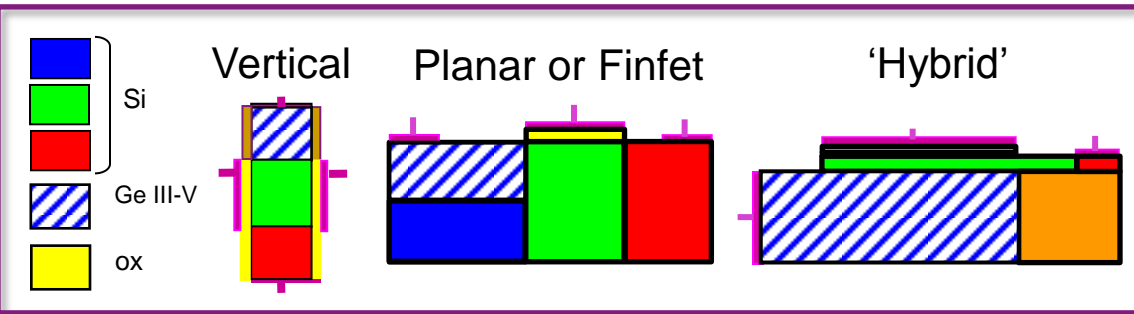
Alan C. Seabaugh and Qin Zhang, Proceedings of the IEEE, Vol. 98, No. 12, p. 2095, 2010

TunnelFET challenge: ON-current

- ▶ ... with $SS < 60$ mV/dec but with (too) low ON current



TunnelFET implementation



- ▶ Extensive modeling effort to calibrate tunneling efficiency (using P-i-N diodes)
- ▶ Exploration of new device concepts with improved field control
- ▶ Integration of demonstrators (vertical & horizontal) in progress

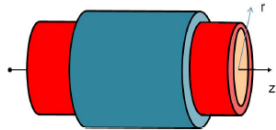
The pinch-off nanowire MOSFET

A junctionless device

- Negative gate voltage will push the majority carriers (electrons) to the middle of the wire. For sufficient negative gate voltage the channel is pinched off.
- No source and drain needed

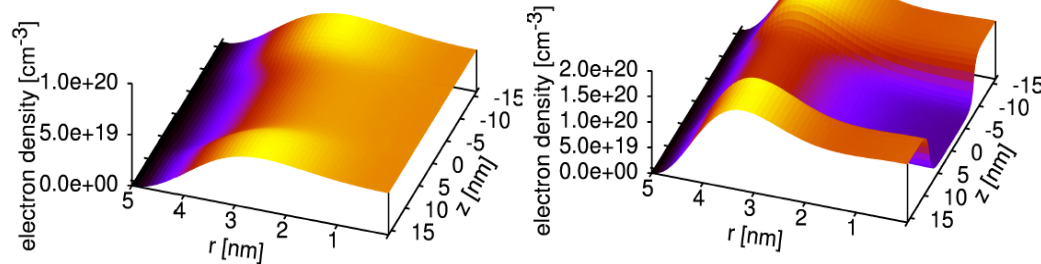
junctionless nPOFET

no strain, [001] channel
 $R = 5 \text{ nm}$, $L = 16 \text{ nm}$
 $V_{DS} = 1 \text{ mV}$
 $V_{GS} = 0 \text{ V}$



junction nMOSFET

no strain, [001] channel
 $R = 5 \text{ nm}$, $L = 16 \text{ nm}$
 $V_{DS} = 1 \text{ mV}$
 $V_{GS} = 1 \text{ V}$



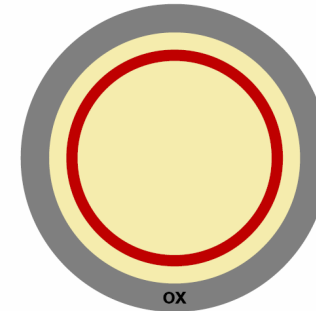
Bulk (volume) transport vs interface transport

Difference in charge density leads to difference in transport type

NMOSFET ON

$$V_G \gg V_T > 0$$

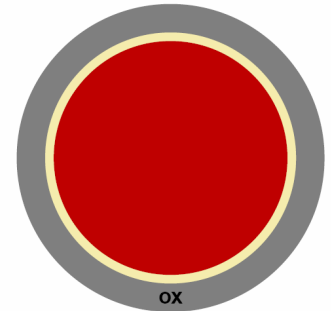
Electron density profile



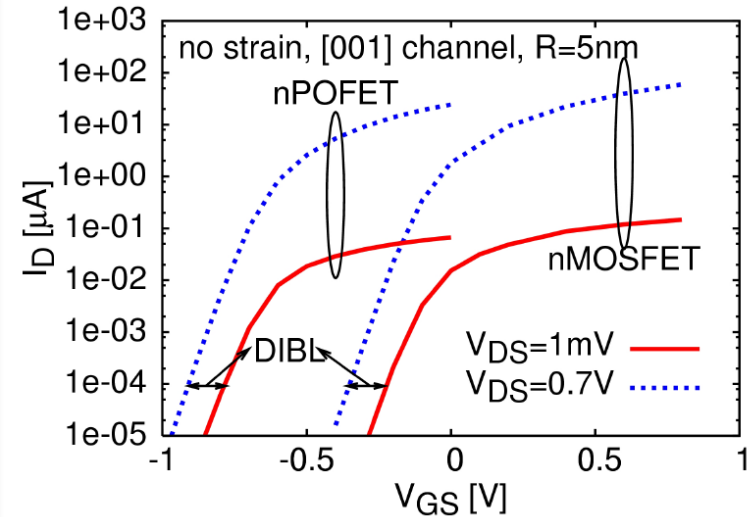
pinch-off MOSFET ON

$$V_G = 0 > V_T$$

Electron density profile



$L = 16 \text{ nm}$

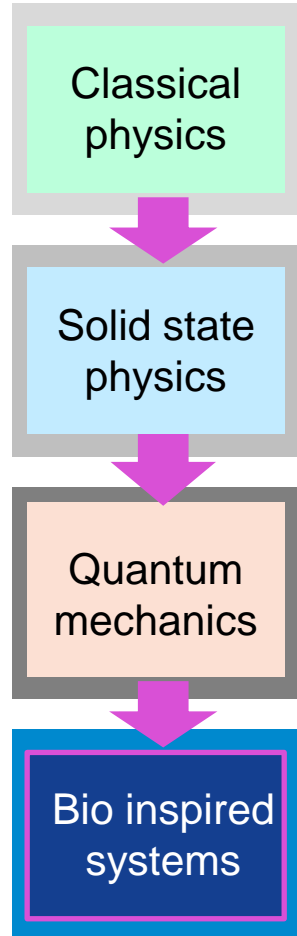
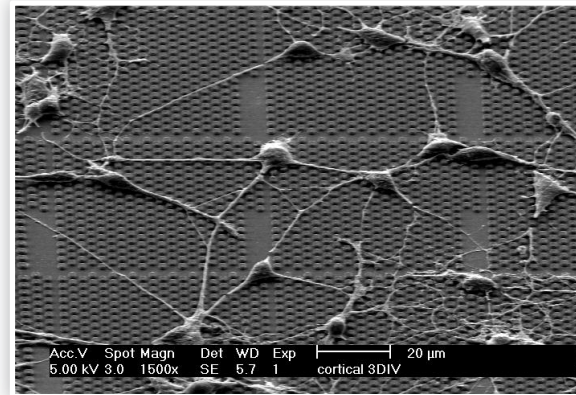
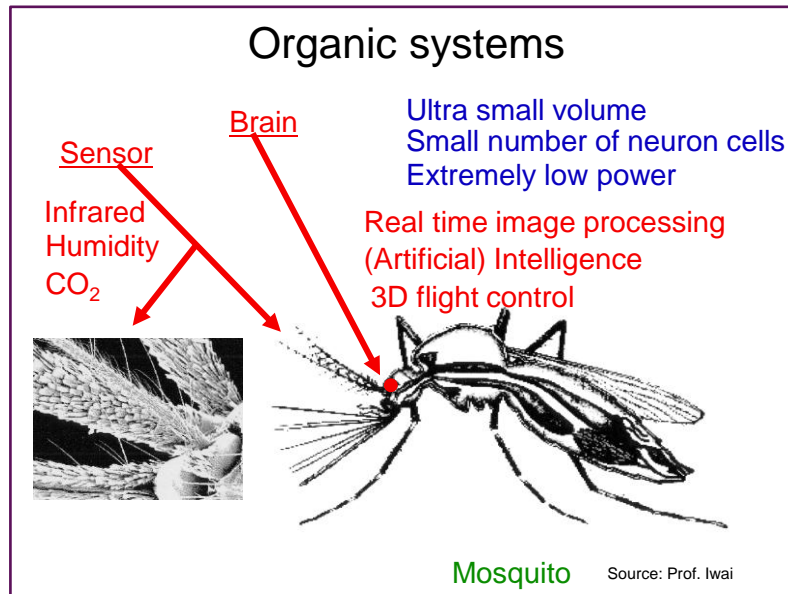
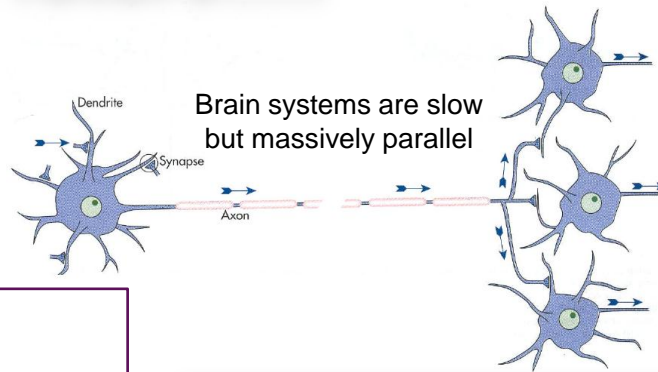


DIBL (nPOFET) \approx DIBL (nMOSFET) $\approx 177 \text{ mV/V}$
 SS (nPOFET) \approx SS (nMOSFET) $\approx 60 \text{ mV/dec}$

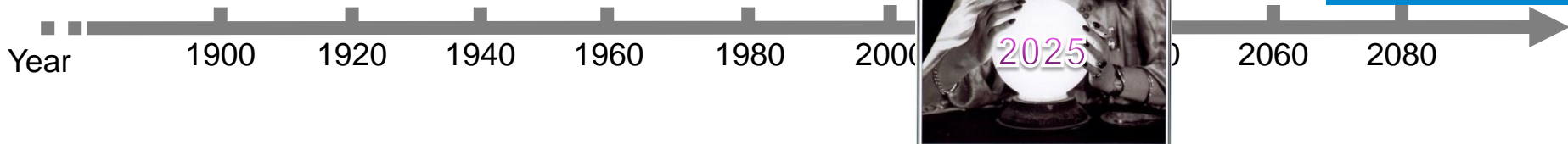
A look into the future.....

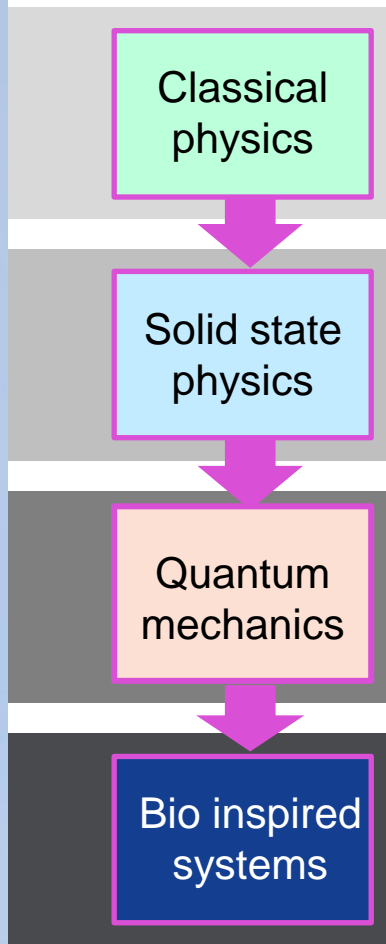
Brain neuron

The master of low power ...



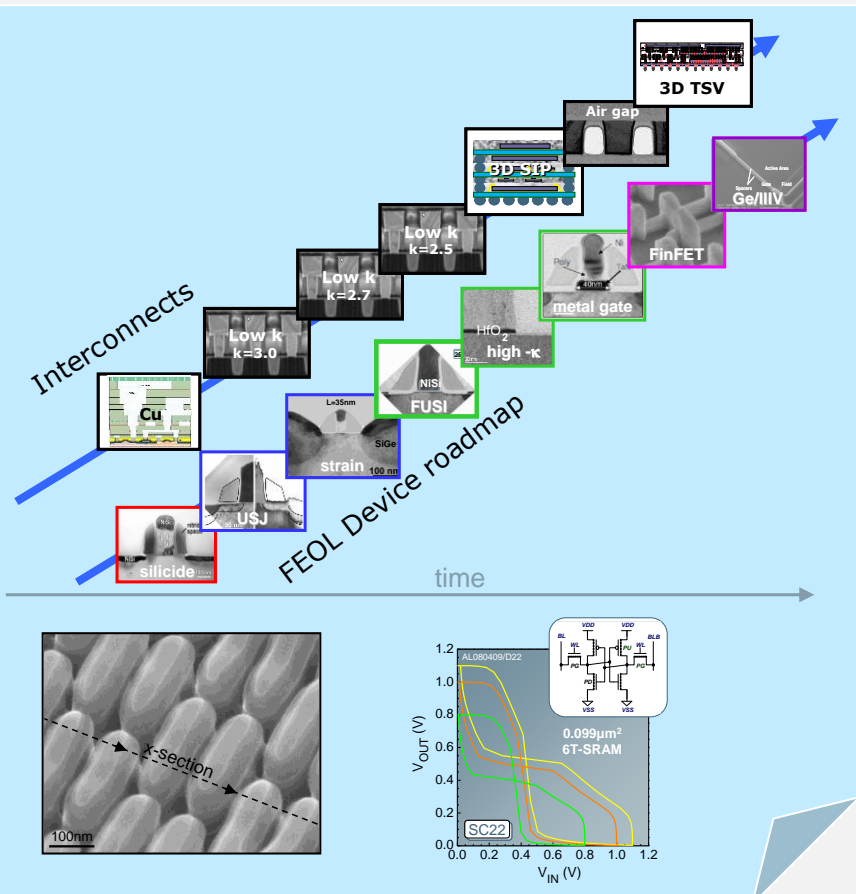
Introduction of bio-inspired systems
(bottom-up approach, self-assembling and self learning)



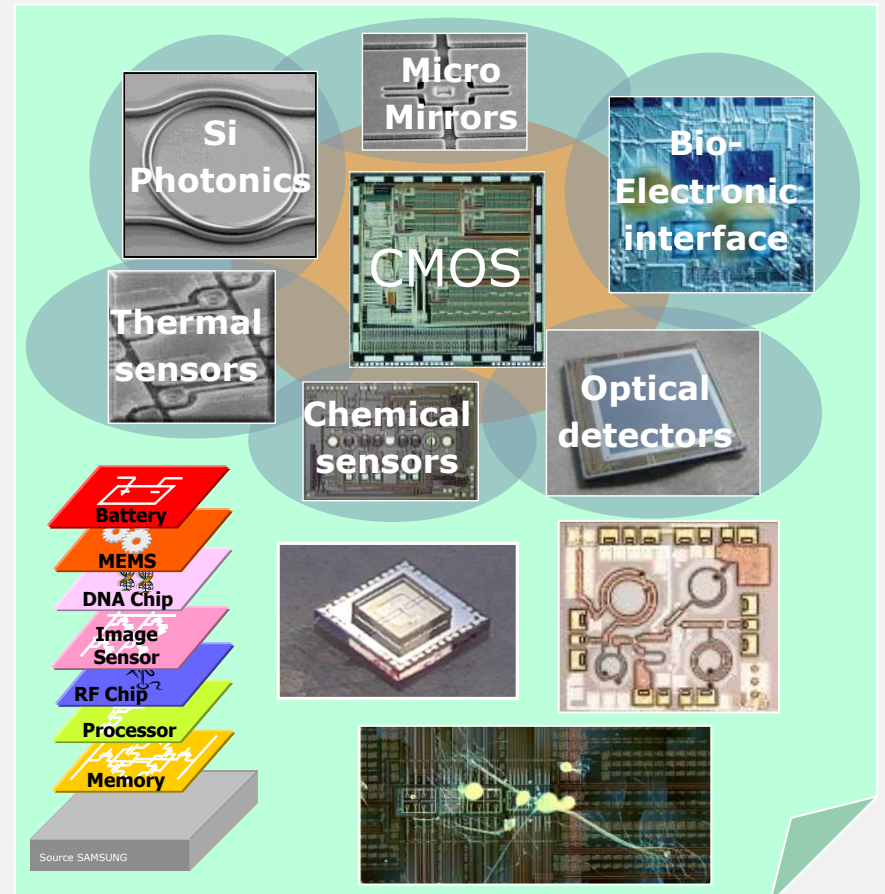


“More Moore” vs “More-than-Moore”

CMOS CMOS Scaling



CMORE Multi-functional SOC/SIP



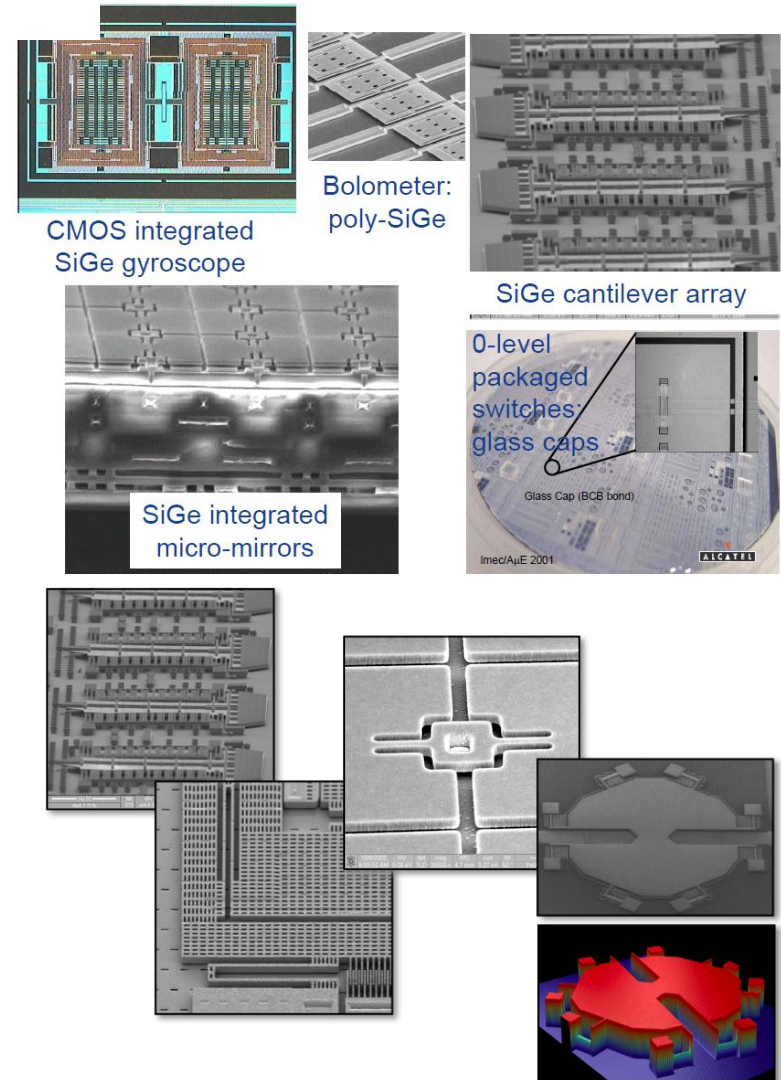
SiGe MEMS technology

For tight integration with driver IC

Different above CMOS MEMS approaches		
	Al	Poly-SiGe
Post CMOS integration	yes	yes
Fracture strength [GPa]	0.2	> 2
Mechanical Q	low	> 10.000
Reliability	creep: hinge memory effect	No creep

Poly-SiGe:

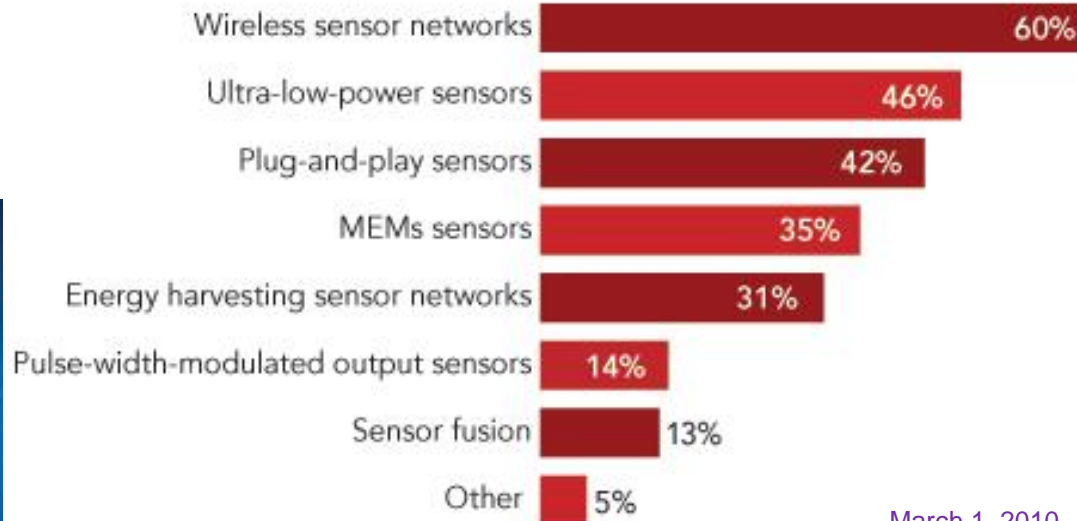
- better mechanical properties than Al: higher strength and Q factor
- better reliability properties than Al: less creep and fatigue



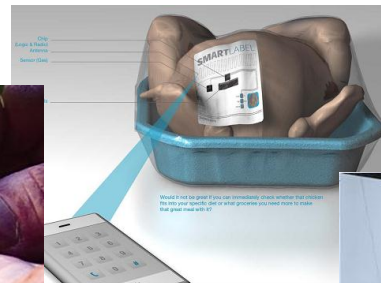
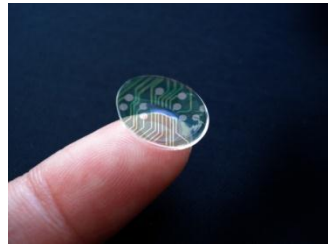
Sensors everywhere

The 2010 Trend Watch Sensor Survey Results

HOT SENSOR TECHNOLOGIES



March 1, 2010



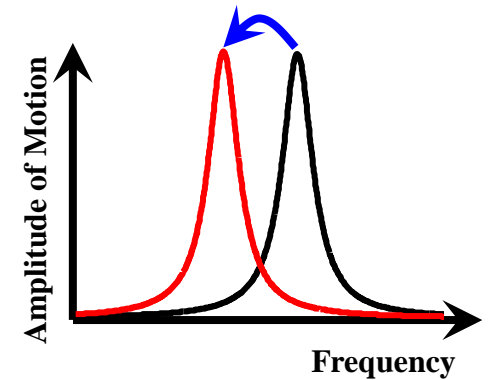
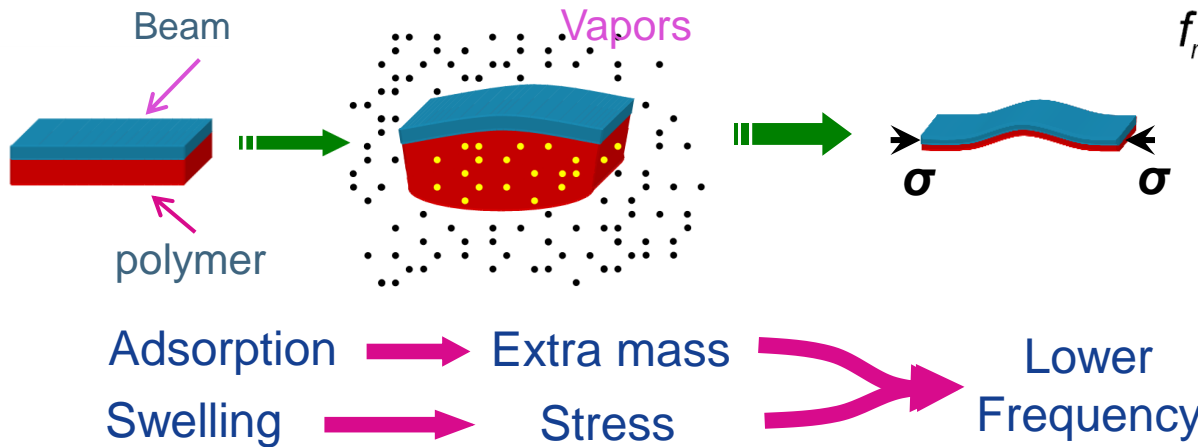
McKinsey: "Get Ready For Sensor-Driven Business Models" (March 3, 2010)

Underlying the Internet of Things are technologies such as RFID, **sensors** and smart-phones

e-nose: sensing in complex environments

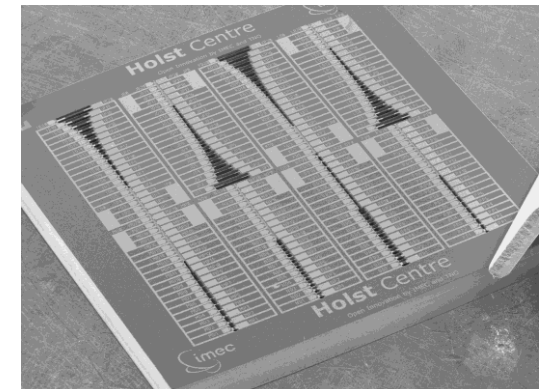
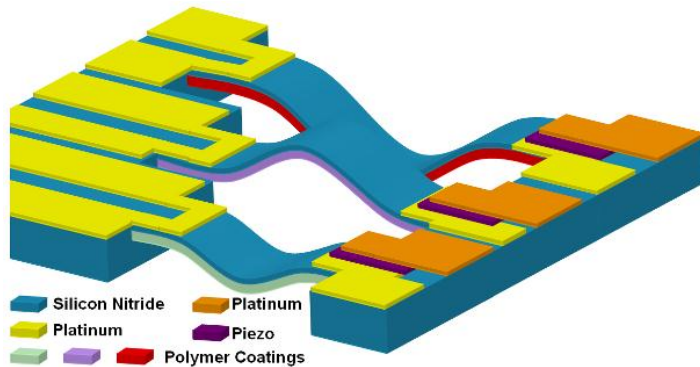
e-nose: array of non-specific, cross-reactive sensors combined with an information processing system

$$\frac{\Delta f_n}{f_n} = \frac{1}{2} \left(-\frac{\Delta m}{m} + \frac{\Delta k}{k} + \frac{\alpha_n \Delta \sigma}{1 + \alpha_n \sigma} \right)$$



e-Nose: from vision to reality:

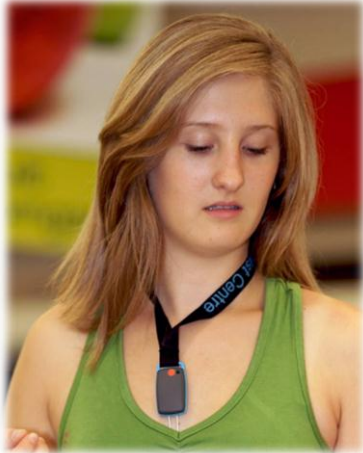
2.6 10⁻³ frequency shift / %EtOH, Power = 0.00017 mW



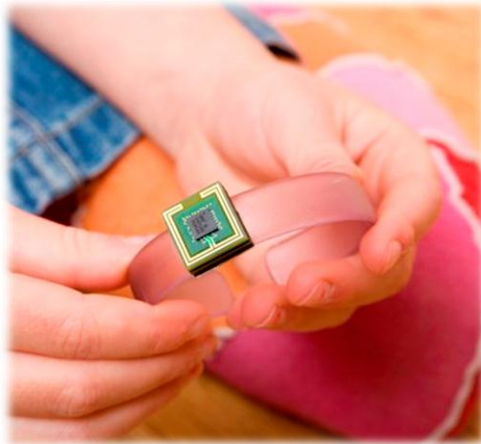
Die = 8.8 mm x 8.8 mm, 160 resonators

Body area network examples

Personal healthcare & lifestyle solutions



Necklaces/patches

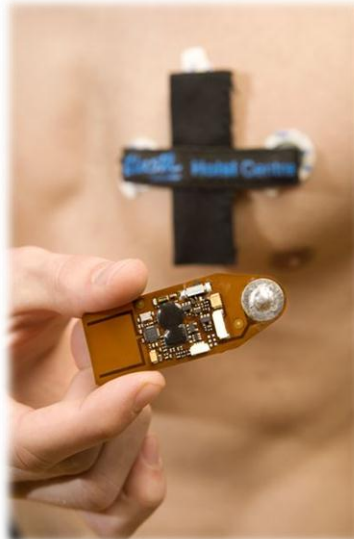


Watch-type



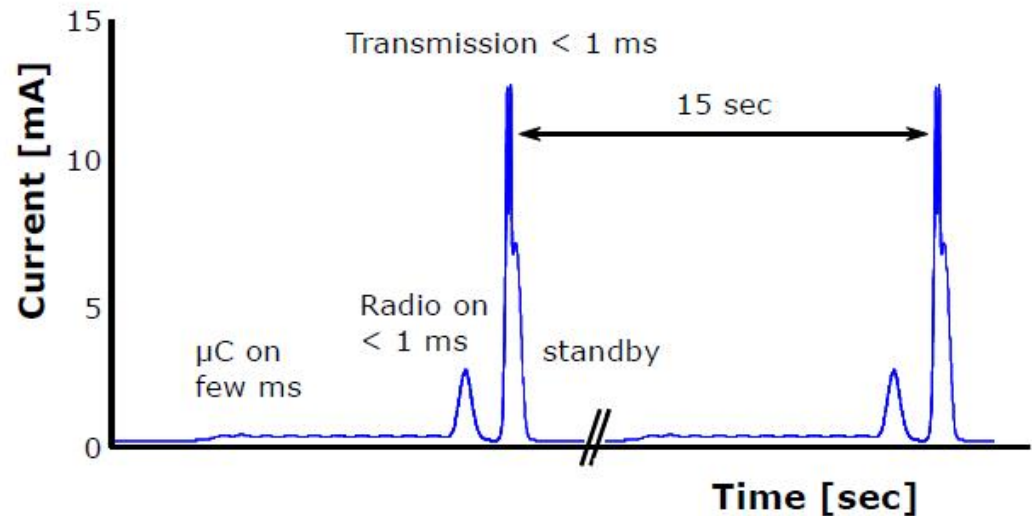
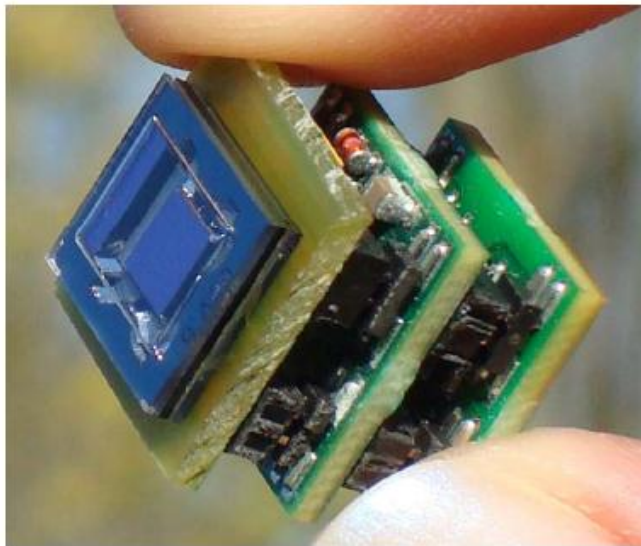
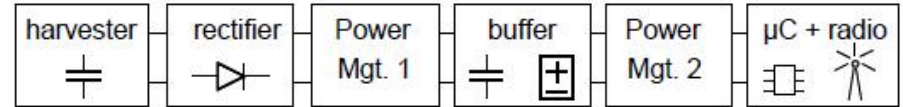
Headsets

Base Stations



Autonomous wireless sensor node

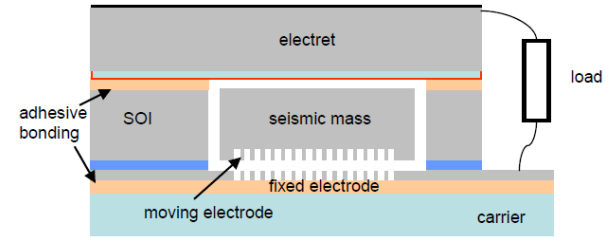
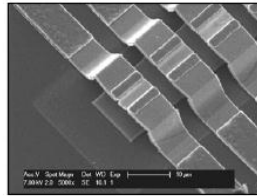
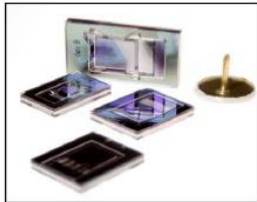
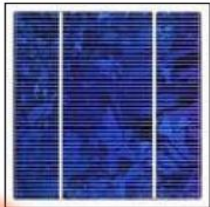
Harvester : 17 μ W, 3.0 – 8.5 V
Rectifier : $\eta = 60\%$
Power Mgt. : 2.2 – 4.2 V
Start-up time : < 1 minute capacitor charging
Transmission : 15 seconds + charging



autonomy by 10 μ W power consumption

Energy harvesting

Micropower Harvesting Sources



Electrostatic energy harvester

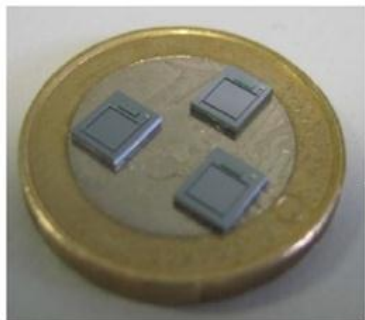
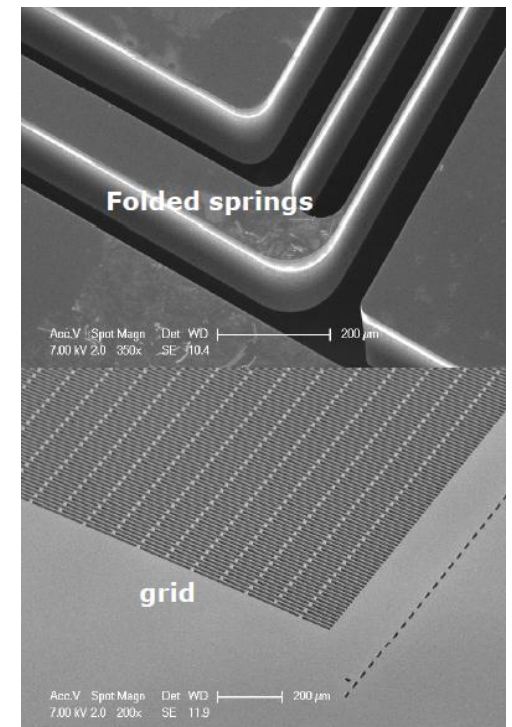
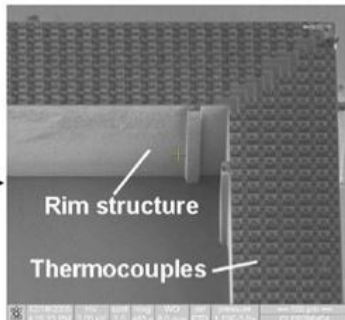
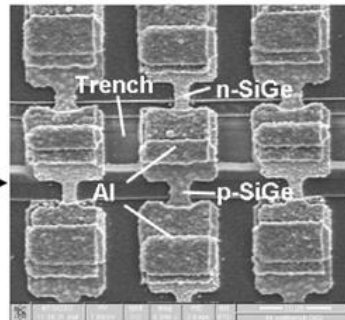


Photo of thermopile chips

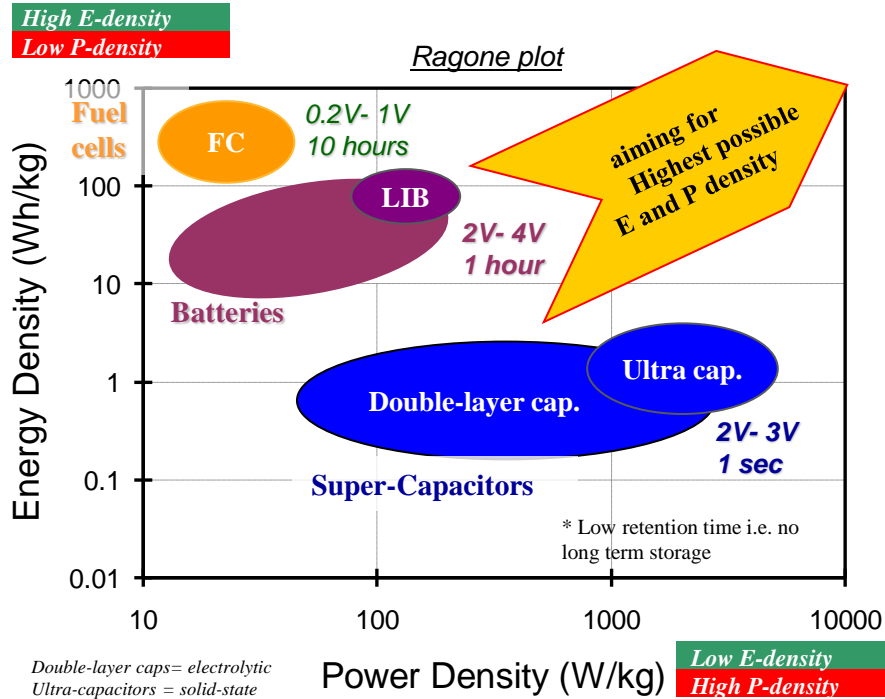


Zoom-in on a corner



Zoom-in on thermocouples

Energy storage



Thin film

Miniature

<~1g
<~0.1cm³
10uAh-1mAh
disposable & autonomous systems



Emerging Technologies

Battery packs

Portable

~10-100g
1-10cm³
10mAh-1Ah
portable electronics



Li-ion battery pack:
8cells
14.4V, 73Wh
(5A.h)

Mobile

~1kg-100kg
0.1-1m³
10Ah-100Ah
automotive transportation

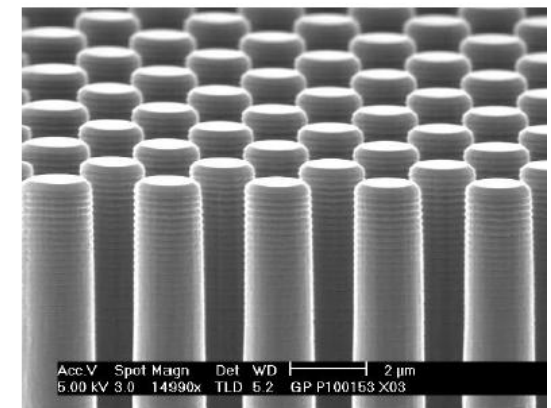


Storage for micro systems:

- All Solid-State devices (integrated systems)
- Microelectronic fabrication techniques

Size determines total capacity:

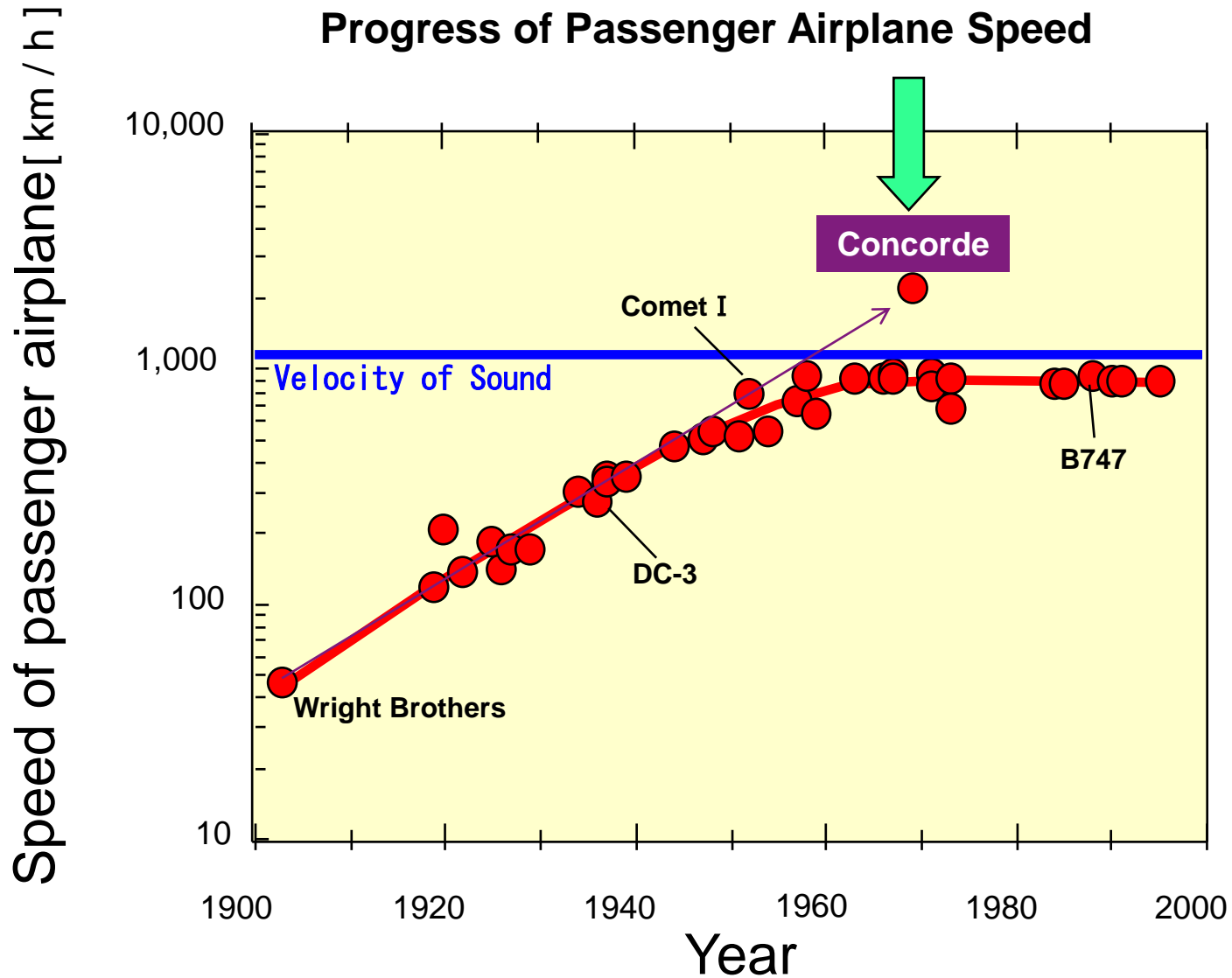
- High energy density even more important for small form systems



Where's the elephant in the room ?



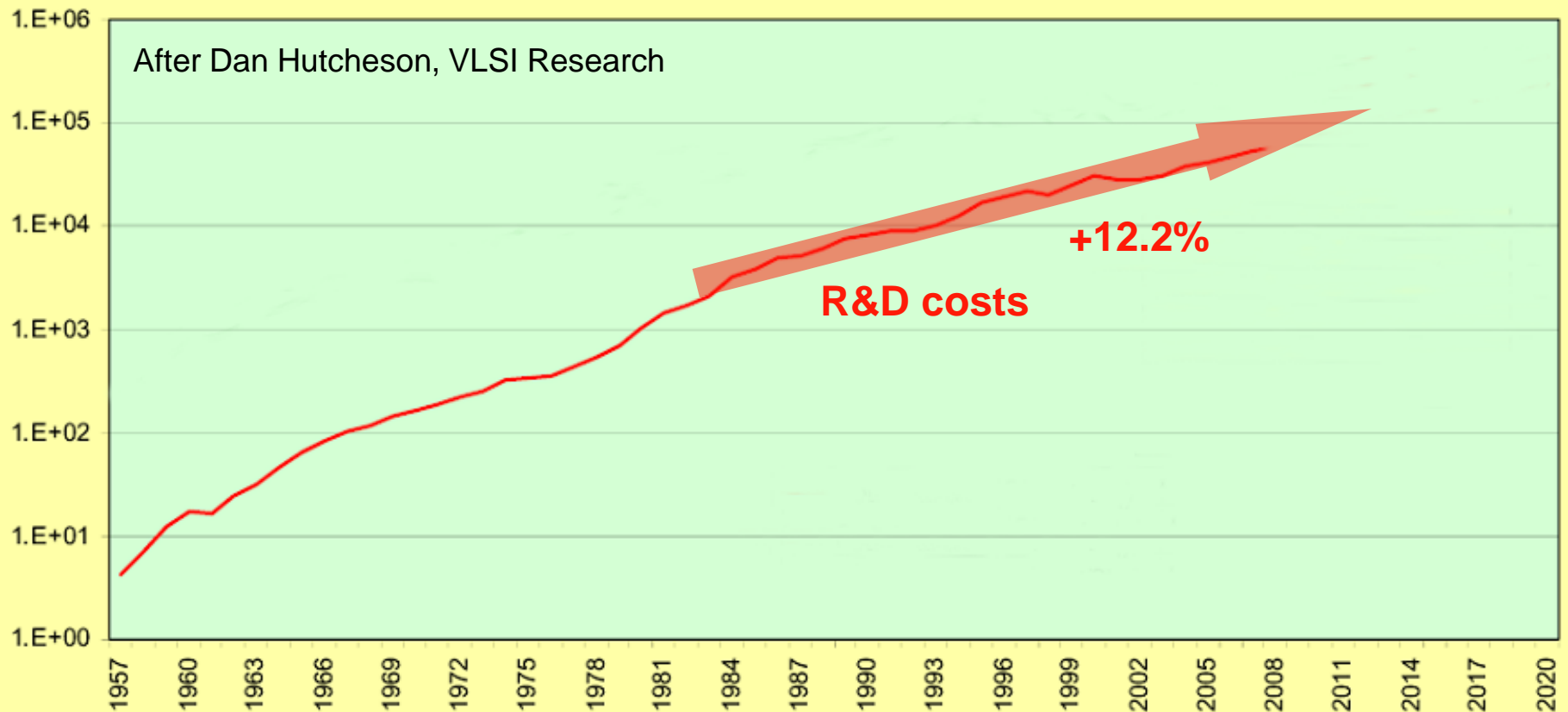
The importance of economics....



Source: Prof. Iwai

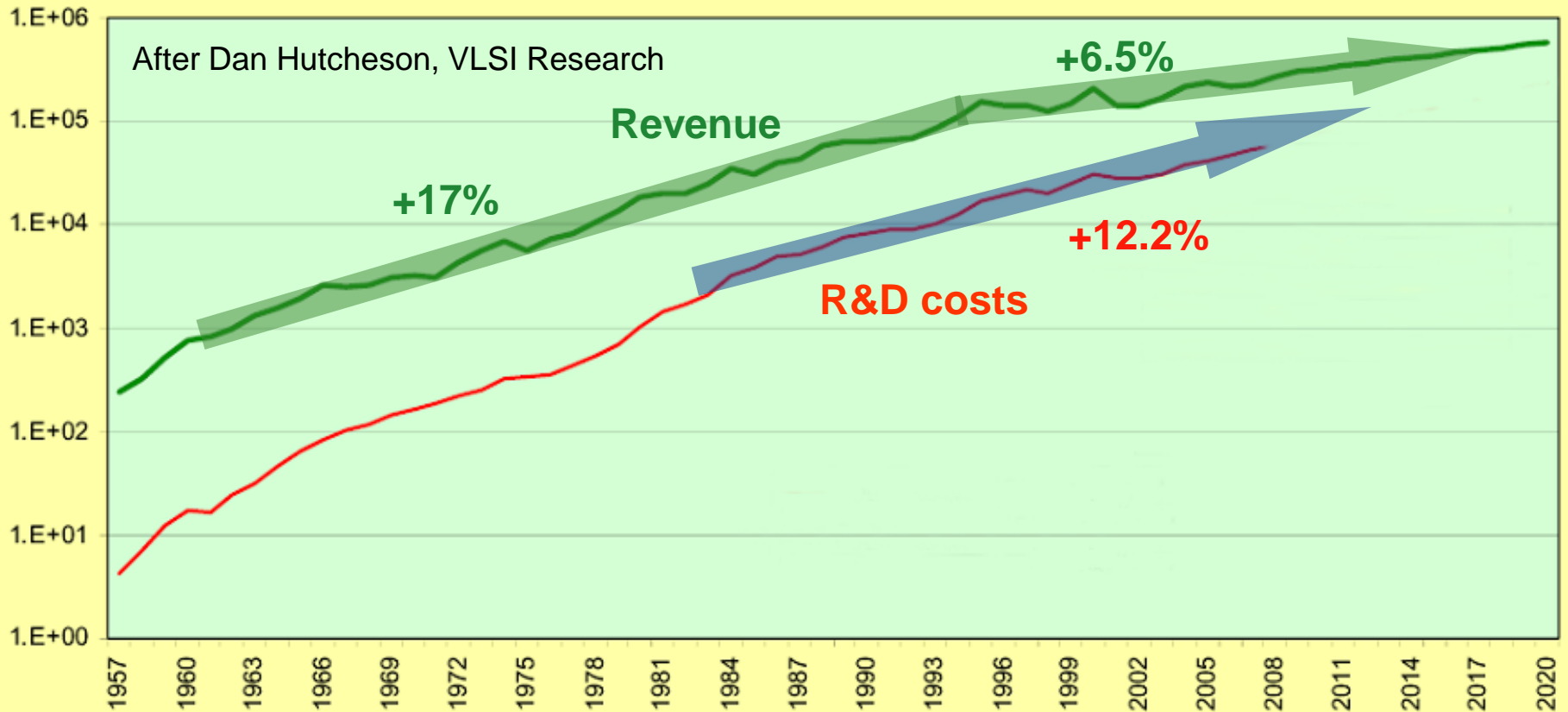
Cost of semiconductor research is increasing dramatically....

Chip Making R&D Versus Revenues (Worldwide in \$M)



...while growth rate of semiconductor revenues is reduced

Chip Making R&D Versus Revenues (Worldwide in \$M)



Joint multi-disciplinary R&D



... THE KEY TO INNOVATION

Conclusions

Will the transition be evolutionary or revolutionary ?

Continuous progress occurs, but once in a while small revolutions happen
(but often their importance is only recognized much later...)



Eugène Delacroix
Liberty leading the people (1830)

Will the transition be evolutionary or revolutionary ?

Continuous progress occurs, but once in a while small revolutions happen
(but often their importance is only recognized much later...)

- What will the driving forces be ?

Value to customers (i.e. “More than Moore”)
Economics (boundary condition)

- How can simulation lead the way ?

Theory starts to run ahead of experimental evidence
In the world of quantum mechanics simulation is of key importance

- Could the transition be ‘disruptive’ ?

Why not? (e.g. bio inspired systems...)

Who will be the winners and losers?

The winners will be the companies that see the revolution coming, quickly adapt to change and successfully team up in joint multi-disciplinary R&D to continuously innovate.

The losers will be everybody else....





**ASPIRE
INVENT
ACHIEVE**



KATHOLIEKE UNIVERSITEIT
LEUVEN



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