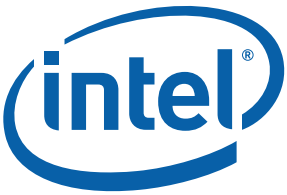

Intel® 81348 I/O Processor

Design Review Checklist

May 2007

Order Number: 315044-003US

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Revision History

Date	Revision	Description
October 2006	002	Reformatted Variable attributes.
September 2006	001	Launch Release.

1.0 Introduction

This document highlights design considerations you must review prior to manufacturing an adapter card or motherboard that implements the 81348.

The checklists address important connections to the 81348 and any critical supporting circuitry. However, the checklists are only for reference; for complete design instructions, refer to the 81348 *Design Guide*. These checklists are not necessarily complete and do not guarantee proper function of a design.

2.0 List of References

Table 1. List of References

Document	Reference
Intel® 81348 I/O Processor Developer's Manual	315036
Intel® 81348 I/O Processor Datasheet	315038
Intel® 81348 I/O Processor Design Guide	315054
Intel® 81348 I/O Processor Thermal Application Note	315050
Intel® 81348 I/O Processor Specification Update	315041
PCI Local Bus Specification, Revision 2.3	_http://www.pcisig.com/specifications/pcix_20
PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0a	http://www.pcisig.com/specifications/pcix_20
PCI Express Specification, Revision 1.0a	http://www.pcisig.com/specifications/pciexpress
PCI Express Base Specification 1.0a	http://www.pcisig.com/specifications/pciexpress
PCI Express Card Electromechanical Specification 1.0a	http://www.pcisig.com/specifications/pciexpress

3.0 Checklist Recommendations

The following tables provide design, debug and the termination recommendations for a 81348 layout.

Important Design and Debug Requirements

The following details are required for all 81348 designs. Note that these table is not an inclusive list. We recommend that design guide is referenced for additional details.

Note: Without implementing the debug requirements Intel will be extremely limited in its ability to assist with debug issues involving the transport firmware and device driver.

Table 2. Termination Values Checklist (Sheet 1 of 2)

Recommendations	Comments	Compliance	
		Yes	No
Debug Requirements			
• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware.	**UART0** is dedicated as the debug port for the transport firmware. This port is also implemented on Intel's development boards.Without the **UART0** port the debug of the transport firmware is extremely limited. ***Note:*** This port can be depopulated on production boards.		
• The serial console port connector to the **UART1** port to assist in debug of the application core firmware.	**UART1** is very useful for debugging user firmware on the application core.		
• The JTAG port must be implemented on the board to assist in debug of third party device drivers.	A JTAG port provides the ability to connect a 3rd party debugger to the 81348. Using a debugger is the only way to pinpoint potential device driver and transport firmware issues. ***Notes:*** 1. JTAG port is required even when the customer has no plans to utilize this connector in their debug process. Without the JTAG port, the debug of the device driver is extremely limited. 2. A low profile 10-pin JTAG port is now recommended to save on board space. Refer to the JTAG chapter of the design guide for implementation recommendations. This port may be depopulated on production boards.		
Design Notes			
• Supported and validated Flash components include Intel® StrataFlash® - J3, J3D and Intel® StrataFlash®h Embedded Memory - P30. • A minimum size of 2 MB is required for the transport firmware.	• For information on migrating from the J3 to P30 refer to the following document: http://developer.intel.com/design/flcomp/applnots/306667.htm ***Note:*** Other CFI Flash memory may work but these components have not been validated.		
• The 1.2 V Core power should be separated from the SAS/SATA and PCIE planes	Separating the 1.2 V core supply will minimize noise coupling.		
• The SAS PLL filtering must be connected to ground. All the other PLL filters are not connected ground.	Refer to Section 3.4.1 of this document		

Table 2. Termination Values Checklist (Sheet 2 of 2)

Recommendations	Comments	Compliance	
		Yes	No
• 1.2 V must be up before the 1.8 V. The 1.2 V must be down after the 1.8 V.	Refer to the power delivery chapter of the design guide for additional details.		
• JTAG **TRST_N** must be asserted at power-on	A reset supervisor to pulse **TRST_N** low on power-on and pull high after power-on. Refer to the JTAG section of the design guide.		
• In PCI-X central resource mode: (using the **P_CLK[3:0]** outputs): **REFCLKP**, **REFCLKN** must have a 100 MHz differential clock input and **CLK_SRC_PCIE#**=0 strapping resistor pulled low.	The 100 MHz clock input is needed to generate PCI clock outputs.		

3.1 Configuration Details

Table 3 provides the reset strap configuration for valid operational modes of the chip: PCI Express root complex or endpoint and PCI-X endpoint or central resource. Note that PCI Express endpoint and PCI-X endpoint mode simultaneously is not supported.

Note: The **PCIXCAP** signal has been defeatured. Refer to non-core Erratum 69 in the *Intel® 81348 I/O Processor Specification Update* for more information. This erratum overrides **PCIXCAP** references throughout this document.

Table 3. PCI Express/PCI-X Strapping Configuration Table

Application	Endpoint Configuration	Strapping Settings		
		INTERFACE_SEL_PCIX#	PCIE_RC# (PCI Express root Complex strap)	PCIX_EP# (PCIX endpoint strap)
HBA or Motherboard	PCI Express endpoint with PCI-X Central Resource (default)	1	1 (PCIE Endpoint)	1 (Central Resource)
HBA or Motherboard	PCI-X endpoint with PCI Express Root Complex	0	0 (PCI Root Complex)	0 (PCIX Endpoint
HBA or Motherboard	PCI Express endpoint	1	1	X
HBA or Motherboard	PCI-X endpoint	0	X	0
Motherboard	PCI Express Root Complex and PCI-X Central Resource	0 (ATU-X is function 0, ATU-E is function 5)	0	1
		1 (ATU-E is function 0, ATU-X is function 5)		
Motherboard	PCI-X Central Resource	0	X	1
Motherboard	PCI Express Root Complex	1	0	X

3.1.1 PCI-E Mode Only

PCI-E active refer to the Table 3 for **INTERFACE_SEL_PCIX#**, **PCIE_RC#** and **PCIX_EP#** straps for the following modes:

1. PCI-E root complex Section 3.1.3.1
2. PCI-E end point Section 3.1.3.2

3.1.1.1 PCI-E Root Complex

- **REFCLKP**, **REFCLKN** differential pins must be connected to 100 MHz oscillator.
- **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75 nF to 200 nF and then to corresponding RX lane pins on device or connector. Unused lanes can be **NC**s.
- **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector.
- **PE_CALP**, **PE_CALN** - Connect **PE_CALP** ball through 1.4 K 1% resistor to the **PE_CALN** ball.
- **INTERFACE_SEL_PCIX#** = 1 - Reset Strap NC (default)
- **PCIE_RC#** = 0, Reset Strap 4.7 K pull-down
- **CLK_SRC_PCIE#** = 0
- **P_CLKIN**: **GND**
- **P_PCIXCAP**: **GND**
- **P_INT[D:A]/XINT[3:0]**: 8.2 K pull-up
- **VCCVIO**: ground
- **VCC1P2PLLP** and **VSSPLLP** filter pins can be grounded.
- All other PCI-X pins are **NC**s

3.1.1.2 PCI-E endpoint

- **REFCLKP**, **REFCLKN** differential pins must be connected to 100 MHz oscillator.
- **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75 nF to 200 nF and then to corresponding RX lane pins on device or connector. Unused lanes can be **NC**s.
- **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector. Unused lanes can be **NC**s.
- **PE_CALP**, **PE_CALN** - Connect **PE_CALP** ball through 1.4 K 1% resistor to the **PE_CALN** ball.
- **INTERFACE_SEL_PCIX#** = 1 - Reset Strap **NC** (default)
- **PCIE_RC#** = 0, Reset Strap 4.7 K pull-down
- **CLK_SRC_PCIE#** = 0
- **P_CLKIN**: **GND**
- **P_PCIXCAP**: **GND**
- **P_INT[D:A]/XINT[3:0]**: 8.2 K pull-up
- **VCCVIO**: ground
- **VCC1P2PLLP** and **VSSPLLP** filter pins can be grounded.
- All other PCI-X pins are **NC**s.

3.1.2 PCI-X Mode Only

Use the following provisions when PCI-X interface is used and PCI Express is not used:

- **REFCLKP**/**REFCLKN** needs 100 MHz differential signal on it to generate **P_CLKO**s.
- **PE_CALP**, **PE_CALN** - Connect **PE_CALP** ball through 1.4 K 1% resistor to **PE_CALN** ball.
- **INTERFACE_SEL_PCIX#** = 0 - Reset Strap NC (default)
- **PCIE_RC#** = 1, Reset Strap 4.7 K pull-down
- **CLK_SRC_PCIE#** strap: Make sure strapping reflects whether clock source is the **REFCLKP**/**REFCLKN** **CLK_SRC_PCIE#** = 0 or PCI clock in **CLK_SRC_PCIE#** = 1 (default).
- All other PCI Express pins can be no connects. Make sure configuration strapping options are set correctly for operation mode refer to Table 3 for additional details.

3.1.2.1 Central Resource Mode: (PCIX_EP# = 1)

1. **P_PCIXCAP**:
   - **CLK_SRC_PCIE#** = 0, (using **P_CLK[3:0]** outputs): **P_PCIXCAP** connect signal with 3.3 KΩ pull-up to 3.3 V.
   - **CLK_SRC_PCIE#** = 0, (using **P_CLK[3:0]** outputs but limit PCI clock frequency): refer to Table 3. Note, strapping **PCIXM1_100#** is pulled low to limit frequency to 100 MHz.
   - **CLK_SRC_PCIE#** = 1, (**P_CLKIN** primary clock source): refer to Section 3.1.1 PCI frequency selection in the PCI-X Chapter of the design guide.
2. P_M66EN:
   - **CLK_SRC_PCIE#** = 0, (using **P_CLK[3:0]** outputs): pull-up signal 8.2 KΩ to 3.3 V.
   - **CLK_SRC_PCIE#** = 0, (using **P_CLK[3:0]** outputs but limiting the PCI clock frequency): refer to Table 3. Note that strapping **PCIXM1_100#** is pulled low to limit frequency to 100 MHz.
   - **CLK_SRC_PCIE#** = 1, (**P_CLKIN** primary clock source): Refer to the Section 3.1.1 of the PCI-X chapter for frequency selection.
3. **P_IDSEL**: pull-down the signal 1 KΩ resistor.
4. **P_REQ[0]#**/**P_GNT#**: This is an input request signal and should have a 8.2 K pull-up resistor.
5. **P_GNT[0]#**/**P_REQ#**: (internal arbiter): This is an output grant signal.
6. **P_GNT[3:1]#**: (internal arbiter) - These are output grant signals and unused signals can be **NC**s.
7. **P_REQ[3:1]#**: (internal arbiter) - These are input request signals and unused signals can be **NC**s.
8. **P_CLKIN**:
   - **CLK_SRC_PCIE#** = 0, Connect to **P_CLKOUT** through a 26 Ω +/- 1% resistor.
   - **CLK_SRC_PCIE#** = 1, (**P_CLKIN** primary clock source) connect to system clock.
9. **P_CLKOUT**:
   - **CLK_SRC_PCIE#** = 0, Connect to **P_CLKIN** through a 26 Ω +/- 1% resistor.
   - **CLK_SRC_PCIE#** = 1, (**P_CLKIN** primary clock source) signal can be left unconnected.

3.1.2.2 PCI-X Endpoint Mode (PCIX_EP# = 0)

1. **P_PCIXCAP**:
   - Pull-up signal with 8.2 K resistor and refer to Frequency Selection section in the PCI-X Chapter of the design guide for termination for the **PCIXCAP** pin on the edge connector.
   - **CLK_SRC_PCIE#** = 1, **P_CLKIN** primary clock source: refer to Frequency Selection Section 3.1.1 in the PCI-X Chapter of the design guide
2. **P_M66EN**: connect to the **M66EN** on the board and refer to Frequency Selection section in the Section 3.1.1 in the PCI-X Chapter of the design guide.
3. **P_IDSEL**: connect to one of the AD lines
4. **P_REQ[0]#/P_GNT#**: This is an input grant signal and should have a 8.2 K pull-up resistor.
5. **P_GNT[0]#/P_REQ#**: (external arbiter): This is an output request signal and should connect to the external arbiter's **P_REQ#** line.
6. **P_GNT[3:1]#**: (external arbiter): These signals are unused signals can be NCs.
7. **P_REQ[3:1]#**: (external arbiter): These signals are unused signals can be NCs.
8. **P_CLKIN**: Connect to system PCI clock.
9. **P_CLKOUT**: this signal can be left unconnected.
10. **REFCLKP** connect to a resistor divider such that the **REFCLKP** node is connected to both a 17.4 K to **VCC3P3** and a 4.7 K connected to **GND**. **REFCLKN** must be connected to **GND**.

3.1.3 Dual Interface Mode

For dual interface mode with PCI-E and PCI-X interfaces active refer to the Table 4 for **INTERFACE_SEL_PCIX#**, **PCIE_RC#** and **PCIX_EP#** straps for the following modes:

1. PCI-E root complex with PCI-X endpoint mode Section 3.1.3.1
2. PCI-X central resource with PCI-E endpoint mode Section 3.1.3.2
3. PCI-E root complex with PCI-X central resource mode Section 3.1.3.3

3.1.3.1 PCI-E Root Complex with PCI-X Endpoint Mode

- PCI-E Root complex:
  - **REFCLKP**, **REFCLKN** differential pins must be connected to 100 MHz oscillator.
  - **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75 nF to 200 nF and then to corresponding RX lane pins on device or connector. Unused lanes can be **NC**s.
  - **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector.
  - **PE_CALP**, **PE_CALN** - Connect **PE_CALP** ball through 1.4 K 1% resistor to the **PE_CALN** ball.
- PCI-X endpoint mode follow recommendations in Section 3.1.2.2

3.1.3.2 PCI-E endpoint with PCI-X Central Resource

- PCI-E Endpoint
  - **REFCLKP**, **REFCLKN** differential pins must be connected to 100 MHz oscillator.
  - **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75 nF to 200 nF and then to corresponding RX lane pins on device or connector. Unused lanes can be **NC**s.
  - **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector. Unused lanes can be **NC**s.
  - **PE_CALP**, **PE_CALN** - Connect **PE_CALP** ball through 1.4 K 1% resistor to the **PE_CALN** ball.
- PCI-X central resource mode follow recommendations in Section 3.1.2.1

3.1.3.3 PCI-E Root Complex with PCI-X Central Resource

- PCI-E Root complex:
  - **REFCLKP**, **REFCLKN** differential pins must be connected to 100 MHz oscillator.
  - **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75 nF to 200 nF and then to corresponding RX lane pins on device or connector. Unused lanes can be **NC**s.
  - **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector. Unused lanes can be **NC**s.
  - **PE_CALP**, **PE_CALN** - connect **PE_CALP** ball through 1.4 K 1% resistor to the **PE_CALN** ball.
- PCI-X central resource mode follow recommendations in Section 3.1.2.1

3.2 Termination Values Checklist

Table 4 lists these 81348 termination values.

Table 4. Termination Values Checklist (Sheet 1 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
S_TXP[7:0], S_TXN[7:0]	• Connect each of **S_TXP[7:0]**, **S_TXN[7:0]** lines with a 10 nF series capacitor with low ESR. • Unused ports can be left unconnected.	**Storage Transmit:** carries the differential output serial data and embedded clock for the SAS/SATA interface.		
S_RXP[7:0], S_RXN[7:0]	• Connect each of **S_RXP[7:0]**, **S_RXN[7:0]** lines with a10 nF series capacitor with low ESR. • Unused ports can be left unconnected.	**Storage Receive:** carries the differential input serial data and embedded clock for the SAS/SATA interface.		
S_CLKN0, S_CLKP0	• connect to differential 125 MHz ±100 ppm or a 150 MHz ±100 ppm oscillator. • use a 0.1 uF AC coupling series capacitor on **S_CLKN0** and **S_CLKP0**.	Differential storage clock		
RBIAS[1:0]	• 6.49 KΩ 1% to **GND**. Refer to Figure 7.			
RBIAS_SENSE[1:0]	• Connect to the same **GND** point of the **RBIAS[1:0]** resistors. Refer to Figure 7.			
S_ACT0/SCLOCK0, S_STAT0/SLOAD0	• **NC** when not used. • **SGPIO[0] is disabled:** Connect to LED with series resistor to indicate activity and status for storage engine[0].			
S_ACT1, S_STAT1	• NC when not used. • **SGPIO[0] is disabled:** These signals can be connected to an LED with series resistor to indicate activity and status for storage engine[1].			
S_ACT2/SDATAIN0, S_STAT2/SDATAOUT0	• NC when not used. • **SGPIO[0] is disabled:** These signals can be connected to an LED with series resistor to indicate activity or status for storage engine[2].			
S_ACT3, S_STAT3	• NC when not used. • **SGPIO[0] is disabled:** These signals can be connected to an LED with series resistor to indicate activity and status for storage engine[3].			
S_ACT4/SCLOCK1, S_STAT4/SLOAD1	• NC when not used. • **SGPIO[1] is disabled:** These signals can be connected to an LED with series resistor to indicate activity/status for storage engine[4].			

Table 4. Termination Values Checklist (Sheet 2 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
S_ACT5, **S_STAT5**	• **NC** when not used. • **SGPIO[1]** is disabled: These signals can be connected to an LED with series resistor to indicate activity /status for storage engine[5].			
S_ACT6/SDATAIN1, **S_STAT6/ SDATAOUT1**	• **NC** when not used. • **SGPIO[1] is disabled:** These signals can be connected to an LED with series resistor to indicate activity/status for storage engine[6].			
S_ACT7, **S_STAT7**	• **NC** when not used. • **SGPIO[1]** is disabled: These signals can be connected to an LED with series resistor to indicate activity/status for storage engine[7].			
REFCLKP, **REFCLKN**	• For PCI Express* interface: connect to a 100 MHz oscillator. • When using PCI-X (**CLK_SRC_PCIE#** = 0) and using the P_CLK[3:0] outputs: connect to these pins to a 100 MHz oscillator. • When PCI-X end point mode (**CLK_SRC_PCIE#** = 1): connect the **REFCLKP** to a resistor divider such that the **REFCLKP** node is connected to both a 17.4 K to V_{CC3P3} and a 4.7K connected to GND. **REFCLKN** must be connected to **GND**.	***Note:*** 100 MHz oscillator is required for the PCI Express differential clock and to generate the **P_CLK**s.		
PETP[7:0], **PETN[7:0]**	• Series capacitors with value of 75 nF to 200 nF (low ESR) on each of the lines. • **NC** when not used.			
PERP[7:0], **PERN[7:0]**	• No series capacitor needed. • **NC** when not used.			
PE_CALP, **PE_CALN**	Connect **PE_CALP** ball through 1.4K 1% resistor to the **PE_CALN** ball. Refer to Figure 5. ***Note:*** This is required even when the PCI-Express interface is not used.			
P_AD[63:32], **P_CBE[7:4]#**, **P_PAR64**	• When only PCI Express interface active, these signals are internally pulled-up and can be left as **NC**. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • When the **PCIX_32BIT#** is enabled (32-bit bus width), these signals are internally pulled-up and can be left as **NC**.			
P_AD[31:0], **P_CBE[3:0]#**	• When only PCI Express interface active these signals are internally pulled-up and can be left as **NC**.			

Table 4. Termination Values Checklist (Sheet 3 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
P_GNT[0]# / P_REQ#	• **PCI Express: P_GNT[0]# / P_REQ#** has an internal pull-up and can be left as a **NC**. • **In Central Resource mode (internal arbiter) with PCIX_EP# = 1: P_GNT[0]#** is output grant signal 0. • **PCI Endpoint mode (external arbiter) PCIX_EP# = 0:** This is the output request signal for the ATU and needs to connect to the external arbiter **P_REQ#** lines.			
P_REQ[0]# / P_GNT#	• **PCI Express: P_REQ[0]# / P_GNT#** has an internal pull-up and can be left as a **NC**. • **In Central Resource mode (internal arbiter) with PCIX_EP# = 1: P_REQ[0]#** is input request signal to the ATU. • **PCI Endpoint mode (external arbiter) PCIX_EP# = 0: P_GNT#** is input grant signal for the ATU. This pin should be pulled up to V_{CC3P3} with an 8.2 KΩ resistor.			
P_GNT[3:1]#	**PCI Bus Grant:** • **In Central Resource mode (internal arbiter) with PCIX_EP# = 1:** These are three output grant signals. Unused signals can be left as **NC**s. • **In endpoint mode (external arbiter) with PCIX_EP# = 0:** These signals are not used and can be left as **NC**s.			
P_REQ[3:1]#	**PCI Bus Request:** • **In Central Resource mode (internal arbiter) with PCIX_EP# = 1:** These are three input request signals to the internal arbiter. Unused signals can be left as **NC**s. • **In endpoint mode (external arbiter) with PCIX_EP# = 0:** These signals are not used and can be left as **NC**s.			
P_REQ64#	• When only PCI Express interface is active, these signals are internally pulled-up and can be left as a **NC**. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • When the device is PCI endpoint then the width of the bus is indicated by the state of **REQ64#** at the rising edge of **RST#**.			
P_ACK64#, P_PAR, P_SERR#, P_PERR#, P_INT[D:A]#	• When only PCI Express interface is active these signals are internally pulled-up and can be left as a **NC**. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up.			

Table 4. Termination Values Checklist (Sheet 4 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
P_FRAME#, P_IRDY#, P_TRDY#, P_STOP#, P_DEVSEL#	• When only PCI Express interface is active these signals are internally pulled-up and can be left as a **NC**. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • When the device is PCI endpoint **PCIX_EP#** = 0 state of these signals are used as for PCI-X initialization pattern at the rising edge of **RST#**.	Refer to the *PCI-X Specification 1.0b* for more information on the PCI-X Initialization pattern.		
P_M66EN	**PCI Express: P_M66EN** has an internal pull-up and can be left as a **NC**. **PCI-X Central Resource mode (PCIX_EP# = 1):** • **CLK_SRC_PCIE#** = 0 **(using the P_CLK[3:0] clock outputs):** Pull-up signal with 8.2 KΩ. • **CLK_SRC_PCIE#** = 1: **(P_CLKIN primary clock source):** Refer to PCI-X Frequency Selection Section of the design guide. **PCI Endpoint mode (PCIX_EP# = 0):** Refer to PCI-X Frequency Selection Section of the design guide.			
P_IDSEL	• **PCI Express: P_IDSEL** has an internal pull-up and can be left as a **NC**. • **PCI Central Resource mode PCIX_EP# = 1:** Pull-down signal with 1.0 KΩ. resistor. • **PCI Endpoint mode PCIX_EP# = 0:** Connect to one of the AD lines. Refer to PCI-X section of the *Intel® 81348 I/O Processor Design Guide.*			
P_CLKIN	For PCI Express only this signal should be connected to **GND**. **PCI Central Resource mode (PCIX_EP# = 1):** • **CLK_SRC_PCIE#** = 0: Connect to P_CLKOUT through a 26 Ω +/- 1% resistor. Refer to the PCI-X chapter for length match details. • **CLK_SRC_PCIE#** = 1 **(P_CLKIN** is the primary clock source): connect to the system PCI clock/ **PCI Endpoint mode (PCIX_EP# = 0)**: connect to the system PCI clock.	***Notes:*** • **REFCLKP**, **REFCLKN** must have 100 MHz clock to generate the **P_CLKO[3:0]** outputs. • When the **P_CLKIN** is the primary clock source (**CLK_SRC_PCIE#** = 1), the PCI Clock outputs are unavailable and must not be used as a clock source for any device.		

Table 4. Termination Values Checklist (Sheet 5 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
P_CLKOUT	For PCI Express only these signals can be unconnected. **PCI Central Resource mode (PCIX_EP# = 1):** • **CLK_SRC_PCIE#** = 0 (**using the P_CLKO[3:0] outputs):** Connect to the **P_CLKIN** through a 26 Ω +/- 1% resistor (see PCI-X chapter of the design guide for length match details) • **CLK_SRC_PCIE#** = 1: this signal can be left unconnected. PCI Endpoint mode **(PCIX_EP# =0)**: this signal can be left unconnected.	***Note:*** **REFCLKP**, **REFCLKN** must have 100 MHz clock to generate the **P_CLKO[3:0]** outputs.		
P_CLKO[3:0]	• Connect to PCI device **P_CLK** inputs through a 28 Ω +/- 1% series resistor for each slot and a 26 Ω +/- 1% for each embedded device. Refer to the PCI-X chapter of the design guide for length match details. • Any unused **P_CLKOs** can be left unconnected.	***Note:*** **REFCLKP**, **REFCLKN** must be have 100 MHz clock to generate the **P_CLKO[3:0]** outputs.		
P_PCIXCAP	**When PCI Express only:** • **GND** this pin. **When PCI Central Resource mode is enabled PCIX_EP# = 1:** • **CLK_SRC_PCIE# = 0 using P_CLK[3:0] outputs:** • **Using PCI bus slots:** connect signal with 3.3 KΩ pull-up to 3.3 V. • Using direct connection to PCI devices: 2. **CLK_SRC_PCIE# = 1 (P_CLKIN primary clock source):** refer to Frequency Selection section in the PCI-X Chapter of the design guide. **When PCI Endpoint mode:** • **PCIX_EP# = 0:** Refer to Frequency Selection section in the PCI-X Chapter of the design guide.	***Note:*** This signal has been defeatured. Refer to non-core Erratum 69 in the *Intel® 81348 I/O Processor Specification Update* for more information.		
P_BMI	• **When PCI Express only:** this signal can be left as a no connect. • **For PCI-X:** no connect when not used.			
P_CAL[0], P_CAL[2]	• When PCI-X interface is used: This pin is connected to a separate 22.1 Ω 1% resistor to **GND**. See PCIX section of the Design Guide for more information. • When PCI-X interface is not used: These pins can be left as **NC**s	**PCI** Calibration: is connected to an external calibration resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations.		
P_CAL[1]	• When PCI-X is used: This pin is connected to a separate 121 Ω 1% resistor to **GND**. • When PCI-X interface is not used: These pins can be left as **NC**s.	**PCI** Calibration: is connected to an external calibration resistor such that the output drivers reference the resistor to dynamically adjust the ODT resistance to compensate for voltage and temperature variations.		

Table 4. Termination Values Checklist (Sheet 6 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
M_CAL[0]	Connect to 24.9 Ω 1% resistor ground. Refer to Figure 6			
M_CAL[1]	Connect to 301 Ω 1% resistor to ground. Refer to Figure 6.			
ODT[1:0]	• **NC** when not used. • When On-Die DDR2 termination used connect to the ODT inputs on the DDR2 SRAM.			
M_CK[2:0], M_CK[2:0]#	Unused **M_CK**/**M_CK#**s can be left unconnected. When used with Registered DIMMs: • connect **M_CK[0]**/**M_CK[0]#** pair, **M_CK[1]**/**M_CK[1]#**, **M_CK[2]**/**M_CK[2]#** can be left unconnected. When used with unbuffered DIMMs: • Connect **M_CK[2:0]**/**M_CK[2:0]#** to the DDR2 **CK**/**CK#** inputs.	These DDR2 clock signals are used to provide the three differential clock pairs. Refer to Memory Controller Layout Section of the Design Guide for more details.		
M_RST#	NC when not used.	This Reset signal asynchronously forces all registered outputs LOW on the registered DDR2 DIMM		
MA[13:0]	• Unused address lines can be left unconnected. • When used refer to the Memory Controller Section of the Design Guide for DDR2 533 termination recommendations.	DDR2 address signals		
RAS#, CAS#, WE#, CS[1:0]#, CKE[1:0]	• Unused lines can be left unconnected. • When used refer to the Memory Controller Section of the Design Guide for DDR2 533 termination recommendations.	DDR2 control signals		
DQ[63:0], DM[8:0], CB[7:0], DQS[8:0], DQS[8:0]#	• Unused pins can be left unconnected. • When used refer to Memory Controller Section of the Design Guide for DDR2 533 termination recommendations.	Source Synchronous signals		
M_VREF	Connect to the memory VREF voltage 0.9 V refer to Memory Controller Layout Section of the Design Guide for DDR2 termination recommendations.			
A[24:0], D[15:0], POE#, PCE[1:0]#, PWE#, PB_RSTOUT#	• Unused pins can be left unconnected. • When used refer to PBI section of the Design Guide for layout connection recommendations.			
HS_ENUM#	Can be left unconnected when Hot-Swap not used.			

Table 4. Termination Values Checklist (Sheet 7 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
HS_LSTAT	When Compact PCI Hot-Swap is not supported, this signal must be tied to **GND**.	Hot-Swap **Latch Status:** An input indicating the state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. 0 = Connect to **GND** 1 = 8.2 KΩ pull-up to V_{CC}.		
HS_LED_OUT	• Connect to Hot-Swap blue LED. • When CompactPCI* Hot-Swap is not supported this signal can be left unconnected.			
HS_FREQ[1:0] / CR_FREQ[1:0]	See comments.	Hot-Swap **Frequency:** While in Hot-Swap mode, (these are only valid when **PCIX_EP#** = 0 and **HS_SM#** = 0). 00 = 133 MHz PCI-X 01 = 100 MHz PCI-X 10 = 66 MHz PCI-X 11 = 33 or 66 MHz. PCI (frequency depends on **P_M66EN**) default. **Central Resource Frequency:** While in Central Resource mode (these are only valid when **PCIX_EP#** = 1). 00 = 133 MHz 01 = 100 MHz 10 = 66 MHz 11 = 33 MHz (default) ***Note:*** 0 = connect to **GND**. 1 = internal pull-up.		
P_INT[D:A]# / XINT[3:0]#/ GPIO[11:8]	• **When using as interrupts and PCIX_EP# = 0:** No termination is required. • **When using as interrupts and PCIX_EP# = 1:** 8.2 KΩ pull-ups required on each line. • **When using as GPIOs:** 8.2 KΩ pull-up required on each line.	• **When INTERFACE_SEL_PCIX# = 0:** PCI Interrupt: These outputs are level sensitive. • **When INTERFACE_SEL_PCIX# = 1:** External Interrupt: requests are used by external devices to request interrupt service. These pins are level-detect inputs and are internally synchronized. These pins go to the **XINT[3:0]#** inputs of the Interrupt Controller.		
HPI#, NMI0#, NMI1#, XINT[7:4]#	8.2 KΩ pull-ups.			

Table 4. Termination Values Checklist (Sheet 8 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
GPIO[7:0] / XINT[15:8]# / CHAPOUT	8.2 KΩ pull-up.	• General Purpose I/O (default mode). • **External Interrupt:** These pins are level-detects and are internally synchronized. • **CHAPOUT: GPIO[7]** When enabled it will override the normal **GPIO[7]** function.		
SCL0, SDA0, SCL1, SDA1, SCL2, SDA2	• When used external pull-up to V_{CC} is required. Refer to the I^2C specification for information on calculating the pull-up. ***Note:*** Note:I2C0 port can only used for SEP enclosure management. • 2KΩ pull-up when unused.	The pull-up value is dependent on the bus loading. Refer to the I^2C specification: http://www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf		
SMBCLK	**For PCI Express adapter cards:** • When the SMBus is used, there should be isolation device such as the LTC4301 between this signal and **PE_SMCK** on the PCI Express connector. **For PCI Express motherboard applications:** • When SMBus is used a pull-up is required (value is dependent on the loading). • When SMBus is unused, a 8.2 KΩ pull-up is required.	LTC4301 is a hot-swappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website: http://www.linear.com/pc/productDetail.do?navId=H0,C1,C1007,C1070,P2460. Refer also to the http://www.smbus.org for the latest specification.		
SMBDAT	**For PCI Express adapter cards:** • When the SMBus is used, there should be isolation device such as the LTC4301 between this signal and **PE_SMDAT** on the PCI Express connector. **For PCI Express motherboard applications:** • When SMBus is used a pull-up is required (value is dependent on the loading). • When SMBus is unused, a 8.2 KΩ pull-up is required.	LTC4301 is a hot-swappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website: http://www.linear.com/pc/productDetail.do?navId=H0,C1,C1007,C1070,P2460. Refer also to the http://www.smbus.org for the latest specification.		
U0_RXD, U1_RXD	When unused, connect to GND.	***Note:*** **UART0** is dedicated as the debug port for the transport firmware as implemented on Intel's development boards. UART 1 is a general purpose port.		
U0_TXD, U0_RTS#, U1_TXD, U1_RTS#	Can be left unconnected when unused.	***Note:*** **UART0** is dedicated as the debug port for the transport firmware as implemented on Intel's development boards. UART 1 is a general purpose port.		

Table 4. Termination Values Checklist (Sheet 9 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
U0_CTS#, U1_CTS#	When unused, 8.2 KΩ pull-up.	***Note:*** **UART0** is dedicated as the debug port for the transport firmware as implemented on Intel's development boards. UART 1 is a general purpose port.		
TCK	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • **GND** when unused. • 8.2K pull-up when used. Refer to JTAG chapter of the Design Guide.	**Test Clock:** Provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG).		
TDI	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • **NC** when unused has weak pull-up. • 8.2K pull-up when used. Refer to JTAG chapter of the Design Guide.	**Test Data Input:** The JTAG serial input pin.		
TDO	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • **NC** when unused.	**Test Data Output:** The serial output pin for the JTAG feature.		
TRST#	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • **GND** when unused.	**Test Reset:** This pin has a weak internal pull-up.		
TMS	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • **NC** when unused has weak pull-up. • 8.2K pull-up when used. Refer to JTAG chapter of the Design Guide.	**Test Mode Select:** This pin has a weak internal pull-up.		
WARM_RST#	• When unused: 1 KΩ pull-up. • When used: This pin can be used only when the sticky-bit functionality is required. In this scenario, the **WARM_RST#** pin must be tied to the system reset **PCI_RST#** signal while the **P_RST#** pin can be tied to the system power good signal.	**Warm Reset** is the same as a cold reset, except sticky configuration bits are ***not*** reset. Notes: - When the PCI Express interface is used as an endpoint, the PCI Express in-band Hot Reset Mechanism can also be used to provide the sticky bit functionality. - On the customer reference board, **WARM_RST#** is tied to the **SRST_N** to provide a JTAG debugger reset. -Driving **WARM_RST#** using any other methods than suggested above may result in unpredictable behavior of the device.		

Table 4. Termination Values Checklist (Sheet 10 of 10)

Signal	Recommendations	Comments	Compliance	
			Yes	No
NC	**No Connect:** pins have no usable function and must not be connected to any signal, power or ground.			
THERMDA	• Connect to the anode of the thermal diode. • **NC** when unused.			
THERMDC	• Connect to the cathode of the thermal diode. • **NC** when unused.			
PUR1	• This pin must be pulled up to V_{CC3P3} with an external 8.2 KΩ resistor for proper operation.			

3.3 Reset Straps Checklist

Table 5 provides a list of reset straps that are multiplexed on the Peripheral Address Bus **A[24:0]**. These pins are latched on the rising edge of **P_RST#**. All reset strap signals are internally pulled to logic 1 by default. An external 4.7 KΩ 5% pull-down resistor is required to force a logic 0 on these pins.

Table 5. Reset Straps Checklist (Sheet 1 of 3)

Signal	Recommendations	Comments	Compliance	
			Yes	No
BOOT_WIDTH_8#	0 = 8 bits wide, 0 = 4.7 KΩ resistor pull down. 1 = 16 bits wide (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[0]**.		
CFG_CYCLE_EN#	0 = Configuration Cycles enabled, 0 = 4.7 KΩ resistor pull down. 1 = Configuration Retry enabled (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[1].**		
HOLD_X0_IN_RST#	0 = Hold Scale in reset, 0 = 4.7 KΩ resistor pull down. 1 = Do not hold in reset (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[2].**		
HOLD_X1_IN_RST#	0 = Hold in reset, 0 = 4.7 KΩ resistor pull down. 1 = Do not hold in reset (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[3].**		
MEM_FREQ[1:0]	10 = 533 MHz 11 = 400 MHz (Default mode). 0 = 4.7 KΩ pull-down resistor. 1 = internal pull-up.	***Note:*** **MEM_FREQ[1:0]** muxed onto signal **A[5]** and **A[4]** respectively. 0 = 4.7 KΩ resistor pull down. 1 = internal pull-up.		
EXT_ARB#	0 =) External arbiter, 0 = 4.7 KΩ resistor pull down. 1 =) Internal arbiter (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[6]**.		
INTERFACE_SEL_PCIX#	0 = ATU-X is function 0 (4.7 KΩ pull-down resistor) and ATUE is function 5. 1 = ATU-E is function 0 and ATUX is function 5. Refer to comments.	0 = 4.7 KΩ resistor pull down. 1 = internal pull up. ***Note:*** Muxed onto signal **A[10].**		
PCIX_EP#	Refer to comments.	**PCI-X End Point:** 0 = Endpoint. 1 = Central Resource (Default mode). ***Note:*** muxed onto signal **A[11].** Setting both **PCIX_EP#** and **PCIE_RC#** to endpoint is unsupported. 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
CONTROLLER_ONLY#	Refer to comments.	Controller only enable: • 0 = Controller only, requires 4.7 KΩ pull-down resistor, ATU disabled. • 1 = RAID enabled (Default mode). NOTE: muxed onto signal **A[23].**		

Table 5. Reset Straps Checklist (Sheet 2 of 3)

Signal	Recommendations	Comments	Compliance	
			Yes	No
DF_SEL[2:0]	• 81348 8 port mode each the **DF_SEL[2:0]** must be pulled low.	**Device Function Select: DF_SEL[2:0].** ***Note:*** **DF_SEL[2]** muxed onto signal **A[9]**. ***Note:*** **DF_SEL[1]** muxed onto signal **A[8]**. ***Note:*** **DF_SEL[0]** muxed onto signal **A[7]**. 0 = 4.7 KΩ resistor pull down.		
PCIE_RC#	Refer to comments.	**PCI-E Root Complex:** 0 = Root Complex. 1 = Endpoint (Default mode) ***Note:*** muxed onto signal **A[12].** Setting both **PCIX_EP#** and **PCIE_RC#** to endpoint is unsupported. 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
SMB_A5, **SMB_A3**, **SMB_A2**, **SMB_A1**	Refer to comments.	**SM Bus Address:** maps to address bits 5, 3, 2, and 1 where bits[7:0] represent the address the SMBus slave port will respond to when access is attempted. 0 = address bit will be low. 1 = address bit will be high (Default mode). ***Note:*** **SMB_A5** muxed onto signal **A[16].** ***Note:*** **SMB_A3** muxed onto signal **A[15].** ***Note:*** **SMB_A2** muxed onto signal **A[14]**. ***Note:*** **SMB_A1** muxed onto signal **A[13].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
PCIX_PULLUP#	When pulled-low enables the following signal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#**, **P_PAR64**, **P_REQ64#**, **P_ACK64#**, **P_FRAME#**, **P_IRDY#**, **P_TRDY#**, **P_STOP#**, **P_DEVSEL#**, **P_SERR#**, **P_PERR#**, **P_INT[D:A]#**	**PCI-X Pull Up:** 0 = enable PCI pull up resistors. 1 = disable PCI pull up resistors (Default mode). ***Note:*** Muxed onto signal **A[17].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
PCIX_32BIT#	When 32 PCI-X bus is enabled the following signals have internal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#** and **P_PAR64** and can be left as NC.	**32-Bit PCI-X Bus:** 0 = 32 bit wide PCI-X bus. 1 = 64 bit wide PCI-X bus. (Default mode) ***Note:*** Muxed onto signal **A[18].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
PCIXM1_100#	Refer to comments.	**PCI-X Mode 1 100 MHz Enable:** 0 = limit PCI-X mode 1 to 100 MHz. 1 = 133 MHz enabled (Default mode). ***Note:*** Muxed onto signal **A[19].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		

Table 5. Reset Straps Checklist (Sheet 3 of 3)

Signal	Recommendations	Comments	Compliance	
			Yes	No
HS_SM#	Refer to comments.	Hot-Swap **Startup Mode:** 0 = Hot-Swap mode enabled. 1 = Hot-Swap mode disabled (Default mode). ***Note:*** Muxed onto signal **A[21].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
FW_TIMER_OFF#	Refer to comments.	**Firmware Timer Off:** 0 = firmware timer disabled. 1 = firmware timer enabled (Default mode). ***Note:*** Muxed onto signal **A[22].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
CONTROLLER_ONLY#	Refer to comments.	Controller-Only Enable: 0 = Controller only, RAID disabled. 1 = RAID enabled (default mode). **NOTE:** Muxed onto signal **A[23].**		
LK_DN_RST_BYPASS#	Refer to comments.	Link Down Reset Bypass: Disables the full chip reset that. would normally be caused by a Link Down or hot reset. 0 = Do not reset on Link Down. 1 = Reset on Link Down (default mode). ***Note:*** Muxed onto signal **A[24].**		
CLK_SRC_PCIE#	Refer to comments.	**Clock Source PCI-E:** selects the PCI Express Refclk pair as the input clock to the PLLs that control most internal logic. 0 = source clock is **REFCLKP**/**REFCLKN**. 1 = source clock comes from the active PCI interface (Default mode). 0 = 4.7 KΩ resistor pull down. 1 = internal pull up. ***Note:*** Muxed onto signal **PWE#.**		
PCE[1:0]#	Pull up both these signals with 8.2 KΩ resistor.			

3.4 Analog Filter Checklist

This section describes filters needed for the PLL circuitry. Table 6 lists the PLLs that are required for this part.

Table 6. Required PLLs

Interface	Filtered Voltage	V_{CC} PLL Balls	V_{SS} PLL Balls	Layout Guideline Table
Storage	1.2 V	**VCC1P2PLLS0**	**VSSPLLS0**	Table 7
		VCC1P2PLLS1	**VSSPLLS1**	
PCI-X	1.2 V	**VCC1P2PLLP**	**VSSPLLP**	Refer to the: *Intel® 81341 and Intel® 81342 I/O Processors Design Guide*, Layout section.
Core Digital Logic	1.2 V	**VCC1P2PLLD**	**VSSPLLD**	
Intel XScale® core and XSI bus logic	3.3 V	**VCC3P3PLLX**	**VSSPLLX**	

3.4.1 VCC1P2PLLS0, VCC1P2PLLS1 Filter Requirements

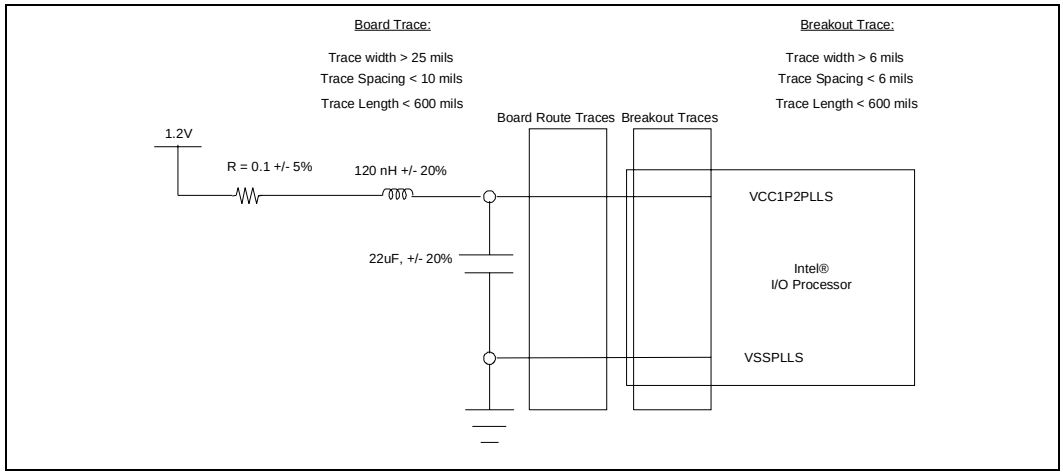
The low-pass filter, as shown in Figure 1, "VCC1P2PLLS0, VCC1P2PLLS1 Configuration" on page 27 reduces noise induced clock jitter and its effects on timing relationships in system designs. The Figure 1 filter circuit is recommended for the two PLL pairs:

- **VCC1P2PLLS0–VSSPLLS0**
- **VCC1P2PLLS1–VSSPLLS1**

Table 7. $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground. • **VCC1P2PLLS0**, **VSSPLLS0** and **VCC1P2PLLS1**, **VSSPLLS1** traces must be ground referenced (no **VCC** references).
Inductor	• 120 nH ±20%. • L must be magnetically shielded. • ESR: max < 0.3 Ω. • rated at 45 mA.
Capacitor	• 22 µF ±20% (Capacitor). • ESR: max < 0.3 Ω. • ESL < 2.5 nH. • Place 22 µF capacitor as close as possible to package pin.
Resistor	• 0.1 Ω 5% (Resistor). • 0.1 Ω 5% resistor must be placed between **VCC1P2** and L.
Breakout Trace	• Trace Width > 6 mils. • Trace Spacing < 6 mils. • Trace Length < 600 mils.
Board Trace	• Trace Width > 25 mils. • Trace Spacing < 10 mils. • Trace Length < 600 mils.
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	• 1.2"
Routing Guideline 1	• Route **VCC1P2PLLS** and **VSSPLL** as differential traces.
Routing Guideline 2	• Nodes connecting **VCC1P2PLLS** and capacitor must be as short as possible.
Routing Guideline 3	• 1.2 V supply regulator used for PLL filter must have less than ±3% tolerance.

Figure 1. VCC1P2PLLS0, VCC1P2PLLS1 Configuration



3.4.2 VCC1P2PLLP, VCC1P2PLLD Filter Requirements

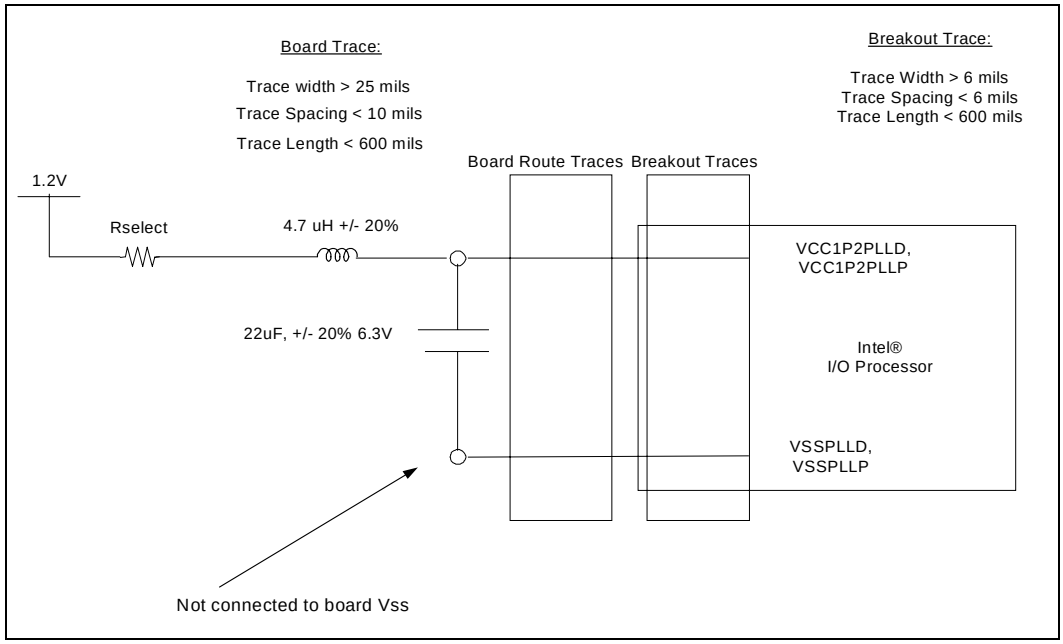
The low-pass filter (as shown in Figure 2, "VCC1P2PLLP, VCC1P2PLLD Low-Pass Filter Configuration" on page 29) reduces noise-induced clock jitter and its effects on timing relationships in system designs. The Figure 2 filter circuit is recommended for each of the PLL pairs: **VCC1P2PLLP–VSSPLLP**, **VCC1P2PLLD–VSSPLLD** pairs.

Note: When the PCI-X interface is not used the $V_{CC1P2PLLP}$ and V_{SSPLLP} pins can be grounded.

Table 8. $V_{CC1P2PLLP}$, $V_{CC1P2PLLD}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground. • **VCC1P2PLLP**, **VCC1P2PLLD** traces must be ground referenced (no **VCC** references).
Inductor	• 4.7 µH ±25%. • L must be magnetically shielded. • ESR: max < 0.3 Ω. • rated at 45 mA.
Capacitor	• 22 µF ±20% 6.3 V (Capacitor). • ESR: max < 0.3 Ω. • ESL < 2.5 nH. • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2 V plane to the top end of the capacitor is > 0.35 Ω (including board and component resistance) and • 1.2 V plane to **VCC1P2PLL** < 1.5 Ω. • 1/16 6.3 V. • resistor must be placed between **VCC1P2** and L. • Note: When trace and component resistance is large enough, discrete resistor is not required.
Breakout Trace	• Trace Width > 6 mils. • Trace Spacing < 6 mils. • Trace Length < 600 mils.
Board Trace	• Trace Width > 25 mils. • Trace Spacing < 10 mils. • Trace Length < 600 mils.
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	• 1.2"
Routing Guideline 1	• Route **VCC1P2PLLD** and **VSSPLLD**, **VCC1P2PLLP** and **VSSPLLP** as differential traces.
Routing Guideline 2	• Nodes connecting **VCC1P2PLLD** and capacitor, **VCC1P2PLLP** and capacitor must be as short as possible.
Routing Guideline 3	• 1.2 V supply regulator used for PLL filter must have less than ±3% tolerance.

Figure 2. VCC1P2PLLP, VCC1P2PLLD Low-Pass Filter Configuration



3.4.3 VCC3P3PLLX PLL Requirements

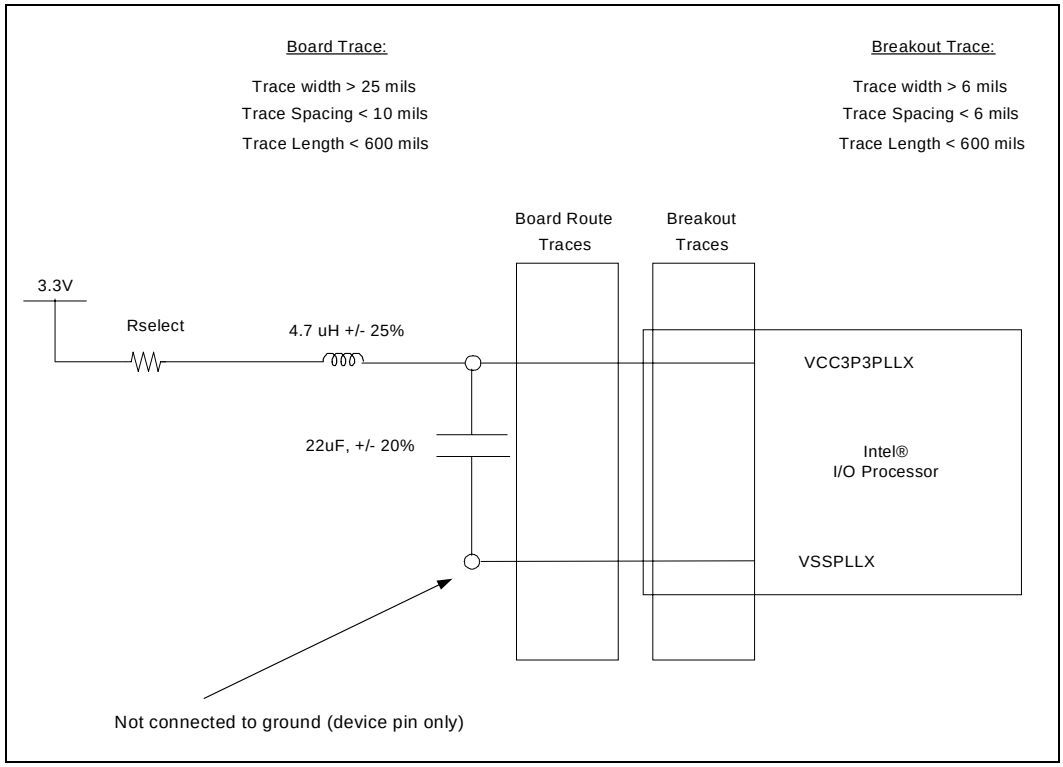
To reduce clock skew, a PLL is implemented for Intel XScale® processor and core logic. The balls associated with this PLL are **VCC3P3PLLX** and **VSSPLLX**. The low-pass filter, as shown in Figure 3 reduces noise induced clock jitter and its effects on timing relationships in system designs. The node connecting **VCC3P3PLLX** and the capacitor must be as short as possible.

The following notes list the layout guidelines for this filter.

Table 9. $V_{CC3P3PLL}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground referenced • **VCC3P3PLL** and **VSSPLLX** traces must be ground referenced (no V_{CC} references)
Inductor	• 4.7 µH • L must be magnetically shielded • ESR: max < 0.4 Ω • rated at 45 mA • An example of this inductor is TDK part number MLZ2012E4R7P.
Capacitor	• 22 µF (Capacitor) • ESR: max < 0.3 Ω • ESL < 2.5 nH • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 3.3 V plane to the top end of the capacitor is > 0.35 Ω • 3.3 V plane to **VCC3P3PLL** < 1.5 Ω • resistor ratings: 1/16 6.3 V • resistor must be placed between **VCC3P3** and L. • Note: When trace and component resistance is large enough the discrete resistor is not required
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	• 1.2"
Routing Guideline 1	• Route **VCC3P3PLLX** and V_{SSPLLX} as differential traces.
Routing Guideline 2	• Nodes connecting **VCC3P3PLL** and the capacitor must be as short as possible.

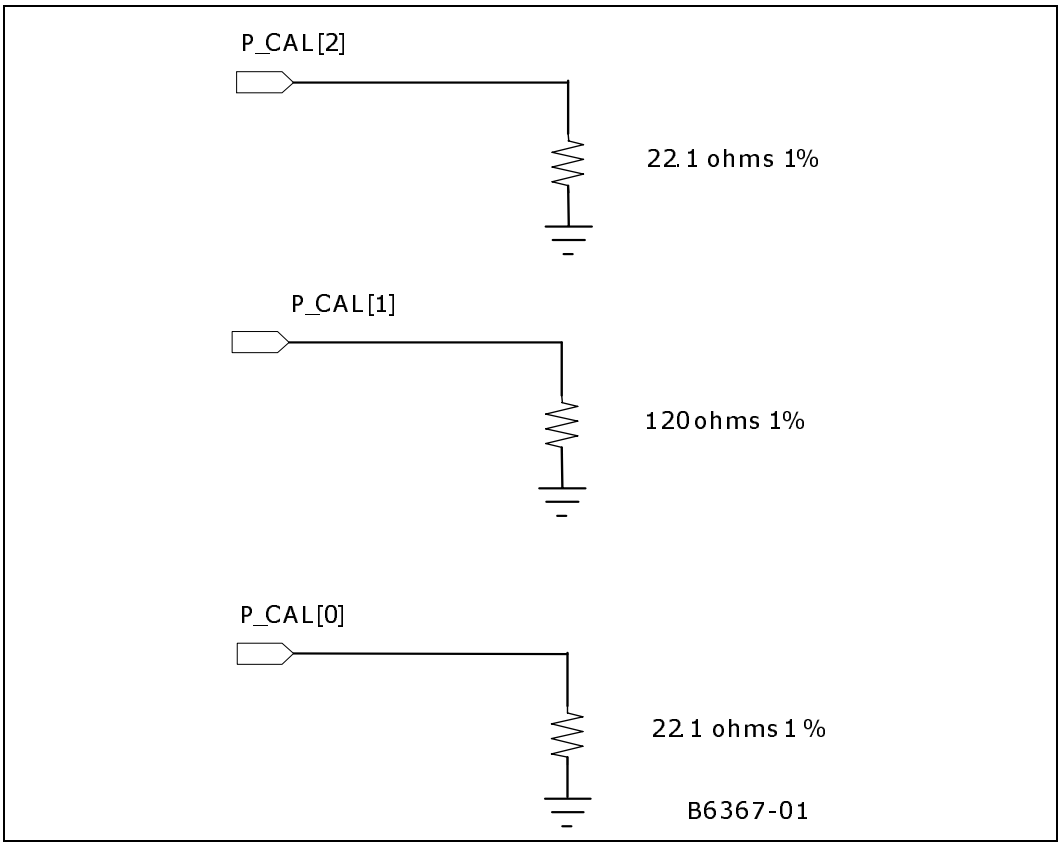
Figure 3. VCC3P3PLL Filter Configuration



3.5 PCI Resistor Calibration

Figure 4 shows the termination required for the PCI calibration circuitry. PCI Calibration pins **P_CAL[1:0]** are connected to an external calibration resistors. The PCI output drivers can reference the resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations.

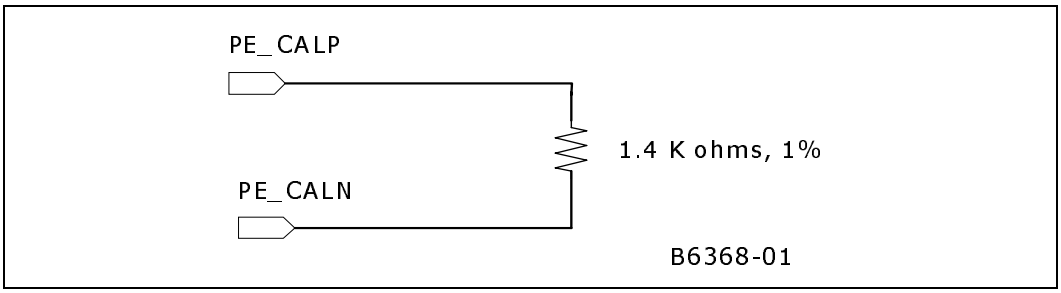
Figure 4. PCI Resistor Calibration



3.6 PCI Express Resistor Compensation

Figure 5 shows the termination required for the PCI Express RCOMP circuit.

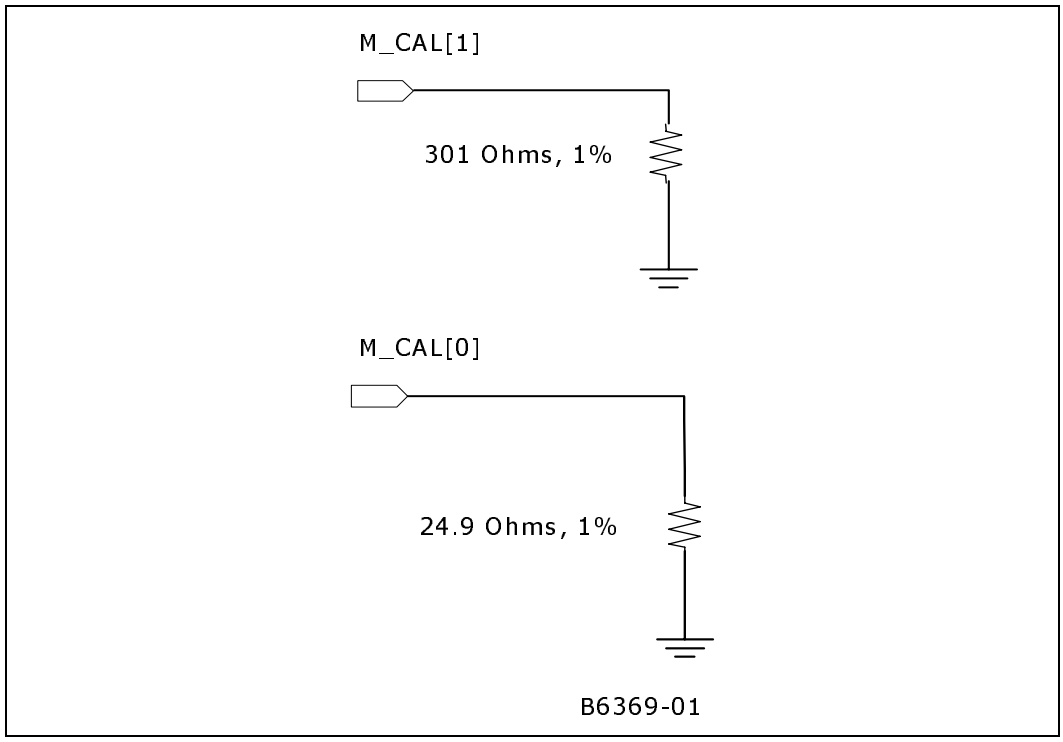
Figure 5. PCI Express RCOMP



3.7 Memory Calibration Circuitry

The Figure 6 shows the memory calibration pins **M_CAL[1]** and **M_CAL[0]** connected to external calibration resistors to ground. The memory output drivers reference the resistor to dynamically adjust the drive strength to compensate for temperature and voltage variations.

Figure 6. Memory Calibration Circuitry



3.8 RBIAS Circuit

Figure 7 provides a diagram on how to connect the **RBIAS0** and **RBIAS_SENSE0** pins. **RBIAS1** and **RBIAS_SENSE1** must be connected in the same manner.

Figure 7. RBIAS[0], RBIAS_SENSE[0] Connections