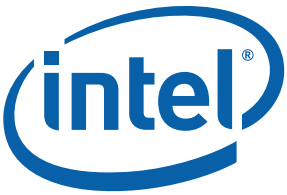

Intel® 413808 and Intel® 413812 I/O Controllers

Design Guide

May 2007

Order Number: 315055-002US

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Contents

Figures

Tables

Revision History

Date	Revision	Description
May 2007	002	Updated product naming conventions and fixed links. Converted to new template.
September 2006	001	Initial release

1.0 Introduction

1.1 About This Document

This document provides layout information and guidelines for designing platform or add-in board applications with Intel® 413808 and Intel® 413812 I/O Controllers (Figure 1). The Intel® 413808 I/O Controller is an 800 MHz controller and the Intel® 413812 I/O Controller is a 1200 MHz controller.

Intel recommends employing best-known design practices using board-level simulation, signal integrity testing and validation to create a robust design. Designers should note that this guide focuses on specific design considerations for this part and is not intended to be an all-inclusive list of good design practices. It is recommended that this guide is used in conjunction with empirical data to optimize your particular design.

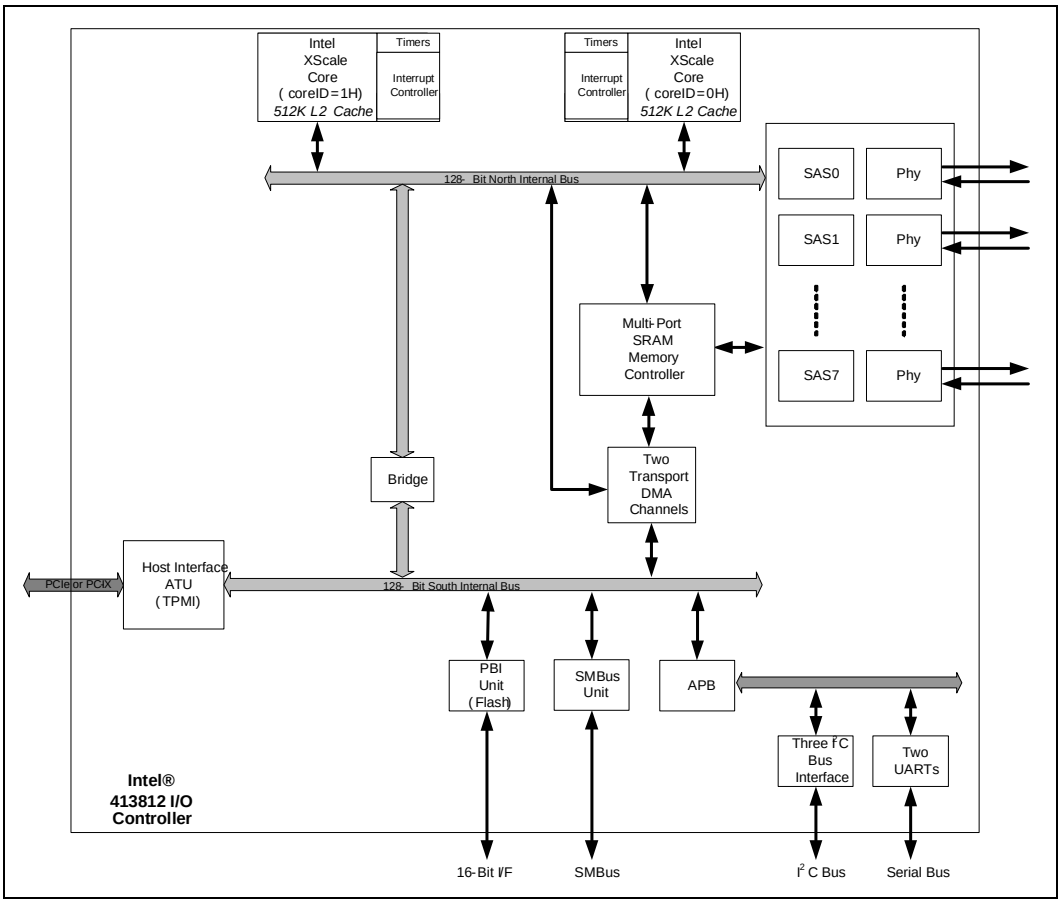
The simulation conditions used for each of the interfaces are listed in Appendix A. The simulations were performed for motherboard and adapter card topologies. The impedance used for the motherboard is 50 ohm +/- 15% and the adapter card trace impedance is 60 ohm +/- 15%. These results are based on the six layer board stackup that is provided in Chapter 3.0.

1.2 Document Details

This document is partitioned into the following chapters:

- The top level block diagram and package dimensions are provided in Chapter 2.0, "Package Information".
- The example stackups for a motherboards and adapter cards are provided in Chapter 3.0, "Board Layout Guidelines".
- The layout guidelines external interfaces are listed in the following chapters: Chapter 4.0, "PCI-X Layout Guidelines", Chapter 5.0, "PCI Express Layout", Chapter 6.0, "SATA/SAS Bus Layout", and Chapter 7.0, "Peripheral Local Bus".
- The required terminations are listed in Chapter 11.0, "Terminations". This chapter also details the recommended filtering.
- The summary of the layout guidelines for each of the interfaces and the filters is listed in Chapter 12.0, "Layout Checklist".
- The details on power sequencing and decoupling recommendations are provided in Chapter 8.0, "Power Delivery".
- The details on our recommended heatsink solutions are listed in Chapter 10.0, "Thermal Solutions".
- The details on test equipment are listed in Chapter 9.0, "Debug and Test".
- The references are listed in Chapter 13.0, "References".
- The definitions and the simulation conditions (used for all the simulations described in this document) are provided in Appendix A.

Figure 1. Two Core I/O Controller



2.0 Package Information

2.1 Package Introduction

Intel® 413808 and Intel® 413812 I/O Controllers are offered in a 1357-ball FCBGA5 package. This package is shown in Figure 2. Figure 3 shows the top view of the package with the interfaces labeled and color coded. This figure is helpful during board layout. The signals are located on the FCBGA package to simplify signal routing and system implementation.

Figure 2. Intel® 413808 and Intel® 413812 I/O Controllers 1357-ball FCBGA Package Diagram

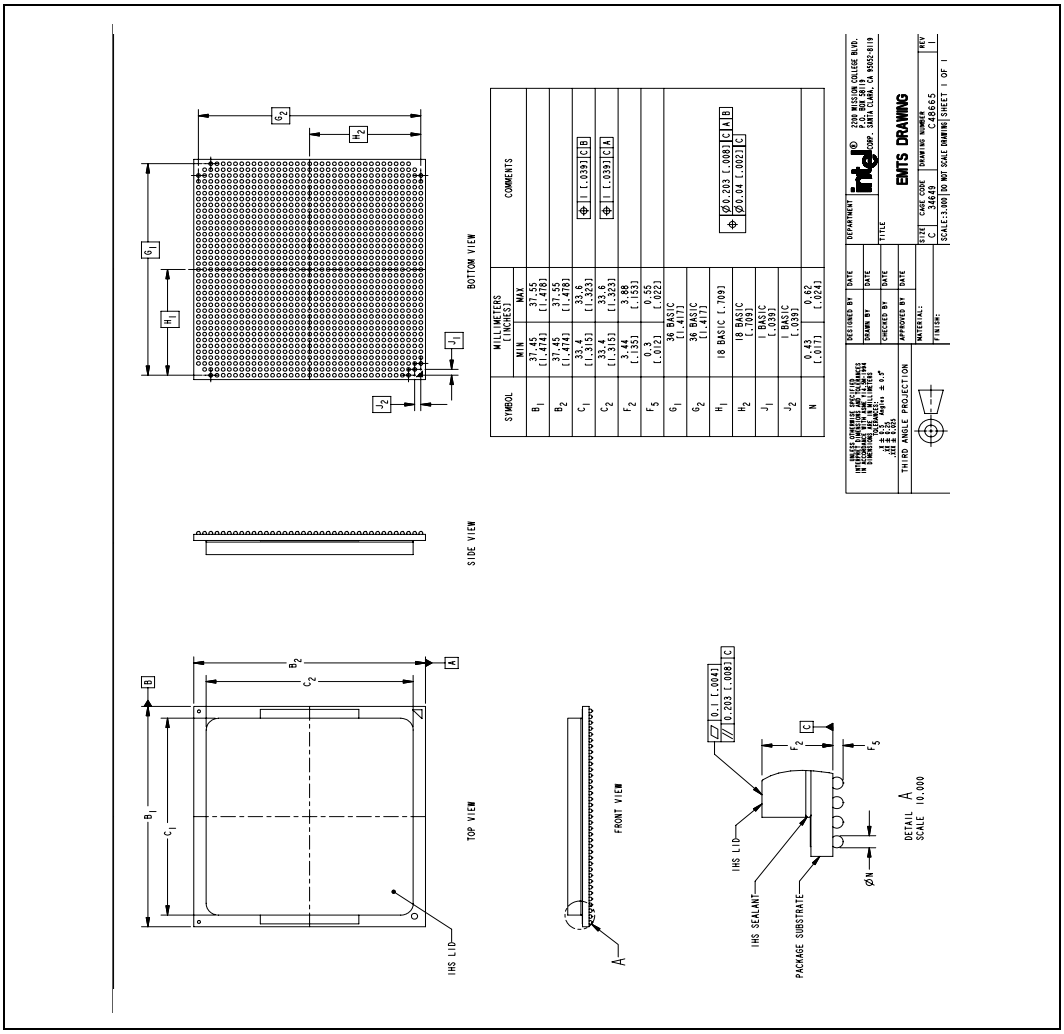
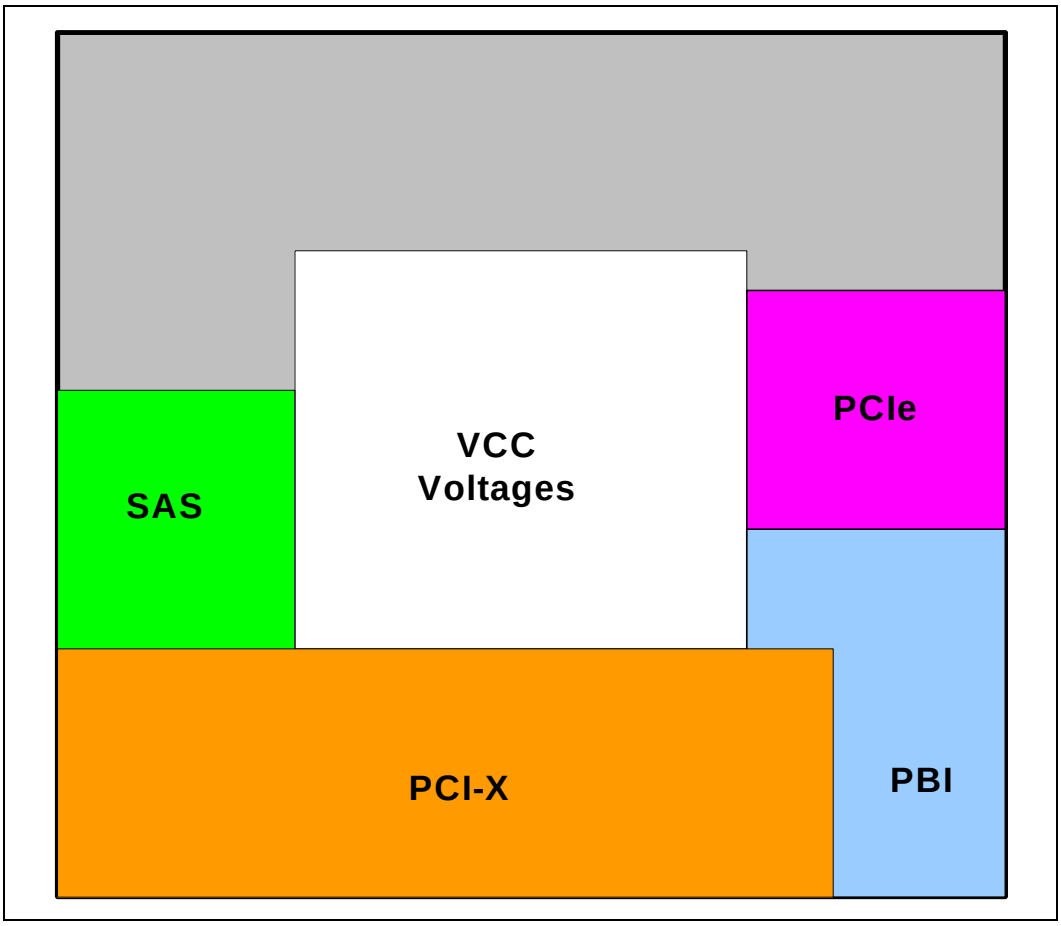


Figure 3. Top View Ball Map With Interfaces



3.0 Board Layout Guidelines

This chapter provides an example of a motherboard and a adapter card stackup implementation. This stackup was used for all simulations listed in this design guide. It is highly recommended that signal integrity simulations be conducted to verify each PCB layout. This is especially true when the layout deviates from the recommendations listed in these design guidelines.

3.1 Motherboard Stack Up Information

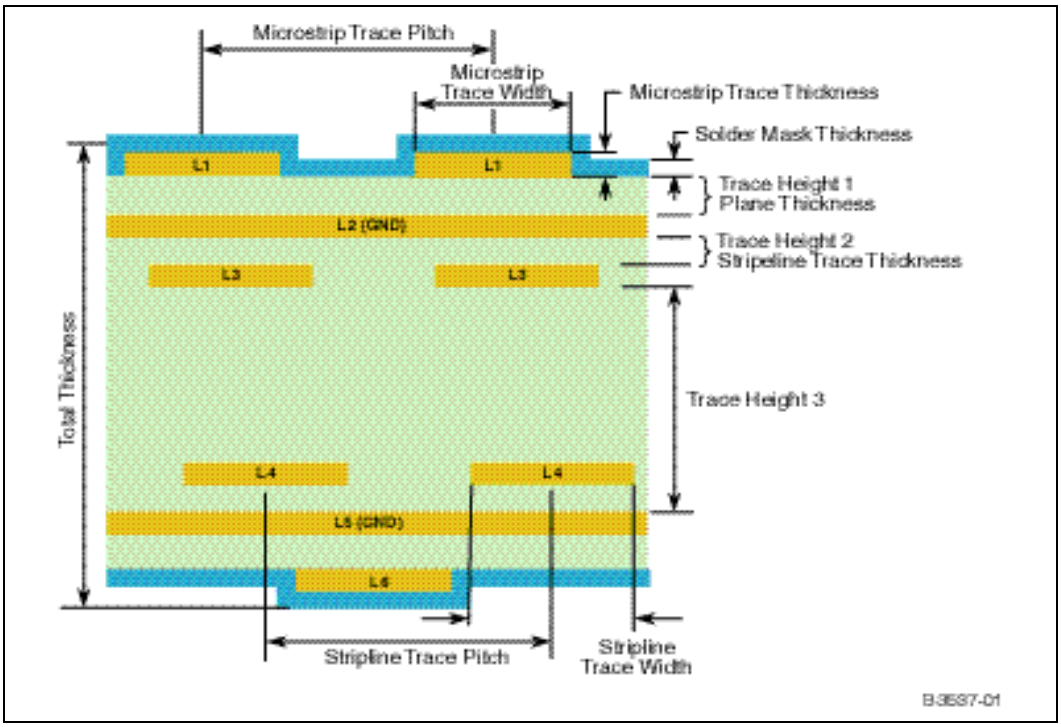
When the Intel® 413808 and Intel® 413812 I/O Controllers are used in server and workstation Raid On Mother Board (ROMB) applications, the motherboard is implemented on six layers. The specified impedance range for all board implementations is 50ohms +/-15%. Adjustments are made for interfaces specified at other impedances. Table 1 defines the typical layer geometries for a six layer board.

The motherboard impedance guidelines are based on the typical server/workstation impedance for their processor and memory subsystem of 50-ohms. Dimensions and tolerances for the motherboard are listed in Table 1. Refer to Figure 4 for location of variables in Table 1.

Table 1. Motherboard Stack Up, Stripline and Microstrip

Variable	Type	Nominal	Minimum	Maximum	Notes
Solder Mask Thickness (mil)	N/A	0.8	0.6	1.0	
Solder Mask E_r	N/A	3.65	3.65	3.65	
Core Thickness (mil)	N/A	9.8	9.6	10	
Core E_r	N/A	4.30	3.75	4.85	2113 material
Plane Thickness (mil)	Power	2.7	2.5	2.9	
	Ground	1.35	1.15	1.55	
Trace Height (mil)	1	3.5	3.3	3.7	The trace height is determined to achieve a nominal 50 ohms.
	2	3.5	3.3	3.7	
	3	10.5	9.9	11.1	
Preg E_r	Microstrip	4.30	3.75	4.85	
	Stripline1	4.30	3.75	4.85	
	Stripline2	4.66	4.19	5.13	
Trace Thickness (mil)	Microstrip	1.75	1.2	2.3	
	Stripline	1.4	1.2	1.6	
Trace Width (mil)	Microstrip	5.0	3.5	6.5	
	Stripline	4.0	2.5	5.5	
Trace Spacing (mil)	Microstrip	15.0	-	-	Each interface sets the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.
	Stripline	12.0	-	-	
Total Thickness (mil)	FR4	62.0	56.0	68.0	
Trace Velocity (ps/in)	Microstrip		135	141	Velocity varies based on variation in Er. It cannot be controlled during the fab process.
	Stripline		167	178	
Trace Impedance (ohms)	Microstrip	50	42.5	57.5	
	Stripline	50	45	55	

Figure 4. Motherboard Stackup Recommendations



3.2 Adapter Card Topology

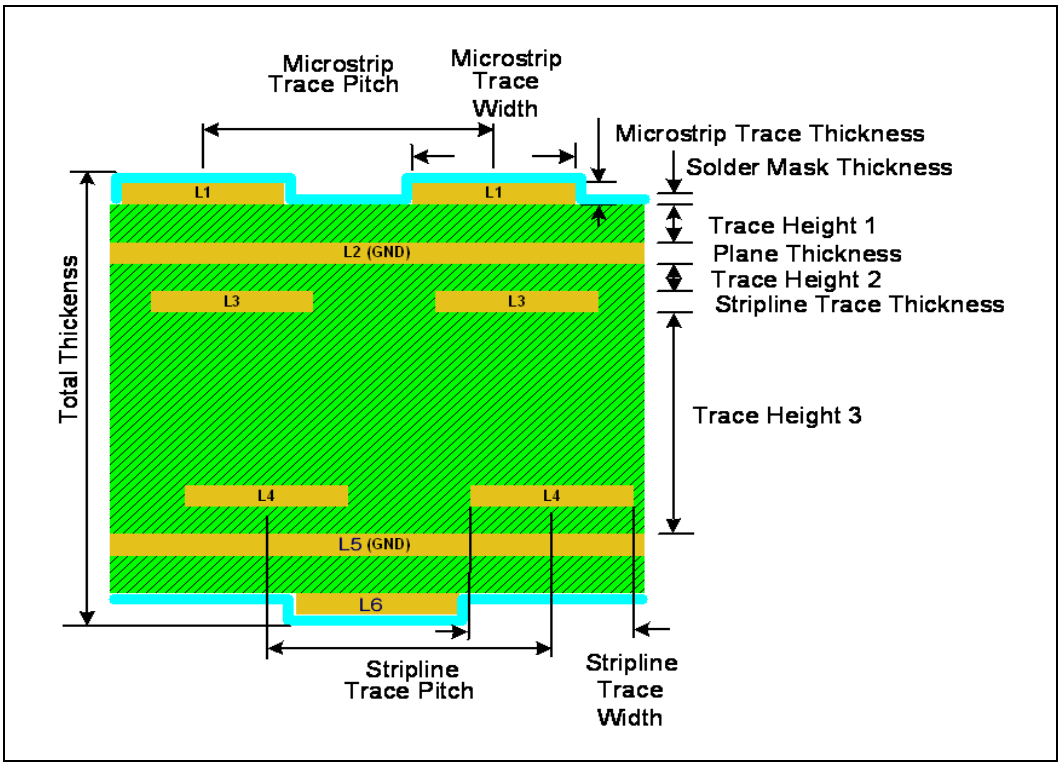
Intel® 413808 and Intel® 413812 I/O Controllers are implemented on PCI Express or PCI-X adapter cards with six layers. The specified impedance range for all adapter card implementations is 60ohms +/-15%. Table 2 defines the typical layer geometries for a six layer board. Note that the values are the same as the motherboard stack up with the exception of the impedance.

Table 2. Adapter Card Stack Up, Microstrip and Stripline

Variable	Type	Nominal	Minimum	Maximum	Notes
Solder Mask Thickness (mil)	N/A	0.8	0.6	1.0	
Solder Mask E_r	N/A	3.65	3.65	3.65	
Core Thickness (mil)	N/A	2.8	3.0	3.2	
Core E_r	N/A	4.3	3.75	4.85	2113 material
Plane Thickness (mil)	Power	2.7	2.5	2.9	
	Ground	1.35	1.15	1.55	
Trace Height (mil)	1	3.5	3.3	3.7	The trace height is determined to achieve a nominal 60 ohms.
	2	7.0	6.7	7.3	
	3	7.0	6.7	7.3	
Preg E_r	Microstrip	4.30	3.75	4.85	2113 material
	Stripline1	4.30	3.75	4.85	
	Stripline2	4.66	4.19	5.13	
Trace Thickness (mil)	Microstrip	1.75	1.2	2.3	
	Stripline	1.4	1.2	1.6	
Trace Width (mil)	Microstrip	4.0	2.5	5.5	
	Stripline	4.0	2.5	5.5	
Total Thickness (mil)	FR4	62.0	56.0	68.0	
Trace Velocity (ps/in)	Microstrip		135	141	Velocity varies based on variation in Er. It cannot be controlled during the fab process.
	Stripline		167	178	
Trace Impedance	Microstrip	60	51	69	
	Stripline	60	51	69	

Note: Each interface sets the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.

Figure 5. Adapter Card Stackup



3.3 PCB Impedance Targets

The below tables provide the impedance ranges and the associated trace dimensions for single-ended and differential traces. Figure 4 shows an example of a differential trace.

Table 3. Single-ended Trace Parameters

Single Line						
Topology	Ohms	Actual Impedance Range			Width (mils)	Spacing (mils)
		Min	Max	Nominal		
Stripline	50	44.17	57.47	50.82	4	N/A
Stripline	60	51.16	66.62	58.89	4	N/A
Microstrip	50	42.97	57.46	50.22	5	N/A
Microstrip	60	51.30	67.89	59.60	4	N/A

Table 4. Differential Trace Dimensions

Differential Pair						
Topology	Ohms	Actual Impedance Range			Width (mils)	Edge to edge Spacing (mils)
		Min	Max	Nominal		
Stripline	85	74.24	102.28	92	4	8
Stripline	100	87.06	121.84	100	4	8
Microstrip	85	71.56	119.36	88	5	7
Microstrip	100	80.36	114.28	100	4	8

4.0 PCI-X Layout Guidelines

This section provides an overview of the PCI-X layout recommendations based on Intel's presilicon simulation results. The results were compiled for a motherboard with 50 ohm impedance and an adapter card with 60 ohm impedance.

- Section 4.1 provides details on the PCI-X Frequency control.
- Section 4.2 provides the layout recommendations for each of the topologies and PCI-X speeds.

For more information on the PCI-X standard refer to *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0a on the www.pcisig.com website.

4.1 PCI/PCI-X Frequency Selection

Intel® 413808 and Intel® 413812 I/O Controllers can only function as an endpoint mode **PCIX_EP#** = 0 strap is set with a pull-down.

Figure 6 provides layout guidelines for locating the connections from the PCIXCAP pin on the card edge connector for an adapter card. With Intel® 413808 and Intel® 413812 I/O Controllers on an adapter card the P_PCIXCAP pin should be pulled-up with an 8.2K resistor.

Figure 6. P_PCIXCAP Layout Guidelines

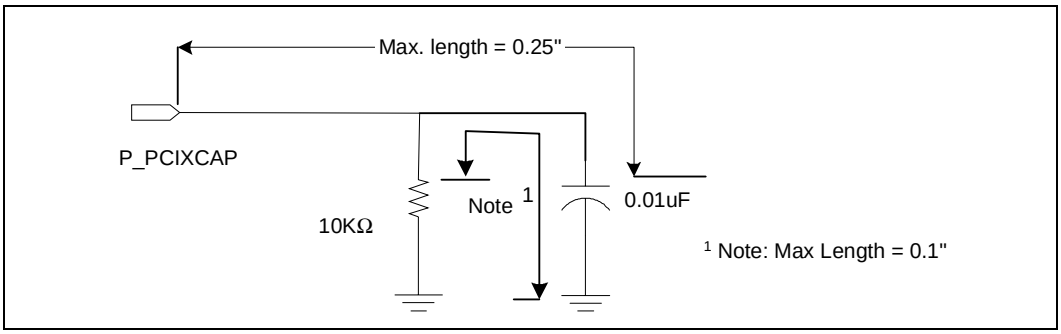


Table 5 describes the PCI-X bus mode and frequency initialization pattern. Intel® 413808 and Intel® 413812 I/O Controllers will decode this initialization pattern to determine the bus frequency.

Table 5. PCI-X Initialization Pattern

DEVSEL#	STOP#	TRDY#	Mode	Clock Period (ns)		Clock Frequency (MHz)	
				Max	Min	Min	Max
Deasserted	Deasserted	Deasserted	PCI 33	60	30	16	33
			PCI 66	30	15	33	66
Deasserted	Deasserted	Asserted	PCI-X	20	15	50	66
Deasserted	Asserted	Deasserted	PCI-X	15	10	66	100
Deasserted	Asserted	Asserted	PCI-X	10	7.5	100	133

4.2 PCI-X Layout Recommendations

This section provides the layout recommendations for PCI-X topologies in the following subsections:

- Section 4.2.1, "PCI-X Clock Routing"
- Section 4.2.2, "133 MHz One Slot Topology"
- Section 4.2.3, "Embedded 133 MHz Topology"
- Section 4.2.4, "Mixed 133 MHz Topology"
- Section 4.2.5, "100 MHz Two Slot Topology"
- Section 4.2.6, "Embedded 100 MHz Topology"
- Section 4.2.7, "Mixed 100 MHz Topology"
- Section 4.2.8, "66 MHz PCIX Four Slot Topology"
- Section 4.2.9, "Embedded 66 MHz Topology"
- Section 4.2.10, "Mixed 66 MHz Topology"

4.2.1 PCI-X Clock Routing

This section lists general recommendations for routing the PCI-X clock to the Intel® 413808 and Intel® 413812 I/O Controllers PCI-X clock input.

Table 6. PCI-X Clock Layout Guidelines

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane.
Recommended Layer	Stripline
Trace Impedance: Motherboard	Microstrip: 50 ohm +/- 15%, stripline: 50 ohm +/- 10%
Trace Impedance: Adapter Card	Microstrip or stripline: 60 ohm +/- 15%
Trace Spacing (edge to edge)	• between two different clock lines ≥ 25 mils • between two segments of the same clock line≥ 25 mils • between clock and other signals ≥ 50 mils
Series Resistors	28 ohms 1% for an adapter card with a connector 26 ohms 1% for embedded (device to device)
Trace Length TL1 from clock input to the resistor	1.0" max
Total Trace Length: from device ball to device (including resistor segment)	11" max
Length Matching:	Match all clock lines to within 0.25 mils
Vias	≤ 2 vias

4.2.1.1 Point-to-Point Signals (REQ#/GNT#)

This section provides the layout guidelines for REQ# and GNT# lines. Topology in Figure 7 for 133MHz slot design is the same as the one used for point-to-point signals.

Table 7. PCI-X REQ#/GNT# Layout Guidelines

Parameter	Routing Guidelines
Signal Group	REQ# and GNT# lines
Reference Plane	Route over unbroken reference plane.
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline
Motherboard Trace Spacing	14 mils microstrip and 12 mils stripline
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline
Group Spacing: Spacing from other groups	25 mils minimum, edge to edge
Trace Length TL1 - from buffer to the connector	• 0.5″ min to 4.5″ max for 133MHz • 0.5″min to 12.0″ max for 100MHz • 0.5″ min to 15.0″ max for 66MHz
Trace Length TL2 - from connector to the receiver	2.4″ - 2.6″ max
Vias	≤ 3 vias

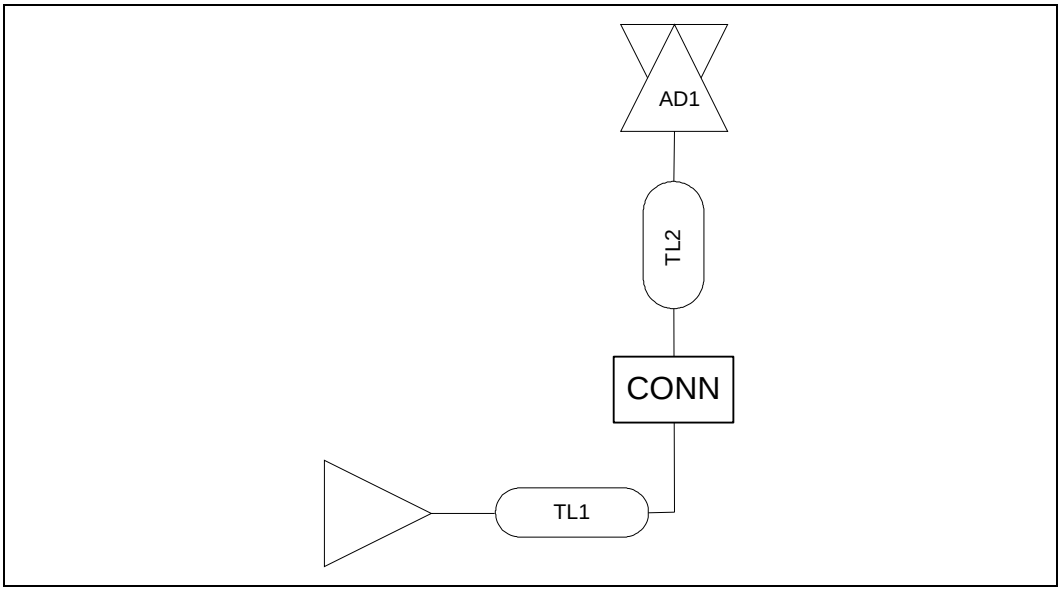
4.2.2 133 MHz One Slot Topology

This section lists the parameters used for the address/data and control lines for 133 MHz single slot design.

Table 8. 133 MHz Single-Slot Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	14 mils microstrip 12 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	14 mils microstrip and stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the connector	1.0" - 6.0" max	0.5" - 5.0" max
Trace Length TL2 - from connector to the receiver	0.75" - 1.5" Max	1.75" - 2.75" Max
Vias	< 3 vias	

Figure 7. 133 MHz One Slot Topology



4.2.3 Embedded 133 MHz Topology

This section lists the parameters used for the address, data and control signals for 133 MHz embedded design with two embedded devices.

Figure 8. Embedded 133 MHz Topology

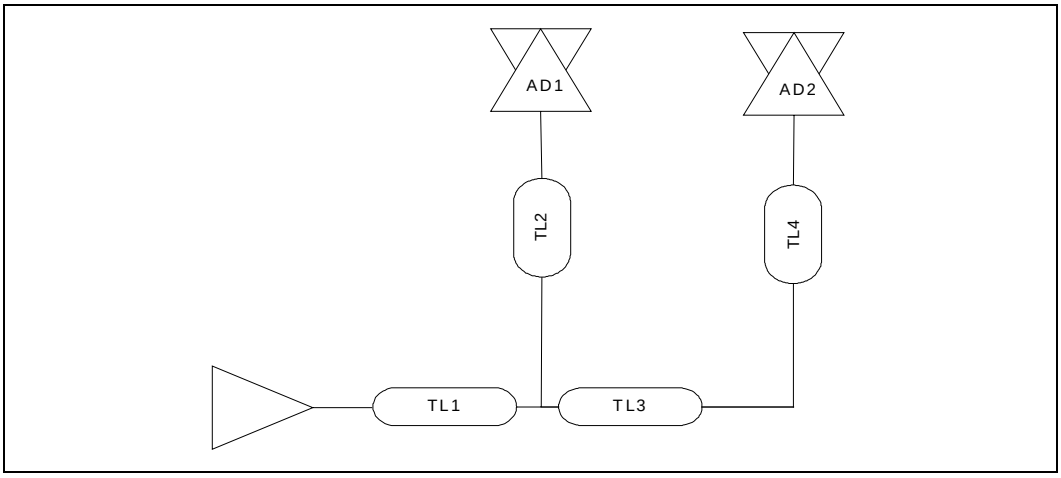


Table 9. Embedded 133 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (Stripline	50 ohm +/- 10%	
Motherboard Trace Spacing	14 mils microstrip, 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from ball to the junction	0.75" min. to 2.5" max	
Trace Length TL3 - from junction to junction	0.75" min. to 2.5" max	
Trace Length TL2, TL4, from junction to receiver	0.75" min. to 2.5" max	
Vias	< 3 vias	

4.2.4 Mixed 133 MHz Topology

This section lists the parameters used for the address, data and control signals for 133 MHz embedded design with one embedded load and one connector.

Figure 9. Mixed 133 MHz Topology

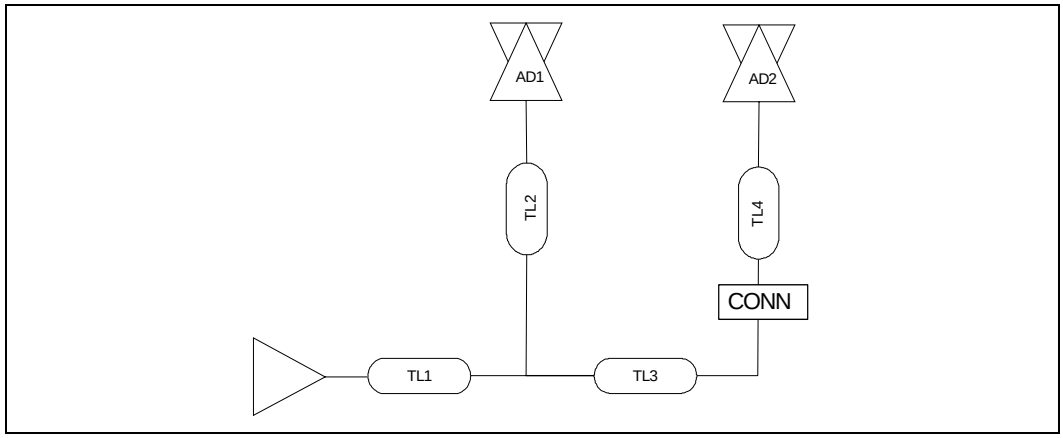


Table 10. Mixed 133 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.0″ max	0.5″ min. to 2.0″ max
Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	0.5″ min. to 2.0″ max
Trace Length TL3, from junction to CONN	0.5″ min. to 3.5″ max	0.5″ min. to 2.25″ max
Trace Length TL4, from CONN to adapter	0.75″ min. to 1.5″ max	1.75″ min. to 2.75″ max
Vias	< 3 vias	

4.2.5 100 MHz Two Slot Topology

This section lists the parameters used for the address, data and control signals for 100 MHz. This topology is shown in Figure 10.

Figure 10. 100 MHz Dual Slot Topology

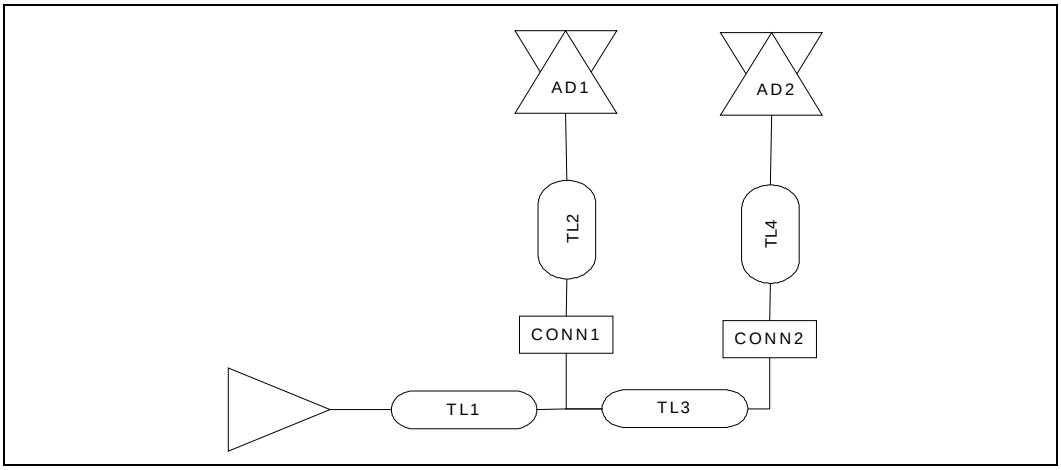


Table 11. 100 MHz Two Slot Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from ball to the connector	0.5″ - 12.0″ max	0.5″ - 10.0″ max
Trace Lengths TL3 - Between connectors	0.5″ - 3.0″ max	0.5″ - 3.0″ max
Trace Lengths TL2 - from connector to the first receiver, TL4 - from connector to the second receiver	0.75″ - 1.50″ max	1.75″ - 2.75″ max
Vias	< 3 vias	

4.2.6 Embedded 100 MHz Topology

This section lists the parameters used for the address, data and control signals for 100 MHz embedded design with five embedded loads.

Figure 11. Embedded 100 MHz Topology

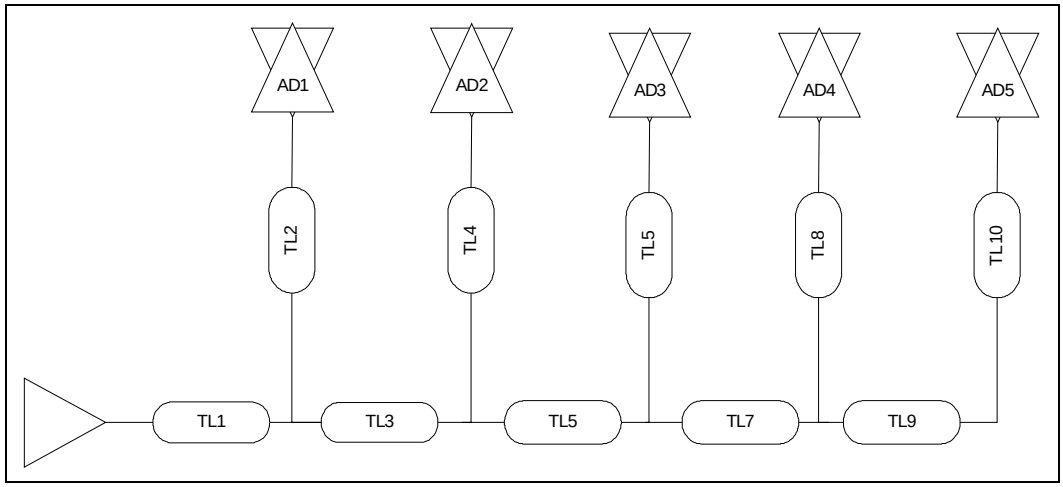


Table 12. Embedded 100 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Group Spacing	spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5" min. to 3.0" max (3 loads, 5 loads)	
Trace Length TL3, TL5, TL7, TL9: from junction to junction	0.5" min. to 2.0" max (3 loads) 0.5" min. to 1.0" max (5 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10: from junction to receiver	0.5" min. to 3.0" max (3 loads) 0.5" min to 2.0" max (5 loads)	
Vias	≤ 4 vias	

4.2.7 Mixed 100 MHz Topology

This section lists the parameters used for the address, data and control signals for 100 MHz embedded design with one embedded load and two connectors.

Figure 12. Mixed 100 MHz Topology

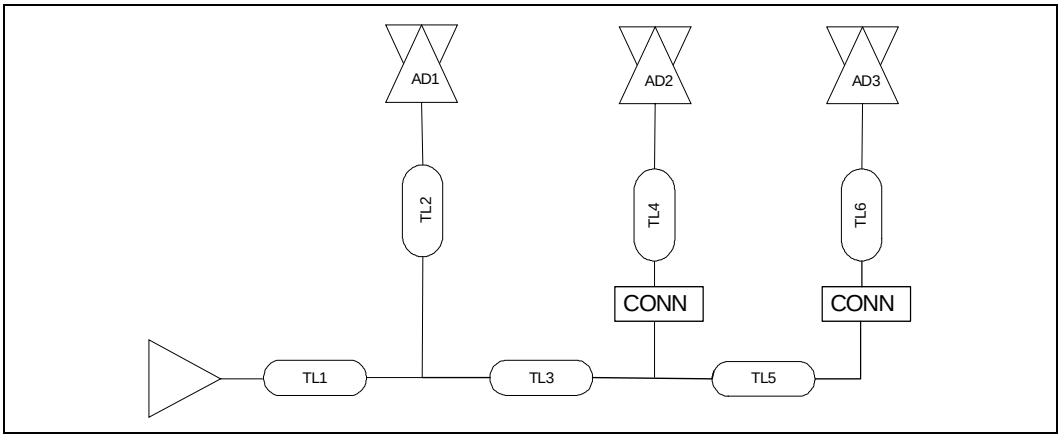


Table 13. Mixed 100 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.5″ max	0.5″ min. to 2.5″ max
Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	0.5″ min. to 2.0″ max
Trace Length TL3, from junction to first CONN	0.5″ min. to 3.5″ max	0.5″ min. to 3.0″ max
Trace Length TL5, from 1st CONN to 2nd CONN	0.5″ min. to 3.5″ max	0.5″ min. to 3.5″ max
Trace Length TL4, from 1st CONN to AD2 Trace Length TL6, from 2nd CONN to AD3	0.75″ min. to 1.5″ max	1.75″ min. to 2.75″ max
Vias	≤ 3 vias	

4.2.8 66 MHz PCIX Four Slot Topology

This section lists the parameters used for the address, data and control signals for 66 MHz. This topology is shown in Figure 13.

Figure 13. 66 MHz Four Slot Topology

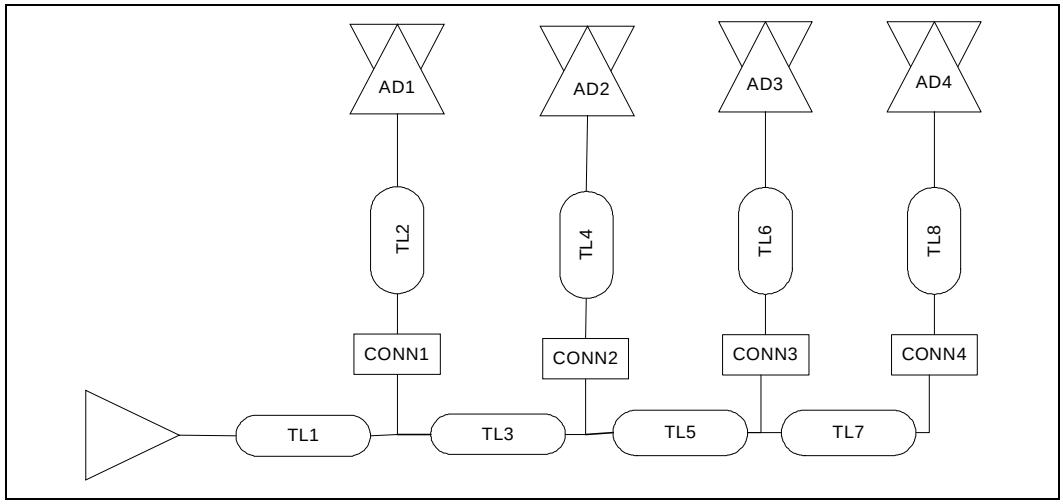


Table 14. 66 MHz Four Slot Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	12 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from ball to the connector	0.5" - 12.0" max	0.5" - 9.0" max
Trace Lengths TL3, TL5, TL7 - Between connectors	0.5" - 2.0" max	0.5" - 2.0" max
Trace Lengths TL2, TL4, TL6, TL8- from connector to the receivers	0.75" - 1.50" max	1.75" - 2.75" max
Vias	≤ 4 vias	

4.2.9 Embedded 66 MHz Topology

This section lists the parameters used for the address, data and control signals for 66 MHz embedded design with 8 embedded loads.

Figure 14. Embedded 66 MHz Topology

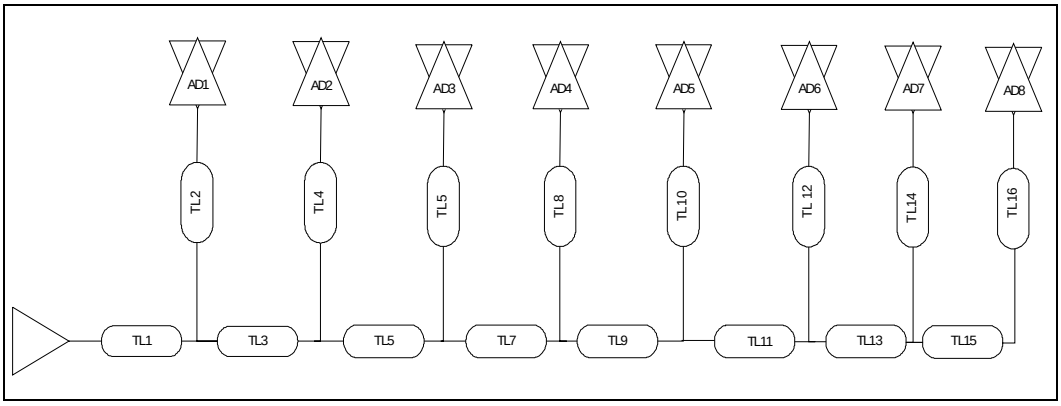


Table 15. Embedded 66 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5" min. to 3.0" max (8 loads) 0.5" min. to 3.5" max (6 loads)	
Trace Length TL3, TL5, TL7, TL9,TL11,TL13,TL15: from junction to junction	0.5" min. to 1.5" max (8 loads) 0.5" min. to 2.5" max (6 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10,TL12,TL14,TL16: from junction to receiver	0.5" min. to 1.5" max (8 loads) 0.5" min to 2.0" max (6 loads)	
Vias	≤ 4 vias	

4.2.10 Mixed 66 MHz Topology

This section lists the parameters used for the address, data and control signals for 66 MHz embedded design with one embedded load and two connectors.

Figure 15. Mixed 66 MHz Topology

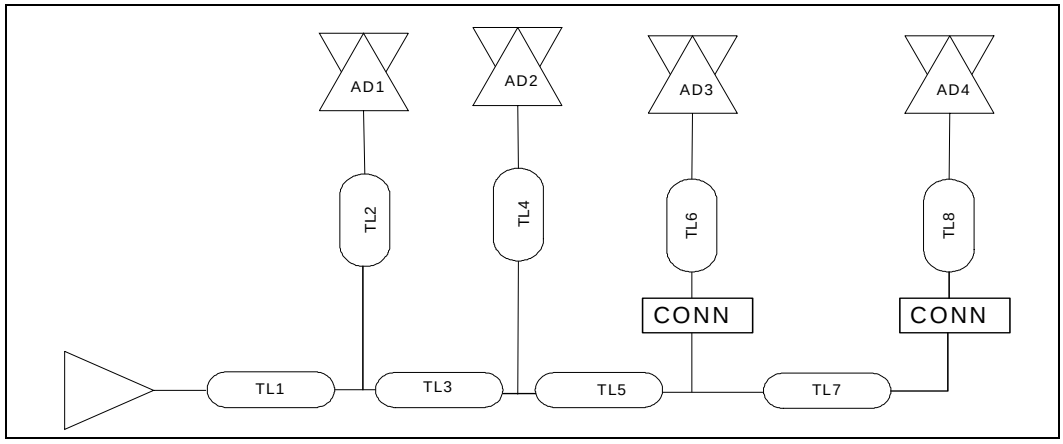


Table 16. Mixed 66 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	12 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5″ min. to 11″ max	0.5″ min. to 10″ max
Trace Length TL2, TL4 - from junction to AD1, AD2	0.5″ min. to 4.5″ max	0.5″ min. to 4.0″ max
Trace Length TL3, TL5, TL7 from junction to junction	0.5″ min. to 4.0″ max	0.5″ min. to 4.0″ max
Trace Length TL6 from 1st CONN to AD3, TL8: from 2nd CONN to AD4	0.75″ min. to 1.5″ max	1.75″ min. to 2.75″ max
Vias	≤ 4 vias	

4.2.11 Additional PCI Layout Notes

- The **P_INT[D:A]#** signals do not have any length restrictions.
- When **PCIX_PULLUP#** is pulled-low, it enables internal pull-ups on the following PCI signals: **P_AD[63:32]**, **P_C/BE[7:4]#**, **P_PAR64**, **P_REQ64#**, **P_ACK64#**, **P_FRAME#**, **P_IRDY#**, **P_TRDY#**, **P_STOP#**, **P_DEVSEL#**, **P_SERR#**, **P_INT[D:A]#**, and **P_PERR#**.
- If application requires external pull-ups on the upper P_AD bus make sure that the location of the pull-up is less than ≤ 1″ from the ball.

5.0 PCI Express Layout

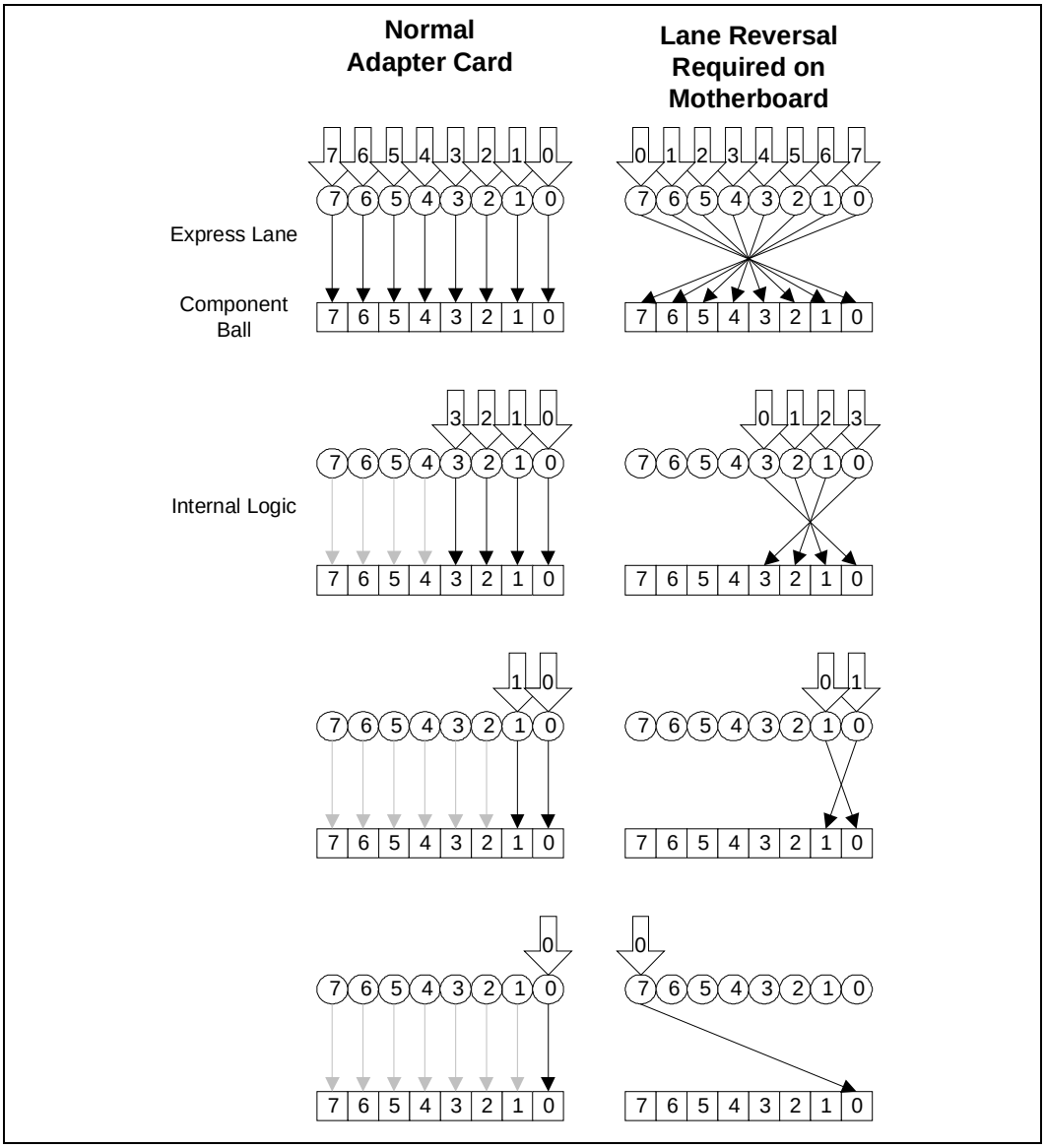
This section provides an overview of the PCI Express layout recommendation based on simulation results. PCI Express is a serial differential low-voltage point-to-point interconnect. The PCI Express was designed to support 20 inches between components with standard FR4.

For more information on the PCI Express standard refer to PCI Express Base Specification 1.0a and the *PCI Express Card Electromechanical Specification*, revision1.0a, found on the http://www.pcisig.com/home website.

5.1 Optional PCI Express Lane Reversal

The following Figure 16 describes the lane reversal which can be considered when you are designing a PCI-E x8 motherboard slot or an adapter card to improve PCB routing. Note that the adapter card PCI-E pins map with a straight through connection but the motherboard can implement lane reversal in x8, x4, x2 and x1 configurations as shown in Figure 16.

Figure 16. PCI Express Lane Reversal To Improve PCB Routing



5.2 PCI Express Layout recommendations

The following recommendations are summarized based on our presilicon simulation results for the following topologies:

1. motherboard topology with the PCI Express device on the board Section 5.2.1.
2. motherboard topology with a PCI Express connector and an adapter card topology with the device on the card Section 5.2.2.

The PCI Express clock layout recommendations are listed in Section 5.2.3.

5.2.1 PCI Express Motherboard Layout Guidelines

The following layout recommendations were determined for a motherboard application with the PCI Express device on the board.

Figure 17. Motherboard Topology

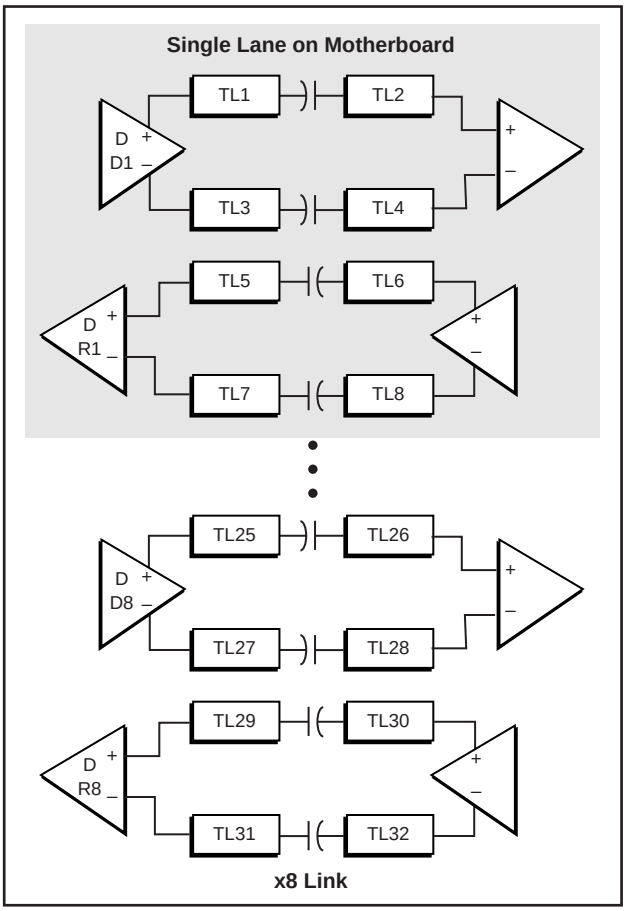


Table 17. PCI Express Layout for a Motherboard

Parameter	Routing Guidelines
Signal Group	Transmit and receive differential pairs
Reference Plane	Routing over unbroken ground plane is preferred. If unbroken ground plane is not available, route over unbroken voltage plane.
Characteristic Trace Impedance:	Single-ended: 50 ohms +/- 15% Differential: 85 ohms nominal +/-15%
Microstrip Trace Width	5 mils (Refer to Table Note)
Microstrip Trace Spacing	• Between + (P) and - (N) of pair: 7 mils edge to edge • Between other signals: ≥ 25 mils edge to edge • Transmit and receive pairs should be interleaved. If interleaving is not possible, then the spacing between pairs (inter pair) should be increased to ≥ 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of Positive of one pair to edge of Negative of the next pair or vice versa.
Stripline Trace Width	5 mils (Refer to Table Note below)
Stripline Trace Spacing	• Between + (P) and - (N) of pair: 7 mils edge to edge • Between other pairs : ≥ 25 mils edge to edge • Transmit and receive pairs should be interleaved. If interleaving is not possible, then inter pair spacing should be increased to 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of Positive of one pair to edge of Negative of the next pair or vice versa.
Group Spacing	Spacing from other groups: > 25 mils minimum from edge to edge for microstrip or stripline.
AC Coupling	AC Coupling capacitors must be located at the transmitter. Required values of 75 nF to 200 nF.
Total Trace Length - (Transmitter/Receiver) from device signal pin to AC coupling capacitor and AC coupling capacitor to PCI Express device pin	1.0″ min. - 30.0″ max
Length Matching Requirements	• Total allowable between pair (length skew between + and - signals of the pair) length mismatch on a system board must not exceed 10 mils. • Length should be matched on a segment by segment basis. • Each routing segment to be matched as close as possible. • Total skew across all lanes must be less than 20 ns.
Number of Vias	4 max

Note: Width and Intra Pair (length skew between + and - signals of the pair) spacing recommendations need not be strictly adhered to, but it is very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.

5.2.2 PCI Express Layout Motherboard-Adapter Card Guidelines

This section provides the routing guidelines for the motherboard-adapter card topology as shown in Figure 18. Table 18 provides the routing guidelines for a motherboard with a PCI Express connector on it and the routing guidelines for an adapter card.

Figure 18. Motherboard-Adapter Card Topology

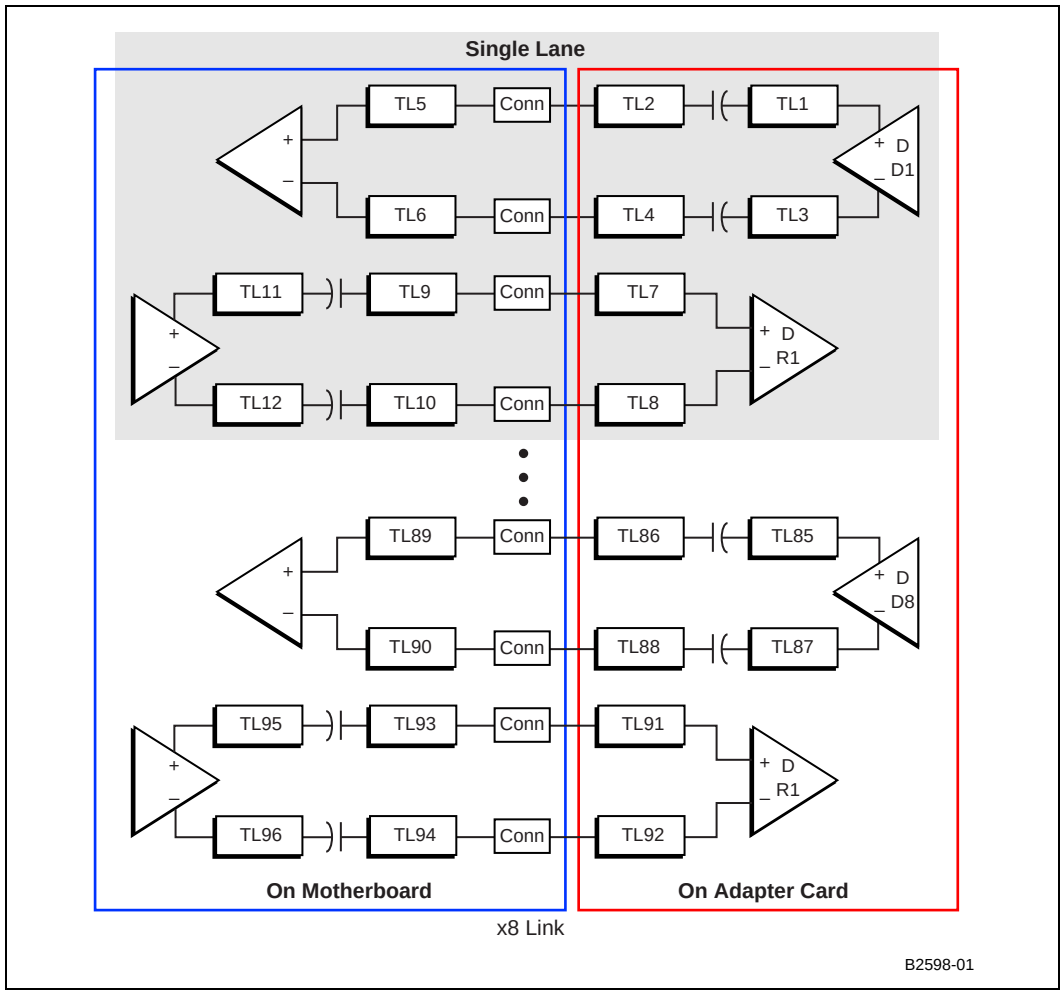


Table 18. PCI Express Layout for Motherboard-Adapter Card Topology

Parameter	Routing Guidelines
Signal Group	Transmit and Receive differential pairs
Reference Plane	Routing over unbroken ground plane is preferred. If unbroken ground plane is not available route over unbroken voltage plane.
Characteristic Trace Impedance motherboard	Single Ended: 50 +/-15% ohms nominal
	Differential: 85 +/-15% ohms nominal
Characteristic Trace Impedance adapter card	Single Ended: 60 +/-15% ohms nominal
	Differential: 100 +/-15% ohms nominal
Microstrip Trace Width	5 mils
Microstrip Trace Spacing	• Between intra-pair (between + (P) and - (N) of pair): 7 mils edge to edge (see Table Note) • Between other pairs : ≥ 25 mils edge to edge • Transmit and receive pairs should be interleaved. If interleaving is not possible, then the spacing between pairs (inter pair) should be increased to ≥ 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of the positive of one pair to edge of negative of the next pair or vice versa
Stripline Trace Width	5 mils (see Table Note)
Stripline Trace Spacing	• Between + (P) and - (N) of pair: 7 mils edge to edge • Between other pairs: ≥ 25 mils edge to edge • Transmit and Receive pairs should be interleaved. If interleaving is not possible, then inter pair spacing should be increased to 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of the positive of one pair to edge of negative of the next pair or vice versa
Group Spacing	Spacing from other groups: > 20 mils minimum from edge to edge for microstrip or stripline.
AC Coupling	AC Coupling capacitors must be located at the transmitter. Required value of 75 nF to 200 nF.
Total Length: Topology 1: from device signal pin transmitter on motherboard with PCI-E device receiver on adapter card	1.0″ min. - 27″ max
Total Length: Topology 2: from device signal pin transmitter on adapter card and the PCI-E device receiver on motherboard.	1.0″ min. - 25″ max
Length Matching Requirements	• Total allowable intra-pair (length skew between + and - signals of the pair) trace mismatch for a lane that must not exceed 15 mils for the motherboard-adapter card combination (10 mils for the motherboard, 5 mils for the adapter card). • Length should be matched on a segment by segment basis. • Total skew across all lanes must be less than 20 ns.
Number of Vias	4 max

Note: Width and Intra Pair Spacing (between + (P) and - (N) of pair) recommendations need not be strictly adhered to, but it is very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.

5.2.3 Clock Routing Guidelines

This section provides routing guidelines for the PCI Express Clocks in an application. The *PCI Express Card Electromechanical Specification Rev 1.0a* states in that any terminations required by the clock are to be on the system board.

The termination in Figure 19 would only be required on the system board if these resistors were not already provided.

- PCI Express adapter cards do not have to add Rs and Rt termination resistors.

Figure 19. PCI Express Clock Routing Topology

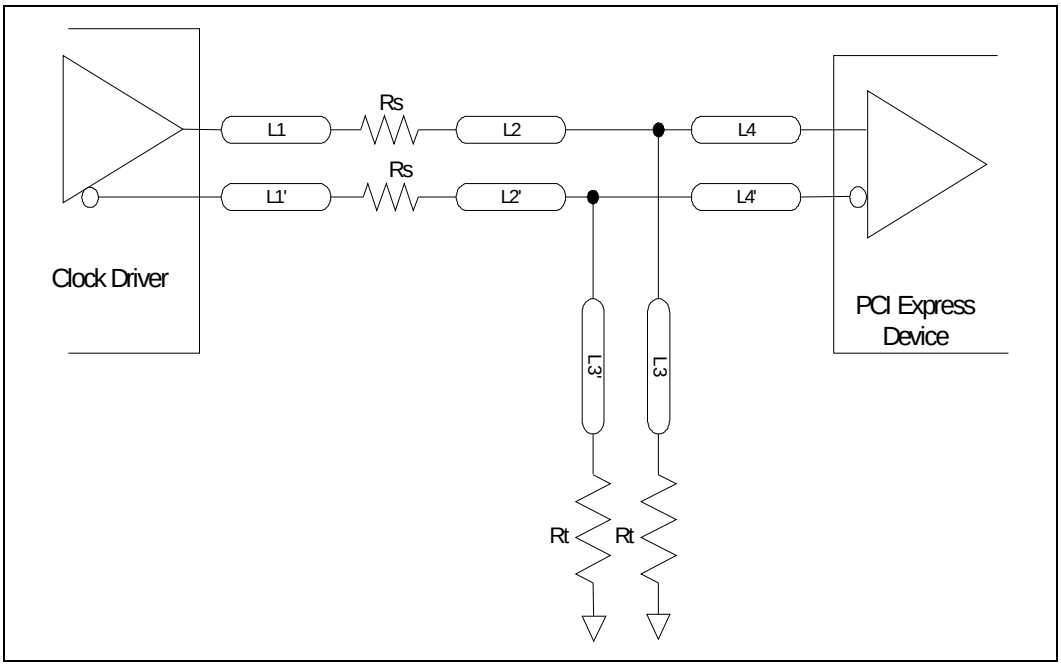


Table 19. PCI Express Layout for Clock Routing

Parameter	Routing Guidelines
Signal Group	REFCLKP, REFCLKN differential pairs
Reference Plane	Routing over unbroken ground plane is preferred. If unbroken ground plane is not available route over unbroken voltage plane.
Characteristic Trace Impedance	Single Ended: 50 +/-15% ohms nominal
	Differential: 100 +/-15% ohms nominal
Trace Width[1]	5 mils (see Table Note 2)
REFCLKP, REFCLKN differential clock Pair Spacing	< 1.4 x Space Width
Serpentine Spacing (spacing of a clock lines from itself)	> 25 mils
Clock to Other Signal Spacing	> 25 mils
Trace Lengths[2]	L1, L1': 0.5" max
	L2, L2': 0.2" max
	L3, L3': 0.2" max
	L4, L4' • Device down: 2" to 15.3" or • Connector: 2" to 11.3
	Total Length = L1+L2_+L4 • Device Down: 3" to 16" or • Connector: 3" to 12"
Length Matching Requirements within differential pair	+/- 5 mils
Rs Series Resistors	33 +/- 5%
Rt Shunt Resistors	49.9 +/- 1%
Number of Vias	4 max

Notes:

1. Termination resistors are only required on system boards if not already present. Adapter cards do not require Rs and Rt resistors)
2. Width and Intra Pair Spacing recommendations need not be strictly adhered to, but it is very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.

6.0 SATA/SAS Bus Layout

This section provides an overview of the SAS and SATA layout recommendations. Due to the fact that the SAS standard supports the interoperability with SATA devices, the layout guidelines for SAS listed in this section are valid for SATA as well.

6.1 SAS/SATA General Recommendations

SATA is a serial differential point-to-point interconnect. For more information on the SATA standard refer to Serial ATA Specification 2.5 found at the www.serialata.org website.

SAS is also a serial differential low-voltage point-to-point interconnect. For more information on the SAS standard, refer to *Serial Attached SCSI 1.1* found at the www.t10.org website.

The analysis was performed for SAS compliant implementations. For more details on meeting the transmitter, receiver compliance and the transfer function (TCTF) refer to the SAS specification.

- Refer to the Table 20 for the for SAS compliant guidelines.
- The SAS inter-enclosure topology is shown in Figure 20 shown with an external cable connecting to a external storage system.
- A SAS intra-enclosure topology is shown in Figure 21 with a connection through the backplane to SAS drives. The intra-enclosure topologies also includes the storage controller directly attaching to the SAS drives.
- Table 21 provides maximum parallel lengths to minimize crosstalk effects.

Figure 20. SAS Inter-enclosure Topology

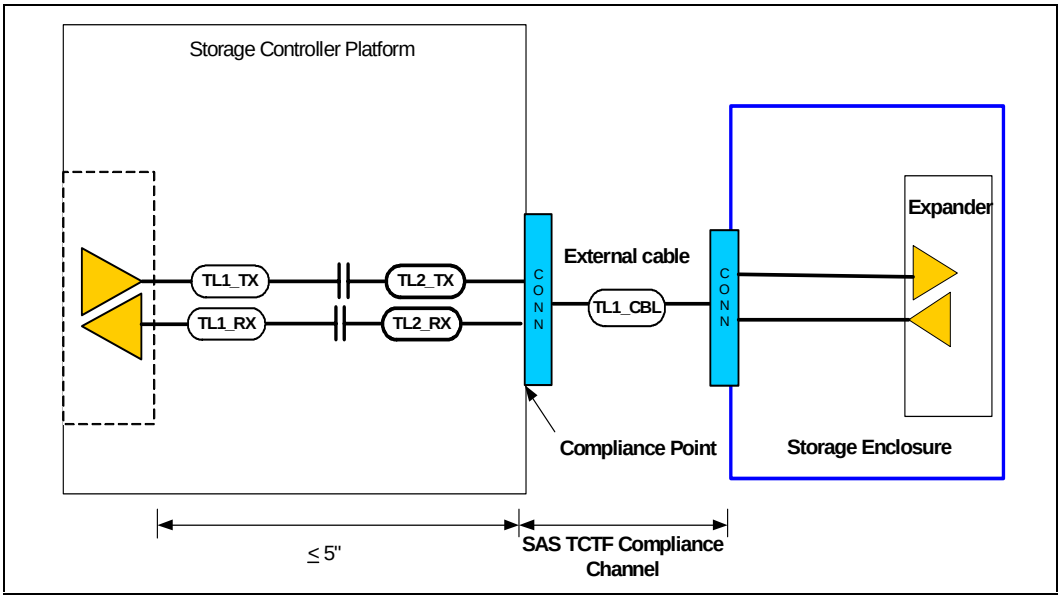


Figure 21. SAS Intra-enclosure Topology

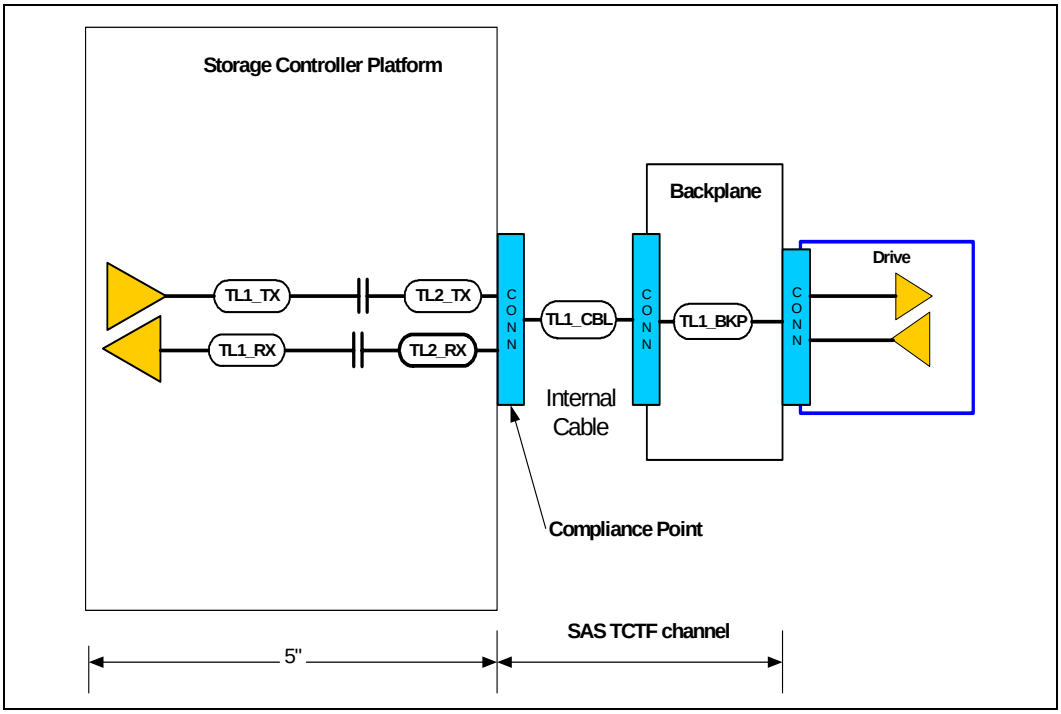


Table 20. SAS Compliant Guidelines

Parameter	Routing Guidelines
Signal Group	**S_TXP[7:0]**, **S_TXN[7:0]**, **S_RXP[7:0]**, **S_RXN[7:0]** Transmit and Receive differential pairs
Reference Plane	Unbroken ground plane preferred
Trace Impedance	100 ohms +/- 15% differential motherboard and adapter card
Trace Spacing	• breakout: SAS pair to pair spacing 20 mils ≤ 0.5" of the device ball • ≥ 50 mils from other types of signals • Refer to Table 20 for interpair spacing recommendations
Group Spacing (edge to edge)	• Keep SAS signals ≥ 50 mils away from the other types of signals. • SAS pair to pair spacing may be reduced to ≥ 20 mils in the breakout region within 0.5" of the pin field as necessary
Maximum trace length: Motherboard or Add-in card (Intel®81348 I/O Processor ball to first connector (compliance point))	≤ 5" (max)
Length Matching requirements intrapair (with differential pair)	• Must be matched to within 0.025 inches • Maintain consistent spacing between P and N signals for achieving differential trace impedance (takes precedence over length matching)
AC Coupling on TX+, TX- and RX+, RX-	• 10 nF with low ESR and ESL. • As close to the TX pad as possible
Vias	• Board thickness 0.062 inches max for though hole vias. • Drill width 20mils • No more than 2 vias per signal between device package ball and connector pin • Note: Reducing the number of vias takes precedence over the AC capacitor placement. • Impedance controlled vias (100% +/-15%) preferred

Table 21. Interpair (Between Pair) Spacing Requirements

Parallel Routed Length Next to Each Other	Microstrip/Stripline	Spacing Recommendation Between Lanes (edge to edge in mils)
0 - 2"	Microstrip	25
2 - 5"	Microstrip and Stripline	30

7.0 Peripheral Local Bus

This section provides the layout guidelines for the Peripheral Bus Interface Unit (PBI) of the Intel® 413808 and Intel® 413812 I/O Controllers. The PBI bus is commonly used to interface flash components to the Intel® 413808 and Intel® 413812 I/O Controllers Peripheral Bus.

The PBI unit includes two chip enables. The PBI chip enables activate the appropriate peripheral device when the address falls within one of the PBIs two programmable address ranges. Each chip enable can support up to 32 MBytes of addressability.

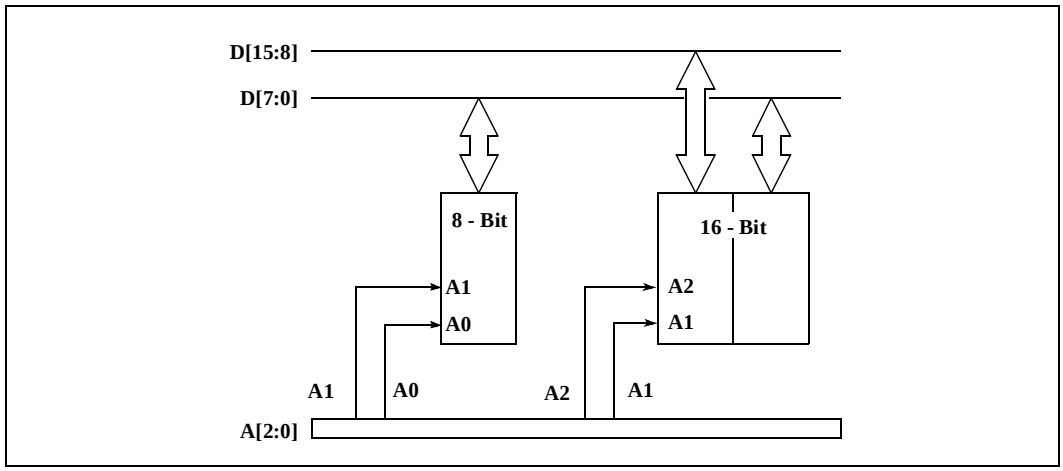
7.1 Peripheral Bus Signals

Bus signals consist of three groups: address A[24:0], data D[15:0], and control/status lines POE#, PWE#, PCE[1:0], PB_RSTOUT#.

7.2 PBI Bus Width

The PBI allows an 8-, or 16-bit data bus width for each range. The PBI places 8- and 16-bit data on low-order data signals, simplifying the interface to narrow bus external devices. As shown in Figure 22, 8-bit data is placed on lines **D[7:0]**; 16-bit data is placed on lines **D[15:0]**.

Figure 22. Data Width and Low Order Address Lines



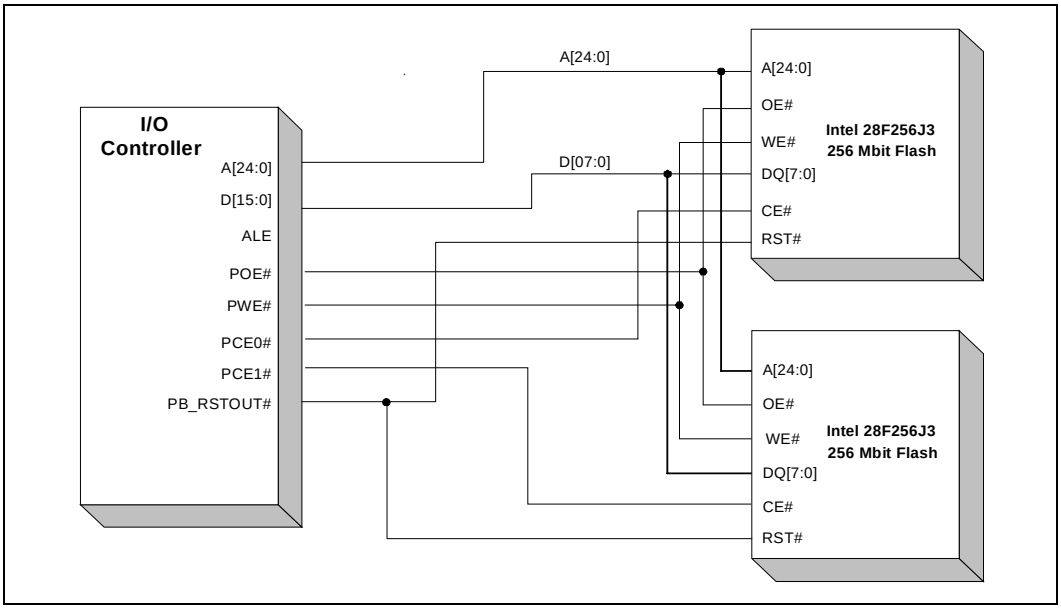
The user needs to wire up the flash memories in a manner consistent with the programmed bus width:

- 8-bit region: **A[1:0]** provide the demultiplexed byte address for a read burst.
- 16-bit region: **A[2:1]** provide the demultiplexed short-word address for a read burst.

7.3 Flash Memory Support

PBI peripheral bus interface supports 8-, or 16- bit Flash devices. Figure 23 shows two 8-bit flash devices would connect with the Intel® 413808 and Intel® 413812 I/O Controllers through the PBI Interface.

Figure 23. Sixty-Four Mbyte Flash Memory System



7.4 PBI Topology Layout Guidelines

This section provides the topologies for routing the Address and Data bus for single load, double load and three load topologies. Note that no length matching is required between the Address and Data lines.

Figure 24. Peripheral Bus Single Load Topology

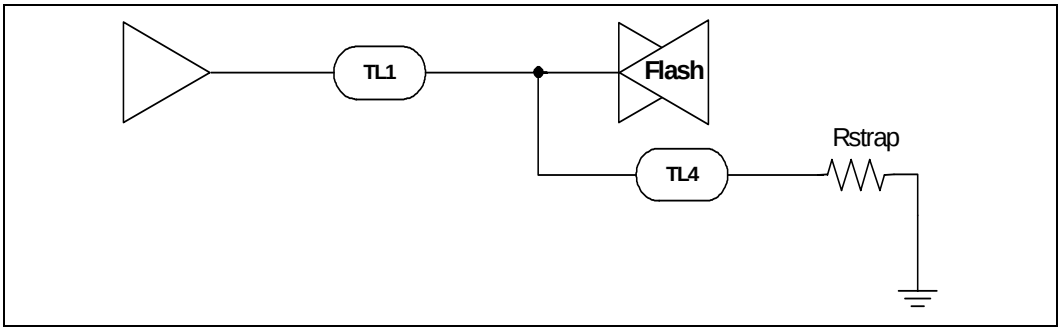


Table 22. PBI Routing Guideline Single Load

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or unbroken power plane. If routing over power plane maintain this consistency throughout the topology.
Routing	Microstrip or stripline or combination of microstrip and stripline.
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (edge to edge)	• ≥ 5 mils between all Address and Data lines • ≥ 20 mils must be maintained from all other signals or vias (for 5 mils trace width)
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Trace Length TL1	0" to 20.0"
Trace Length to strapping resistors TL4	0.5" to 3.0" from the last device on the bus.
Routing Recommendations	Number of vias ≤ 8
Routing Recommendations	Route as Daisy Chain

Figure 25. Peripheral Bus Dual Load Topology

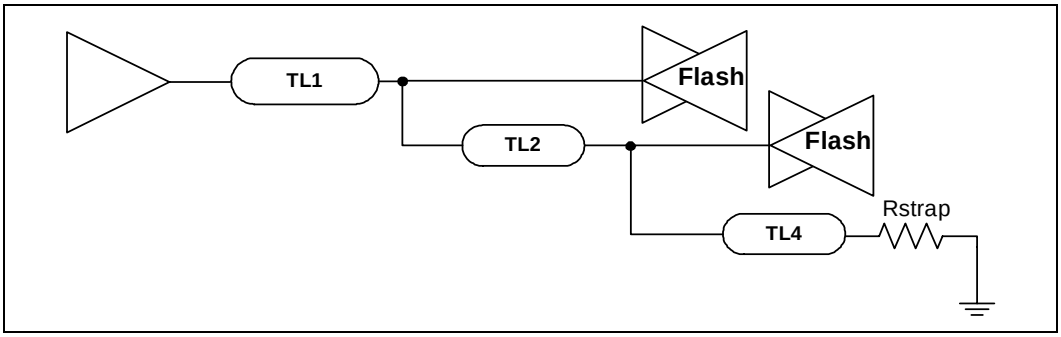


Table 23. PBI Routing Guidelines for Two Loads

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or unbroken power plane. If routing over power plane maintain this consistency throughout the topology.
Routing	Microstrip or stripline or combination of microstrip and stripline
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (edge to edge)	• $\geq$ 5 mils between all Address and Data lines • $\geq$ 20 mils must be maintained from all other signals or vias (for 5 mils trace width)
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils
Trace Length TL1	2.0″ to 20.0″
Trace Length to TL2	0.5″ to 2.0″
Trace Length to strapping resistor TL4	0.5″ to 3.0″ from the last device on the bus
Routing Recommendations	Number of vias for microstrip $\leq$ 8
	Route as daisy-chain only

Figure 26. Peripheral Bus Three Load Topology

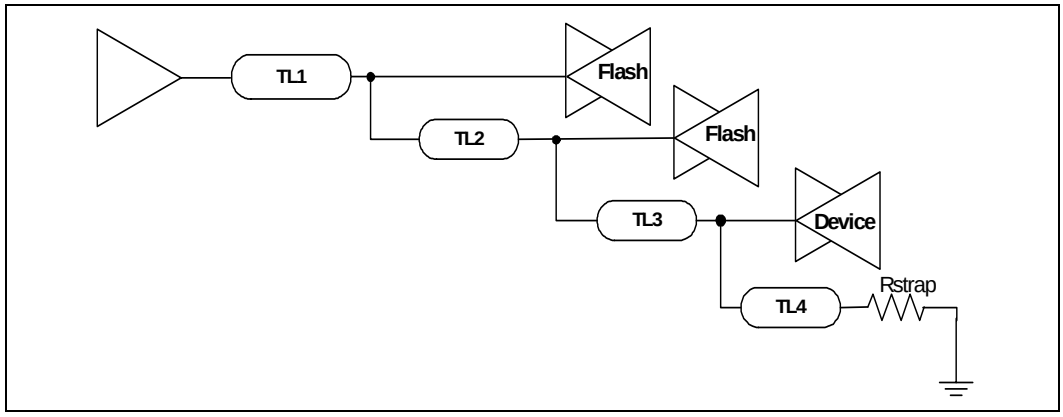


Table 24. PBI Routing Guideline for Three Loads

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or unbroken power plane. If routing over power plane maintain this consistency throughout the topology.
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Routing	Microstrip or stripline minimize the layer changes.
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (edge to edge)	• $\geq$ 5 mils between all Address and Data lines • $\geq$ 20 mils must be maintained from all other signals or vias (for 5 mils trace width)
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Trace Length TL1	2.0" to 20.0"
Trace Length TL2, TL3	0.5" to 2.0"
Trace Length to strapping resistor TL4	0.5" to 3.0" from the last device on the bus.
Routing Recommendations	Number of vias for microstrip $\leq$ 8
	Route as daisy-chain only

8.0 Power Delivery

This section provides information on the power delivery for this chip including:

- the different voltage domains that are required on the Intel® 413808 and Intel® 413812 I/O Controllers are provided in Table 25
- an example of the power plane layout used on the eight layer customer reference board Section 8.1
- decoupling recommendations Section 8.2
- required power sequencing Section 8.1
  - ESL for a 0603 package is 150pH, divide this by 6 = 25nH
  - Total ESL: 25nH || 19 pH = ~ 18.9pH

Table 25. Supply Voltages

Voltage Supply	Voltage	Minimum	Maximum
V_{CC3P3}	3.3 V supply voltage for PCI-X interface and general purpose I/Os	3.0	3.6
V_{CC1P8S}	1.8 V supply voltage for storage interface	1.71	1.89
V_{CC1P8E}	1.8 V supply voltage for PCI Express* interface	1.71	1.89
V_{CC1P8}	1.8 V supply voltage for I/Os	1.71	1.89
V_{CCVIO}	3.3 V supply voltage for PCI-X interface	3.0	3.6
V_{CC1P2X}	1.2 V supply voltage for Intel XScale® processors	1.164	1.236
V_{CC1P2}	1.2 V supply voltage for most digital logic	1.164	1.236
V_{CC1P2E}	1.2 V supply voltage for PCI Express* interface digital logic	1.164	1.236
$V_{CC1P2AE}$	1.2 V supply voltage for PCI Express* interface analog logic	1.164	1.236
$V_{CC1P2AS}$	1.2 V supply voltage for storage interface analog logic	1.164	1.236
$V_{CC1P2DS}$	1.2 V supply voltage for storage interface digital logic	1.164	1.236
VCC1P2PLLS0	1.2 V supply voltage for storage PLL 0	1.164	1.236
VCC1P2PLLS1	1.2 V supply voltage for storage PLL 1	1.164	1.236
VCC1P2PLLP	1.2 V supply voltage for PCI-X PLL	1.164	1.236
VCC3P3PLLX	3.3 V supply voltage for core logic PLL	3.0	3.6

8.1 Power Plane Layout

This section provides the layout of the power planes around our Intel® 413808 and Intel® 413812 I/O Controllers package on the eight layer customer reference board (CRB). While these figures provide additional supplies required for the storage interface, they are included in the Intel® 413808 and Intel® 413812 I/O Controllers design guide for reference purposes. The voltage plane descriptions are listed in Table 26 and the stackup for the customer reference board is listed in Table 27. Figure 27 provides the voltage layout for layer 3, Figure 28 provides the voltage layout for layer 5, Figure 29 provides the voltage layout for layer 6 and Figure 30 provides the voltage layout for layer 8.

Table 26. Customer Reference Board Voltage Planes

CRB Voltage Plane	Package Voltage Planes	Voltage Description
+1_2V	VCC1P2X, VCC1P2	1.2V digital voltage for core logic
+1_2VB[1]	VCC1P2DS	1.2V digital voltage for storage
+1_2VA[1]	VCC1P2AE, VCC1P2AS, VCC1P2E	1.2V analog voltage for PCI-E and storage interfaces
+1_8VA	VCC1P8E, VCC1P8S	1.8V analog voltage for PCI-E and storage interfaces
+3_3V	VCC3P3, VCCVIO	3.3V digital voltage for PCI-X and peripheral bus interfaces

Note: +1_2VA and +1_2VB are supplied from the same regulator on the CRB.

Table 27. Customer Reference Board Layer Stackup

Layer	Layer Description	Voltage Planes	Color Code
1	Primary side	none	
2	Ground plane 1		
3	Internal routing layer 1	+1_2V	Red
		+1_2VB	Blue
		+1_8VA	Yellow
		+1_2VA	Purple
		+3_3V	Pink
4	VCC split plane	+1_2V	Red
		+3_3V	Pink
5	Ground plane 2		
6	Internal routing layer 2	+1_2V	Red
		+1_2VB	Blue
		+1_2VA	Purple
		+3_3V	Pink
		+1_8V	Green
7	Ground plane 3		
8	Secondary layer	+1_8VA	Yellow
		+1_8V	Green

Figure 27. Split Voltage Planes for Layer 3 (Top View)

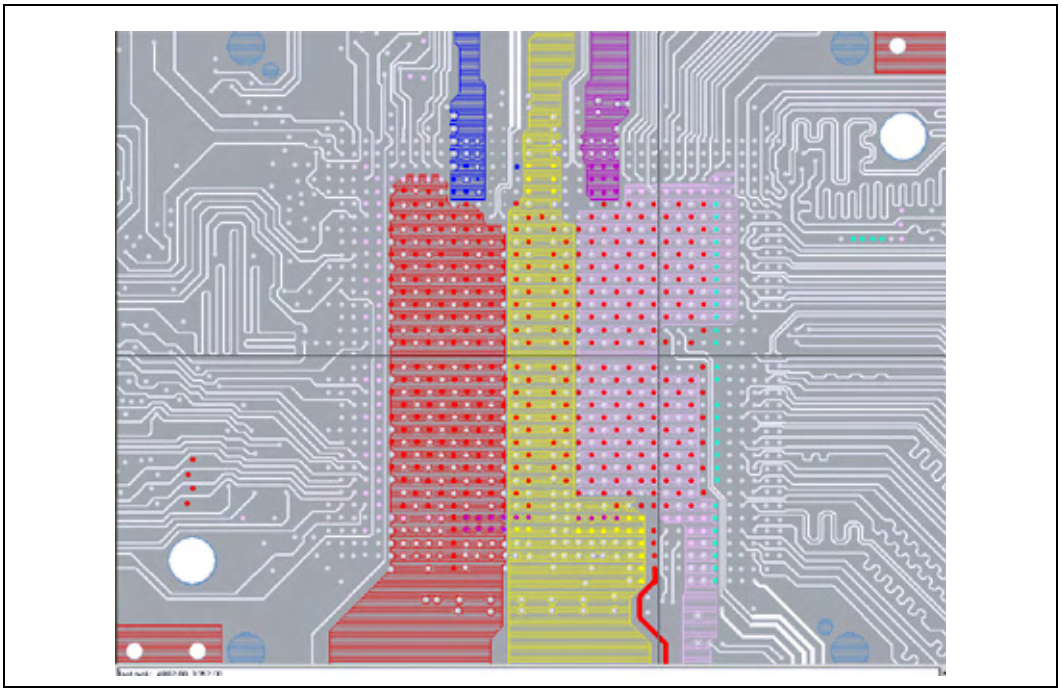


Figure 28. Split Voltage Planes for Layer 4 (Top View)

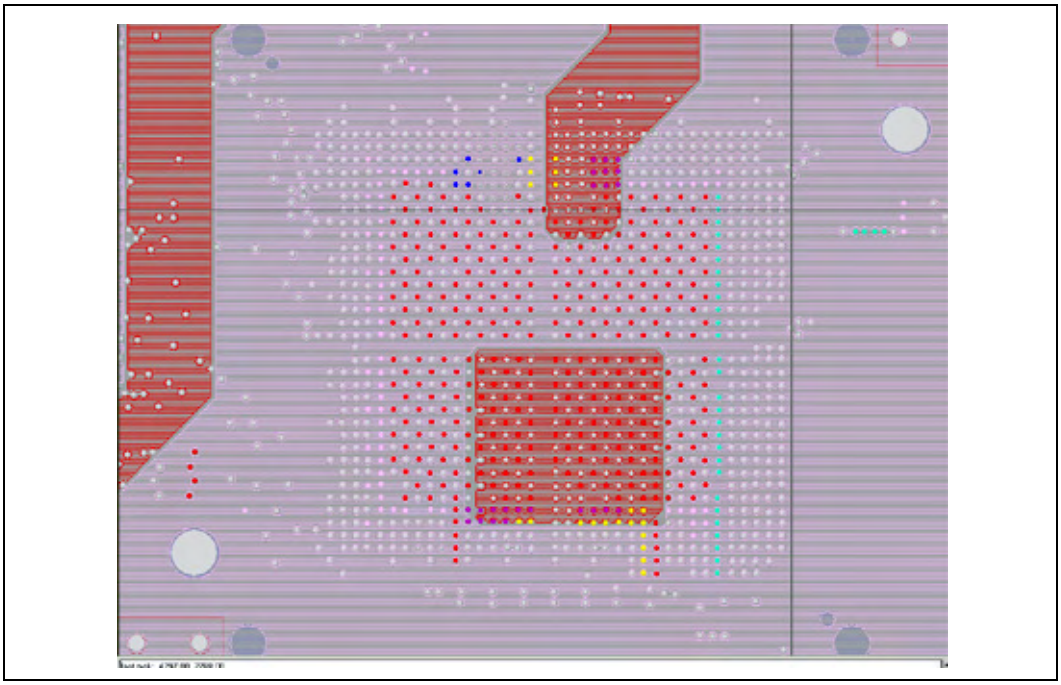


Figure 29. Split Voltage Planes for Layer 6 (Top View)

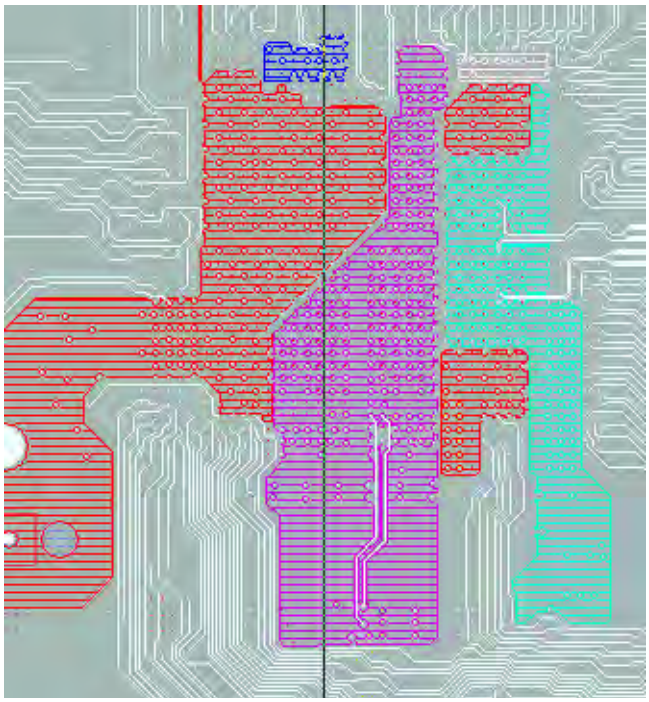
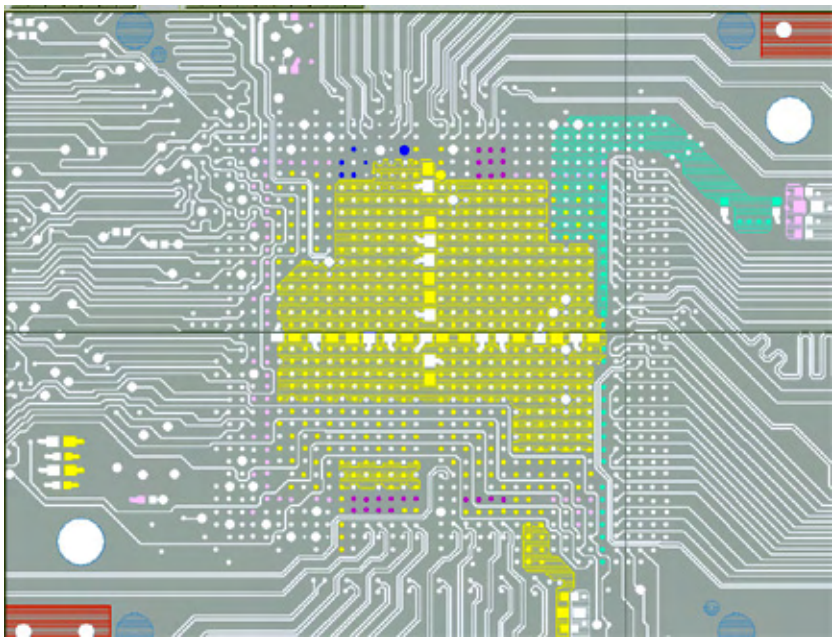


Figure 30. Split Voltage Planes for Layer 8 (Top View)



8.2 Decoupling Recommendations

Table 28 contains the preliminary decoupling recommendations for Intel® 413808 and Intel® 413812 I/O Controllers. Note that the recommendations provide the total minimum capacitance for each voltage plane. The recommended decoupling capacitance, ESR and ESL for each voltage plane is an minimum aggregate value that can be achieved with adding multiple decoupling capacitors in parallel.

Each decoupling capacitor should be placed with a single via to a voltage plane (or plane fill area) and solid ground plane, such that copper loss and inductance between the capacitor and nearby ball via is negligible. Distribute the capacitors so that all power ball vias have decoupling nearby. It is recommended that the distance from ball vias to decoupling be minimized.

Note: The 1.2V High Speed Voltage for the SAS/SATA and the PCI Express should be generated from a regulator that is isolated from the 1.2V core regulator.

Table 28. Decoupling Recommendations

Voltage	Interface	Capacitors
1.2V Digital	Intel XScale® processor 1 Voltage	1 x 20uF min with < 150pH ESL, ~1mohm ESR
	Intel XScale® processor 2 Voltage	1 x 20uF min with < 150pH ESL, ~1mohm ESR
1.2V High Speed Serial	PCI Express	< 150pH ESL, ~3mohm ESR
	SAS/SATA	< 150pH ESL, ~3mohm ESR
1.2V Analog	SAS/SATA Serial Interface	< 150pH ESL, ~3mohm ESR
1.8V Digital	SAS/SATA	1 x 10uF < 100pH ESL, ~1mohm ESR
1.8V Analog	SAS/SATA	1 x 5 uF min with <150pH ESL, ~3mohm ESR
	PCI Express, SAS	1 x 5 uF min with <150pH ESL, ~3mohm ESR
3.3V	PCI-X	1 x 10 uF min with <150pH ESL, ~1mohm ESR

9.0 Debug and Test

This chapter provides information on test equipment that can be used to test the PCI-X, PCI Expressand SAS/SATA interfaces of this part. It is recommended to check the bus interface and manufacturers' websites for the latest test techniques and test equipment.

9.1 PCI-X Debugging

There are several tools available that can aid in the debug and development of PCI-X bus based systems and cards. Agilent Technologies*, VMetro* and Catalyst Enterprises* make analyzer/exercisers cards for capturing and generating PCI-X transactions. These cards also provide capability to trigger on errors, emulate an initiator or target, invoke errors, measure performance, and check for protocol and compliance issues. For pure analysis of the PCI-X bus, both Tektronix and Agilent make passive interposer probe cards that plug into the PCI-X slot of the device under test to capture PCI-X traffic. An example of an interposer card that works with the Agilent logic analyzers is the FuturePlus Systems* FS2007. Another method to capture the PCI-X bus signals with a logic analyzer is to place AMP* Mictor-38 connectors or Agilent Soft Touch Connectorless Probes on the PCB. For the pinout of the connectors that work with the Agilent logic analyzer refer to the FuturePlus Systems* website www.futureplus.com.

9.2 PCI Express Debugging

Debugging a PCI Express design may require analysis at the physical layer to verify the layout and the data link/transaction layer to ensure that the read and write request packets are being transmitted correctly.

9.2.1 Physical Layer Debugging

For PCI Express, the fundamental signaling frequency is 1.25GHz (half the bit rate) and the specified 20-80% rise-time is 100 ps. The Tektronix™ TDS6604 Real-Time Digital Storage Oscilloscope and the Agilent Technologies ™ 54855A provides an analog bandwidth of 6 GHz (with a 20GSa/sec. sampling rate) sufficient to measure the PCI Express differential signals with their respective differential probes.

The alternative equipment to the high speed oscilloscopes include Vector Network Analyzers or Time Domain Reflectometry (TDR) scopes which can help pinpoint signal integrity issues with the PCBs and connectors. This test equipment allows checking the lane-to-lane skew, analyzing jitter and measuring drive strength and receiver tolerance for verification of the physical layer. For more information on using TDR analysis, the application note from Tektronix may be useful:

TDR Impedance Measurements: A Foundation for Signal Integrity.

9.2.2 Data Link and Transaction Layer Testing

The Data Link/Transaction layer can be debugged and validated with PCI Express protocol analyzers or PCI Express analyzer/exerciser tools. Companies that make protocol analyzers for PCI Express include: Catalyst Enterprises, LeCroy (formerly CATC), Agilent, Tektronix and Finisar (formerly DataTransit). For more information on the PCI Express test equipment refer to Intel's PCI Express Developer's website http://www.pciexpressdevnet.org/kshowcase/. The probing solutions for the PCI Express bus include an interposer card and a mid-bus probing solution.

Agilent Technology has a PCI Express Packet Analysis Probe N4220B which works in conjunction with their 16700 family of logic analyzers. The Agilent slot interposer part numbers that work with the 16700 logic analyzer include: N4224A for a x8 slot, N4225A for a x4 slot and N4227A for a x1 slot. The Tektronix slot interposer solution that works with their TLA700 logic analyzer is the TMS817.

9.2.3 PCI Express Analyzer/Exercisers

Agilent's E2960A, Catalyst Enterprises' SPX-8E and LeCroy's PETRacer/PETrainer provide the ability to capture and exercise the PCI Express bus.

9.2.4 Mid-bus Probing

The mid-bus probe provides probing between two devices without PCI Express connector. Catalyst Enterprises, Agilent and Tektronix support mid-bus PCI Express probing. Agilent makes a protocol analyzer/exerciser, E2960A, which uses the Soft touch mid-bus probe e2941A. The Agilent solution that works with the 16700 analyzer is the N4221A. Tektronix's solution is the TMSIC6. The PCB must be designed with the PCI Express mid-bus footprint to allow probing between two devices. Refer to the following paper for more information on PCI Express mid-bus probing and the layout of the mid-bus probe.

http://www.tek.com/Measurement/logic_analyzers/contact/_notes/probe_design_guide_pci.pdf.

9.3 SAS Debugging

Debugging your SAS bus can be aided with SAS protocol analyzer. There are several companies that have SAS test tools including: Catalyst Enterprises, Finisar (formerly Data Transit) and LeCroy (formerly CATC). Most of these protocol analysis tools provide multi-level triggering, filtering, state configuration and post-capture filtering of SAS packets. The Catalyst Enterprises solution STX-430 provides both protocol analysis and exerciser capability for SAS/SATA links running at 3.0Gbps. LeCroy also provides both analysis and exerciser capability with their *SASTracer/Trainer* for links up to 3.0Gbps.

9.4 SATA Debugging

Debugging your SATA bus can be aided with a SATA protocol analyzer. There are several companies that make SATA test tools including: Catalyst Enterprises, Finisar (formerly Data Transit) and LeCroy (formerly CATC). Refer to the www.serialata.org website for more test manufacturer information. Most of these protocol analysis tools provide multi-level triggering, filtering, state configuration and post-capture filtering of Serial ATA packets. The Catalyst Enterprises solution STX-430 provides both protocol analysis and exerciser capability for SAS/SATA links running at 3.0Gbps. LeCroy also provides both analysis and exerciser capability with their *SASTracer/Trainer* for links up to 3.0Gbps.

10.0 Thermal Solutions

For information on our thermal solutions, please refer to the *Intel® 413808 and Intel® 413812 I/O Controllers Thermal Application Note*.

§End of Chapter§

11.0 Terminations

This chapter provides the recommended pull-up and pull-down terminations for a Intel® 413808 and Intel® 413812 I/O Controllers layout.

11.1 Important Design and Debug Requirements

The following details are required for all Intel® 413808 and Intel® 413812 I/O Controllersdesigns. Note that these table is not an inclusive list. We recommend that design guide is referenced for additional details.

Note: Without implementing the debug requirements Intel will be extremely limited in its ability to assist with debug issues involving the transport firmware and device driver.

Table 29. Design and Debug Checklist

Recommendations	Comments	Compliance	
		Yes	No
Debug Requirements			
• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware.	UART 0 is dedicated as the debug port for the transport FW. This port is also implemented on Intel's development boards. Without the UART0 port the debug of the transport firmware is extremely limited. This port can be depopulated on production boards.		
• The JTAG port must be implemented on the board to assist in debug of third party device drivers.	A JTAG port provides the ability to connect a 3rd party debugger to Intel® 413808 and Intel® 413812 I/O Controllers. Using a debugger is the only way to pinpoint potential device driver and transport firmware issues. ***Notes:*** 1. JTAG port is required even if the customer has no plans to utilize this connector in their debug process. Without the JTAG port, the debug of the device driver is extremely limited. 2. A low profile 10 pin JTAG port is now recommended to save on board space. Refer to the JTAG chapter of the design guide for implementation recommendations. This port may be depopulated on production boards.		
Design Notes			
• Supported and validated flash components include Intel Strata Flash - J3, J3D and Intel Strata Flash Embedded Memory - P30. • A minimum size of 2MB is required for the transport firmware.	• For information on migrating from the J3 to P30 refer to the following document: http://developer.intel.com/design/flcomp/applnots/306667.htm ***Note:*** Other CFI flash memory may work but these components have not been validated.		
• The 1.2V Core power should be separated from the SAS/SATA and PCIE planes	Separating the 1.2V core supply will minimize noise coupling.		
• The SAS PLL filtering must be connected to ground. All the other PLL filters are not connected ground.	Refer to Section 11.4.1 of this document		
• Maximum SAS trace lengths (TX and RX) from controller ball to first connector	≤ 5"		
• 1.2V must be up before the 1.8V. The 1.2V must be down after the 1.8V.	Refer to the power delivery chapter of the design guide for additional details.		
• JTAG TRST_N must be asserted at power-on	A reset supervisor to pulse TRST_N low on power-on and pull high after power-on. Refer to the JTAG section of the design guide.		

11.2 Checklist Recommendations

The following tables provide the recommended pull-up and pull-down terminations for a Intel® 413808 and Intel® 413812 I/O Controllers layout.

Table 30. Terminations: Pull-up/Pull-down (Sheet 1 of 6)

Signal	Recommendations	Comments
S_TXP[7:0], S_TXN[7:0]	• connect each of **S_TXP[7:0], S_TXN[7:0]** lines with a 10 nF series capacitor with low ESR • Unused ports can be left unconnected	**Storage Transmit: carries** the differential output serial data and embedded clock for the **SAS/SATA** interface.
S_RXP[7:0], S_RXN[7:0]	• connect each of **S_RXP[7:0], S_RXN[7:0]** lines with a10 nF series capacitor with low ESR • Unused ports can be left unconnected	**Storage Receive: carries** the differential input serial data and embedded clock for the **SAS/SATA** interface.
S_CLKN0, S_CLKP0	• connect to differential 125 MHz ±100 ppm oscillator	Differential storage clock
S_ACT0/SCLOCK0, S_STAT0/SLOAD0	• NC if not used • SGPIO[0] is disabled: connect to LED with series resistor to VCC to indicate activity and status for storage engine[0]	These signals are open drain.
S_ACT1, S_STAT1	• NC if not used. • SGPIO[0] is disabled: these signals can be connected to an LED with series resistor to VCC to indicate activity and status for storage engine[1]	These signals are open drain.
S_ACT2/SDATAIN0, S_STAT2/ SDATAOUT0	• NC if not used. • SGPIO[0] is disabled: these signals can be connected to an LED with series resistor to to VCC in order to indicate activity or status for storage engine[2]	These signals are open drain.
S_ACT3, S_STAT3	• NC if not used. • SGPIO[0] is disabled: these signals can be connected to an LED with series resistor to VCC in order to indicate activity and status for storage engine[3]	These signals are open drain.
S_ACT4/SCLOCK1, S_STAT4/SLOAD1	• NC if not used • SGPIO[1] is disabled: these signals can be connected to an LED with series resistor to VCC in order to indicate activity/status for storage engine[4]	TThese signals are open drain.
S_ACT5, S_STAT5	• NC if not used. • SGPIO[1] is disabled: these signals can be connected to an LED with series resistor to VCC in order to indicate activity /status for storage engine[5]	These signals are open drain.
S_ACT6/SDATAIN1, S_STAT6/ SDATAOUT1	• NC if not used. • SGPIO[1] is disabled: these signals can be connected to an LED with series resistor to VCC in order to indicate activity/status for storage engine[6]	These signals are open drain.
S_ACT7, S_STAT7	• NC if not used. • SGPIO[1] is disabled: these signals can be connected to an LED with series resistor to VCC in order to indicate activity/status for storage engine[7]	These signals are open drain.

Table 30. Terminations: Pull-up/Pull-down (Sheet 2 of 6)

Signal	Recommendations	Comments
REFCLKP, **REFCLKN**	• For PCI-Express: connect to a 100MHz oscillator. • For PCI-X end point mode: connect the REFCLKP to a resistor divider such that the REFCLKP node is connected to both a 17.4K to VCC3P3 and a 4.7K connected to GND. REFCLKN must be connected to GND.	Note: 100 MHz oscillator is required for the PCI Express differential clock and to generate the P_CLK's.
PETP[7:0], **PETN[7:0]**	• Series capacitors with value of 75nF to 200nF (low ESR) on each of the lines. • NC if not used	
PERP[7:0], **PERN[7:0]**	• No series capacitor needed • NC if not used	
P_AD[63:32], **P_CBE[7:4]#**, **P_PAR64**	• If only PCI Express interface active these signals are internally pulled-up and can be left as a NCs. • If the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • If the PCIX_32BIT# is enabled (32 bit bus width), these signals are internally pulled-up and can be left as a NCs.	
P_AD[31:0], **P_CBE[3:0]#**	If only PCI Express interface active these signals are internally pulled-up and can be left as a NCs.	
P_REQ#	• PCI Express: P_GNT[0]# / **P_REQ#** has an internal pull-up and can be left as a NC. • PCI Endpoint mode (external arbiter) PCIX_EP# = 0: This is the output request signal for the ATU and needs to connect to the external arbiter's P_REQ# lines.	
P_GNT#	• PCI Express: **P_REQ[0]#** / **P_GNT#** has an internal pull-up and can be left as a NC. • PCI Endpoint mode (external arbiter) PCIX_EP# = 0: **P_GNT#** is input grant signal for the ATU. This pin should be pulled up to VCC3P3 with an 8.2K resistor.	
P_REQ64#	• If only PCI Express interface is active these signals are internally pulled-up and can be left as a NC. • If the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • If the device is PCI endpoint then the width of the bus is indicated by the state of REQ64# at the rising edge of RST#	
P_ACK64#, **P_PAR** **P_SERR#**, **P_PERR#**, **P_INT[D:A]#**	• If only PCI Express interface is active these signals are internally pulled-up and can be left as a NC. • If the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up.	
P_FRAME#, **P_IRDY#**, **P_TRDY#**, **P_STOP#**, **P_DEVSEL#**	• If only PCI Express interface is active these signals are internally pulled-up and can be left as a NC. • If the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • PCI endpoint **PCIX_EP#** = 0 the state of these signals are used for PCI-X initialization pattern at the rising edge of RST#.	Refer to the *PCI-X Specification 1.0b* for more information on the PCI-X Initialization pattern.

Table 30. Terminations: Pull-up/Pull-down (Sheet 3 of 6)

Signal	Recommendations	Comments
P_M66EN	• PCI Express: P_M66EN has an internal pull-up and can be left as a NC. • PCI Endpoint mode: No connect.	
P_IDSEL	• PCI Express: P_IDSEL has an internal pull-up and can be left as a NC. • PCI Endpoint mode: connect to AD lines Section 4.1	
P_CLKIN	• **PCI Endpoint mode (PCIX_EP# = 0)**: connect to the system PCI clock. • For PCI Express only this signal should be connected to GND.	Notes: • REFCLKP, REFCLKN must have 100 MHz clock to generate the P_CLKO[3:0] outputs.
P_PCIXCAP	If PCI Express only: • GND this pin. PCI Endpoint mode: • **PCIX_EP#** = 0: No connect.	Refer to PCI-X Specification 1.0b and Section 4.1
P_BMI	• If PCI Express only: this signal can be left as a no connect. • For PCI-X : no connect if not used.	
P_CAL[0], **P_CAL[2]**	• If PCI-X interface is used: This pin is connected to a separate 22.1 Ω 1% resistor to GND. See Section 11.5 for more information. • If PCI-X interface is not used: These pins can be left as NC's	**PCI** Calibration: is connected to an external calibration resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations.
P_CAL[1]	• If PCI-X is used: This pin is connected to a separate 121Ω 1% resistor to GND. See Section 11.5 for more information. • If PCI-X interface is not used: These pins can be left as NC's	**PCI** Calibration: is connected to an external calibration resistor such that the output drivers reference the resistor to dynamically adjust the ODT resistance to compensate for voltage and temperature variations.
PE_CALP PE_CALN	Connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball. Refer to Figure 35. Note: this is required even if the PCI-Express interface is not used.	
A[24:0], POE#, **PB_RSTOUT#**	• Unused pins can be left unconnected. • If used refer to Section 7.3 for PBI bus connection recommendations.	
D[15:0], **PCE[1:0]#**, PWE#	• These are used for reset straps refer to the Reset Strap Table 31. • Also refer to Section 7.3 for PBI bus connection recommendations.	
HS_ENUM#	Can be left unconnected if hot swap not used.	
HS_LSTAT	If Compact PCI Hot Swap is not supported, this signal must be tied to GND.	Hot Swap Latch Status: An input indicating the state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. 1 = 8.2K pull-up to VCC 0 = connect to GND.
HS_LED_OUT	• Connect to Hot Swap blue LED. • If Compact PCI Hot Swap is not supported this signal can be left unconnected.	

Table 30. Terminations: Pull-up/Pull-down (Sheet 4 of 6)

Signal	Recommendations	Comments
HS_FREQ[1:0]	See comments	Hot Swap Frequency: While in Hot Swap mode, (these are only valid when **PCIX_EP#** = 0 and **HS_SM#** = 0). 00 = 133MHz PCI-X 01 = 100MHz PCI-X 10 = 66MHz PCI-X 11 = 33 or 66MHz. PCI (frequency depends on **P_M66EN**)
P_INT[D:A]# / **XINT[3:0]#**/ GPIO[11:8]	• If using these pins as interrupts and PCIX_EP# = 0: No termination is required • If using these pins as interrupts and PCIX_EP# = 1: 8.2 K pull-ups required on each line • If using as GPIO's then 8.2 K pull-ups required on each of the line	• **When INTERFACE_SEL_PCIX# = "0":** PCI Interrupt: **These outputs are level sensitive.** • **When INTERFACE_SEL_PCIX# = "1": External Interrupt**: requests are used by external devices to request interrupt service. These pins are level-detect inputs and are internally synchronized. These pins go to the **XINT[3:0]#** inputs of the Interrupt Controller.
HPI#, NMI0#, NMI1#, **XINT[7:4]#**	8.2 K pull-ups	
GPIO[7:0] / **XINT[15:8]#** / **CHAPOUT**	8.2 K pull-up	• General Purpose I/O (default mode). • **External Interrupt**: These pins are level-detects and are internally synchronized. • CHAPOUT: GPIO[7] When enabled it will override the normal GPIO[7] function.
SCL0, **SDA0**, **SCL1**, **SDA1**, **SCL2**, **SDA2**	• If used external pull-up to VCC is required. Refer to the I^2C specification for information on calculating the pull-up. ***Note:*** I^2C port 0 can only used for SEP enclosure management. ***Note:*** I^2C port 1 and port 2 are not available on Intel® 413808 and Intel® 413812 I/O Controllers and must have pull-ups. • 2K pull-up if unused.	The pull-up value is dependent on the bus loading. Refer to the I^2C specification http://www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf
SMBCLK	For PCI Express adapter cards: • If the SMBus is used, there should be isolation device such as the LTC4301 between this signal and PE_SMCK on the PCI Express connector. For PCI Express motherboard applications: • If SMBus is used a pull-up is required (value is dependent on the loading). • If SMBus is unused, a 8.2K pull-up is required.	LTC4301 is a hotswappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pdf/4301fa.pdf Refer also to the http://www.smbus.org for the latest specification.
SMBDAT	For PCI Express adapter cards: • If the SMBus is used, there should be isolation device such as the LTC4301 between this signal and PE_SMDAT on the PCI Express connector. For PCI Express motherboard applications: • If SMBus is used a pull-up is required (value is dependent on the loading). • If SMBus is unused, a 8.2K pull-up is required.	LTC4301 is a hotswappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pdf/4301fa.pdf Refer also to the http://www.smbus.org for the latest specification.

Table 30. Terminations: Pull-up/Pull-down (Sheet 5 of 6)

Signal	Recommendations	Comments
U0_RXD, U1_RXD	• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware. • If unused, connect to GND. • UART 1 is not available for Intel® 413808 and Intel® 413812 I/O Controllers	
U0_TXD, U0_RTS#, U1_TXD, U1_RTS#	• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware. • Can be left unconnected if unused. • UART 1 is not available for Intel® 413808 and Intel® 413812 I/O Controllers	
U0_CTS#, U1_CTS#	• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware. • If unused, 8.2 K ohm pull-up. • UART 1 is not available for Intel® 413808 and Intel® 413812 I/O Controllers	
TCK	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • 10K pull-up if used. Refer to the JTAG chapter. • GND if unused.	Test Clock: provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG).
TDI	• The JTAG port must be implemented on the board to assist in debug. • 10K pull-up if used. Refer to the JTAG chapter. • NC if unused has weak pull-up	Test Data Input: is the JTAG serial input pin.
TDO	• The JTAG port must be implemented on the board to assist in debug. • If used refer to the JTAG chapter. • NC if unused	Test Data Output: is the serial output pin for the JTAG feature.
TRST#	• The JTAG port must be implemented on the board to assist in debug. • If used refer to the JTAG chapter. • GND if unused.	Test Reset: This pin has a weak internal pull-up.
TMS	• The JTAG port must be implemented on the board to assist in debug. • 8.2K pull-up if used. Refer to the JTAG chapter. • NC if unused has weak pull-up.	Test Mode Select: This pin has a weak internal pull-up.
WARM_RST#	• If PCI-X interface is used: 1K pull-up. • If PCI-Express used: This pin can only be used when the sticky bit functionality is required. In this scenario, the WARM_RST# pin must be tied to the system reset PCI_RST# signal while the P_RST# pin can be tied to the system power good signal.	**Warm Reset** is the same as a cold reset, except sticky configuration bits are ***not*** reset. Notes: - When the PCI Express interface is used as an endpoint, the PCI Express in-band Hot Reset Mechanism can also be used to provide the sticky bit functionality. -Driving WARM_RST# using any other methods than suggested above may result in unpredictable behavior of the device.
NC	No Connect: pins have no usable function and must not be connected to any signal, power or ground.	
THERMDA	• Connect to the anode of the thermal diode. • NC if unused	

Table 30. Terminations: Pull-up/Pull-down (Sheet 6 of 6)

Signal	Recommendations	Comments
THERMDC	• Connect to the cathode of the thermal diode. • NC if unused	
VCCVIO	• If PCI-X interface is used: connect to VCC3P3 • If PCI-X interface is not used: connect to GND	
VCC1P2PLLP, VCC1P2PLLD	• If PCI-X interface is used: refer to the filter ecommendation in Section 11.4.2. • If PCI-X interface is not used: connect both VCC1P2PLLP and VCC1P2PLLD to GND	
PUR1	This pin must be pulled up to VCC3P3 with an external 8.2K ohm 5%resistor for proper operation.	

11.3 Reset Straps

Table 31 provides a list of reset straps which are multiplexed on the Peripheral Address Bus A[24:0]. These pins are latched on the rising edge of **P_RST#**. All reset strap signals are internally pulled to logic 1 by default. An external 4.7K ohm 5% pull-down resistor is required to force a logic 0 on these pins.

Table 31. Reset Straps (Sheet 1 of 3)

Signal	Recommendations	Comments
BOOT_WIDTH_8#	0 = 8 bits wide, 0 = 4.7K ohms resistor pull down 1 = 16 bits wide (Default mode internal pull-up)	***Note:*** Muxed onto signal **A[0]**.
CFG_CYCLE_EN#	0 = Configuration Cycles enabled, 0 = 4.7K ohms resistor pull down 1 = Configuration Retry enabled (Default mode internal pull-up)	NOTE: Muxed onto signal **A[1]**
HOLD_X0_IN_RST#	• 0 - Hold Scale in reset, 0 = 4.7 K ohms resistor pull down • 1 - Do not hold in reset (Default mode internal pull-up)	***Note:*** Muxed onto signal **A[2:0]**
HOLD_X1_IN_RST#	0 = Hold in reset, 0 = 4.7K ohms resistor pull down 1 = Do not hold in reset (Default mode internal pull-up).	***Note:*** Muxed onto signal A[3]
EXT_ARB#	Requires 4.7K ohms resistor pull down	***Note:*** Muxed onto signal **A[6]**, Only external arbiter mode is supported
INTERFACE_SEL_PCIX#	• For PCI Express -No connect (default) • For PCI-X - Requires a 4.7K ohms resistor pull down.	Interface Select PCI-X: determines which interface will be function 0. 0 = 4.7K ohms resistor pull down PCI-X is enabled 1 = internal pull up (default) PCI-Express interface is enabled. Muxed onto signal **A[10]**
CONTROLLER_ONLY#	Requires a 4.7K ohm pull-down	**Controller-Only Enable:** 0 = Controller only, RAID disabled 1 = RAID enabled (default mode) this is not supported in Intel® 413808 and Intel® 413812 I/O Controllers Muxed onto signal **A[23]**
DF_SEL[2:0]	Intel® 413808 and Intel® 413812 I/O Controllers configurations: • single core 8 port Intel® 413808 and Intel® 413812 I/O Controllers DF_SEL[2:0] = 000 • dual core 8 port Intel® 413808 and Intel® 413812 I/O Controllers DF_SEL[2:0] = 100	***Note:*** **DF_SEL[2]** muxed onto signal **A[9]** ***Note:*** **DF_SEL[1]** muxed onto signal **A[8]** ***Note:*** **DF_SEL[0]** muxed onto signal **A[7]** 0 = 4.7K ohms resistor pull down
PCIX_EP#	Requires a 4.7K ohm resistor pull-down	Only PCI-X End Point mode is supported (no central resource mode). (Default mode) NOTE: muxed onto signal **A[11]**
PCIE_RC#	No connect	PCI-E Root Complex: Endpoint mode only supported (no root complex) Internal pull-up NOTE: muxed onto signal **A[12]**

Table 31. Reset Straps (Sheet 2 of 3)

Signal	Recommendations	Comments
PCIXM1_100#	No connect. Not used in	PCI-X Mode 1 100MHz Enable: 0 = limit PCI-X mode 1 to 100MHz 1 = 133MHz enabled (Default mode) ***Note:*** Muxed onto signal A[19]
SMB_A5, **SMB_A3**, **SMB_A2**, **SMB_A1**	Refer to comments.	SM Bus Address: maps to address bits 5,3,2, and 1 where bits 7- 0 represent the address the SMBus slave port will respond to when access is attempted. 0 = address bit will be low 1 = address bit will be high (Default mode) ***Note:*** **SMB_A5** muxed onto signal A[16] ***Note:*** **SMB_A3** muxed onto signal **A[15]** ***Note:*** **SMB_A2** muxed onto signal **A[14]** ***Note:*** **SMB_A1** muxed onto signal **A[13]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
PCIX_PULLUP#	When pulled-low enables the following signal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#**, **P_PAR64**, **P_REQ64#**, **P_ACK64#**, **P_FRAME#**, **P_IRDY#**, **P_TRDY#**, **P_STOP#**, **P_DEVSEL#**, **P_SERR#**, **P_PERR#**, **P_INT[D:A]#**	PCI-X Pull Up: 0 = enable PCI pull up resistors 1 = disable PCI pull up resistors (Default mode) ***Note:*** Muxed onto signal A[17] 0 = 4.7K ohms resistor pull down 1 = internal pull up.
PCIX_32BIT#	When 32 PCI-X bus enabled the following signals have internal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#** and **P_PAR64** and can be left as NCs.	32-Bit PCI-X Bus: 0 = 32 bit wide PCI-X bus. 1 = 64 bit wide PCI-X bus. (Default mode) ***Note:*** Muxed onto signal A[18] 0 = 4.7K ohms resistor pull down 1 = internal pull up.
HS_SM#	Refer to comments	Hot Swap Startup Mode: 0 = Hot Swap mode enabled 1 = Hot Swap mode disabled (Default mode) ***Note:*** Muxed onto signal **A[21]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
FW_TIMER_OFF#	Refer to comments.	Firmware Timer Off: 0 = firmware timer disabled 1 = firmware timer enabled (Default mode) ***Note:*** Muxed onto signal **A[22]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.

Table 31. Reset Straps (Sheet 3 of 3)

Signal	Recommendations	Comments
CLK_SRC_PCIE#	Refer to comments.	Clock Source PCI-E: selects the PCI Express Refclk pair as the input clock to the PLLs that control most internal logic. 0 = source clock is **REFCLKP/REFCLKN** 1 = source clock comes from the active PCI interface (Default mode) ***Note:*** Muxed onto signal PWE# 0 = 4.7K ohms resistor pull down 1 = internal pull up.
LK_DN_RST_BYPASS#	Use for PCI Express mode	Link Down Reset Bypass: Disables the full chip reset that would normally be caused by a Link Down or hot reset. 0 = Do not reset on Link Down 1 = Reset on Link Down (default mode) Muxed onto signal **A[24]**
PCE[1:0]#	Pull up both these signals with 8.2K resistor	

The following table provides the reset strap configuration for valid operational modes of the chip: PCI Express endpoint or PCI-X endpoint modes.

Table 32. PCI Express/PCI-X Strap Configuration Table

Endpoint Configuration	Strapping Settings			
	CONTROLLER_ONLY#	INTERFACE_SEL_PCIX#	PCIE_RC# (PCI Express root Complex strap)	PCIX_EP# (PCIX endpoint strap)
PCI Express endpoint	0	1	1	X
PCI-X endpoint	0	0	X	0

11.4 Analog Filters

This section describes filters needed for the PLL circuitry. Table 33 lists the PLL's that are required for this part.

Table 33. Required PLLs

Interface	FilteredVoltage	VCC PLL Balls	VSS PLL Balls	Layout Guideline Table
Storage	1.2V	VCC1P2PLLS0	VSSPLLS0	Table 34
		VCC1P2PLLS1	VSSPLLS1	
PCI-X	1.2V	VCC1P2PLLP	VSSPLLP	Table 35
Core Digital Logic	1.2V	VCC1P2PLLD	VSSPLLD	Table 35
Intel XScale® processor and XSI bus logic	3.3V	VCC3P3LLX	VSSPLLX	Table 36

11.4.1 $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Filter Requirements

The lowpass filter, as shown in Figure 31 reduces noise induced clock jitter and its effects on timing relationships in system designs. The filter has the following characteristics:

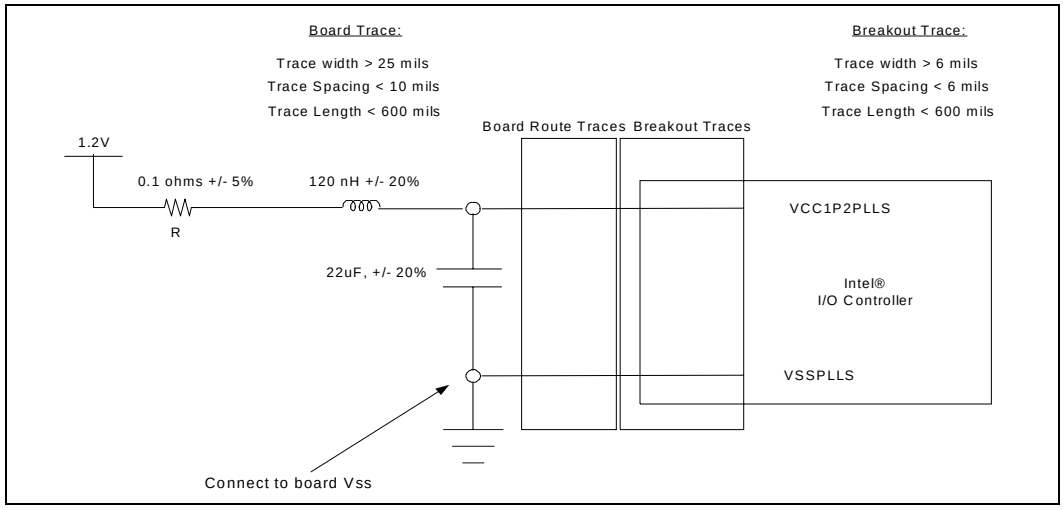
- the purpose of this filter is to achieve at least 10 dB rejection of frequencies between 1 and 20 MHz.
- the filter components are selected to achieve a corner frequency of 100KHz.
- the current draw for these pins is less than 85mA

The Figure 31 filter circuit is recommended for the two PLL pairs: VCC1P2PLLS0 - VSSPLLS0 and VCC1P2PLLS1 - VSSPLLS1 pairs.

Table 34. $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground • VCC1P2PLLS0, VSSPLLS0 and VCC1P2PLLS1, VSSPLLS1 traces must be ground referenced (no V_{CC} references)
Inductor	• 120 nH +/- 20% • L must be magnetically shielded • ESR: max < 0.3 Ω • rated at 45 mA
Capacitor	• 22 µF +/- 20% • ESR: max < 0.3 Ω • ESL < 2.5 nH • Rated: 6.3V • Place 22 µF capacitor as close as possible to package pin.
Resistor	• 0.1 Ω 5% (Resistor) • rated at 6.3 V • 0.1 ohm 5% resistor must be placed between $V_{CC1P2PLL}$ and L.
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2″
Routing Guideline 1	Route VCC1P2PLLS and VSSPLL as differential traces.
Routing Guideline 2	The nodes connecting VCC1P2PLLS and the capacitor must be as short as possible.
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance

Figure 31. VCC1P2PLLS0, VCC1P2PLLS1 Configuration



11.4.2 $V_{CC1P2PLLP}$, $V_{CC1P2PLLD}$ Filter Requirements

The lowpass filter, as shown in Figure 32 reduces noise induced clock jitter and its effects on timing relationships in system designs. The Table 35 filter circuit is recommended for each of the PLL pairs: VCC1P2PLLP-VSSPLLP, VCC1P2PLLD - VSSPLLD pairs. The low pass filter has the following characteristics:

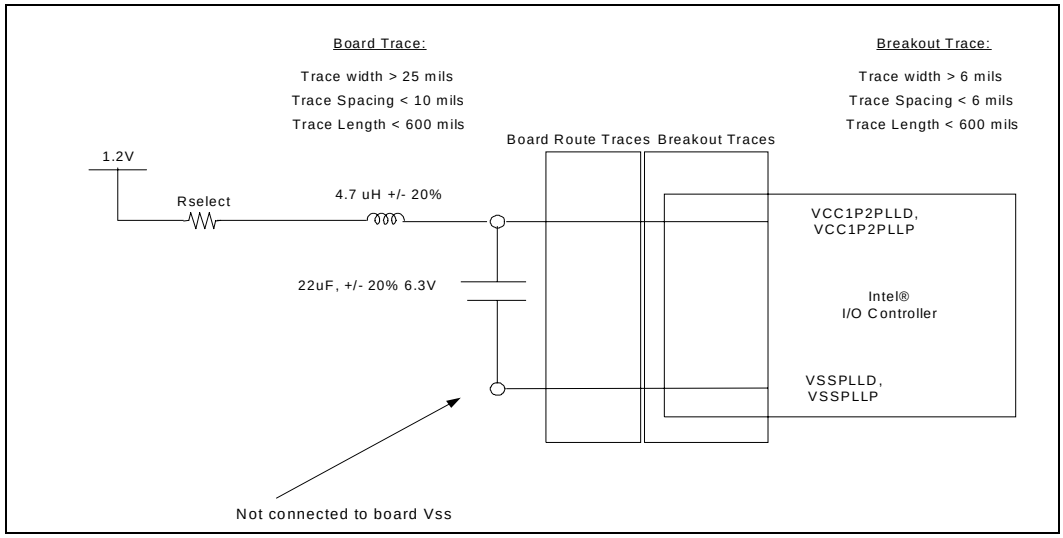
- The filter components must be able to handle a DC current of 30mA.
- < 0.2dB gain in pass band and < 0.5dB attenuation in pass band < 1Hz. Passband is DC through 1Hz.
- > 34dB attenuation from 1MHz to 66MHz
- > 28dB attenuation from 66MHz to core frequency

Note: If the PCI-X interface is not used the VCC1P2PLLP and VSSPLLP pins can be grounded.

Table 35. $V_{CC1P2PLLP}$, $V_{CC1P2PLLD}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground • VCC1P2PLLP, VCC1P2PLLD traces must be ground referenced (no V_{CC} references)
Inductor	• 4.7 uH +/- 25% • L must be magnetically shielded • ESR: max < 0.3 Ω • rated at 45 mA
Capacitor	• 22 µF +/- 20% 6.3V (Capacitor) • ESR: max < 0.3 Ω • ESL < 2.5 nH • Rated: 6.3V • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2V plane to the top end of the capacitor is > 0.35 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • 1.2V plane to $V_{CC1P2PLL}$ < 1.5 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • 1/16 W 6.3 V • resistor must be placed between V_{CC1P2} and L. • Note: if trace and component resistance is large enough a discrete resistor is not required
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2”
Routing Guideline 1	Route VCC1P2PLLD and VSSPLLD, VCC1P2PLLP and VSSPLLP as differential traces.
Routing Guideline 2	The nodes connecting VCC1P2PLLD and the capacitor, VCC1P2PLLP and the capacitor must be as short as possible.
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance

Figure 32. VCC1P2PLLD, VCC1P2PLL Lowpass Filter Configuration



11.4.3 $V_{CC3P3PLLX}$ PLL Requirements

To reduce clock skew, a PLL is implemented for Intel XScale® processor and core logic. The balls associated with this PLL are VCC3P3PLLX and VSSPLLX. The lowpass filter, as shown in Figure 33 reduces noise induced clock jitter and its effects on timing relationships in system designs. The node connecting VCC3P3PLLX and the capacitor must be as short as possible.

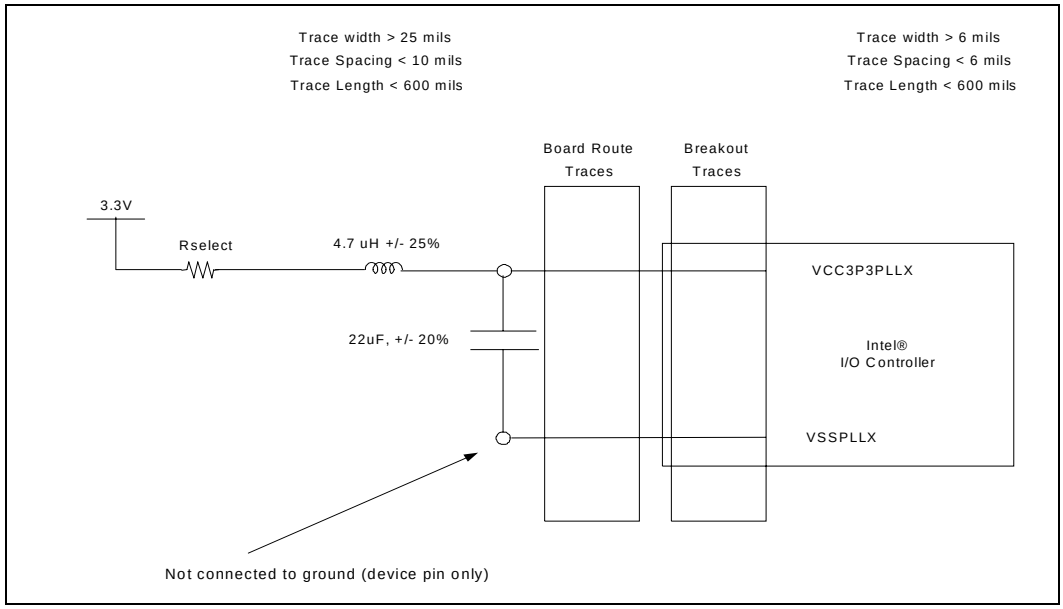
The following notes list the layout guidelines for this filter:

- The filter components must be able to handle a DC current of 30mA.
- < 0.2dB gain in pass band and < 0.5dB attenuation in pass band < 1Hz. Passband is DC through 1Hz.
- > 34dB attenuation from 1MHz to 66MHz
- > 28dB attenuation from 66MHz to core frequency

Table 36. $V_{CC3P3PLL}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground referenced • VCC3P3PLL and VSSPLLX traces must be ground referenced (no V_{CC} references)
Inductor	• 4.7 µH • L must be magnetically shielded • ESR: max < 0.4 Ω • rated at 45 mA • An example of this inductor is TDK part number MLZ2012E4R7P.
Capacitor	• 22 µF +/- 20% • ESR: max < 0.3 Ω • ESL < 2.5 nH • Rated: 6.3V • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 3.3V plane to the top end of the capacitor is > 0.35 Ω • 3.3V plane to $V_{CC3P3PLL}$ < 1.5 Ω • resistor ratings: 1/16 W 6.3 V • resistor must be placed between V_{CC3P3} and L. • Note: if the trace and component resistance is large enough the discrete resistor is not required
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2”
Routing Guideline 1	Route VCC3P3PLLX and VSSPLLX as differential traces.
Routing Guideline 2	The nodes connecting VCC3P3PLL and the capacitor must be as short as possible.

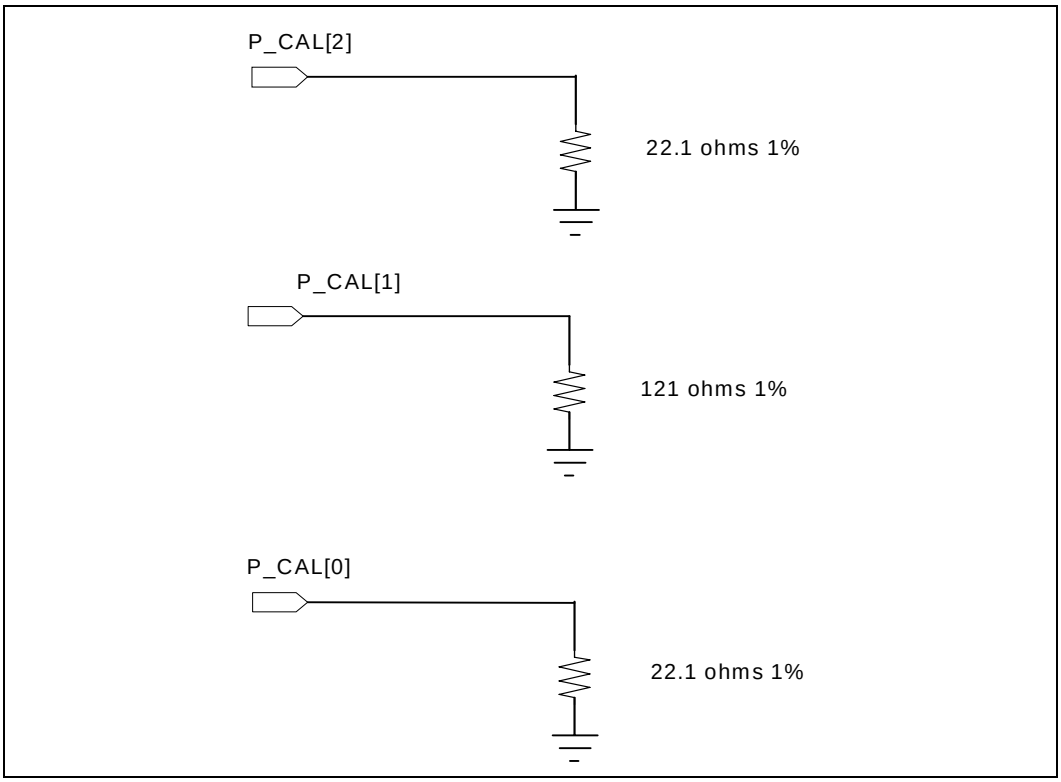
Figure 33. VCC3P3PLL Filter Configuration



11.5 PCI Resistor Calibration

Figure 34 shows the termination required for the PCI calibration circuitry. **PCI** Calibration pins P_CAL[1:0] are connected to an external calibration resistors. The PCI output drivers can reference the resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations.

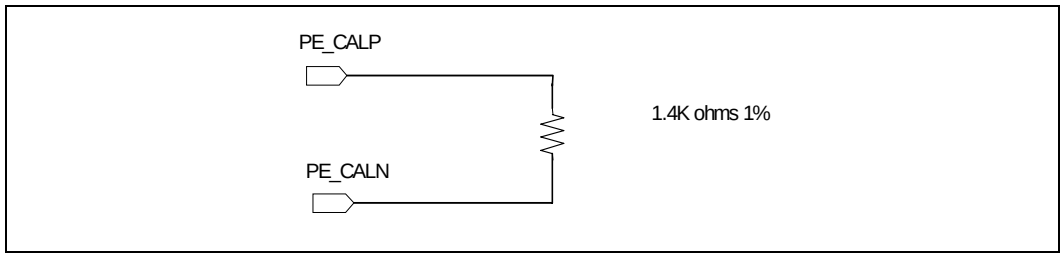
Figure 34. PCI Resistor Calibration



11.6 PCI Express Resistor Compensation

Figure 35 shows the termination required for the PCI Express RCOMP circuit.

Figure 35. PCI Express RCOMP



12.0 Layout Checklist

12.1 Layout Checklist

The Table 37 provides a summary of layout guidelines for each of the interfaces described in detail in the previous sections. The spacing and width specifications are based on the stackup provided in Section 3.0.

Table 37. Layout Checklist (Sheet 1 of 14)

Checklist Items	Recommendations	Comments
PCI Express for Motherboard Layout Recommendations (PETP[7:0]/ PETN[7:0],PERP[7:0],PERN[7:0])		Refer to Section 5.2.1
Reference Plane	Routing over unbroken ground plane is preferred. If unbroken ground plane is not available route over unbroken voltage plane.	
Trace Impedance	• Single-ended: 50 ohms +/- 15% • Differential: 85 ohms +/- 15%	
Microstrip Trace Width	5 mils	
Microstrip Trace Spacing (edge to edge)	• between + and - : 7 mils • Between other signals ≥ 25 mils • Transmit and Receive pairs should be interleaved. • For non interleaved pairs interpair spacing ≥ 45 mils.	
Stripline Trace Width	5 mils	
Stripline Trace Spacing (edge to edge)	• between + and - : 7 mils • Between other signals ≥ 25 mils • Transmit and Receive pairs should be interleaved. • For non interleaved pairs interpair spacing ≥ 45 mils.	
Length Matching	• Total allowable pair mismatch on system board ≤ 10 mils • Total allowable interpair trace mismatch for a lane that consists of system board and an add-in card < 15 mils • Length matched on a segment by segment basis.	
AC coupling capacitor	• 75 nF - 200 nF located at the transmitter	
Total Trace Length - (Transmitter/Receiver) from device signal pin to AC coupling capacitor and AC coupling capacitor to PCI Express device pin	• 1" - 30" max.	
Via counts	4 vias or less	

Table 37. Layout Checklist (Sheet 2 of 14)

Checklist Items	Recommendations	Comments
PCI Express Baseboard (for Motherboard-Adapter Card) Layout Recommendations (PETP[7:0]/PETN[7:0],PERP[7:0],PERN[7:0])		Refer to Section 5.2.2
Reference Plane	Routing over unbroken ground plane is preferred. If unbroken ground plane is not available route over unbroken voltage plane.	
Trace Impedance motherboard	• Single -ended: 50 ohms +/- 15% • Differential microstrip: 85 ohms +/- 15%	
Trace Impedance adapter card	• Single Ended: 60 +/-15% ohms nominal • Differential: 100 +/-15% ohms nominal	
Microstrip Trace Width	5 mils	
Microstrip Trace Spacing (edge to edge)	• between + and - : 7 mils • Between other signals ≥ 25 mils • Transmit and Receive pairs should be interleaved. If interleaving • For non interleaved pairs interpair spacing ≥ 45 mils.	
Stripline Trace Width	5 mils	
Stripline Trace Spacing (edge to edge)	• Between + (P) and - (N) of pair: 7 mils • Between other signals ≥ 25 mils • Transmit and Receive pairs should be interleaved. • For non interleaved pairs interpair spacing ≥ 45 mils.	
Length Matching	• Total allowable length skew between + and - signals of the pair length mismatch on a base board must not exceed 25 mils. • Total allowable length skew between + and - signals of the pair trace mismatch for a lane that consists of a base board and an add-in card must not exceed 15 mils. • Total skew across all lanes must be less than 20 ns.	
AC coupling capacitor	• 75nF - 200 nF located at the transmitter	
Total Trace Length - (Transmitter/Receiver) from device signal pin to AC coupling capacitor and AC coupling capacitor to PCI Express device pin	• 1.0" - 27" max	
Total Length: Topology 2: transmitter on adapter card and the PCI-E device receiver on motherboard	• 1.0" min. - 25" max.	
Via counts	4 vias or less	

Table 37. Layout Checklist (Sheet 3 of 14)

Checklist Items	Recommendations	Comments
PCI Express Clock Layout Recommendations (REFCLKP, REFCLKN)		Refer to Section 5.2.3
Reference Plane	Routing over unbroken ground plane is preferred. If unbroken ground plane is not available route over unbroken voltage plane.	
Trace Impedance	Differential target: 100 ohm, tolerance +/-15% Single Ended: 50 ohms +/- 15%	
Trace Width	5 mils	
REFCLKP, REFCLKN differential Clock Pair Spacing	< 1.4 x Space Width	
Serpentine Spacing (spacing of clock lines from itself)	spacing ≥ 25 mils.	
Clock to Other Spacing (edge to edge)	Spacing from clock to other groups ≥ 25 mils.	
Trace Lengths[2]	L1, L1': 0.5" max	
	L2, L2': 0.2" max	
	L3, L3': 0.2" max	
	L4, L4' • Device down: 2" to 15.3" or • Connector: 2" to 11.3	
	Total Length = L1+L2_+L4 • Device Down: 3" to 16" or • Connector: 3" to 12"	
Length Matching Requirements within differential pair	+/- 5 mils	
Rs Series Resistor	33 +/- 5% ohms	
Rt Shunt Resistor	49.9 +/- 1% ohms	
Number of Vias	4 max	

Table 37. Layout Checklist (Sheet 4 of 14)

Checklist Items	Recommendations	Comments
SAS Interface for Compliant Implementations (S_TXP[7:0], S_TXN[7:0], S_RXP[7:0], S_RXN[7:0])		Refer to Section 6.1
Reference Plane	Route over unbroken ground plane.	
Trace Impedance	Differential 100 ohms +/- 15%	
Trace Width	• Microstrip: 5 mils nominal • Stripline: 4 mils nominal	
Trace Spacing edge to edge	• breakout: SAS pair to pair spacing 20 mils ≤ 0.5" of the device ball • Refer to Table 20 for interpair spacing recommendations	Refer to stackup Chapter 3.0
Group Spacing (edge to edge)	• Keep SAS signals ≥ 50 mils away from the other types of signals. • SAS pair to pair spacing may be reduced to ≥ 20 mils in the breakout region within 0.5" of the pin field as necessary	
Compliant: maximum trace length: Motherboard (ball to first connector)	≤ 5" (max)	
Length Matching (between TX+ and TX-) and (between RX+ and RX-)	• ≤ 25 mils • Maintain consistent spacing between P and N signals for achieving differential trace impedance (takes precedence over length matching)	
AC Coupling on TX+, TX- and RX+, RX-	10 nF (low ESR) as close to the pad as possible.	
Vias	• 2 vias per signal between device package ball and connector pin • Board thickness 0.062 inches max for though hole vias. • Drill width 20mils • Note: Reducing the number of vias takes precedence over the AC capacitor placement. • Impedance controlled vias (100% +/-15%) preferred	
PBI Interface (A[24:0], D[15:0]) One, Two and Three Loads		Refer to Section 7.4
Reference Plane	Route over unbroken ground plane or unbroken power plane.	
Recommended Layer	Microstrip or stripline or combination	
Trace Impedance	Motherboard: 50 ohms +/- 15% Add-in Card: 60 ohms +/- 15%	
Trace Spacing (edge to edge)	• ≥ 5 mils between all Address and Data lines • ≥ 20 mils must be maintained from all other signals or vias.	
Breakout TL0	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.	
Trace LengthTL1 single load	0" to 20.0"	
Trace Length TL1 multiple loads	2" to 20.0"	
Trace Length TL2, TL3	0.5" to 2.0" from the last device on the bus.	
Trace Length to strapping resistors TL4	0.5" to 3.0" from the last device on the bus.	
Routing Guideline	Route as daisy-chain only.	
Via counts	8 vias or less	

Table 37. Layout Checklist (Sheet 5 of 14)

Checklist Items	Recommendations	Comments
PCI-X Routing Recommendations (Clocks P_CLK[0-3], PCLKIN, PCLKOUT)		Refer to Section 4.0
Reference Plane	Route over unbroken ground plane.	
Recommended Layer	Stripline	
Trace Impedance: Motherboard	Microstrip: 50 ohm +/- 15%, stripline: 50 ohm +/- 10%	
Trace Impedance: Adapter Card	Microstrip or stripline: 60 ohm +/- 15%	
Trace Spacing (edge to edge)	• between two different clock lines ≥ 25 mils • between two segments of the same clock line ≥ 25 mils • between clock and other signals ≥ 50 mils	
Series Resistors	28 ohms 1% for connectors 26 ohms 1% for embedded	
Trace Length TL1 from buffer to the resistor	1.0″ max	
Total Trace Length: from device ball to device (including resistor segment)	11″ max	
Length Matching:	All clock lines including PCLKOUT to PCLKIN (feedback clock) must be matched to within 25 mils. Refer to Figure 28.	
• Topologies with only embedded devices.	Match clocks to within 25 mils	
• Topologies with only connectors .	• Match clocks to within 25 mils. • Feedback clock should be routed longer to compensate for the adapter card length (2.4″ to 2.6″) + 0.85″ (for the connector delay)	
• Topologies with both slots and devices used in the design	• Match Clocks to within 25 mils • Feedback clock should be routed longer to compensate for the adapter card length (2.4″ to 2.6″) + 0.85″ (for the connector delay) • PCLK's going to the embedded devices must be compensate for the adapter card length (2.4″ to 2.6″) + 0.85″ (for the connector delay)	
Vias	≤ 2 vias	
PCI-X Point to Point Signals (REQ#, GNT#)		
Signal Group	REQ# and GNT# lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	14 mils microstrip and 12 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing: Spacing from other groups	25 mils minimum, edge to edge	
Trace Length TL1 - from buffer to the connector	• 0.5″ min - 4.5″ max for 100MHz • 0.5″ - 12.0″ for 100MHz • 0.5″ - 15.0″ for 66MHz	
Trace Length TL2 - from connector to the receiver	2.4″ - 2.6″ max	
Vias	≤ 3 vias	

Table 37. Layout Checklist (Sheet 6 of 14)

Checklist Items	Recommendations	Comments
PCI-X 133 MHz Single Slot Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	14 mils microstrip 12 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	14 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from SL ball to the connector	1.0" - 6.0" max	
Lower AD: Trace Length TL2 - from connector to the receiver	0.75" - 1.5" Max	
Upper AD: Trace Length TL1 - from SL ball to the connector	0.5" - 5.0" max	
Upper AD: Trace Length TL2 - from connector to the receiver	1.75" - 2.75" Max	
Vias	$\leq$ 2 vias	
PCI-X 133 MHz Embedded Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	14 mils microstrip 12 mils stripline	
Group Spacing edge to edge	Spacing from other groups: 25 mils minimum	
Trace Length TL1 - from SL ball to the junction	0.75" min - 2.5" max	
Trace Length TL2, TL4 from connector to the receiver	0.75" min - 2.5" Max	
Trace Length TL3 from junction to junction	0.75 "min. to 2.5" max	
Vias	$\leq$ 3 vias	

Table 37. Layout Checklist (Sheet 7 of 14)

Checklist Items	Recommendations	Comments
PCI-X 133 MHz Mixed Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 stripline	
Group Spacing edge to edge	Spacing from other groups: 25 mils minimum	
Lower AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.0″ max	
Lower AD: Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Lower AD: Trace Length TL3, from junction to CONN	0.5″ min. to 3.5″ max	
Lower AD: Trace Length TL4, from CONN to adapter	0.75″ min. to 1.5″ max	
Upper AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.0″ max	
Upper AD: Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Upper AD: Trace Length TL3, from junction to CONN	0.5″ min. to 2.25″ max	
Upper AD: Trace Length TL4, from CONN to adapter	1.75″ min. to 2.75″ max	
Vias	< 3 vias	

Table 37. Layout Checklist (Sheet 8 of 14)

Checklist Items	Recommendations	Comments
PCI-X 100 MHz Slot Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 stripline	
Group Spacing edge to edge	Spacing from other groups: 25 mils minimum	
Lower AD: Trace Length TL1 - from ball to the junction	0.5″ - 12.0″ max	
Lower AD: Trace Lengths TL3 - Between connectors	0.5″ - 3.0″ max	
Lower AD: Trace Lengths TL2 - from connector to the first receiver, TL4 - from connector to the second receiver	0.75″ - 1.50″ max	
Upper AD: Trace Length TL1 - from ball to the junction	0.5″ - 10.0″ max	
Upper AD: Trace Lengths TL3 - Between connectors	0.5″ - 3.0″ max	
Upper AD: Trace Lengths TL2 - from connector to the first receiver, TL4 - from connector to the second receiver	1.75″ - 2.75″ max	
Vias	< 3 vias	
PCI-X 100 MHz Embedded Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	14 mils microstrip and stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5″ min. to 3.0″ max (3 loads, 5 loads)	
Trace Length TL3, TL5, TL7, TL9: from junction to junction	0.5″ min. to 2.0″ max (3 loads) 0.5″ min. to 1.0″ max (5 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10: from junction to receiver	0.5″ min. to 3.0″ max (3 loads) 0.5″ min to 2.0″ max (5 loads)	
Vias	≤ 4 vias	

Table 37. Layout Checklist (Sheet 9 of 14)

Checklist Items	Recommendations	Comments
PCI-X 100 MHz Mixed Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip and 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.5″ max	
Lower Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Lower Trace Length TL3, from junction to first CONN and TL5, from junction to second CONN	0.5″ min. to 3.5″ max	
Lower Trace Length TL4, from 1st CONN to AD2 Lower AD: Trace Length TL6, from 2nd CONN to AD3	0.75″ min. to 1.5″ max	
Upper AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.5″ max	
Upper AD: Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Upper AD: Trace Length TL3, from 1st junction to first CONN	0.5″ min. to 3.0″ max	
Upper AD: From 2nd junction to second CONN	0.5″ min. to 3.5″ max	
Upper AD: Trace Length TL4, from 1st CONN to AD2 Upper AD: Trace Length TL6, from 2nd CONN to AD3	1.75″ min. to 2.75″ max	
Vias	≤ 3 vias	

Table 37. Layout Checklist (Sheet 10 of 14)

Checklist Items	Recommendations	Comments
PCI-X 66 MHz Slot Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	12 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from ball to the connector	0.5" - 12.0" max	
Lower AD: Trace Lengths TL3, TL5, TL7 - Between connectors	0.5" - 2.0" max	
Lower AD: Trace Lengths TL2, TL4, TL6, TL8- from connector to the receivers	0.75" - 1.50" max	
Upper AD: Trace Length TL1 - from ball to the connector	0.5" - 9.0" max	
Upper AD: Trace Lengths TL3, TL5, TL7 - Between connectors	0.5" - 2.0" max	
Upper AD: Trace Lengths TL2, TL4, TL6, TL8- from connector to the receivers	1.75" - 2.75" max	
Vias	≤ 4 vias	
PCI-X 66 MHz Embedded Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5" min. to 3.0" max (8 loads) 0.5" min. to 3.5" max (6 loads)	
Trace Length TL3, TL5, TL7, TL9,TL11,TL13,TL15: from junction to junction	0.5" min. to 1.5" max (8 loads) 0.5" min. to 2.5" max (6 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10,TL12,TL14,TL16: from junction to receiver	0.5" min. to 1.5" max (8 loads) 0.5" min to 2.0" max (6 loads)	
Vias	≤ 4 vias	

Table 37. Layout Checklist (Sheet 11 of 14)

Checklist Items	Recommendations	Comments
PCI-X 66 MHz Mixed Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip and 14 mils stripline	
Adapter Card Trace Impedance	60 ohm +/- 15% (microstrip and stripline)	
Adapter Card Trace Spacing	12 mils microstrip and mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 11″ max	
Lower AD: Trace Length TL2, TL4 - from junction to AD1, AD2	0.5″ min. to 4.5″ max	
Lower AD: Trace Length TL3, TL5, TL7 from junction to junction	0.5″ min. to 4.0″ max	
Lower AD: Trace Length TL6 from 1st CONN to AD3, TL8: from 2nd CONN to AD4	0.75″ min. to 1.5″ max	
Upper AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 10″ max	
Upper AD: Trace Length TL2, TL4 - from junction to AD1, AD2	0.5″ min. to 4.0″ max	
Upper AD: Trace Length TL3, TL5, TL7 from junction to junction	0.5″ min. to 4.0″ max	
Upper AD: Trace Length TL6 from 1st CONN to AD3, TL8: from 2nd CONN to AD4	1.75″ min. to 2.75″ max	
Vias	$\leq$ 4 vias	

Table 37. Layout Checklist (Sheet 12 of 14)

Checklist Items	Recommendations	Comments
VCC1P2PLLS0 - VSSPLLS0, VCC1P2PLLS1 - VSSPLLS0 Storage PLL Filters		
Reference Plane	• Ground • VCC1P2PLLS0, VSSPLLS0 and VCC1P2PLLS1, VSSPLLS1 traces must be ground referenced (no V_{CC} references)	
Inductor	• 120 nH +/- 20%, • L must be magnetically shielded • RDC: max < 0.3 ohms • rated at 45 mA	
Capacitor	• 22 µF +/- 20% 6.3V (Capacitor) • ESR: max < 0.3 ohms • ESL < 2.5 nH • Place 22 µF capacitor as close as possible to package pin.	
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2V plane to the top end of the capacitor is > 0.35 Ω (inclusive of board and component resistance) • 1.2V plane to $V_{CC1P2PLL}$ < 1.5 Ω (inclusive of board and component resistance) • resistor must be placed between V_{CC1P2} and L. • Note: if trace and component resistance is large enough a discrete resistor is not required	
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils	
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils	
Trace Spacing	• ≥ 30 mils from any other signals.	
Trace Length maximum	1.2″	
Routing Guideline 1	Route VCC1P2PLLS and VSSPLLS as differential traces.	
Routing Guideline 2	The nodes connecting VCC1P2PLLS and the capacitor must be as short as possible.	

Table 37. Layout Checklist (Sheet 13 of 14)

Checklist Items	Recommendations	Comments
VCC1P2PLLD - VSSPLLP PCI-X PLL Filters		
Reference Plane	• Ground • VCC1P2PLLP, VCC1P2PLLD traces must be ground referenced (no V_{CC} references)	
Inductor	• 4.7 uH +/- 25% 45 mA • L must be magnetically shielded • ESR: max < 0.3 ohms • rated at 45 mA	
Capacitor	• 22 µF +/- 20% 6.3V (Capacitor) • ESR: max < 0.3 ohms • ESL < 2.5 nH • Place 22 µF capacitor as close as possible to package pin.	
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2V plane to the top end of the capacitor is > 0.35 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • 1.2V plane to $V_{CC1P2PLL}$ < 1.5 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • 1/16 W 6.3 V • resistor must be placed between V_{CC1P2} and L. • Note: if trace and component resistance is large enough a discrete resistor is not required	
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils	
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils	
Trace Spacing	• ≥ 30 mils from any other signals.	
Trace Length maximum	1.2″	
Routing Guideline 1	Route VCC1P2PLLD and VSSPLLD, VCC1P2PLLP and VSSPLLP as differential traces.	
Routing Guideline 2	The nodes connecting VCC1P2PLLD and the capacitor, VCC1P2PLLP and the capacitor must be as short as possible.	
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance	

Table 37. Layout Checklist (Sheet 14 of 14)

Checklist Items	Recommendations	Comments
VCC3P3PLLX - VSSPLLX PLL Filters		
Reference Plane	• Ground referenced • VCC3P3PLL and VSSPLLX traces must be ground referenced (no V_{CC} references)	
Inductor	• 4.7 µH • L must be magnetically shielded • ESR: max < 0.4 ohms • rated at 45 mA • An example of this inductor is TDK part number MLZ2012E4R7P.	
Capacitor	• 22 µF 20% 6.3V (Capacitor) • ESR: max < 0.4 ohms • ESL < 3.0 nH • Place 22 µF capacitor as close as possible to package pin.	
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 3.3V plane to the top end of the capacitor is > 0.35 Ω • 3.3V plane to $V_{CC3P3PLL}$ < 1.5 Ω • resistor ratings: 1/16 W 6.3 V • resistor must be placed between V_{CC3P3} and L. • Note: if trace and component resistance is large enough the discrete resistor is not required	
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils	
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils	
Trace Length Max	• 1.2"	
Trace Spacing	• ≥ 30 mils from any other signals.	

13.0 References

The following manuals and specifications may be helpful in designing an application using Intel® 413808 and Intel® 413812 I/O Controllers.

13.1 Relevant Documents

1. *Intel® 413808 and Intel® 413812 I/O Controllers Datasheet*, Intel Corporation
2. *Intel® 413808 and Intel® 413812 I/O Controllers Thermal Guidelines Application Note*, Intel Corporation
3. *PCI Express Specification*, Revision 1.0a
4. PCI Express Base Specification 1.0a
5. PCI Express Card Electromechanical Specification 1.0a
6. *PCI Local Bus Specification*, Revision 2.3 - PCI Special Interest Group
7. *PCI-X Specification,* Revision 1.0b - PCI Special Interest Group
8. *PCI Hot-Plug Specification,* Revision 1.0 - PCI Special Interest Group
9. *PCI Bus Power Management Interface Specification*, Revision 1.1 - PCI Special Interest Group
10. Serial Attached SCSI - 1.1 (SAS 1.1) Specification, ANSI/INCITS 376-2003
11. IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE JTAG-1149.1-1990)
12. The I2C Bus Specification version 2.1 at http://www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf
13. The SMBus Specification at http://www.smbus.org/specs/

Table 38. Design References

Design References
Transmission Line Design Handbook, Brian C. Wadell
Microstrip Lines and Slotlines, K. C. Gupta. Et al.
Design, Modeling and Simulation Methodology for High Frequency PCI-X Subsystems, Moises Cases, Nam Pham, Dan Neal www.pcisig.com
High-Speed Digital Design "A Handbook of Black Magic" Howard W. Johnson, Martin Graham
"Terminating Differential Signals on PCBs", Steve Kaufer, Kelee Crisafulli, Printed Circuit Design, March 1999
"Board Design Guidelines for PCI Express™ Interconnect", http://www.intel.com/technology/pciexpress/downloads/PCI_EI_PCB_Guidelines.pdf

Table 39. Intel Related Documentation

Document Title	Order #
Intel® Packaging Databook	240800

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

To obtain Intel literature write to or call:

Intel Corporation
Literature Sales
P.O. Box 5937
Denver, CO 80217-9808
(1-800-548-4725) or visit the Intel website at http://www.intel.com

13.2 Electronic Information

Table 40. Electronic Information

The Intel World-Wide Web (WWW) Location:	http://www.intel.com
Customer Support (US and Canada):	800-628-8686

Appendix A Appendix

A.1 Terminology

To aid the discussion of Intel® 413808 and Intel® 413812 I/O Controllers, Table 41 provides the terminology used in this document.

Table 41. Terminology and Definitions (Sheet 1 of 2)

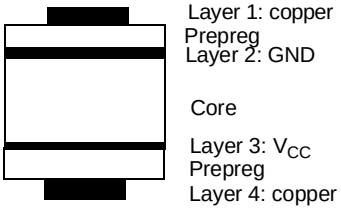
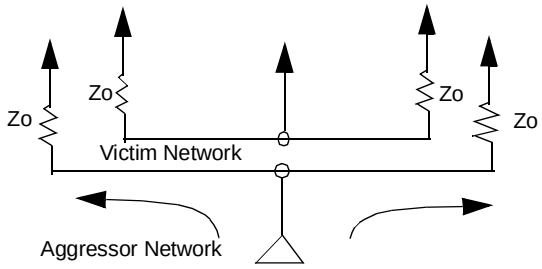
Term	Definition	
Stripline		Stripline in a PCB is composed of the conductor inserted in a dielectric with GND planes to the top and bottom. ***Note:*** An easy way to distinguish stripline from microstrip is that you need to strip away layers of the board to view the trace on stripline.
Microstrip		Microstrip in a PCB is composed of the conductor on the top layer above the dielectric with a ground plane below
Prepreg	Material used for the lamination process of manufacturing PCBs. It consists of a layer of epoxy material that is placed between two cores. This layer melts into epoxy when heated and forms around adjacent traces.	
Core	Material used for the lamination process of manufacturing PCBs. This material is two sided laminate with copper on each side. The core is an internal layer that is etched.	
PCB	 Example of a Four-Layer Stack	Printed circuit board. Example manufacturing process consists of the following steps: • Consists of alternating layers of core and prepreg stacked • The finished PCB is heated and cured. • The via holes are drilled • Plating covers holes and outer surfaces • Etching removes unwanted copper • Board is tinned, coated with solder mask and silk screened
SSTL_2	Series Stub Terminated Logic for 2.5 V	
JEDEC	Provides standards for the semiconductor industry.	
PLL	Phase Lock Loop - A phase-locked loop (PLL) is an electronic circuit with a voltage- or current-driven oscillator that is constantly adjusted to match in phase (and thus lock on) the frequency of an input signal.	

Table 41. Terminology and Definitions (Sheet 2 of 2)

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is aggressor network. 
Victim	A network that receives a coupled cross-talk signal from another network is a victim network.
Network	The trace of a PCB that completes an electrical connection between two or more components.
Stub	Branch from a trunk terminating at the pad of an agent.
ISI	Intersymbol Interference (ISI). This occurs when a transition that has not been completely dissipated, interferes with a signal being transmitted down a transmission line. ISI can impact both the timing and signal integrity. It is dependent on frequency, time delay of the line and the refection coefficient at the driver and receiver. Examples of ISI patterns that could be used in testing at the maximum allowable frequencies are the sequences shown below: 0101010101010101 0011001100110011 0001110001110001111
CRB	Customer Reference Board
Host processor	Processor located upstream from the Intel® 413808 and Intel® 413812 I/O Controllers
Local processor	Intel XScale® processor within Intel® 413808 and Intel® 413812 I/O Controllers
Downstream	• PCI Express: At or toward a PCI Express port directed away from root complex (to a bus with a higher number). • PCI-X: At or toward a PCI bus with a higher number (after configuration) away from host processor.
Upstream	• PCI Express: At or toward a PCI Express port directed to the PCI Express root complex (to a bus with a lower number). • PCI-X: At or toward a PCI bus with a higher number (after configuration) toward host processor.
Local memory	Memory subsystem on the Intel XScale® processor or Peripheral Bus Interface busses.
WORD	16-bits of data.
DWORD	32-bit data word.
QWORD	64-bit data word
Local bus	Internal Bus.
Outbound	At or toward the PCI interface of the ATU from the Internal Bus.
Inbound	At or toward the Internal Bus from the PCI interface of the ATU.
Core processor	Intel XScale® processor within the part.
Flip Chip	FC-BGA (flip chip-ball grid array) chip packages are designed with core flipped up on the back of the chip, facing away from the PCB. This allows more efficient cooling of the package.
Mode Conversion	Mode Conversions are due to imperfections on the interconnect which transform differential mode voltage to common mode voltage and common mode voltage to differential voltage.
ROMB	Raid on motherboard
ODT	On Die Termination - eliminates the need for termination resistors by placing the termination at the chip.

A.2 Simulation Conditions

This section provides the simulation conditions that were used in the analysis for each of the interfaces.

A.2.1 PCI-X Simulation Conditions

The following list provides the PCI-X simulation conditions used in this analysis:

- Simulations were done for 133 MHz, 100 MHz and 66MHz.
- Various combinations of stripline and microstrip routing were analyzed.
- Vias and connectors were modeled using some estimated L and C parasitic values based on previous projects, or commonly used values from the literature.
- Connector Model: distributed PCI/PCI-X connector model
- PCI-X Package Model - Generic PCI-X spec device model
- SL Package Model: ball (RLC) + 1 via (RLC) + Stripline (W element) + 3 via + 1PTH (plated through hole RLC) + 4 via + 1 Ball.
- Motherboard trace: Impedance 50 ohm +/- 15% for stripline.
- Adapter Card Trace: Impedance 60 ohm +/- 15% for both microstrip and stripline.

A.2.2 SAS/SATA Simulation Conditions

The following list provides the SAS/SATA simulation conditions used in this analysis:

- Estimated Package parasitics were modeled as part of the topology.
- Power and ground parasitics are not included in the simulations.
- Stackups were set for nominal spacing, and then tolerance was applied to the line width (Spacing= nominal_line_pitch – actual_line_width).
- Various combinations of stripline and microstrip routing were analyzed.
- Vias and connectors were modeled using some estimated L and C parasitic values based on previous projects, or commonly used values from the literature.
- The HSPICE simulator was used to perform all simulation runs.
- SAS Package Model - package traces modeled using short transmission line segments and estimated minimum and maximum impedance values. Two package trace lengths were modeled, 0.1 inch and 0.75 inch.
- ISI Analysis -A test pattern was chosen that has been shown to be very close to worst case for ISI.

A.2.3 PCI Express Simulation Conditions

The following list provides the SAS simulation conditions used in this analysis:

- Jitter and insertion loss budgets used as per PCI Express Specifications
- AC coupling capacitors 75 nF with low ESL and ESR
- Both receiver and transmitter eyes were evaluated for the PCI Express mask specifications
- Modified worst case ISI pattern (8b/10b was used)
- Both near end and far end crosstalk were taken into consideration
- SSO simulated but the impact was found to be not significant.

A.2.4 PBI Simulation Conditions

The following list provides the PBI simulation conditions used in this analysis:

- System Board Stack up: 50 ohm +/- 15%, single ended impedance
- Add-In Card Stack up: 60 ohm +/- 15% single ended impedance
- Flash Model: RC128J3A
- Latch Model: 74LVC573A
- CPLD Model: XC9500XL TQFP package
- NVRAM Model: Same as flash
- Lossy un-coupled transmission lines were used in simulations.
- Trace spacings were set to three times the height of the trace over the reference plane to avoid crosstalk
- Up to 200ns of cycles for AD lines are examined for every topology and are assumed to be equivalent to subsequent cycles.