Intel® Pentium® 4 Processor VR-Down Design Guidelines

November 2002

Order Number 249891-004

[1]Hyper-Threading Technology requires a computer system with an Intel® Pentium® 4 processor at 3.06 GHz or higher, a chipset and BIOS that utilize this technology, and an operating system that includes optimizations for this technology. Look for systems with the Intel® Pentium® 4 Processor with HT Technology logo which your system vendor has verified utilize Hyper-Threading Technology. Performance will vary depending on the specific hardware and software you use. See the following URL for more information: http://www.intel.com/info/hyperthreading

Contents

Applications and Terminology

This document defines DC-to-DC converters to meet the power requirements of computer systems using Intel microprocessors. Requirements will vary according to the needs of different computer systems and processors that a specific voltage regulator (VR) is expected to support. The "VR" designation in this document refers to an embedded voltage regulator on a system board. Please refer to the VRM 9.1 Design Guidelines for Voltage Regulator Module design guidelines. The major differences between this document and the VRM 9.1 guidelines are:

- This document defines solutions for systems with a single processor; it does not include current-sharing requirements, which are applicable to powering multiple processors.
- Voltages are specified at the processor socket instead of the VRM connector.

This document is specifically intended to meet the needs of systems based on the Intel® Pentium® 4 processor in the 423-pin package, Intel Pentium 4 processor in the 478-pin package, and Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. The specifications in the respective data sheet always take precedence over the data provided in this document, which are guidelines to meet processor requirements.

Each guideline is placed into one of three categories. The category immediately follows the section heading and is one of the following:

REQUIRED:	An essential part of the design—necessary to meet processor voltage and current specifications and follow processor layout guidelines.
EXPECTED:	Part of Intel's processor power definitions: necessary for consistency among the designs of many systems and power devices. May be specified or expanded by system OEMs.
PROPOSED:	Normally met by this type of DC-to-DC converter and, therefore, included as a design target. May be specified or expanded by system OEMs.

1 Output Requirements

1.1 Voltage and Current REQUIRED

The voltage regulator for the Intel® Pentium® 4 processor in the 478-pin package and Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is a DC-DC converter that supplies the required voltage and current to a single processor. A five-bit VID code provided by the processor to the voltage regulator (VR) determines a reference output voltage, as described in Section 3.1. Sections 1.2 and 1.3 specify deviations from the VID reference voltage.

Table 1, VRD Output Voltage and Current Ratings

Symbol	Parameter	Processor	Minimum	Typical	Maximum
V_{VID} (V)	Reference output voltage selected by VID outputs from processor	1 2		1.750 1.500	
V_{CC_CORE} (V)	Output voltage measured at Vcc and Vss pins on solder side of processor socket		See Figure 1 and Table 2		
V_{MAX} (V)	Non-operating (failure) voltage	1 2			2.10 1.75
Icc_max (A)	Maximum current the processor draws during operation	1 2			57.4 70[3]

Notes:
1. Intel Pentium 4 processor in the 478-pin package
2. Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process
3. Design target covering the load line in Figure 1 and Table 2; each specific motherboard design will have an output current requirement determined by the processor frequencies it supports.

1.2 Voltage Tolerance REQUIRED

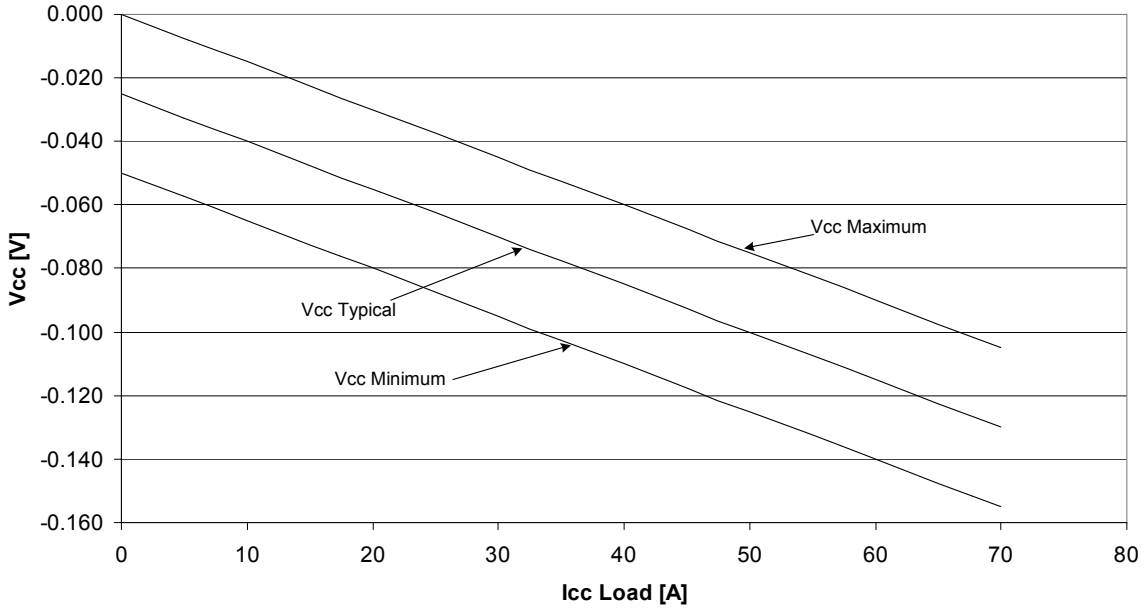
The voltage measured at the processor must be within the range shown in Section 1.3. Measurements are based on socket voltages measured at processor Vcc and Vss pins. Data in the processor data sheet always take precedence over the data provided in this document.

Voltage tolerance includes:
- Initial DC output voltage set-point error
- Component aging effects
- Output ripple and noise
- Full ambient temperature range and warm up.
- Static operation
- Dynamic output load changes from minimum-to-maximum or maximum-to-minimum loads specified in the load lines in section 1.3, as measured over a 100 MHz bandwidth.

The load lines in Section 1.3 show the relationship between Vcc and Icc for the Intel Pentium 4 processor in the 478-pin package and Pentium 4 processor with 512-KB L2 cache on 0.13 micron process, and also the tolerances from Vcc_typical to Vcc_min and Vcc_max.

1.3 Load Line Definitions REQUIRED

The following load lines contain DC and transient-droop data, as well as maximum and minimum voltage levels. The voltages are measured at the processor socket Vcc and Vss pins. The following figure and table show load-line voltage offsets and current levels based on the VID (maximum) voltage settings specified in. The load-line slopes are same for Pentium 4 in the 478 Package and Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.



Notes:
1. The load line specification includes both static and transient limits.
2. This load line specification applies to both the Pentium 4 processor in the 478-pin package and the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
3. The VID voltage has been normalized to zero; i.e., the graph shows the voltage offset to the VID voltage

Figure 1: Load Line at Processor Socket

Table 2, Load Line at Processor Socket

Icc (A)	Voltage Deviation from VID Setting (V)		
	Minimum	Typical	Maximum
0	-0.050	-0.025	0.000
5	-0.057	-0.033	-0.008
10	-0.065	-0.040	-0.015
15	-0.072	-0.047	-0.023
20	-0.080	-0.055	-0.030
25	-0.087	-0.063	-0.038
30	-0.095	-0.070	-0.045
35	-0.103	-0.077	-0.053
40	-0.110	-0.085	-0.060
45	-0.118	-0.092	-0.067
50	-0.125	-0.100	-0.075
55	-0.133	-0.108	-0.083
60	-0.140	-0.115	-0.090
65	-0.148	-0.123	-0.097
70	-0.155	-0.130	-0.105

Notes:
1. The load line specification includes both static and transient limits.
2. This load line specification applies to both the Pentium 4 processor in the 478-pin package and the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
3. The VID voltage has been normalized to zero; i.e., the table shows the voltage offset to the VID voltage

1.4 Processor Electrical And Thermal Current Support EXPECTED

System boards supporting Intel Pentium 4 must include voltage regulator designs compliant to motherboard electrical and thermal standards. This includes full electrical support of 70A Icc_max specifications and robust cooling solutions to support 63A thermal design current (TDC) indefinitely within the envelope of the system's operating conditions.

TDC is the sustained (DC equivalent) current that the Pentium 4 processor is capable of drawing indefinitely and defines the current to use for worst-case voltage regulator temperature assessment. At TDC, voltage regulator components (such as switching FETs and inductors) reach maximum temperature and may heat the motherboard layers and neighboring components above their thermal limits. Actual component and board temperatures are established by the envelope of system operating conditions. This includes but is not limited to the voltage regulator layout, processor fan selection, ambient temperature, chassis configuration, etc. To avoid heat related failures, system boards must be validated for thermal compliance at TDC under the envelope of the system's operating conditions.

1.5 No-Load Operation EXPECTED

The VR should operate in a no-load condition: i.e., with no processor installed. The VR does not need to meet the output regulation specifications described in section 1.3, but its output must not exceed 110% of the value of the maximum DC output voltage, and it must not trigger over-voltage fault detection circuitry.

1.6 Turn-on Response Time PROPOSED

The processor socket voltage should reach its specified range within 50 ms of the input power reaching its minimum voltage. Please refer to the next paragraph and related figures for complete power up timing requirements.

1.7 Processor Power Sequencing REQUIRED

The Pentium 4 processor in the 478-pin package and Pentium 4 processor with 512-KB L2 cache on 0.13 micron process require a 1.2V supply to the VCCVID pin to support the on-die VID generation circuitry. The current requirement for this voltage is approximately 30mA, typically from a linear regulator. The on-die VID generation circuitry also has power sequencing requirements. Figure 2 shows a block diagram of a power sequencing implementation. Figure 3 and Figure 4 illustrate timing diagrams of the power sequencing requirements.

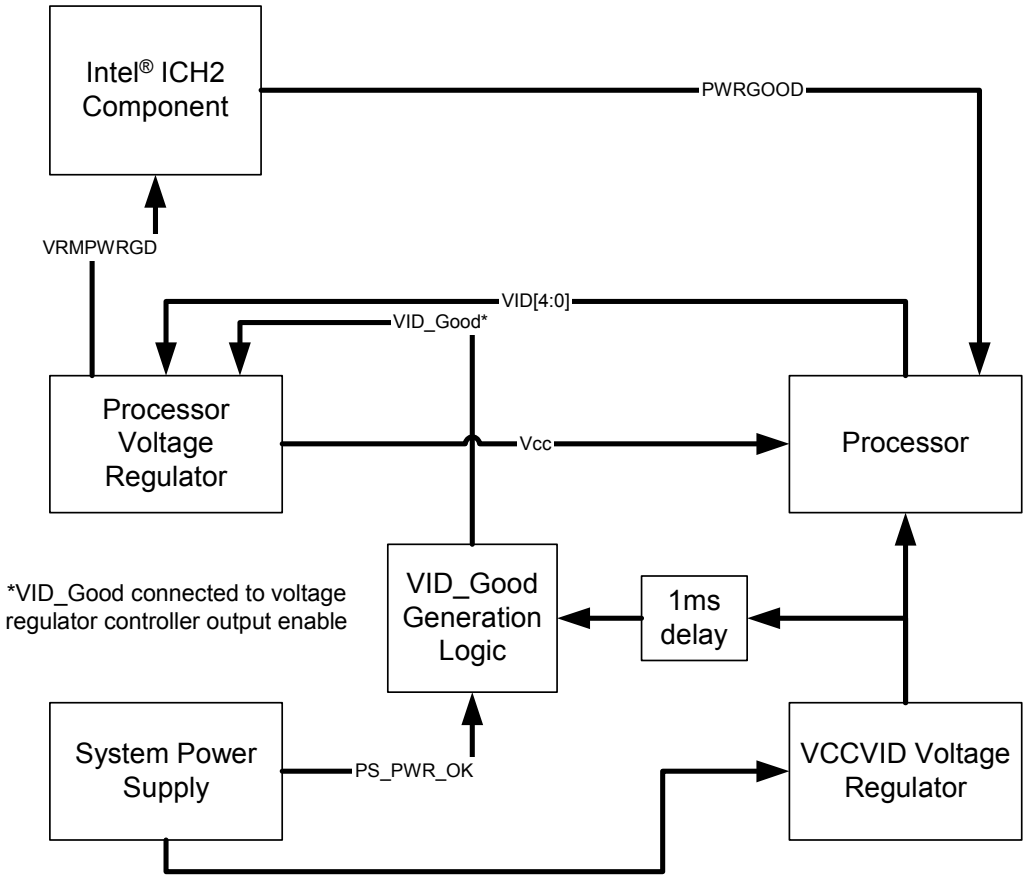
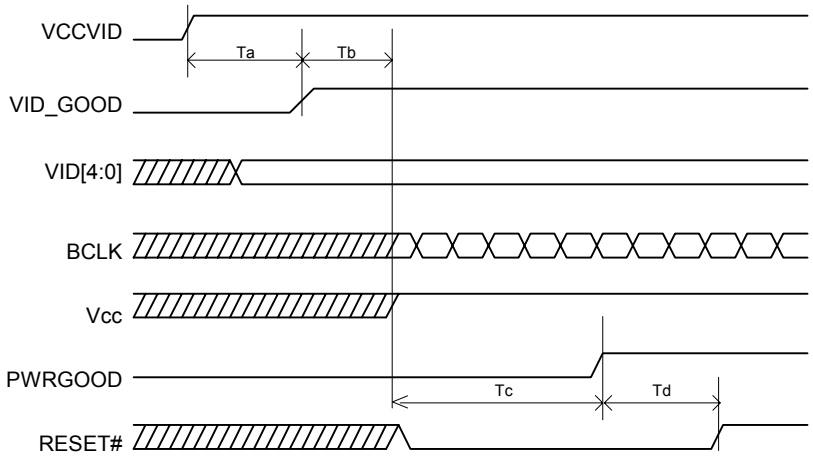


Figure 2: Power Sequencing Block Diagram



Ta= 1ms minimum (VCCVID > 1V to VID_GOOD high)
Tb= 50ms maximum (VID_GOOD to Vcc valid maximum time)
Tc= T37 (PWRGOOD inactive pulse width) = 10 BCLKs min
Td= T36 (PWRGOOD to RESET# de-assertion time) = 1ms(min), 10ms(max)

Note: VID_GOOD is not a processor signal. This signal is routed to the output enable pin of the voltage regluator control silicon.

Figure 3: Power-on Sequence Timing Diagram

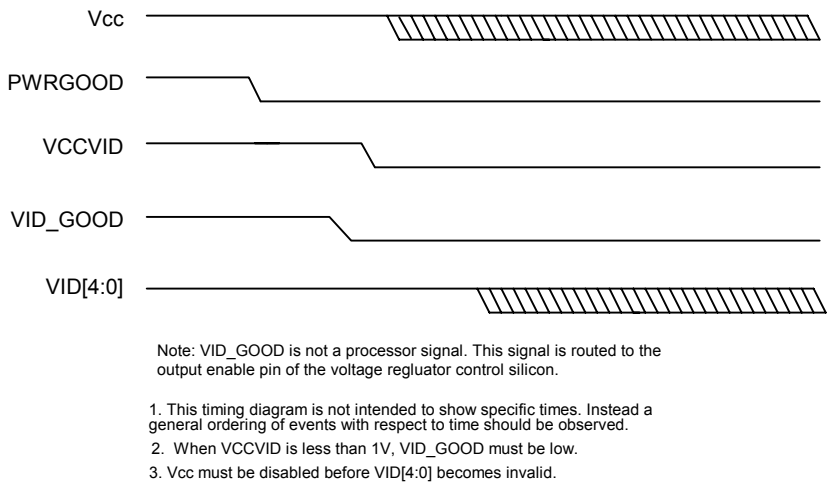


Figure 4: Power-off Sequence Timing Diagram

1.8 Overshoot at Turn-On or Turn-Off REQUIRED

Overshoot upon the application or removal of the input voltage must be such that Vcc does not exceed the limits specified in Section 1.3. No negative voltage may be present on any output during turn-on or turn-off.

1.9 Converter Stability REQUIRED

The VR needs to be unconditionally stable under all output voltage ranges and current transients. Stability requirements include a Thermal Monitor operating condition in which the processor may periodically stop to reduce its power dissipation in response to a high-temperature alert. Figure 5 shows worst-case Thermal Monitor operation (maximum current in the ON state).

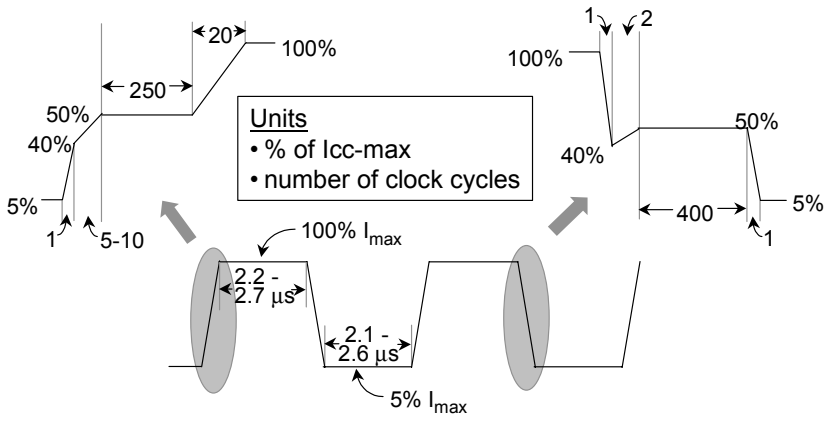


Figure 5: Processor Current during Thermal Monitor Operation

Notes:

- Duration of on-off periods depends on processor speed: faster processors have shorter durations.
- Other operating system-controlled events could have on-times as short as 700 internal clock cycles.
- A possible worst-case routine could cause processor Icc to go through a 100% → 40% → 100% set of transitions within 30-50 cycles.

1.10 Thermal Monitoring PROPOSED

This section describes how to protect the voltage regulator design from heat damage while supporting thermal design current (TDC) specifications. It is included for reference and is applicable to Intel® Pentium® 4 processors supporting Hyper-Threading Technology[1] operating at 3.06 GHz or higher. Intel does not recommend integrating this feature into Vcc PWM controller designs. Each customer is responsible for identifying maximum temperature specifications for all components in the voltage regulator design and ensuring that these specifications are not violated while continuously drawing specified TDC levels. In the event of a catastrophic thermal failure, the thermal monitoring circuit is to assert the Pentium 4 processor signal PROCHOT# immediately prior to exceeding maximum motherboard and component thermal ratings to prevent heat damage. Assertion of this signal will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Assertion of PROCHOT# degrades system performance and must never occur when drawing less than specified thermal design current.

VR temperature violations can be detected using a thermal sensor and associated control circuitry (see Figure 6). For this implementation, a thermistor (THMSTR) is placed in the temperature sensitive region of the voltage regulator. The location must be chosen carefully and is to represent the position where initial thermal violations are expected to occur. When exceeded, the thermal monitor circuit is to initiate PROCHOT# to protect the voltage regulator from heat damage.

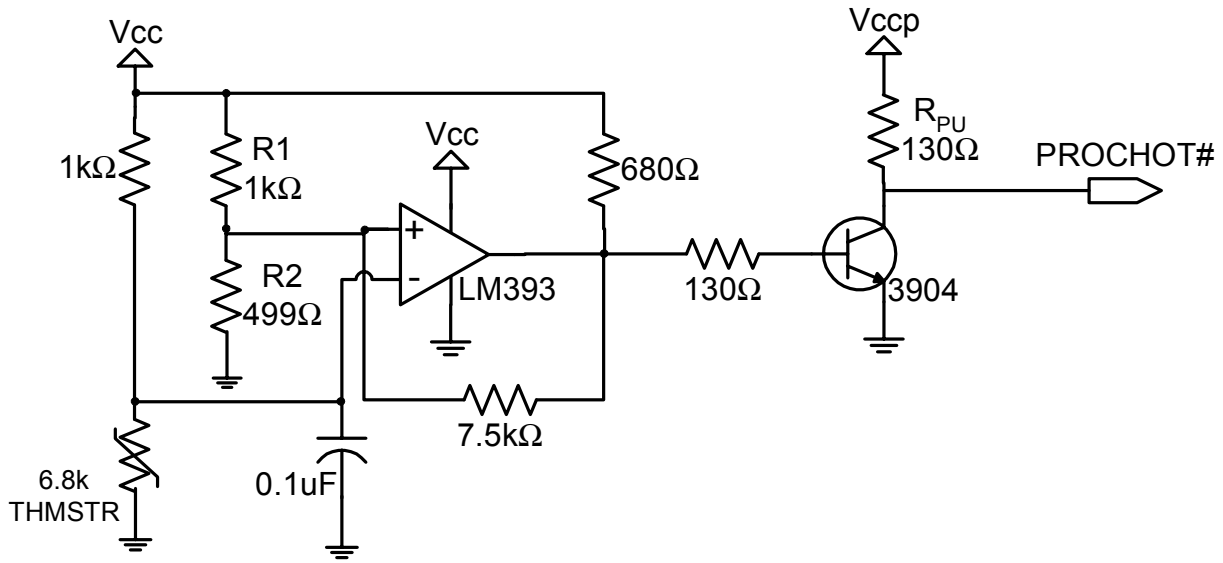


Figure 6: Typical VR Thermal Monitor Circuit Design

Assertion of PROCHOT# is governed by the comparator (LM393) using the sensor voltage (at the negative comparator terminal) and a trigger reference voltage (at the positive comparator terminal). As the thermistor temperature increases due to system loading, the resistance will decrease. When the voltage drop across the thermistor falls below the trigger reference voltage, established by R1 and R2, the comparator will change state and bias the bipolar transistor (BJT). When biased, the BJT provides the active low signal assertion of PROCHOT# compliant to signaling specifications (see Table 3).

Table 3, Thermal Monitor Specifications

Parameter	Specification		Units
	Minimum	Maximum	
Termination voltage †	(Vcc)		Volts
Output on (low) resistance		11	Ohms
Output leakage current		200	Microamperes
Transition time	0.550	100	Nanoseconds
Time in or out of Thermal Monitor state	1.0		Milliseconds
R_{PU} (Pull-up Resistor)†	130Ω +/- 5%		Ohms

† The thermal monitor circuit is to use a single motherboard pull up resistor to bias the BJT collector. This is provided in the PROCHOT# circuit design. Additional termination must not be integrated into the thermal monitoring circuit.

PROCHOT# is an open-drain, active-low i/o buffer terminated to the system Vtt (FSB termination voltage). To maintain reliable signaling between thermal monitor circuit, processor, and chipset, the bipolar transistor must be selected to operate with a collector bias established using a single 130Ω pull-up resistor. Use of additional termination or pull-up resistors may lead to signal integrity or logic threshold failures.

The values for R1 and R2 in Figure 6 are included as an example and must be calculated using specific design parameters. The value of R2 is adjusted to calibrate the comparator's trigger reference voltage (and assertion of PROCHOT#) against the sensor voltage representing a thermal violation.

2 Input Voltage and Current

2.1 Input Voltages REQUIRED

The main power source for the VR is 12V +5%, -8%. This voltage is supplied by a conventional computer power supply through a cable to the system board. The system board will supply local bulk bypassing on the 12V rail. Adequate connector current handling capacity must be part of system power budgeting.

2.2 Load Transient Effects on Input Current EXPECTED

When the VR is providing an output current step to the load from $Iout_{MIN}$ to $Iout_{MAX}$ or $Iout_{MAX}$ to $Iout_{MIN}$ at the slew rate of 350A/us at the processor, the slew rate of the input current to the VR should not exceed 0.5A/µsec. The system board needs sufficient bulk decoupling to ensure that the supply voltage on the system board does not go outside of regulation requirements during VR load transients.

3 Control Inputs REQUIRED

3.1 Output Enable—(OUTEN)

The VR should accept an open-collector, open-drain, open-switch-to-ground, low-voltage TTL or low-voltage CMOS signal to enable the output. The input should have a pull-up resistor between 1 kΩ and 10 kΩ to a maximum voltage of 3.3V. The maximum low-input voltage is 0.8V; the minimum high-input voltage is 1.7V. When disabled, the VR should not sink or source current. When Output Enable is pulled low during the shutdown process, the VR should not exceed its previous voltage level regardless of the VID setting.

3.2 Voltage Identification—(VID [0:4])

The VR must accept five input lines to set the nominal voltage as defined by the table below. Five processor pins (VID[4:0]) will have either an open-ground combination (Pentium 4 processor in the 478-pin package) or open-drain driver outputs (Pentium 4 processor with 512-KB L2 cache on 0.13 micron process). When all five VID inputs are high (11111), such as when no processor is installed, the VR should disable its output.

The maximum low-input voltage is 0.8V; the minimum high-input voltage is 1.7V. Each VID input should have a 1 kΩ ± 10% pull-up resistor to 3.3V ± 5%. Board designers using other values should check them against data sheets for the VR components and the processor.

Table 4, Voltage Identification (VID)

Processor Pins (0 = low, 1 = high)					Vcc	Processor Pins (0 = low, 1 = high)					Vcc
VID4	VID3	VID2	VID1	VID0	(VDC)	VID4	VID3	VID2	VID1	VID0	(VDC)
1	1	1	1	1	Off	0	1	1	1	1	1.475
1	1	1	1	0	1.1	0	1	1	1	0	1.5
1	1	1	0	1	1.125	0	1	1	0	1	1.525
1	1	1	0	0	1.15	0	1	1	0	0	1.55
1	1	0	1	1	1.175	0	1	0	1	1	1.575
1	1	0	1	0	1.2	0	1	0	1	0	1.6
1	1	0	0	1	1.225	0	1	0	0	1	1.625
1	1	0	0	0	1.250	0	1	0	0	0	1.65
1	0	1	1	1	1.275	0	0	1	1	1	1.675
1	0	1	1	0	1.3	0	0	1	1	0	1.7
1	0	1	0	1	1.325	0	0	1	0	1	1.725
1	0	1	0	0	1.35	0	0	1	0	0	1.75
1	0	0	1	1	1.375	0	0	0	1	1	1.775
1	0	0	1	0	1.4	0	0	0	1	0	1.8
1	0	0	0	1	1.425	0	0	0	0	1	1.825
1	0	0	0	0	1.45	0	0	0	0	0	1.85

4 Power Good Output (PWRGD) PROPOSED

The VR should provide an open collector PWRGD signal consistent with TTL DC levels. On power-up the PWRGD signal remains in the low-impedance state until the output voltage has stabilized, and transition to the open (>100kΩ) state within 10 milliseconds of the output voltage stabilizing within the range specified in Section 1.3. After the output voltage has stabilized, the signal should be in the low-impedance (to ground) state whenever Vcc is outside of the required range below and be in the open state whenever Vcc is within its specified range.

This output should be capable of sinking up to 4mA, while maintaining a voltage of 0.4V or lower. When the output is in the open state it should be capable of withstanding up to 3.3V. Latch-up or damage cannot occur if the pull-up voltage on the system board is present with no +12V input present.

The maximum PWRGD voltage should be the maximum Vcc specified in Section 1.3 plus margin to prevent false de-assertion, but never higher than VID plus 250 mV.

The minimum voltage at which PWRGD is asserted should be the minimum Vcc specified in Section 1.3**,** minus margin to prevent false de-assertion, but at least 95% of (VID minus 175mV).

VR PWRGD should remain low if the Output Enable control disables the VR.

Please refer to Section 1.7 for power up timing requirements.

5 Efficiency PROPOSED

The efficiency of the VR should be greater than 80% at maximum output current and input voltage. It should not dissipate more power under any load condition than it does at maximum output current and maximum input voltage.

6 Fault Protection

6.1 Over Voltage Protection EXPECTED

The VR should provide over-voltage protection (OVP) by including a circuit, separate from the voltage sense path, capable of shutting off the output drive when the output voltage rises beyond Vtrip. If practical, the protection circuit should also enable a low-resistance path to ground such that if the output transistor shorts to input power the output voltage will not rise above Vtrip. A non-resettable or resettable fuse may be included in the input of the VR for this function. The response time should be such that the output voltage will not exceed the non-operating VMAX in Table 1 corresponding to the selected VID.

Minimum Vtrip should be the Maximum Vout specified in Section 1.3 plus margin to prevent false trips. No combination of input voltage sequences should falsely trigger an OVP event.

6.2 Fuse Protection for Power Input PROPOSED

The power input (12V) should be protected with a fuse rated not greater than 30A, which sustains all operating and inrush conditions and which "blows" only on catastrophic failure of the converter.

6.3 Overload Protection EXPECTED

The VR should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. Output current under this condition will be limited to no more than 150% of the maximum rated output of the VR. Latching off or hiccup mode is acceptable during over-current conditions. The VR should be capable of starting into a constant current load of 50% of maximum rated load current with maximum load capacitance, as defined in Section 1.3, without tripping the Over Current Protection (OCP) circuitry.

6.4 Reset After Shutdown PROPOSED

If the VR goes into a shutdown state due to a fault condition on its output (not an internal failure) it should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.