



Voltage Regulator-Down (VRD) 10.0

Design Guide
For Desktop Socket 478

February 2004

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Revision History

Revision Number	Description	Revision Date
-001	<ul style="list-style-type: none"> • Initial Release. 	April 2003
-002	<ul style="list-style-type: none"> • Corrected load line formula in Section 2.2. 	November 2003
-003	<ul style="list-style-type: none"> • Added Section 1.1 Terminology and Table 2. Glossary. • Section 2.2 added Tables 3 – 5, 10; modified Tables 6 – 9 and Figures 1 –4. • Added Section 2.3 TOB: Tolerance Band. • Renumbered Sections 2.4 – 2.10 to Sections 2.5 – 2.11 • Added Section 2.8.1 Validation summary, Figures 10 – 11 • Added Section 2.9.1 Specification Overview and Figures 12 – 14. • Added 2.9.2 Example: Socket Vcc Overshoot Test • Modified Section 2.10 • Modified Section 4.2 • Modified Section 6.2 • Added Section 8 Motherboard Power Plane Recommendations • Added Section 8.1 Minimize Power Path Resistance • Added Section 8.2 Minimize Power Delivery Inductance • Added Section 8.3 Four Layer Boards • Added Section 8.4 Six Layer Boards 	February 2004

1 Introduction

This document defines the power delivery feature set necessary to support Intel processors' Vcc power delivery requirements for desktop computer systems using socket 478. This includes design recommendations for DC-to-DC regulators which convert the 12 V supply to the processor consumable Vcc voltage along with specific feature set implementation such as thermal monitoring and Dynamic Voltage Identification.

Hardware solutions for the Vcc regulator are dependent upon the microprocessors to be supported by a specific motherboard. At this time, four different VRD hardware configurations have been defined for socket 478 processors. The Vcc regulator design on a specific board must meet the specifications of all processors supported by that board. The voltage regulator configuration for a given processor is defined in that processor's datasheet. In some instances, this data is not published and the proper mapping of processor to VRD configuration can be found

Table 5 or from an authorized Intel representative.

The voltage regulator-down (VRD) designation of this document refers to a regulator with all components mounted directly on the motherboard for intent of supporting a single processor. For the corresponding documentation detailing voltage regulator modules (VRM) or a multiple-processor VRD, please refer to the VRM 10 and EVRD 10 design guidelines document.

VRD 10 incorporates functional changes from previous VRD standards:

- Addition of Dynamic Voltage Identification (D-VID): Ability to change the Vcc reference by request of the processor (Section 2.8)
- Simplified definition of power-good as a power-up indication (Section 6.1)
- VRD recognition of processor induced off states (Section 3.2)
- Thermal monitoring of the VRD (Section 6.2).
- V_{CC} Overshoot specification (Section 2.9)

1.1 Terminology

Table 1. Design Guideline Requirement Categories

Term	Description
REQUIRED	An essential feature of the design that must be supported to ensure correct processor and VRD functionality.
EXPECTED	A feature to ensure correct VRD and processor functionality that can be supported using an alternate solution. The feature is necessary for consistency among system and power designs and is traditionally modified only for custom configurations. The feature may be modified or expanded by system OEMs if the intended functionality is fully supported.
PROPOSED	A feature that adds standard functionality to the VRD and, therefore, is included as a design target. May be specified or expanded by system OEMs.

Table 2. Glossary

Term	Description
Socket 478	Processor socket
DAC	Digital to Analog Converter
DCR	Direct Current Resistance
D-VID	Dynamic Voltage Identification. A low power mode of operation where the processor instructs the VRD to operate at a lower voltage.
ESL	Effective series inductance
ESR	Effective series resistance.
FET	Field Effect Transistor
FMS	Flexible Mobile Specifications for transportable platform design
FR 4	A type of printed circuit board (PCB) material
HVM	High volume manufacturing
I_{cc} , V_{cc}	Processor current, processor voltage
Loadline	A mathematical model that describes voltage current relationship given system impedance (R_{LL}). The loadline equations is $V_{cc} = VID - I \cdot R_{LL}$
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
RDS-ON	FET source to drain channel resistance when bias on.

Term	Description
R _{LL}	Socket loadline impedance. Defined as the ratio: Voltage droop/current step. This is the loadline slope defined across specific nodes at the processor-socket interface.
RSS	Root Sum Square. A method of adding statistical variables
PROCHOT#	Under thermal monitoring, the VRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal places the processor in a low power state, thereby cooling the voltage regulator.
Slope	Loadline resistance. See R _{LL}
Socket Loadline	Defines the characteristic impedance of the motherboard power delivery circuit to the node of regulation. Not the same as the processor loadline that is published in the datasheet, which is defined across the processor V _{ccsense} and V _{ssense} pins. In conjunction with high frequency decoupling, design compliance to this parameter ensures that the processor voltage specifications are satisfied.
Static Loadline	The PWM controlled constant resistance at the defined socket-motherboard interface reference nodes. Also known as the DC loadline or resistance at the defined regulation node. Defined as the quotient of voltage and current (V/I) under steady state conditions. This value is configured by proper tuning of the PWM controller voltage positioning circuit.
Thermal Monitor	A feature of the voltage regulator that places the processor in a low power state when critical VRD temperatures are reached, thereby reducing power and VRD temperature.
TOB	V _{cc} regulation tolerance. Defines the voltage regulator's maximum, 3- σ voltage variation across temperature, manufacturing variation, and age factors. Must be guaranteed by design through component selection. Defined at maximum current and VID levels.
Transient Loadline	A metric that is used as a measure of transient noise. The larger the number, the larger the V _{cc} noise. The parameter equals dV/di or V _{droop} /I _{step} & is controlled by switching frequency, decoupling capacitor selection, motherboard layout parasitics.
V _{cc} , I _{cc}	Processor core voltage and current, defined in the processor datasheet.
VID	Voltage Identification: Max voltage at 0 Amps. A code supplied by the processor that determines the reference output voltage to be delivered to the processor power pins. VID is defined in the processor datasheet.
VR_TDC	Thermal Design Current. It is the sustained DC current which the voltage regulator must support under the system defined cooling solution.
VRD	Voltage regulator down. A VR circuit resident on the motherboard.
VRM	Voltage regulator module that is socketed to a motherboard.
V _{tt}	Voltage provided to the processor to drive I/O buffer circuits.



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2 Processor Voltage Requirements

2.1 Voltage and Current (REQUIRED)

A six-bit VID code transmitted by the processor to the VRD determines a reference output voltage as described in Table 18. The loadlines in Section 2.2 define the relationship between Vcc and Icc for the processor at the socket-motherboard interface across pins AC14 and AC15.

Intel performs exhaustive testing against multiple software test vectors and applications to identify valid processor Vcc operating ranges. Failure to satisfy the loadline, loadline tolerance band, and overshoot specifications (Sections 2.2, 2.3 and 2.9) may invalidate Intel warranties and lead to premature processor failure, intermittent system lock-up, and/or data corruption.

2.2 Loadline Definitions (REQUIRED)

To ensure processor reliability and performance, platform DC voltage regulation and transient-droop noise levels must always be contained within the Vccmin and Vccmax loadline boundaries, known at the loadline window. Loadline compliance must be guaranteed across 3-sigma component manufacturing tolerances, thermal variation, and age degradation. Socket loadline boundaries are defined by the following equations in conjunction with the Vcc regulator design parameter values defined in Table 4. Loadline voltage tolerance is defined in Section 2.3. In these equations, VID, R_{LL}, and TOB are known. Plotting Vcc in these equations while varying Icc from 0 A to Iccmax establishes the Vccmax and Vccmin loadlines. Vccmax establishes the maximum DC loadline boundary and Vccmin establishes the minimum AC and DC voltage boundary. Short transient bursts above the Vccmax loadline are permitted; this condition is defined in Section 2.9.

Table 3. Socket Loadline Equations

Loadline	Equation
Vccmax	$V_{cc} = VID - (R_{LL} * I_{cc})$
Vcctyp	$V_{cc} = VID - TOB - (R_{LL} * I_{cc})$
Vccmin	$V_{cc} = VID - 2*TOB - (R_{LL} * I_{cc})$

NOTE: R_{LL} is the socket loadline impedance (slope)

Socket loadline recommendations are established to provide guidance for satisfying processor die loadline specifications, which are defined in the processor datasheet Die loadline requirements must be satisfied at all times and may require adjustment in the socket loadline value.

Table 4. Vcc Regulator Design Parameters

VR Configuration	Iccmax	VR TDC	Dynamic Icc	R _{LL}	TOB	Maximum VID
478_VR_CONFIG_A	91 A	80 A	70 A	1.24 mΩ	±19 mV	1.4 V
478_VR_CONFIG_B	78 A	68 A	55 A	1.3 mΩ	±25 mV	1.4 V
478_VR_CONFIG_C	70 A	63 A	50 A	1.5 mΩ	±25 mV	1.6 V
478_VR_CONFIG_D	91 A	80 A	70 A	1.5 mΩ	±19 mV	1.6 V

VRD transient loadline circuits should meet or exceed rated conditions defined in Table 4. For example, 478_VR_CONFIG_A requires a loadline slope of 1.24 mΩ. A transient loadline slope of 1.0 mΩ will satisfy this requirement without adversely impacting system performance or processor reliability. However, the static loadline condition must be set to the recommended value. Operating at a low loadline resistance will result in higher processor operating temperature, which may result in damage or a reduced processor life span. Processor temperature rise from higher functional voltages may lead to operation at low power states which directly reduces processor performance. Operating at a higher loadline resistance will result in minimum voltage violations which may result in system lock-up, blue screening, or data corruption.

Table 4 provides a comprehensive list of socket 478 voltage regulator design configurations. The specific configuration to be adopted by VRD hardware will depend on the specific processors the design is intended to support. It is common for a motherboard to support processors that require different VR configurations. In this case, the Vcc regulator design must meet the specifications of all processors supported by that board. For example, If a motherboard is targeted to support processors that require 478_VR_CONFIG_A and 478_VR_CONFIG_C, then the voltage regulator must have the ability to support 80 A of VR TDC, 91 A of electrical peak current, satisfy overshoot requirements of Section 2.9 with a dynamic load step of 70 A, satisfy a VRD tolerance band of ±19 mV (see Section 2.3), and have the ability to detect the specific processor installed in the socket and automatically configure the loadline slope (R_{LL}) to the correct value. VR configuration requirements will be defined in processor data sheets. However, Intel is aware that some data sheets do not contain this necessary information and a partial mapping of processors to VR configurations is provided in Table 5.



Table 5. Mapping of Intel Processors to VRD Configurations

Processor	VR Configuration
Intel® Pentium® 4 Processor	478_VR_CONFIG_C
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process at 3.40 GHz	478_VR_CONFIG_D
Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology ¹ Process	478_VR_CONFIG_D
Intel® Pentium® 4 Processor on 90 nm Process ¹	478_VR_CONFIG_A
	478_VR_CONFIG_B
Intel® Celeron® Processor on 0.13 Micron Process in the 478-Pin Package ³	478_VR_CONFIG_C

NOTES:

1. Processor functions under multiple VR configurations. Consult the processor's data sheet for the required configuration.
2. Compatible with most systems designed to Iccmax=70 A. Consult the product datasheet for the actual value of Iccmax.
3. Consult product data sheet for actual Iccmax value

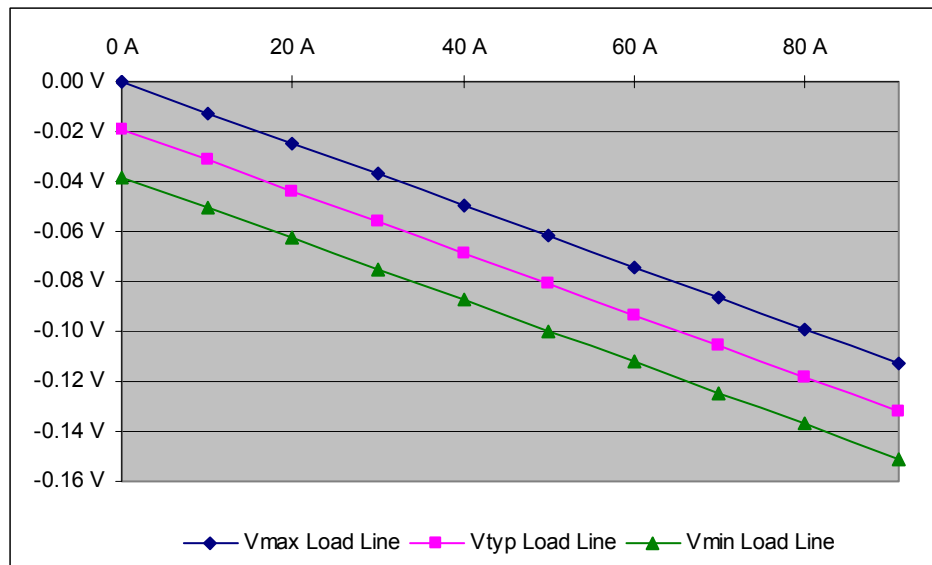
The following tables and figures show minimum and maximum voltage boundaries for each loadline design configuration defined in Table 4. Typical loadline orientation is provided for design reference; designs should calibrate the loadline to the mean of the tolerance band – centered in the loadline window. Note that Intel processors are shipped with a multiple VID values. A single loadline chart and figure for each VRD design configuration can represent functionality for each value. Tables and figures presented as voltage deviation from VID provide the necessary information to identify voltage requirements at any reference VID. This avoids the redundancy of publishing tables and figures for each of the multiple cases.



**Table 6. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_A Presented As a Deviation from VID.
Socket Loadline = 1.24 mΩ, VR Tolerance Band = ±19 mV.**

icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
10 A	-0.012 V	-0.031 V	-0.050 V
20 A	-0.025 V	-0.044 V	-0.063 V
30 A	-0.037 V	-0.056 V	-0.075 V
40 A	-0.050 V	-0.069 V	-0.088 V
50 A	-0.062 V	-0.081 V	-0.100 V
60 A	-0.074 V	-0.093 V	-0.112 V
70 A	-0.087 V	-0.106 V	-0.125 V
80 A	-0.099 V	-0.118 V	-0.137 V
91 A	-0.113 V	-0.132 V	-0.151 V

**Figure 1. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_A Presented As a Deviation from VID.
Socket Loadline = 1.24 mΩ, VR Tolerance Band = ±19 mV.**



**Table 7. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_B Presented As a Deviation from VID.
Socket Loadline = 1.30 mΩ, VR Tolerance Band = ±25 mV.**

I _{cc}	Maximum	Typical	Minimum
0 A	0.000 V	-0.025 V	-0.050 V
10 A	-0.013 V	-0.038 V	-0.063 V
20 A	-0.026 V	-0.051 V	-0.076 V
30 A	-0.039 V	-0.064 V	-0.089 V
40 A	-0.052 V	-0.077 V	-0.102 V
50 A	-0.065 V	-0.090 V	-0.115 V
60 A	-0.078 V	-0.103 V	-0.128 V
70 A	-0.091 V	-0.116 V	-0.141 V
78 A	-0.101 V	-0.126 V	-0.151 V

**Figure 2. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_B Presented As a Deviation from VID.
Socket Loadline = 1.30 mΩ, VR Tolerance Band = ±25 mV.**

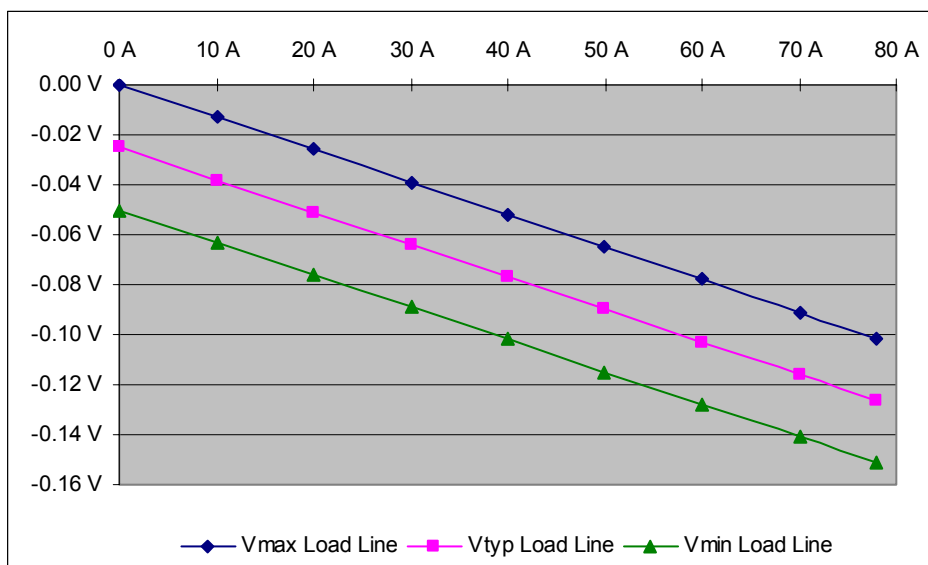




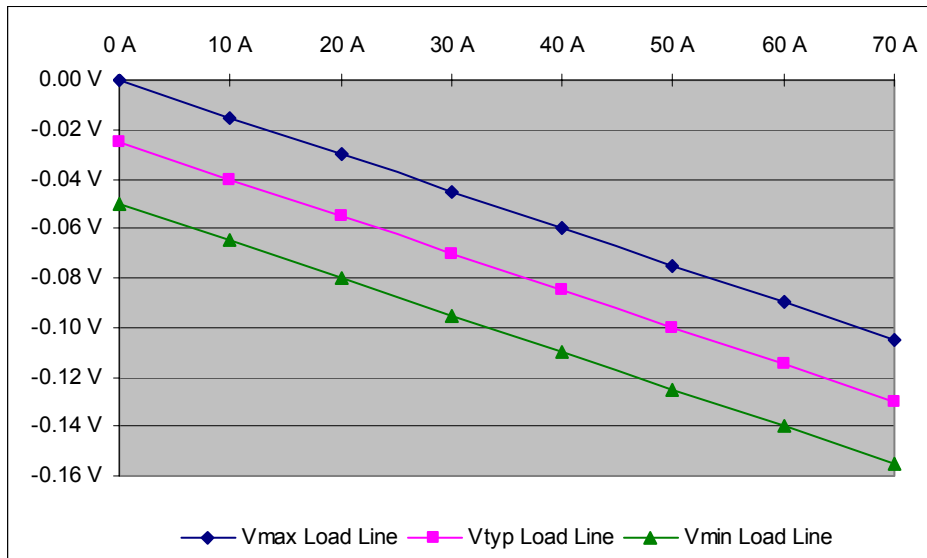
Table 8. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_C Presented As a Deviation from VID.

Socket Loadline = 1.50 mΩ, VR Tolerance Band = ±25 mV.

I _{cc}	Maximum	Typical	Minimum
0 A	0.000 V	-0.025 V	-0.050 V
10 A	-0.015 V	-0.040 V	-0.065 V
20 A	-0.030 V	-0.055 V	-0.080 V
30 A	-0.045 V	-0.070 V	-0.095 V
40 A	-0.060 V	-0.085 V	-0.110 V
50 A	-0.075 V	-0.100 V	-0.125 V
60 A	-0.090 V	-0.115 V	-0.140 V
70 A	-0.105 V	-0.130 V	-0.155 V

Figure 3. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_C Presented As a Deviation from VID.

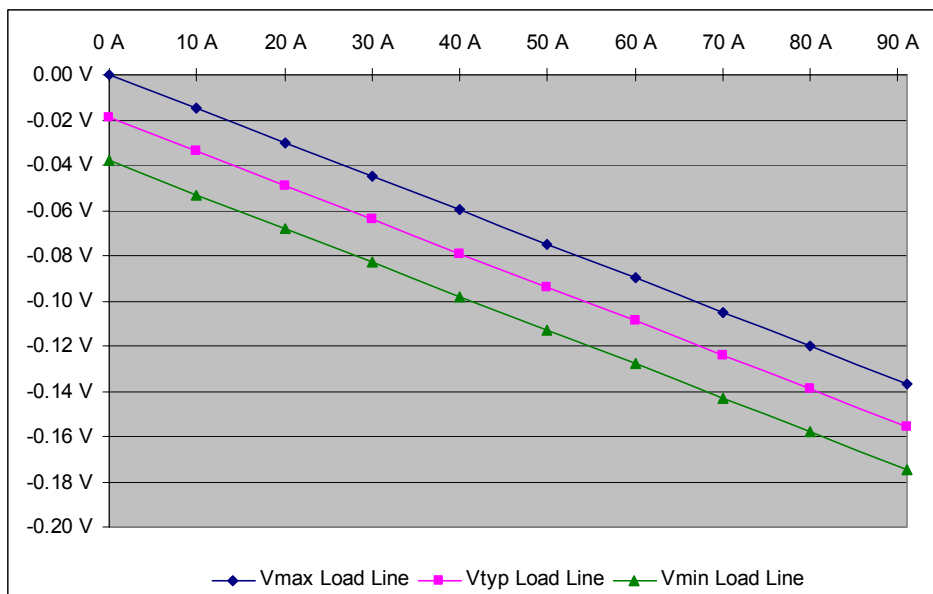
Socket Loadline = 1.50 mΩ, VR Tolerance Band = ±25 mV.



**Table 9. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_D Presented As a Deviation From VID.
Socket Loadline = 1.50 mΩ, VR Tolerance Band = ±19 mV.**

I _{cc}	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
10 A	-0.015 V	-0.034 V	-0.053 V
20 A	-0.030 V	-0.049 V	-0.068 V
30 A	-0.045 V	-0.064 V	-0.083 V
40 A	-0.060 V	-0.079 V	-0.098 V
50 A	-0.075 V	-0.094 V	-0.113 V
60 A	-0.090 V	-0.109 V	-0.128 V
70 A	-0.105 V	-0.124 V	-0.143 V
80 A	-0.120 V	-0.139 V	-0.158 V
91 A	-0.137 V	-0.156 V	-0.175 V

**Figure 4. Socket 478 Loadline Window for Design Configuration 478_VR_CONFIG_D Presented As a Deviation From VID.
Socket Loadline = 1.50 mΩ, VR Tolerance Band = ±19 mV.**



To properly calibrate the socket loadline parameter, the VR designer must excite the processor socket with a current step that generates a voltage droop which must be checked against the loadline window requirements. The table below identifies the steady state and transient current values to use for this calibration. For additional information, please consult the Loadline Calculator for the appropriate Intel processor.

Table 10. Intel® Processor Current Step Values for Transient Loadline Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
478_VR_CONFIG_A	21 A	91 A	70 A
478_VR_CONFIG_B	23 A	78 A	55 A
478_VR_CONFIG_C	20 A	70 A	50 A
478_VR_CONFIG_D	21 A	91 A	70 A

VRD designs must be loadline compliant across the full tolerance band window to avoid data corruption, system lock-up, and reduced performance. When validating a system's loadline, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical loadline may fit in the specification window, however designs residing elsewhere in the tolerance band distribution may violate the specifications. For example, Figure 5 Example A shows a loadline that is contained in the specification window and, in this single instance, complies with V_{ccmin} and V_{ccmax} specifications. The positioning of this loadline will shift up and down as the tolerance drifts from typical to the design limits. Figure 5 Example B shows that V_{ccmax} limits will be violated as the component tolerances shift the loadline to the upper tolerance band limits. Figure 5 Example C shows that the V_{ccmin} limits will be violated as the component tolerances shift the loadline to the lower tolerance band limits.

To satisfy specifications across high volume manufacturing variation, a typical loadline must be centered in the loadline window and have a slope equal to the value specified in Table 4. Figure 6 Example A shows a loadline that meets this condition. Under full 3-sigma tolerance band variation, the loadline slope will intercept the V_{ccmax} loadline (Figure 6 Example B) or V_{ccmin} loadline (Figure 6 Example C) limits.

Figure 5. Examples of High Volume Manufacturing Loadline Violations

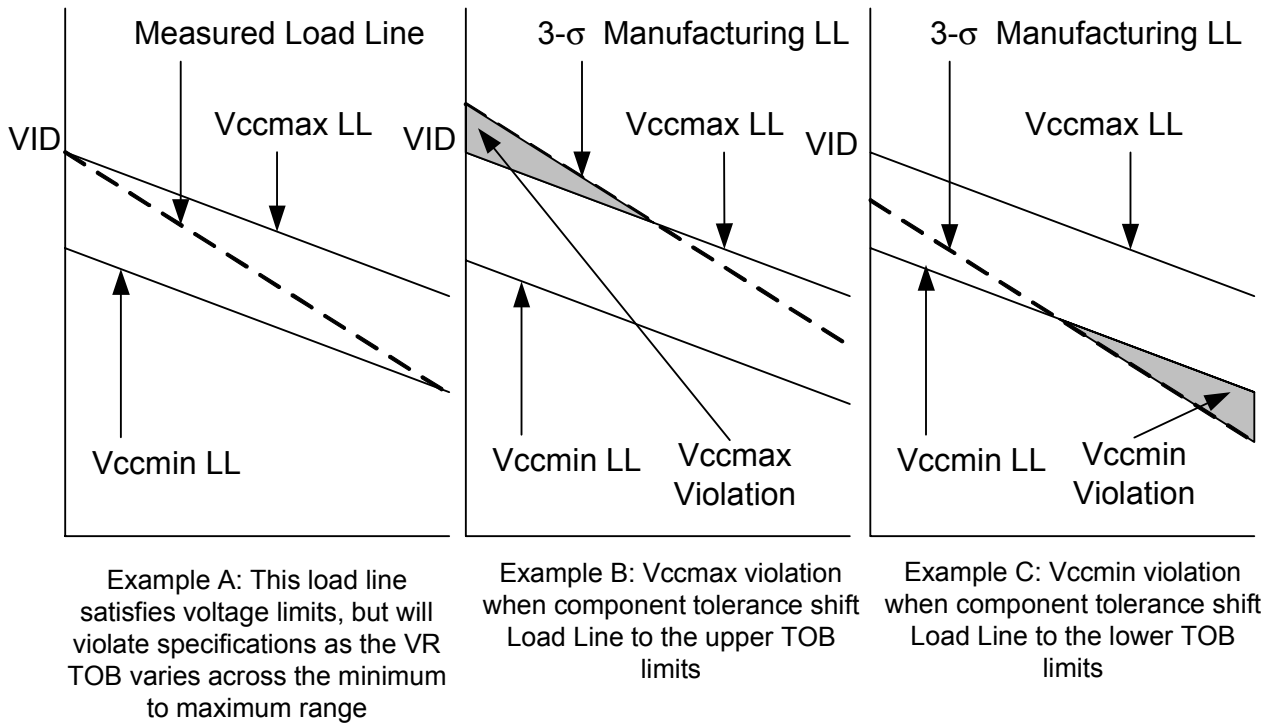
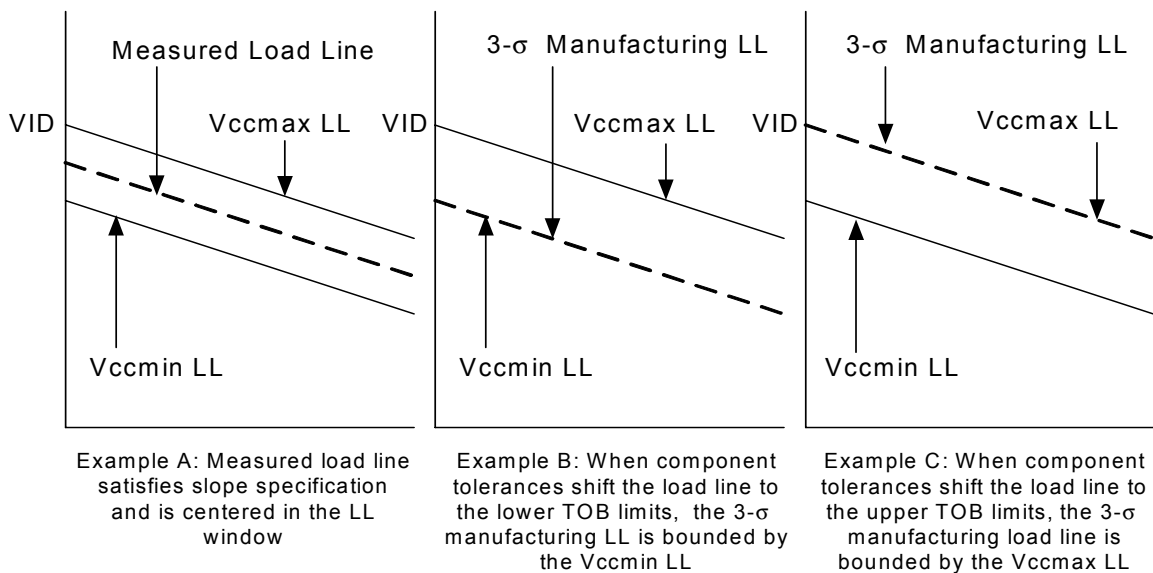


Figure 6. High Volume Manufacturing Compliant Loadline



2.3 TOB: Voltage Tolerance Band (REQUIRED)

Processor loadline specifications must be guaranteed across component process variation, system temperature extremes, and age degradation limits. The VRD topology and component selection must maintain a 3-sigma tolerance of The VRD Tolerance Band around the typical loadline (see Section 2.2). The critical parameters include voltage ripple, VRD controller tolerance, and current sense tolerance. Individual tolerance components will vary among designs; the processor requires only that the total error stack-up stay within the defined VR configuration tolerance band under the conditions defined in Table 4.

2.3.1 Sources of Voltage Deviation and Input Parameters

The standard VRD tolerance band (TOB) can be sliced into three main categories: controller tolerance, current sense variation, and voltage ripple.

Controller tolerance is determined by the DAC accuracy (digital to analog conversion) and DC offset of the internal controller circuitry (i.e., op amp offset). These tolerance parameters are functions of the operating voltage associated with the programmed VID (defined in Table 4). Internal controller circuitry also includes a tolerance associated with current sense signal conversion that must be included in the TOB calculation. Consult the controller data sheet or vendor for the particular component specifications.

VRD current sensing occurs by processing a sensed voltage across a component in the direct output current path. Current conversion occurs with knowledge of the device resistance and/or impedance. The tolerance of this sense method is directly aligned with the sense element's tolerance. For inductor, resistor, and FET sensing, the series resistance tolerance of the sense component is a critical factor for calculating the TOB. Integrating capacitors are part of the inductor current sense circuit and the manufacturing tolerance including thermal drift must be identified to ensure correct TOB calculations. For inductor and FET sensing, thermal compensation (see Section 2.4) is required to maintain a linear loadline across the full, operational system temperature range.

Peak ripple should not exceed ± 5 mV at the VRD measurement nodes. Ripple is typically suppressed by increasing the value of the output inductance or by increasing the value/quantity of ceramic capacitors in the high frequency filter (see Section 2.10).

Table 11. Input Parameters for VRD TOB Calculation

Parameter	Definition	Units
I_{dyn}	Defined current step amplitude ¹	A
I_{max}	Maximum load current ¹	A
k_C	Tolerance of CS capacitance ^{2 3}	[±% @ 3-σ]
k_{ESR}	Tolerance of inductor ESR ^{4 6}	[±% @ 3-σ]
k_{gm}	Controller tolerance of current signal conversion	[±% @ 3-σ]
k_L	Tolerance of output inductance ⁴	[±% @ 3-σ]
k_{RDS}	Tolerance of FET RDS-ON ⁴	[±% @ 3-σ]
k_{rsense}	Tolerance of sense resistor ⁴	[±% @ 3-σ]
k_{VID}	Controller reference voltage (VID) tolerance	[±% @ 3-σ]
n_{ph}	Number of independent phases in VRD	-
n_{rsense}	Number of sense resistors	-
R_{AVP}	AVP (Socket Loadline) resistance	[Ω]
V_{ripple}	Peak ripple voltage: Max = 5 mV peak	[±V]
V_{TC}	Thermal compensation transient error	[±V]

NOTES:

1. See Table 4
2. Statistical root-sum-square may be applied if more than one component is used
3. Tolerance is to include parameter thermal drift across operational temperature
4. Thermal variation of parameter is included in V_{TC} if thermal compensation is applied
5. All parameter tolerances are defined at 3-sigma. Many vendors define some common parameters, such as inductor tolerance and inductor ESR, at 6-sigma. These numbers should be translated to 3-sigma to obtain an accurate TOB calculation.
6. Vendors commonly refer to this parameter as RDC and it is generally a 6-sigma tolerance value. Quite often RDC is not, or is loosely, specified and engineering evaluation of the specific inductor manufacturing variables is needed to determine a reasonable RDC variation.

2.3.2 TOB: Tolerance Band Calculation

Reference TOB equations for each major current sense topology are provided in the next three subsections. Equations are presented in a manner for simple entry into a spreadsheet to simplify TOB calculation and design iterations. Contact your chosen PWM controller vendor for exact formulas.

2.3.2.1 Inductor RDC Current Sense TOB Calculations

Inductor sensing is the best general approach to satisfying the tolerance band requirements. TOB can be directly controlled by selecting output inductors and integrating capacitors of sufficient tolerance. Inductor thermal drift will require thermal compensation to keep the loadline linear (see Section 2.4). Capacitor thermal drift must also be considered in the tolerance and Intel recommends COG capacitors for their thermal stability. Understanding component variation is critical for calculating Inductor Sense TOB; many component tolerances are defined under 6-sigma variation, which should be translated to 3-sigma for calculation purposes.

$$TOB_{manuf} = \sqrt{(VID \cdot k_{VID})^2 + V_{AVP}^2 \cdot \left(k_{gm}^2 + \frac{k_{ESR}^2}{n_{ph}}\right) + V_{AVPdyn}^2 \cdot \left(\frac{k_L^2 + k_C^2}{n_{ph}}\right)}$$

$$V_{AVPdyn} = I_{dyn} \cdot R_{AVP}$$

$$V_{AVP} = I_{max} \cdot R_{AVP}$$

$$TOB = TOB_{manuf} + V_{ripple} + V_{TC}$$

2.3.2.2 Resistor Current Sense TOB Calculations

Resistor sensing topologies have the capability to provide the tightest TOB solutions due to a wide industry selection of precision resistors. However, the accuracy comes at a price. Resistors are placed in series with the output current, which results in substantial power loss and heat generation. The resulting power dissipation requires large, expensive, high wattage resistors, which demand additional cooling to keep components and motherboard layers below maximum allowable temperature limits. Power loss may be mitigated by selecting a low value of resistance, however minimum signal amplitude must be considered for adequate current conversion (i.e., signal to noise ratio).

$$TOB_{manuf} = \sqrt{(VID \cdot k_{VID})^2 + V_{AVP}^2 \cdot \left(k_{gm}^2 + \frac{k_{rsense}^2}{n_{rsense}}\right)}$$

$$V_{AVP} = I_{max} \cdot R_{AVP}$$

$$TOB = TOB_{manuf} + V_{ripple}$$

2.3.2.3 FET RDS-ON Current Sense TOB Calculations

Current can be determined by sensing the voltage across the VRD switching FET's drain to source 'on' resistance. While this provides a direct method of voltage to current conversion, the standard FET RDS-ON tolerance of ~20% is not acceptable to satisfy tolerance band requirements. If RDS-ON sensing is to be applied, FET thermal compensation is required (see Section 2.4) together with a tight FET RDS-ON distribution (approximately 5% at 3-sigma). Since boards are generally built with FETs from similar manufacturing lots, process to process variation is not random and the RDS-ON parameter may not be reduced through statistical analysis.

$$TOB_{manuf} = \sqrt{(VID \cdot k_{VID})^2 + V_{AVP}^2 \cdot (k_{gm}^2 + k_{RDS}^2)}$$

$$V_{AVP} = I_{max} \cdot R_{AVP}$$

$$TOB = TOB_{manuf} + V_{ripple} + V_{TC}$$

2.4 VRD Thermal Compensation (REQUIRED)

Intel processors in Socket 478 can draw significant levels of current, resulting in a varying temperature gradient across electrical components. Electrical parameters of these components are functions of temperature and their values will drift with the thermal gradient. This drift will result in a loadline violation if not minimized. To ensure compliance to specifications, the voltage regulator requires thermal compensation.

Thermal compensation allows the processor Vcc voltage regulator to respond to temperature drift in VRD electrical parameters. It is required to ensure that regulators using inductor or FET RDS-ON current sensing maintain a stable voltage over the full range of load current and system temperatures.

If thermal compensation is not included, the output voltage of the regulator will droop as the resistance of the sense element increases with temperature. With the increased resistance, the regulator falsely detects an increase in load current and regulates to a lower voltage. Thermal compensation prevents this thermally induced voltage droop by adjusting the feedback path based on the temperature of the regulator. This is accomplished by placing a thermistor in the feedback network (tuned with a proper resistor configuration) to negate the effects of the increased resistance of the sense element.

The thermal compensation circuit is to be validated by running the regulator at VR TDC for 30 to 45 minutes. This is to ensure the board is thermally saturated and system temperatures have reached a maximum steady state condition. If the thermal compensation has been properly implemented, the output voltage will only drift 1-2 mV from its coolest temperature condition. If the thermal compensation has not been properly implemented, voltage error can be measured in the 10's of millivolts. Care must be taken to avoid over-temperature conditions during this validation exercise. Sustained current draw above VR TDC can easily result in component failure and/or board damage.

2.5 Processor Electrical and Thermal Current Support (EXPECTED)

System boards supporting Intel processors in Socket 478 must have voltage regulator designs compliant to applicable processor's electrical and electrical-thermal standards. This includes full electrical support of I_{cmax} specifications and robust cooling solutions to support the VRD thermal design current (VR TDC) indefinitely within the envelope of system operating conditions (see Table 4).

Processor VR TDC is the sustained (DC equivalent) current parameter that is to be used for voltage regulator thermal design with supporting Thermal Monitor circuitry (see Section 6.2). At TDC, switching FETs reach maximum temperature heating the motherboard layers, processor socket, and neighboring components to the pass/fail boundary of thermal limits. Actual component and board temperatures are established by the envelope of the system's operating conditions and component physical properties. This includes voltage regulator layout, processor fan selection, ambient temperature, chassis configuration, component selection, etc.

In some instances the processor's VRD will also power other motherboard components such as the chipset. Under these conditions, the VRD may supply current above the stated I_{cmax} and/or TDC limits; VR designers must budget this additional current support in final VRD designs while remaining compliant to electrical and thermal specifications.

2.6 Stability (EXPECTED)

The VRD must be unconditionally stable under all specified output voltage ranges and current transients. The VRD should operate in a no-load condition: i.e., with no processor installed. Normally the no-processor VID code will be x1111, disabling the VRD (Section 2.11).

2.7 Processor Power Sequencing (REQUIRED)

The VRD must correctly sequence power in accordance with Intel processor requirements. Figure 7 is a block diagram of the VRD connectivity with necessary signals and relevant power rails. Figure 8 provides the timing protocol for these signals and power rails in socket 478 platforms.

Figure 7. Power Sequence Block Diagram

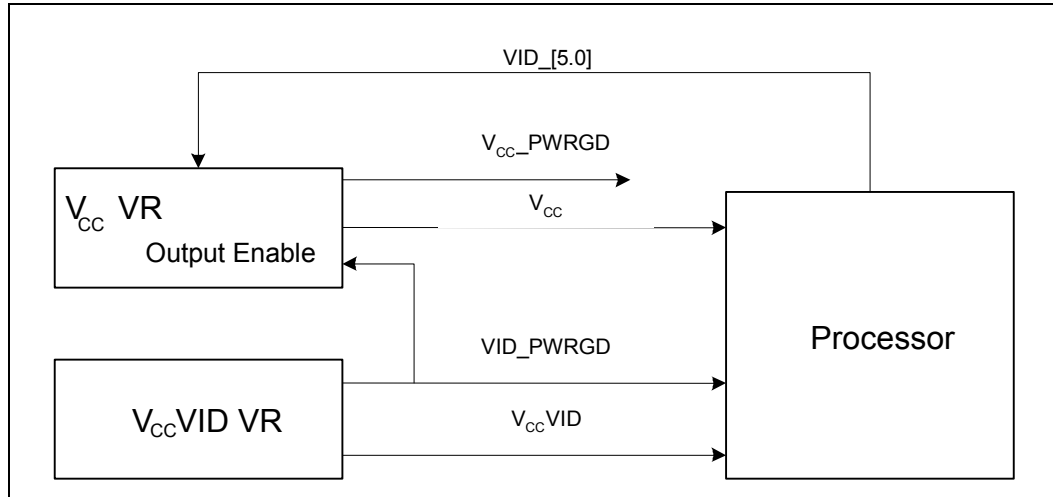
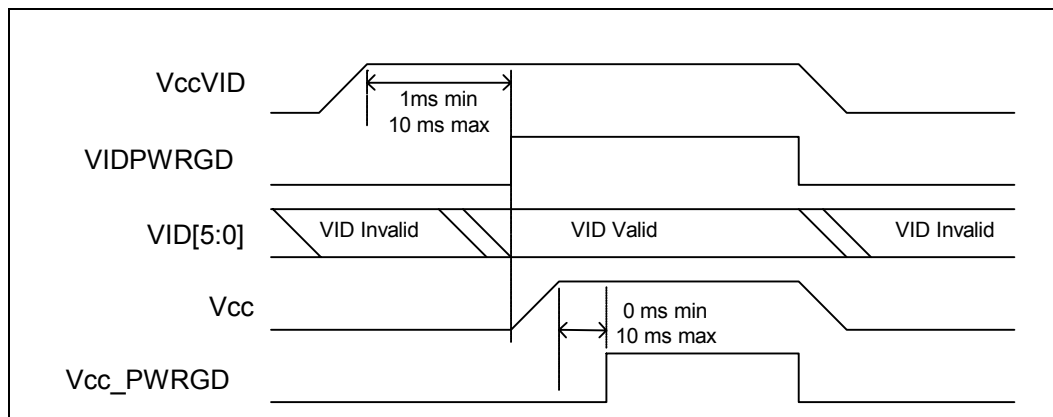


Figure 8. Power Sequence Timing Diagram



NOTES:

- V_{CC}VID comes up at the application of system power to the V_{CC}VID VR.
- V_{CC}VID VR generates VID_PWRGD, to latch the processor's VID outputs and enable V_{CC} VR after the V_{CC}VID supply is valid.
- V_{CC}_PWRGD is generated by the V_{CC} VR and may be used elsewhere in the system.

2.8 Dynamic Voltage Identification (REQUIRED)

2.8.1 Dynamic-Voltage Identification Functionality

VRD10 architecture includes the Dynamic Voltage Identification (D-VID) feature set, which enables the processor to reduce power consumption and processor temperature. Reference VID codes are dynamically updated by the processor to the VRD controller via the VID bus when a low power state is initiated. VID codes are updated sequentially in 12.5 mV steps and are transmitted every 5 microseconds until the final voltage code is encountered. Processors are capable of transitioning from standard operational VID levels to the minimum table entry of 0.8375V. They are also capable of returning to a higher VID code in a similar manner. The low voltage code will be held for a minimum of 50 microseconds prior to sequentially transitioning

through the VID table to a new voltage reference which can be any higher VID code, but is generally the original reference VID.

Figure 9 illustrates processor-operating states as the VID level is lowered. The diagram assumes steady state, maximum current during the transition for ease of illustration. In this figure, the processor begins in a high-load condition. Upon entering D-VID, the processor will shift to a low power state and stop executing code (sequence 1 => 2). After reaching state 2, the processor encounters a brief delay to prepare for low power operation then re-initiates code, resulting in current draw and a loadline IR drop to state 3. Sequencing from state 3 to 4 is a simplification of the multiple steps from the original VID loadline window to the low-voltage VID window. Transition from state 4 to state 5 is an example of a load change during normal operation in the low voltage VID setting. Transition from a low to high VID reference follows the reverse sequence

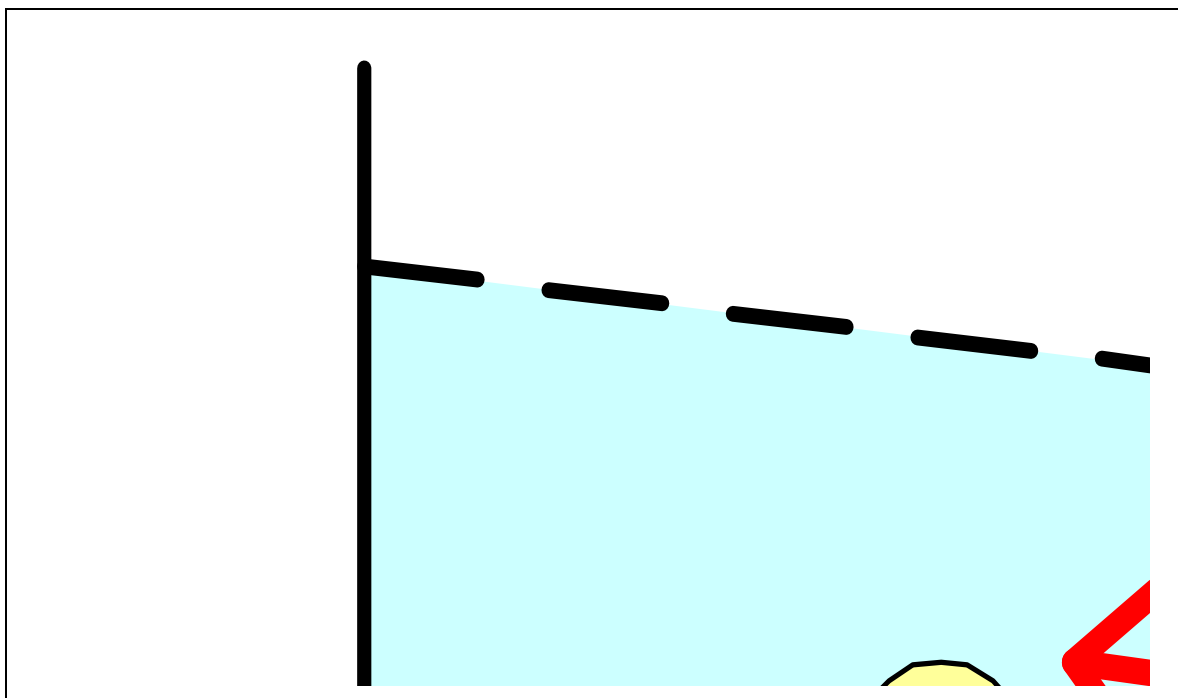
During a D-VID transition, Vcc must always reside above the minimum loadline of the current VID setting (see Figure 9). The loadline values of each VID increment are required to match the slope defined in Table 4. In addition, the voltage tolerance band and ripple specifications defined in Table 4 Section 2.3 must be satisfied in this state. To expedite power reduction and processor cooling, the VRD must lower the maximum Vcc value to reside within the low voltage VID window within 50 microseconds of the final VID code transmission (see Figure 9 and Figure 10). The VRD must respond to a transition from VID-low to VID-high by regulating the Vcc output to the range defined by the new VID code within 50 microseconds of the final code transmission.

Note: The minimum VID is not constant among all processors; the value will vary with frequency and standard VID settings. This results in numerous possible D-VID states. A simple and direct D-VID validation method is defined at the end of this section.

During a D-VID event, the processor load may not be capable of absorbing output capacitor energy when the VID reference is lowered. As a result, reverse current may flow into the AC-DC regulator's input filter, potentially charging the input filter to a voltage above the over voltage value. Upon detection of this condition, the AC-DC regulator will react by shutting down the AC-DC regulator supply voltage. The VRD and AC-DC filter must be designed to ensure this condition does not occur. In addition, reverse current into the AC-DC regulator must not impair the operation of the VRD, the AC-DC supply, or any other part of the system.

Under all functional conditions, including D-VID, the Vcc supply must satisfy loadline and overshoot constraints to avoid data corruption, system lock-up events, or system blue-screen failures.

Figure 9. Processor D-VID Loadline Transition States



2.8.2 D-VID Validation

Intel processors are capable of generating numerous D-VID states and the VRD must be designed to properly transition to and function at each possible code. However, exhaustive validation of each state is unnecessary and impractical. Validation can be simplified by verifying the VRD conforms to loadline requirements, tolerance band specifications, and D-VID timing requirements. Then, by default, each processor D-VID state will be valid. The key variables for V_{cc} under D-VID conditions are processor loading, starting VID, ending VID, and V_{cc} slew rate. The V_{cc} slew rate is defined by VRD bulk decoupling, the output inductors, the switching FET resistance, and the processor load. This indicates that the V_{cc} slewing will have an exponential behavior, where the response to code 'n+1' takes longer to settle than code 'n'. As a result, a test from maximum to minimum and from minimum to maximum will be sufficient to guarantee slew rate requirements and VID code regulation.

To ensure support for any valid VID reference, testing should be performed from the maximum table entry of 1.6 V to the minimum value of 0.8375 V. The VRD must ensure that this 0.7625 V transition occurs within 50 microseconds of the final VID code, in 350 microseconds. Slew rate timing is referenced from 0.4 V on the rising edge of the initial VID code to the time the final voltage is settled within 5 mV of the final V_{cc} value. Intel testing has noted a 10% change to the V_{cc} slew rate between VRD no load (5 A) and full load (VR TDC) conditions. For this reason, the V_{cc} slewing must be tested under both loading conditions.

During the D-VID test defined in the previous paragraph, V_{cc} droop and undershoot amplitudes must be limited to avoid processor damage and performance failures. If the processor experiences an undershoot due to D-VID transitions, an application initiated di/dt droop can superimpose with this event and potentially violate minimum voltage specifications. Droop during this D-VID test must be limited to 5 mV. This value was derived by calculating VRD tolerance band improvements at the low D-VID current and voltage values. If the processor experiences an overshoot due to D-VID transitions, an application initiated di/dt overshoot can superimpose with this event and potentially violate overshoot specifications. Overshoot is permitted, but must be properly budgeted with respect to the specifications defined in Section 2.9. Superposition of the dynamic VID overshoot event and the overshoot resulting from the transient test defined in Section 2.9, must not exceed the amplitude and time requirements defined in the overshoot specification.

2.8.3 Validation Summary

Consult Figure 10 and Figure 11 for graphic representation of validation requirements.

1. Constraints:

- a: 762.5 mV \pm 5 mV transition must occur within 350 μ s (see Figure 10)
- b. Start time is referenced to 0.4 V on the rising edge of the initial D-VID code
- c. End time is referenced to the steady state V_{cc} voltage after the final D-VID code
- d. Undershoot during maximum to minimum VID transition must be limited to 5 mV. This 5 mV is included within the \pm 5 mV tolerance on the final VID value defined under test condition a.
- e. Overshoot observed when transitioning from minimum to maximum VID must conform to overshoot specifications. Specifically, superposition of the dynamic VID overshoot event and the overshoot resulting from the transient test defined in section 2.9 must not exceed the overshoot amplitude and time requirements defined in the overshoot specification.
- f. Care must be taken to avoid motherboard and component heat damage resulting from extended operations with high current draw.

2. Validation exercises:

- a. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.8375 V with an applied 5 A Load.
- b. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.8375 V with an applied VR TDC Load.
- c. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied 5 A Load.
- d. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied VR TDC Load.

Figure 10. D-VID Transition Timing States

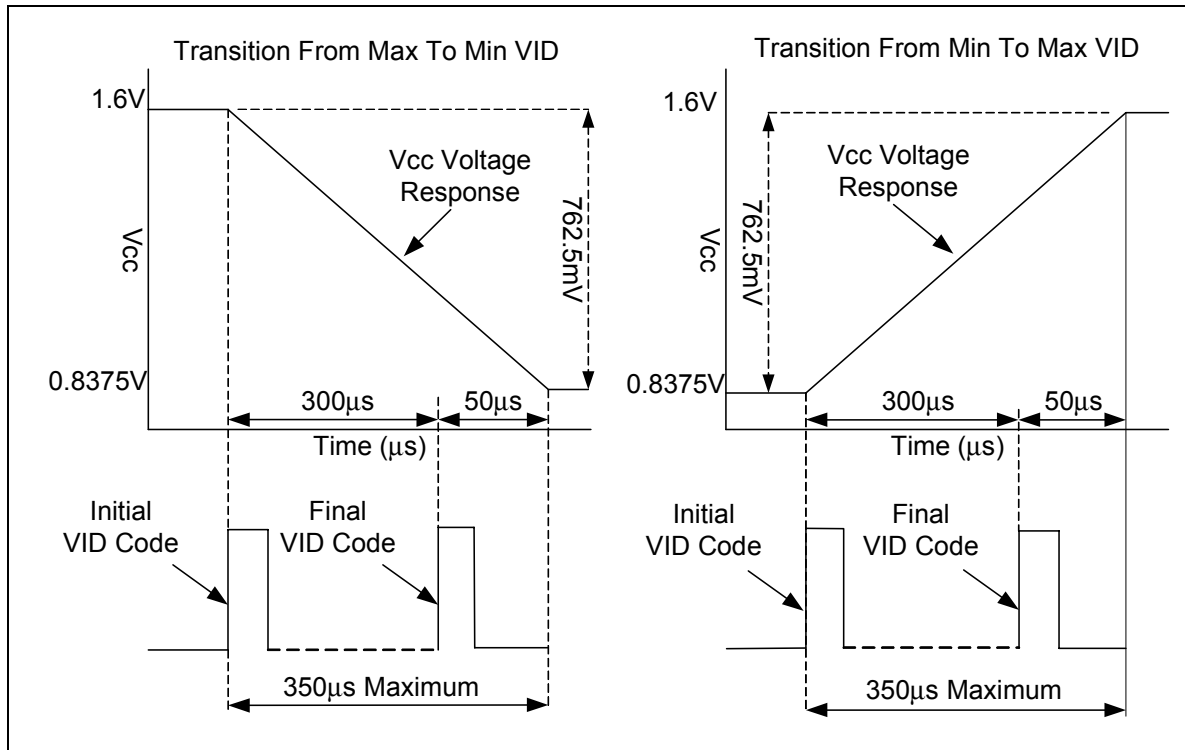


Figure 11. Overshoot and Undershoot During Dynamic VID Validation

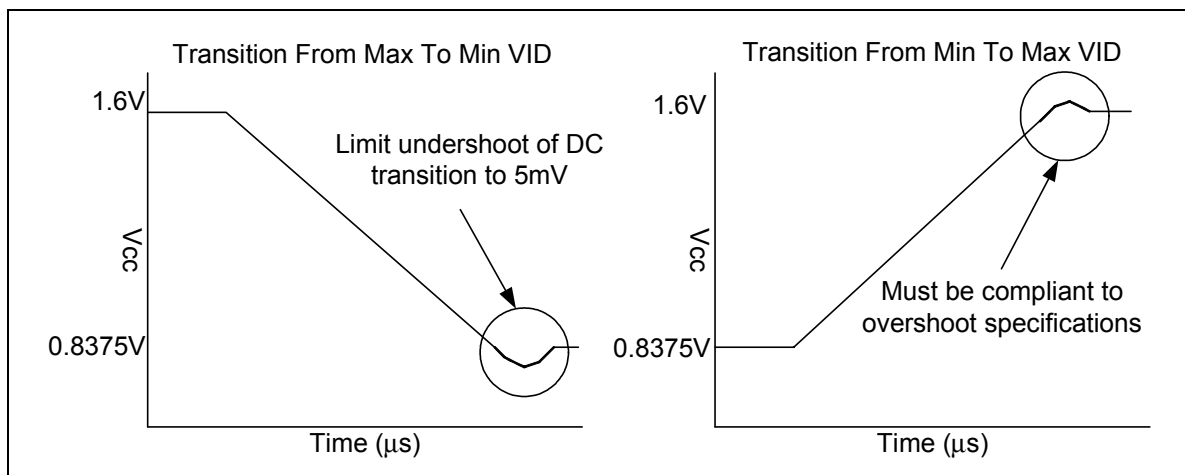




Table 12. D-VID Validation Summary Table

Parameter	Minimum	Typical	Maximum
VID	0.8375 V	-	1.6000 V
Voltage Transition	0.7575 V	0.7625 V	0.7675 V
Transition Time	-	-	350µs ¹
Current Load	5A	-	VR TDC ²

NOTES:

1. Time is measured from 0.4V on rising edge of the first D-VID code to the convergent Vcc voltage value after the final D-VID code is transmitted.
2. Consult Table 4 for definition of VR TDC

2.9 Processor Vcc Overshoot (REQUIRED)

2.9.1 Specification Overview

Intel desktop processors in socket 478 are capable of tolerating short transient overshoot events above VID on the Vcc supply that will not impact processor lifespan or reliability. Maximum processor Vcc overshoot, VOS, cannot exceed VID+VOS_MAX. Overshoot duration, TOS, cannot stay above VID for a time more than TOS_MAX. See Table 13 and Table 14 for details.

Table 13. Vcc Overshoot Terminology

Parameter	Definition
VOS	Measured peak overshoot voltage
VOS_MAX	Maximum specified overshoot voltage allowed above VID
TOS	Measured overshoot time duration
TOS_MAX	Maximum specified overshoot time duration above VID
Vzc	Zero current voltage: The voltage where the measured loadline intercepts the voltage axis
Vzco	$Vzco = VID - Vzc.$

Table 14. Vcc Overshoot Specifications

Parameter	Specification
VOS_MAX	50 mV
TOS_MAX	25 µs
VOS	Maximum = VID + VOS_MAX
TOS	Maximum = TOS_MAX

Maximum overshoot in socket 478 is validated by monitoring the voltage across the recommended test pins (defined in Section 2.2) while applying a current load release across the socket Vcc and Vss pin field. Amperage values for performing this validation under each VRD design configuration are identified in Table 15. The platform voltage regulator output filter must be stuffed with a sufficient quality and number of capacitors to ensure that overshoot stays above VID for a time no longer than TOS_MAX and never exceeds the maximum amplitude of VID+VOS_MAX. Measurements are to be taken using an oscilloscope with a 20 MHz bandwidth. Boards in violation must be redesigned for compliance to avoid processor damage.

Table 15. Intel® Processor Current Release Values for Overshoot Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
478_VR_CONFIG_A	75 A	5 A	70 A
478_VR_CONFIG_B	60 A	5 A	55 A
478_VR_CONFIG_C	55 A	5 A	50 A
478_VR_CONFIG_D	75 A	5 A	70 A

To prevent processor damage, VRD designs should comply to overshoot specifications across the full loadline tolerance band window (see Section 2.2). When validating a system’s overshoot, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical design may fit in the loadline window; however designs residing elsewhere in the tolerance band distribution may violate the Vcc overshoot specifications. Figure 13 provides an illustration of this concept. A typical board will have the Vcc zero current voltage (Vzc) centered in the loadline window at VID-TOB; for this example, assume TOB is 20 mV (waveform A). Now assume that the VRD has maximum overshoot amplitude of VOS_MAX = 50 mV above VID. Under this single case, the overshoot aligns with the specification limit and there is zero margin to violation. Under manufacturing variation Vzc can drift to align with VID (waveform B). This drift will shift the overshoot waveform by the same voltage level. Since this example has zero overshoot amplitude margin, this increase in Vzc due to manufacturing drift will yield a 20 mV overshoot violation which will reduce the processor life span. To address this issue in validation, a voltage margining technique can be employed to ensure overshoot amplitudes stay below a safe value. This technique translates the specification baseline from VID to a VRD validation baseline of Vzc + VOS_MAX, which defines a test limit for specification compliance across the full TOB range:

Equation 1: Overshoot Voltage Limit

$$VOS < Vzc + VOS_MAX$$

This equation is to be used during validation to ensure overshoot is in compliance to specifications across high volume manufacturing variation. In addition, the overshoot duration must be reference to Vzc and cannot exceed this level by more than 25 μs.

Figure 12. Graphical Representation of Overshoot Parameters

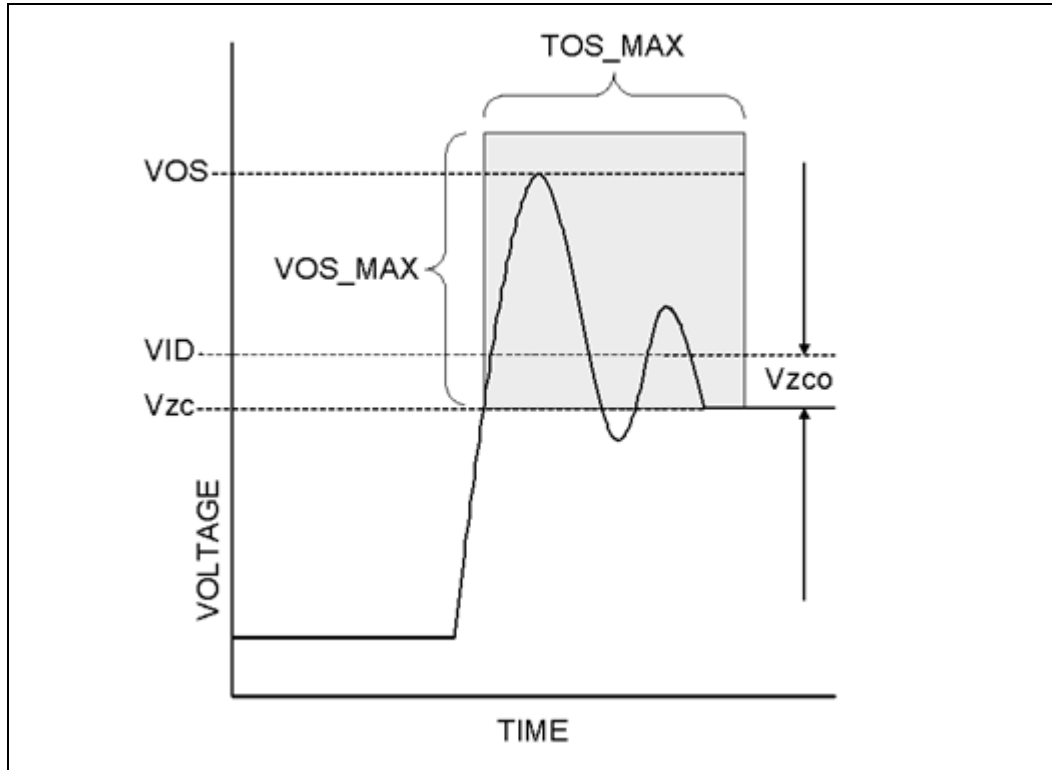


Figure 13. Processor Overshoot in High Volume Manufacturing

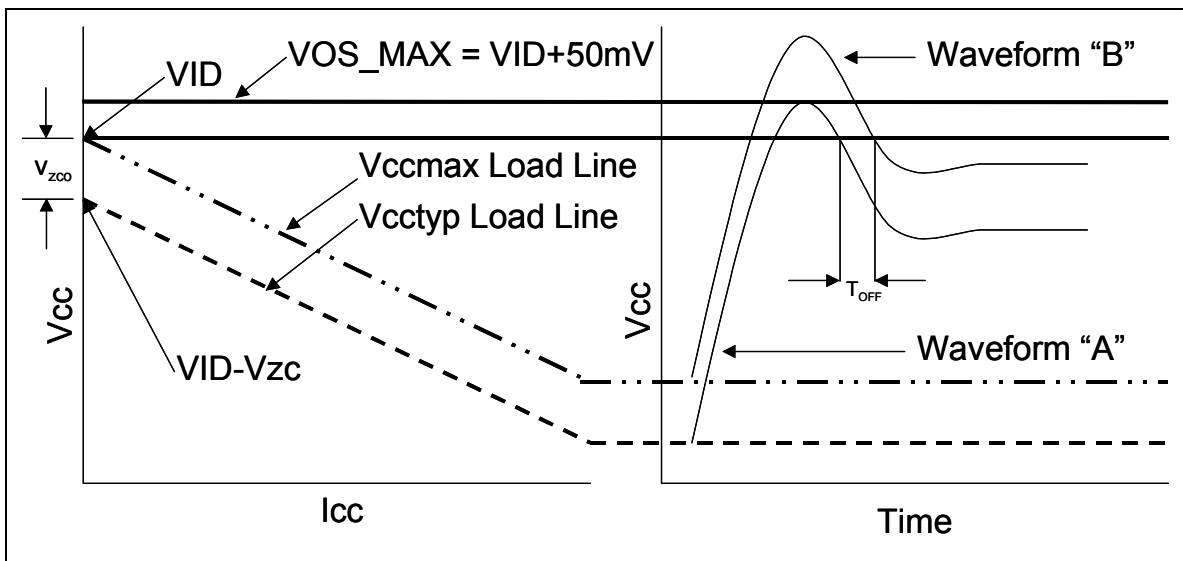
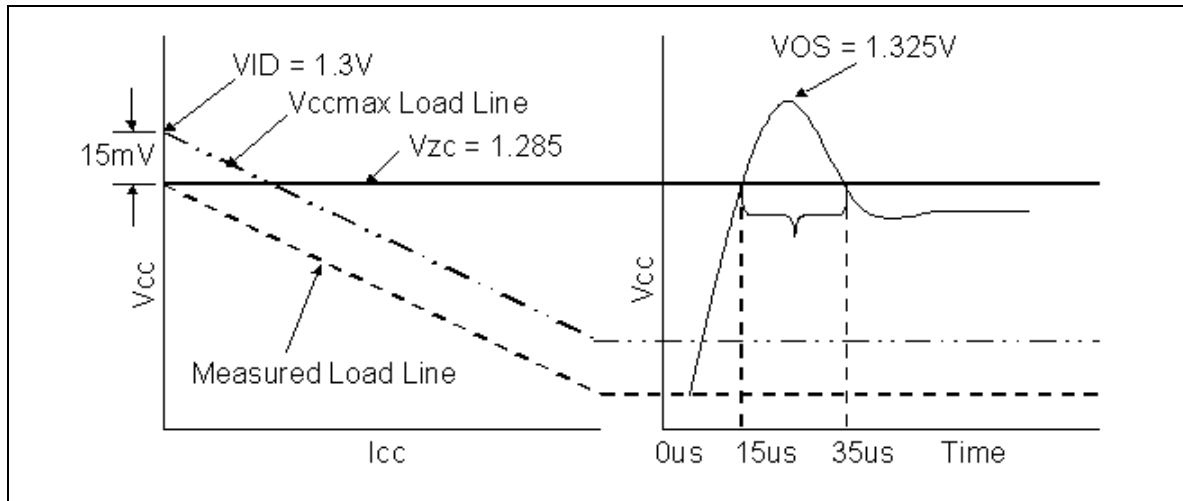


Figure 14. Example Socket Vcc Overshoot Waveform





2.9.2 Example: Socket Vcc Overshoot Test

To pass the overshoot specification, the amplitude constraint of Equation 1 and time duration requirement of TOS_MAX must be satisfied. This example references Figure 14.

Amplitude Test Constraint: Overshoot amplitude, VOS, must be less than $V_{zc} + VOS_MAX$

Input parameters

VOS = 1.325 V – Obtained from direct measurement

V_{zc} = 1.285 V – Obtained from direct measurement

VOS_Max = 0.050 V – An Intel specified value

Amplitude Analysis:

$V_{zc} + VOS_MAX = 1.285 \text{ V} + 0.050 \text{ V} = 1.335 \text{ V}$

VOS = 1.325 < 1.335 V

Amplitude Test Satisfied

Time Duration Test Constraint: Overshoot duration above V_{zc} must be less than 25 μs

Input Parameters

Initial crossing of overshoot: 15 μs – Obtained from direct measurement

Final crossing of overshoot: 35 μs – Obtained from direct measurement

TOS_MAX = 25 μs – An Intel specified value

Overshoot Duration Analysis

TOS = Final Crossing of V_{zc} – Initial Crossing of V_{zc}

TOS = 35 μs – 15 μs = 20 μs < 25 μs = TOS_MAX

Time duration test passed

Amplitude Test Passed & Time Duration Test Passed => Overshoot specification is satisfied

2.10 Desktop VR Output Filter (REQUIRED)

Processor voltage regulators include an output filter to minimize transient noise on the Vcc rail. Design analysis determined that the most cost efficient filter solution, for satisfying loadline requirements, incorporates 680 μF aluminum-poly capacitors with 5 $\text{m}\Omega$ average ESR. High frequency noise and ripple suppression is best minimized by 22 μF and/or 10 μF multi-layer ceramic capacitors (MLCC's). It is recommended to maximize the MLCC count in the socket cavity to help suppress transients induced by microprocessor packaging hardware. Remaining MLCC's should be first placed adjacent to the socket edge in the region between the socket cavity and the voltage regulator. If additional MLCC's are needed to satisfy the loadline, they should be placed on the socket edge that is opposite the VR adjacent edge.

The Dynamic VID mode of operation is directly impacted by the choice of bulk capacitors in the output filter. It is recommended to minimize Vcc setting time during Dynamic VID operation to hasten the speed of core power and temperature reduction. The speed of recovery is directly related to the RC time constant of the output filter. To ensure adequate thermal recovery time, it is recommended to design the output filter with a minimal amount of bulk capacitance with minimum ESR, while providing a sufficient amount of decoupling to maintain loadline requirements. At this time, 680 μF aluminum poly capacitors with 5 $\text{m}\Omega$ average ESR have been identified as the preferred solution.

It is common for a motherboard to support processors that require different VRD configurations (see Table 4). In this case, the Vcc regulator design must meet the specifications of all processors supported by that board. This requires the VRD to adopt an output filter design that satisfies the lowest socket loadline value of all supported processors. For example, if a motherboard is to support processors requiring 478_VR_CONFIG_A with a 1.24 $\text{m}\Omega$ loadline slope and 478_VR_CONFIG_D requiring a 1.5 $\text{m}\Omega$ loadline slope, the VRD output filter must have a transient loadline value of 1.24 $\text{m}\Omega$ to satisfy the noise requirements of each processor.

Note: The VRD hardware must always be configured to each specific processor's static loadline. For the previous example, the VRD must recognize which processor is residing in the socket. If a 478_VR_CONFIG_A processor is detected, the static loadline must be set to 1.24 $\text{m}\Omega$. If a 478_VR_CONFIG_D processor is replaced with a 478_VR_CONFIG_A processor, the VRD hardware must detect the change and update the static loadline to 1.5 $\text{m}\Omega$.

2.11 Shutdown Response (REQUIRED)

The VRD is to turn off the Vcc supply within 500ms upon receiving a processor driven OFF VID code (see Table 18) or when the Output Enable signal is de-asserted (see section 3.1).



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3 Control Inputs

3.1 Output Enable (REQUIRED)

The VRD controller is to recognize the Output Enable signal to assert/disable Vcc regulation. When disabled, the VRD output is to function in a high-impedance state and not source current. Once the VRD is operating after power-up, it should respond to a de-asserted Output Enable by turning off Vcc within 500 ms. When Output Enable is pulled low during the shutdown process, the VRD should not exceed its previous voltage level regardless of the VID setting during the shutdown process.

Table 16. Output Enable Specifications

Design Parameter	Specification		
	Minimum	Maximum	Units
Pull-Up Voltage Range	0	VCC VID	Volts
Pull-Up Resistor ¹	1 k	2.6 k	Ohms
V _{IH}	0.8	-	Volts
V _{IL}	-	0.3	Volts

NOTES: 1. Range includes tolerances

3.2 Voltage Identification (VID [5:0]) (REQUIRED)

The VRD is to read a five or six bit code transmitted by the processor across the VID bus to set the reference Vcc value. A comprehensive list of all VID codes is provided in Table 18. VID buffer signaling requirements are provided in Table 17.

Table 17. VID Signal Specifications

Design Parameter	Specification		
	Minimum	Maximum	Units
Pull-Up Voltage Range	3.135	3.465	Volts
Pull-Up Resistor ¹	950	1050	Ohms
V _{IH} ²	0.8	-	Volts
V _{IL} ²	-	0.4	Volts
VID Buffer leakage current	100	200	Microamperes

NOTES:

1. Range includes tolerances. Pull-up resistors should not be integrated into the PWM controller (values may be adjusted on the system board for signal integrity).
2. Other platform components may use VID inputs and require tighter limits.
3. Table shown for reference.

Table 18. Voltage Identification (VID) Table

Processor Pins (0 = low, 1 = high)						Vout (V)	Processor Pins (0 = low, 1 = high)						Vout (V)
VID5	VID4	VID3	VID2	VID1	VID0		VID5	VID4	VID3	VID2	VID1	VID0	
0	0	1	0	1	0	0.8375	0	1	1	0	1	0	1.2125
1	0	1	0	0	1	0.8500	1	1	1	0	0	1	1.2250
0	0	1	0	0	1	0.8625	0	1	1	0	0	1	1.2375
1	0	1	0	0	0	0.8750	1	1	1	0	0	0	1.2500
0	0	1	0	0	0	0.8875	0	1	1	0	0	0	1.2625
1	0	0	1	1	1	0.9000	1	1	0	1	1	1	1.2750
0	0	0	1	1	1	0.9125	0	1	0	1	1	1	1.2875
1	0	0	1	1	0	0.9250	1	1	0	1	1	0	1.3000
0	0	0	1	1	0	0.9375	0	1	0	1	1	0	1.3125
1	0	0	1	0	1	0.9500	1	1	0	1	0	1	1.3250
0	0	0	1	0	1	0.9625	0	1	0	1	0	1	1.3375
1	0	0	1	0	0	0.9750	1	1	0	1	0	0	1.3500
0	0	0	1	0	0	0.9875	0	1	0	1	0	0	1.3625
1	0	0	0	1	1	1.0000	1	1	0	0	1	1	1.3750
0	0	0	0	1	1	1.0125	0	1	0	0	1	1	1.3875
1	0	0	0	1	0	1.0250	1	1	0	0	1	0	1.4000
0	0	0	0	1	0	1.0375	0	1	0	0	1	0	1.4125
1	0	0	0	0	1	1.0500	1	1	0	0	0	1	1.4250
0	0	0	0	0	1	1.0625	0	1	0	0	0	1	1.4375
1	0	0	0	0	0	1.0750	1	1	0	0	0	0	1.4500
0	0	0	0	0	0	1.0875	0	1	0	0	0	0	1.4625
1	1	1	1	1	1	OFF ¹	1	0	1	1	1	1	1.4750
0	1	1	1	1	1	OFF ¹	0	0	1	1	1	1	1.4875
1	1	1	1	1	0	1.1000	1	0	1	1	1	0	1.5000
0	1	1	1	1	0	1.1125	0	0	1	1	1	0	1.5125
1	1	1	1	0	1	1.1250	1	0	1	1	0	1	1.5250
0	1	1	1	0	1	1.1375	0	0	1	1	0	1	1.5375
1	1	1	1	0	0	1.1500	1	0	1	1	0	0	1.5500
0	1	1	1	0	0	1.1625	0	0	1	1	0	0	1.5625
1	1	1	0	1	1	1.1750	1	0	1	0	1	1	1.5750
0	1	1	0	1	1	1.1875	0	0	1	0	1	1	1.5875
1	1	1	0	1	0	1.2000	1	0	1	0	1	0	1.6000

NOTES:

The Vcc output is disabled upon communication of an OFF VID code. This is the same as de-asserting the output enable input (Section 3.1).

VID [4:0] are compatible with Intel desktop processors using five-bit VID codes.

VID [5:0] will be used on processors with six-bit codes.

3.3 Differential Remote Sense Input (REQUIRED)

The PWM controller must include differential sense inputs to compensate for an output voltage offset of ≤ 300 mV in the power distribution path. The remote sense lines should not draw more than 10 mA to minimize offset errors. Refer to Section 2.2 for measurement location.

4 *Input Voltage and Current*

4.1 **Input Voltages (EXPECTED)**

The main power source for the VRD is 12 V \pm 15%. This voltage is supplied by an AC DC power supply through a cable to the motherboard. For input voltages outside the normal operating range, the VRD should either operate properly or shut down.

4.2 **Load Transient Effects on Input Current (EXPECTED)**

The design of the VRD, which includes the input power delivery filter, must ensure that the maximum slew rate of the input current does not exceed 1 A/ μ s, as specified for the ATX12V, SFX12V, TFX12V (Thin Form Factor with 12-Volt Connector), CFX12V (Compact Form Factor with 12-Volt Connector) and LFX12V (Low profile Form Factor with 12-Volt Connector) power supplies.



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5 *Output Protection*

Output protection features are necessary to prevent damage to the VRD, the processor, and other system components.

5.1 **Over-Voltage Protection (OVP) (PROPOSED)**

An OVP circuit should monitor the output for an over-voltage condition. If the output is more than 200 mV above the maximum VID level, the VRD should shut off the Vcc supply to the processor.

5.2 **Over-Current Protection (OCP) (PROPOSED)**

The VRD should be capable of withstanding a continuous, abnormally low resistance on the output without overstressing the voltage regulator. Output current under this condition should be limited to avoid component damage and violation of the VRD thermal specifications (see Section 2.5).



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6 Output Indicators

6.1 Processor Power Good Output (Vcc_PWRGD) (PROPOSED)

The VRD must provide a power-good signal, which remains in the low state for a maximum of 10 milliseconds after the output voltage reaches the range specified in Section 2.2. The signal should then remain asserted when the VRD is operating, except for fault or shutdown conditions. Vcc_PWRGD must not be de-asserted due to the low voltage functionality of Dynamic Voltage Identification.

Table 19. Power Good Specifications

Design Parameter	Specification
Signal Type	Open-collector or equivalent
Voltage Range	5.5 V (maximum) in open state
Minimum I _{OL}	4 mA
Maximum V _{OL}	0.4 V

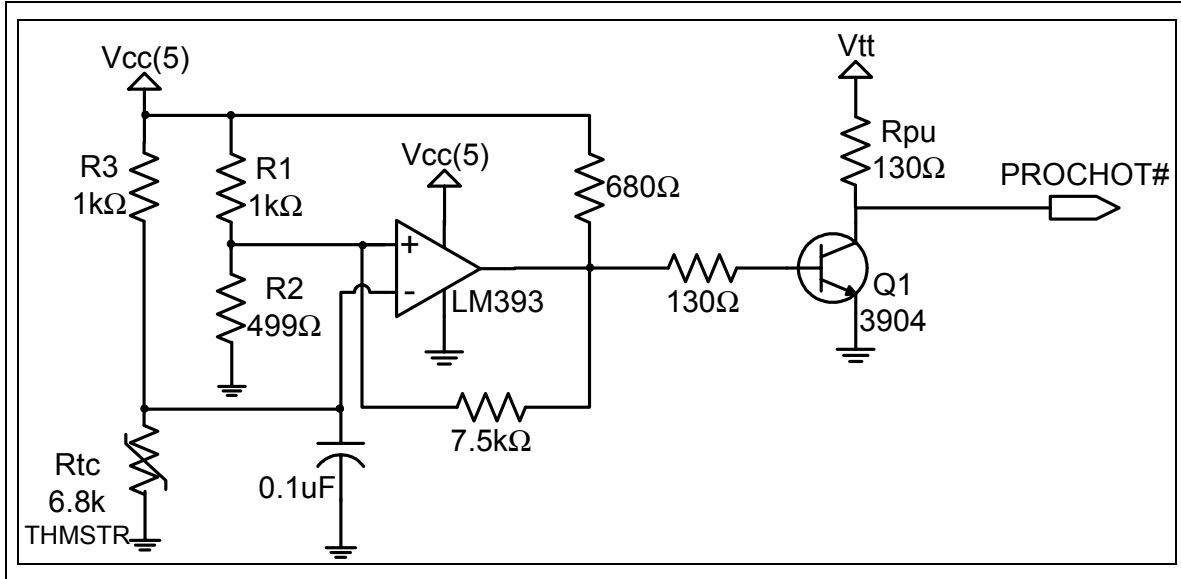
6.2 VRD Thermal Monitoring (PROPOSED)

This section describes a circuit to protect the voltage regulator design from heat damage while supporting thermal design current (VR TDC) specifications.

Each customer is responsible for identifying maximum temperature specifications for all components in the voltage regulator design and ensuring that these specifications are not violated while continuously drawing specified VR TDC levels. In the event of a catastrophic thermal failure, the thermal monitoring circuit is to assert the processor signal PROCHOT# immediately prior to exceeding maximum motherboard and component thermal ratings to prevent heat damage. Assertion of this signal will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Assertion of PROCHOT# degrades system performance and must never occur when drawing less than specified thermal design current.

VRD temperature violations can be detected using a thermal sensor and associated control circuitry (see Figure 15). For this implementation, a thermistor (THMSTR) is placed in the temperature sensitive region of the voltage regulator. The location must be chosen carefully and is to represent the position where initial thermal violations are known to occur. When the critical temperature is exceeded, the thermal monitor circuit is to initiate PROCHOT# to protect the voltage regulator from heat damage.

Figure 15: Example VRD Thermal Monitor Circuit Design



Note: Where $R_2 = R_1/R_3 * R_{tc}$. Thermister is NTHS0603N02N6801JR or equivalent. R_{tc} represents the thermister resistance at maximum allowable temperature.

Assertion of PROCHOT# is governed by the comparator (LM393) using the sensor voltage (at the negative comparator terminal) and a trigger reference voltage (at the positive comparator terminal). As the thermister temperature increases due to system loading, the resistance will decrease. When the voltage drop across the thermister falls below the trigger reference voltage, established by R1 and R2, the comparator will change state and bias the bipolar transistor (Q1). When biased, Q1 provides the active low signal assertion of PROCHOT# compliant to signaling specifications (see Table 20).

Table 20. Thermal Monitor Specifications

Parameter	Specification			Units
	Min	Typ	Max	
V_{TT} voltage	-	$(V_{TT})^1$	-	Volts
V_{CC}^1	4.75	5.00	5.25	Volts
Transistor Q1 output 'on' (low) resistance	-	-	11	Ohms
PROCHOT# leakage current	-	-	200	Microamperes
Transition time 20% to 80% signal rise for PROCHOT#	0.550	100	-	Nanoseconds
Minimum time in or out of Thermal Monitor state	1.0	-	-	Milliseconds
RPU (Pull-up Resistor) ²	-	130 Ω ± 5%	-	Ohms

NOTES:

1. Consult Vtt specifications for min and max limits.
2. The thermal monitor circuit is to use a single motherboard pull up resistor to bias the Q1 collector. This is provided in the PROCHOT# circuit design. Additional termination must not be integrated into the thermal monitoring circuit.

PROCHOT# is an open-drain, active-low i/o buffer terminated to the system V_{tt} (FSB termination voltage). To maintain reliable signaling between thermal monitor circuit, processor, and chipset, the bipolar transistor must be selected to operate with a collector bias established using a single, 130 Ω pull-up resistor. Use of additional termination or pull-up resistors may lead to signal integrity or logic threshold failures. The values for R1, R2 and R3 in Figure 15 are included as an example and must be calculated using specific design parameters. The value of R2 is adjusted to calibrate the comparator's trigger reference voltage (and assertion of PROCHOT#) against the sensor voltage representing a thermal violation.

6.3 Load Indicator Output (PROPOSED)

To assist VRD circuit debug and validation, the PWM controller supplier may choose to include an output voltage that is a defined function of the VRD output current.



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7 VccVID Voltage (PROPOSED)

The VccVID rail powers the processor VID buffers. This rail must power to regulation and assert an active-high VID_PWRGD output according to the timing specified in Figure 8 and Figure 16 under the signaling conditions defined in Table 21. There is no enable function for the VccVID regulator controller

Figure 16. VID PWRGD Timing

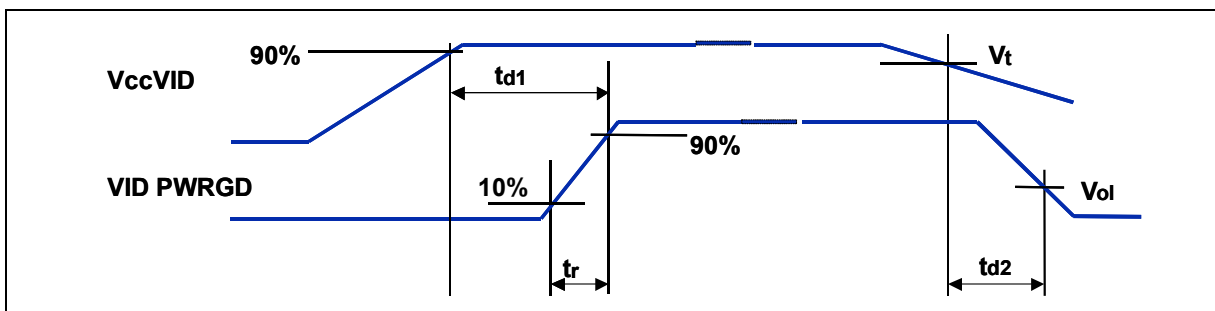


Table 21. VccVID Specifications

Parameter	Minimum	Maximum	Units
VccVID	1.14	1.26	Volts
VccVID current	150	-	Milliamperes
VID PWRGD voltage	1.14	1.32	Volts
VID PWRGD Voh	1	VccVID	Volts
VID PWRGD Vol	-0.2	0.2	Volts
VID PWRGD de-assertion threshold, Vt	80% VccVID	-	Volts
VID PWRGD leakage	-	50	Microamperes
Delay from VccVID to VID PWRGD, td1	1	10	Milliseconds
VID PWRGD rise time, tr	-	150	Nanoseconds
VID PWRGD de-assertion delay, td2	-	1	Milliseconds



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8 **Motherboard Power Plane Recommendations (EXPECTED)**

The motherboard layer stack-up should be designed to ensure robust, noise-free power delivery to the processor. Failure to minimize and balance power plane resistance may result in non-compliance to the die loadline specification. A poorly planned stack-up or excessive holes in the power planes may increase system inductance and generate oscillation on the rail at the processor. Both of these types of design errors can lead to processor failure and must be avoided by careful Vcc and Vss plane layout and stack-up. The types of noise introduced by these errors may not be immediately observed on the processor power pins or during system-board voltage transient validation, so issues must be resolved by design, prior to layout, to avoid unexpected failures.

Following basic layout rules can help avoid excessive power plane noise. All motherboard layers in the area surrounding the processor socket should be used for Vcc power delivery; copper shapes that encompass the power delivery region of the processor pin field are required. A careful motherboard design will help ensure a well-functioning system that minimizes the noise profile at the processor die. The following subsections provide further guidance.

8.1 **Minimize Power Path DC Resistance**

Power path resistance can be minimized by ensuring that the copper layout area is balanced between Vcc and Vss planes. A good four layer board design will have two Vcc layers and two Vss layers. Because there is generally more Vss copper in the motherboard stack-up, care should be taken to maximize the copper in Vcc floods. This includes care to minimize unnecessary plane splits and holes when locating through hole components, vias, and connection pads.

8.2 **Minimize Power Delivery Inductance**

At higher frequencies the ordering of the motherboard layers becomes critical as it is Vcc/Vss plane pairs which carry current and determine power plane inductance. The layer stack-up should maximize adjacent (layer-to-layer) planes at a minimized spacing to achieve the smallest possible inductance. Care must be taken to minimize unnecessary plane splits and holes when locating through-hole components, vias, and connection pads. Minimized inductance will ensure that the board does not develop low frequency noise which may cause the processor to fail (loadline violation).

8.3 **Four-Layer Boards**

A well-designed 4-layer board will feature generous Vcc shapes on the outer layers and large Vss shapes on the inner layers. The Vss-reference requirements for the front side bus are best accommodated with this layer ordering. The power plane area should be maximized and cut-out areas should be carefully placed to minimize parasitic resistance and inductance.



8.4 Six-Layer Boards

Six layer boards provide layout engineers with greater design flexibility. Adjacent plane pairs of the same potential are not useful at higher frequencies, so the best approach is to maximize adjacent, closely spaced Vcc/Vss plane pairs. The plane pair separated by the PCB core material is of lesser importance since it is generally an order of magnitude larger in spacing than other plane pairs in the stack-up. Because the Vss planes are typically full floods of copper, a well-designed six-layer stack-up has four Vcc layers and two layers for Vss. The DC resistive requirements (section 8.1) of the power delivery loop can still be met because the Vss floods are larger than the Vcc floods, and the higher frequency needs are considered as there are four Vcc/Vss plane pairs to deliver current and reduce inductance. In this example stack-up, the two Vss layers should be the inner layers on each side of the PCB core, so that the stack-up is Vcc-Vss-Vcc-(core)-Vcc-Vss-Vcc.