CK98 Clock Synthesizer/Driver Design Guidelines

(Includes CK133 Definition)

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Table of Contents

List of Figures

List of Tables

1. Introduction

This document is designed to provide the industry with the technical specifications required by clock drivers and synthesizers to meet the needs of Intel architecture platforms. Split power supply signaling to provide 2.5V and 3.3V clocks is a stated requirement for this class of products. Additionally, the clocking solution must provide processor and chipset clock frequencies of 133 MHz (7.50 nS period) and 100 MHz (10.00 nS period.)

This document is intended to aid clock circuit suppliers and computer OEMs in defining and using the clock synthesizer components for all desktop system clocking requirements.

The 3.3V power supply is used to power the inputs, some of the outputs, all internal logic and the PLL cores for the clock device. The 2.5V power supply is used to power the remaining outputs for the clock device. Because the two power supplies are independent, and because current PC technology does not control the power sequencing for turning on or turning off the system, latch-up and potentially damaging conditions can exist during these power sequencing phases. **Your design is required to operate properly and make no requirement of the system to sequence the power supplies.**

This 2.5V signaling specification follows the JEDEC standard 8-X. **It should be noted that the preferred implementation of the 2.5V supply will be a 2.5V ±5% voltage regulator. Processor and chipset clock voltages above the specified +5% variation are not allowed.** The 3.3V input signaling specification follows the JEDEC standard for LVTTL signaling. The 3.3V power delivery specification follows the JEDEC standard range 3.3V ±5%.

This document provides a baseline of development for future Intel Architecture processor-based platform clock driver requirements. It is not the only implementation that can be developed; however, this baseline functionality is required for most desktop platforms.

1.1 Clock Synthesizer Overview

Clock synthesizers are expected to source multiple clock types: e.g. Host clock, PCI clock and others as defined by IA system requirements. This document deals with the processor clock, other Host bus clocks, PCI clocks, IOAPIC clocks, 48MHz, and copies of the reference clock. This class of products will also be required to generate fixed frequency 66 MHz outputs.

There are no references to the number of clocks or the types of clocks any given clock driver chip will supply in the main body of the document. Examples of clock synthesizer designs are located in the appendix. The number of clocks and types of outputs, package type and load conditions are also defined.

1.2 Applicable Documents

The latest revision of the following are used as reference documents:

JEDEC Standard No. 8-1A, Interface Standard for 3.3±0.3 V Power Supply & Digital Integrated Circuits.
JEDEC Standard No. 8-X, 2.5V±0.2V (normal range), and 1.8V to 2.7V (wide range) Power supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuit.
PCI Specification 2.1
IBIS Modeling Specification
Audio Codec 98 Specification (AC98)
AGP specification

Other Intel Clock Specification Documents:
CK97 Clock Design Guidelines

See section 6 on how to obtain copies of PCI, AC98, AGP and IBIS specifications.

1.3 Drive Specification

The primary motivation for this document is to specify the issues associated with split I/O voltage and the effects of it on system power delivery, signaling, timing and test. The signaling, timing, and test characteristics change with the different supply voltages and need to be thoroughly understood and simulated for optimal system performance.

The clock driver output buffers are specified in terms of the AC switching characteristics and their DC drive characteristics. The primary electrical parameters are the voltage to current relationship (V/I), and rise and fall time (Trise/Tfall) of the driver through its active switching range.

2. Electrical Requirements

This section details the electrical parameters for two types of 2.5V clock output buffers, multiple types of 3.3V clock output buffers and a 5.0V compatible 3.3V PCI clock driver output buffer. The different types of 2.5V and 3.3V drivers are needed to compensate for corresponding board layout topologies.

Due to the low voltage (<3.0V) required by the CPU, TTL output signaling levels are no longer viable. A signaling level to support 2.5V is being used for that portion of the design. The JEDEC standard called “2.5V±0.2V (normal range), and 1.8V to 2.7V (wide range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuit”, hereafter referred to as 2.5V signaling and 2.5V supply is being used. The 3.3V clocking requirements still support the TTL-level compatible requirements and will be called by their appropriate name, LVTTL, even though they are TTL signaling levels.

A clock driver designed to operate in the 2.5V Pentium® and Pentium® III Processor signaling environment will not necessarily operate correctly in the 3.3V LVTTL or the 5.0V PCI I/O bus signaling environment. Great care must be taken in this design environment to properly support the extremely tight timing requirements between clocks.

The clock driver for all clocks must generate monotonic edges through the input threshold regions as specified for each signaling environment. Many conditions exist in the design of the clock driver and the system that can affect the monotonic operation of the clock driver. Power supply noise, pin inductance and capacitance, ratio of clock signals to Vddq and Vss pins, and routing topology will affect the monotonicity of these clocks. The electrical requirements outlined here ensure components connect directly together without any external buffers or other "glue" logic. Series terminating resistors may be required to keep noise within limits on strong drivers under lightly loaded conditions. Components should be designed to operate within the "commercial" range of environmental parameters. However, this does not preclude the option of other operating environments at the vendor's discretion.

Clock driver output buffers are specified in terms of their V/I curves and Trise/Tfall times. Limits on acceptable V/I curves provide for a maximum output impedance that can achieve acceptable timing in typical configurations, and for a minimum output impedance that keeps the reflected wave within reasonable bounds for signal quality. It is important to understand that drive strength and layout topology go hand in hand. Point-to-point or multiple stubs at the receiver end will work with a weaker driver, whereas a route that splits at the driver requires a stronger buffer. The signal quality problems of a strong driver under light loads can be negated somewhat with a series termination resistor placed as close to the driver as possible. See Section 5 for more detail.

Examples of possible clock driver designs are contained in the appendices. These are not the only solutions that can be achieved, but are a good starting point to design a component to meet specific design requirements.

Due to the mixed power supplies now required for proper system operation, it is very important to understand that specific power supply sequencing is not supported. The clock synthesizer CANNOT force power sequencing requirements in the system.

2.1 DC Specifications

DC parameters must be sustainable under steady state (DC) conditions.

Table 1 Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	-0.5	4.6	V	
V_{DDQ2}	2.5V I/O Supply Voltage	-0.5	3.6	V	
V_{DDQ3}	3.3V I/O Supply Voltage	-0.5	4.6	V	
Ts	Storage Temperature	-65	150	°C	

Table 2 Absolute Maximum DC I/O

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ih3}	3.3V Input High Voltage	-0.5	4.6	V	1
V_{il3}	3.3V Input Low Voltage	–0.5		V	
ESD prot.	Input ESD protection	2000		V	2

Notes:

1. Maximum Vih is not to exceed maximum V_{DD3} + 0.5 V.
2. Human body model.

Table 3 DC Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{DDQ3}	3.3V I/O Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{DDQ2}	2.5V I/O Supply Voltage	2.5V ±5%	2.375	2.625	V	4
$V_{DD\ 3}$= 3.3V±5%						
V_{ih3}	3.3V Input High Voltage	VDD3	2.0	V_{DD}+0.3	V	7
V_{il3}	3.3V Input Low Voltage		V_{SS}-0.3	0.8	V	7
I_{il}	Input Leakage Current	$0 < V_{in} < V_{DDQ3}$	-5	+5	µA	3, 7
V_{DDQ2} = 2.5V±5%						
V_{oh2}	2.5V Output High Voltage	Ioh = -1 mA	2.0		V	1
V_{ol2}	2.5V Output Low Voltage	Iol = 1 mA		0.4	V	1
V_{DDQ3}= 3.3V±5%						
V_{oh3}	3.3V Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{ol3}	3.3V Output Low Voltage	Iol = 1 mA		0.4	V	1
V_{DDQ3}= 3.3V±5%						
V_{poh}	PCI Bus Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{pol}	PCI Bus Output Low Voltage	Iol = 1 mA		0.55	V	1, 5
C_{in}	Input Pin Capacitance			5	pF	2
C_{xtal}	Xtal Pin Capacitance		13.5	22.5	pF	6
Cout	Output Pin Capacitance			6	pF	2
L_{pin}	Pin Inductance			7	nH	2
Ta	Ambient Temperature	No Airflow	0	70	°C	

Notes:

1. Signal edge is required to be monotonic when transitioning through this region.
2. This is a recommendation, not an absolute requirement as the package size and type are not being specified. The actual value should be provided with the component data sheet.
3. Input Leakage Current does not include inputs with Pull-Up or Pull-down resistors. Inputs with resistors should state current requirements.
4. No power sequencing is implied or allowed to be required in the system.
5. Conforms to 5V PCI Signaling specification.
6. As seen by the crystal. Device is intended to be used with a 17-20pF AT crystal. See next section for more details.
7. All inputs referenced to 3.3V power supply.

2.1.1 Load Capacitance As Seen By External Crystal Reference

Earlier clock design guidelines do not specify a target load capacitance for the clock synthesizer as seen by the crystal. Most of the clock vendors targeted 12-13 pF due to historical reasons but, few vendors specified the variation in their datasheets. However, the common crystals used today are in the 17-20 pF range.

To reduce the ambiguity with this issue, this specification requires that the clock driver load capacitance (as seen by the crystal, **not the capacitance of the individual XTAL_IN and XTAL_OUT pins**) be targeted **at 18pF ± 25%.** This specification includes the clock driver component only and does not include any capacitance associated with board vias and traces.

Doing this:

- Directs all designs to the same target load capacitance.
- Requires testing/guarantee by design of the variation.
- Eliminates external compensation capacitors if the frequency variation can be tolerated.

2.2 Buffer Specifications:

The V/I curves, and Trise/Tfall specifications are targeted at achieving acceptable switching behavior under the lumped load conditions as described in section 4 of this document. Pull-up and pull-down sides for each of the buffers have separate V/I curves, which are provided, in the following sections. The DC drive curve specifies steady state conditions that must be maintained, but does not indicate real output drive strength.

AC parameters must be guaranteed under transient switching (AC) conditions. The sign on all current parameters (direction of current flow) is referenced to a ground inside the component; i.e. positive currents flow into the component while negative currents flow out of the component.

Table 4 Buffer Types

Buffer Name	VCC Range (V)	Impedance (Ohms)	Buffer Type
CPU, CPU_Div2, IOAPIC	2.375 - 2.625	13.5 - 45	Type 1
48MHz, REF	3.135 - 3.465	20 - 60	Type 3
PCI, 3V66	3.135 - 3.465	12 - 55	Type 5

1. CK98 buffer types are a subset of previous clock driver design guidelines. Type 2 and Type 4 buffer types are not required for this implementation.

2.2.1 TYPE 1: Buffer Characteristics

Table 5 TYPE 1: Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-27			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 2.375 V			-27	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.2 V	27			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.3 V			30	mA	1
T_{rh}	2.5V Type 1 Output Rise Edge Rate	2.5V ±5% @ 0.4V - 2.0 V	1/1		4/1	V/nS	2
T_{fh}	2.5V Type 1 Output Fall Edge Rate	2.5V ±5% @ 2.0V - 0.4 V	1/1		4/1	V/nS	2

Notes:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 8 CK133 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.7 and Vih=1.7 Volts.
5. Ron 13.5-45 Ohm with a 29 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-28	-61	-107
0.4	-28	-61	-107
0.6	-28	-61	-107
0.8	-28	-61	-107
1	-27	-60	-105
1.2	-26	-58	-101
1.4	-24	-53	-94
1.6	-21	-48	-85
1.8	-17	-40	-73
1.9	-15	-36	-67
2	-12	-31	-59
2.1	-9	-25	-51
2.2	-6	-20	-43
2.3	-3	-14	-34
2.375	0	-9	-27
2.5		0	-14
2.625			0

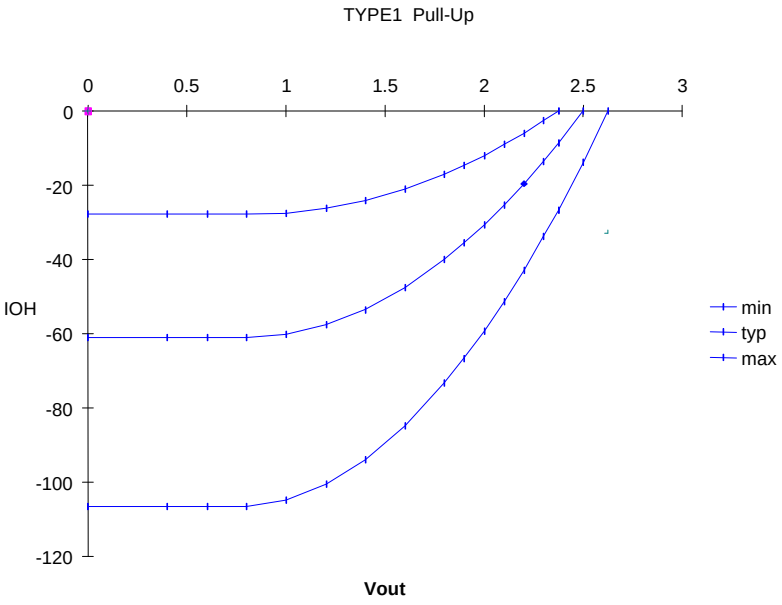


Figure 1 TYPE 1: Pull-Up Characteristics

Notes (Figure 1)**:**

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing.

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.1	3	7	11
0.2	6	13	21
0.3	9	19	30
0.4	12	24	40
0.5	15	30	48
0.6	17	35	56
0.7	19	39	63
0.8	21	43	70
0.9	23	47	77
1	24	50	83
1.1	25	53	88
1.2	27	56	93
1.3	27	58	97
1.4	28	60	100
1.6	29	62	106
1.8	29	63	110
2	29	63	111
2.2	29	63	111
2.375	29	63	111
2.5		63	111
2.625			111

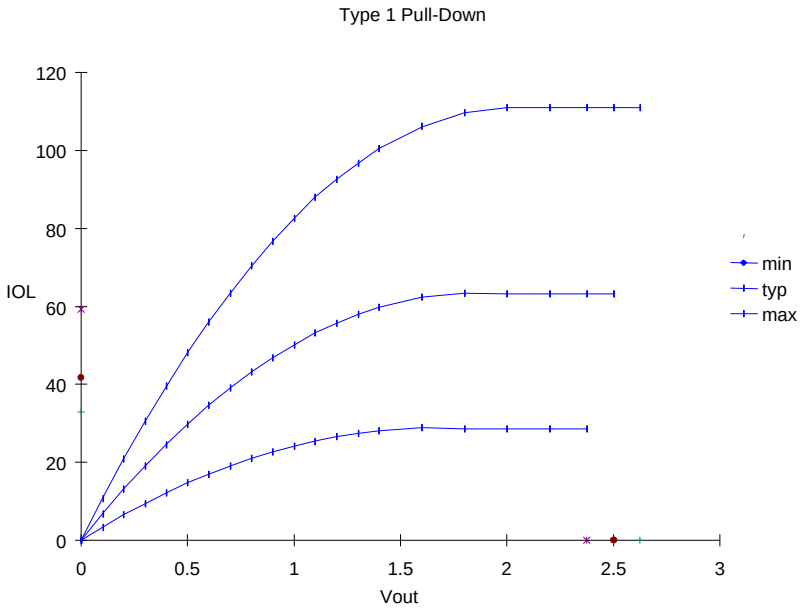


Figure 2 TYPE 1: Pull-Down Characteristics

Notes (Figure 2)**:**

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing.

2.2.2 TYPE 3: Buffer Characteristics

Table 6 Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-29			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-23	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95 V	29			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			27	mA	1
t_{rh}	3.3V Type 3 Output Rise Edge Rate	3.3V ±5% @ 0.4V – 2.4 V	0.5		2.0	V/nS	2
t_{fh}	3.3V Type 3 Output Fall Edge Rate	3.3V ±5% @ 2.4V – 0.4 V	0.5		2.0	V/nS	2

Notes:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Waveform Figure for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC, process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 20-60 Ohm with a 40 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.

Pull-Up			
Voltage	I (mA)	I (mA)	I (mA)
(V)	min	typ	max
0	-29	-46	-99
1	-29	-46	-99
1.4	-27	-44	-94
1.5	-27	-43	-92
1.65	-25	-41	-89
1.8	-24	-39	-85
2	-22	-36	-79
2.4	-16	-28	-63
2.6	-12	-22	-53
3.135	0	-6	-23
3.3		0	-12
3.465			0

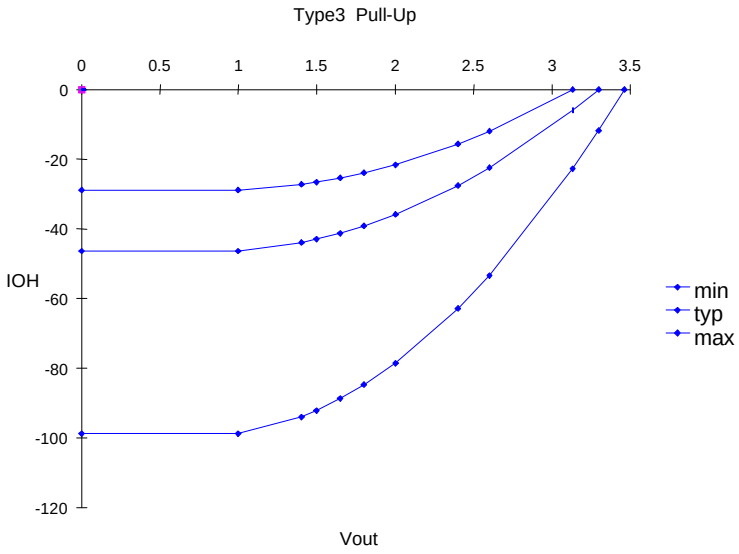


Figure 3 TYPE 3: Pull-Up Characteristics

Notes (Figure 3)**:**

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 6 Operating Requirements. .

Pull-Down			
Voltage	I (mA)	I (mA)	I (mA)
(V)	min	typ	max
0	0	0	0
0.4	9	13	27
0.65	14	21	41
0.85	17	26	52
1	20	29	59
1.4	25	37	76
1.5	26	39	79
1.65	27	41	84
1.8	28	43	88
1.95	29	45	92
3.135	29	45	102
3.6		45	102

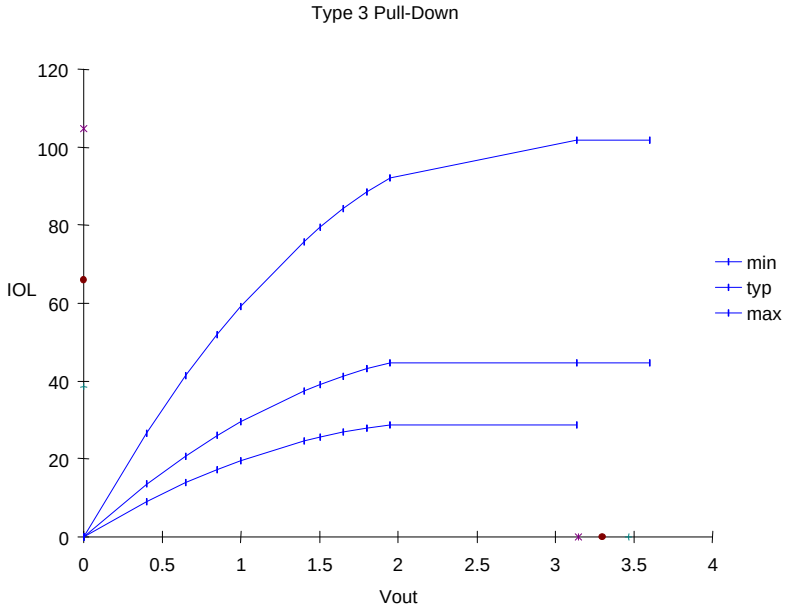


Figure 4 TYPE 3: Pull-Down Characteristics

Notes (Figure 4)**:**

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing.

2.2.3 TYPE 5: Buffer Characteristics

Table 7: Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-33			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-33	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95 V	30			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			38	mA	1
T_{rh}	3.3V Type 4 Output Rise Edge Rate	3.3V ±5% @ 0.4V - 2.4 V	1/1		4/1	V/nS	2
T_{fh}	3.3V Type 4 Output Fall Edge Rate	3.3V ±5% @ 2.4V - 0.4 V	1/1		4/1	V/nS	2

Notes:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 8 CK133 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 12-55 Ohm with a 30 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.
7. See PCI specification for additional PCI details.

	Pull-Up		
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-34	-59	-195
1	-33	-58	-194
1.4	-31	-55	-189
1.5	-30	-54	-184
1.65	-28	-52	-172
1.8	-25.5	-50	-159
2	-22	-46	-140
2.4	-14.5	-35	-100
2.6	-11	-28	-83
3.135	0	-6	-33
3.3		0	-19
3.6			0

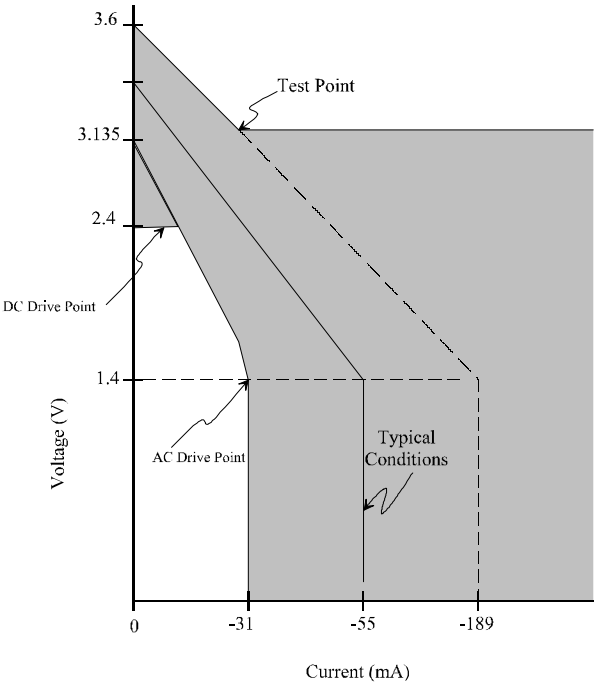


Figure 5 TYPE 5: Pull-Up Characteristics

Notes (Figure 5):

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements.
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to it and to Table 7: Operating Requirements

Pull-Down			
Voltage (V)	I (mA) min	I(mA) typ	I (mA) max
0	0	0	0
0.4	9.4	18	38
0.65	14	30	64
0.85	17.7	38	84
1	20	43	100
1.4	26.5	53	139
1.5	28	55	148
1.65	29	56	163
1.8	30	57	175
1.95	30	58	178
3.135	31	59	187
3.6	32	59	188

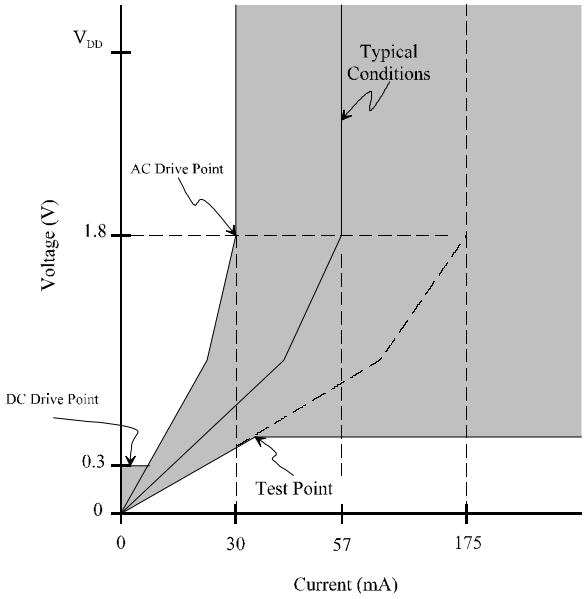


Figure 6 TYPE 5: Pull-Down Characteristics

Notes (Figure 6)**:**

1. Must meet the temperature and voltage range specified in Table 3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to it and to Table 7: Operating Requirements

2.2.4 Vendor Provided Specifications

Vendors should make the following information available in their data sheets:

- Pin capacitance for all pins (min and max).
- Pin inductance for all pins (min and max).
- Output V/I curves under switching conditions. Two graphs/tables should be given for each output type used: one for driving high, the other for driving low. Both should show best and worst case conditions.
- Loaded rise/fall times for each output type for loads as specified in the test section of this document.
- Absolute maximum data, including operating and non-operating temperature, DC maximums, etc.

It is strongly recommended that component vendors make the following information electronically available in the IBIS model format. Include the following minimum information:

- Output V/I curves under switching conditions. Two curves should be supplied one for driving high, the other for driving low. Both should show best-typical-worst curves.
- Unloaded rise/fall times for each output type as specified by IBIS.
- Package Resistance (R_pkg [min, max]), Package Inductance (L_pkg [min, max]), Package Capacitance (C_pkg [min, max]); Component Capacitance (C_comp [min, max]).

3. AC Timing

3.1 Timing Requirements

Table 8 Host Bus AC Timing Requirements

		133 MHz Host		100 MHz Host			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
TPeriod	Host/CPU CLK period	7.5	7.65	10.0	10.3	nS	2, 9
THIGH	Host/CPU CLK high time	1.87	N/A	3.0	N/A	nS	5, 10
TLOW	Host/CPU CLK low time	1.67	N/A	2.8	N/A	nS	6, 10
TRISE	Host/CPU CLK rise time	0.4	1.6	0.4	1.6	nS	8
TFALL	Host/CPU CLK fall time	0.4	1.6	0.4	1.6	nS	8
TPeriod	CPU_Div2 CLK period	15.0	15.3	20.0	20.6	nS	2, 9
THIGH	CPU_Div2 CLK high time	5.25	N/A	7.5	N/A	nS	5, 10
TLOW	CPU_Div2 CLK low time	5.05	N/A	7.3	N/A	nS	6, 10
TRISE	CPU_Div2 CLK rise time	0.4	1.6	0.4	1.6	nS	8
TFALL	CPU_Div2 CLK fall time	0.4	1.6	0.4	1.6	nS	8
TPeriod	IOAPIC CLK period	60.0	61.2	60.0	61.2	nS	2, 9
THIGH	IOAPIC CLK high time	25.5	N/A	25.5	N/A	nS	5, 10
TLOW	IOAPIC CLK low time	25.3	N/A	25.3	N/A	nS	6 ,10
TRISE	IOAPIC CLK rise time	0.4	1.6	0.4	1.6	nS	8
TFALL	IOAPIC CLK fall time	0.4	1.6	0.4	1.6	nS	8
TPeriod	3V66 CLK period	15.0	15.3	15.0	15.3	nS	2, 4, 9
THIGH	3V66 CLK high time	4.95	N/A	4.95	N/A	nS	5 ,10
TLOW	3V66 CLK low time	4.55	N/A	4.55	N/A	nS	6 ,10
TRISE	3V66 CLK rise time	0.5	2.0	0.5	2.0	nS	8
TFALL	3V66 CLK fall time	0.5	2.0	0.5	2.0	nS	8
TPeriod	PCI CLK period	30.0	N/A	30.0	N/A	nS	2, 3, 9
THIGH	PCI CLK high time	12.0	N/A	12.0	N/A	nS	5 ,10
TLOW	PCI CLK low time	12.0	N/A	12.0	N/A	nS	6 ,10
TRISE	PCI CLK rise time	0.5	2.0	0.5	2.0	nS	8
TFALL	PCI CLK fall time	0.5	2.0	0.5	2.0	nS	8
TPeriod	48 MHz CLK period	20.83	20.83	20.83	20.83	nS	2, 3, 9
THIGH	48 MHz CLK high time	7.57	N/A	7.57	N/A	nS	5 ,10
TLOW	48 MHz CLK low time	7.17	N/A	7.17	N/A	nS	6 ,10
TRISE	48 MHz CLK rise time	1.0	4.0	1.0	4.0	nS	8
TFALL	48 MHz CLK fall time	1.0	4.0	4.0	4.0	nS	8
tpZL, tpZH	Output enable delay (All outputs)	1.0	10.0	1.0	10.0	nS	
tpLZ, tpZH	Output disable delay (All outputs)	1.0	10.0	1.0	10.0	nS	

tstable	All clock Stabilization from power-up		3		3	mS	7

Notes:

1. Output drivers must have monotonic rise/fall times through the specified VOL/VOH levels.
2. Period, jitter, offset and skew measured on rising edge @1.25V for 2.5V clocks and @ 1.5V for 3.3V clocks.
3. The PCI clock is the Host clock divided by four at Host=133MHz. PCI clock is the Host clock divided by three at Host = 100MHz.
4. 3V66 is internal VCO frequency divided by four for Host=133MHz. 3V66 clock is internal VCO frequency divided by three for Host=100MHz
5. THIGH is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
6. TLOW is measured at 0.4V for all outputs.
7. The time specified is measured from when Vddq achieves its nominal operating level (typical condition Vddq = 3.3V) till the frequency output is stable and operating within specification.
8. TRISE and TFALL are measured as a transition through the threshold region VOL and VOH.
9. The average period over any 1 uS period of time must be greater than the minimum specified period
10. Calculated at minimum edge-rate (1V/nS) to guarantee 45/55% duty-cycle. Pulse width is required to be wider at faster edge-rate to ensure duty-cycle specification is met.

Table 9 Group Skew And Jitter Limits

Output group	Pin-pin Skew MAX	Cycle-Cycle Jitter	Duty Cycle	Nom Vdd	Skew, jitter measure point
CPU	175 pS	250 pS	45/55	2.5 V	1.25 V
CPU_Div2	175 pS	250 pS	45/55	2.5 V	1.25 V
IOAPIC	250 pS	500 pS	45/55	2.5 V	1.25 V
48MHz	N/A	500 pS	45/55	3.3 V	1.5 V
3V66	250 pS	500 pS	45/55	3.3 V	1.5 V
PCI	500 pS	500 pS	45/55	3.3 V	1.5 V
REF	N/A	1000 pS	45/55	3.3V	1.5 V

Table 10 Group Offset limits

Group	Offset	Measurement loads (lumped)	Measure Points
CPU to 3V66	0.0-1.5 nS CPU leads	CPU@20 pF, 3V66@30 pF	CPU@1.25 V, 3V66@1.5 V
3V66 to PCI	1.5-4.0 nS 3V66 leads	3V66@30 pF, PCI@30 pF	3V66@1.5 V, PCI@1.5 V
CPU to IOAPIC	1.5-4.0 nS CPU leads	CPU@20 pF, IOAPIC@20 pF	CPU@1.25 V, IOAPIC@1.25 V

Notes:

1. All offsets are to be measured at rising edges

Only offset specifications listed above are required to be guaranteed/tested. The specification should be treated as ANY output within first specified bank to ANY output of the second specified bank. Pin-pin skew is implied within offset specification, jitter is not. Previous offset specifications such as CPU to PCI offset are no longer required.

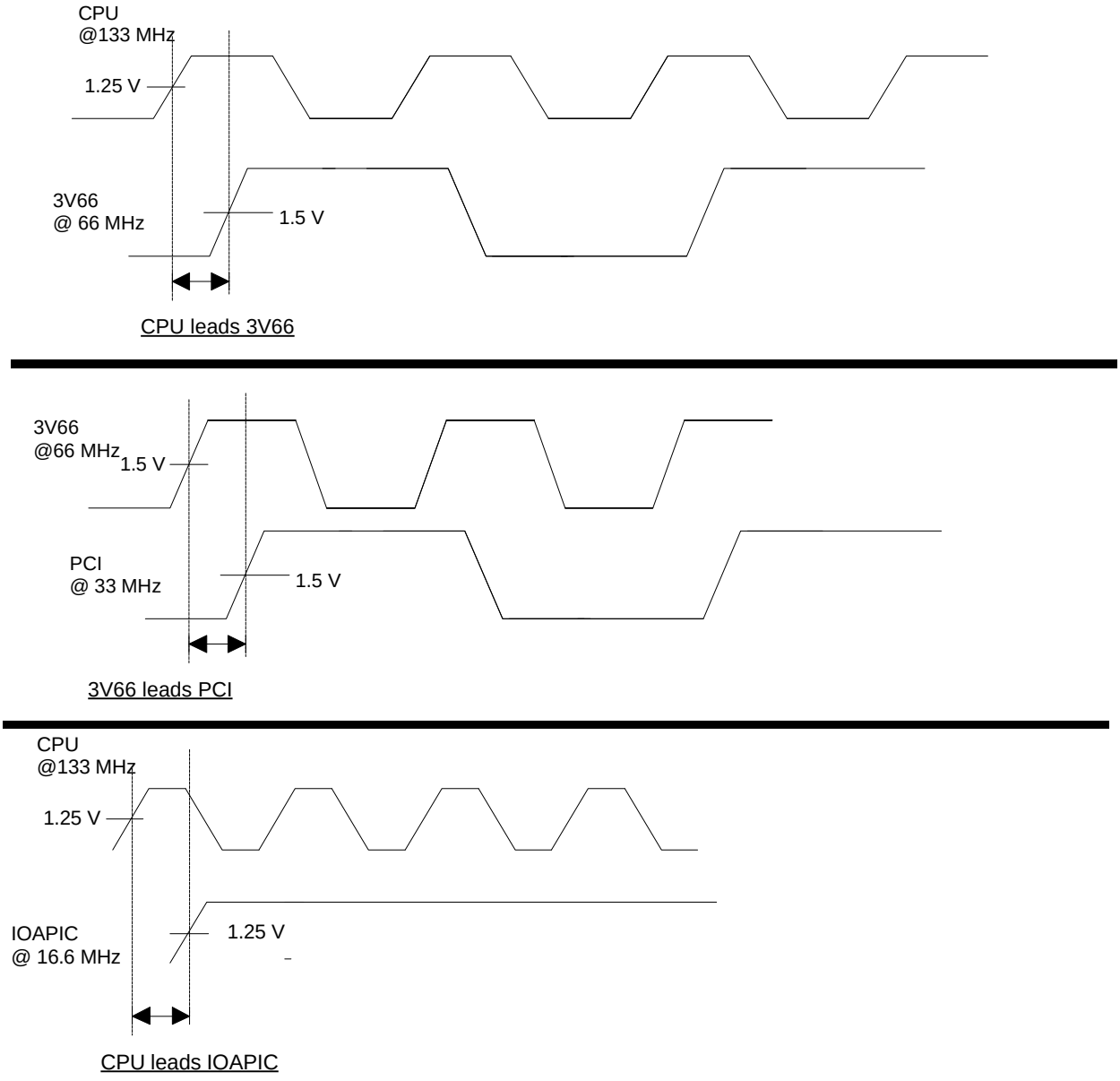


Figure 7 Group Offset Waveforms

3.1.1 Frequency Accuracy of 48MHz outputs

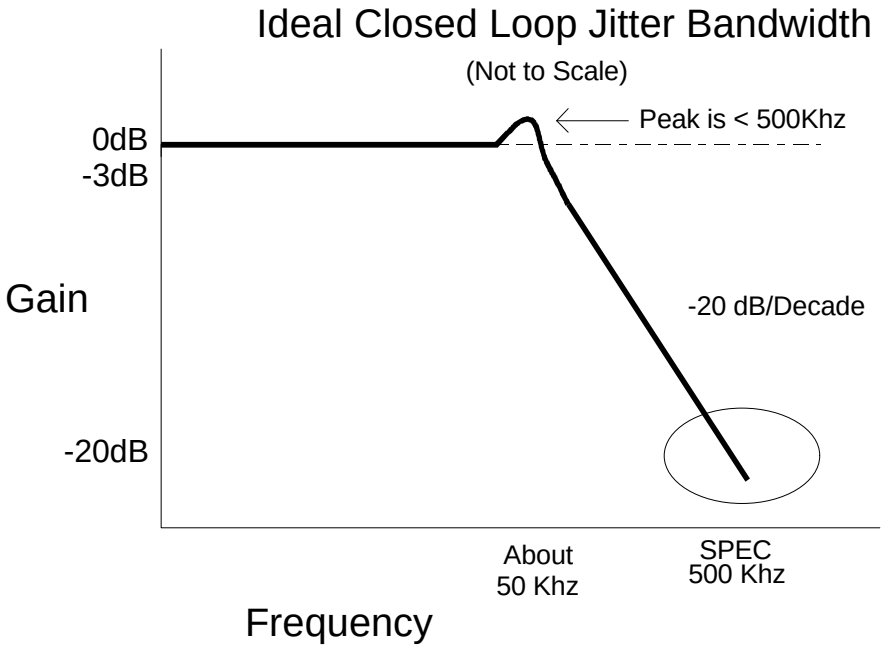
The 48 MHz PPM of the nominal frequency is REQUIRED to be +167 from 48.00MHz to conform to the USB default frequency accuracy specification.

3.1.2 Multiple PLL Jitter Tracking Specification.

The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. This 1:1 relationship is critical when the clock driver drives two or more PLLs. A worst case timing issue would occur if one PLL attenuated the jitter and another device (PLL or non-PLL) tracked the jitter completely. To reduce the possibility of this we require that the -20dB attenuation point be less than or equal to 500Khz. Most clock vendors do not specify their jitter bandwidth characteristics or specify it only at the -3dB level. To allow for greatest flexibility in loop design we require the vendor to provide the -20dB point. This specification may be guaranteed by design and/or measured with a spectrum analyzer.

This specification is intended to replace/clarify the Pentium® processor specification which was stated as:

"To ensure a 1:1 jitter frequency relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 kHz and 1/3 of the clock operating frequency."



4. Test and Measurement

Board level simulations are usually done using ideal output buffer models which are defined/modeled with no output load. The typical source of these models comes from one or more Silicon level simulators. Clock driver vendor validation of these models under a no load condition is extremely time consuming. The table below provides acceptable lumped load test loads over which the vendor is expected to test/guarantee all AC parameters for the clock driver. The vendor is encouraged to provide information on the correlation between lumped load performance and no-load performance as an applications exercise to fully describe the operation of the product.

Table 11 Minimum and Maximum Lumped Capacitive Test Loads

Clock	Min Load	Max Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads.
PCI Clocks (PCLK)	10	30	pF	Must meet PCI 2.1 requirements
CPU_div2	10	20	pF	1 device load, possible 2 loads
3V66	10	30	pF	1 device load, possible 2 loads
48 MHz Clock	10	20	pF	1 device load
REF	10	20	pF	1 device load
IOAPIC	10	20	pF	1 device load

Notes:

1. Maximum rise/fall times are to be guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are to be guaranteed at minimum specified load for each type of output buffer
3. Rise/fall times are specified with pure capacitive load as shown. Testing may be done with an additional 500 ohm resistor in parallel if properly correlated with the capacitive load.

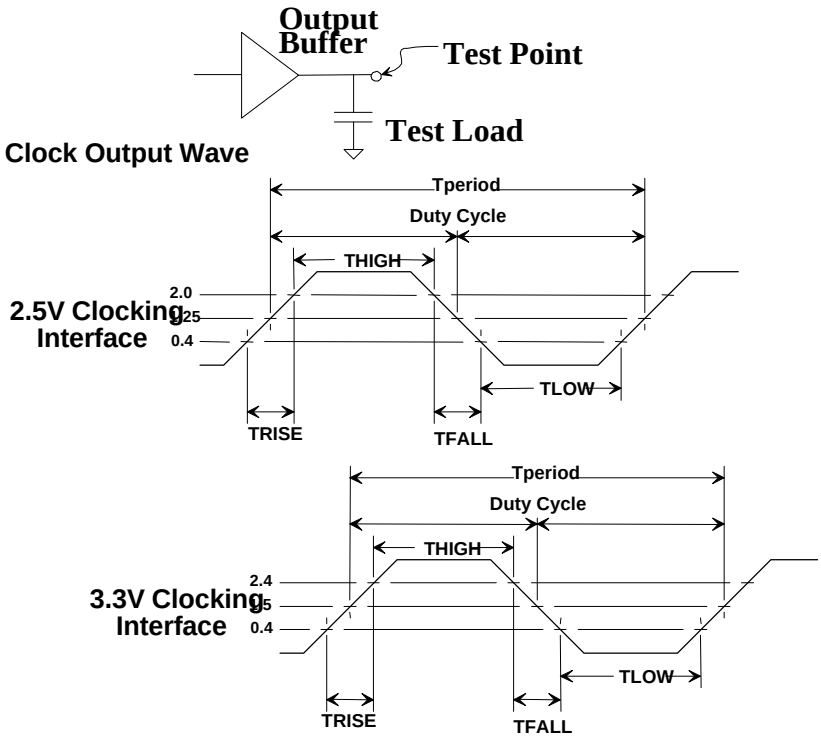


Figure 8 CK133 Clock Waveforms

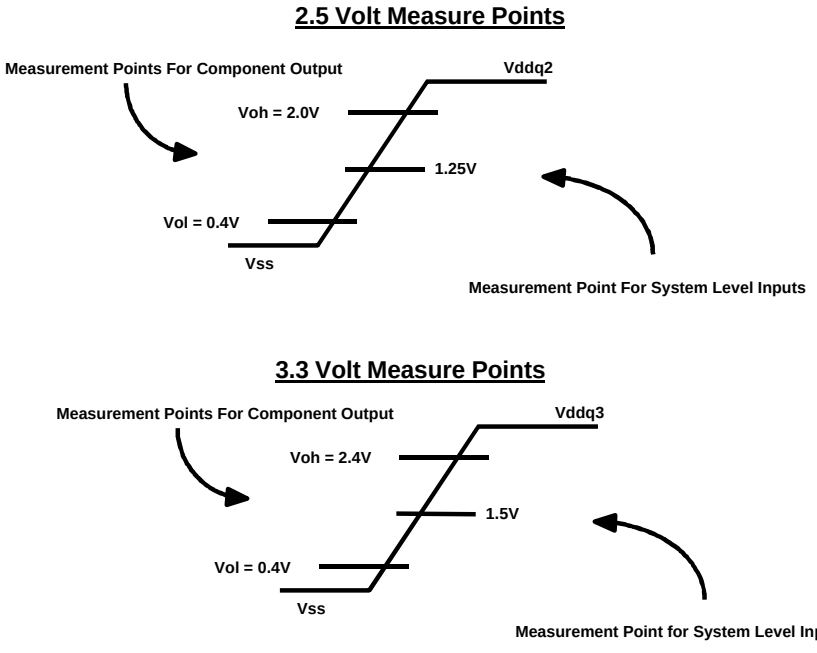


Figure 9 Component Versus System Measure Points

5. System Considerations

The diagrams shown below are typical clock routing topologies for the Pentium® III processor-based desktop platforms. These are meant as an aid to the OEM in laying out clocks for PC Desktop platforms. It is also meant as an aid to clock driver vendors to simulate and check their buffers. All clock layouts must be simulated by the board designer to guarantee compatibility across different clock and board processes.

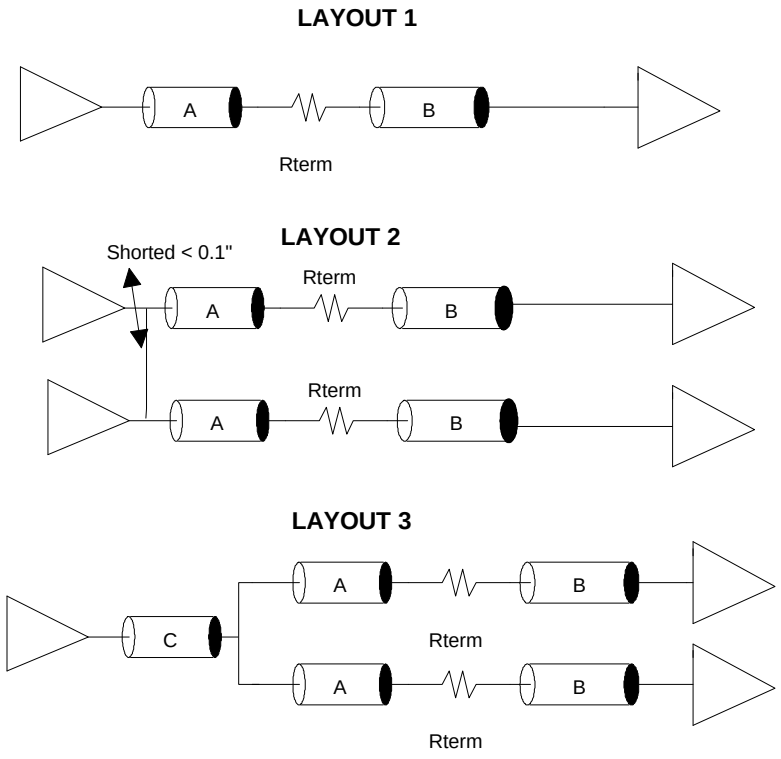


Figure 10 Typical Clock Layout Topologies

Table 12 Layout Dimensions

CLK	Topology	A	B	C	D	R_{TERM}	Notes
CPU, IOAPIC, CPU_Div2, PCI, 3V66	LAYOUT 1	0.25”- 0.5 “	3” - 7”	n/a	n/a	33	1
CPU	LAYOUT 2	0.1”- 0.25”	3” - 6”	n/a	n/a	33	2
48MHz, REF	LAYOUT 1	0.25”- 0.5”	3” - 7”	n/a	n/a	22	3

Notes:
1. Primary topology for CPU outputs. One load.
2. Secondary topology for CPU outputs. Two loads.
3. Point-to-Point only

Table 13 Board Level Simulation Conditions

Symbol	*Parameter*	*Slow*	*Typ*	*Fast*
Z_O	Line Impedance	54 Ω	60 Ω	66 Ω
S	Line Velocity	2.2 nS/ft	1.9 nS/ft	1.6 nS/ft
V_{DD}	Core Supply Voltage	3.135 V	3.30 V	3.465 V
V_{DDQ}	IO Supply Voltage	2.375 V	2.5 V	2.625 V
T	Ambient Temperature (no airflow)	70° C	25° C	0° C

The topologies listed above in Figure 10 are typical topologies for Desktop PC clock routings. The parameters listed in Table 12 give typical minimum and maximum dimension ranges to be used for clock buffer driver simulation.

Series termination resistors will be required to control the output driver variation from platform to platform. Series termination should be placed as close to the driver as possible for best signal quality results.

Table 14 Typical DC Characteristics at 3.3V Clock Destination

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{ih3}	3.3V Input High Voltage		2.0	V_{DDQ} + .3	V	1
V_{il3}	3.3V Input Low Voltage		-0.3	0.8	V	1
C_{in}	Input Pin Capacitance			6 - 9	pF	

Notes:
1. Signal edge is required to be monotonic when transitioning through this region.

The clock input to the processor and other system components must meet signal quality specifications to guarantee the clock signal is sensed properly and to ensure the clock signal does not affect the long term reliability of the components. There are two AC signal quality parameters defined: Overshoot/Undershoot and Ringback. Typically, these values are determined by board designers as the result of multiple system level simulations. However, the data has been provided to allow the clock driver vendor to complete a first approximation of these system events. These simulations are encouraged and should be seen as a step in the validation of the IBIS models for the device. Each device will have a different sensitivity to the over and undershoot, due to various input capacitance and clamping circuits. Board impedance, termination and trace topology will dominate these measurements. The specifications should be taken as applications information and a design target for the clock driver vendor, but should be met by the board designer.

Table 15 AC Signal Quality Requirements at Destination

Symbol	Parameter	Min	Max	Units	Notes
T_{over} CPU/Chipset	Overshoot/Undershoot Voltage		Vddq +0.7 Vss - 0.7	V	
T_{ring} CPU/Chipset	Ring back		Vih Vil	V	

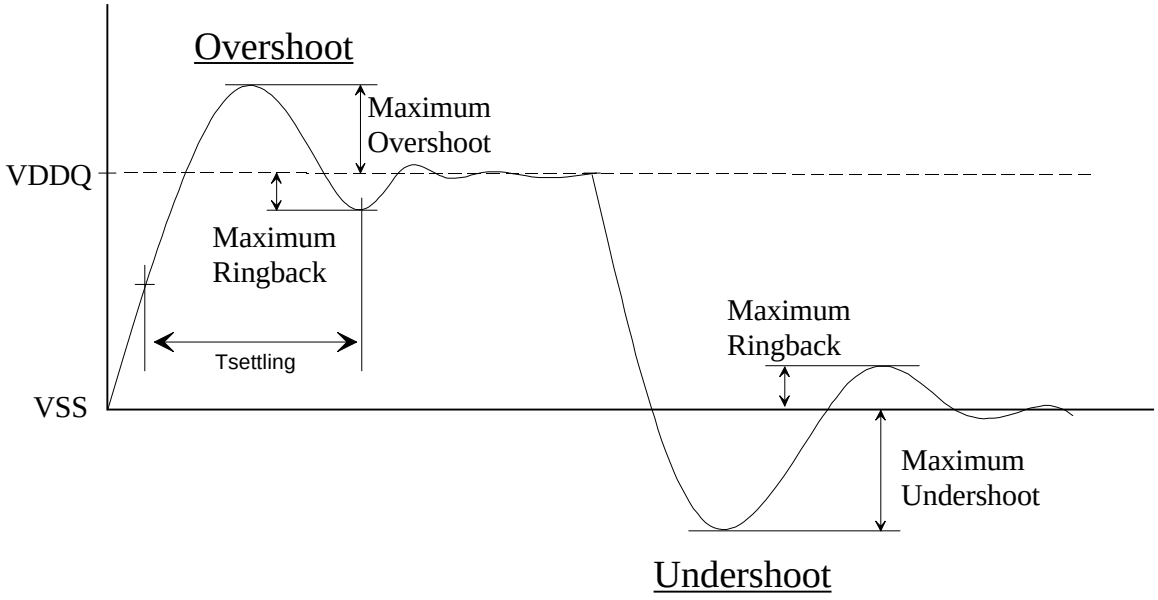


Figure 11 Overshoot & Undershoot

6. How To Obtain Reference Material

6.1 PCI Reference

The PCI Special Interest Group is an industry-wide group that controls the official PCI specification. You can obtain the latest copies of the PCI specification by contacting the PCI Special Interest Group at the following numbers:

(800) 433-5177 - USA
(503) 797-4297 - International
(503) 234-6762 - Fax

There is a nominal fee for obtaining this specification.

6.2 IBIS Reference

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are on-line at "vhdl.org". To join in the email discussions, send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

The IBIS home page can be found at **http://www.eia.org/eig/ibis/ibis.htm**

6.3 Audio Codec 98 (AC98) Reference

The AC97 home page can be found at **http://www.intel.com/pc-supp/platform/aud98**

6.3 AGP Reference

AGP information can be found at **http://developer.intel.com/solutions/tech/agp.htm**

7. Appendices

7.1 Appendix A: CK133 56 pin SSOP Pin-out

The following addendum defines a generic pin-out and base requirements for Intel Architecture based platforms. It is intended to be used with another clock driver to clock the memory devices. This appendix can be used as an example for development of other custom clock components. This is not the only solution that can be derived.

Features (56 Pin SSOP Package):

- Four copies of CPU Clock
- Eight copies of PCI Clock (Synchronous w/CPU Clock). One free running PCI.
- Two CPU/2 outputs for synchronous memory reference
- Four copies of fixed frequency 3.3V Clock
- Three copies of IOAPIC Clock @16.667 MHz, synchronous to CPU Clock
- One copy of 48MHz Clock
- Two copies of Ref. Clock @14.31818 MHz
- Ref. 14.31818MHz Xtal Oscillator Input
- 133MHz or 100MHz operation
- Power Management Control Input Pins

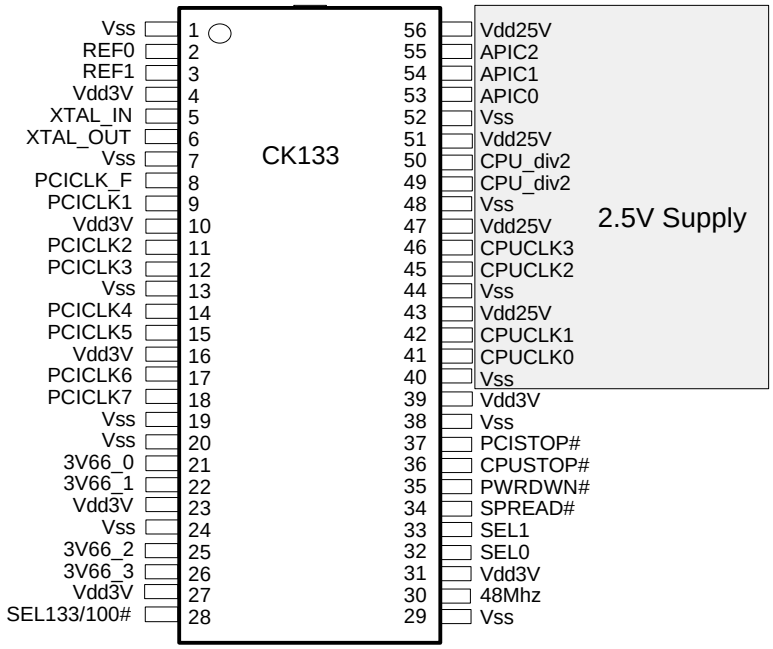


Table 16 CK133 Pin Description Table

Pin	Type	Qty	Symbol	Description
2,3	output	2	REF [0-1]	3.3V 14.318 MHz clock output
5	input	1	XTAL_IN	14.318 MHz Crystal input
6	output	1	XTAL_OUT	14.318 MHz Crystal output
8	output	1	PCICLK_F	3.3V Free running PCI clock
9,11,12,14,15,17,18	output	7	PCICLK [1-7]	3.3V PCI clock outputs
21,22,25,26	output	4	3V66 [0-3]	3.3V Fixed 66MHz clock outputs
28	input	1	SEL133/100#	3.3V LVTTL compatible input for 133MHz or 100MHz CPU outputs. H = 133MHz, L = 100MHz
30	output	1	48MHz	3.3V Fixed 48MHz clock output
32,33	input	2	SEL [0-1]	3.3V LVTTL compatible inputs for logic selection
34	input	1	SPREAD#	3.3V LVTTL compatible input. Enables spread spectrum mode when held LOW
35	input	1	PWRDWN#	3.3V LVTTL compatible input. Device enters power-down mode when held LOW
36	input	1	CPUSTOP#	3.3V LVTTL compatible input. Stops all CPU, and 3V66 clocks when held LOW. CPU_div2 output remains on all the time.
37	input	1	PCISTOP#	3.3V LVTTL compatible input. Stops all PCI clocks except PCICLK_F when held LOW
41,42,45,46	output	4	CPUCLK [0-3]	2.5V Host bus clock output. 133MHz or 100MHz depending on state of SEL133/100#
49,50	output	2	CPU_div2[0-1]	2.5V output running at 1/2 CPU (Host bus) clock frequency. 66MHz or 50MHz depending on state SEL133/100#
53,54,55	output	3	APIC [0-2]	2.5V clock outputs running divide synchronous with the CPU (Host bus) clock frequency. Fixed 16.67MHz limit. If CPU = 133MHz, APIC = CPU/8 If CPU = 100MHz, APIC = CPU/6
4,10,16,23,27,31,39	3.3V Power	7	Vdd3V	3.3V power supply
1,7,13,19,20,24,29,38,40,44,48,52	Vss	12	Vss	Ground
43,47,51,56	2.5V Power	4	Vdd25V	2.5V power

7.1.1 Spread Spectrum Clocking (SSC) Clarification:

Spread Spectrum functionality on the CK133 clock driver is required by most OEMs and acts as an on/off switch for different forms of spread spectrum modulation techniques. Any given OEM may or may not use this feature due to platform-level timing issues. The following specifications are added to the current CK133 definition:

1. No external modulation frequency source is required by the CK133.
2. Vendor needs to synchronously modulate all the CPU, PCI, APIC, 3V66, and CPU/2 output clocks. REF and fixed frequency 48MHz clock outputs are not modulated.
3. All device timings (including jitter, skew, min-max clock period, output rise/fall time) MUST meet the existing non-spread spectrum specifications
4. All non-spread CPU and PCI functionality must be maintained in the spread spectrum mode (includes all power management functions.)
5. The minimum clock period cannot be violated. The preferred method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called “down-spreading”. An example triangular frequency modulation profile is shown in Figure 12. The modulation profile in a modulation period can be expressed as:

$$f = \begin{cases} (1-\mathrm{d})\, f_{nom} + 2 f_m \cdot \mathrm{d} \cdot f_{nom} \cdot t & when \quad 0 < t < \dfrac{1}{2 f_m}; \\ (1+\mathrm{d})\, f_{nom} - 2 f_m \cdot \mathrm{d} \cdot f_{nom} \cdot t & when \quad \dfrac{1}{2 f_m} < t < \dfrac{1}{f_m}, \end{cases}$$

where f_{nom} is the nominal frequency in the non-SSC mode, f_m is the modulation frequency, δ is the modulation amount, and t is time.

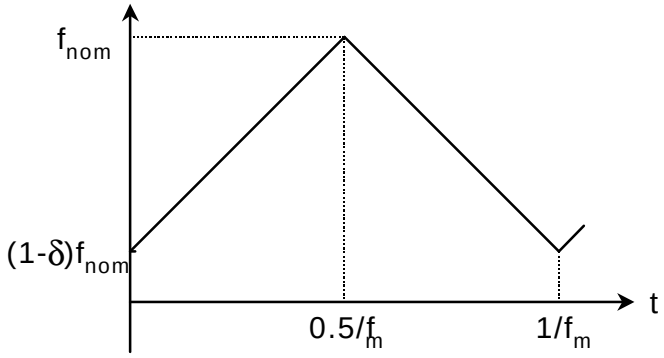


Figure 12 Triangular Frequency Modulation Profile.

6. For triangular modulation, the clock frequency deviation (δ) is required to be no more than 0.6% “down-spread” from the corresponding nominal frequency, i.e., +0%/-0.6%. The absolute spread amount at the fundamental frequency is shown in Figure 13, as the width of its spectral distribution (between the -3dB roll-off). The ratio of this width to the fundamental frequency cannot exceed 0.6%. This parameter can be measured in the frequency domain using a spectrum analyzer. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream PLL tracking skew (see explanation in 8), which cannot exceed that of a 0.6% triangular modulation. Typically, it is about 0.5%.

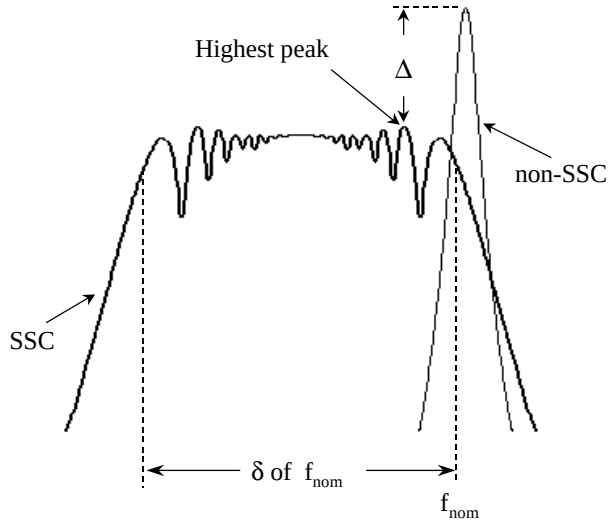


Figure 13 Spectral Fundamental Frequency Comparison

7. To achieved sufficient system-level EMI reduction, it is desired that SSC reduce the spectral peaks in the non-SSC mode by the amount specified in Table 17. The peak reduction Δ is defined, as shown in Figure 13, as the difference between the spectral peaks in SSC and non-SSC modes at the specified measurement frequency

Table 17 Desired Peak Amplitude Reduction by SSC.

CPU Clock Freq.	Peak Reduction Δ	Measurement Freq.
133 MHz	7 dB	666 MHz (5^{th} harmonics)
100 MHz	7 dB	700 MHz (7^{th} harmonics)

Notes:

a) The spectral peak reduction is not necessarily the same as the system EMI reduction. However, this relative measurement gives the component-level indication of SSC's EMI reduction capability at the system level.

b) It is recommended that a spectrum analyzer be used for this measurement. The spectrum analyzer should have measurement capability out to 1 GHz. The measured SSC clock needs to be fed into the spectrum analyzer via a high-impedance probe compatible with the spectrum analyzer. The output clock should be loaded with 20 pF capacitance. The resolution bandwidth of the spectrum analyzer needs to be set at 120 kHz to comply with FCC EMI measurement requirements. The video band needs to be set at higher than 300 kHz for appropriate display. 100 kHz may be used as the resolution bandwidth in case of measurement equipment limitation. The display should be set with maximum hold. The corresponding harmonic peak readings should be recorded in both the non-SSC and the SSC modes, and be compared to determine the magnitude of the spectral peak reduction.

8. The modulation frequency of SSC is required to be in the range of 30-33 kHz to avoid audio band demodulation and to minimize system timing skew. The downstream PLL tracking skew, i.e., the accumulative phase difference between the downstream PLL input and output clocks, is shown in Figure 14, as functions of modulation frequency, modulation profile, and spread amount. This plot is obtained through PLL behavior simulations assuming a jitter-free ideal modulated input clock to the PLL. The parameters of the simulated PLL are:

(VCO gain) * (charge-pump current) = 2800 (Hz/V)(A),
feedback divider =2, 2nd-order filter: C_1 = 11 pF; C2 = 356 pF; R = 9.75 kΩ.

9. This skew should be minimized as it reduces system timing margins. Different system implementations have different requirements and PLL characteristics, and may require tighter/looser skew. It is always true that lower modulation frequency results in smaller tracking skew. The skew is proportional to the amount of spreading. **Any implemented modulation profile must induce less than 110 pS skew with the above PLL parameters by properly adjusting its spread amount. Sinusoidal modulation is strongly not recommended due to its low peak reduction capability.**

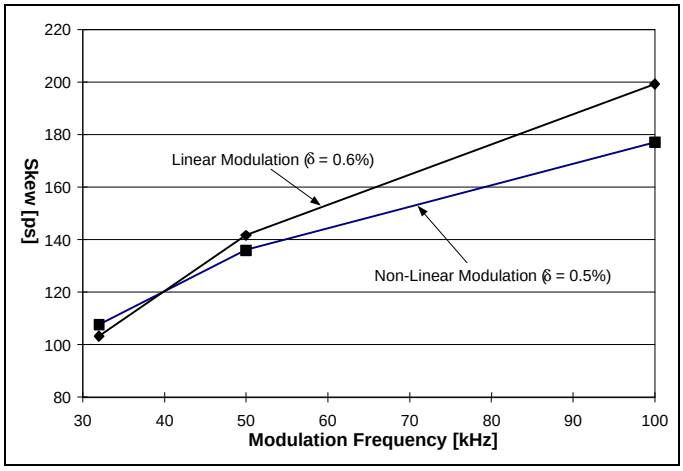


Figure 14 Downstream PLL tracking skew and modulation frequency

7.1.2 IOAPIC Clock Outputs Required To Be Synchronous With CPUCLK

The IOAPIC clocks, which were previously obtained by buffering the input reference crystal frequency, are now required to be synchronous with the CPUCLK outputs. The IOAPIC voltage will track that of the Host bus and will have a maximum frequency of 16.667MHz. The IOAPIC clocks will be derived by dividing the CPUCLK outputs by eight when the Host bus is 133.33MHz, and by six when the Host bus is 100MHz. The IOAPIC clocks will lag the Host bus clocks by 1.5-4.0 nS at the maximum device load (20pF.)

This functionality is to be defined to allow the clock driver to meet the previously optional "functional redundancy check (FRC) mode." However, it is believed that the synchronous IOAPIC clocks will help reduce the jitter variation seen across vendors by allowing a common decoupling scheme for IOAPIC noise.

Table 18 CK133 Select Functions

SEL133/100#	SEL1	SEL0	Function
0	0	0	All outputs Tri-State
0	0	1	(Reserved)
0	1	0	Active 100MHz, 48MHz PLL inactive
0	1	1	Active 100MHz, 48MHz PLL active
1	0	0	Test Mode
1	0	1	(Reserved)
1	1	0	Active 133MHz, 48MHz PLL inactive
1	1	1	Active 133MHz, 48MHz PLL active

Table 19 CK133 Truth Table

SEL 133/100#	SEL1	SEL0	CPU	CPU_div2	3V66	PCI	48MHz	REF	IOAPIC	Notes
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1
0	0	1	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
0	1	0	100 MHz	50 MHz	66 MHz	33 MHz	HI-Z	14.318 MHz	16.67 MHz	3
0	1	1	100 MHz	50 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	4, 7, 8
1	0	0	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	5, 6
1	0	1	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2
1	1	0	133 MHz	66 MHz	66 MHz	33 MHz	HI-Z	14.318 MHz	16.67 MHz	3
1	1	1	133 MHz	66 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	4, 7, 8

Notes:

1. Required for board level "bed of nails" testing.

2. Used to support Intel confidential application. Contact Intel representative for more details.
3. 48MHz PLL disabled to reduce component jitter. Vendor expected to tighten jitter spec in this mode to <200pS. 48 MHz outputs to be held HI-Z instead of driven to a LOW state.
4. "Normal" mode of operation
5. TCLK is a test clock over driven on the XTAL_IN input during test mode. TCLK mode is based on 133 MHz CPU select logic.
6. Required for DC output impedance verification
7. Range of reference frequency allowed is min = 14.316 nominal = 14.31818 MHz, max = 14.32 MHz.
8. Frequency accuracy of 48MHz must be +167PPM to match USB default. See Section 3.1.1 for details

7.1.2 Non-production Processor Frequencies For System Debug

Some system debug applications exist where processor frequencies that are above and below the specified 100, 133 MHz are of interest for this device. The ability to use this device in a lab environment using a 10 or 20 MHz crystal is desired. Another desired feature of this product is the ability to use a function generator (in lab environment only) to drive XTAL_IN (float XTAL_OUT) in test mode to create up to a 66 MHz CPU output.

7.1.3 CK133 System Considerations:

The SEL133/100# frequency select pin requires a specific motherboard pull-up resistor (preliminary = 220 Ohms) to 3.3V to allow the CK133 device to sense the maximum Host bus frequency of the processor to automatically configure the CK133 to either 133 or 100MHz.

No internal pull-up or pull-down resistors are allowed on the SEL100/133# pin.

7.1.4 CK133 Power Management

The following power-consumption conditions for the device should be tested/guaranteed by each vendor. The values below are estimates for the power specs.

Table 20 CK133 Maximum Allowed Current

CK133 Condition	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or Vss	Max 3.3V supply consumption Max discrete cap loads Vddq3 = 3.465V All static inputs = Vddq3 or Vss.
Power-down Mode (PWRDWN# = 0)	100 uA	200 uA
Full Active 100 MHz SEL133/100# = 0 SEL1, 0 = 11 CPUSTOP#, PCISTOP# = 1	75 mA	160 mA
Full Active 133 MHz SEL133/100# = 1 SEL1,0 = 11	90 mA	160 mA

CPUSTOP#, PCISTOP# = 1		

The power-down controller provides a signal that is latched with its own copy of the PCI clock. In theory, this should be synchronous with the clock driver output IF the following is quantified:

1. The flight time of the clock trace from PCI clock to the controller
2. Input edge-rate at the controller, input load at the controller, set/hold time at the controller.
3. Variance of output edge-rate from PCI of clock driver
4. Internal delay from output of PCI on clock driver to internal clock signal

However, the large number of platform level variables that must be taken into account for the input to be described as “synchronous” to the clock driver output is large and highly dependent on the board design. To simplify the platform design, the CPU_STOP# and the PCI_STOP# inputs are defined to be ASYNCHRONOUS from the clock driver external PCI clock. The clock driver must synchronize the input signal and resynchronize it with its own PCI clock output. This leaves the board timing issues up to the board designer rather than the clock vendor.

Clock sequencing must always guarantee full clock timing parameters at all times after the system has initially powered up except where noted. During power up and power down operations using the PWR_DWN# select pin, partial clocks are not allowed and all clock timing parameters must be met except for the following. It is understood that the first clock pulse coming out of a stopped clock condition could be slightly distorted due to clock network charging requirements. It is also understood that board routing and signal loading have a large impact on the initial clock distortion.

7.1.5 Vdd3v Power-down Removal: Required

There is a specific power-down procedure that will be used by some platform implementations of this device. The CK133 device is required to meet the following requirement to allow for a common design across multiple platforms.

To allow for multiple devices in platforms to share voltage regulators, the CK133 must be able to allow the removal of power from the Vdd3v voltage pins during the following specific condition. Leakage currents from the Vdd3v and Vdd25v pins are not allowed to violate existing powerdown# specifications.

Going into power-down mode:
1) Assert the PWRDWN# signal to the CK133.
2) Remove power from the 3.3V pins of the CK133.
3) All input pins of CK133 will be either powered down or driven to ground.
4) The Vdd3 power plane will be pulled to or discharge to <250 mV.
5) The 2.5V pins will remain powered at 2.5V.

Restore power:
1) Apply 3.3V to the CK133.
2) Wait 200 - 2000mSec
3) De-assert the PWRDWN# signal
4) Wait longer than lock time specified for device

5) Continue operation as normal

Table 21 CK133 Clock Enable Configuration

CPU_STOP#	PWR_DWN#	PCI_STOP#	CPUCLK	CPU_div2	APIC	3V66	PCI	PCI_F	REF, 48Mhz	Osc	VCOs
X	**0**	**X**	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
0	**1**	**0**	LOW	ON	ON	LOW	LOW	ON	ON	ON	ON
0	**1**	**1**	LOW	ON	ON	LOW	ON	ON	ON	ON	ON
1	**1**	**0**	ON	ON	ON	ON	LOW	ON	ON	ON	ON
1	**1**	**1**	ON	ON	ON	ON	ON	ON	ON	ON	ON

Notes:
1. LOW means outputs held static LOW as per latency requirement below.
2. ON means active.
3. PWR_DWN# pulled LOW, impacts all outputs including REF and 48 MHz outputs.
4. All 3V66 as well as all CPU clocks should stop cleanly when CPU_STOP# is pulled LOW.
5. CPU_div2, IOAPIC, REF, 48MHz signals are not controlled by the CPU_STOP# functionality and are enabled all in all conditions except PWR_DWN#=LOW.

Table 22 CK133 Power Management Requirements

Signal	Signal State	Latency
		No. of rising edges of PCICLK
CPU_STOP#	0 (disabled)	1
	1 (enabled)	1
PCI_STOP#	0 (disabled)	1
	1 (enabled)	1
PWR_DWN#	1 (normal operation)	3 mS
	0 (power down)	2 max.

Notes:
1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high) to when the first valid clocks are driven from the device.

CPU_STOP# is an input to the clock synthesizer. It is used to turn off the CPU and 3V66 clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock (and hence CPU clock) and must be internally synchronized to the external PCI_F output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. **ONLY one rising edge of PCI_F is allowed** after the clock control logic switched for both the CPU and 3V66 outputs to become enabled/disabled.

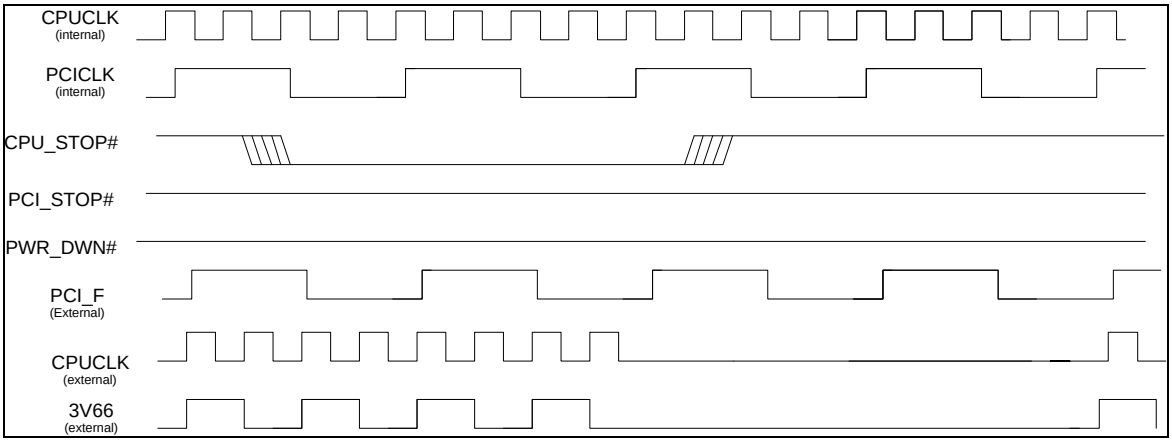


Figure 15 CK33 CPU_STOP# Timing Diagram

Notes:

1. All internal timing is referenced to the CPUCLK
2. The Internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. CPU_STOP# signal is an input signal that must be made synchronous to free running PCI_F
4. 3V66 clocks also stop/start before one rising edge of PCI_F when CPU_STOP# is asserted/deasserted.
5. PWR_DWN# and PCI_STOP# are shown in a high state.
6. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz

PCI_STOP# is an input to the clock synthesizer and must be made synchronous to the clock driver PCI_F output. It is used to turn off the PCI clocks for low power operation. PCI clocks are required to be stopped in a low state and started such that a full high pulse width is guaranteed. **ONLY one rising edge of PCI_F is allowed** after the clock control logic switched for the PCI outputs to become enabled/disabled.

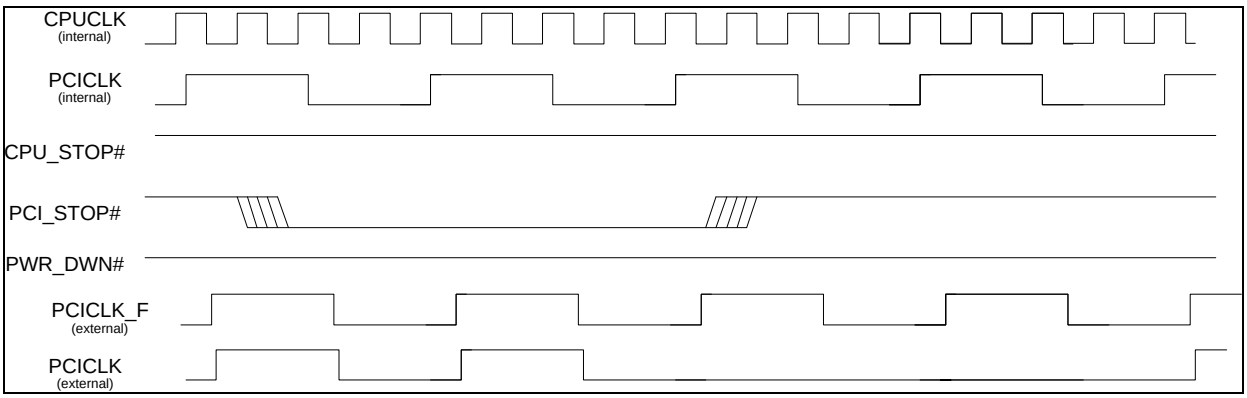


Figure 16 CK133 PCI_STOP# Timing Diagram

Notes:

1. All internal timing is referenced to the CPUCLK.
2. PCI_STOP# signal is an input signal which must be made synchronous to PCI_F output.
3. Internal means inside the chip.
4. All other clocks continue to run undisturbed.
5. PWR_DWN# and CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100 MHz

The power down selection is used to put the part into a very low power state without turning off the power to the part. PWR_DWN# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PWR_DWN# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PWR_DWN# is active low all clocks need to be driven to a low value and held prior to turning off the VCO's and the Crystal. The power -up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48Mhz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

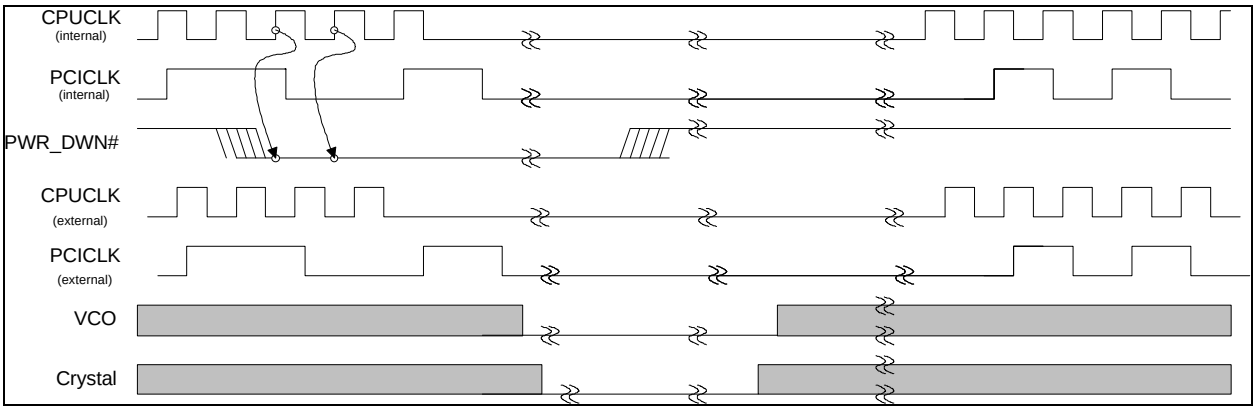
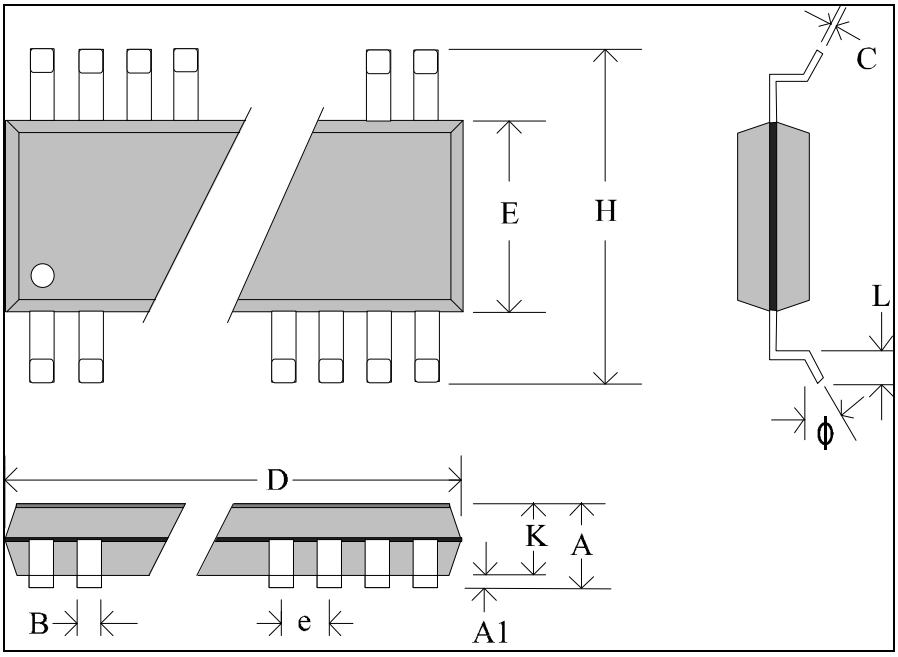


Figure 17 CK133 PWR_DWN# Timing Diagram

Notes:

1. All internal timing is referenced to the CPUCLK
2. Internal means inside the chip
3. PWR_DWN# is an asynchronous input and metastable conditions could exist. This signal is required to be synchronized inside the part.
4. The Shaded sections on the VCO and the Crystal signals indicate an active clock
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100 MHz

7.2 Appendix B: 56 Pin SSOP Package Data



56 SSOP: Table of Dimensions (inches, unless otherwise specified)

Body		Symbol										
		E	H	C	L	ϕ	D	K	A	A1	e	B
56	Min	0.291	0.395	0.009	0.020	0°	0.720	-	0.095	0.008	0.025	0.008
(300mil)	Max	0.299	0.420	0.013	0.040	8°	0.730	-	0.110	0.016		0.012

UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119
Tel: +1 408 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26
Tel: + 81-29847-8522

FRANCE, Intel Corporation S.A.R.L.
1, Quai de Grenelle, 75015 Paris
Tel: +33 1-45717171

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: +44 1-793-641440

GERMANY, Intel GmbH
Dornacher Strasse 1
85622 Feldkirchen/ Muenchen
Tel: +49 89/99143-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: +852 2844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario M9W 6H8
Tel: +416 675-2438

BRAZIL, Intel Semicondutores do Brasil
Centro Empresarial Nações Unidas - Edifício Torre Oeste
Av. das Nações Unidas, 12.901 - 18o. andar - Brooklin Novo
04578.000 São Paulo - S.P. – Brasil
Tel: +55-11-5505-2296