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Low Voltage Intel® Pentium® III Processor 512K and Ultra Low Voltage Intel® Celeron® Processor/815E Chipset Platform

Design Guide

November 2003

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Revision History

Date	Revision	Description
March 2002	001	First release of public document.
October 2002	002	Included updates for ULV Intel® Celeron® support
November 2003	003	Inserted new schematics
November 2003	004	Schematics updated

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Introduction 1

This design guide organizes Intel design recommendations for the Intel® 815E chipset platform for use with the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor. In addition to providing motherboard design recommendations (e.g., layout and routing guidelines), this document also addresses system design issues (e.g., thermal requirements) for the chipset platform.

This design guide contains design recommendations, debug recommendations, and a system checklist. These design guidelines are developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

Board designers should consult the debug recommendations when debugging their design. However, these debug recommendations should be understood before completing board design to ensure that the debug port, in addition to other debug features, are implemented correctly.

The Intel 815E chipset platform supports the following processors:

- Low Voltage Intel® Pentium® III processor 512K based on 0.13 micron technology (CPUID = 06Bxh).
- Ultra Low Voltage Intel® Celeron® processor based on 0.13 micron technology (CPUID = 06Bxh)

Note: The system bus speeds supported by the design are100/133 MHz only.

1.1 Terminology

This section describes some of the terms used in this document. Additional power delivery term definitions are provided at the beginning of Chapter 13, "Power Delivery."

Term	Description
AGP	Accelerated Graphics Port
AGTL	Refers to processor bus signals that are implemented using its lower voltage variant (AGTL).
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. Backward Crosstalk–coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. Forward Crosstalk–coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. Even Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. Odd Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Term	Description
GMCH	Graphics and Memory Controller Hub. A component of the Intel$^®$ 815E chipset platform for use with the Low Voltage/Intel$^®$ Pentium$^®$ III processor.
ICH	Intel$^®$ 82801AA I/O Controller Hub component.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network Length	The distance between agent 0 pins and the agent pins at the far end of the bus.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on a substrate such as the motherboard. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) Effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "push-out"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
System Bus	The system bus is the processor bus.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

1.2 Reference Documents

Document	Document Number / Location
Low Voltage Intel Pentium III Processor 512K Datasheet	273673
Ultra Low Voltage Intel® Celeron® Processor (0.13 μ) in the Micro FC-BGA Package Datasheet	*273804*
Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet	298351
Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet	290658
Intel® 82801BA I/O Controller Hub (ICH2) and Intel® 82801BAM I/O Controller Hub (ICH2-M) Datasheet	290687
Intel® Pentium® III Processor Specification Update	244453
AP 907 Intel® Pentium® III Processor Power Distribution Guidelines	*245085*
AP-585 Intel® Pentium® II Processor AGTL+ Guidelines	*243330*
AP-587 Intel® Pentium® II Processor Power Distribution Guidelines	*243332*
Accelerated Graphics Port Interface Specification, Revision 2.0	
Graphics Performance Accelerator Specification	ftp://download.intel.com/ technology/agp/ downloads/agp20.pdf
PCI Local Bus Specification, Revision 2.2	
AC'97 2.1 Specification	http:// developer.intel.com/pc- supp/platform/ac97/ index.htm.
82562EH HomePNA 1 Mb/s Physical Layer Interface Datasheet	Doc # 278313
82562EH HomePNA 1 Mb/s Physical Layer Interface Brief Datasheet	Doc # 278314
Communication Network Riser Specification, Revision 1.1	http:// developer.intel.com/ technology/cnr/
Universal Serial Bus, Revision 1.0 Specification	

1.3 System Overview

The Intel 815E chipset platform for use with the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor contain a Graphics and Memory Controller Hub (GMCH) component and I/O Controller Hub 2 (ICH2) component for applied computing platforms.

The GMCH provides the processor interface (for the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor), DRAM interface, hub interface, and an Accelerated Graphics Port (AGP) interface or internal graphics. This product provides flexibility and scalability in graphics and memory subsystem performance. Competitive internal graphics may be scaled via an AGP card interface, and PC133 system memory.

The Accelerated Hub Architecture interface (i.e., the chipset component interconnect) is designed into the chipset to provide an efficient, high-bandwidth communication channel between the GMCH and the I/O controller hub. The chipset architecture also enables a security and manageability infrastructure through the Firmware Hub component.

An ACPI-compliant Intel 815E chipset platform can support the *Full-on (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4),* and *Soft-off (S5)* power management states. The chipset also supports *wake-on-LAN*[*] for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software-configurable* AC'97 audio and modem coder/decoders (codecs), instead of the traditional ISA devices.

1.3.1 System Features

The Intel 815E chipset platform contains two components: the Intel® 82815 Graphics and Memory Controller Hub (GMCH) and the Intel® 82801BA I/O Controller Hub 2 (ICH2). The GMCH integrates a 66/100/133 MHz, P6 family system bus controller, integrated 2D/3D graphics accelerator or AGP (2X/4X) discrete graphics card, 100/133 MHz SDRAM controller, and a high-speed accelerated hub architecture interface for communication with the ICH2. The ICH2 integrates an UltraATA/100 controller, 2 Universal Serial Bus (USB) host controllers with a total of 4 ports, Low Pin Count (LPC) interface controller, Firmware Hub (FWH) interface controller, PCI interface controller, Intel® AC'97 digital link, integrated LAN controller, and a hub interface for communication with the GMCH.

Figure 1. System Block Diagram
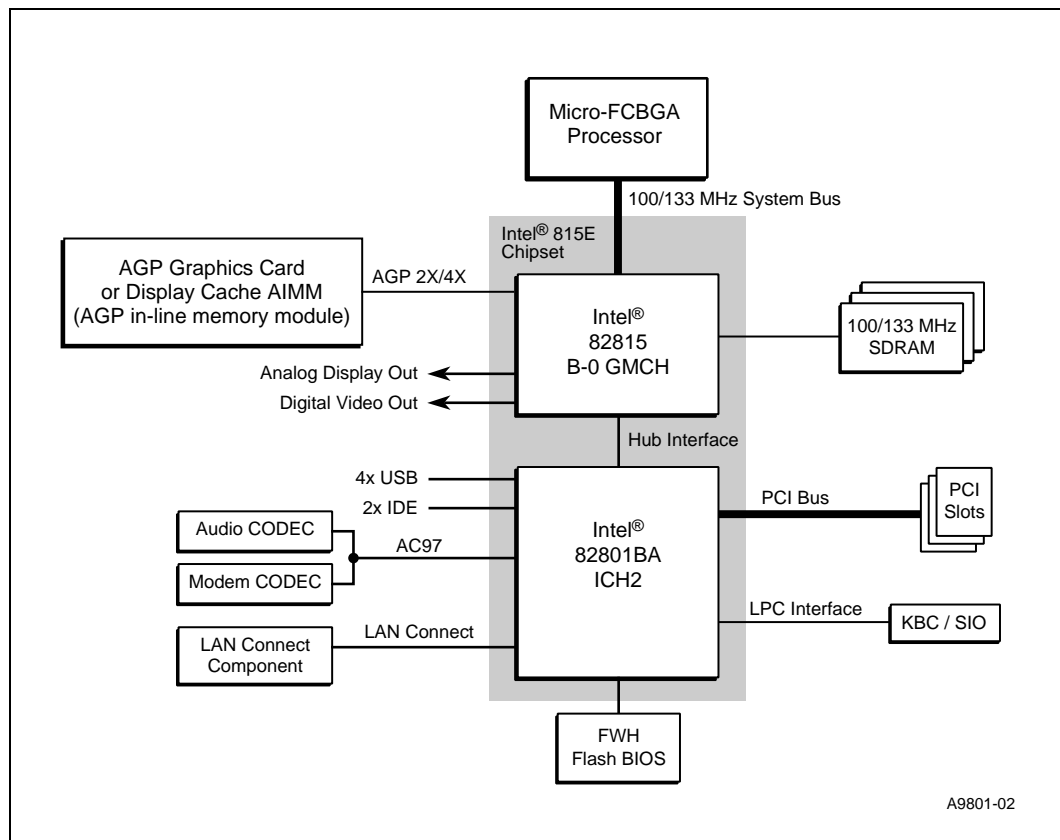
1.3.2 Component Features

Figure 2. Component Block Diagram
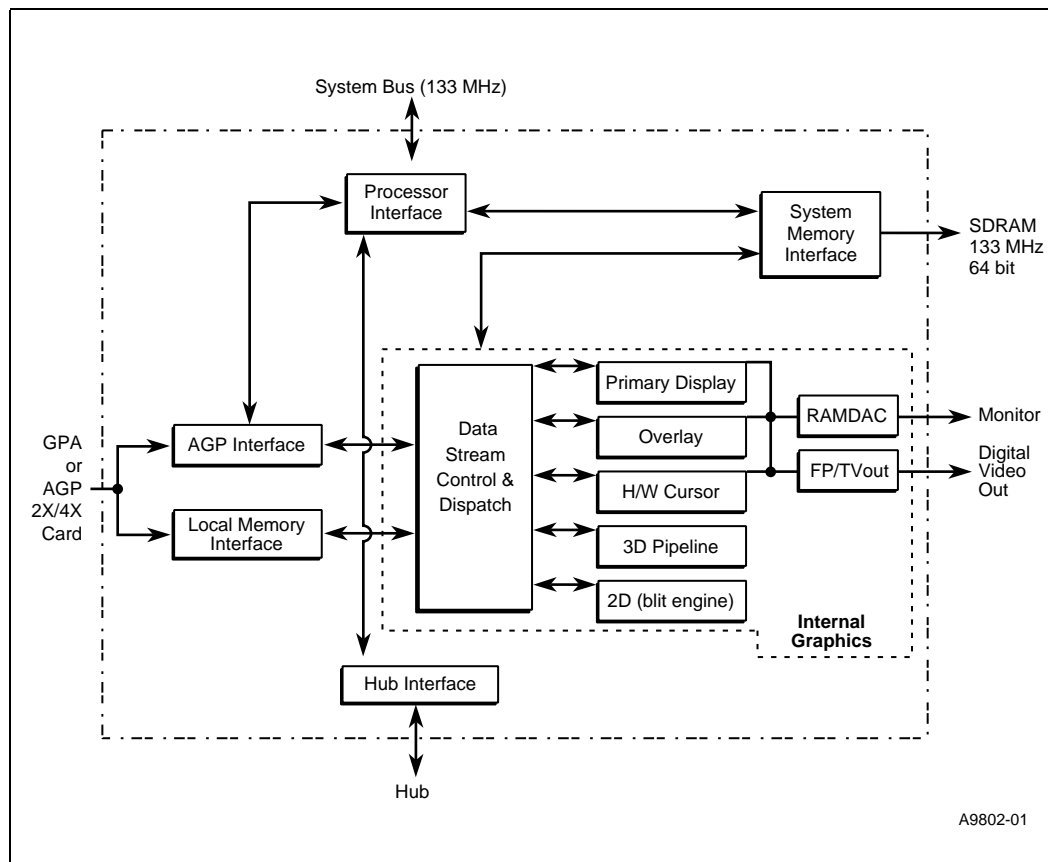
1.3.2.1 Intel® 82815 GMCH Features

- Processor/System Bus Support
  - Optimized for Intel® Pentium® III processors at 133 MHz system bus frequency
  - Support for Intel® Celeron™ processors (CPUID = 068xh) (66 MHz system bus)
  - Supports 32-bit AGTL bus addressing
  - Supports uniprocessor systems
  - Utilizes AGTL bus driver technology (gated AGTL receivers for reduced power)
- Integrated DRAM controller
  - 32 MB to 512 MB using 16Mbit/64Mbit/128 Mbit technology
  - Supports up to 3 double-sided DIMMS (6 rows)
  - 100 MHz, 133 MHz SDRAM interface
  - 64-bit data interface
  - Standard Synchronous DRAM (SDRAM) support (x-1-1-1 access)

- — Supports only 3.3 V DIMM DRAM configurations
- — No registered DIMM support
- — Support for symmetrical and asymmetrical DRAM addressing
- — Support for x8, x16 DRAM device widths
- — Refresh mechanism: CAS-before-RAS only
- — Support for DIMM serial PD (presence detect) scheme via SMbus interface
- — Suspend-To-RAM (STR) power management support via self-refresh mode using CKE
- Accelerated Graphics Port (AGP) Interface
  - — Supports AGP 2.0, including 4X AGP data transfers, but not the 2X/4X Fast Write protocol
  - — AGP universal connector support via dual-mode buffers to allow AGP 2.0 3.3 V or 1.5 V signaling
  - — 32-deep AGP request queue
  - — AGP address translation mechanism with integrated fully associative 20-entry TLB
  - — High-priority access support
  - — Delayed transaction support for AGP reads that can not be serviced immediately
  - — AGP semantic traffic to the DRAM not snooped on system bus and therefore not coherent with processor caches
- Integrated Graphics Controller
  - — Full 2D/3D/DirectX acceleration
  - — Texture-mapped 3D with point sampled, bilinear, trilinear, and anisotropic filtering
  - — Hardware setup with support for strips and fans
  - — Hardware motion compensation assist for software MPEG/DVD decode
  - — Digital Video Out interface for support of digital displays and TV-Out
  - — PC99A/PC2001 compliant
  - — Integrated 230 MHz DAC
- Integrated Local Graphics Memory Controller (Display Cache)
  - — 0 Mbytes to 4 Mbytes (via Graphics Performance Accelerator) using zero, one or two parts
  - — 32-bit data interface
  - — 133 MHz memory clock
  - — Supports ONLY 3.3 V SDRAMs
- Packaging/Power
  - — 544 BGA with local memory port
  - — 1.85 V core and mixed 3.3 V, 1.5 V, and AGTL+ I/O. Note that the 82801BA ICH2 has a 1.8 V requirement and the 82815 GMCH has a 1.85 V requirement. Instead of separate voltage regulators to meet these requirements, a single voltage regulator can be set to 1.795 V to 1.910 V. See

1.3.2.2 Intel® 82801BA I/O Controller Hub 2 (ICH2)

The Intel® I/O Controller Hub 2 allows the I/O subsystem to access the rest of the system, as follows:

- Upstream accelerated hub architecture interface for access to the GMCH
- PCI 2.2 interface (6 PCI Request/Grant pairs)
- Two channel Ultra ATA/100 Bus Master IDE controller
- USB controller (Expanded capabilities for four ports)
- I/O APIC
- SMBus controller
- FWH interface
- LPC interface
- AC'97 2.1 interface
- Integrated system management controller
- Alert-on-LAN*
- Integrated LAN controller
- Packaging/Power
  - 360 EBGA
  - 1.8 V (± 3% within margins of 1.795 V to 1.9 V) core and 3.3 V standby

1.3.2.3 Firmware Hub (FWH)

The hardware features of the firmware hub include:

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- Five General Purpose Interrupts (GPI)
- Packaging/Power
  - 40L TSOP and 32L PLCC
  - 3.3 V core and 3.3 V/12 V for fast programming

1.3.3 Platform Initiatives

1.3.3.1 Intel® PC 133

The Intel® PC133 initiative provides the memory bandwidth necessary to obtain high performance from the processor and AGP graphics controller. The platform's SDRAM interface supports 100 MHz and 133 MHz operation. The latter delivers 1.066 GB/s of theoretical memory bandwidth compared with the 800 Mbytes/s theoretical memory bandwidth of 100 MHz SDRAM systems.

The Low Voltage Intel® Pentium® III processor 512K only supports a 133 MHZ PSB.

1.3.3.2 Accelerated Hub Architecture Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge becomes significant. With the addition of AC'97 and Ultra ATA/100, coupled with the existing USB, I/O requirements could impact PCI bus performance. The Intel 815E platform's *accelerated hub architecture* ensures that the I/O subsystem, both PCI and the integrated I/O features (IDE, AC'97, USB, LAN), receives adequate bandwidth. By placing the I/O bridge on the accelerated hub architecture interface instead of PCI, I/O functions integrated into the ICH2 and the PCI peripherals are ensured the bandwidth necessary for peak performance.

1.3.3.3 Internet Streaming SIMD Extensions

The Pentium III processors provide 70 new SIMD (single instruction, multiple data) instructions. The new extensions are floating-point SIMD extensions. Intel® MMX™ technology provides integer SIMD instructions. The Internet Streaming SIMD extensions complement the MMX technology SIMD instructions and provide a performance boost to floating-point-intensive 3D applications.

1.3.3.4 AGP 2.0

The AGP 2.0 interface allows graphics controllers to access main memory at over 1 GB/s, twice the bandwidth of previous AGP platforms. AGP 2.0 provides the infrastructure necessary for *photorealistic 3D.* In conjunction with the Internet Streaming SIMD extensions, AGP 2.0 delivers the next level of 3D graphics performance.

1.3.3.5 Integrated LAN Controller

The Intel 815E chipset platform incorporates an ICH2 integrated LAN Controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of LAN connect components to target the desired market segment. The Intel® 82562EH provides a HomePNA 1 Mbit/sec connection. The Intel® 82562ET provides a basic Ethernet 10/100 connection. The Intel® 82562EM provides an Ethernet 10/100 connection with the added flexibility of Alert on LAN. More advanced LAN solutions can be implemented with the Intel® 82550 or other PCI based product offerings.

1.3.3.6　Ultra ATA/100 Support

The Intel 815E chipset platform incorporates an IDE controller with two sets of interface signals (primary and secondary) that can be independently enabled, tri-stated or driven low. The component supports Ultra ATA/100, Ultra ATA/66, Ultra ATA/33, and multiword PIO modes for transfers up to 100 MB/sec.

1.3.3.7　Expanded USB Support

The Intel 815E chipset platform contains two USB Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of four USB ports. The addition of a second USB Host Controller expands the functionality of the platform.

1.3.3.8　Manageability and Other Enhancements

The Intel 815E chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups, without the aid of an external microcontroller.

SMBus

The ICH2 integrates an SMBus controller. The SMBus provides an interface for managing peripherals such as serial presence detection (SPD) and thermal sensors. The slave interface allows an external microcontroller to access system resources.

Interrupt Controller

The interrupt capabilities of the platform expand support for up to eight PCI interrupt pins and PCI 2.2 message-based interrupts. In addition, the ICH2 supports system bus interrupt delivery.

Firmware Hub (FWH)

The platform supports firmware hub BIOS memory sizes up to 8 MB for increased system flexibility.

1.3.3.9　AC'97 6-Channel Support

The *Audio Codec '97* (AC'97) Specification defines a digital interface that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and an MC. The AC'97 Specification defines the interface between the system logic and the audio or modem codec known as the *AC'97 Digital Link*.

The Intel 815E chipset platform's AC'97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC'97 digital link. Using the platform's integrated AC'97 digital link reduces cost and eases migration from ISA.

By using an audio codec, the AC'97 digital link allows for cost-effective, high-quality, integrated audio. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC'97. The Intel 815E chipset platform's integrated digital link allows several external codecs to be connected to the ICH2. The system

designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (Figure 3c). The digital link is expanded to support two audio codecs (Figure 3a) or a combination of an audio and modem codec (Figure 3b).

Modem implementation for different countries must be taken into consideration, as telephone systems may vary. By implementing a split design, the audio codec can be on board, and the modem codec can be placed on a riser. Intel is developing an AC'97 digital link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the ICH2 is AC'97 Rev. 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high-quality, two-speaker audio solution. Wake-on-ring-from-suspend also is supported with the appropriate modem codec.

The Intel 815E chipset platform expands audio capability with support for up to six channels of PCM audio output (i.e., full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer, for a complete surround sound effect. ICH2 has expanded support for two audio codecs on the AC'97 digital link.

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Figure 3. AC'97 Audio and Modem Connections

a) AC'97 with Audio Codecs (4-Channel Secondary)

ICH2 360 EBGA — AC'97 Digital Link — AC'97 Audio Codec → Audio Port

AC'97 Audio Codec → Audio Port

b) AC'97 with Modem and Audio Codecs

Modem Port

ICH2 360 EBGA — AC'97 Digital Link — AC'97 Modem Codec → Modem Port

AC'97 Audio Codec → Audio Port

c) AC'97 with Audio/Modem Codec

Modem Port

ICH2 360 EBGA — AC'97 Digital Link — AC'97 Audio/ Modem Codec → Modem Port / Audio Port

AC97_connections

1.3.3.10   Low-Pin-Count (LPC) Interface

In the Intel 815E chipset platform, the Super I/O (SIO) component has migrated to the Low-Pin-Count (LPC) interface. Migration to the LPC interface allows for lower-cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The 15-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of the devices offered and the features supported.

In addition, depending on system requirements, specific system I/O requirements may be integrated into the LPC Super I/O. For example, a USB hub may be integrated to connect to the ICH2 USB output and extend it to multiple USB connectors. Other SIO integration targets include a device bay controller or an ISA-IRQ-to-serial-IRQ converter to support a PCI-to-ISA bridge. Contact your Super I/O vendor to ensure the availability of desired LPC Super I/O features.

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General Design Considerations 2

This design guide provides motherboard layout and routing guidelines for systems based on the Intel 815E chipset for use with the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor. The document does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations be completed for each design. Even when the guidelines are followed, critical signals should be simulated to ensure the proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely. Any deviation from these guidelines should be simulated.

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the "nominal" trace impedance for a 5 mil-wide trace. That is, it is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace, based on the switching of neighboring traces. The use of wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section.

The routing guidelines in this design guide have been created using a PCB *stack-up* similar to that shown in Figure 4. If this stack-up is **not** used, extremely thorough simulations of every interface must be completed.

2.1   Nominal Board Stack-up

The Intel 815E chipset platform requires a board stack-up yielding a target impedance of 60 Ω ± 15% with a 5 mil nominal trace width. Figure 4 shows an example stack-up that achieves this. It is a six-layer printed circuit board (PCB) construction using 53%-resin FR4 material.

Figure 4. Board Construction Example for 60 Ω Nominal Stack-up


```
        ┌──────────────────────────┐     ▲
        │  Component-side Layer Cu. │     │
        └──────────────────────────┘     │
                  prepreg                 │
        ┌──────────────────────────┐     │
        │   Power Plane Layer Cu.   │     │
        └──────────────────────────┘     │
                  prepreg            Total thickness:
        ┌──────────────────────────┐     62 mils
        │     Signal Layer Cu.      │     │
        └──────────────────────────┘     │
                  prepreg                 │
        ┌──────────────────────────┐     │
        │     Signal Layer Cu.      │     │
        └──────────────────────────┘     │
                  prepreg                 │
        ┌──────────────────────────┐     │
        │     Ground Layer Cu.      │     │
        └──────────────────────────┘     │
                  prepreg                 │
        ┌──────────────────────────┐     ▼
        │   Solder-side Layer Cu.   │
        └──────────────────────────┘
```

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![intel® logo]

Component Layouts   3
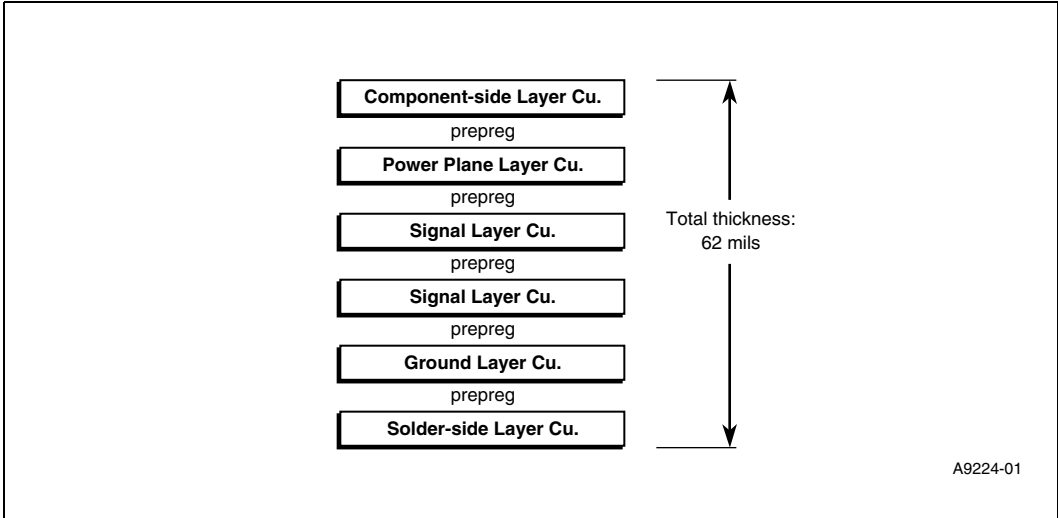
Figure 5 illustrates the relative signal quadrant locations on the GMCH ballout. It does not represent the actual ballout. Refer to the *Intel® 82815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet* for the actual ballout.

Figure 5. GMCH 544-Ball mBGA CSP Quadrant Layout (Top View)
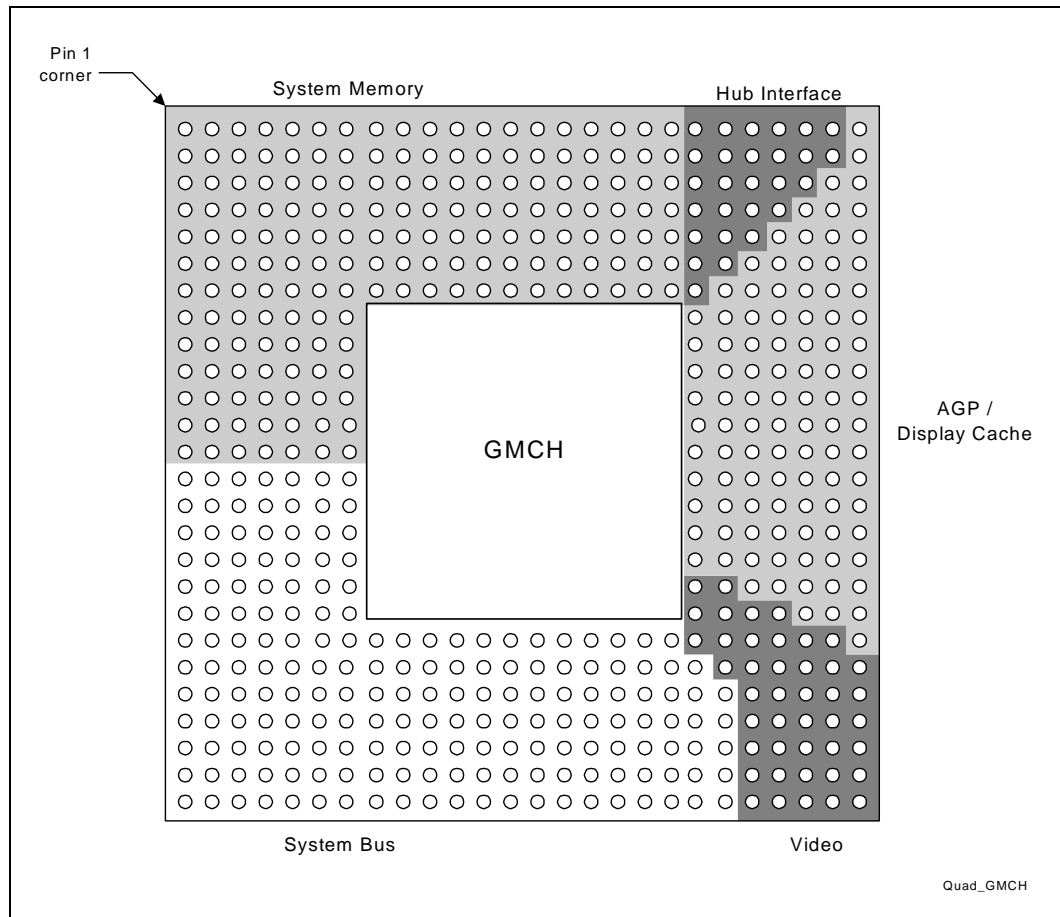
Figure 6 illustrates the relative signal quadrant locations on the ICH2 ballout. It does not represent the actual ballout. Refer to the *Intel® 82801BA I/O Controller Hub (ICH2) and Intel® 82801BAM I/O Controller Hub (ICH2-M) Datasheet* for the actual ballout.

Figure 6. ICH2 360-Ball EBGA Quadrant Layout (Top View)
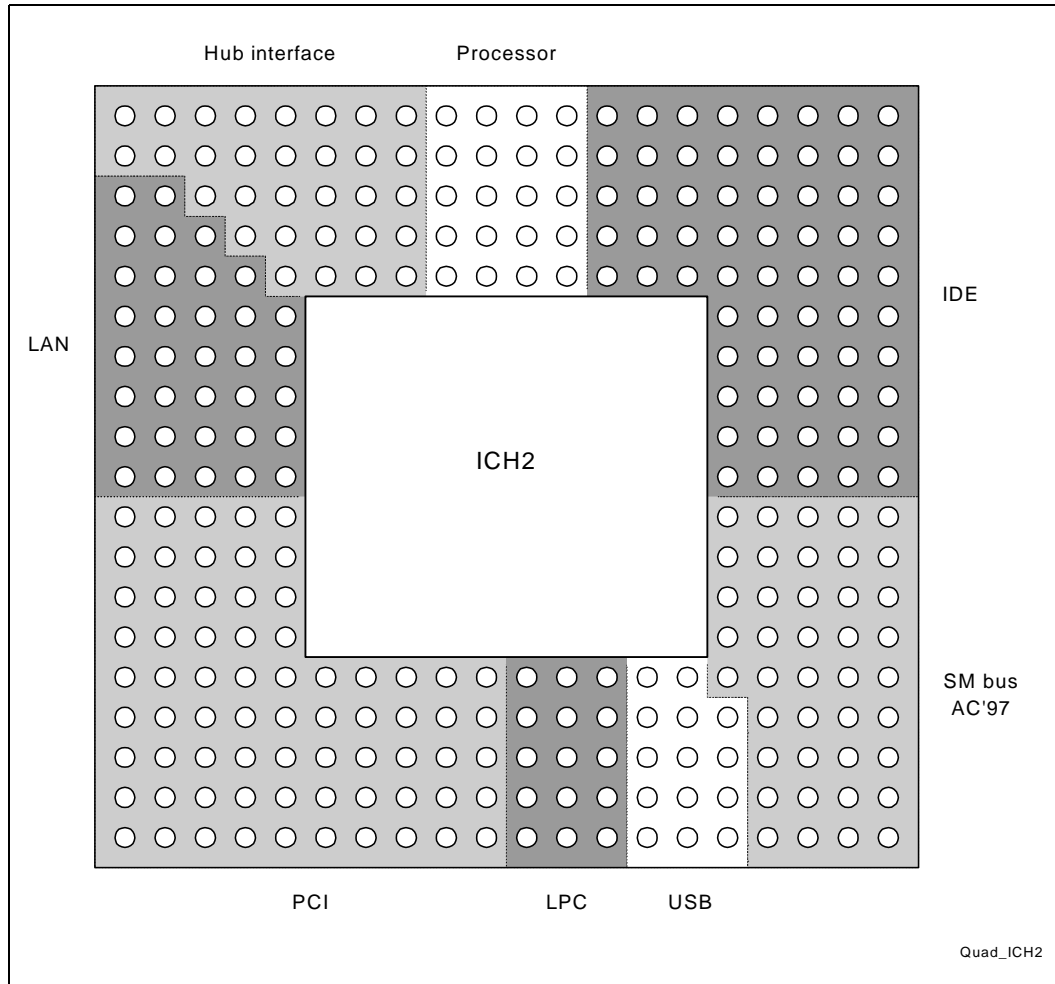
Figure 7. Firmware Hub (FWH) Packages

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Processor Design Considerations   **4**
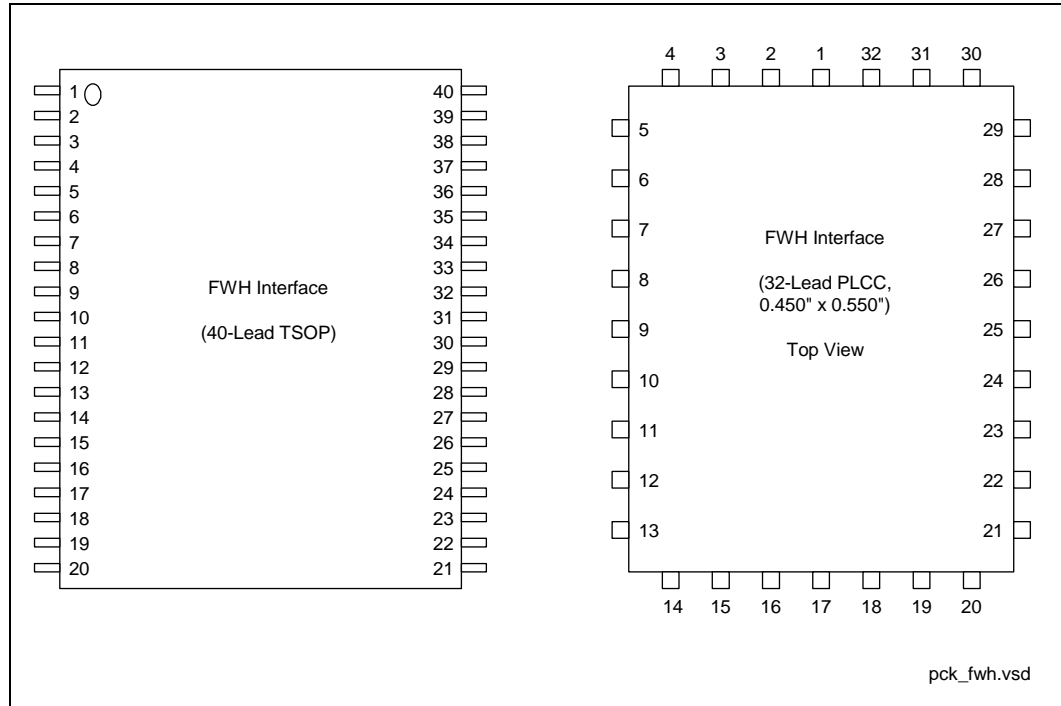
4.1   Configuring Non-V$_{TT}$ Processor Pins

When asserted, the VTT_PWGRD signal must be level-shifted to 12 V to properly drive the gating circuitry of the Intel® CK-815. Furthermore, while the VTT-PWRGD signal is connected to the VTT_PWRGD pin on a Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor. To provide proper functionality, a 1.0 kΩ resistor must be placed in series between the circuitry that generates the signal VTT_PWRGD and the processor pin VTT_PWRGD. Refer to Figure 8 for an example implementation. Voltage regulators that generate the standard VTT_PWRGD signal are available.

Figure 8. VTT-PWRGD Configuration Circuit
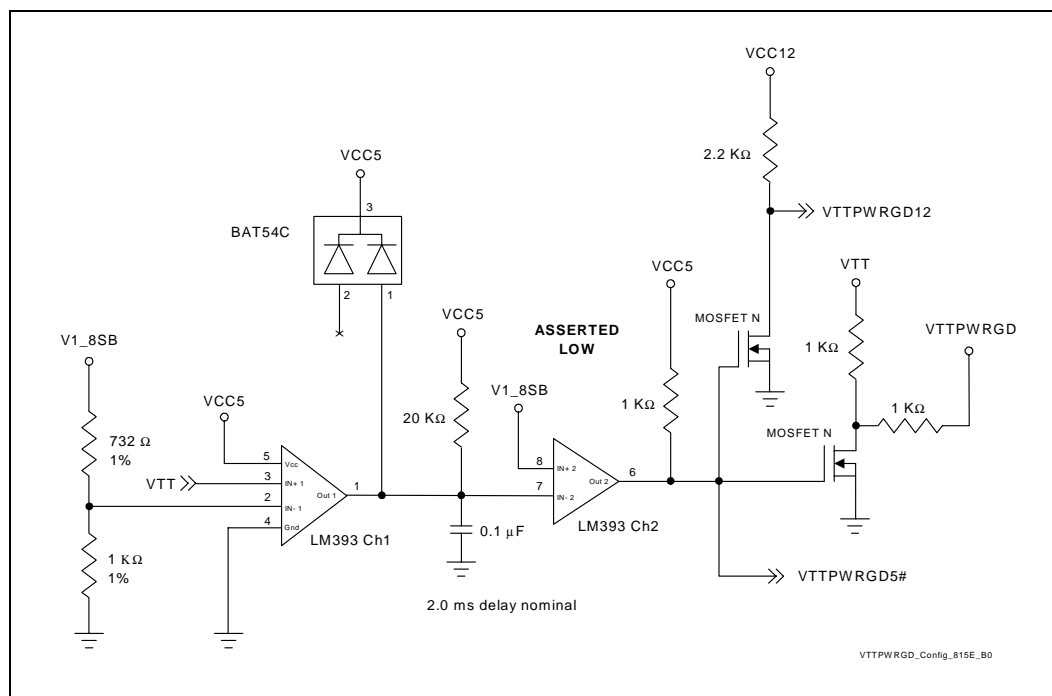
NOTE: The diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20 ms delay.

4.2   VCMOS Reference

In previous platforms supporting the Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh), VCMOS was generated by the same power plane as V$_{TT}$. The Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor do not generate VCMOS, and the platform is required to generate this separately on the motherboard. The GTL_REF pin on a Pentium® III processor (CPUID=068xh) and Celeron® processor

(CPUID=068xh), has been changed to a VCMOS_REF pin on the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor. Referring to Figure 9, a network of resistors and a capacitor must be added so that this pin operates appropriately.

Figure 9. GTL_REF/VCMOS_REF Voltage Divider Network

A9805-01
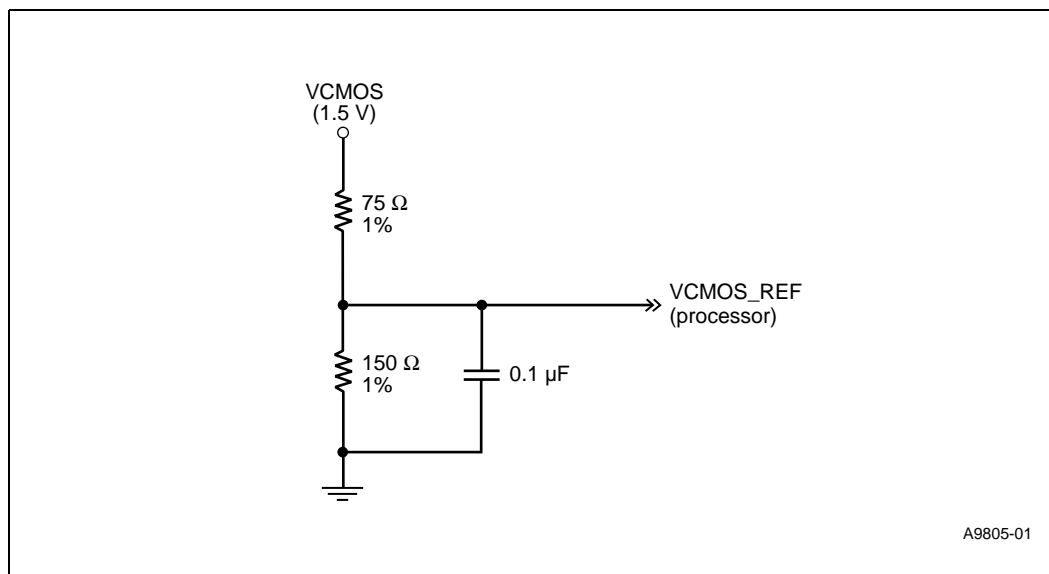
4.3 Processor Signal PWRGOOD

The processor signal PWRGOOD is specified at 1.8 V for the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor. See Figure 10 for an example implementation, or pull up to 1.8 VSB through 1.5 K Ω, 1 percent resistor.

Figure 10. Resistor Divider Network for Processor PWRGOOD
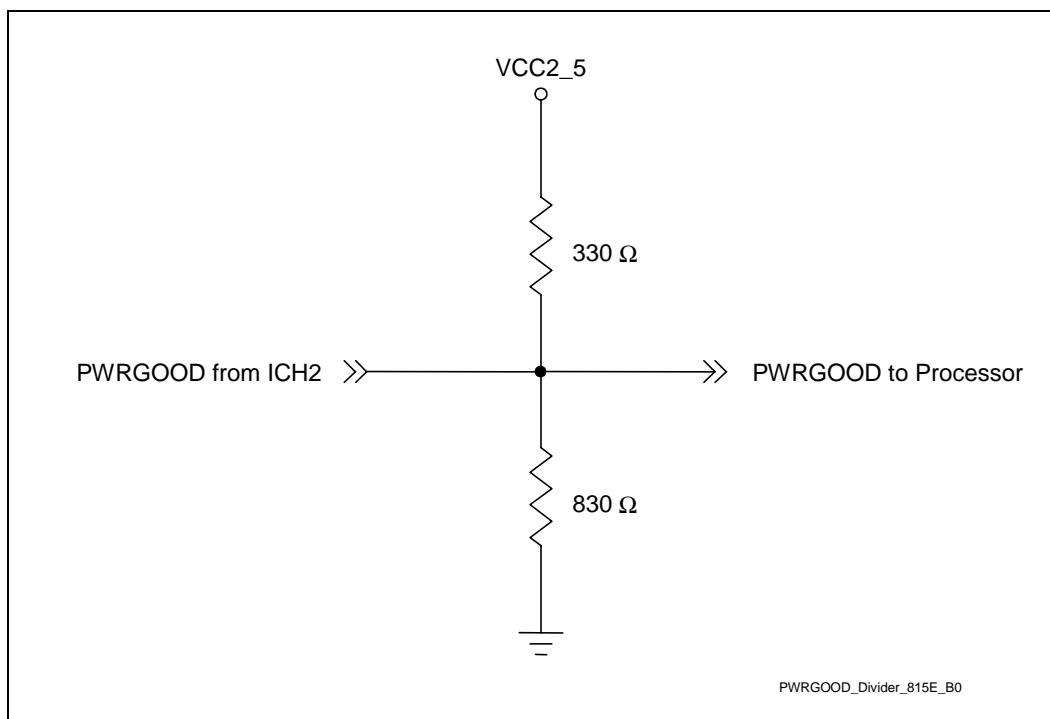
4.4   APIC Clock Voltage Switching Requirements

The processor's APIC clock is specified at 2.0 V, so a voltage divider is required to ensure proper operation. Figure 11 shows an example implementation.

Figure 11. Voltage Divider for Processor APIC Clock
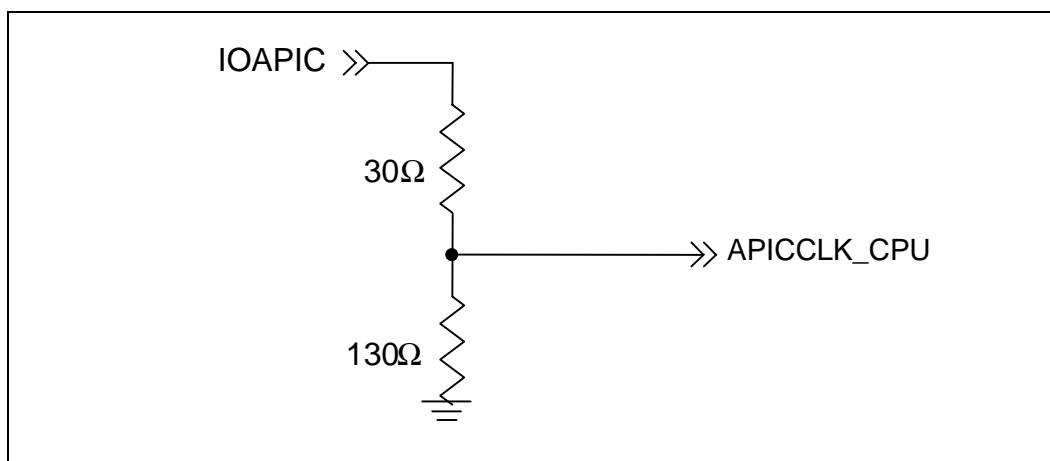
NOTE: The 30 Ω resistor represents the series resistor typically used in connecting the APIC clock to the processor.

4.5 GTLREF Topology and Layout

The GTLREF on the processor is specified to be 2/3 x V_{TT}, while the GTLREF on the chipset is 0.7 * V_{TT}. This difference requires that separate resistor sites be added to the layout to split the GTLREF sources. The recommended GTLREF circuit topology is shown in Figure 12.

Note: If an A-2 stepping of the GMCH is used with the design, the GTLREF for the GMCH should be set at 2/3 x V_{TT}. This requires changing the 63.4 Ω, 1% resistor on the GMCH side to 75 Ω, 1%.

Figure 12. GTLREF Circuit Topology
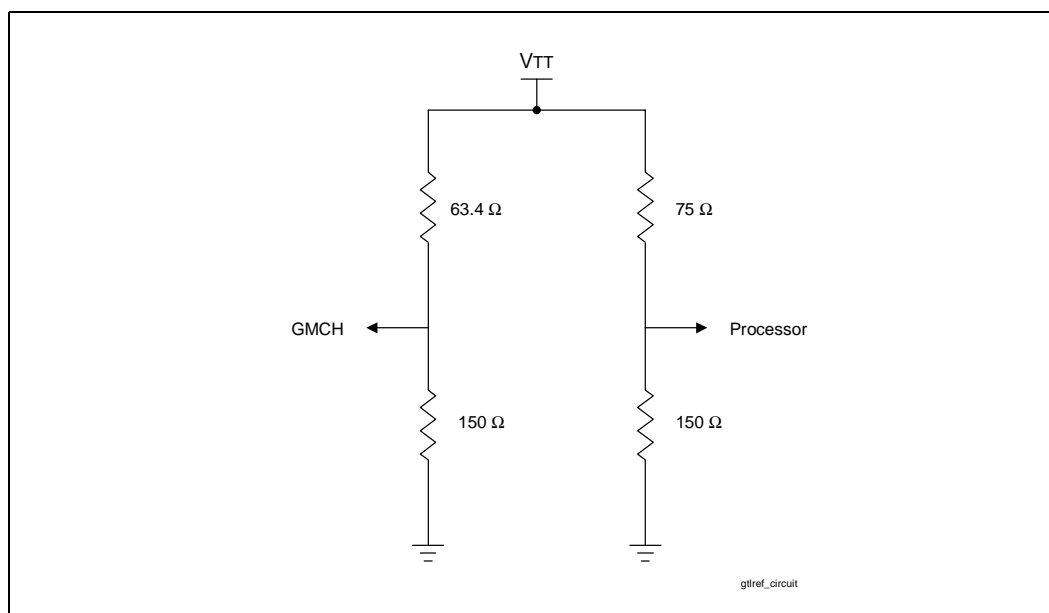
GTLREF Layout and Routing Guidelines

- Place all resistor sites for GTLREF generation close to the GMCH.

- Route GTLREF with as wide a trace as possible.

- Use one 0.1 μF decoupling capacitor for every two GTLREF balls at the processor (four capacitors total). Place as close as possible (within 500 mils) to the processor REF balls.

- Use one 0.1 μF decoupling capacitor for each of the two GTLREF balls at the GMCH (two capacitors total). Place as close as possible to the GMCH GTLREF balls.

Given the higher GTLREF level for the GMCH, a debug test hook should be added for validation purposes. The debug test hook should be placed on the processor signal ADS# and consists of laying down the site for a 56 Ω pull-up to V_{TT}. The resistor site should be located within 150 mils of the GMCH, and placed as close to the ADS# signal trace as possible.

4.6 Power Sequencing on Wake Events

Special handling of wake events is required for the Intel 815 chipset platform. When a wake event is triggered, the GMCH and the Intel CK-815 must not sample BSEL[1:0] until the signal VTT-PWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the Intel CK-815-compliant clock driver until VTT-PWRGD12 is asserted.

2. Clocks to the ICH2 stabilize before the power supply asserts PWROK to the ICH2. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus it is necessary to gate PWROK to the ICH2 from the power supply while the Intel CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.

3. ICH2 takes the GMCH out of reset.

4. GMCH samples BSEL[1:0]. Intel CK-815 will have sampled BSEL[1:0] much earlier.

4.6.1 Gating of Intel® CK-815 to VTT_PWRGD

System designers must ensure that the VTT_PWRGD signal is asserted before the Intel CK-815-compliant clock driver receives power. This is handled by having the 3.3 V rail of the clock driver gated by the VTT_PWRGD12 reference schematic signal. Unlike previous Intel 815E chipset designs, the 3.3 V standby rail is not used to power the clock because the VTT_PWRGD12 reference schematic signal will cut power to the clock when going into any sleep state. Refer to Figure 13 for an example implementation.

Figure 13. Gating Power to Intel® CK-815
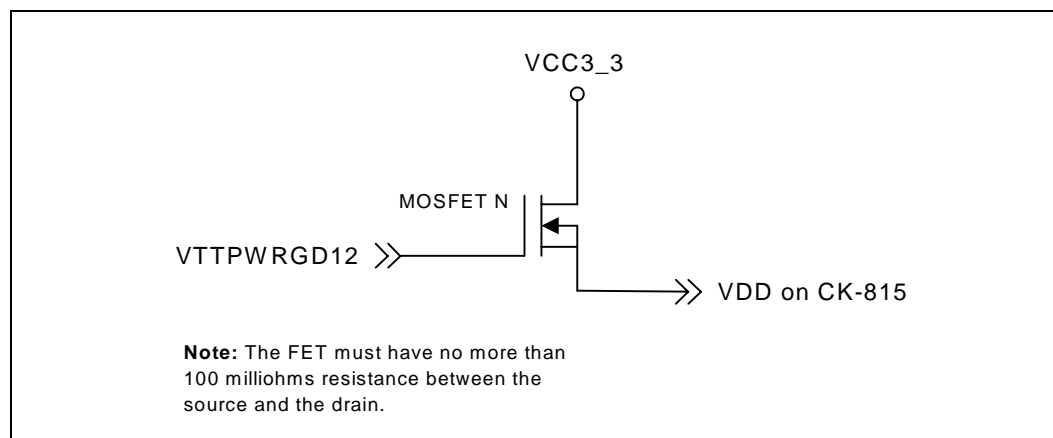
4.6.2 Gating of PWROK to ICH2

With power being gated to the Intel CK-815 by the signal VTT-PWRGD12, it is important that the clocks to the ICH2 are stable before the power supply asserts PWROK to the ICH2. As the clocking power gating circuitry relies on the 12 V supply, there is no guarantee that these conditions will be met. This is why an estimated minimum time delay of 20 ms must be added after power is connected to the Intel CK-815 to give the clock driver sufficient time to stabilize. This time delay will gate the power supply's assertion of PWROK to the ICH2. After the time delay, the power supply can safely assert PWROK to the ICH2, with the ICH2 subsequently taking the GMCH out of reset. Refer to Figure 14 for an example implementation.

Figure 14. PWROK Gating Circuit For ICH2
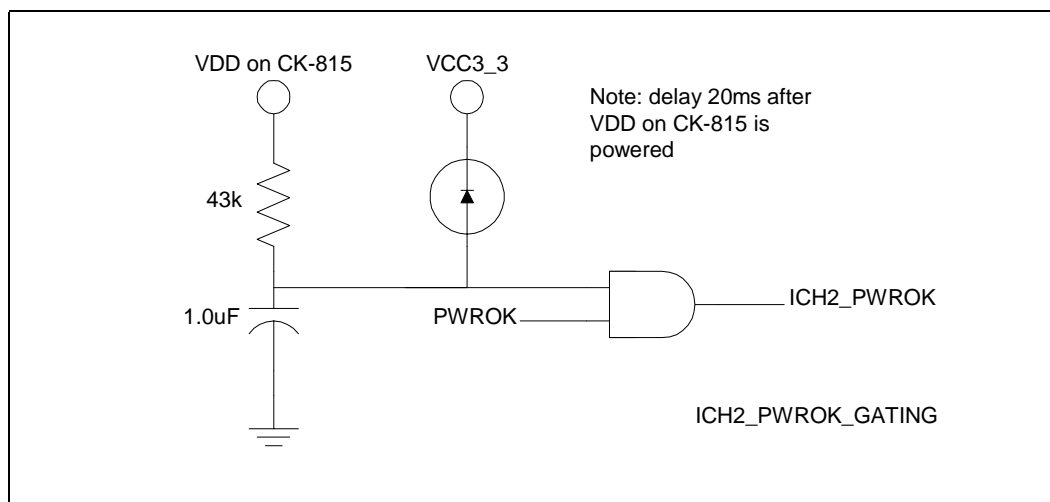
Note: The diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20 ms delay.

System Bus Design Guidelines **5**

The Pentium® III processor delivers higher performance by integrating the Level 2 cache into the processor and running it at the processor's core speed. The Pentium III processor runs at higher core and system bus speeds than previous-generation IA-32 processors while maintaining hardware and software compatibility with earlier Pentium III processors.

5.1 System Bus Routing Guidelines

The following layout guide supports designs using the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor with the Intel 815E chipset platform. The solution covers system bus speeds of 100/133 MHz only. The processor must also be configured to 56 Ω on-die termination.

5.1.1 Initial Timing Analysis

Table 1 lists the AGTL component timings of the processors and Intel 815E platform's GMCH defined at the pins.

Note: These timings are for reference only. Obtain the processor's specifications from the respective processor datasheet and the chipset values from the appropriate Intel 815 chipset datasheet.

Table 1. Intel® Pentium® III Processor AGTL Parameters for Example Calculations

IC Parameters	Intel® Pentium® III Processor at 133 MHz System Bus	GMCH	Notes
Clock to Output maximum (T_{CO-MAX})	3.25 ns (for 100/133 MHz system bus speeds)	**4.1 ns**	**1, 2**
Clock to Output minimum (T_{CO-MIN})	0.40 ns (for 100/133 MHz system bus)	**1.05 ns**	**1, 2**
Setup time (T_{SU-MIN})	1.20 ns for BREQ Lines 0.95 ns for all other AGTL Lines @ 133 MHz 1.20 ns for all other AGTL lines @ 100 MHz	**2.65 ns**	**1, 2,3**
Hold time (T_{HOLD})	1.0 ns (for 100/133 MHz system bus speeds)	**0.10 ns**	**1**

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only**. These timing parameters are subject to change. Check the appropriate component documentation for the valid timing parameter values.
3. T_{SU-MIN} = 2.65 ns assumes that the GMCH sees a minimum edge rate equal to 0.3 V/ns.

Table 2 contains an example AGTL initial maximum flight time, and Table 3 contains an example minimum flight time calculation for a 133 MHz, uniprocessor system using the Low Voltage Intel® Pentium® III processor 512K and the Intel 815E chipset platform's system bus. Note that assumed values were used for the clock skew and clock jitter.

Note: The clock skew and clock jitter values depend on the clock components and the distribution method chosen for a particular design, and must be budgeted into the initial timing equations as appropriate for each design.

Table 2 and Table 3 were derived assuming the following:

- CLK_{SKEW} = 0.20 ns (Note: This assumes that the clock driver pin-to-pin skew is reduced to 50 ps by tying the two host clock outputs together (i.e., "ganging") at the clock driver output pins, and that the PCB clock routing skew is 150 ps. The system timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together as well as the use of a clock driver that meets the Intel CK-815 Clock Synthesizer/Driver Specification.)

- CLK_{JITTER} = 0.250 ns

See the respective processor datasheet and the appropriate Intel 815 chipset platform documentation for details on clock skew and jitter specifications. Exact details regarding the host clock routing topology are provided with the platform design guideline.

Table 2. Example T_{FLT_MAX} Calculations for 133 MHz Bus

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}
Processor	GMCH	7.50	3.25	2.65	0.20	0.25	0.40	1.1
GMCH	Processor	7.50	4.1	.95	0.20	0.25	0.40	1.2

NOTES:
1. All times in nanoseconds
2. BCLK period = 7.50 ns @ 133.33 MHz

Table 3. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	THOLD	ClkSKEW	TCO_MIN	Recommended TFLT_MIN
Processor	GMCH	0.10	0.20	0.40	0.10
GMCH	Processor	1.00	0.20	1.05	0.15

NOTE: All times in nanoseconds

The flight times in Table 2 include margin to account for the following phenomena that Intel observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect the flight time and signal quality and sometimes are not accounted for during simulation. Accordingly, the maximum flight times depend on the baseboard design, and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in

- Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay

- Crosstalk on the PCB and inside the package which can cause variation in the signals

Additional effects exist that may not necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. These effects are included as M_{ADJ} in the example calculations in Table 7. Examples include:

- The effective board propagation constant (S_{EFF}), which is a function of:

— Dielectric constant (ε_r) of the PCB material

— Type of trace connecting the components (stripline or microstrip)

— Length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a component of the flight time, but not necessarily equal to the flight time.

5.2 General Topology and Layout Guidelines

Figure 15. Topology for Designs with Single-Ended Termination (SET)
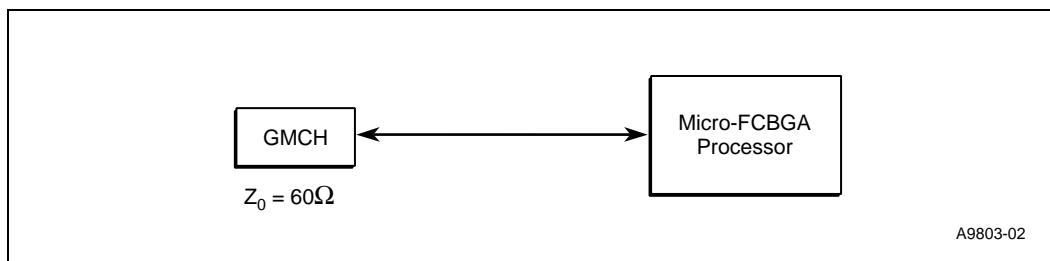
Table 4. Trace Guidelines for Figure 15

Description	Min. Length (inches)	Max. Length (inches)
GMCH to processor trace	2	4

NOTES:
1. All AGTL bus signals should be referenced to the ground plane for the entire route.
2. Use an intragroup AGTL spacing: line width: dielectric thickness ratio of at least 2:1:1 for microstrip geometry. If ε_r = 4.5, this should limit coupling to 3.4%. For example, intragroup AGTL routing could use 10 mil spacing, 5 mil traces, and a 5 mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
3. The recommended trace width is 5 mils, but not greater than 6 mils.

Table 5 contains the trace width: space ratios assumed for this topology. Three types of crosstalk are considered in this guideline: Intragroup AGTL, Intergroup AGTL, and AGTL to non-AGTL. Intragroup AGTL crosstalk involves interference between AGTL signals within the same group. Intergroup AGTL crosstalk involves interference from AGTL signals in a particular group to AGTL signals in a different group. An example of AGTL to non-AGTL crosstalk is when CMOS and AGTL signals interfere with each other. The AGTL signals consist of the following groups: data signals, control signals, clock signals, and address signals.

Table 5. Trace Width:Space Guidelines

Crosstalk Type	Trace Width:Space Ratios[1, 2]
Intragroup AGTL signals (same group AGTL)	5:10 or 6:12
Intergroup AGTL signals (different group AGTL)	5:15 or 6:18
AGTL to System Memory Signals	5:30 or 6:36
AGTL to non-AGTL	5:25 or 6:30

NOTES:
1. Edge-to-edge spacing.
2. Units are in mils.

5.2.1 Motherboard Layout Rules for AGTL Signals

Ground Reference

It is strongly recommended that AGTL signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide an effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane. If a signal has to go through routing layers, the recommendations are:

Note: Following these layout rules is critical for AGTL signal integrity, for the 0.13 micron process technology.

- For signals going from a ground reference to a power reference, add capacitors between ground and power near the vias to provide an AC return path. One capacitor should be used for every three signal lines that change reference layers. Capacitor requirements are as follows: C=100 nF, ESR=80 mΩ, ESL=0.6 nH. Refer to Figure 16 for an example of switching reference layers.

- For signals going from one ground reference to another, separate ground reference, add vias between the two ground planes to provide a better return path.

Figure 16. AGTL Trace Routing
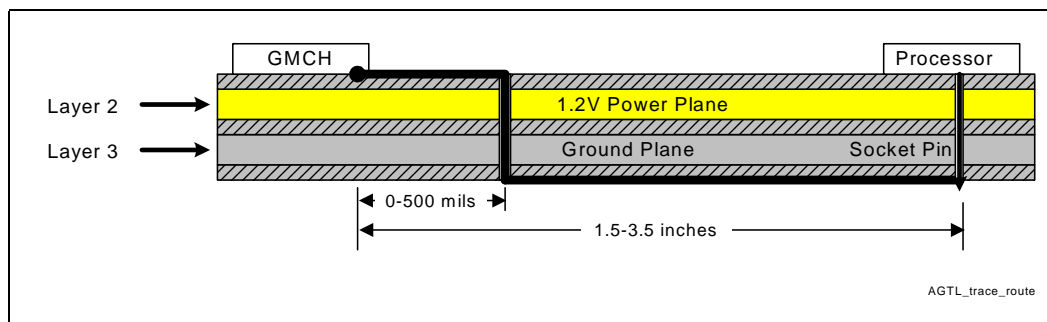
Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance.

Processor Breakout

It is strongly recommended that AGTL signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the processor on the same layer. If routing is tight, break out from the processor on the opposite routing layer over a ground reference and cross over to main signal layer near the processor.

Minimizing Crosstalk

The following general rules minimize the impact of crosstalk in a high-speed AGTL bus design:

- Maximize the space between traces. Where possible, maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges. It may be necessary to use tighter spacing when routing between component pins. When traces must be close and parallel to each other, minimize the distance that they are close together and maximize the distance between the sections when the spacing restrictions are relaxed.

- Avoid parallelism between signals on adjacent layers, if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.

- Since AGTL is a low-signal-swing technology, it is important to isolate AGTL signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings (e.g., 5 V PCI).

- AGTL signals must be well isolated from system memory signals. AGTL signal trace edges must be at least 30 mils from system memory trace edges within 100 mils of the ball of the Intel 82815 GMCH.

- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes crosstalk.

- Route AGTL address, data, and control signals in separate groups to minimize crosstalk between groups. Keep at least 15 mils between each group of signals.

- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.

- Minimize the dielectric process variation used in the PCB fabrication.

- Minimize the cross-sectional area of the traces. This can be done by means of narrower traces and/or by using thinner copper, but the trade-off for this smaller cross-sectional area is higher trace resistivity, which can reduce the falling-edge noise margin because of the I*R loss along the trace.

5.2.1.1   Motherboard Layout Rules for Non-AGTL (CMOS) Signals

Table 6.   Routing Guidelines for Non-AGTL Signals (Sheet 1 of 2)

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1" to 9"
FERR#	5 mils	10 mils	1" to 9"
FLUSH#	5 mils	10 mils	1" to 9"
IERR#	5 mils	10 mils	1" to 9"
IGNNE#	5 mils	10 mils	1" to 9"

Table 6.   Routing Guidelines for Non-AGTL Signals (Sheet 2 of 2)

Signal	Trace Width	Spacing to Other Traces	Trace Length
INIT#	5 mils	10 mils	1" to 9"
LINT[0] (INTR)	5 mils	10 mils	1" to 9"
LINT[1] (NMI)	5 mils	10 mils	1" to 9"
PICD[1:0]	5 mils	10 mils	1" to 9"
PREQ#	5 mils	10 mils	1" to 9"
PWRGOOD	5 mils	10 mils	1" to 9"
SLP#	5 mils	10 mils	1" to 9"
SMI#	5 mils	10 mils	1" to 9"
STPCLK	5 mils	10 mils	1" to 9"
THERMTRIP#	5 mils	10 mils	1" to 9"

NOTE: Route these signals on any layer or combination of layers.

5.2.1.2   THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor's thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance.

Figure 17. Routing for THRMDP and THRMDN

Signal Y

1 — Maximize (min. – 20 mils)

THRMDP

2 — Minimize

THRMDN

1 — Maximize (min. – 20 mils)

Signal Z

bus_routing_thrmdp-thrmdn
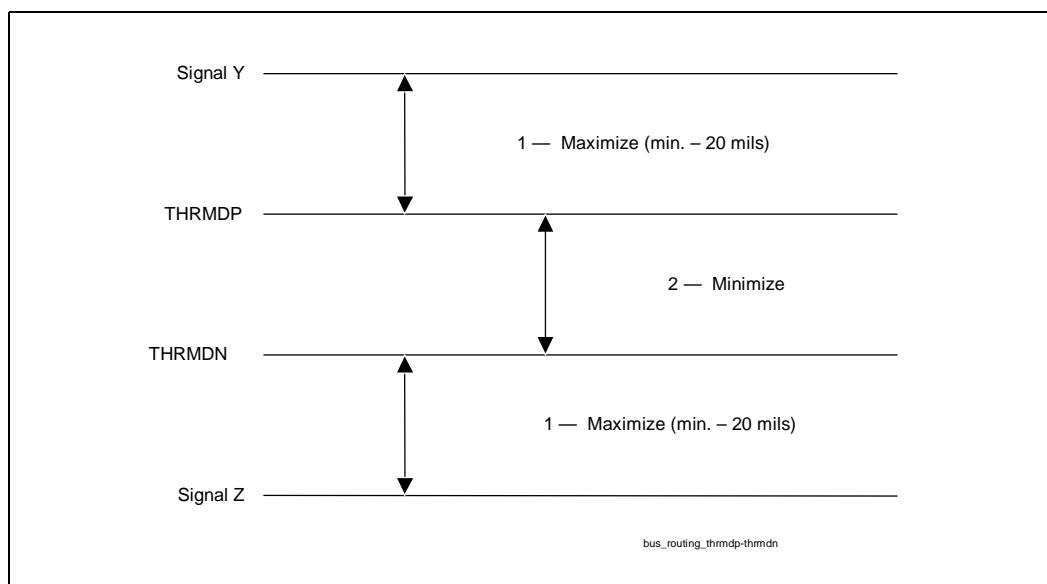
NOTES:
1. Route these traces parallel and equalize lengths within ± 0.5 inch.
2. Route THRMDP and THRMDN on the same layer.

5.2.1.3 Additional Routing and Placement Considerations

- Distribute VTT with a wide trace. An 0.050 inch minimum trace is recommended to minimize DC losses. Route the VTT trace to all components on the host bus. Be sure to include decoupling capacitors.

- The VTT voltage should be 1.25 V ± 3% for static conditions, and 1.25 V ± 9% for worst-case transient conditions.

- Place resistor divider pairs for VREF generation at the GMCH component. VREF also is delivered to the processor.

5.3 Electrical Differences for the Low Voltage Intel® Pentium® III Processor 512K and Ultra Low Voltage Intel® Celeron® Processor

There are several electrical changes between previous Pentium III processors and the current Low Voltage Intel® Pentium® III processor 512K and and Ultra Low Voltage Intel® Celeron® processor, as follows:

- Addition of VTTPWRGD signal to ensure stable VID selection.
- Addition of THERMTRIP circuit to allow processor to detect catastrophic overheat.
- Addition of VID[25mV] signal.
- Processor VTT level is 1.25 V.
- The Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor do not generate V_{CMOS}_REF.

Thre are also several electrical differences that exist between the current Low Voltage Intel® Pentium® III processor 512K and the Ultra Low Voltage Intel® Celeron® processor.

- Low Voltage Intel® Pentium® III processor 512K only supports a 133 MHz PSB, whereas the Ultra Low Voltage Intel® Celeron® processor only supports a 100 MHz PSB.
- Low Voltage Intel® Pentium® III processor 512K supports the VRM8.5 VID code whereas the Ultra Low Voltage Intel® Celeron® processor supports the IMVP-II VID code.
- The Ultra Low Voltage Intel® Celeron® processor does not support THERMTRIP

5.3.1 THERMTRIP Circuit

To ensure that the processor detects and prevents catastrophic overheat, THERMTRIP is required on all Low Voltage Intel® Pentium® III processor 512K designs. Figure 18 offers one possible implementation that makes use of the
Power Button feature on the ICH2.

Figure 18. Example Implementation of THERMTRIP Circuit
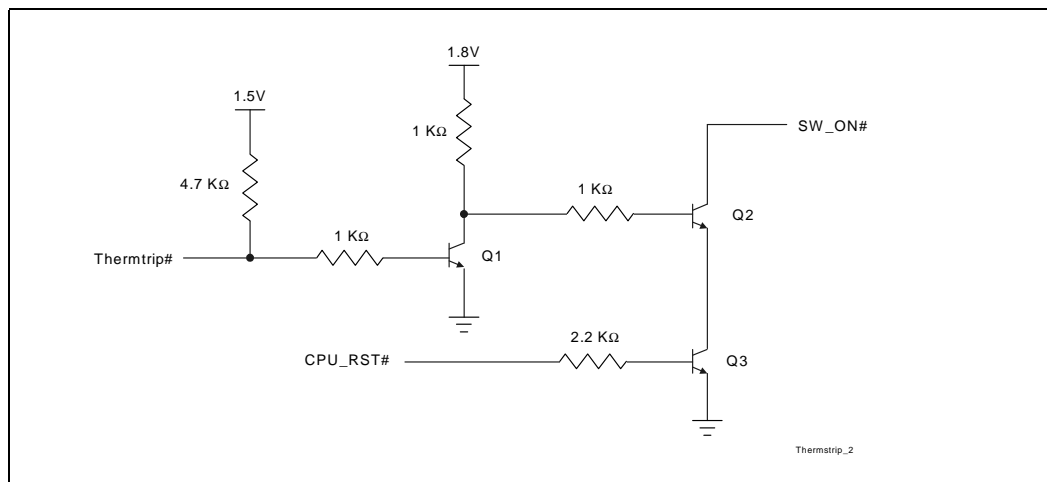
NOTES:
1. The pull-up voltage on the collector of Q1 is required to be 1.8 V derived from a 3.3 V source.
2. THERMTRIP is not valid until after CPU_RST# is deasserted. This is handled by gating the assertion of THERMTRIP with CPU_RST#. Using the CPU_RST# in this manner has minimal impact to the signal quality.
3. THERMTRIP must not go higher than VccCMOS levels. The pull-up on THERMTRIP is now connected to 1.5 V.
4. CPU_RST# must gate SW_ON# from ground. This prevents glitching on SW_ON# during power-up and power-down.
5. The resistance to the base of the transistor gating CPU_RST# must be at least 2.2 KΩ for proper Vih levels on CPU_RST#.

5.3.1.1   THERMTRIP Timing

When the THERMTRIP signal is asserted, both the VCC and VTT supplies to the processor must be turned off to prevent thermal runaway of the processor. The time required from THERMTRIP asserted to VCC rail at ½ nominal is 5 s, and THERMTRIP asserted to VTT rail at ½ nominal is 5 s. System designers must ensure that the decoupling scheme used on these rails does not violate the THERMTRIP timing specifications.

5.3.1.2   THERMTRIP Support

A platform supporting the Low Voltage Intel® Pentium® III 512K processor must implement a thermtrip workaround.

The internal control register bit responsible for operation of the THERMTRIP circuit functionality may power up in an un-initialized state. As a result, THERMTRIP# may be incorrectly asserted during de-assertion of RESET# at nominal operating temperatures. When THERMTRIP# is asserted as a result of this, the processor may shut down internally and stop execution. In addition, when the THERMTRIP# pin is asserted the processor may incorrectly continue to execute, leading to intermittent system power-on boot failures. The occurrence and repeatability of failures is system dependent, however all systems and processors are susceptible to failure.

To prevent the risk of power-on boot failures, a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:

- Rising edge occurs after Vcc_core is valid and stable

- Rising edge occurs before or at the de-assertion of RESET#
- Rising edge occurs after all Vref input signals are at valid voltage levels
- TCK input meets the Vih min (1.3 V) and max (1.65 V) spec requirements

Specific workaround implementations may be platform specific. The following examples have been tested as acceptable workaround implementations.

Note: The example workaround circuits attached require circuit modification for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Review the accompanying notes with each workaround for ITP modification details. If the system fails to boot when using ITP, issuing the ITP 'Reset Target' command on failing systems will reset the system and provide a sufficient rising edge on the TCK pin to ensure proper system boot.

In addition, the example workaround circuits shown do not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround solutions must be found if such test capability is required.

Figure 19. THERMTRIP# Workaround Circuit
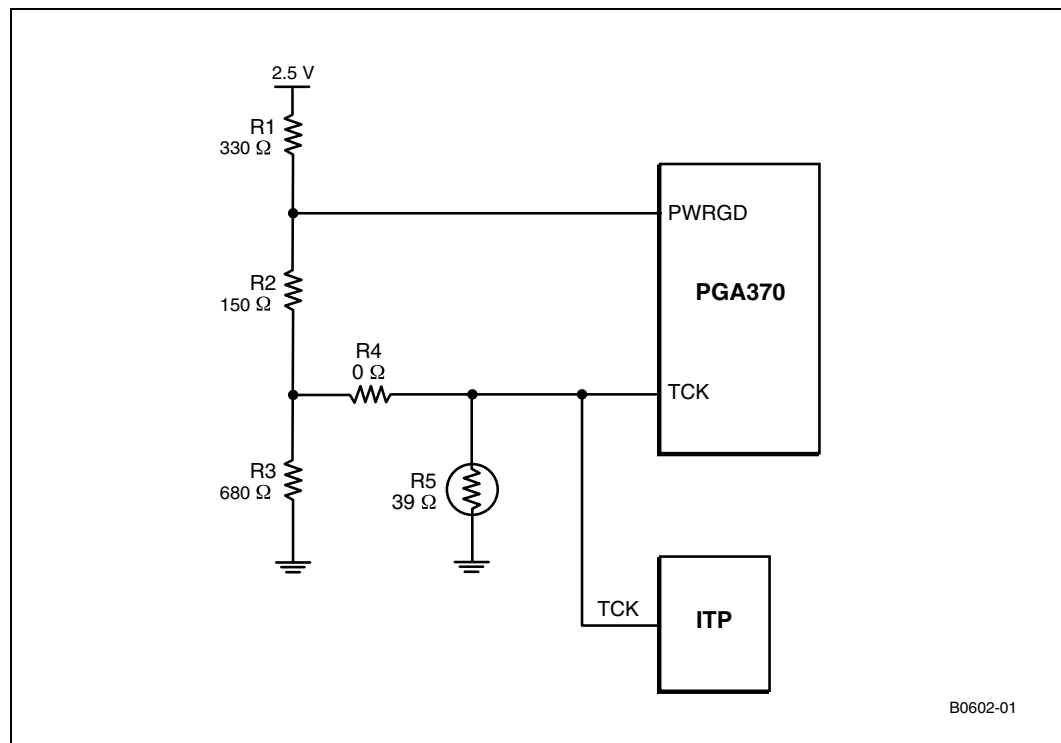
For Production Boards: Depopulate R5

To use ITP: Install R5, Depopulate R4

5.3.2   Single-Ended Clocking BSEL[1:0] Implementation

In a Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor platform that is using single-ended (SE) clocking or a clock source that does not support the VTT_PWRGD protocol, the normal BSEL frequency selection process will not work. Since the clock generator is not compatible with dynamic BSEL assertions, all BSEL[1:0] signals should not be connected together. Instead, the BSEL pins on the clock generator should be pulled-up to 3.3 V through a 1 KΩ, 5% resistor. This strapping will force the clock generator into 133 MHz clocking mode and will only support the 133 MHz capable Low Voltage Intel® Pentium® III processor 512K. To support 100 MHz PSB for the Ultra Low Voltage Intel® Celeron® processor populate the 0 Ω, pull-down resistor to ground on BSEL1. In addition, each BSEL[1:0] of each processor should be left unconnected. Figure 20 shows a diagram of this implementation.

The BSEL[1:0] lines are not valid until VTT_PWRGD is asserted.

Figure 20. Single-Ended Clock BSEL Circuit (100/133 MHz)
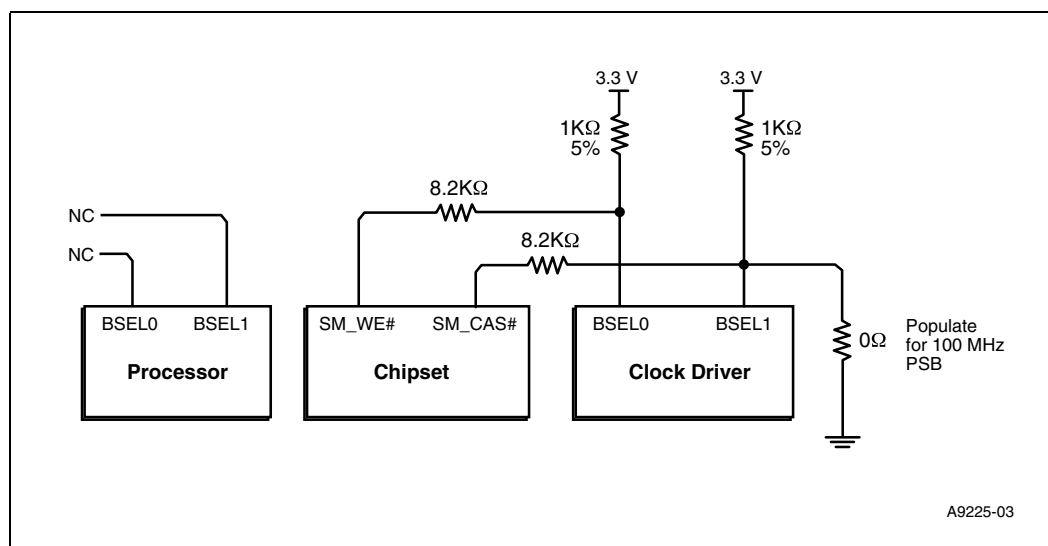
5.4   CLKREF Circuit Implementation

The CLKREF input requires a 1.25 V source. It can be generated from a voltage divider on the VCC2.5 or VCC3.3 sources utilizing 1% tolerant resistors. A 4.7 µF decoupling capacitor should be included on this input. See Figure 21 and Table 7 for example CLKREF circuits. Do not use V_{TT} as the source for this reference.

Figure 21. Examples for CLKREF Divider Circuit
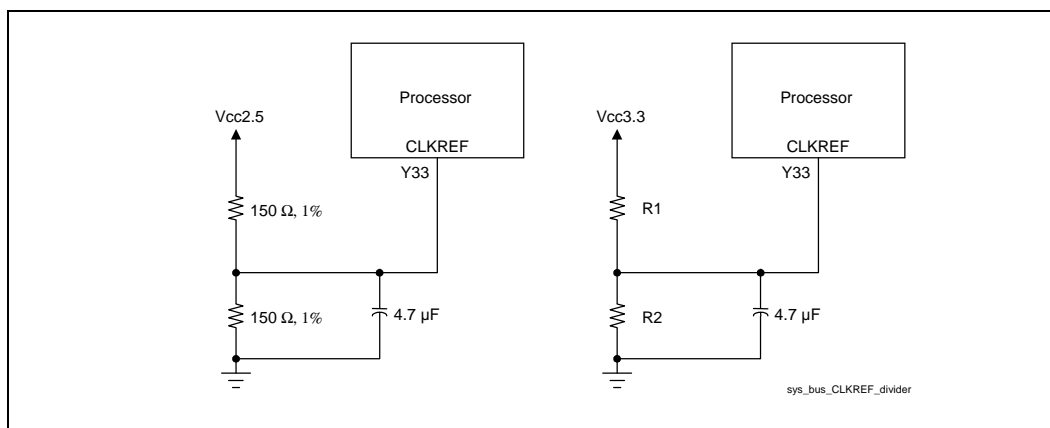
Table 7. Resistor Values for CLKREF Divider (3.3 V Source)

R1 (Ω), 1%	R2 (Ω), 1%	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

5.5 Undershoot/Overshoot Requirements

Undershoot and overshoot specifications become more critical as the process technology for microprocessors shrinks due to thinner gate oxide. Violating these undershoot and overshoot limits will degrade the life expectancy of the processor.

The Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor have more restrictive overshoot and undershoot requirements for system bus signals than previous processors. These requirements stipulate that a signal at the output of the driver buffer and at the input of the receiver buffer must not exceed the maximum absolute overshoot voltage limit or the minimum absolute undershoot voltage limit. Exceeding either of these limits will damage the processor. There is also a time-dependent, non-linear overshoot and undershoot requirement that depends on the amplitude and duration of the overshoot/undershoot. See the processor datasheet for more details on the processor overshoot/undershoot specifications.

5.6 Processor Reset Requirements

Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor designs must route the AGTL reset signal from the chipset to the processor as well as to the debug port connector. This reset signal is connected to the following balls at the processor.

> **B15 (RESET#).** The reset signal is connected to this ball for the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor

Note: The AGTL reset signal must always terminate to VTT on the motherboard.

Designs that do not support the debug port will not utilize the 240 Ω series resistor or the connection of RESET# to the debug port connector.

The routing rules for the AGTL reset signal are shown in Figure 22.

Figure 22. RESET# Routing Guidelines

A9227-01
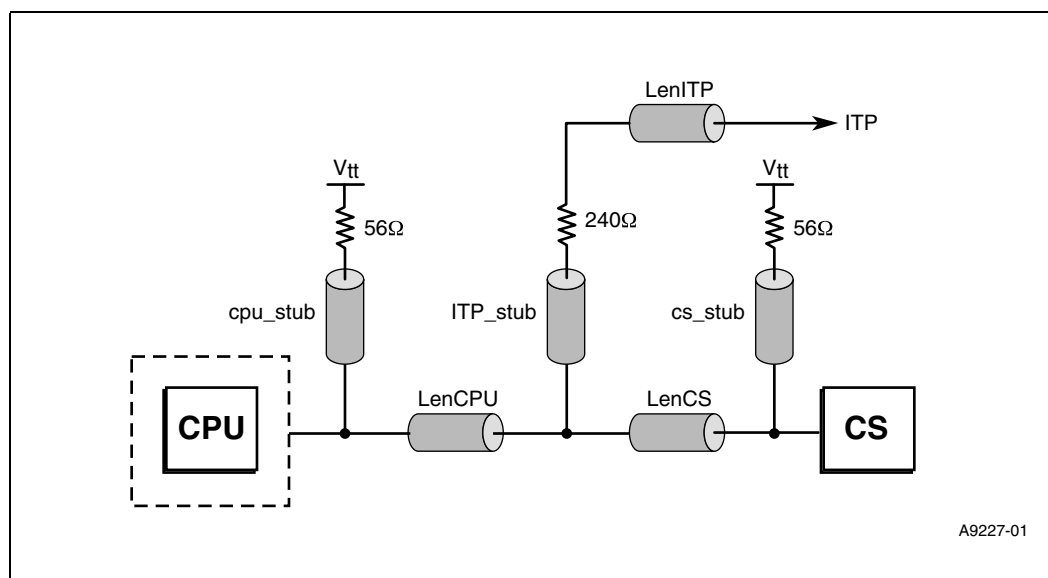
Table 8. RESET# Routing Guidelines

Parameter	Minimum (in)	Maximum (in)
LenCS	0.5	1.5
LenITP	1	3
LenCPU	0.5	1.5
cs stub	0.5	1
cs stub	0.5	1
ITP stub	short as possible	

5.6.1   PLL Filter Recommendations

It is highly critical that phase lock loop power delivery to the processor meets Intel's requirements. A low pass filter is required for power delivery to pins PLL1 and PLL2. This serves as an isolated, decoupled power source for the internal PLL.

5.6.1.1   Topology

The Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor has internal phase lock loop (PLL) clock generators, which are analog and require a quiet power supply to minimize jitter. PLL1 should have a 4.7-µH inductor connected in series to VTT, and PLL2 should be connected through a capacitor (22- to 100-µF) to PLL1.

5.6.2   Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 27.

Figure 23. Filter Specification
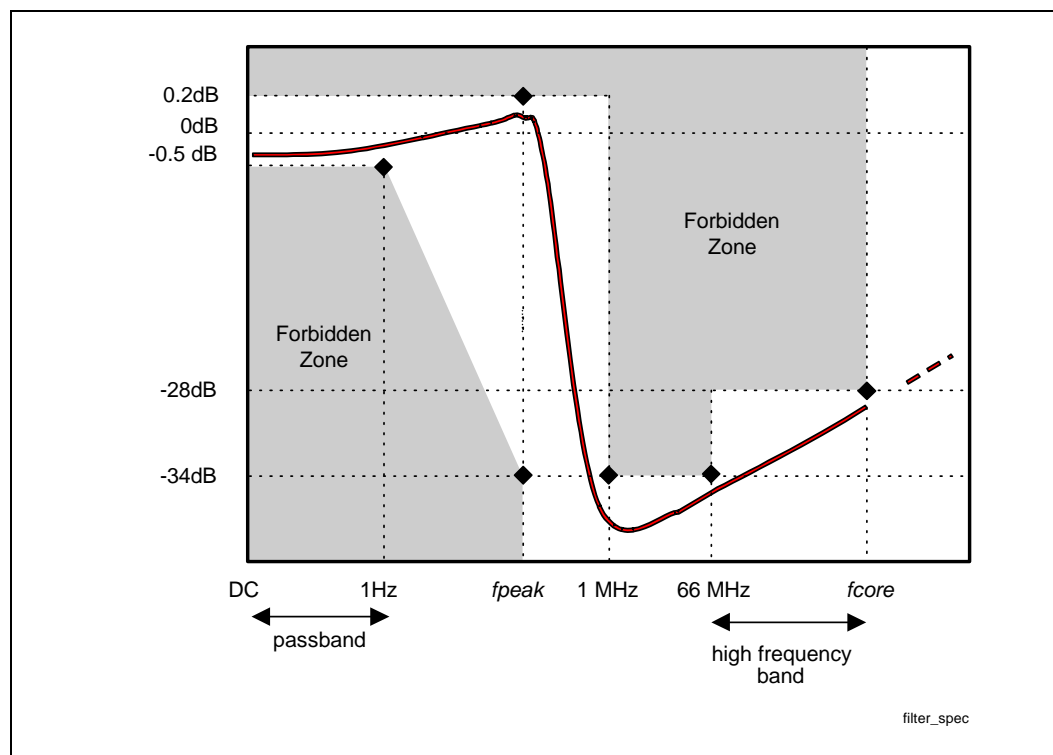
NOTES:
6. Diagram not to scale.
7. No specification for frequencies beyond *fcore*.
8. *fpeak* should be less than 0.05 MHz.

Other requirements:

- Use shielded-type inductor to minimize magnetic pickup.
- Filter should support DC current > 30 mA.

- DC voltage drop from VCC to PLL1 should be < 60 mV, which in practice implies series R < 2 Ω. This also means pass-band (from DC to 1 Hz) attenuation < 0.5 dB for VCC = 1.1 V, and < 0.35 dB for VCC = 1.5 V.

5.6.3   Recommendation for Intel Platforms

The following tables contains examples of components that meet Intel's recommendations when configured in the topology of Figure 24.

Table 9.   Component Recommendations – Inductor

Part Number	Value	Tolerance	SRF	Rated Current	DCR (Typical)
TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max.)
Murata LQG21N4R7K00T1	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (±50%)
Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3 Ω max.

Table 10. Component Recommendations – Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%	2.5 nH	0.2 Ω

Table 11. Component Recommendation – Resistor

Value	Tolerance	Power	Note
1 Ω	10%	1/16 W	Resistor may be implemented with trace resistance, in which case a discrete R is not needed. See Figure 25.

To satisfy damping requirements, total series resistance in the filter (from VCC_{CORE} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component or routing or both. For example, if the chosen inductor has minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1 (1 Ω ± 1%), the maximum DCR of the L (trace plus inductor) should be less than 2.0 – 1.1 = 0.9 Ω, which precludes the use of some inductors and sets a max. trace length.

Other routing requirements:

- The capacitor (C) should be close to the PLL1 and PLL2 pins, < 0.1 Ω per route. These routes do not count towards the minimum damping R requirement.

- The PLL2 route should be parallel and next to the PLL1 route (i.e., minimize loop area).

- The inductor (L) should be close to C. Any routing resistance should be inserted between VCC_{CORE} and L.

- Any discrete resistor (R) should be inserted between VCC_{CORE} and L.

Figure 24. Example PLL Filter Using a Discrete Resistor
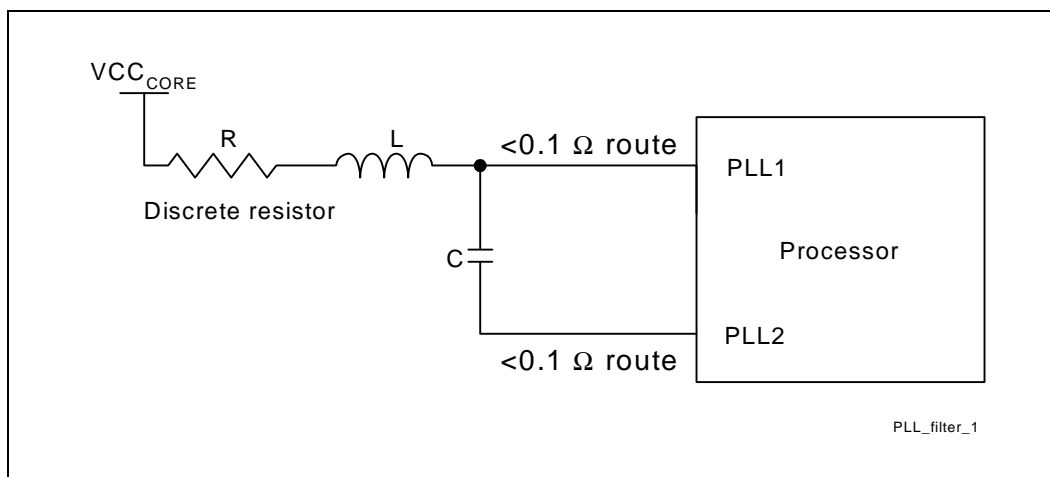
Figure 25. Example PLL Filter Using a Buried Resistor
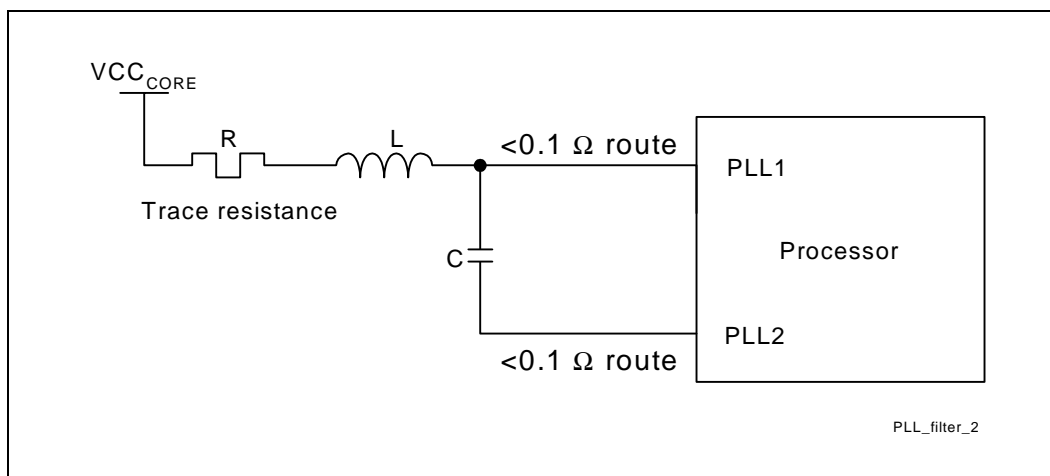
5.6.4   Custom Solutions

As long as designers satisfy filter performance and requirements as specified and outlined in Section 5.6.2, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in Figure 26.

Figure 26. Core Reference Model
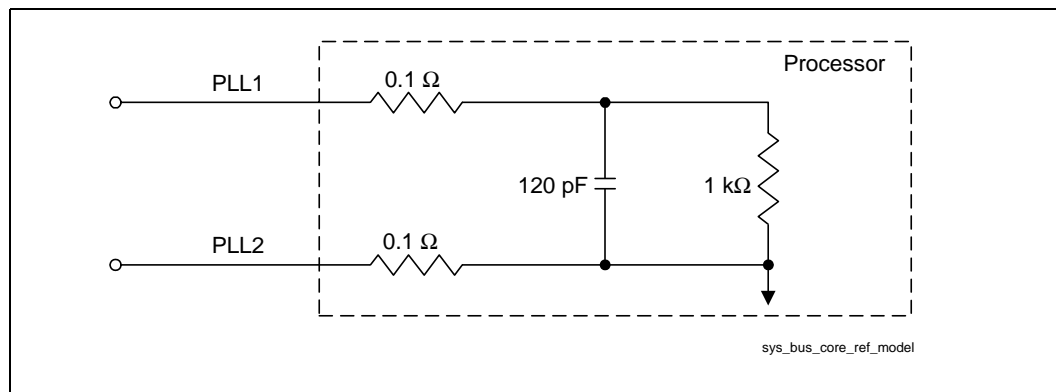
NOTES:
1. 0.1 Ω resistors represent package routing.
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1 kΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum VCC_{CORE} level.
7. For other modules (interposer, DMM, etc.), adjust routing resistor if desired, but use minimum numbers.

5.6.5 Supplying Voltage

Local (point of load) regulation is recommended for the Low Voltage Intel Pentium lll processor 512K and Ultra Low Voltage Intel® Celeron® processor to satisfy their higher current requirements and to maintain power converter output voltage tolerance. For example, a DC-to-DC converter, placed close to the load, converts a higher DC voltage to a lower level using either a linear or switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R) and localizes losses to the planes between the converter and the processor sockets.

It is recommended that voltage regulator solutions employ differential remote sense to compensate for voltage drops between the regulators and the socket pins. The sense lines should be terminated as close to the center of the socket as possible and should not have an impedance greater than 1 Ω.

5.6.5.1 AGTL V_{REF} Decoupling Design

Three 0.1-µF capacitors in 0603 packages should be placed within 500 mils of the V_{REF} pins. Two should be connected between V_{TT} and V_{REF}, and one should be connected between V_{REF} and ground. If this circuit is far from the Low Voltage Intel Pentium lll Processor 512K and Ultra Low Voltage Intel® Celeron® processor, add a 0.1-µF capacitor for decoupling.

5.7 Thermal Requirements

In the event the processor drives the THERMTRIP# signal active during valid operation, both the V_{CC} and V_{TT} supplies to the processor must be powered off to prevent thermal runaway of the processor. Valid operation refers to the operating conditions where the THERMTRIP# signal is guaranteed valid. The time required from THERMTRIP# assertion to V_{CC} rail at 1/2 nominal is 5 seconds and THERMTRIP# asserted to V_{TT} rail at 1/2 nominal is 5 seconds.

5.8   Debug Port Changes

Due to the lower voltage technology employed with newer processors, changes are required to support the debug port. Previously, test access port (TAP) signals used 2.5 V logic. The Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor utilizes 1.5 V logic levels on the TAP. The 1.5 V connector is a mirror image of the older 2.5 V connector. Either connector will fit into the same printed circuit board layout. Only the pin numbers change (Figure 26). Also required, along with the new connector, is an In-Target Probe* (ITP) that is capable of communicating with the TAP at the appropriate logic levels.

Figure 27. TAP Connector Comparison
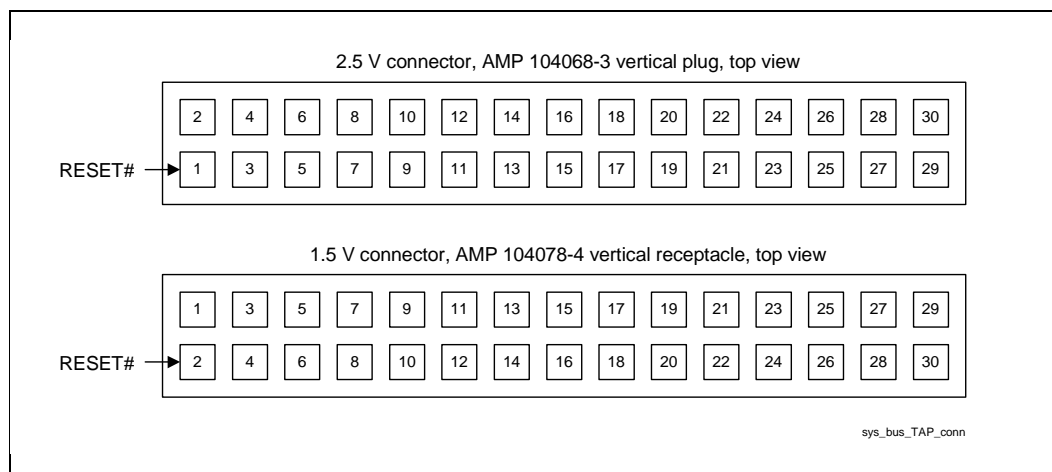
Caution: The Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor requires an in-target probe (ITP) compatible with 1.5 V signal levels on the TAP. Previous ITPs were designed to work with higher voltages and may damage the processor if connected to any of these specified processors.

See the processor datasheet for more information regarding the debug port.

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System Memory Design Guidelines   **6**

6.1   System Memory Routing Guidelines

Ground plane reference all system memory signals. To provide a good current return path and limit noise on the system memory signals, the signals should be ground referenced from the GMCH to the DIMM connectors and from DIMM connector-to-DIMM connector. If ground referencing is not possible, system memory signals should be, at a minimum, referenced to a single plane. If single plane referencing is not possible, stitching capacitors should be added no more than 200 mils from the signal via field. System memory signals may via to the backside of the PCB under the GMCH without a stitching capacitor as long as the trace on the topside of the PCB is less than 200 mils.

Note: Intel recommends that a parallel plate capacitor between VCC3.3SUS and GND be added to account for the current return path discontinuity (See Decoupling section). Use (1).01uf X7R capacitor per every (5) system memory signals that switch plane references. No more than two vias are allowed on any system memory signal.

If a group of system memory signals must change layers, a via field should be created and a decoupling capacitor should be added at the end of the via field. Do not route signals in the middle of a via field, this causes noise to be generated on the current return path of these signals and can lead to issues on these signals (see Figure 28). The traces shown are on layer 1 only. The figure shows signals that are changing layer and two signals that are not changing layer. Note that the two signals around the via field create a keepout zone where no signals that do not change layer should be routed.

Figure 28. System Memory Routing Guidelines

Do not route any signal in the middle of the via field that do not change layers

Add (1) 0.01 uf capacitor X7R (5) signals that via

Stagger vias in via field to avoid power/ground plane cut off because of the antipad on the internal layers

sys-mem-route
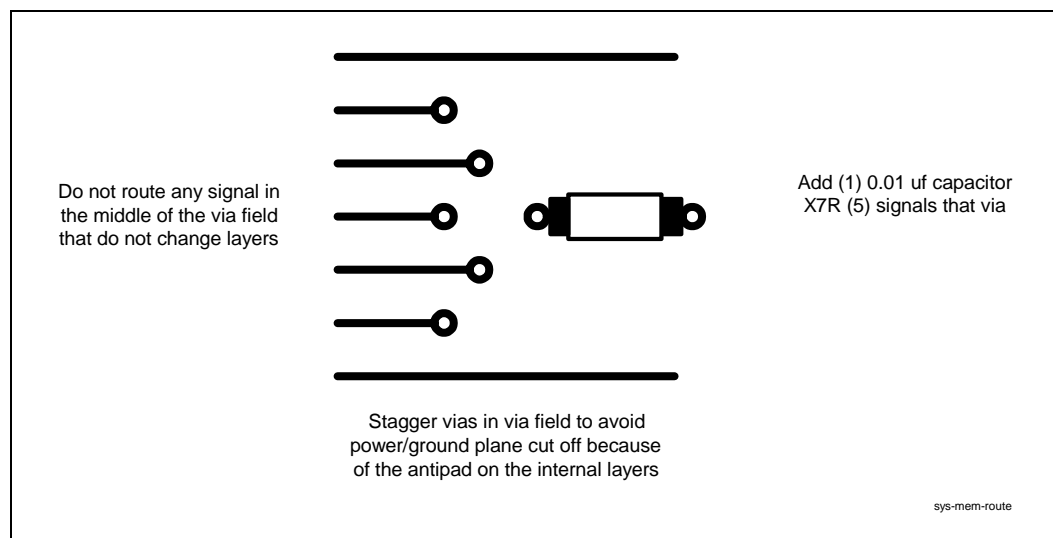
6.2   System Memory Two-DIMM Design Guidelines

6.2.1   System Memory Two-DIMM Connectivity

Figure 29. System Memory Connectivity (Two DIMM)
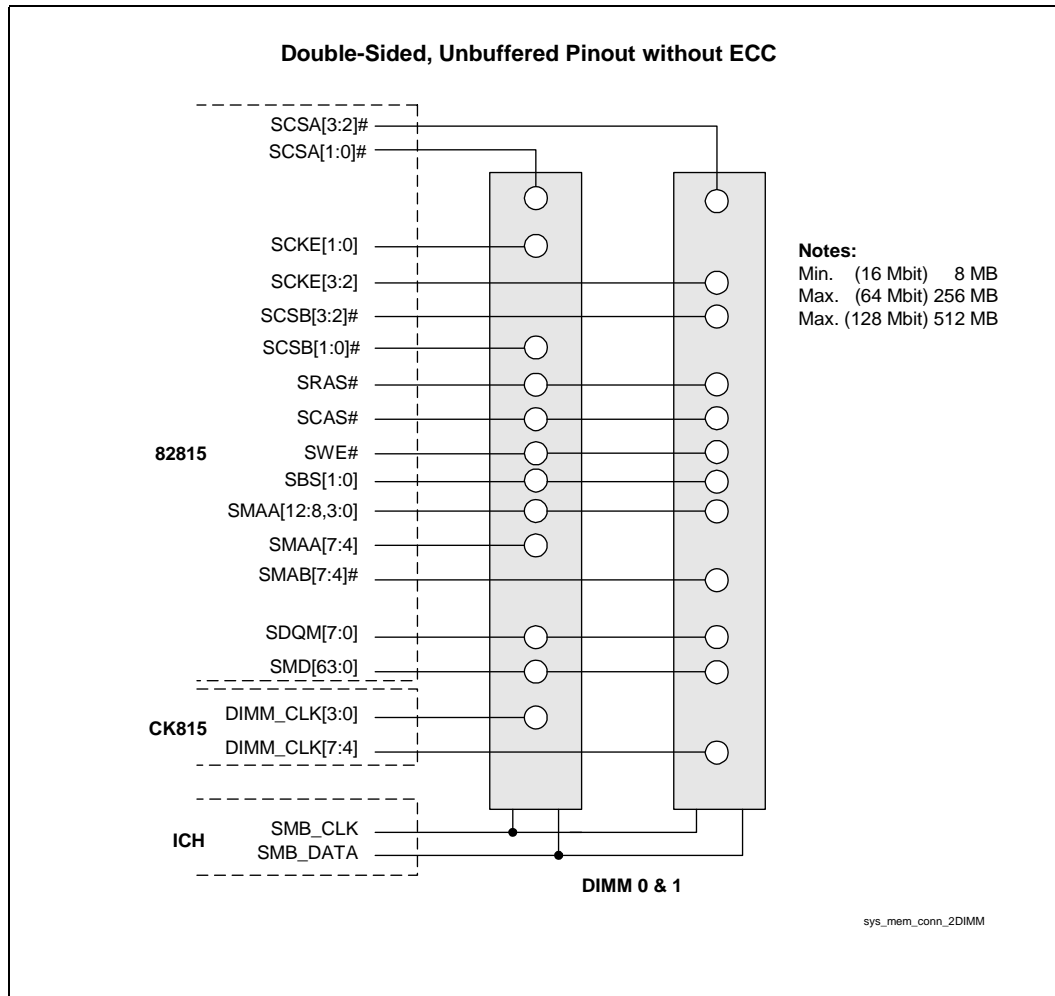
6.2.2 System Memory Two-DIMM Layout Guidelines

Figure 30. System Memory Two-DIMM Routing Topologies

```
                82815                                              DIMM 0   DIMM 1

   Topology 1   |>      [======== A ========]          •—[ B ]—•
   Topology 2   |>      [======== C ========]          •                   •
   Topology 3   |>      [======== D ========]          •                   •
                             10 Ω
   Topology 4   |>    [E]-/\/\/-[======= F =======]    •
                             10 Ω
   Topology 5   |>    [E]-/\/\/-[======= F =======]                        •

                                             sys_mem_2DIMM_routing_topo
```
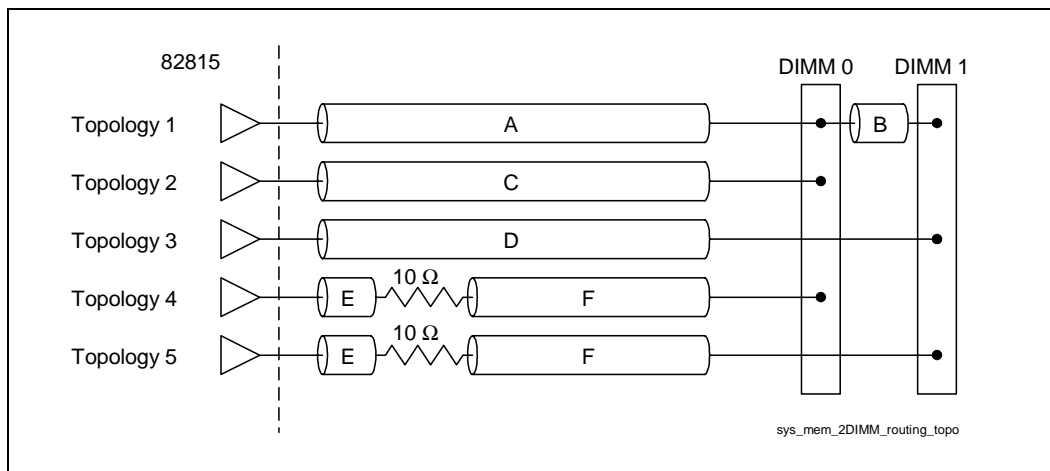
Table 12. System Memory Two-DIMM Solution Space

Signal	Top	Trace (mils)		Trace Lengths (inches)											
				A		B		C		D		E		F	
		Width	Spacing	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SCS[3:2]#	3	5	10							1	4.5				
SCS[1:0]#	2	5	10					1	4.5						
SMAA[7:4]	4	10	10									0.4	0.5	2	4
SMAB[7:4]#	5	10	10									0.4	0.5	2	4
SCKE[3:2]	3	10	10							3	4				
SCKE[1:0]	2	10	10					3	4						
SMD[63:0]	1	5	10	1.75	4	0.4	0.5								
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5								
SCAS#, SRAS#, SWE#	1	5	10	1	4.0	0.4	0.5								
SBS[1:0], SMAA[12:8, 3:0]	1	5	10	1	4.0	0.4	0.5								

In addition to meeting the spacing requirements outlined in Table 12, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

Figure 31. System Memory Routing Example
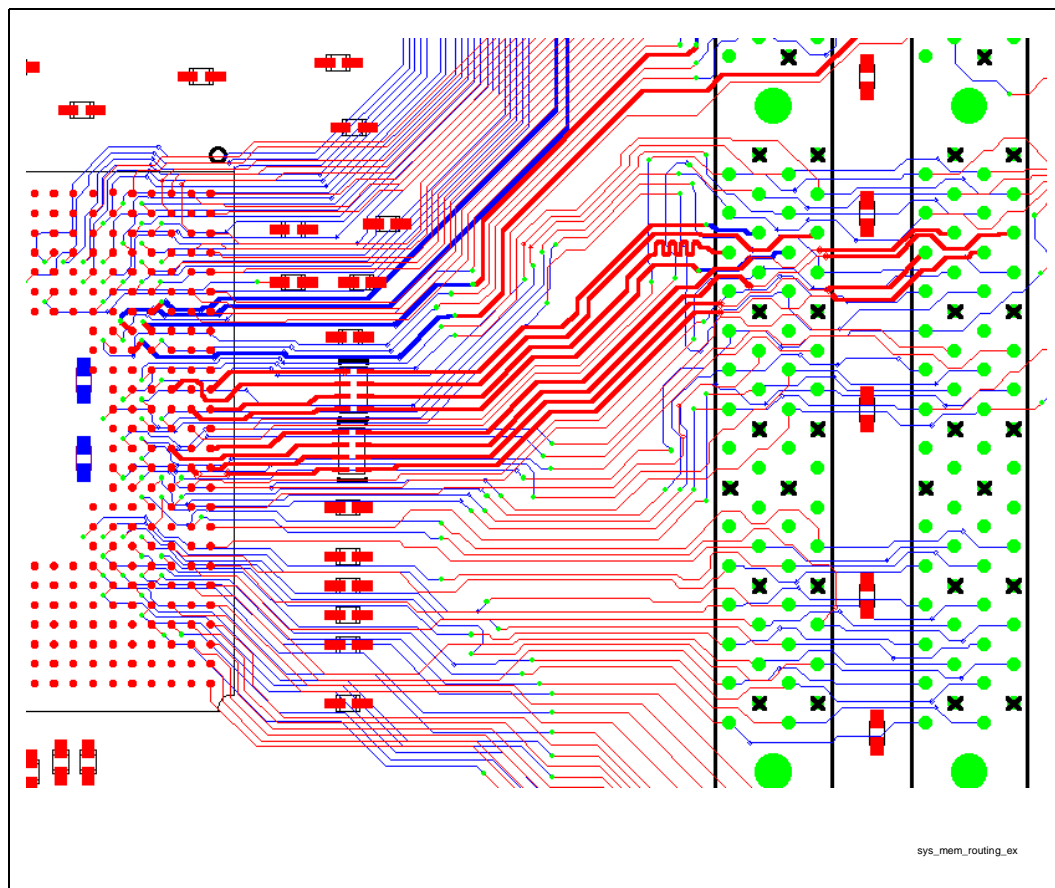
NOTE: Routing in this figure is for example purposes only. It does not necessarily represent complete and correct routing for this interface.

6.3   System Memory Three-DIMM Design Guidelines

6.3.1   System Memory Three-DIMM Connectivity

Figure 32. System Memory Connectivity (Three DIMM)
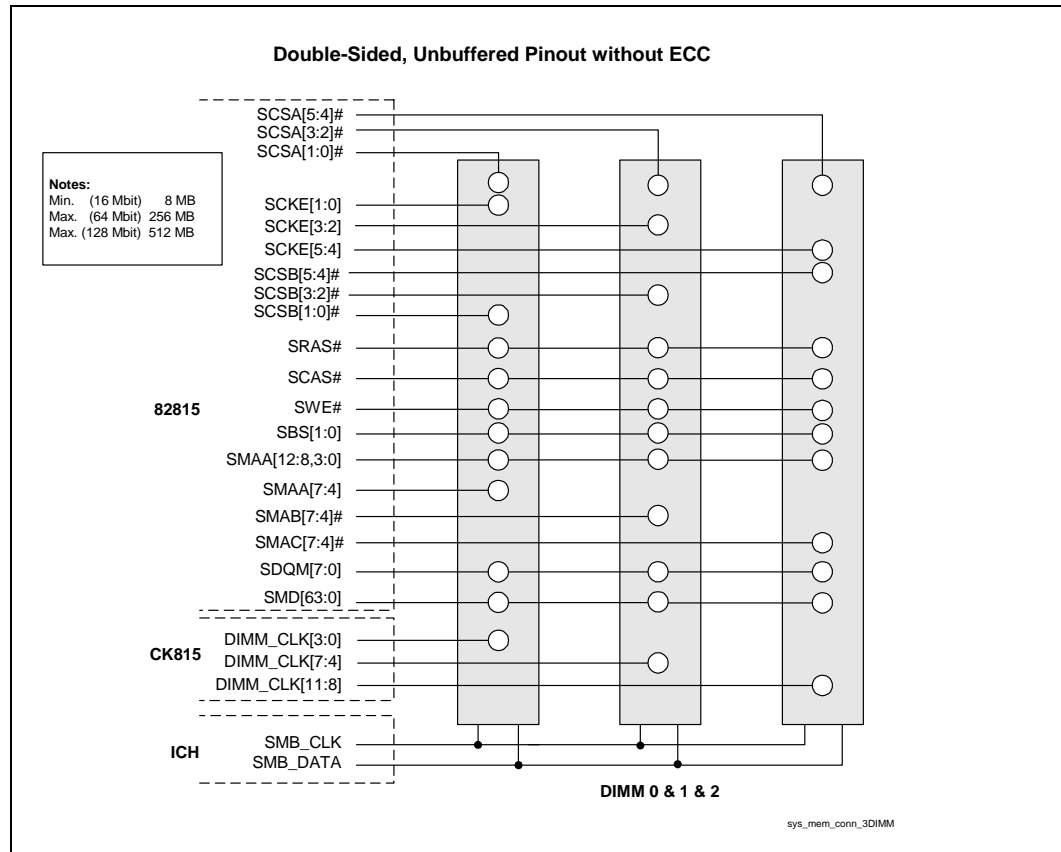
In addition to meeting the spacing requirements outlined in Table 13, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

Table 13. System Memory Three-DIMM Solution Space

Signal	Top	Trace (mils)		Trace Lengths (inches)													
				A		B		C		D		E		F		G	
		Width	Spacing	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SCS[5:4]#	4	5	10									1	4.5				
SCS[3:2]#	3	5	10							1	4.5						
SCS[1:0]#	2	5	10					1	4.5								
SMAA[7:4]	6	10	10					2	4							0.4	0.5
SMAB[7:4]#	7	10	10							2	4					0.4	0.5
SMAC[7:4}	8	10	10									2	4			0.4	0.5
SCKE[5:4]	4	10	10									3	4				
SCKE[3:2]	3	10	10							3	4						
SCKE[1:0]	2	10	10					3	4								
SMD[63:0]	1	5	10	1.75	4	0.4	0.5										
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5										
SCAS#,SRAS#, SWE#	5	5	10			0.4	0.5							1	4		
SBS[1:0], SMAA[12:8,3:0]	5	5	10			0.4	0.5							1	4		

6.4　System Memory Decoupling Guidelines

A minimum of eight 0.1 µF low-ESL ceramic capacitors (e.g., 0603 body type, X7R dielectric) are required and must be as close as possible to the GMCH. They should be placed within at most 70 mils to the edge of the GMCH package edge for VSUS_3.3 decoupling, and they should be evenly distributed around the system memory interface signal field including the side of the GMCH where the system memory interface meets the host interface. There are power and GND balls throughout the system memory ball field of the GMCH that need good local decoupling. Make sure to use at least 14 mil drilled vias and wide traces from the pads of the capacitor to the power or ground plane to create a low inductance path. If possible multiple vias per capacitor pad are recommended to further reduce inductance. To add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (500 mils max).

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To further de-couple the GMCH and provide a solid current return path for the system memory interface signals it is recommended that a parallel plate capacitor be added under the GMCH. Add a topside or bottom side copper flood under center of the GMCH to create a parallel plate capacitor between VCC3.3 and GND (see Table 33). The dashed lines indicate power plane splits on layer 2 or layer 3 depending on stack-up. The filled region in the middle of the GMCH indicates a ground plate (on layer one if the power plane is on layer two or on layer four if the power layer is on layer three).

Figure 33. Intel® 815 Chipset Platform Decoupling Example
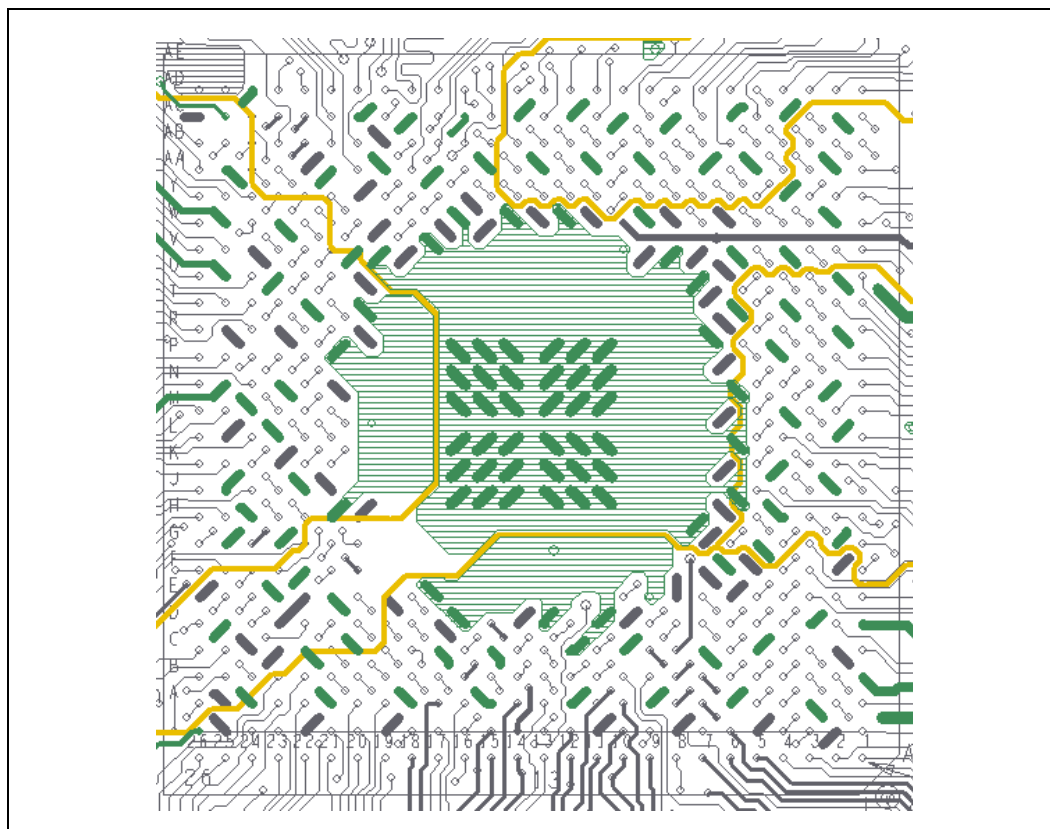
Yellow lines show layer two plane splits. Note that the layer 1 shapes do NOT cross the plane splits. The bottom shape is a VSS fill over VddSDRAM. The left-side shape is a VSS fill over VddAGP. The larger upper-right-side shape is a VSS fill over VddCORE.

Additional decoupling capacitors should be added between the DIMM connectors to provide a current return path for the reference plane discontinuity created by the DIMM connectors themselves. One 0.01 µF X7R capacitor should be added per every ten SDRAM signals. Capacitors should be placed between the DIMM connectors and evenly spread out across the SDRAM interface.

For debug purposes, four or more 0603 capacitor sites should be placed on the backside of the board, evenly distributed under the Intel 815E chipset platform's system memory interface signal field.

Figure 34. Intel® 815 Chipset Decoupling Example
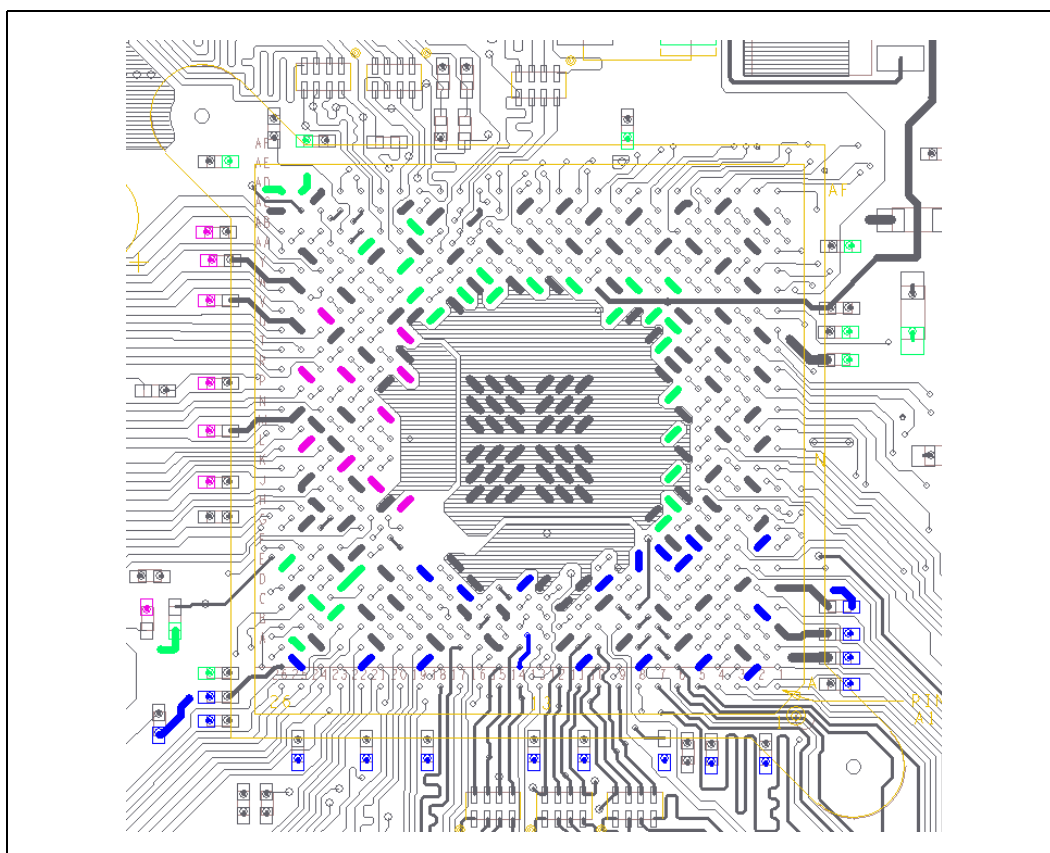
6.5 Compensation

A system memory compensation resistor (SRCOMP) is used by the GMCH to adjust the buffer characteristics to specific board and operating environment characteristics. Refer to the *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet* for details on compensation. Tie the SRCOMP pin of the GMCH to a 40 Ω 1% or 2% pull-up resistor to 3.3 Vsus (3.3 V standby) via a 10 mil-wide, 0.5 inch trace (targeted for a nominal impedance of 40 Ω).

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AGP/Display Cache Design Guidelines 7

For the detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest *AGP Interface Specification*, *Revision 2.0*, which can be obtained from http://www.agpforum.org. This design guide focuses only on specific Intel 815 chipset platform recommendations.

7.1   AGP Interface

A single AGP connector is supported by the GMCH AGP interface. LOCK# and SERR#/PERR# are not supported. See the display cache discussion for a description of display cache/AGP muxing as well as a description of the Graphics Performance Accelerator (GPA).

The AGP buffers operate in one of two selectable modes, to support the AGP universal connector:

- 3.3 V drive, not 5 V safe. This mode is compliant with the AGP 1.0 66 MHz specification
- 1.5 V drive, not 3.3 V safe. This mode is compliant with the AGP 2.0 specification

The AGP 4X must operate at 1.5 V and only use differential clocking mode. The AGP 2X can operate at 3.3 V or 1.5 V. The AGP interface supports up to 4X AGP signaling, though 4X fast writes are not supported. AGP semantic cycles to DRAM are not snooped on the host bus.

The GMCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. The GMCH contains a 32-deep AGP request queue. High-priority accesses are supported. All AGP semantic accesses hitting the graphics aperture pass through an address translation mechanism with a fully-associative, 20-entry TLB.

Accesses between AGP and the hub interface are limited to hub interface-originated memory writes to AGP. Cacheable accesses from the IOQ queue flow through one path, while aperture accesses follow another path. Cacheable AGP (SBA, PIPE#, and FRAME#) reads to DRAM all snoop the cacheable global write buffer (GWB) for system data coherency. Aperture AGP (SBA, PIPE#) reads to DRAM snoop the aperture queue (GCMCRWQ). Aperture AGP (FRAME#) reads and writes to DRAM proceed through a FIFO and there is no RAW capability, so no snoop is required.

The AGP interface is clocked from the 66 MHz clock (3V66). The AGP-to-host/memory interface is synchronous with a clock ratio of 1:1 (66 MHz: 66 MHz), 2:3 (66 MHz: 100 MHz) and 1:2 (66 MHz: 133 MHz).

7.1.1   Graphics Performance Accelerator

The GMCH multiplexes the AGP signal interface with the integrated graphics' display cache interface. As a result, for a motherboard that supports both integrated graphics and add-in AGP video cards, display cache (for integrated graphics) must be populated on a card in the universal AGP slot. The card is called a Graphics Performance Accelerator (GPA) card. Intel provides a specification for this card in a separate document (*Graphics Performance Accelerator Specification*).

AGP guidelines are presented in this section for motherboards that support the population of a GPA card in their AGP slot as well as for those that do not, and for AGP "down" implementations in which AGP-compliant devices are implemented directly on motherboards. Where there are distinct guidelines dependent on whether or not a motherboard will support a GPA card, the section detailing standard routing guidelines is divided into subsections, as follows:

- The Flexible Motherboard Guidelines subsection is to be complied with if the motherboard supports a GPA card populated in the AGP slot.

- The AGP-Only Motherboard Guidelines subsection is to be complied with if the motherboard does **not** support a GPA card populated in the AGP slot.

7.1.2   AGP Universal Retention Mechanism

Environmental testing and field reports indicate that AGP cards and Graphics Performance Accelerator (GPA) cards may come unseated during system shipping and handling without proper retention. To avoid disengaged AGP cards and GPA modules, Intel recommends that AGP-based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket that is used to properly locate the card with respect to the chassis and to assist with card retention. The AGP RM is available in two different handle orientations: left-handed (see Figure 35) and right-handed. Most system boards accommodate the left-handed AGP RM. The manufacturing capacity of the left-handed RM currently exceeds the right-handed capacity, and as a result Intel recommends that customers design their systems to insure they can use the left-handed version of the AGP RM. The right-handed AGP RM is identical to the left-handed AGP RM, except for the position of the actuation handle. This handle is located on the same end as the primary design, but extends from the opposite side (mirrored about the center axis running parallel to the length of the part). Figure 36 contains keepout information for the left hand AGP retention mechanism. Use this information to make sure that the motherboard design leaves adequate space to install the retention mechanism.

The AGP interconnect design requires that the AGP card must be retained to the extent that the card not back out more than 0.99 mm (0.039 in) within the AGP connector. To accomplish this it is recommended that new cards implement an additional notch feature in the mechanical keying tab to allow an anchor point on the AGP card for interfacing with an AGP RM. The retention mechanism's round peg engages with the AGP or GPA card's retention tab and prevents the card from disengaging during dynamic loading. The additional notch feature in the mechanical keying tab is required for 1.5 V AGP cards and is recommended for the new 3.3 V AGP cards.

Figure 35. AGP Left-Handed Retention Mechanism
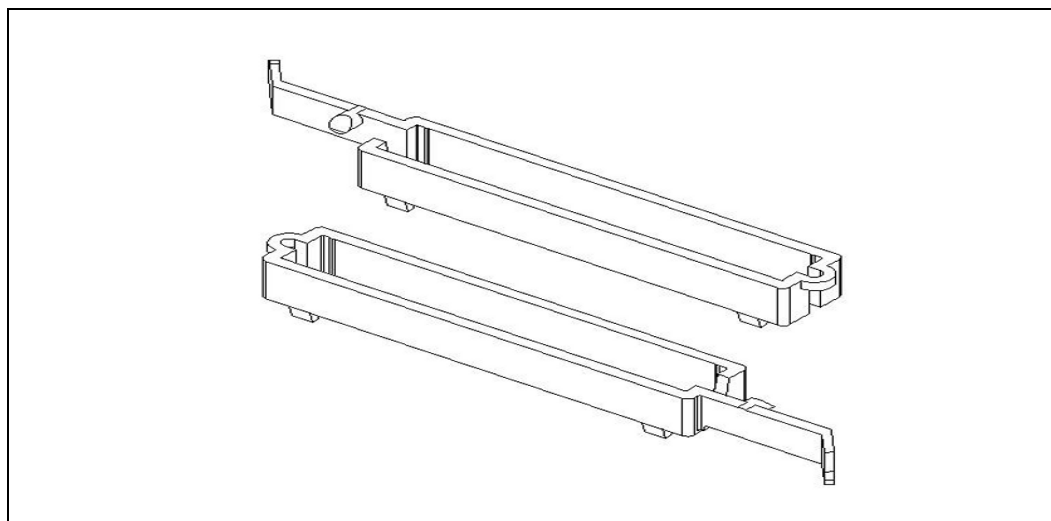
Figure 36. AGP Left-Handed Retention Mechanism Keepout Information
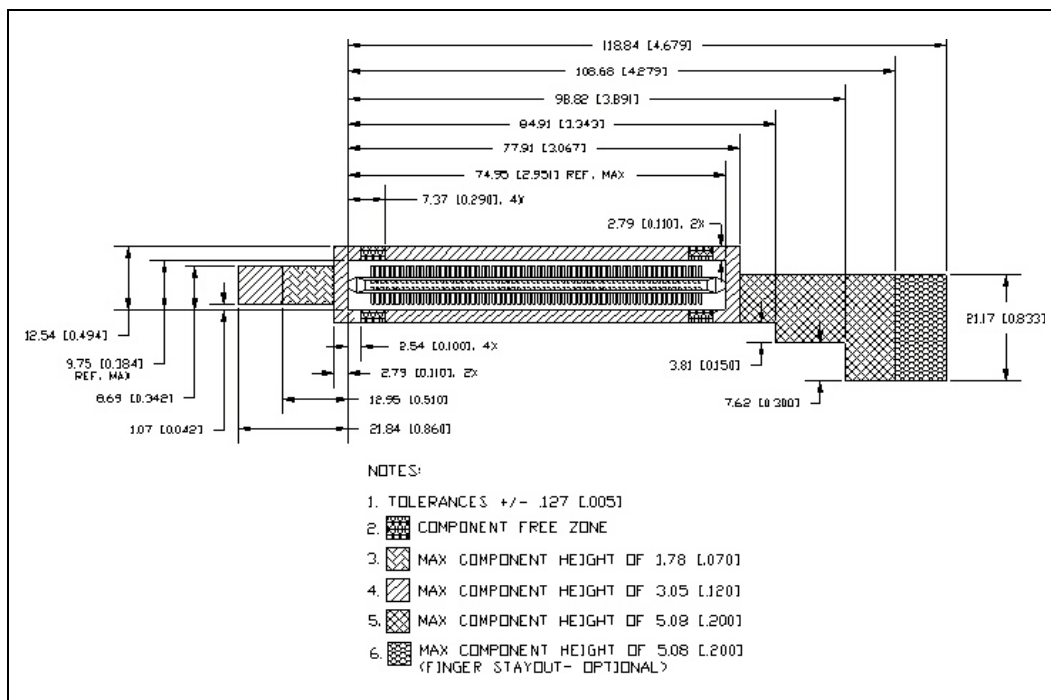
Engineering Change Request number 48 (ECR #48) of the AGP specification details the AGP RM, which is recommended for all AGP cards. These are approved changes to the *Accelerated Graphics Port (AGP) Interface Specification*, Revision 2.0. Intel intends to incorporate the AGP RM changes into later revisions of the AGP Interface Specification. In addition, Intel has defined a reference design of a mechanical device to utilize the features defined in ECR #48.

ECR #48 can be viewed at the Intel website at: http://developer.intel.com/technology/agp/ecr.htm.

More information regarding this component (AGP RM) is available from the following vendors. The inclusion of this list should not be considered as a recommendation or product endorsement by Intel Corporation.

Table 14. Retention Mechanism Vendors

Resin Color	Supplier Part Number	"Left Handed" Orientation (Preferred)	"Right Handed" Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

7.2 AGP 2.0

Rev. 2.0 of the AGP Interface Specification enhances the functionality of the original *AGP Interface Specification,* Revision 1.0, by allowing 4X data transfers (four data samples per clock) and 1.5 V operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66 MHz AGP clock, which means that each data cycle is ¼ of a 15 ns (66 MHz) clock, or 3.75 ns. Note that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66 MHz clock cycle, so the data cycle time is 7.5 ns. To allow for such high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data-cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines causes the settling time to be long. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on the AGP (1.5 V) requires even more noise immunity. For example, during 1.5 V operation, V_{ilmax} is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

7.2.1 AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: *1X timing domain signals*, *2X/4X timing domain signals*, and *miscellaneous signals*. Each group has different routing requirements. In addition, within the *2X/4X timing domain signals*, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. However, trace length matching requirements only must be satisfied within each set of 2X/4X timing domain signals. The signal groups are listed in Table 15.

Table 15. AGP 2.0 Signal Groups

Groups	Signal
1X Timing Domain	CLK (3.3 V), RBF#, WBF#, ST[2:0], PIPE#, REQ#, GNT#, PAR, FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#
2X/4X Timing Domain	**Set #1:** AD[15:0], C/BE[1:0]#, AD_STB0, AD_STB0#[1] **Set #2:** AD[31:16], C/BE[3:2]#, AD_STB1, AD_STB1#[1] **Set #3:** SBA[7:0], SB_STB, SB_STB#[1]
Miscellaneous, async.	USB+, USB-, OVRCNT#, PME#, TYPDET#, PERR#, SERR#, INTA#, INTB#

NOTE: These signals are used in 4X AGP mode ONLY.

Table 16. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section the term *data* refers to AD[31:0], C/BE[3:0]#, and SBA[7:0]. The term *strobe* refers to AD_STB[1:0], AD_STB[1:0]#, SB_STB, and SB_STB#. When the term *data* is used, it refers to one of the three sets of data signals, as listed in Table 15. When the term *strobe* is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (*1X timing domain signals*, *2X/4X timing domain signals*, *miscellaneous signals)* will be addressed separately.

7.3 Standard AGP Routing Guidelines

7.3.1 1X Timing Domain Routing Guidelines

7.3.1.1 Flexible Motherboard Guidelines

- The AGP 1X timing domain signals (Table 15) have a maximum trace length of 4 inches for motherboards that support a Graphics Performance Accelerator (GPA) card. This maximum applies to ALL signals listed as 1X timing domain signals in Table 15.

- AGP 1X signals multiplexed with display cache signals (listed below) should be routed with a 1:3 trace width-to-spacing ratio. All other AGP 1X timing domain signals can be routed with 5 mil minimum trace separation.

- There are no trace length matching requirements for 1X timing domain signals.

The following are multiplexed AGP1X signals on flexible motherboards:

- RBF#
- ST[2:0]
- PIPE#
- REQ#
- GNT#
- PAR

- FRAME#
- IRDY#
- TRDY#
- STOP#
- DEVSEL#

7.3.1.2   AGP-Only Motherboard Guidelines

- AGP 1X timing domain signals (Table 17) have a maximum trace length of 7.5 inches for motherboards that will **not** support a Graphics Performance Accelerator (GPA) card. This maximum applies to ALL signals listed as 1X timing domain signals in Table 17.

- All AGP 1X timing domain signals can be routed with 5 mil minimum trace separation.

- There are no trace length matching requirements for 1X timing domain signals.

7.3.2   2X/4X Timing Domain Routing Guidelines

- These trace length guidelines apply to ALL signals listed in Table 15 as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

- The maximum line length and length mismatch requirements depend on the routing rules used on the motherboard. These routing rules were created to provide design freedom by making trade-offs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6 inches) and long AGP interfaces (e.g., > 6 inches and < 7.25 inches) are documented separately. The maximum length allowed for the AGP interface (on AGP-only motherboards) is 7.25 inches.

7.3.2.1   Flexible Motherboard Guidelines

- For motherboards that support either an AGP card or a GPA card in the AGP slot, the maximum length of AGP 2X/4X timing domain signals is 4 inches.

- 1:3 trace width-to-spacing is required for AGP 2X/4X signal traces.

- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 15), within ± 0.5 inch.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 3.7 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 3.2 inches to 4 inches long (since there is a 4 inches max. length). Another strobe set (e.g., SB_STB and SB_STB#) could be 3.1 inches long, so that the associated data signals (e.g., SBA[7:0]) can be 2.6 inches to 3.6 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Since each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in

a strobe pair should be routed using 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length-matched to less than ± 0.1 inch (i.e., a strobe and its complement must be the same length within 0.1 inch).

Figure 37. AGP 2X/4X Routing Example for Interfaces < 6 inches and GPA/AGP Solutions
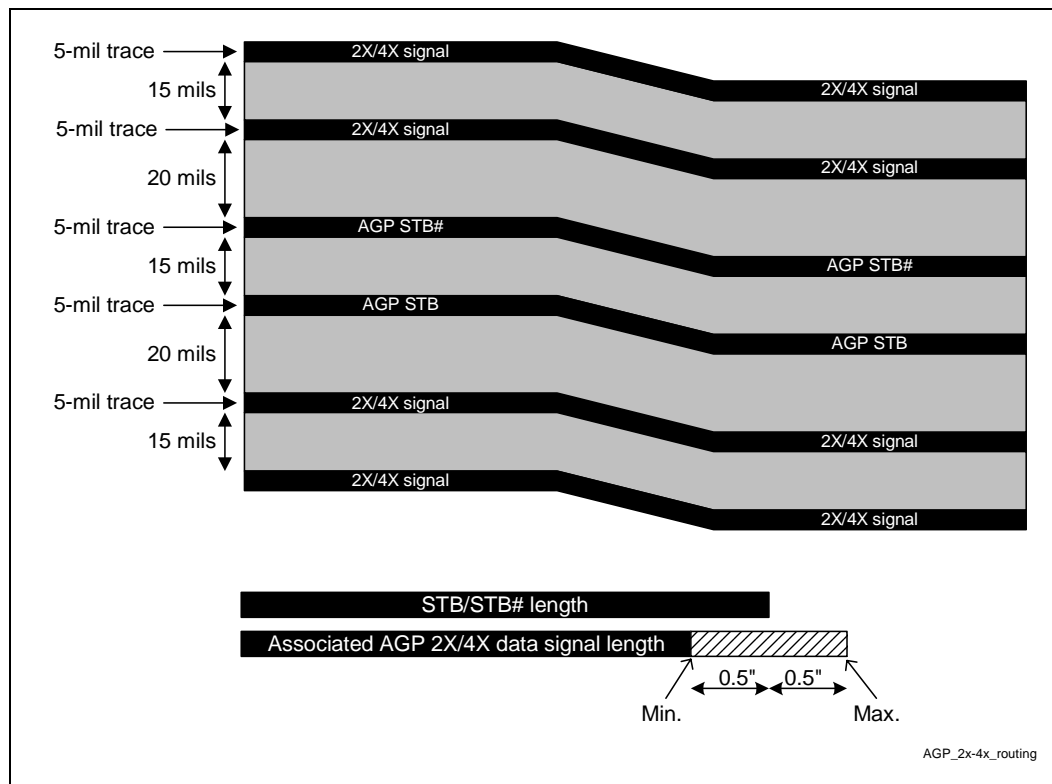
7.3.2.2   AGP-Only Motherboard Guidelines

For motherboards that will not support a GPA card populated in the AGP slot, the maximum AGP 2X/4X signal trace length is 7.25 inches. However, there are different guidelines for AGP interfaces shorter than 6 inches (e.g., all AGP 2X/4X signals are shorter than 6 inches) and those longer than 6 inches but shorter than the 7.25 inches maximum.

AGP Interfaces Shorter Than 6 Inches

The following guidelines are for designs that require less than 6 inches between the AGP connector and the GMCH:

- 1:3 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 15), within ± 0.5 inch.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 4.8 inches to 5.8 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 3.7 inches to 4.7 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length-matched to less than ± 0.1 inches (i.e., a strobe and its complement must be the same length, within 0.1 inches). Refer to Table 15 for an illustration of these requirements.

AGP Interfaces Longer Than 6 Inches

Since longer lines have more crosstalk, they require wider spacing between traces to reduce the skew. The following guidelines are for designs that require more than 6 inches (but less than the 7.25 inches max.) between the AGP connector and the GMCH:

- 1:4 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.

- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 21), within ± 0.125 inches.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 6.475 inches to 6.625 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 6.075 inches to 6.325 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1 inch (i.e., a strobe and its complement must be the same length, within 0.1 inch).

7.3.3   AGP Routing Guideline Considerations and Summary

This section applies to all AGP signals in any motherboard support configuration (e.g., "flexible" or "AGP only"):

- The 2X/4X timing domain signals can be routed with 5 mil spacing when breaking out of the GMCH. The routing must widen to the documented requirements within 0.3 inches of the GMCH package.

- When matching trace lengths for the AGP 4X interface, all traces should be matched from the ball of the GMCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the GMCH package.

- Reduce line length mismatch to ensure added margin. The trace length mismatch for all signals within a signal group should be as close as possible to zero, to provide timing margin.

- To reduce trace-to-trace coupling (i.e., crosstalk), separate the traces as much as possible.

- All signals in a signal group should be routed on the same layer.

- The trace length and trace spacing requirements **must not** be violated by any signal.

Table 17. AGP 2.0 Routing Summary

Signal	Maximum Length	Trace Spacing (5 Mil Traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	7.5 inches [4]	5 mils	No requirement	N/A	None
2X/4X Timing Domain Set 1	7.25 inches [4]	20 mils	±0.125 inch	AD_STB0 and AD_STB0#	AD_STB0 and AD_STB0# must be the same length.
2X/4X Timing Domain Set 2	7.25 inches [4]	20 mils	±0.125 inch	AD_STB1 and AD_STB1#	AD_STB1 and AD_STB1# must be the same length.
2X/4X Timing Domain Set 3	7.25 inches[4]	20 mils	±0.125 inch	SB_STB and SB_STB#	SB_STB and SB_STB# must be the same length.
2X/4X Timing Domain Set 1	6 inches [3]	15 mils[1]	±0.5 inch	AD_STB0 and AD_STB0#	AD_STB0 and AD_STB0# must be the same length.
2X/4X Timing Domain Set 2	6 inches[3]	15 mils[1]	±0.5 inch	AD_STB1 and AD_STB1#	AD_STB1 and AD_STB1# must be the same length.
2X/4X Timing Domain Set 3	6 inches[3]	15 mils[1]	±0.5 inch	SB_STB and SB_STB#	SB_STB and SB_STB# must be the same length.

NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils.
2. These guidelines apply to board stack-ups with 15% impedance tolerance.
3. 4 inches is the maximum length for flexible motherboards.
4. Solution valid for AGP-only motherboards

7.3.4   AGP Clock Routing

The maximum total AGP clock skew, between the GMCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on a clock edge that falls within in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew. (The motherboard designer must determine how the 0.9 ns is allocated between the board and the synthesizer.)

For the Intel 815E platform's AGP clock routing guidelines, refer to

7.3.5   AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for an optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the GMCH. The following guidelines are not intended to replace thorough system validation of products based on the Intel 815E chipset platform:

- A minimum of six 0.01 μF capacitors are required and must be as close as possible to the GMCH. These should be placed within 70 mils of the outer row of balls on the GMCH for VDDQ decoupling. The closer the placement, the better.

- The designer should evenly distribute the placement of decoupling capacitors within the AGP interface signal field.

- It is recommended that the designer use a low-ESL ceramic capacitor (e.g., a 0603 body-type X7R dielectric)

- To add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of the space between traces should be minimal and for as short a distance as possible (1 inch max.).

- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. *In a typical four-layer PCB design, the signals transition from one side of the board to the other.* One extra 0.01 µF capacitor is required per 10 vias. The capacitor should be placed as close as possible to the center of the via field.

The designer should ensure that the AGP connector is well decoupled, as described in the *AGP Design Guide,* Revision 1.0, Section 1.5.3.3.

Figure 38. AGP Decoupling Capacitor Placement Example
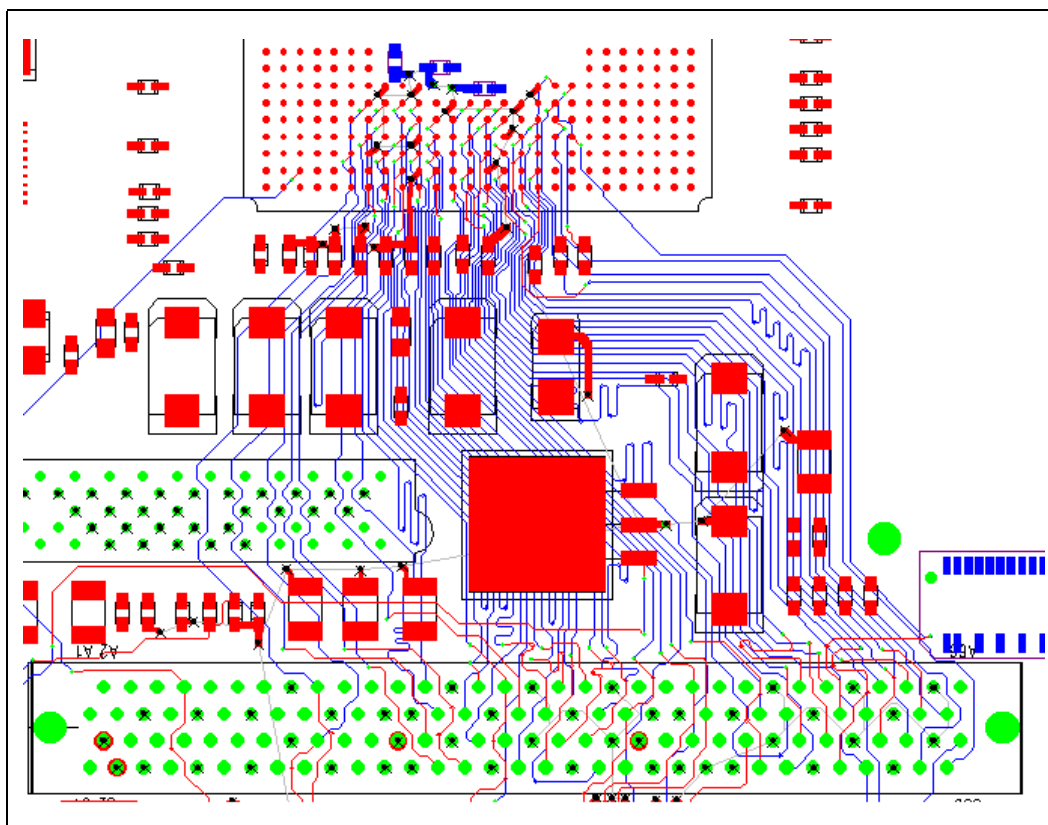
NOTE: This figure is for example purposes only. It does not necessarily represent complete and correct routing for this interface.

7.3.6   AGP Routing Ground Reference

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the GMCH to an AGP connector (or to an AGP video controller if implemented as a "down" solution on an AGP-only motherboard), using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the minimum signal set listed previously, it is strongly recommended that half of all AGP signals be reference to ground, depending on board layout. In an ideal design, the entire AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all designs using the Intel 815E chipset platform.

7.4   AGP Down Routing Guidelines

The routing guidelines in this section are for AGP down implementations with AGP-compliant devices that are implemented directly on the motherboards, eliminating the need for connectors or add-in cards.

7.4.1   1X AGP Down Option Timing Domain Routing Guidelines

Routing guidelines for an AGP device on the motherboard are very similar to those when the device is implemented with an AGP connector.

- AGP 1X timing domain signals (Table 17) have a maximum trace length of 7.5 inches. This maximum applies to ALL signals listed as 1X timing domain signals in Table 17.
- All AGP 1X timing domain signals can be routed with 5 mil minimum trace separation
- There are no trace length matching requirements for 1X timing domain signals

7.4.2   2X/4X AGP Down Timing Domain Routing Guidelines

These trace length guidelines apply to ALL signals listed in Table 15 as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

- The maximum AGP 2X/4X signal trace length is 6 inches.
- 1:3 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.

AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 15), within ±0.5 inch.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) is 5.3 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) could be 4.8 inches to 5.8 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 3.7 inches to 4.7 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed

together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals and all other signals by at least 20 mils (1:4). The strobe pair must be length-matched to less than ± 0.2 inch (i.e., a strobe and its complement must be the same length, within 0.2 inch).

Figure 39. AGP Down 2X/4X Routing Recommendations
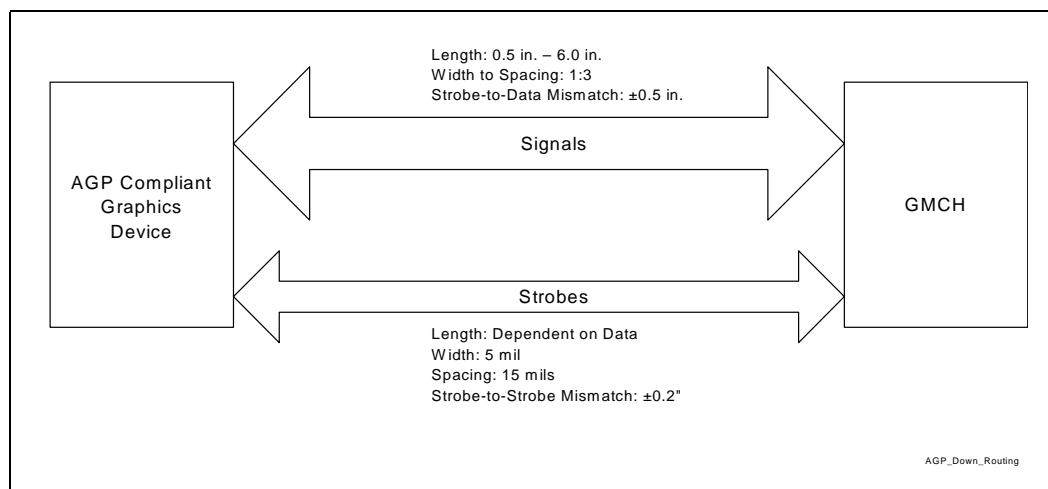
7.4.3   AGP Routing Guideline Considerations and Summary

This section applies to all AGP signals, as follows:

- The 2X/4X timing domain signals can be routed with 5 mil spacing when breaking out of the GMCH. The routing must widen to the documented requirements, within 0.3 inch of the GMCH package.

- When matching the trace length for the AGP 4X interface, all traces should be matched from the ball of the GMCH to the ball on the AGP compliant device. It is not necessary to compensate for the lengths of the AGP signals on the GMCH package.

- Reduce line length mismatch to ensure added margin. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

- To reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible.

- All signals in a signal group should be routed on the same layer.

- The trace length and trace spacing requirements **must not** be violated by any signal.

Table 18. AGP 2.0 Down Routing Summary

Signal	Max. Length	Trace Spacing (5 mil Traces)	Length Mismatch	Relative to	Notes
1X Timing Domain	7.5 inches	5 mils	No requirement	N/A	None
2X/4X Timing Domain Set 1	6 inches	15 mils[1]	±0.5 inch	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set 2	6 inches	15 mils[1]	±0.5 inch	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set 3	6 inches	15 mils[1]	±0.5 inch	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

NOTE: Each strobe pair must be separated from other signals by at least 20 mils.

7.4.4   AGP Clock Routing

The maximum total AGP clock skew, between the GMCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but at all points on the clock edge that fall within the switching range. For AGP clock routing guidelines for the Intel 815E chipset platform, refer to Section 12.3.

7.4.5   AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the GMCH. The following guidelines are not intended to replace thorough system validation for products based on the Intel 815E chipset platform.

- A minimum of six 0.01 µF capacitors are required and must be as close as possible to the GMCH. These should be placed within 70 mils of the outer row of balls on the GMCH for VDDQ decoupling. The closer the placement, the better.

- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.

- It is recommended that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.

- To add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1 inch max.).

- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. On a typical four-layer PCB design, the signals transition from one side of the board to the other. One extra 0.01 µF capacitor is required per ten vias. The capacitor should be placed as close as possible to the center of the via field.

7.4.6 AGP Routing Ground Reference

It is strongly recommended that at least the following critical signals be referenced to ground from the GMCH to an AGP video controller on an AGP-only motherboard using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to this minimum signal set, it is strongly recommended that half of all AGP signals be referenced to ground, depending on the board layout. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all Intel 815E chipset platform designs.

7.5 AGP 2.0 Power Delivery Guidelines

7.5.1 VDDQ Generation and TYPEDET#

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. This voltage is **always** 3.3 V. VDDQ is the interface voltage. In AGP 1.0 implementations, VDDQ also was 3.3 V. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ, since both are tied to the 3.3 V power plane on the motherboard.

AGP 2.0 requires that these power planes be separate. In conjunction with the 4X data rate, the AGP 2.0 Interface Specification provides for low-voltage (1.5 V) operation. The AGP 2.0 specification implements a TYPEDET# (type detect) signal on the AGP connector that determines the operating voltage of the AGP 2.0 interface (VDDQ). The motherboard must provide either 1.5 V or 3.3 V to the add-in card, depending on the state of the TYPEDET# signal (see Table 19). 1.5 V low-voltage operation applies **only** to the AGP interface (VDDQ). VCC is always 3.3 V.

Note: The motherboard provides 3.3 V to the VCC pins of the AGP connector. If the graphics controller needs a lower voltage, then the add-in card must regulate the 3.3VCC voltage to the controller's requirements. The graphics controller may **only** power AGP I/O buffers with the VDDQ power pins.

The TYPEDET# signal indicates whether the AGP 2.0 interface operates at 1.5 V or 3.3 V. If TYPEDET# is floating (i.e., No Connect) on an AGP add-in card, the interface is 3.3 V. If TYPEDET# is shorted to ground, the interface is 1.5 V.

Table 19. TYPDET#/VDDQ Relationship

TYPEDET# (on Add-in Card)	VDDQ (Supplied by MB)
GND	1.5 V
N/C	3.3 V

As a result of this requirement, the motherboard must provide a *flexible* voltage regulator or key the slot to preclude add-in cards with voltage requirements incompatible with the motherboard. This regulator must supply the appropriate voltage to the VDDQ pins on the AGP connector. For specific design recommendations, refer to the schematics in Appendix A. VDDQ generation and AGP VREF generation must be considered together. Before developing VDDQ generation circuitry, refer to this section and the *AGP 2.0 Interface Specification*.

Figure 40. AGP VDDQ Generation Example Circuit
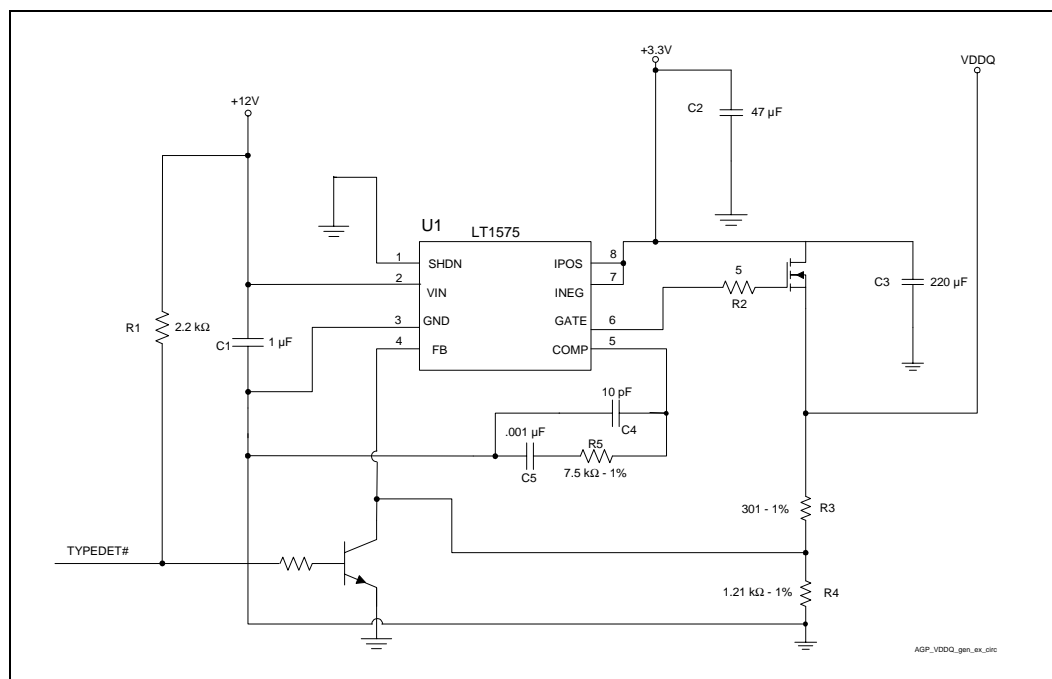
Figure 40 demonstrates **one** way to design the VDDQ voltage regulator. This regulator is a linear regulator with an external, low-Rds_{on} FET. The source of the FET is connected to 3.3 V. This regulator converts 3.3 V to 1.5 V or passes 3.3 V, depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3 V (not 5 V) to control thermals. (i.e., 5 V regulated down to 1.5 V with a linear regulator will dissipate approximately 7 W at 2 A.) Because it must draw power from 3.3 V and, in some situations, must simply pass that 3.3 V to VDDQ (when a 3.3 V add-in card is placed in the system), the regulator MUST use a low-Rds_{on} FET.

AGP 1.0 ECR #44 modified VDDQ 3.3_{min} to 3.1 V. When an ATX power supply is used, the 3.3 V_{min} is 3.168. Therefore, 68 mV of drop is allowed across the FET at 2 A. This corresponds to an FET with an Rds_{on} of 34 mΩ.

How does the regulator switch? The feedback resistor divider is set to 1.5 V. When a 1.5 V card is placed in the system, the transistor is off and the regulator regulates to 1.5 V. When a 3.3 V card is placed in the system, the transistor is on, and the feedback will be pulled to ground. When this happens, the regulator will drive the gate of the FET to nearly 12 V. This will turn on the FET and pass 3.3 V – 2 A * Rds_{on} to VDDQ.

7.5.2 VREF Generation for AGP 2.0 (2X and 4X)

VREF generation for AGP 2.0 is different, depending on the AGP card type used. The 3.3 V AGP cards generate VREF locally. That is, they have a resistor divider on the card that divides VDDQ down to VREF (see Figure 41). To account for potential differences between VDDQ and GND at the GMCH and graphics controller, 1.5 V cards use source-generated VREF. That is, the VREF signal is generated at the graphics controller and sent to the GMCH, and another VREF is generated at the GMCH and sent to the graphics controller (see Figure 41).

Both the graphics controller and the GMCH must generate VREF and distribute it through the connector (1.5 V add-in cards only). The following two pins defined on the AGP 2.0 universal connector allow this VREF passing:

- VREFGC; VREF from the graphics controller to the chipset
- VREFCG; VREF from the chipset to the graphics controller

To preserve the common-mode relationship between the VREF and data signals, the routing of the two VREF signals must be matched in length to the strobe lines, within 0.5 inch on the motherboard and within 0.25 inch on the add-in card.

The voltage divider networks consist of AC and DC elements, as shown in Figure 41.

The VREF divider network should be placed as close as practical to the AGP interface, to get the benefit of the common-mode power supply effects. However, the trace spacing around the VREF signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

During 3.3 V AGP 2.0 operation, VREF must be 0.4 VDDQ. However, during 1.5 V AGP 2.0 operation, VREF must be 0.5 VDDQ. This requires a flexible voltage divider for VREF. Various methods of accomplishing this exist, and one such example is shown in Figure 41.

Figure 41. AGP 2.0 VREF Generation and Distribution

Notes:
1. The resistor dividers should be placed near the GMCH. The AGPREF signal must be 5 mils wide and routed 10 mils from adjacent signals.
2. R7 is the same resistor seen in AGP VDDQ generation example circuit figure (R1).
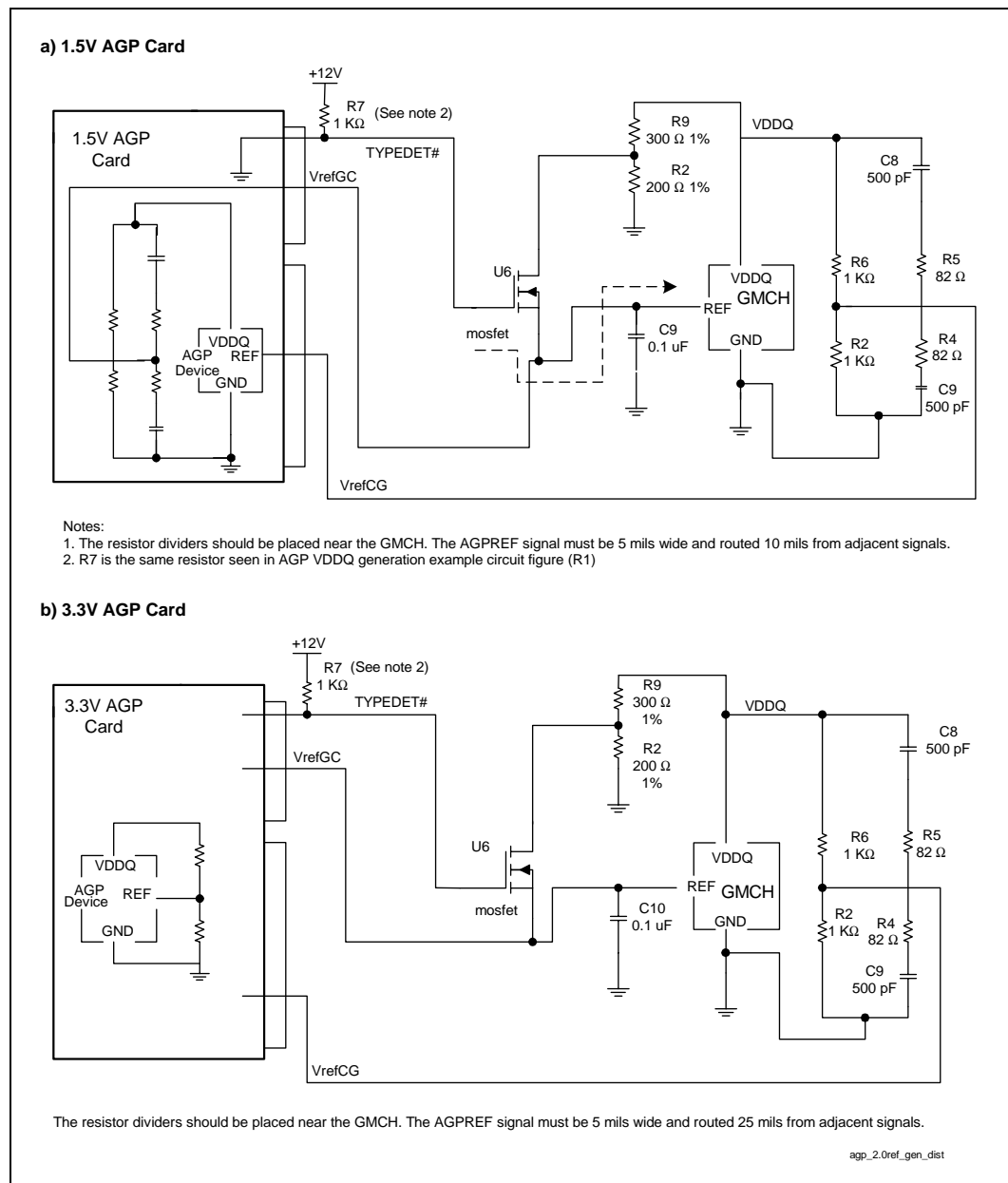
The flexible VREF divider shown in Figure 41 uses a FET switch to switch between the locally generated VREF (for 3.3 V add-in cards) and the source-generated VREF (for 1.5 V add-in cards).

Use of the source-generated VREF at the receiver is optional and is a product implementation issue beyond the scope of this document.

7.6 Additional AGP Design Guidelines

7.6.1 Compensation

The GMCH AGP interface supports resistive buffer compensation (RCOMP). Tie the GRCOMP pin to a 40 Ω, 2% (or 39 Ω, 1%) pull-down resistor (to ground) through a 10 mil-wide, very short (<0.5 inch) trace.

7.6.2 AGP Pull-ups

AGP control signals require pull-up resistors to VDDQ on the motherboard, to ensure that they contain stable values when no agent is actively driving the bus. The pull-up/pull-down resistor value requirements are Rmin = 4 kΩ and Rmax = 16 kΩ. The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

1X Timing Domain Signals Requiring Pull-up Resistors

The following bullets list the 1X timing domain signals that require pull-up resistors.

- FRAME#
- TRDY#
- IRDY#
- DEVSEL#
- STOP#
- SERR#
- ST[2:0]

- PERR#
- RBF#
- PIPE#
- REQ#
- WBF#
- GNT#

Note: It is **critical** that these signals be pulled up to VDDQ, not 3.3 V.

The trace stub to the pull-up resistor on 1X timing domain signals should be kept shorter than 0.5 inch to avoid signal reflections from the stub.

Note: INTA# and INTB# should be pulled to 3.3 V, not VDDQ.

2X/4X Timing Domain Signals Requiring Pull-Up/Pull-Down Resistors

The following bullets list the 2X/4X timing domain signals that require pull-up/pull-down resistors. The strobe signals require pull-up/pull-downs on the motherboard to ensure that they are at a stable level when no agent is driving the bus.

- AD_STB[1:0]Pull-Up to VDDQ
- SB_STBPull up to VDDQ
- AD_STB[1:0]#Pull Down to Ground
- SB_STB#Pull Down to Ground

The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept shorter than 0.1 inch to avoid signal reflections from the stub.

7.6.2.1   AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3 V tolerant during 1.5 V operation:

- PME#
- INTA#
- INTB#
- GPERR#
- GSERR#
- CLK
- RST

The following signals on the AGP interface are 5 V tolerant (see USB specification):

- USB+
- USB-
- OVRCNT#

The following signal is a special AGP signal. It is either grounded or left as a no connect on an AGP card.

- TYPEDET#

Note: All other signals on the AGP interface are in the VDDQ group. They are not 3.3 V tolerant during 1.5 V AGP operation!

7.7   Motherboard / Add-in Card Interoperability

There are three AGP connectors: *3.3V AGP connector, 1.5 V AGP connector*, and *Universal AGP connector*. To maximize add-in flexibility, it is highly advisable to implement the universal connector in systems based on the Intel 815E platform. All add-in cards are *either* 3.3 V or 1.5 V cards. The 4X transfers at 3.3 V are not allowed due to timings.

Table 20. Connector/Add-in Card Interoperability

Card	1.5 V Connector	3.3 V Connector	Universal Connector
1.5 V card	Yes	No	Yes
3.3 V card	No	Yes	Yes

Table 21. Voltage/Data Rate Interoperability

Voltage	1X	2X	4X
1.5 V VDDQ	Yes	Yes	Yes
3.3 V VDDQ	Yes	Yes	No

7.8 AGP/Display Cache Shared Interface

As described earlier, the AGP and display cache interfaces of the Intel 815E chipset platform are multiplexed or shared. In other words, the same component pins (balls) are used for both interfaces, although obviously only one interface can be supported at any given time. As a result, almost all display cache interface signals are mapped onto the new AGP interface. The Intel 815E platform can be configured in either AGP mode or Graphics mode. In the AGP mode, the interface supports a full AGP 4X interface. In the Graphics mode, the interface becomes a display cache interface similar to the Intel® 810E chipset. Note, however, that in the Graphics mode, the display cache is optional. There do not have to be any SDRAM devices connected to the interface. The only dedicated display cache signals are OCLK and RCLK, which need not connect directly to the SDRAM devices. These are not mapped onto existing AGP signals.

7.8.1 GPA Card Considerations

To support the fullest flexibility, the display cache exists on an add-in card (Graphics Performance Accelerator, or GPA) that complies with the AGP connector form factor. If the motherboard designer follows the flexible routing guidelines for the AGP interface detailed in previous sections, the customer can choose to populate the AGP slot in a system based on the Intel 815E chipset with either an AGP graphics card, with a GPA card to enable the highest-possible internal graphics performance, or with nothing to get the lowest-cost internal graphics solution. Some of the GPA/ Intel 815E chipset platform interfacing implications are listed below. For a complete description of the GPA card design, refer to the *Graphics Performance Accelerator Card Specification* available from Intel.

- A strap is required to determine which frequency to select for display cache operation. This is the L_FSEL pin of the GMCH. The GPA card will pull this signal up or down as appropriate to communicate to the Intel 815E chipset platform the appropriate operating frequency. The Intel 815E chipset platform will sample this pin on the deasserting edge of reset.

- Since current SDRAM technology is always 3.3 V rather than the 1.5 V option also supported by AGP, the GPA card should set the TYPEDET# signal correctly to indicate that it requires a 3.3 V power supply. Furthermore, the GPA card should have only the 3.3 V key and not the 1.5 V key, thereby preventing it from being inserted into a 1.5 V-only connector.

- The pad buffers on the chip will be the normal AGP buffers and will work for both interfaces.

- In internal graphics mode, the AGPREF signal, which is required for the AGP mode, should remain functional as a reference voltage for sampling 3.3 V LMD inputs. The voltage level on AGPREF should remain exactly the same as in the AGP mode, as opposed to the VCC/2 used for previous products.

7.8.1.1 AGP and GPA Mechanical Considerations

The GPA card will be designed with a notch on the PCB to go around the AGP universal retention mechanism. To guarantee that the GPA card will meet all shock and vibration requirements of the system, the AGP universal retention mechanism will be required on all AGP sockets that are to support a GPA card.

7.8.2 Display Cache Clocking

The display cache is clocked source-synchronously from a clock generated by the GMCH. The display cache clocking scheme uses three clock signals.

- **LTCLK** clocks the SDRAM devices, is muxed with an AGP signal, and should be routed according to the flexible AGP guidelines.

- **LOCLK and LRCLK** clock the input buffers of the platform. LOCLK is an output of the GMCH and is a buffered copy of LTCLK. LOCLK should be connected to LRCLK at the GMCH, with a length of PCB trace to create the appropriate clock skew relationship between the clock input (LRCLK) and the SDRAM capacitor clock input(s).

The guidelines are illustrated in Figure 42.

Figure 42. Display Cache Input Clocking
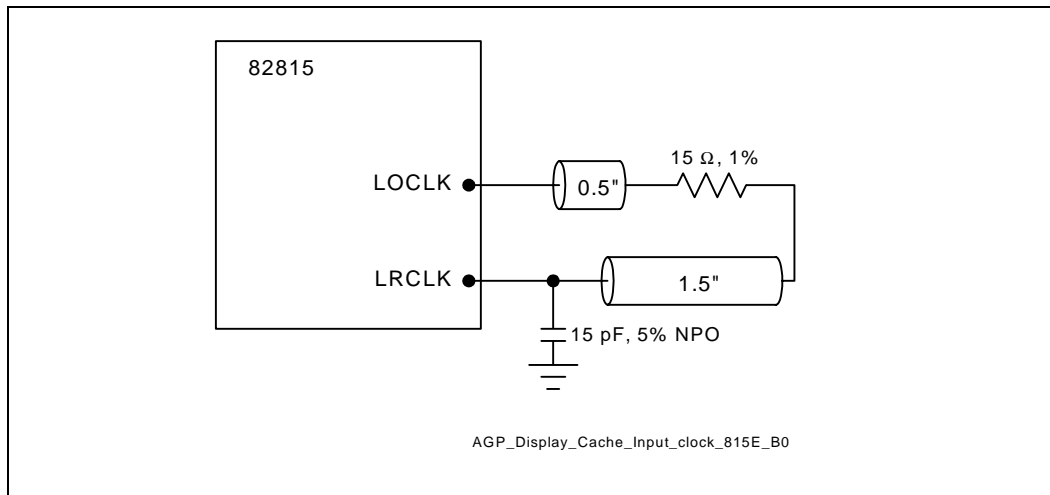
The capacitor should be placed as close as possible to the GMCH LRCLK pin. To minimize skew variation, we recommend a 1% series termination resistor and a 5% NPO capacitor, to stabilize the value across temperatures. In addition to the 15 Ω, 1% resistor and the 15 pF, 5% NPO capacitor. The following combination also can be used: 10 Ω, 1% and 22 pF, 5% NPO.

7.9   Designs That Do Not Use the AGP Port

Intel 815E chipset platform designs that do not use the AGP port should terminate the AGP pins of the GMCH. Except for the GPAR pin (which requires a 100 KΩ pull down resistor to ground), the pull-up or pull-down resistor value should be 8.2 KΩ. Any external graphics implementation not using the AGP port should terminate the GMCH AGP control and strobe signals as recommended in Section 14.3.2.

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Integrated Graphics Display Output   8

8.1   Analog RGB/CRT

8.1.1   RAMDAC/Display Interface

Figure 43 shows the interface of the RAMDAC analog current outputs with the display. Each DAC output is doubly terminated with a 75 Ω resistance. One 75 Ω resistance is from the DAC output to the board ground and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC output is 37.5 Ω. The output current of each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also an LC pi-filter that is used to reduce high-frequency glitches and noise and to reduce EMI. To maximize performance, the filter impedance, cable impedance, and load impedance should be the same. The LC pi-filter consists of two 3.3 pF capacitors and a ferrite bead with a 75 Ω impedance at 100 MHz. The LC pi-filter is designed to filter glitches produced by the RAMDAC while maintaining adequate edge rates to support high-end display resolutions.

Figure 43. Schematic of RAMDAC Video Interface

Diodes D_1, D_2 are clamping diodes with low leakage and low capacitive loading. An example is: California Micro Devices' PActive® 6 Channel ESD Protection Array.

In addition to the termination resistance and LC pi-filter, there are protection diodes connected to the RAMDAC outputs to help prevent latch-up. The protection diodes must be connected to the same power supply rails as the RAMDAC. An LC filter is recommended for connecting the segmented analog 1.85 V power plane of the RAMDAC to the 1.85 V board power plane. The LC filter should be designed for a cut-off frequency of 100 kHz.

8.1.2   Reference Resistor (Rset) Calculation

The full-swing video output is designed to be 0.7 V, according to the VESA video standard. With an equivalent DC resistance of 37.5 Ω (two 75 Ω resistors in parallel; one 75 Ω termination on the board and one 75 Ω termination within the display), the full-scale output current of a RAMDAC channel is 0.7/37.5 Ω = 18.67 mA. Since the RAMDAC is an 8-bit current-steering DAC, this full-scale current is equivalent 255 I, where I is a unit current. Therefore, the unit current or LSB current of the DAC signals equals 73.2 μA. The reference circuitry generates a voltage across this R_{set} resistor equal to the bandgap voltage divided by three (i.e., 407.6 mV). The RAMDAC reference current generation circuitry is designed to generate a 32-I reference current using the reference voltage and the R_{set} value. To generate a 32-I reference current for the RAMDAC, the reference current setting resistor, R_{set}, is calculated from the following equation:

Equation 1. R_{set} = VREF / 32*I = 0.4076 V / 32 * 73.2 μA = 174 Ω

8.1.3   RAMDAC Board Design Guidelines

Figure 44 shows a general cross section of a typical four-layer board. The recommended RAMDAC routing for a four-layer board is such that the red, green, and blue video outputs are routed on the top (bottom) layer over (under) a solid ground plane to maximize the noise rejection characteristics of the video outputs. It is essential to prevent toggling signals from being routed next to the video output signals to the VGA connector. A 20 mil spacing between any video route and any other route is recommended.

Figure 44. Cross-Sectional View of a Four-Layer Board
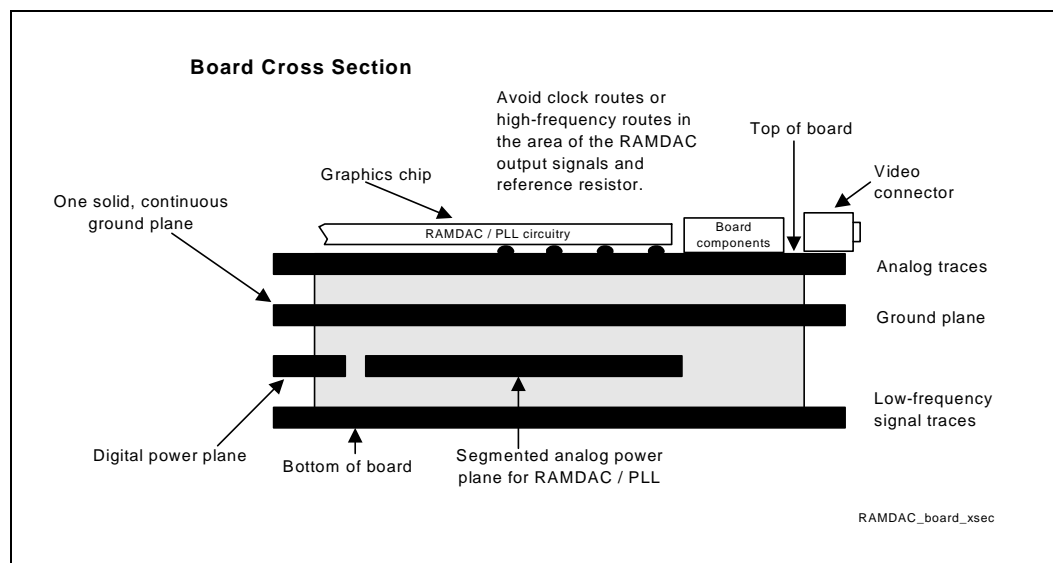
Matching of the video routes (i.e., red, green, blue) from the RAMDAC to the VGA connector is also essential. The routing for these signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends, and jogs).

Figure 45 shows the recommended RAMDAC component placement and routing. The termination resistance can be placed anywhere along the video route from the RAMDAC output to the VGA connector, as long as the trace impedances are designed as indicated in Figure 45. It is advisable to place the pi-filters in close proximity with the VGA connector, to maximize the EMI filtering

effectiveness. The LC filter components for the RAMDAC/PLL power plane, the decoupling capacitors, the latch-up protection diodes, and the reference resistor should be placed in close proximity with the respective pins. Figure 45 shows the recommended reference resistor placement and the ground connections.

Figure 45. Recommended RAMDAC Component Placement and Routing
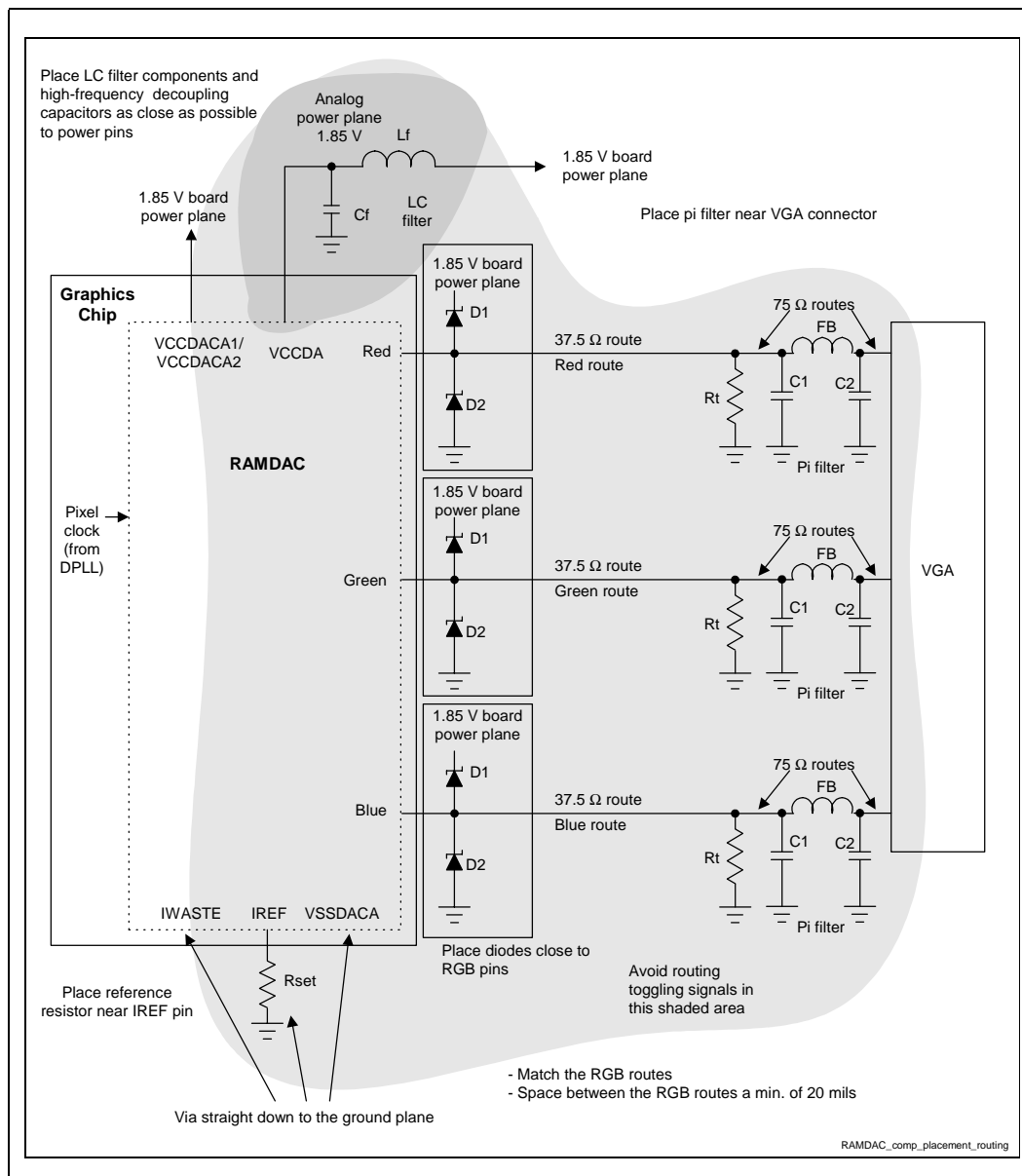
Diodes D_1, D_2 are clamping diodes with low leakage and low capacitive loading. An example is: California Micro Devices' PActive® 6 Channel ESD Protection Array.

Figure 46. Recommended RAMDAC Reference Resistor Placement and Connections
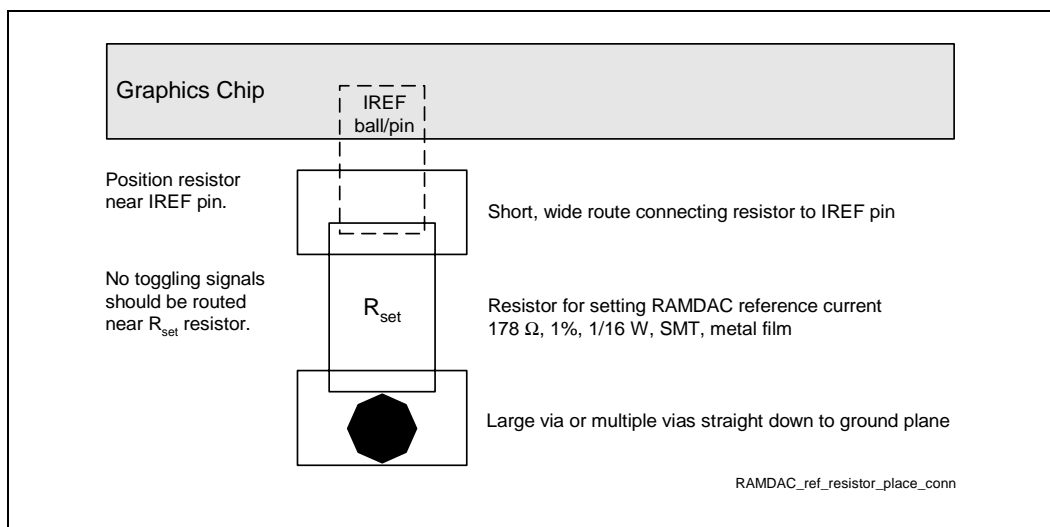
8.1.4 RAMDAC Layout Recommendations

- The primary concern with regard to the RGB signal length is that the RGB routes are matched and routed with the correct impedance. The impedance should be 37.5 Ω, single-ended trace to the 75 Ω, termination resistor. Routing from the 75 Ω resistor to the video PI-filter and to the VGA connector should be 75 Ω impedance.

- The trace width for the RGB signal should be selected for a 37.5 Ω impedance (single-ended route) to the 75 Ω termination resistor. The 75 Ω termination resistor should be placed near the VGA connector.

- The spacing for each DAC channel routing (i.e., between red & green, green & blue outputs) should be a minimum of 20 mils.

- The space between the RGB signal route and other routes should be a minimum of 20 mils for each DAC route.

- All RGB signals should be referenced to ground.

- The trace width for the HSYNC and VSYNC signal routes should be selected for an approximately 40 Ω impedance.

- The spacing between the HSYNC /VSYNC signal routes should be at least 10 mils, preferably 20 mils.

- The space between HSYNC/VSYNC signal routes and others routes should be at least 10 mils, preferably 20 mils.

- Route the HSYNC and VSYNC over the ground plane, if possible. The HSYNC and VSYNC signals should not route over or near any clock signals or any other high switching routing.

8.1.5 HSYNC/VSYNC Output Guidelines

The Hsync and Vsync output of the GMCH may exhibit up to 1.26 V P-P noise when driven high under high traffic system memory conditions. To minimize this, the following is required.

- Add External Buffers to Hsync and Vsync.
  - Examples include: Series 10 Ω resistor with a 74LVC08

8.2 Digital Video Out

The Digital Video Out (DVO) port is a scaleable, low-voltage interface that ranges from 1.1 V to 1.8 V. This DVO port interfaces with a discrete TV encoder to enable platform support for TV-Out, with a discrete TMDS transmitter to enable platform support for DVI-compliant digital displays, or with an integrated TV encoder and TMDS transmitter.

The GMCH DVO port controls the video front-end devices via an I^2C interface, by means of the LTVDA and LTVCK pins. I^2C is a two-wire communications bus/protocol. The protocol and bus are used to collect EDID (extended display identification) from a digital display panel and to detect and configure registers in the TV encoder or TMDS transmitter chips.

8.2.1 DVO Interface Routing Guidelines

Route data signals (LTVDATA[11:0]) with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the GMCH, the DVO data signals can be routed with a trace width of 5 mils and a trace spacing of *5* mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH component. The maximum trace length for the DVO data signals is 7 inches. These signals should each be matched within ±0.1 inch of the LTVCLKOUT[1] and LTVCLKOUT[0] signals.

Route the LTVCLKOUT[1:0] signals 5 mils wide and 20 mils apart. This signal pair should be a minimum of 20 mils from any adjacent signals. The maximum length for LTVCLKOUT[1:0] is 7 inches and the two signals should be the same length.

8.2.2 DVO I^2C Interface Considerations

LTVDA and LTVCK should be connected to the TMDS transmitter, TV encoder or integrated TMDS transmitter/TV encoder device, as required by the specifications for those devices. LTVDA and LTVCK also should be connected to the DVI connector as specified by the DVI specification. Pull-up resistors of 4.7 kΩ (or pull-ups with the appropriate value derived from simulation) are required on both LTVDA and LTVCK.

8.2.3 Leaving the DVO Port Unconnected

If the motherboard does not implement any of the possible video devices with the Intel 815E chipset platform's DVO port, the following are recommended on the motherboard:

- Pull up LTVDA and LTVCK with 4.7 kΩ resistors at the GMCH. This will prevent the GMCH's DVO controller from confusing noise on these lines with false I^2C cycles.

- Route LTVDATA[11:0] and LTVCLKOUT[1:0] out of the BGA to test points for use by automated test equipment (if required). These signals are part of one of the GMCH XOR chains.

Hub Interface 9

The GMCH ball assignment and ICH2 ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals be routed directly from the GMCH to the ICH2 on the top signal layer. Refer to Figure 47.

The hub interface is divided into two signal groups: data signals and strobe signals.

- Data Signals:
    HL[10:0]

- Strobe Signals:
    HL_STB
    HL_STB#

Note: HL_STB/HL_STB# is a differential strobe pair.

No pull-ups or pull-downs are required on the hub interface. HL11 on the ICH2 should be brought out to a test point for NAND Tree testing. Each signal should be routed such that it meets the guidelines documented for its signal group.

Figure 47. Hub Interface Signal Routing Example
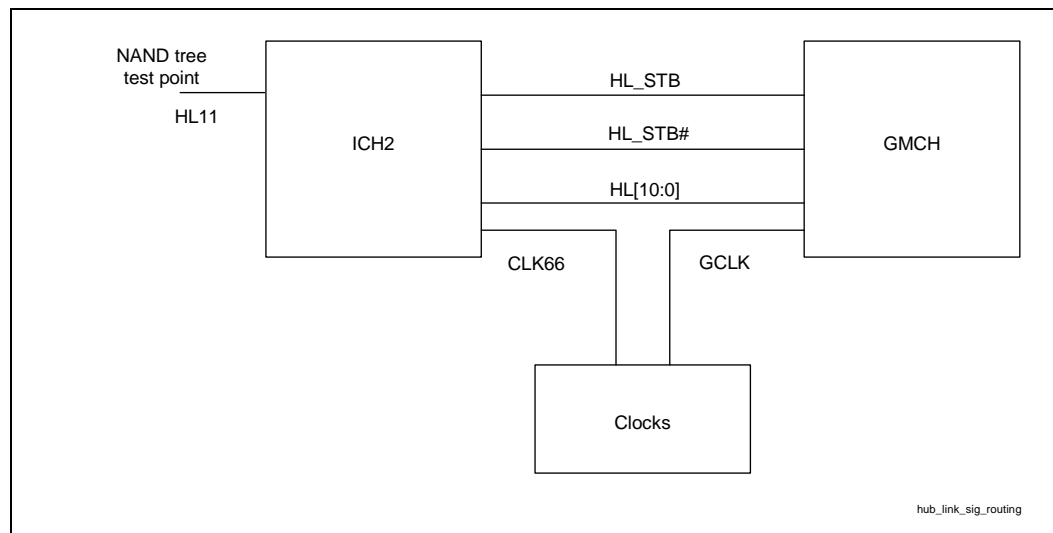
9.1   Data Signals

Hub interface data signals should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the GMCH and the ICH2, the hub interface data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH/ICH2 components.

The maximum trace length for the hub interface data signals is 8 inches. These signals should each be matched within ±0.1 inch of the HL_STB and HL_STB# signals.

9.2 Strobe Signals

- Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 8 inches, and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes, within ±0.1 inch.

9.3 HREF Generation/Distribution

HREF, the hub interface reference voltage, is $0.5 * 1.85$ V $= 0.92$ V $\pm 2\%$. It can be generated using a single HREF divider or locally generated dividers (as shown Figure 48 and Figure 49). The resistors should be equal in value and rated at 1% tolerance, to maintain 2% tolerance on 0.92 V. The values of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from a minimum of 100 Ω to a maximum of 1 kΩ (300 Ω shown in example).

The single HREF divider should not be located more than 4 inches away from either GMCH or ICH2. If the single HREF divider is located more than 4 inches away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor must be close to the component HREF pin.

9.4 Compensation

Independent hub interface compensation resistors are used by the GMCH and ICH2 to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet* and the *Intel® 82801BA I/O Controller Hub* (ICH2*) and Intel® 82801BAM I/O Controller Hub (ICH2-M) Datasheet* for details on compensation. The resistive Compensation (RCOMP) guidelines are as follows:

RCOMP: Tie the HLCOMP pin of each component to a 40 Ω, 1% or 2% pull-up resistor (to 1.8 V) via a 10 mil-wide, 0.5 inch trace (targeted at a nominal trace impedance of 40 Ω). The GMCH and ICH2 each require its own RCOMP resistor.

Figure 48. Single Hub Interface Reference Divider Circuit
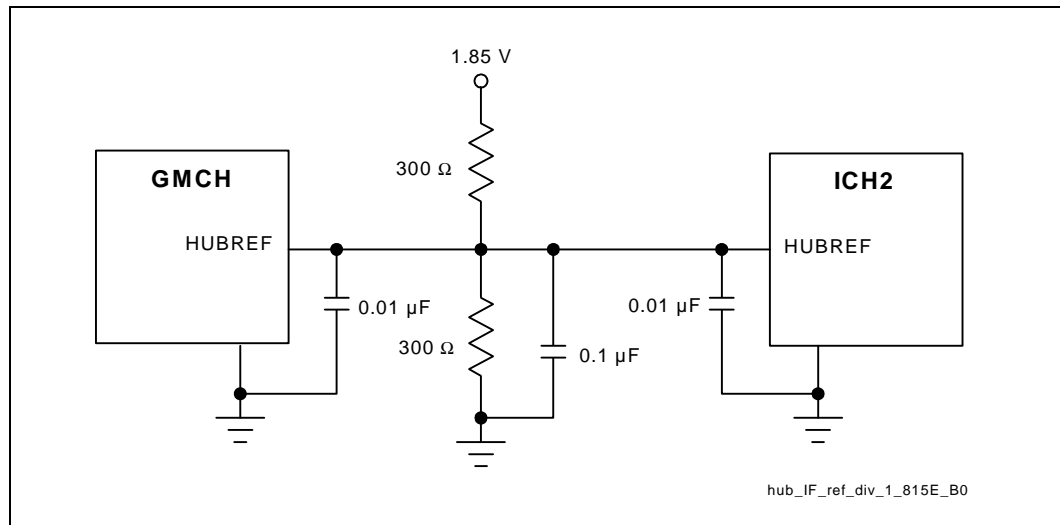
Figure 49. Locally Generated Hub Interface Reference Dividers

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I/O Controller Hub 2 (ICH2) **10**
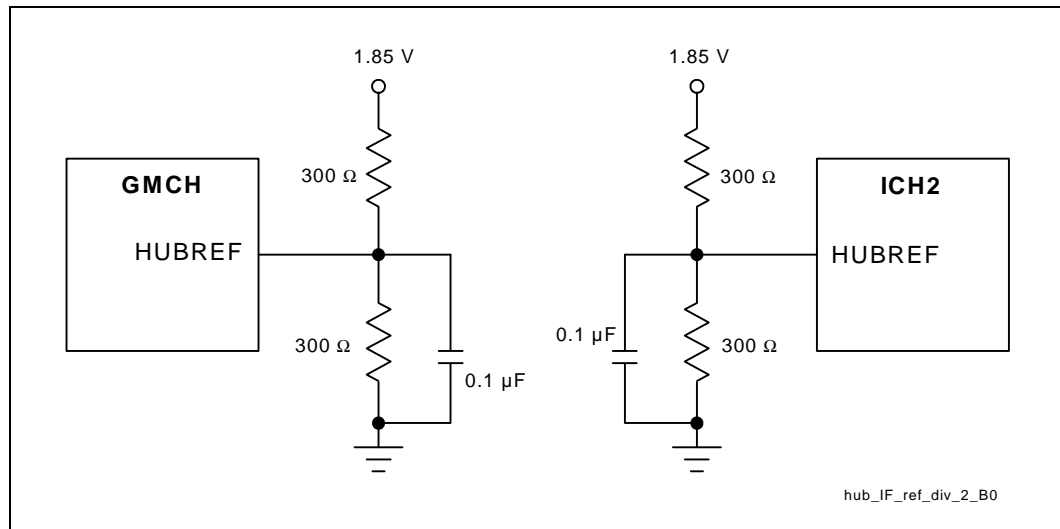
10.1 Decoupling

The ICH2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 22 to ensure that the component maintains stable supply voltages. The capacitors should be placed as close as possible to the package, without exceeding 400 mils (200 mils nominal).

Note: Routing space around the ICH2 is tight. A few decoupling caps may be placed more than 300 mils away from the package. System designers should simulate the board to ensure that the correct amount decoupling is implemented. Refer to Figure 50 for a layout example, with the decoupling capacitors circled with an arrow showing which power plane/trace they are connected to. Intel recommends that, for prototype board designs, the designer include pads for extra power plane decoupling capacitors.

Table 22. Decoupling Capacitor Recommendation

Power Plane/Pins	Decoupling Capacitors	Capacitor Value
3.3 V core	6	0.1 µF
3.3 V standby	1	0.1 µF
Processor interface (1.3 ~ 2.5 V)	1	0.1 µF
1.85 V core	2	0.1 µF
1.85 V standby	1	0.1 µF
5 V reference	1	0.1 µF
5 V reference standby	1	0.1 µF

Figure 50. ICH2 Decoupling Capacitor Layout

10.2   1.85 V/3.3 V Power Sequencing

The ICH2 has two pairs of associated 1.85 V and 3.3 V supplies. These are, {VCC1_85, VCC3_3} and {VCCSus1_85, VCCSus3_3}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.85 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.85 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violation of the 2 V Rule is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.85 V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.85 V logic is powered up. Some signals that are defined as input-only actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.85 V supply is not.

Figure 51 shows an example power-on sequencing circuit that ensures the 2 V Rule is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.85 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.85 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.85 V plane, current will not flow from the 3.3 V supply into 1.85 V plane when the 1.85 V plane reaches 1.85 V.

Figure 51. 1.85 V/3.3 V Power Sequencing Circuit Example
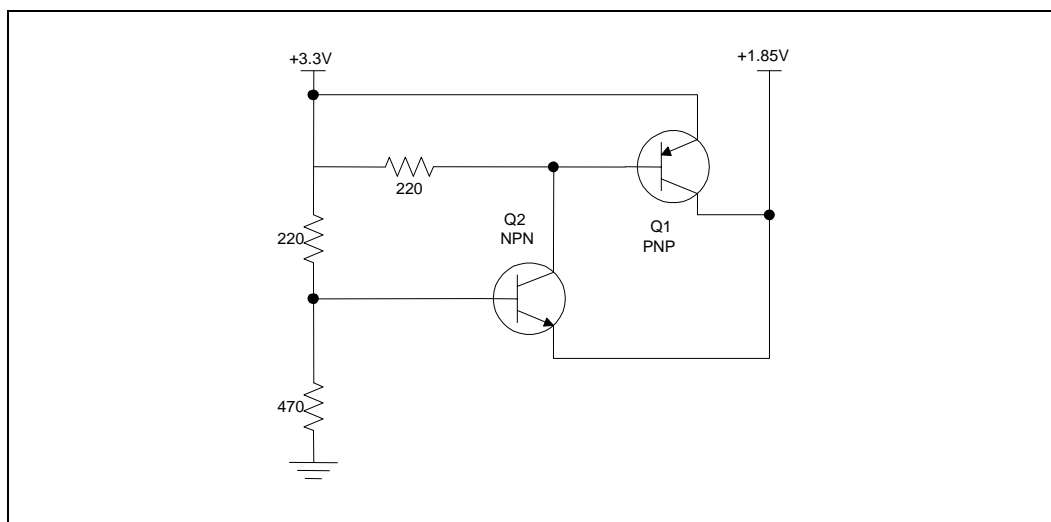
When analyzing systems that may be marginally compliant to the 2 V Rule, pay close attention to the behavior of the ICH2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

10.3   Power Sequencing on Wake Events

Special handling of wake events is required. When a wake event is triggered, the GMCH and the Intel CK-815 must not sample BSEL[1:0] until the signal VTT_PWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the Intel CK-815-compliant clock driver until schematic signal VTT_PWRGD12 is asserted.

2. Clocks to the ICH2 stabilize before the power supply asserts PWROK to the ICH2. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus, it is necessary to gate PWROK to the ICH2 from the power supply while the Intel CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.

3. ICH2 takes the GMCH out of reset.

4. GMCH samples BSEL[1:0]. (Intel CK-815 will have sampled BSEL[1:0] much earlier.)

Refer to Section 4.3 for full implementation details.

10.4 Power Plane Splits

Figure 52. Power Plane Split Example

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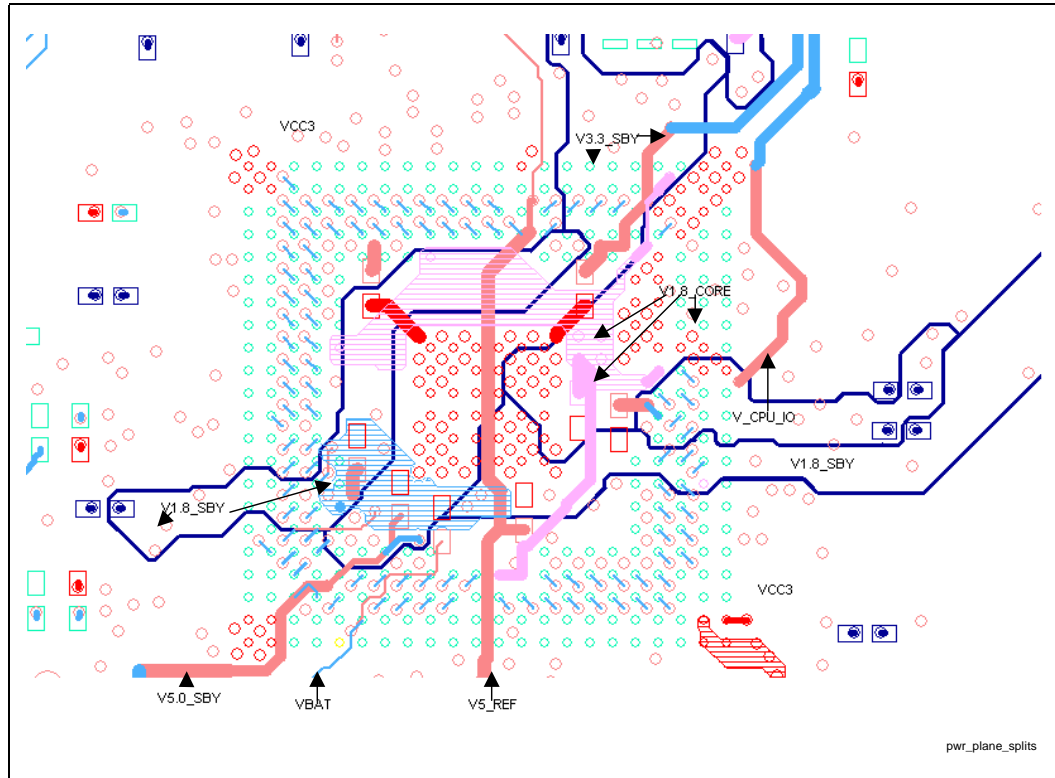
I/O Subsystem 11

This chapter provides guidelines for connecting and routing the IDE, AC'97, USB, IO-APIC, SMBus, PCI, LPC/FWH, and RTC subsystems.

11.1   IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement and signal termination for both IDE channels. The ICH2 has integrated the series resistors that typically have been required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. Intel does not anticipate requiring additional series termination, but OEMs should verify the motherboard signal integrity via simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by providing future stuffing options.

The IDE interface can be routed with 5 mil traces on 7 mil spaces and must be less than 8 inches long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inch shorter than the longest IDE signal (on that channel).

11.1.1   Cabling

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the connector next closest to the end of the cable (6 inches away from the end of the cable).
- **Grounding:** Provide a direct, low-impedance chassis path between the motherboard ground and hard disk drives.
- **ICH2 Placement:** The ICH2 must be placed at most 8 inches from the ATA connector(s).

11.2   Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE controller supports PIO, multiword (8237-style) DMA, and Ultra DMA modes 0 through 5. The ICH2 must determine the type of cable present, to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal' etc. All ground wires are tied together on the cable (and they are tied to the ground

on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049, which is obtainable from the Small Form Factor Committee.

To determine whether the ATA/66 or ATA/100 mode can be enabled, the ICH2 requires that the system software attempt to determine the type of cable used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination host-side/device-side detection mechanism. Note that host-side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the device-side detection mechanism only.

11.2.1   Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-4 Standard*, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 53. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. Not all GPI and GPIO pins on the ICH2 are 5 V tolerant. If non 5 V tolerant inputs are used, a resistor divider is required to prevent 5 V on the ICH2 or FWH pins. The proper value of the divider resistor is 10 kΩ (as shown in Figure 53).

Figure 53. Combination Host-Side / Device-Side IDE Cable Detection
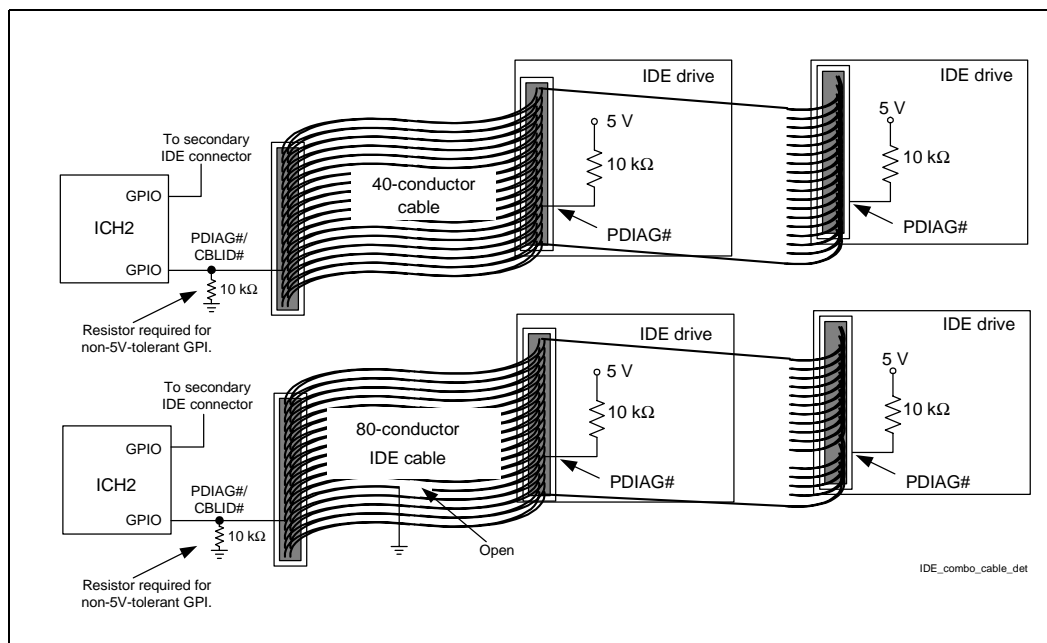
This mechanism allows BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is High, then there is 40-conductor cable in the system and ATA modes 3, 4 and 5 must not be enabled.

If PDIAG#/CBLID# is detected Low, then there may be an 80-conductor cable in the system or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the **Identify Device** information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13, is set to 1, then an 80-conductor cable is present. If this bit is set to 0, then a legacy slave (Device 1) is preventing proper cable detection, so BIOS should configure the system as though a 40-conductor cable were present and then notify the user of the problem.

11.2.2 Device-Side Cable Detection

For platforms that must implement device-side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 54. This capacitor **should not be populated** when implementing the recommended combination host-side/device-side cable detection mechanism described previously.

Figure 54. Device-Side IDE Cable Detection
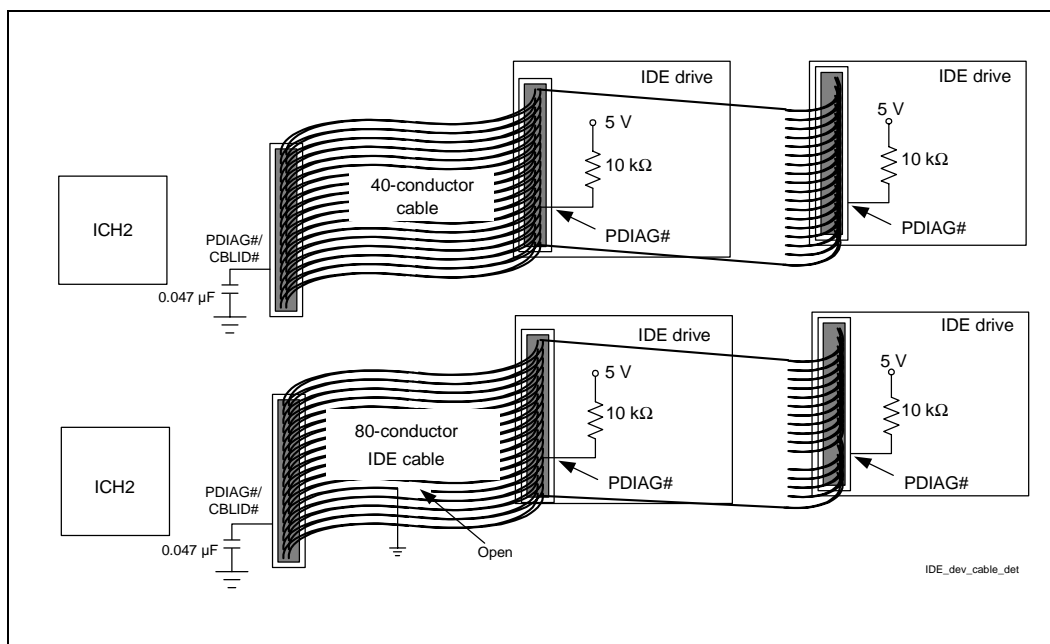
This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4 or 5 drive will drive PDIAG#/CBLID# Low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host, so the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host, so the signal will rise more slowly as the capacitor charges. The drive can detect the difference in rise times and will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot, as described in the ATA/66 specification.

11.2.3 Primary IDE Connector Requirements

Figure 55. Connection Requirements for Primary IDE Connector
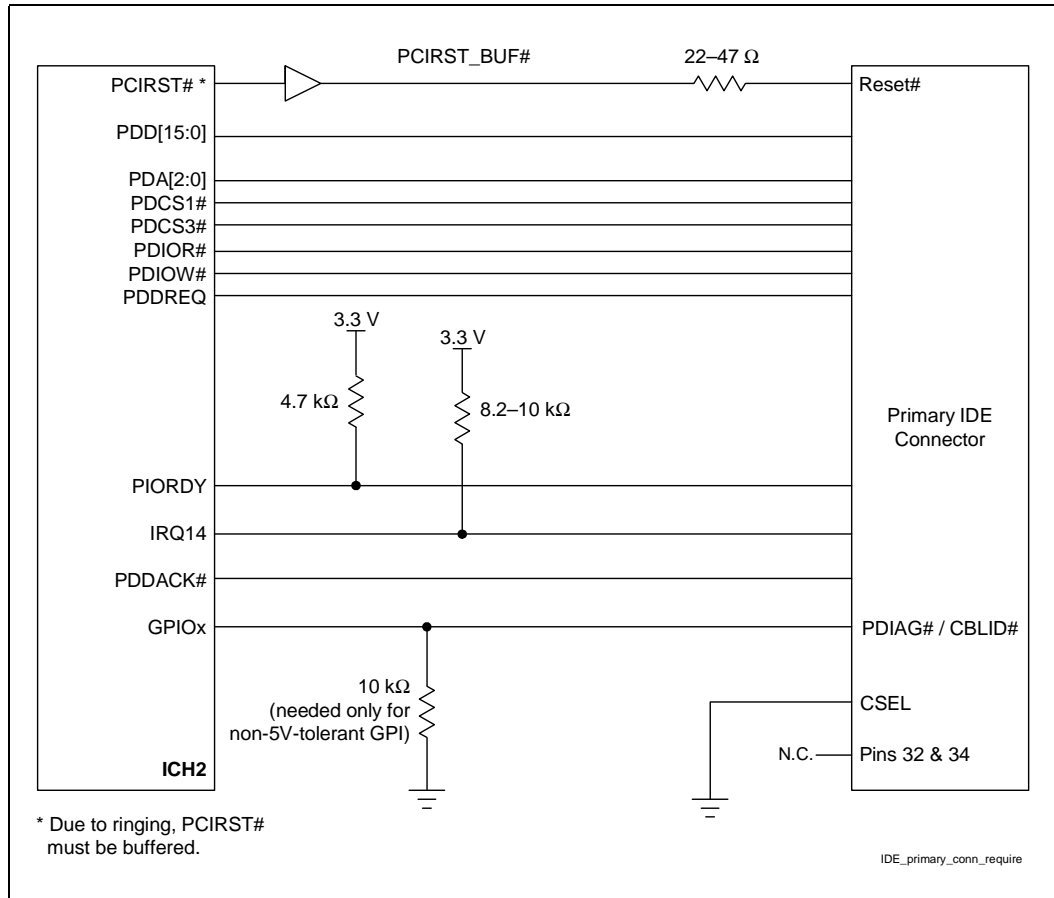
NOTES:
1. 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.
3. A 4.7 kΩ pull-up resistor to VCC3 is required on PIORDY and SIORDY.
4. Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close as possible to the connector. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

11.2.4   Secondary IDE Connector Requirements

Figure 56. Connection Requirements for Secondary IDE Connector

NOTES:
1. 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.
3. A 4.7 kΩ pull-up resistor to VCC3 is required on PIORDY and SIORDY
4. Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close as possible to the connector. Values are determined for each unique motherboard design.

The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

11.3   AC'97

The ICH2 implements an AC'97 2.1-compliant digital controller. Any codec attached to the ICH2 AC-link must be AC'97 2.1 compliant, as well. Contact your codec IHV for information on 2.1-compliant products. For information on the *AC'97 2.1 Specification*, see Section 1.2, *"Reference Documents."*

The AC-link is a bidirectional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, by employing a time-division-multiplexed (TDM) scheme. The AC-link architecture enables data transfer through individual frames transmitted serially. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. Figure 57 shows a two-codec topology of the AC-link for the ICH2.

Figure 57. ICH2 AC'97– Codec Connection
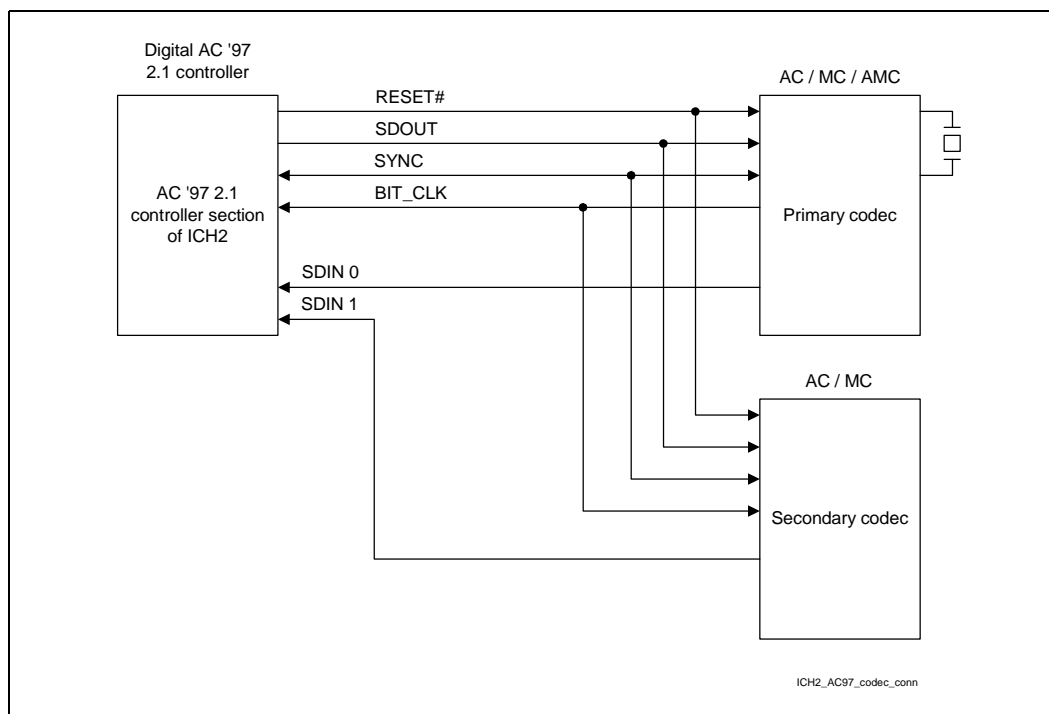
Intel has developed an advanced common connector for both AC'97 as well as networking options. This is known as the Communications and Network Riser (CNR). Refer to Section 11.3.1.

The AC'97 interface can be routed using 5 mil traces with 5 mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14 inches in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC'LINK. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2) and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH2 supports wake-on-ring from S1-S5 via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH2 has weak pull-downs/pull-ups that are enabled only when the AC-Link Shut-off bit in the ICH2 is set. This keeps the link from floating when the AC-link is off or when there are no codecs present.

If the Shut-off bit is not set, it means that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH2, respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, it may be assumed that there is at least one codec. If there is one or no codec onboard, then the unused AC_SDIN pin(s) should have a weak (10 kΩ) pull-down to keep it from floating.

11.3.1 Communications Network Riser (CNR)

For related documents on the Communication Network Riser, refer to the Communication Network Riser Specification, Revision 1.1 (Section 1.2, "Reference Documents" on page 15). The Communication and Networking Riser (CNR) Specification defines a hardware-scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, a V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface that should be configured before system shipment. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Unlike in the case of the AMR, the system designer will not sacrifice a PCI slot after deciding not to include a CNR in a particular build. It is required that the CNR A0-A2 pins be set to a unique address, so that the CNR EEPROM can be accessed.

The Figure 58 indicates the interface for the CNR connector. The Platform LAN Connection (PLC) can either be an Intel 82562EH or Intel 82562ET component. Refer to the CNR specification for additional information.

Figure 58. CNR Interface
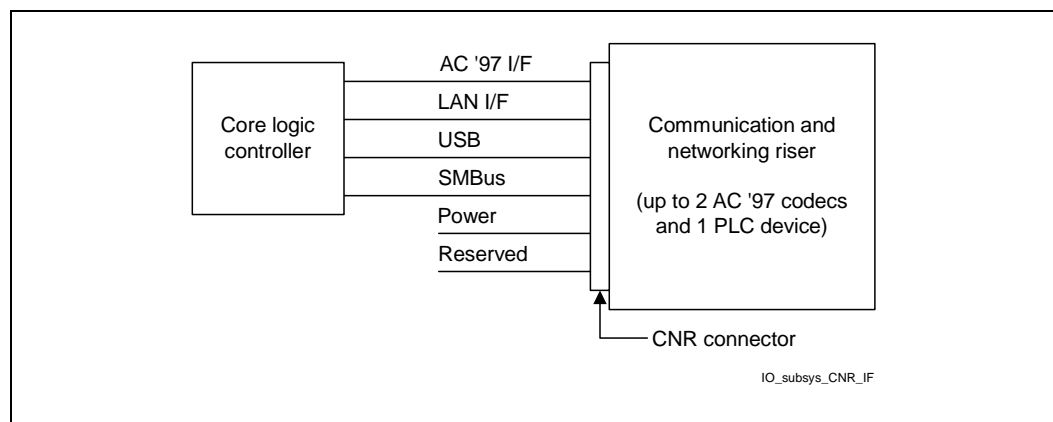
11.3.2 AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. For Intel recommended codec configurations, refer to the *Intel® White Paper Recommendations for ICHx/AC'97 Audio (Motherboard and Communication and Network Riser).*

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC'97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be

programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 59, Figure 60, Figure 61, and Figure 62) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 59. CDC_DN_ENAB# Support Circuitry for a Single Codec on Motherboard
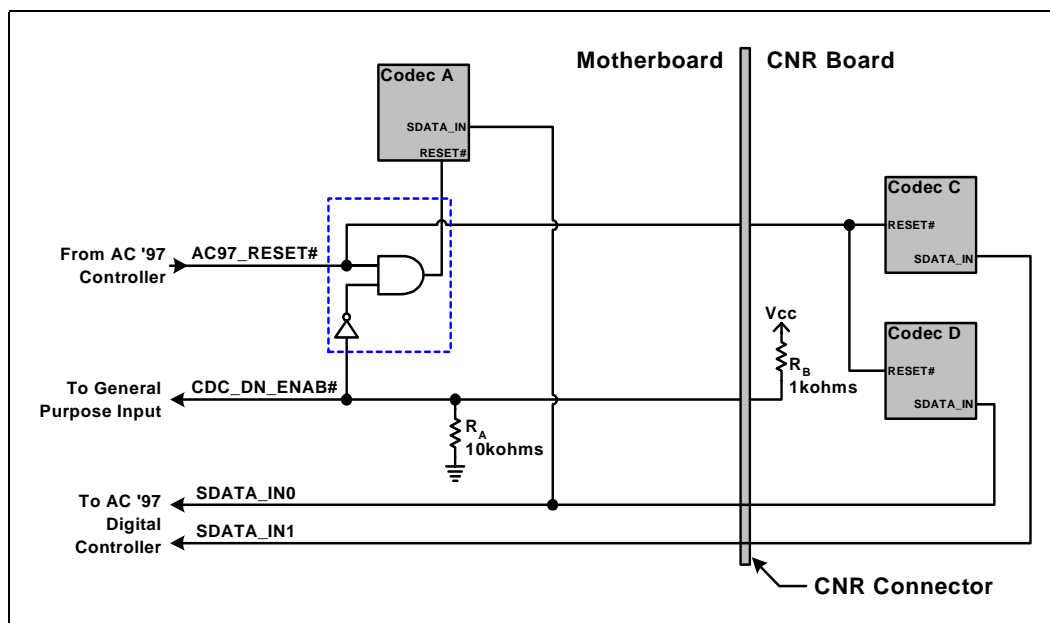
As shown in Figure 59, when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented, on the motherboard. This circuitry is required to disable the motherboard codec when a CNR is installed which contains two AC '97 codecs (or a single AC '97 codec which must be the primary codec on the AC-Link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-Link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 60 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 60 and Figure 61 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN*n* line as to not conflict with the motherboard codec(s).

Figure 60. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade
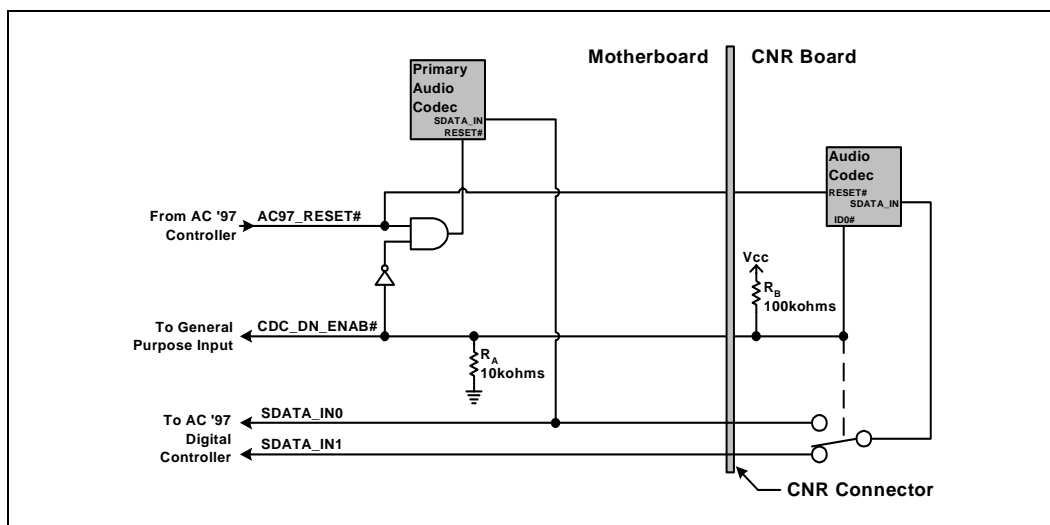
Note: Figure 61shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, RB, has been changed to 100 kΩ.

Figure 61. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard/One-Codec on CNR
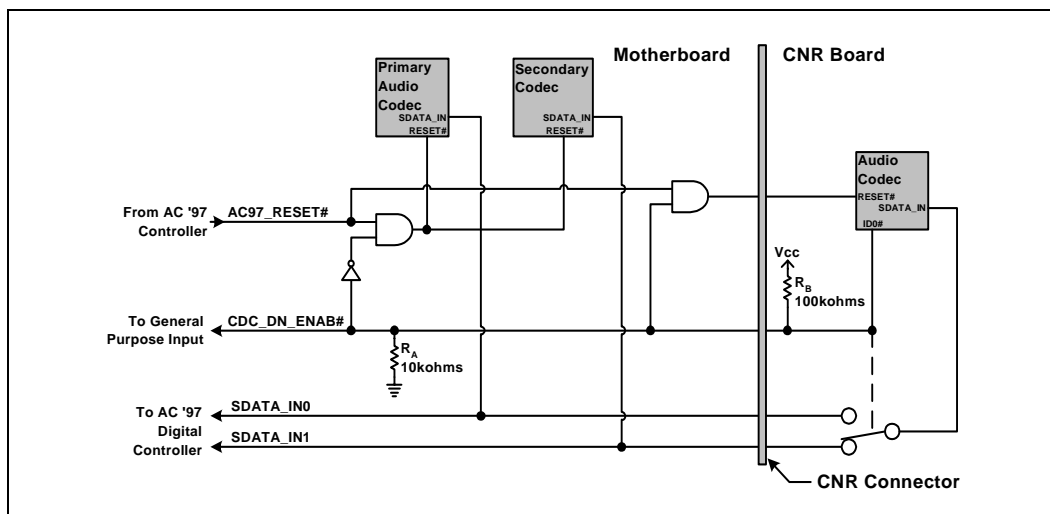
Figure 62 shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ.

Figure 62. CDC_DN_ENAB# Support for Two-Codecs on Motherboard/Two-Codecs on CNR
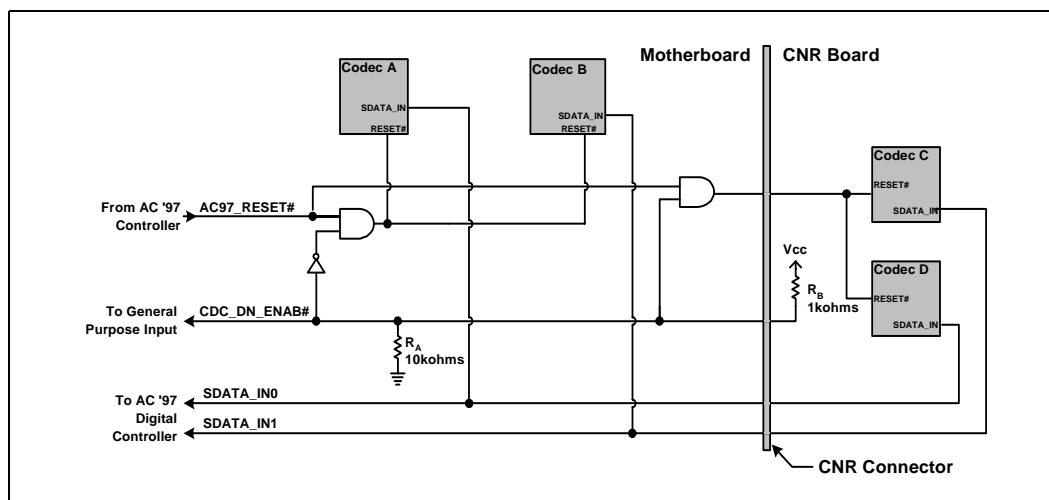
NOTES:

1. While it is possible to disable down codecs, as shown in Figure 59 and Figure 62, it is recommended against for reasons cited in the ICHx/AC'97 white paper, including avoidance of shipping redundant and/or non-functional audio jacks.
2. All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
3. Any CNR with two codecs must implement R_B with value 1 kΩ. If there is one codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
4. A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
5. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is *strongly recommended* for testing purposes.

Table 23. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC'97 interface. When high, indicates that the motherboard codec(s) must be removed from the AC'97 interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC'97 Interface.
AC97_RESET#	Reset signal from the AC'97 digital controller (ICH2).
SDATA_Inn	AC'97 serial data from an AC'97-compliant codec to an AC'97-compliant controller (i.e., the ICH2).

11.3.2.1   Valid Codec Configurations

Table 24. Codec Configurations

Valid Codec Configurations	Invalid Codec Configurations
AC(Primary)	MC(Primary) + X(any other type of codec)
MC(Primary)	AMC(Primary) + AMC(Secondary)
AMC(Primary)	AMC(Primary) + MC(Secondary)
AC(Primary) + MC(Secondary)	
AC(Primary) + AC(Secondary)	
AC(Primary) + AMC(Secondary)	

11.3.3   SPKR Pin Considerations

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull up resistor (the resistor is only enabled during boot/reset). Therefore it's default state when the pin is a "no connect" is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see Figure 63). The value of the pull-down must be such that the voltage divider caused by the pull down and integrated pull up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

Figure 63. Example Speaker Circuit
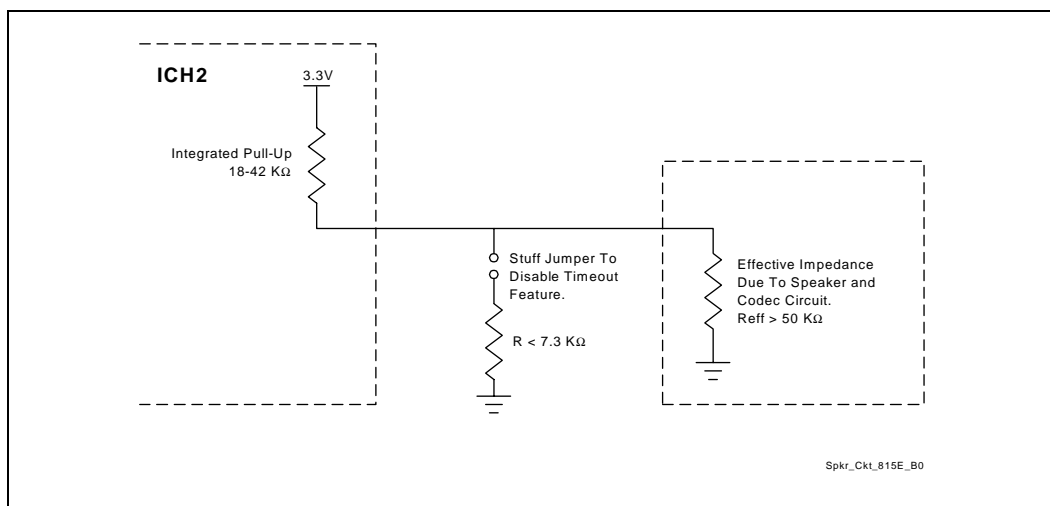
11.3.4   AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.

- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.

- Partition the board with all analog components grouped together in one area and all digital components in another.

- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.

- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.

- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/ isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.

- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

- Analog power and signal traces should be routed over the analog ground plane.

- Digital power and signal traces should be routed over the digital ground plane.

- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.

- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.

- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

- Locate the crystal or oscillator close to the codec.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2) and by any other codec present. The clock is used as the time base for latching and driving data.

11.3.5   System Board Implementation

The following design considerations are provided for the implementation of an ICH2 platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH2 platform.

- Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.

- The ICH2 supports wake-on-ring from S1–S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required. The ICH2 does not wake from the S5 state via the AC'97 link.

- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

11.4   USB

11.4.1   Using Native USB Interface

The general guidelines for the USB interface are as follows:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P- data lines.

- 15 Ω series resistors should be placed as close as possible to the ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.

- An optional 47 pF cap may be placed as close to the USB connector as possible on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap can be used for signal quality (rise/fall time) and to help minimize EMI radiation.

- 15 kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0± … P3±), and they are REQUIRED for signal termination by the USB specification. The stub should be as short as possible.

- The trace impedance for the P0±…P3± signals should be 45 Ω (to ground) for each USB signal P+ or P-. When the stack-up recommended in Section 2.1 is used, the USB requires 9-mil traces. The impedance is 90 Ω between the differential signal pairs P+ and P-, to match the 90 Ω USB twisted-pair cable impedance. Note that the twisted-pair's characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.

- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P-signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

Figure 64 illustrates the recommended USB schematic.

Figure 64. USB Data Signals
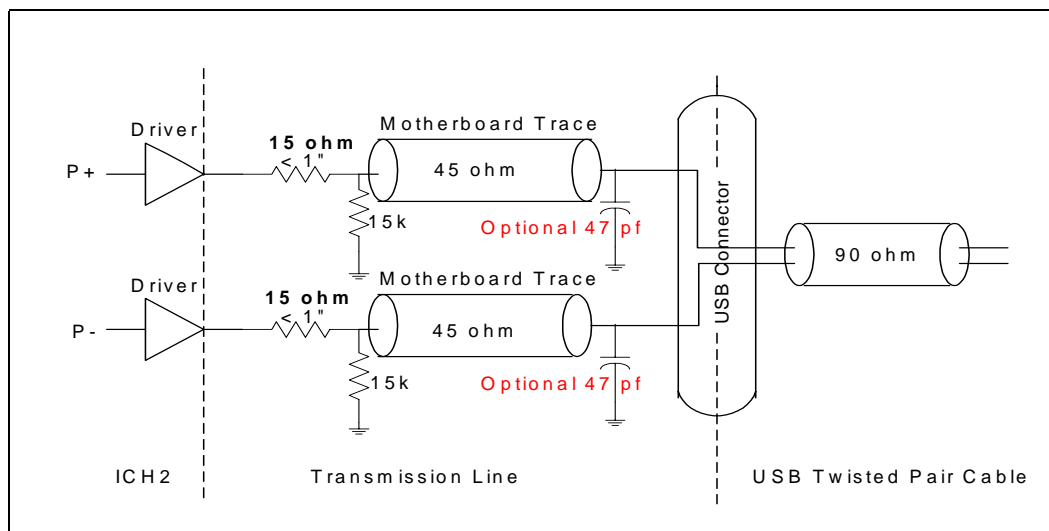
The recommended USB trace characteristics are:

- Impedance 'Z0' = 45.4 Ω

- Line Delay = 160.2 ps

- Capacitance = 3.5 pF

- Inductance = 7.3 nH

- Res @ 20° C = 53.9 mΩ

11.4.2 Disabling the Native USB Interface of ICH2

The ICH2 native USB interface can be disabled. This can be done when an external PCI based USB controller is being implemented in the platform. To disable the native USB Interface, ensure the differential pairs are pulled down through 15 kΩ resistors, ensure the OC[3:0]# signals are de-asserted by pulling them up weakly to VCC3SBY, and that both function 2 & 4 are disabled via the D31:F0;FUNC_DIS register. Ensure that the 48 MHz USB clock is connected to the ICH2 and is kept running. This clock must be maintained even though the internal USB functions are disabled.

11.5 IOAPIC Design Recommendation

Systems not using the IOAPIC should comply with the following recommendations:

- On the ICH2:
  - Tie PICCLK directly to ground.
  - Tie PICD0, PICD1 to ground through a 10 kΩ resistor.
- On the processor:
  - PICCLK requires special implementation for universal motherboard designs.

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— Tie PICD0 to 1.5 V through 10 kΩ resistors.

— Tie PICD1 to 1.5 V through 10 kΩ resistors.

11.5.1   PIRQ Routing Example

PCI interrupt request signals E-H are new to the ICH2. These signals have been added to lower the latency caused by having multiple devices on one Interrupt line. With these new signals, each PCI slot can have an individual PCI interrupt request line (assuming that the system has four PCI slots). Table 25 shows how the ICH2 uses the PCI IRQ when the IOAPIC is active.

Table 25. IOAPIC Interrupt Inputs 16 Through 23 Usage

No	IOAPIC INTIN PIN	Function in ICH2 using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	
2	IOAPIC INTIN PIN 17 (PIRQB)	AC'97, Modem and SMBUS
3	IOAPIC INTIN PIN 18 (PIRQC)	
4	IOAPIC INTIN PIN 19 (PIRQD)	USB Controller #1
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN Device
6	IOAPIC INTIN PIN 21 (PIRQF)	
7	IOAPIC INTIN PIN 22 (PIRQG)	
8	IOAPIC INTIN PIN 23 (PIRQH)	USB Controller #2 (starting from ICH2 B0 stepping)

Interrupts B, D, E and H service devices internal to the ICH2. Interrupts A, C, F, and G are unused and can be used by PCI slots. Figure 65 shows an example of IRQ line routing to the PCI slots.

Figure 65. Example PIRQ Routing
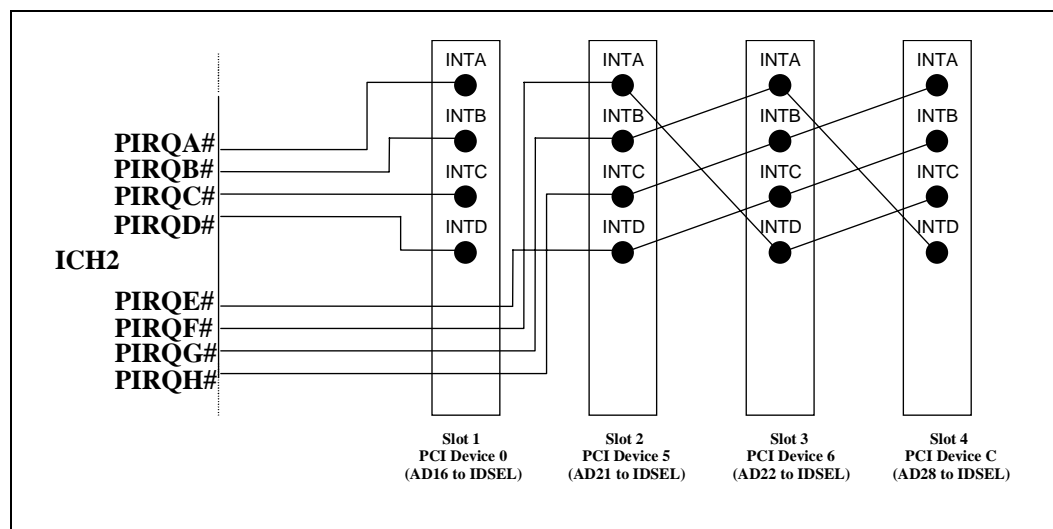
The PCI IRQ Routing shown in Figure 65 allows the ICH2 internal functions to have a dedicated IRQ (assuming add-in cards are single function devices and use INTA). If a P2P bridge card or a multifunction device uses more than one INTn# pin on the ICH2 PCI Bus, the ICH2 internal

functions will start sharing IRQs. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH2's internal device/functions.

11.6   SMBus/SMLink Interface

The SMBus interface on the ICH2 is the same as that on the ICH. It uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH2.

The ICH2 incorporates a new SMLink interface supporting AOL*, AOL2*, and slave functionality. It uses two signals, SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal, and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB slave interface.

For Alert on LAN (AOL) functionality, the ICH2 transmits heartbeat and event messages over the interface. When the Intel 82562EM LAN connect component is used, the ICH2's integrated LAN controller claims the SMLink heartbeat and event messages and sends them out over the network. An external, AOL2-enabled LAN controller will connect to the SMLink signals, to receive heartbeat and event messages as well to as access the ICH2 SMBus slave interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus slave interface obey the SMBus protocol, so the two interfaces can be externally wire-ORed together to allow an external management ASIC to access targets on the SMBus as well as the ICH2 slave interface. This is performed by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA, as shown in Figure 66. Since the SMBus and SMLINK are pulled up to VCCSUS3_3, system designers must ensure that they implement proper isolation for any devices that may be powered down while VCCSUS3_3 is still active (i.e., thermal sensors).

Figure 66. SMBus/SMLink Interface
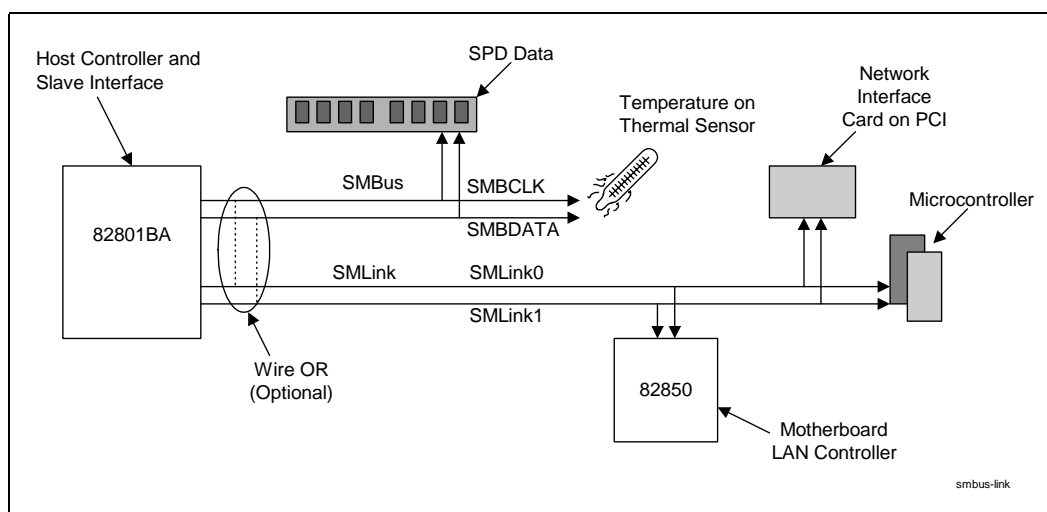
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Note: Intel does not support external access to the ICH2's integrated LAN controller via the SMLink interface. Also, Intel does not support access to the ICH2's SMBus slave interface by the ICH2's SMBus host controller. Table 26 describes the pull-up requirements for different implementations of the SMBus and SMLink signals.

Table 26. Pull-up Requirements for SMBus and SMLink

SMBus / SMLink Use	Implementation
Alert-on-LAN* signals	4.7 kΩ pull-up resistors to 3.3 VSB are required.
GPIOs	Pull-up resistors to 3.3 VSB and the signals must be allowed to change states on power-up. (For example, on power-up the ICH2 will drive *heartbeat* messages until the BIOS programs these signals as GPIOs.) The value of the pull-up resistors depends on the loading on the GPIO signal.
Not Used	4.7 kΩ pull-up resistors to 3.3 VSB are required.

11.6.1   SMBus Architecture & Design Considerations

There are several possibilities for designing an SMBus using the ICH2. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs, where all devices are powered by either VCC$_{CORE}$ or VCC_Suspend, and a mixed design where some devices are powered by each of the two supplies.

Primary considerations in choosing a design are based on:

- Whether there are there devices that must run in STR?
- Amount of VCC_Suspend current available, i.e., minimizing load of VCC_Suspend

11.6.1.1   General Design Issues and Notes

Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2 kΩ This should prevent the SMBus signals from floating, which could cause leakage in the ICH2 and other devices.
- SDRAM DIMMs have their SPD device powered by the same power plane as that used for the DRAM array. Thus, in a system where STR is supported, the SPD device must be powered by VCC_Suspend. In a system not supporting STR, this DIMM can be powered by the core supply.
- RIMM memory modules have a separate power source from the RDRAM array for the SPD device. If this SPD device needs to operate in STR, then it should be connected to the VCC_Suspend supply.
- The ICH2 does not run SMBus cycles while in STR.
- SMBus devices that can operate in STR must be powered by the VCC_Suspend supply.

11.6.1.1.1   The Unified VCC_Suspend Architecture

In this design all SMBus devices are powered by the VCC_Suspend supply. Consideration must be made to provide enough VCC_Suspend current while in STR.

Figure 67. Unified VCC_Suspend Architecture
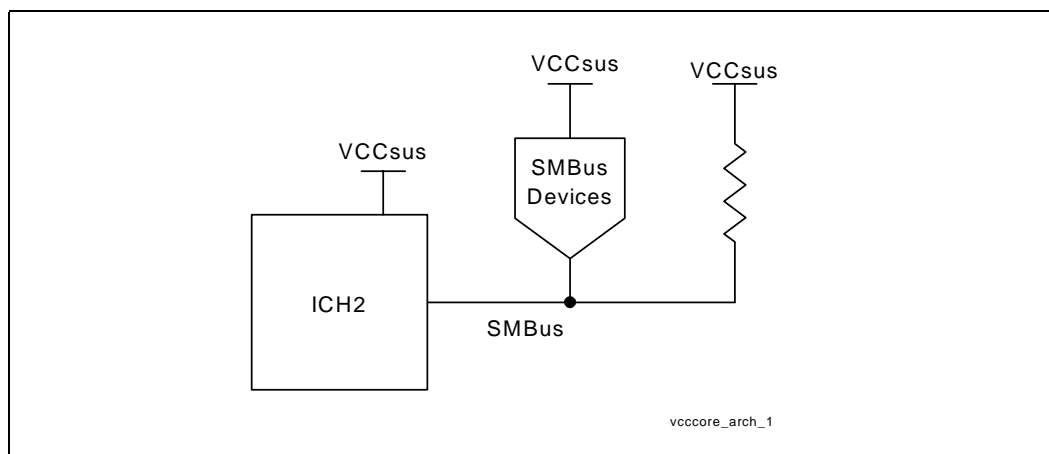
11.6.1.1.2 The Unified VCC$_{CORE}$ Architecture

In this design, all SMBUS devices are powered by the VCC$_{CORE}$ supply. This architecture allows none of the devices to operate in STR, but minimizes the load on VCC_Suspend (VCCsus).

Figure 68. Unified VCC$_{CORE}$ Architecture
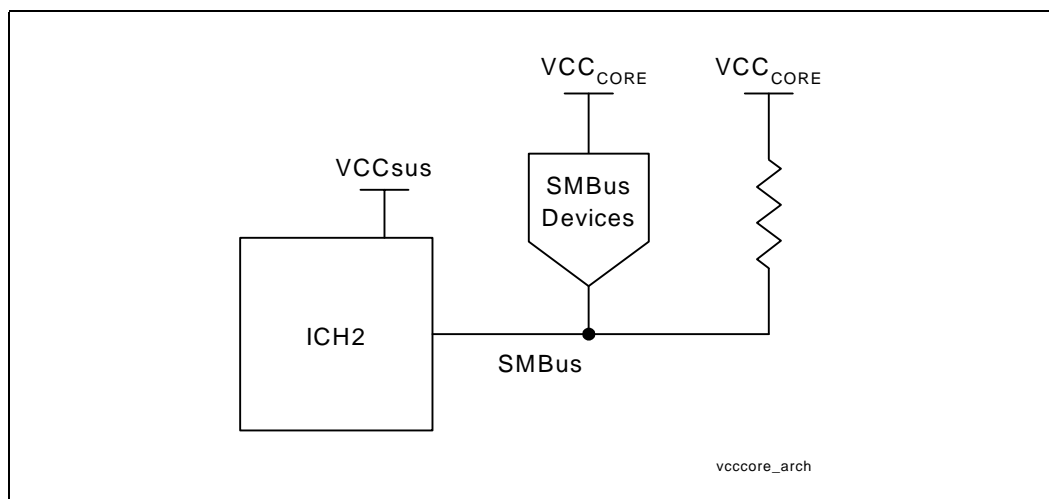
NOTES:
1. The SMBus device needs to be back-drive safe while its supply (VCC$_{CORE}$) is off and VCC_Suspend is still powered.
2. In suspended modes where VCC$_{CORE}$ is OFF and VCC_Suspend is on, the VCC$_{CORE}$ node will be very near ground. In this case the input leakage of the ICH will be approximately 10 uA.

11.6.1.1.3 Mixed Architecture

This design allows for SMBus devices to communicate while in STR, yet minimizes VCC_Suspend (VCCsus) leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a "bus switch" to isolate the devices powered by the core and suspend supplies (see Figure 69).
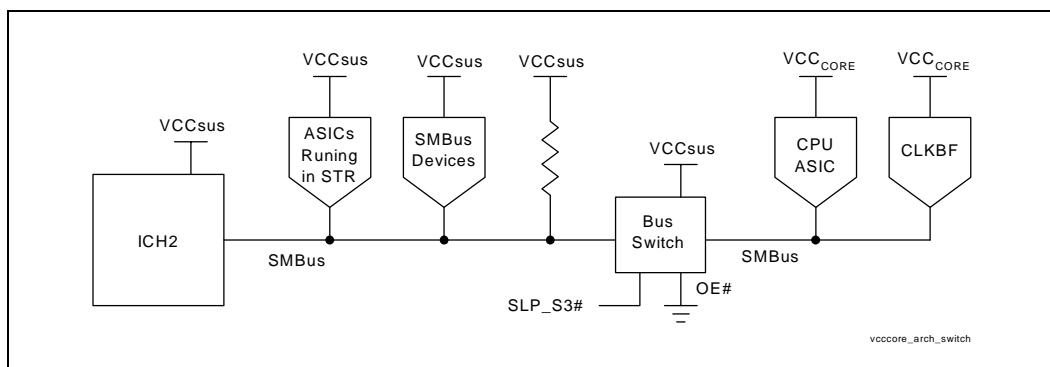
Added Considerations for Mixed Architecture

- The bus switch must be powered by VCC_Suspend (VCCsus)

- If there are 5 V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3 V signal levels.

- Devices that are powered by the VCC_Suspend well must not drive into other devices that are powered off. This is accomplished with the "bus switch".

11.7   PCI

The ICH2 provides a PCI Bus interface compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH2 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH2 supports six PCI Bus masters (excluding the ICH2), by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 70. PCI Bus Layout Example
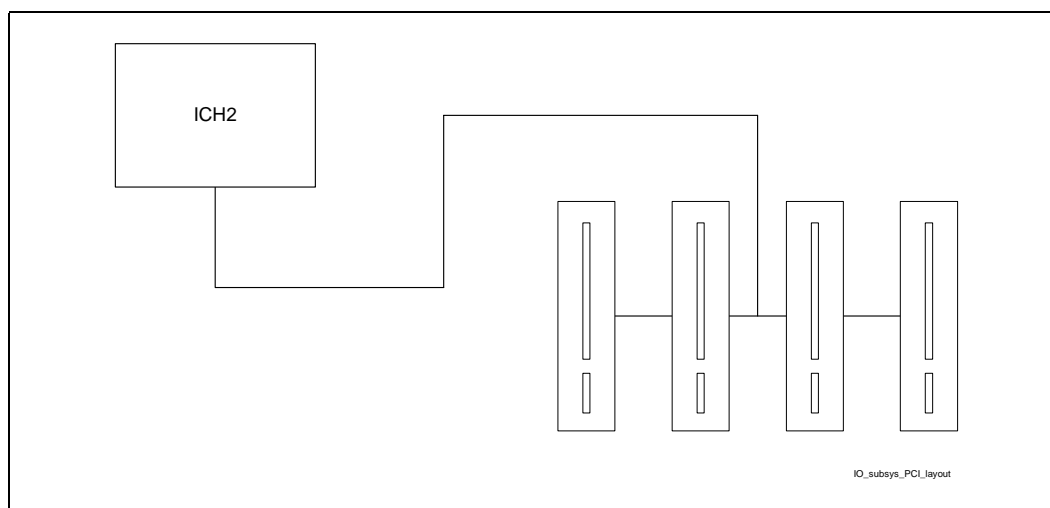
11.8 RTC

The ICH2 contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. The internal
RTC module provides two key functions: keeping the date and time and storing system data in its
RAM when the system is powered down. This section will present the recommended
implementation for the RTC circuit for the ICH2.

11.8.1 RTC Crystal

The ICH2 RTC module requires an external oscillating source of 32.768 kHz connected on the
RTCX1 and RTCX2 pins. Figure 79 shows the external circuitry that comprises the oscillator of the
ICH2 RTC.

Figure 71. External Circuitry for the ICH2 RTC
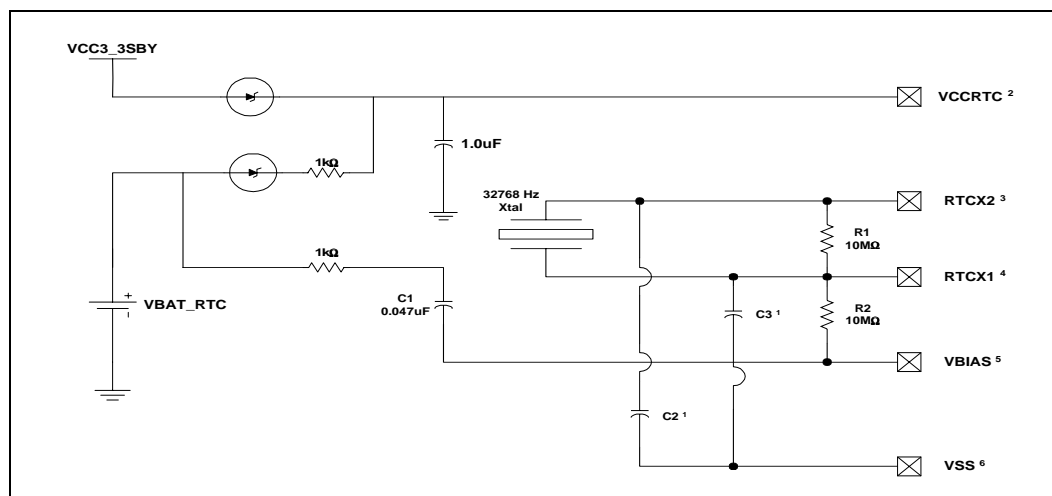
NOTE:
1. The exact capacitor value must be based on the crystal maker's recommendation. (The typical values for C2 and C3 are 18 pF with C_{LOAD} = 12.5 pF.)
2. VccRTC: Power for RTC well
3. RTCX2: Crystal input 2 – Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal input 1 – Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS voltage – This pin is used to provide a reference voltage. This DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground

11.8.2 External Capacitors

To maintain RTC accuracy the external capacitor C1 must be 0.047 µF. The external capacitor values for C2 and C3 should be chosen to provide the manufacturer-specified load capacitance (Cload) for the crystal, when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC.

The following equation can be used to choose the external capacitance values (C2 and C3):

Equation 2. Cload = (C2 * C3) / (C2 + C3) + Cparasitic

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain 32.768 kHz.

11.8.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible. Approximately 0.25 inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean. Use a filter, such as an RC low-pass or a ferrite inductor.

11.8.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system.

Example batteries include the Duracell* 2032, 2025 or 2016 (or equivalent), which give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 μA, the battery life will be at least:

170,000 μAh / 3 μA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is within the range 3.0 V to 3.3 V.

The battery must be connected to the ICH2 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC well to be powered by the battery when system power is unavailable, but by system power when it is available. So, the diodes are set to be reverse-biased when system power is unavailable. Figure 72 shows an example of the used diode circuitry.

Figure 72. Diode Circuit to Connect RTC External Battery
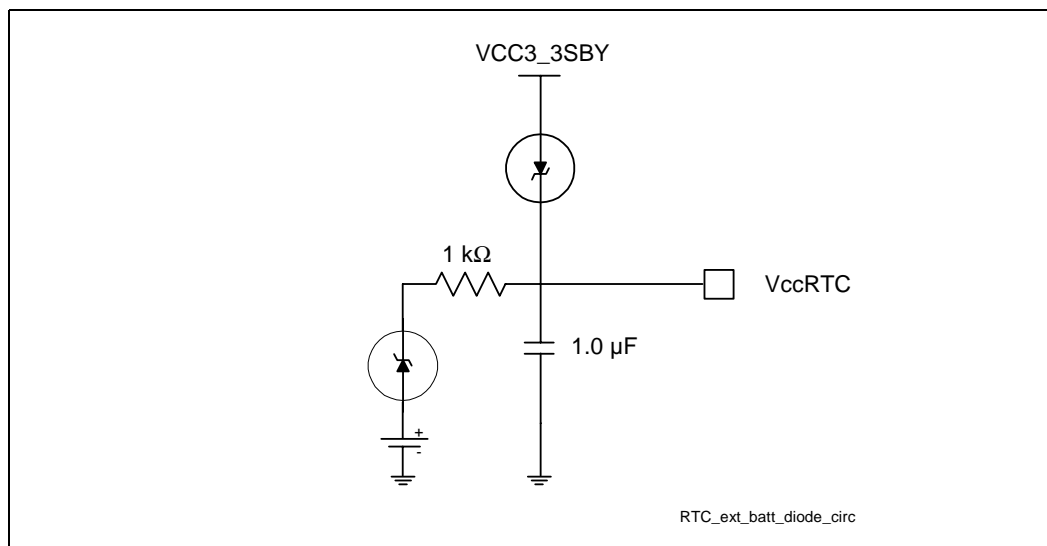
A standby power supply should be used in a desktop system, to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and, thereby, the RTC accuracy.

11.8.5 RTC External RTCRST Circuit

The ICH2 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go High some time after the battery voltage is valid. The RC time delay should be within the range of 10–20 ms.

When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until cleared by software. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

Figure 73. RTCRST External Circuit for ICH2 RTC
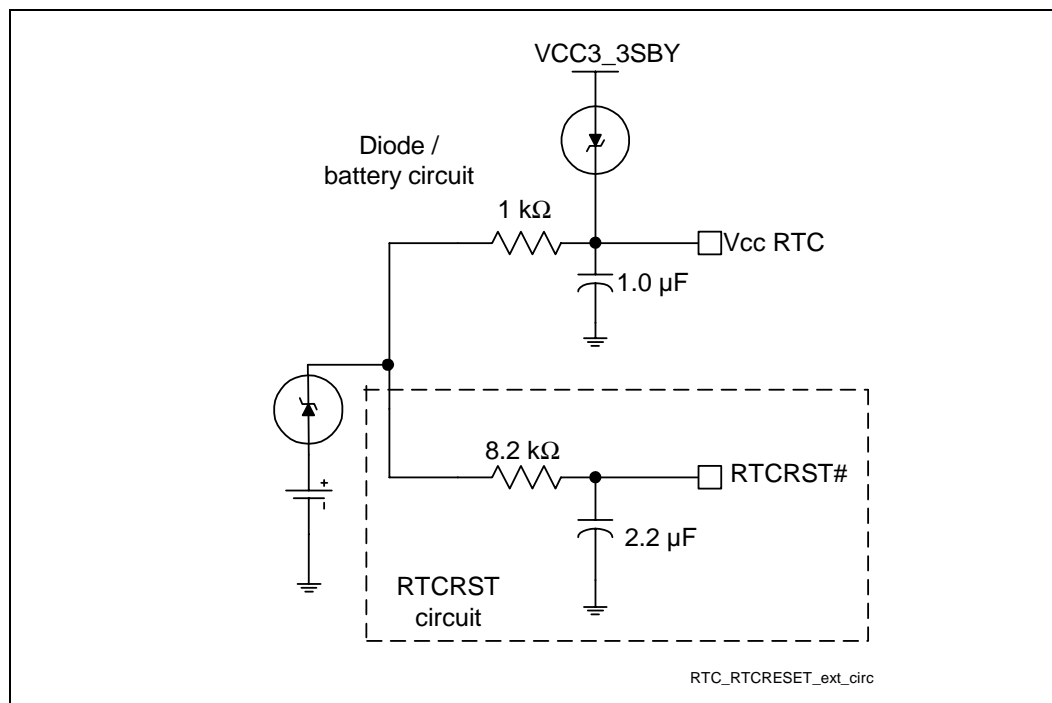
This RTCRST# circuit is combined with the diode circuit (see Figure 73), which allows the RTC well to be powered by the battery when system power is unavailable. Figure 73 shows an example of this circuitry when used in conjunction with the external diode circuit.

11.8.6   Power-Well Isolation Control Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 73 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

The circuit shown in should be implemented to control well isolation between the 3.3 V resume and RTC power wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).Please refer to the Intel® 815E Chipset Platform for Use with Universal Socket 370 Design Guide Update.

11.8.7 RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths less than 1 inch. The shorter, the better.

- Minimize the capacitance between RTCX1 and RTCX2 in the routing. (Optimally, there would be a ground line between them.)

- Put a ground plane under all external RTC circuitry.

- Do not route any switching signals under the external components (unless on the other side of the ground plane).

11.8.8 VBIAS DC Voltage and Noise Measurements

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths less than 1 inch. The shorter, the better.

- Steady-state VBIAS is a DC voltage of about 0.38 V ± .06 V.

- When the battery is inserted, VBIAS will be "kicked" to about 0.7–1.0 V, but it will return to its DC value within a few ms.

- Noise on VBIAS must be kept to a minimum (200 mV or less).

- VBIAS is very sensitive and cannot be directly probed, but it can be probed through a .01 μF capacitor.

- Excessive noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.

- To minimize VBIAS noise, it is necessary to implement the routing guidelines described previously as well as the required external RTC circuitry, as described in the *Intel® 82801BA I/O Controller Hub* (ICH2*) and Intel® 82801BAM I/O Controller Hub (ICH2-M) Datasheet*.

11.9 LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components, depending on the target market. These guidelines use the Intel 82562ET to refer to both the Intel 82562ET and Intel 82562EM. The Intel 82562EM is specified in those cases where there is a difference.

Table 27. LAN Connect

LAN Connect Component	Connection	Features
Intel 82562EM	Advanced 10/100 Ethernet	AOL* & Ethernet 10/100 connection
Intel 82562ET	10/100 Ethernet	Ethernet 10/100 connection
Intel 82562EH	1 Mbit HomePNA* LAN	1 Mbit HomePNA connection

Intel developed a dual footprint for Intel 82562ET and Intel 82562EH, to minimize the required number of board builds. A single layout with the specified dual footprint allows the OEM to install the appropriate LAN connect component to satisfy market demand. Design guidelines are provided for each required interface and connection. Refer Figure 82 and table for the corresponding section of the design guide.

Figure 74. ICH2 / LAN Connect Section
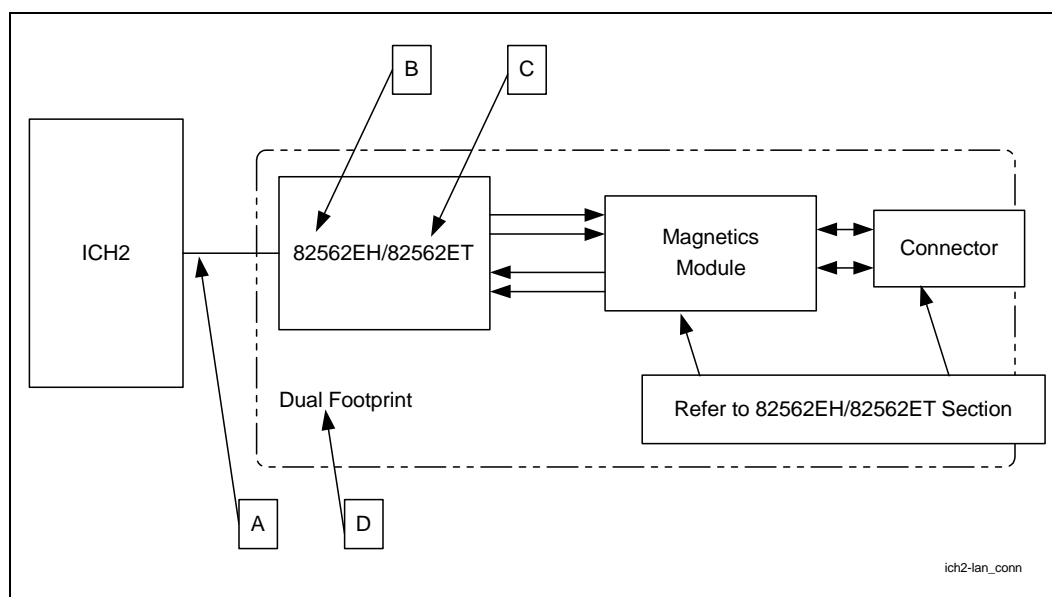
11.9.1   ICH2 – LAN Interconnect Guidelines

This section contains the guidelines for the design of motherboards and riser cards that comply with LAN connect. It should not be considered a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be taken to match the LAN_CLK traces with those of the other signals, as follows. The following guidelines are for the ICH2-to-LAN component interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both Intel 82562EH and Intel 82562ET/82562EM components. Both components share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0]. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when Intel 82562EH is installed. The AC characteristics for this interface are found in the *Intel® 82801BA I/O Controller Hub* (ICH2*) and Intel® 82801BAM I/O Controller Hub (ICH2-M) Datasheet* (document number: 290687). Dual footprint guidelines are found in Section .

11.9.1.1   Bus Topologies

The LAN connect interface can be configured in several topologies:

- Direct point-to-point connection between the ICH2 and the LAN component
- Dual footprint
- LOM/CNR implementation

11.9.1.2 Point-to-Point Interconnect

The following guidelines are for a single-solution motherboard. Either Intel 82562EH, Intel 82562ET or CNR is installed.

Figure 75. Single-Solution Interconnect
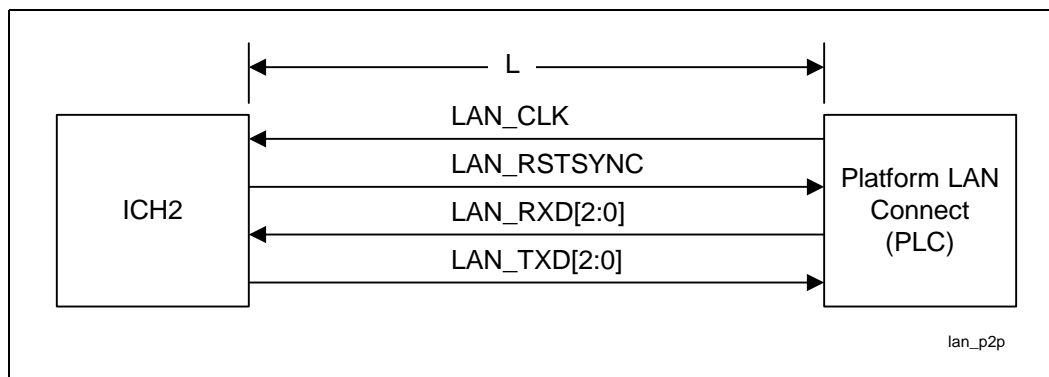
Table 28. Single-Solution Interconnect Length Requirements

(See Figure 75)

Configuration	L	Comment
Intel 82562EH	4.5" to 10"	Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected.
Intel 82562ET	3.5" to 10"	
Intel 82562EM	4.5" to 8.5"	
CNR	3" to 9"	The trace length from the connector to LOM should be 0.5" to 3.0"

11.9.1.3 LOM/CNR Interconnect

The following guidelines allow for an all-inclusive motherboard solution. This layout combines the LOM, dual-footprint, and CNR solutions. The resistor pack ensures that either a CNR option or a LAN on Motherboard option can be implemented at one time, as shown in Figure 76, which shows the recommended trace routing lengths.

Figure 76. LOM/CNR Interconnect
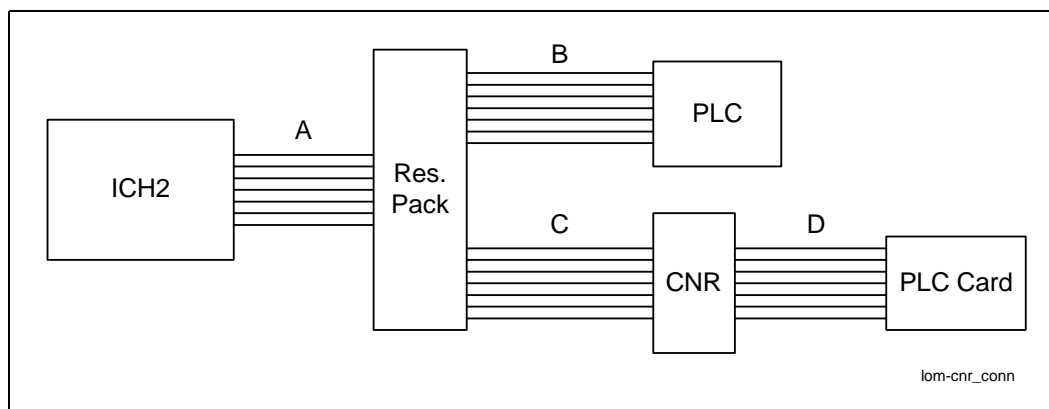
Table 29. LOM/CNR Length Requirements

(See Figure 84)

Configuration	A	B	C	D
Intel 82562EH	0.5" to 6.0"	4.0" to (10.0" – A)		
Intel 82562ET	0.5" to 7.0"	3.0" to (10.0" – A)		
Dual footprint	0.5" to 6.5"	3.5" to (10.0" – A)		
Intel 82562ET/EH card*	0.5" to 6.5"		2.5" to (9" – A)	0.5" to 3.0"

NOTE: The total trace length should not exceed 13 inches.

Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.

- The resistor pack value can be 0 Ω or 22 Ω.

- LAN on Motherboard PLC can be a dual-footprint configuration.

11.9.1.4 Signal Routing and Layout

LAN connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. Following are general guidelines that should be followed. It is recommended that the board designer simulate the board routing, to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard, the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inch shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.) The trace spacing, unless specified otherwise, is 5:10.

Figure 77. LAN_CLK Routing Example
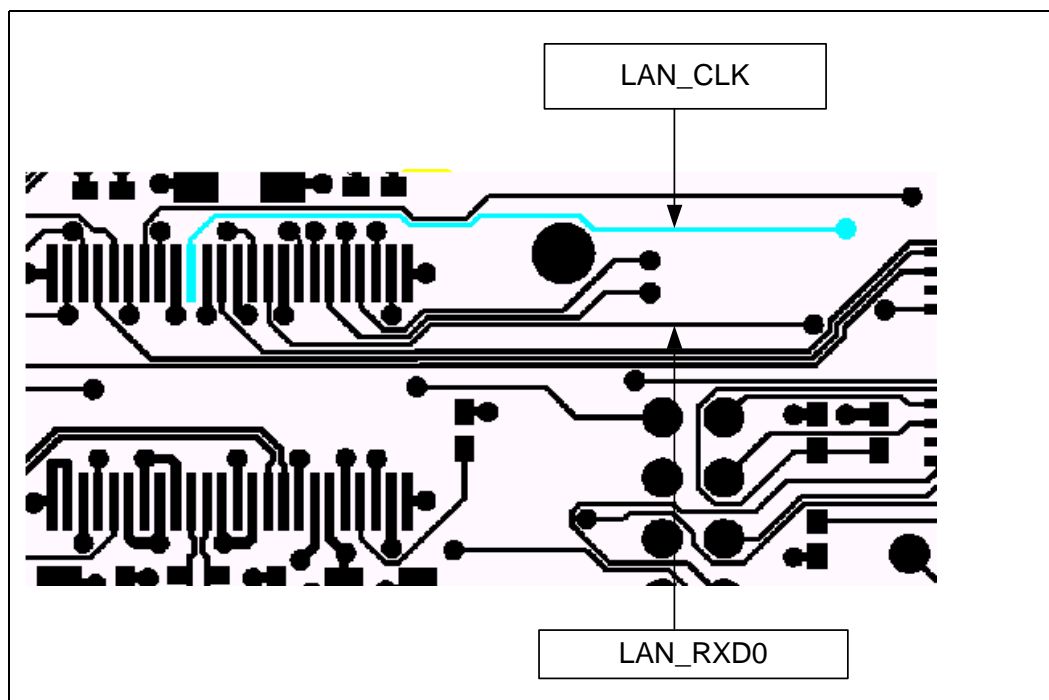
11.9.1.5   Crosstalk Consideration

Noise due to crosstalk must be carefully minimized. Crosstalk is the main cause of timing skews and is the largest part of the t_{RMATCH} skew parameter.

11.9.1.6   Impedances

Motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of $60\ \Omega \pm 15\%$ is strongly recommended. Otherwise, signal integrity requirements may be violated.

11.9.1.7   Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew-rate-controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33 Ω series resistor can be installed at the driver side of the interface, if the developer has concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

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11.9.2   General LAN Routing Guidelines and Considerations

11.9.2.1   General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

- The maximum mismatch between the clock trace length and the length of any data trace is 0.5 inch.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils recommended).
- Keep to 7 mils the maximum separation between differential pairs.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 78.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures, by a distance exceeding the largest aperture dimension.

Figure 78. Trace Routing
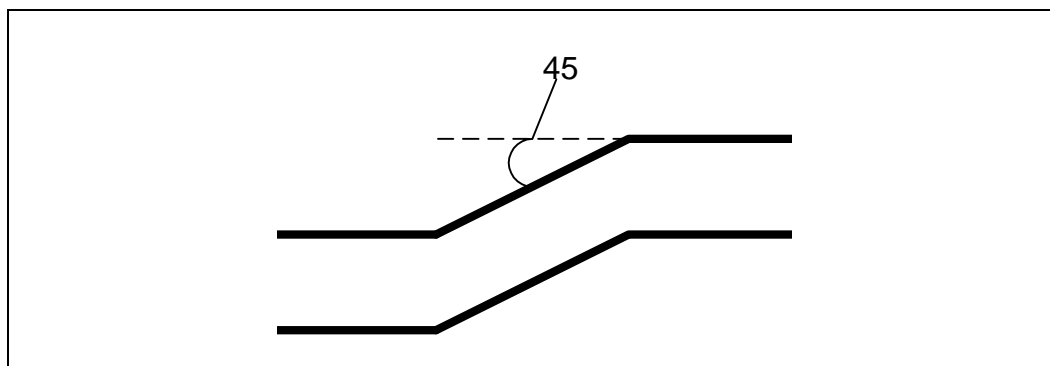
11.9.2.1.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, high-speed signals and signal layers close to a ground or power plane should be as short and wide as practical. Ideally, this ratio of trace width to height above the ground plane is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another, if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 0.030 inch (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long-and-thin traces are more inductive and would reduce the intended effect of the decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should have diameters sufficiently large to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/ magnetics/edge of the board.

11.9.2.1.2 Signal Isolation

Comply with the following rules for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together.

Note: Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal trace.

- Physically group together all components associated with one clock trace, to reduce trace length and radiation.

- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.

- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor or other similar device.

11.9.2.2 Power and Ground Connections

Comply with the following rules and guidelines for power and ground connections:

- All VCC pins should be connected to the same power supply.

- All VSS pins should be connected to the same ground plane.

- Four to six decoupling capacitors, including two 4.7 µF capacitors are recommended.

- Place decoupling as close as possible to power pins.

11.9.2.2.1 General Power and Ground Plane Considerations

To properly implement the common-mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be physically separated from the digital or input ground (primary side) by at least 100 mils.

Figure 79. Ground Plane Separation
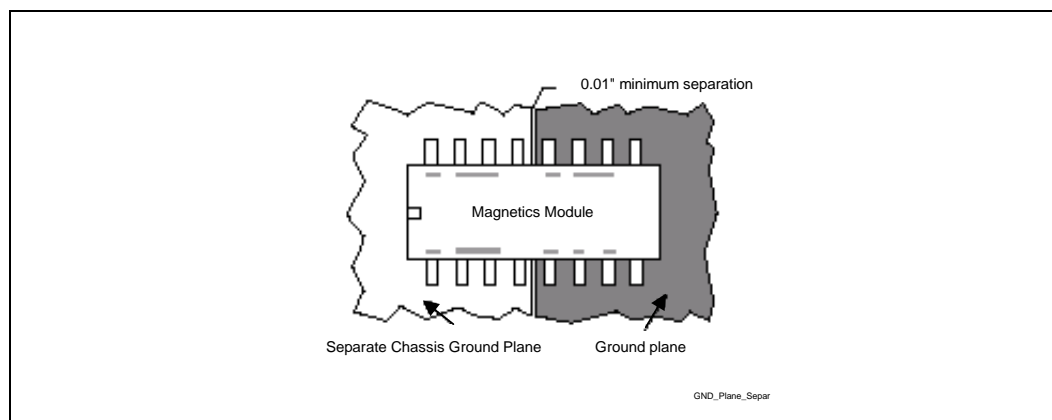
Good grounding requires minimizing inductance levels in the interconnections. Keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return significantly reduces EMI radiation.

Comply with the following rules to help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions (i.e., do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.

- To reduce coupling, separate noisy digital grounds from analog grounds.

- Noisy digital grounds may affect sensitive DC subsystems.

- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.

- Physically locate grounds between a signal path and its return. This minimizes the loop area.

- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which can radiate EMI.

- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between adjacent coils in the transformer. There should not be a power plane under the magnetics module.

- Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6mm (59.0 mil). This is a **critical** requirement needed to past FCC part 68 testing for Phoneline connection. Note that for worldwide certification a trench of 2.5 mm is required. In North America, the spacing requirement is 1.6mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

11.9.2.3   A 4-Layer Board Design

Top-Layer Routing

Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

Ground Plane

A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the Intel 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the Intel 82562 digital ground using a ground cutout, etc.

Power Plane

Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply planes VDD_A. Analog power may be a metal fill "island," separated from digital power, and better filtered than digital power.

Bottom-Layer Routing

Digital high-speed signals, which include all LAN interconnect interface signals, are routed on the bottom layer.

11.9.2.4   Common Physical Layout Issues

Common physical layer design and layout mistakes in LAN On Motherboard designs are as follows:

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and distort the transmit or receive waveforms.

2. Lack of symmetry between the two traces within a differential pair. (For each component and/ or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise, and distort the waveforms.

3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also any impedance mismatch in the traces will be aggravated if they are longer (see step 9). The magnetics should be as close to the connector as possible (<= 1 inch).

4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk on the receive channel will induce degraded long-cable BER. When crosstalk gets onto the transmit channel, it can cause excessive emissions (below the FCC standard) and can cause poor transmit BER on long cables. Other signals should be kept at least 0.3 inch from the differential traces.

5. Routing the transmit differential traces next to the receive differential traces. The transmit trace closest to one of the receive traces will put more crosstalk onto the closest receive trace, which can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. In the

vicinities where the traces enter or exit the magnetics, the RJ-45/11 and the PLC are the only possible exceptions.

6. Use of an inferior magnetics module. The magnetics modules used by Intel have been fully tested for IEEE PLC conformance, long-cable BER problems, and emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto-transformer in the transmit channel.)

7. Another common mistake is using an Intel 82555 or Intel 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different, and there also are differences in the receive circuit. Use the appropriate reference schematic or application notes.

8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and capacitor or termination plane. If these are not terminated properly, there can be emission (FCC) problems, IEEE conformance issues, and long-cable noise (BER) problems. The application notes contain schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.

9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω. (To calculate the differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close (see Note) to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. A 10 Ω to 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. Another common problem is to use a too-large capacitor between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel 82562ET side of the magnetics) to ground. Using capacitors with capacitances exceeding a few pF in either of these locations can slow the 100 Mbps rise and fall times so much that they fail the IEEE rise time and fall time specs, which will cause the return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (Reasonably good success has been achieved by using 6 pF to 12 pF values in past designs.) Unless there is some overshoot in the 100 Mbps mode, these caps are not necessary.

Note: It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces. Close should be considered to be less than 0.030 inch between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

11.9.3   Intel® 82562EH Home/PNA* Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 11.9.2. Additional guidelines for implementing an Intel 82562EH Home/PNA* LAN connect component are as follows are provided in the following subsections.

11.9.3.1   Power and Ground Connections

Obey the following rule for power and ground connections:

- For best performance, place decoupling capacitors on the backside of the PCB, directly under the Intel 82562EH, with equal distance from both pins of the capacitor to power/ground.

The analog power supply pins for Intel 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS as well as the VCCA and VSSA power supplies.

11.9.3.2   Guidelines for Intel® 82562EH Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section discusses guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the HomePNA LAN interface, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

11.9.3.3   Crystals and Oscillators

To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA magnetics module to prevent communication interference. If they exist, the crystal's retaining straps should be grounded to prevent the possibility of radiation from the crystal case, and the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562EH. Minimize the length and do not route any noisy signals in this area.

11.9.3.4   Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1 Ω (1%) resistors. This parallel termination should be placed close to the Intel 82562EH. The center, common point between the 51.1 Ω resistors is connected to a voltage-divider network. The opposite end of one 806 Ω resistor is tied to VCCA (3.3V), and the opposite end of the other 806 Ω resistor and the cap are connected to ground. The termination is shown in Figure 80.

Figure 80. Intel® 82562EH Termination
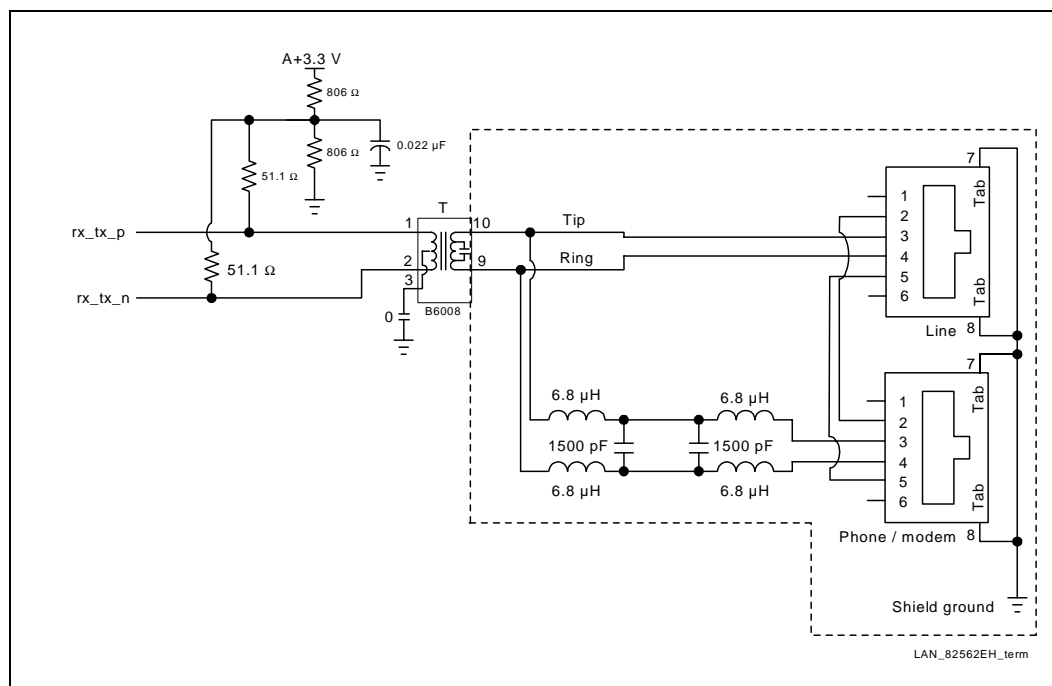
The filter and magnetics component T1 integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA LAN interface.

One RJ-11 jack (labeled "LINE" in Figure 86) allows the node to be connected to the Phoneline, and the second jack (labeled "PHONE" in the previous figure) allows other down-line devices to be connected at the same time. This second connector is not required by the HomePNA. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack, also is recommended by the HomePNA to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This restricts of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Refer to the HomePNA website (www.homepna.org) for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA certifications.

11.9.3.5   Critical Dimensions

There are three dimensions to consider during layout. Distance 'B' from the line RJ11 connector to the magnetics module, distance 'C' from the phone RJ11 to the LPF (if implemented), and distance 'A' from Intel 82562EH to the magnetics module (see Figure 81).

Figure 81. Critical Dimensions for Component Placement
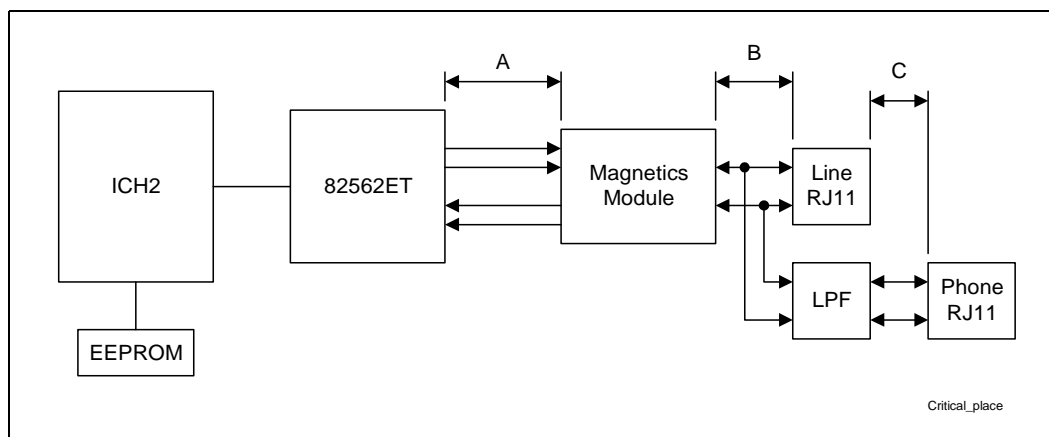
Table 30. Critical Dimensions for Component Placement

(Refer to Figure 81)

Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

11.9.3.5.1 Distance from Magnetics Module to Line RJ11 (Distance B)

This distance 'B' should be given highest priority and should be less then 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequally long differential pairs contribute to common-mode noise. This can degrade the receive circuit performance and contribute to emissions radiated from the transmit side.

11.9.3.5.2 Distance from Intel® 82562EH to Magnetics Module (Distance A)

Due to the high speed of signals present, distance 'A' between the Intel 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance from connects to the magnetics module.

Generally speaking, any section of trace intended for use with high-speed signals should be subject to proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between the device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

11.9.3.5.3 Distance from LPF to Phone RJ11 (Distance C)

This distance 'C' should be less then 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequally long differential pairs contribute to common-mode noise. This can degrade the receive circuit performance and contribute to emissions radiated from the transmit side.

11.9.4 Intel® 82562ET/Intel® 82562EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 11.9.2. Additional guidelines for implementing an Intel 82562ET or Intel 82562EM LAN connect component are provided in the following subsections. For related documents, see Section 1.2, "Reference Documents" on page 15.

11.9.4.1 Guidelines for Intel® 82562ET/Intel® 82562EM Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC and IEEE test specifications.

- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the Ethernet LAN interface, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space. In addition, the Intel 82562ET or Intel 82562EM should be placed more than 1.5 inches away from any board edge to minimize the potential for EMI radiation problems.

11.9.4.2 Crystals and Oscillators

To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference with communication. If they exist, the retaining straps of the crystal should be grounded to prevent possible radiation from the crystal case. Also, the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562ET or Intel 82562EM. Keep the trace length as short as possible and do not route any noisy signals in this area.

11.9.4.3 Intel® 82562ET/Intel® 82562EM Termination Resistors

The 100 Ω 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω 1% receive differential pairs (RDP/RDN) should be placed as close as possible to the LAN connect component (Intel 82562ET or Intel 82562EM). This is due to the fact that these resistors terminate the entire impedance seen at the termination source (i.e., Intel 82562ET), including the wire impedance reflected through the transformer.

Figure 82. Intel® 82562ET/Intel® 82562EM Termination
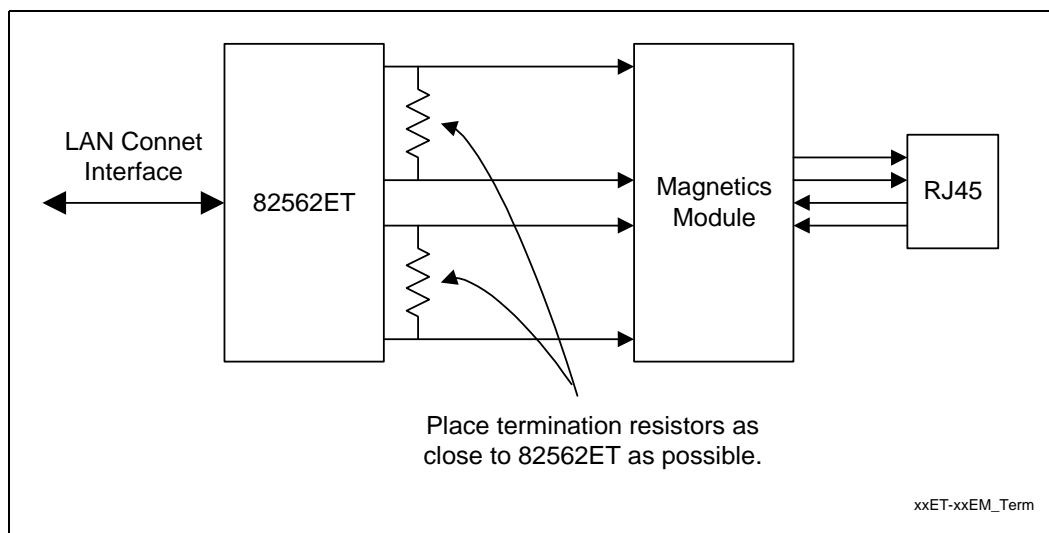
11.9.4.4 Critical Dimensions

There are two dimensions to consider during layout. Distance 'B' from the line RJ45 connector to the magnetics module and distance 'A' from the Intel 82562ET or Intel 82562EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches) (see Figure 83).

Figure 83. Critical Dimensions for Component Placement
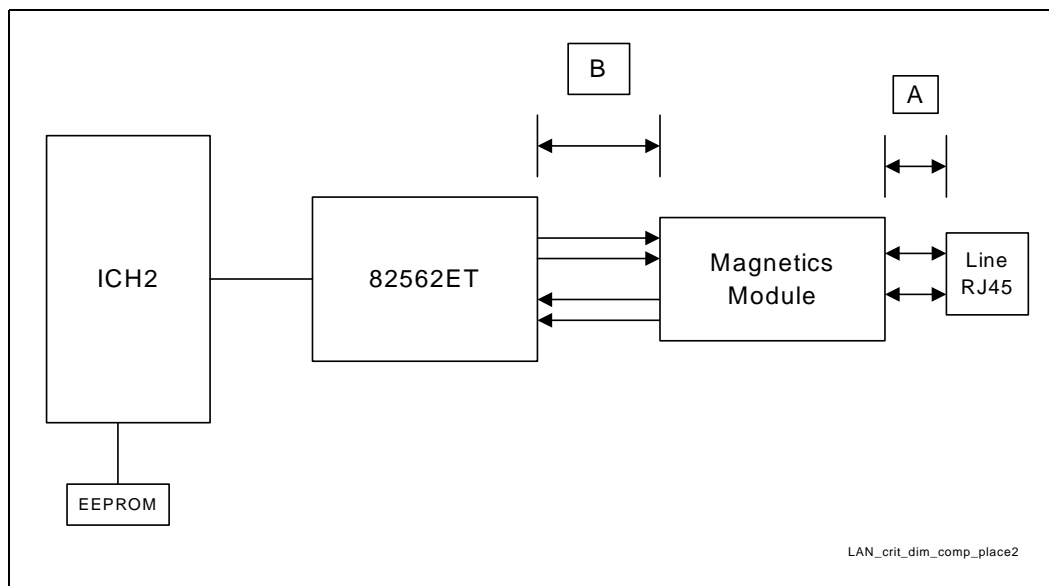
Table 31. Critical Dimensions for Component Placement

(see Figure 83)

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

11.9.4.4.1　Distance from Magnetics Module to RJ45

The distance A in Figure 83 should be given the highest priority in board layout. The separation between the magnetics module and the RJ45 connector should be kept less than 1 inch. The following trace characteristics are important and should be observed:

- Differential impedance: The differential impedance should be 100 Ω. The single-ended trace impedance will be approximately 50 Ω. However, the differential impedance can also be affected by the spacing between the traces.

- Trace Symmetry: Differential pairs (e.g., TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (e.g., width).

Caution:　Asymmetric and unequal length traces in the differential pairs contribute to common-mode noise. This can degrade the receive circuit's performance and contribute to emissions radiated from the transmit circuit. If the Intel 82562ET must be placed farther than a couple of inches from the RJ45 connector, distance B can be sacrificed. It should be a priority to keep the total distance between the Intel 82562ET and RJ-45 as short as possible.

Note:　The measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layouts accordingly. If the actual impedance is consistently low, a target of 105–110 Ω should compensate for second-order effects.

11.9.4.4.2　Distance from Intel® 82562ET to Magnetics Module

Distance B should also be designed to be less than 1 inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should be subject to proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that contributes more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and of equal length within each differential pair.

11.9.4.5　Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both backplanes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems, such as analog-to-digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane. Similarly, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds so as to minimize the loop area between a

signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high-frequency harmonics, that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

Terminating Unused Connections

In Ethernet designs, it is common practice to terminate to ground both unused connections on the RJ-45 connector and the magnetics module. Depending on the overall shielding and grounding design, this may be done to the chassis ground, signal ground or a termination plane. Care must be taken when using various grounding methods to ensure that emission requirements are met. The method most often implemented is called the "Bob Smith" termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

Termination Plane Capacitance

The recommended minimum termination plane capacitance is 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (electrical fast transient) testing. If a discrete capacitor is used, it should be rated for at least 1000 Vac, to satisfy the EFT requirements.

Figure 84. Termination Plane
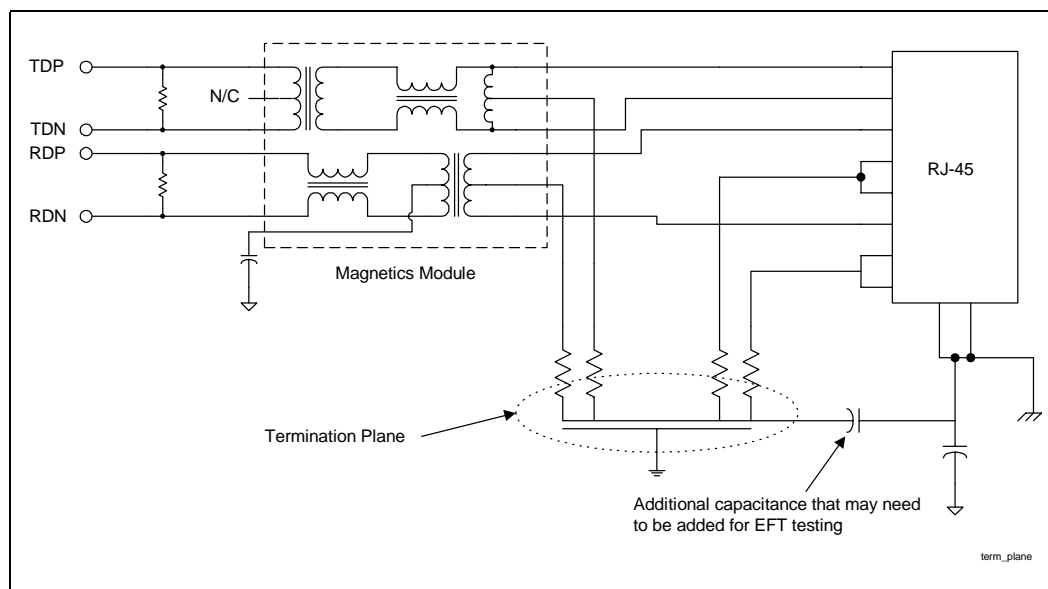
11.9.5   Intel® 82562ET/82562EM Disable Guidelines

To disable the Intel 82562ET/ 82562EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) being asserted. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. The circuit shown in Figure 85 allows this behavior. BIOS can disable the LAN microcontroller by controlling the GPIO.

Figure 85. Intel® 82562ET/82562EM Disable Circuit
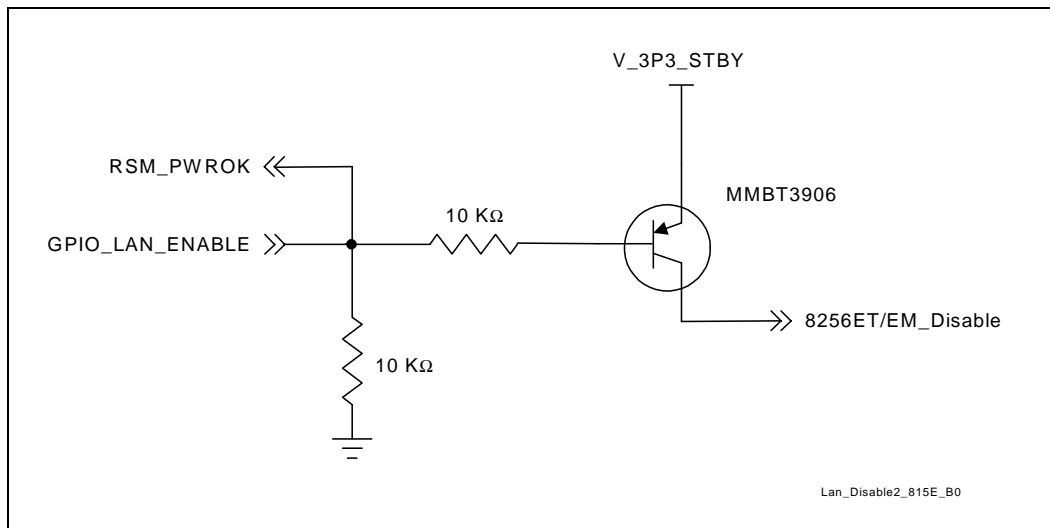
There are four pins that are used to put the Intel 82562ET controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 32 describes the operational/disable features for this design.

The four control signals shown in Table 32 should be configured as follows: Test_En should be pulled-down through a 100 Ω resistor. The remaining three control signals should each be connected through 100 Ω series resistors to the common node "82562ET_Disable" of the disable circuit.

Table 32. Intel® 82562ET Operating States

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled with Clock (low power)
1	1	1	1	Disabled without Clock (lowest power)

11.9.6   Intel® 82562ET/Intel® 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual-footprint solution. This configuration enables the developer to install either the Intel 82562EH or the Intel 82562ET/82562EM components, while using only one motherboard design. The following guidelines are for the Intel 82562ET/82562EH dual-footprint option. The guidelines called out in Sections Section 11.9.1

through Section 11.9.4 apply to this configuration. The dual footprint for this particular solution uses a SSOP footprint for Intel 82562ET and a TQFP footprint for Intel 82562EH. The combined footprint for this configuration is shown in Figure 86 and Figure 87.

Figure 86. Dual-Footprint LAN Connect Interface

dual_ft_lan_conn
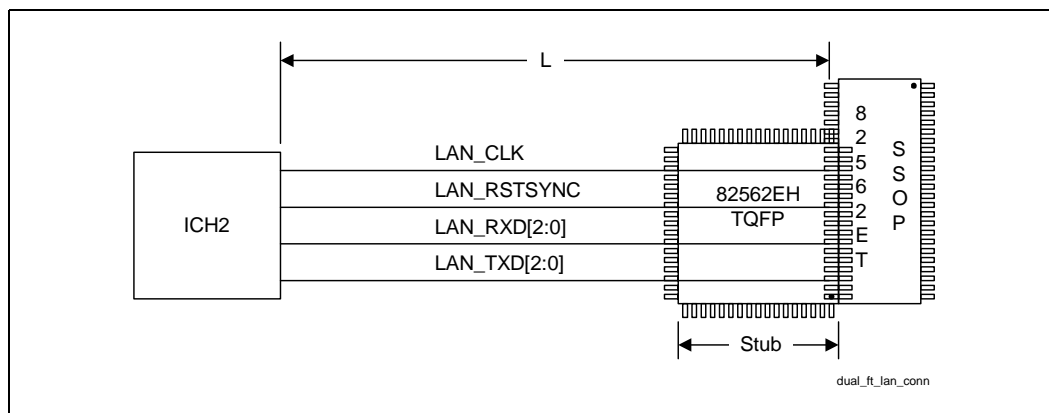
Figure 87. Dual-Footprint Analog Interface

dual_ft_AN_conn
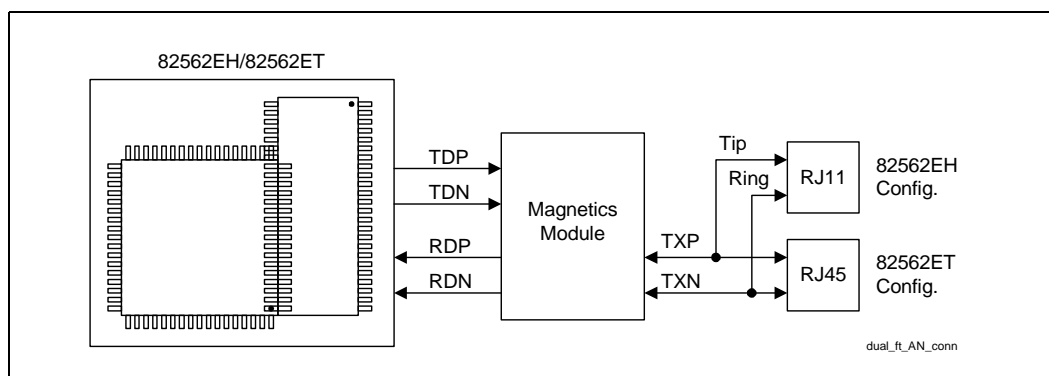
The following are additional guidelines for this configuration:

- L = 3.5 inches to 10 inches

- Stub < 0.5 inch

- Either Intel 82562EH or Intel 82562ET/82562EM can be installed, but not both.

- Intel 82562ET pins 28,29, and 30 overlap with Intel 82562EH pins 17,18, and 19.

- Overlapping pins are tied to ground.

- No other signal pads should overlap or touch.

- Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/ Ring, and RXN/Tip are shared by the Intel 82562EH and Intel 82562ET configurations.

- No stubs should be present when Intel 82562ET is installed.

- Packages used for the dual footprint are TQFP for Intel 82562EH and SSOP for Intel 82562ET.

- A 22 Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.

- Resistor should be placed as close as possible to the component.

- Use components that can satisfy both the Intel 82562ET and Intel 82562EH configurations (i.e., magnetics module).

- Install components for either the Intel 82562ET or the Intel 82562EH configuration. Only one configuration can be installed at a time.

- Route shared signal lines such that stubs are not present or are kept to a minimum.

- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component.

- Use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.

- Traces from magnetics to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.

- Place at least bulk capacitor (4.7 µF or greater) on each side of the component.

- Place decoupling capacitors (0.1 µF) as close to the component as possible.

11.10   LPC/FWH

The following subsections provide general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS.

11.10.1   In-Circuit FWH Programming

All cycles destined for the FWH will appear on the PCI. The ICH2 hub interface-to-PCI Bridge puts all processor boot cycles out on the PCI (before sending them out on the FWH interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on PCI. This enables booting from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH2 in the subtractive decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, two devices will positively decode the same cycle. In systems with the Intel® 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind the Intel 82380AB. Once you have booted from the PCI card, you potentially could program the FWH in circuit and program the ICH2 CMOS.

11.10.2   FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports a V_{PP} of 3.3 V or 12 V. If V_{PP} is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V V_{PP} for 80 hours. The 12 V V_{PP} would be useful in a programmer environment that is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin **must** be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 88. FWH VPP Isolation Circuitry
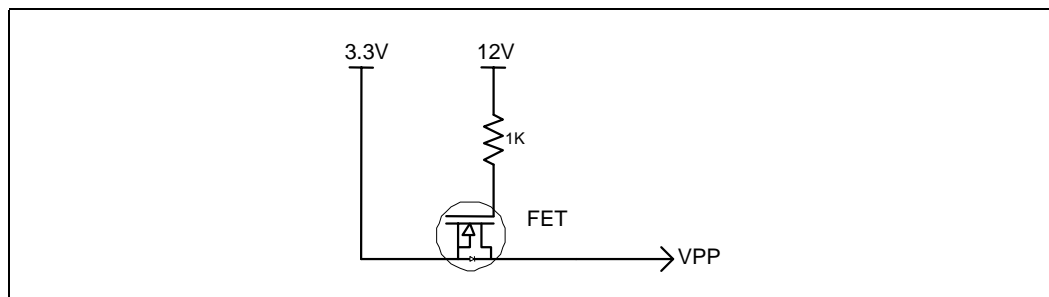
11.10.3   FWH Decoupling

A 0.1 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the VCC supply pins and the VSS ground pin to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

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Clocking 12

For an Intel 815E platform, there are two clock specifications. One is for a 2-DIMM solution, and the other is for a 3-DIMM solution. In both specifications only single-ended clocking is supported. Intel 815E platforms using a Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor cannot implement differential clocking.

12.1 Two-DIMM Clocking

Table 33 shows the characteristics of the clock generator for a 2-DIMM solution.

Table 33. Intel® CK-815 (Two-DIMM) Clocks

Number	Clock	Frequency
3	processor clocks	66/100/133 MHz
9	SDRAM clocks	100/133 MHz
7	PCI clocks	33 MHz
2	APIC clocks	16.67/33 MHz
2	48 MHz clocks	48 MHz
3	3 V, 66 MHz clocks	66 MHz
1	REF clock	14.31818 MHz

The following bullets list the features of the Intel CK-815 clock generator in a 2-DIMM solution:

- Nine copies of 100/133 MHz SDRAM clocks (3.3 V) [SDRAM0…7, DClk]
- Seven copies of PCI clock (33 MHz) (3.3 V)
- Two copies of APIC clock at 33 MHz, synchronous to processor clock (2.5 V)
- One copy of 48 MHz USB clock (3.3 V) (non-SSC) (type 3 buffer)
- One copy of 48 MHz DOT clock (3.3 V) (non-SSC) (see DOT details)
- Three copies of 3 V, 66 MHz clock (3.3 V)
- One copy of REF clock at 14.31818 MHz (3.3 V)
- Ref. 14.31818 MHz xtal oscillator input
- Power-down pin
- Spread-spectrum support
- I^2C support for turning off unused clocks

Figure 89 shows the Intel 815E chipset platform clock architecture for a 2-DIMM solution.

Figure 89. Platform Clock Architecture for a Two-DIMM Solution
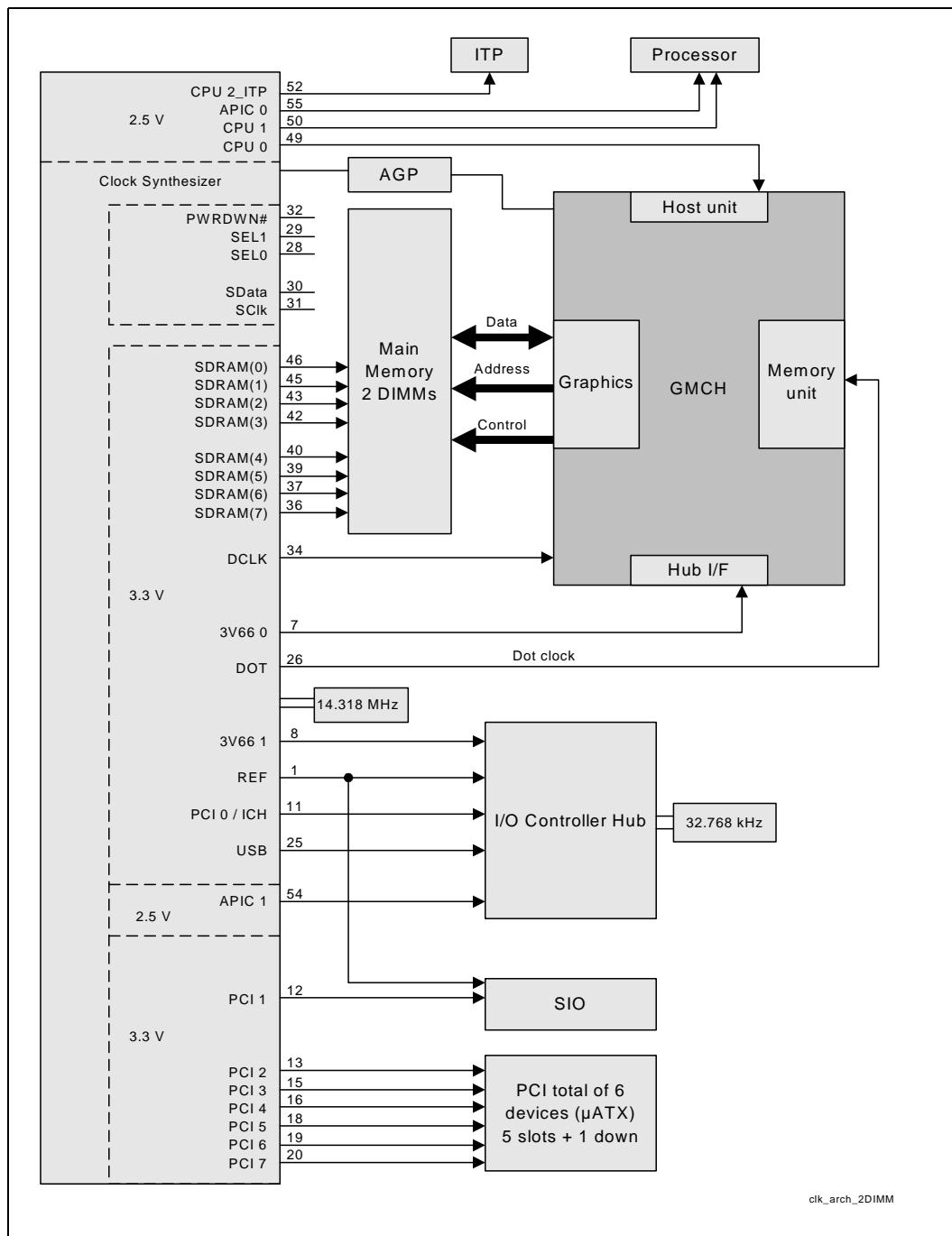
12.2 Three-DIMM Clocking

Table 34 shows the characteristics of the clock generator for a 3-DIMM solution.

Table 34. Intel® CK-815 (3-DIMM) Clocks

Number	Clock	Frequency
2	processor clocks	66/100/133 MHz
13	SDRAM clocks	100/133 MHz
2	PCI clocks	33 MHz
1	APIC clocks	33 MHz
2	48 MHz clocks	48 MHz
3	3 V, 66 MHz clocks	66 MHz
1	REF clock	14.31818 MHz

The following bullets list the features of the Intel CK-815 clock generator in a 3-DIMM solution:

- Thirteen copies of SDRAM clocks
- Two copies of PCI clock
- One copy of APIC clock
- One copy of 48 MHz USB clock (3.3 V) (non-SSC) (type 3 buffer)
- One copy of 48 MHz DOT clock (3.3 V) (non-SSC) (see DOT details)
- Three copies of 3 V, 66 MHz clock (3.3 V)
- One copy of ref. clock at 14.31818 MHz (3.3 V)
- Ref. 14.31818 MHz xtal oscillator input
- Spread-spectrum support
- I^2C support for turning off unused clocks

Figure 90 shows the Intel 815E chipset platform clock architecture for a 3-DIMM solution.

Figure 90. Platform Clock Architecture for a Three-DIMM Solution
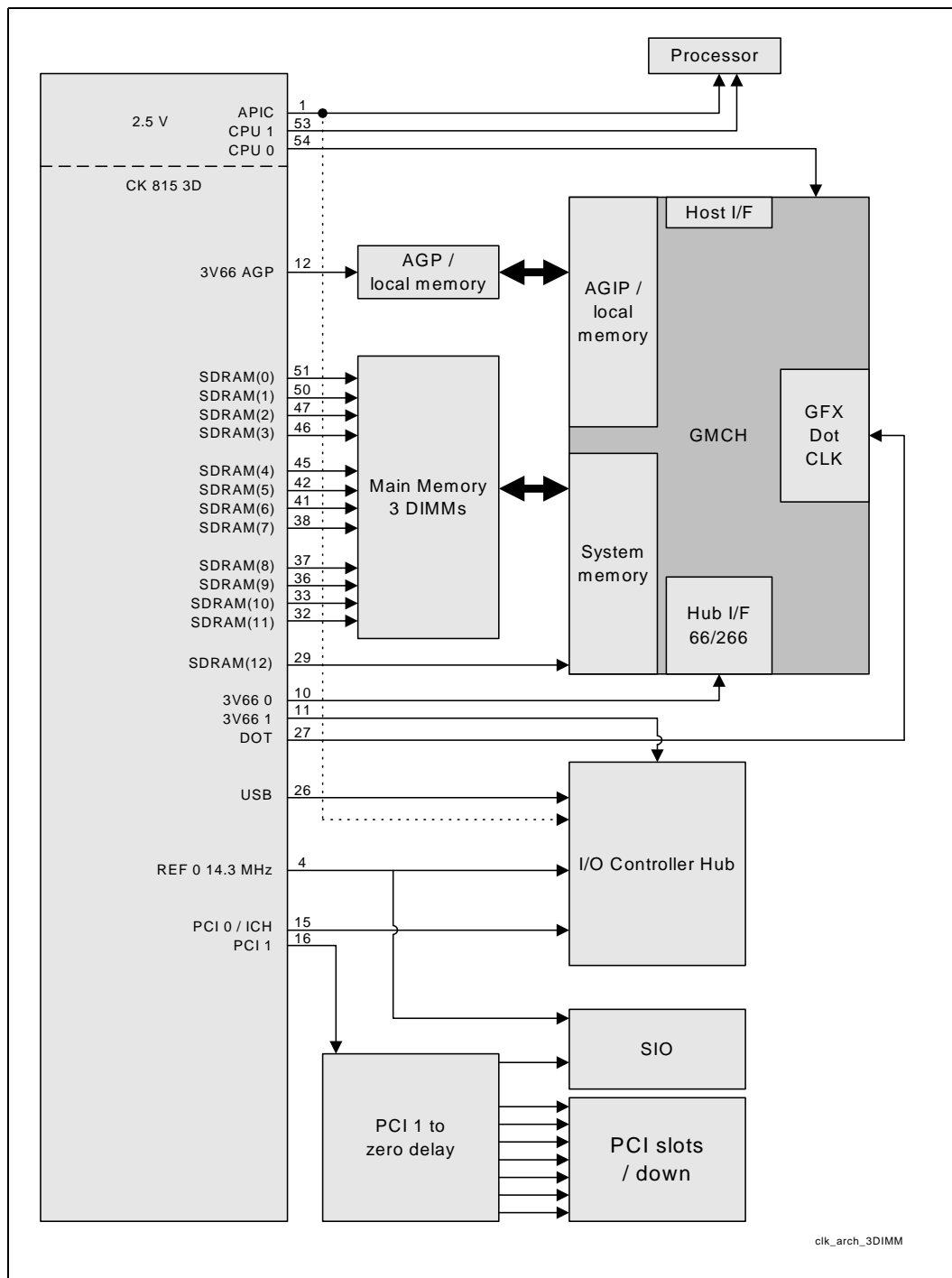
12.3   Clock Routing Guidelines

This section presents the generic clock routing guidelines for both 2-DIMM and 3-DIMM boards. For 3-DIMM boards, additional analysis must be performed by the motherboard designer to ensure that the clocks generated by the external PCI clock buffer meet the PCI specifications for clock skew at the receiver, when compared with the PCI clock at the ICH2.

Figure 91. Clock Routing Topologies
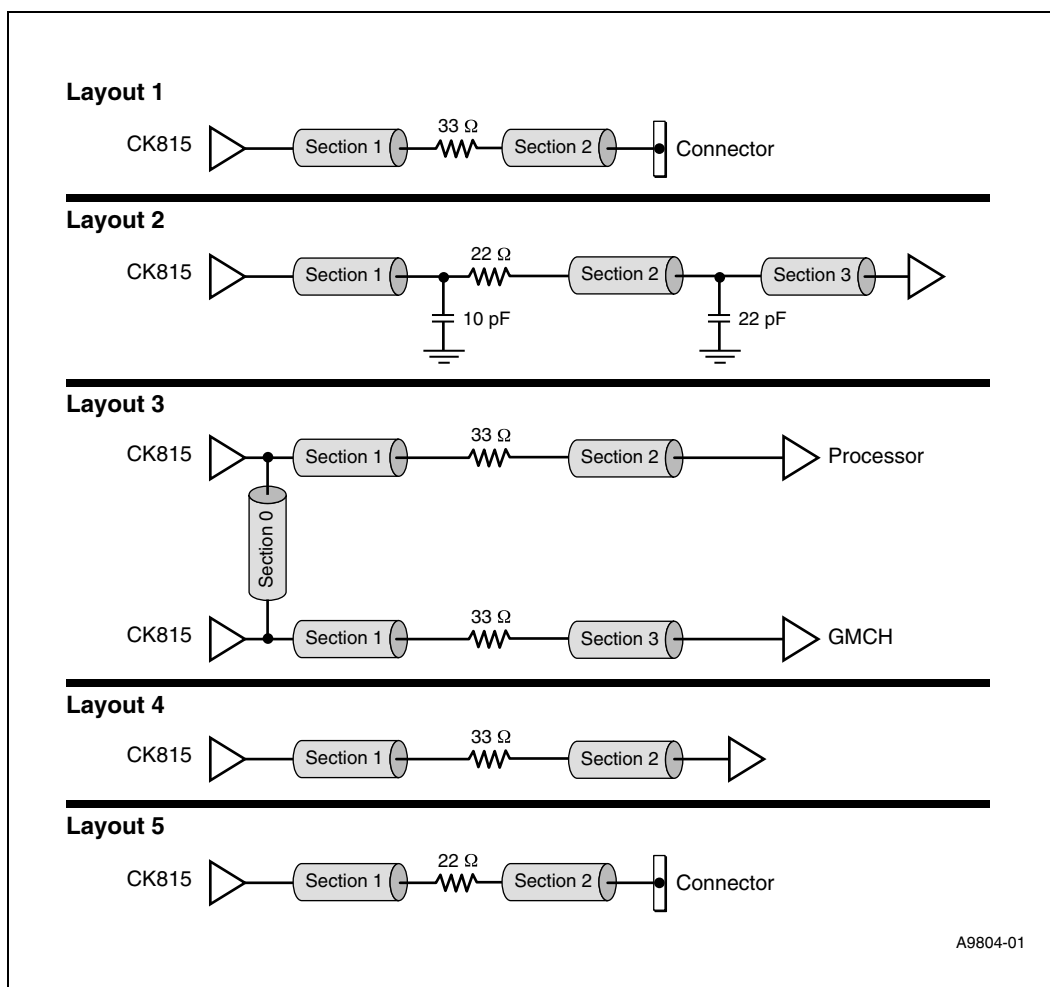
Table 35. Simulated Clock Routing Solution Space

Destination	Topology from Previous Figure	Section 0 Length	Section 1 Length	Section 2 Length	Section 3 Length
SDRAM MCLK	Layout 5	N/A	< 0.5"	A[1]	N/A
GMCH SCLK[3]	Layout 2	N/A	< 0.5"=L1	A + 3.5" – L1	0.5"
Processor BCLK	Layout 3	< 0.1"	< 0.5"	A + 5.2"	A + 8"
GMCH HCLK			<0.5"		
GMCH HUBCLK	Layout 4	N/A	<0.5"	A + 8"	N/A

Table 35. Simulated Clock Routing Solution Space

ICH2 HUBCLK	Layout 4	N/A	<0.5"	A + 8"	N/A
ICH2 PCICLK	Layout 4	N/A	<0.5"	A + 8"	N/A
AGP CLK	Layout 4	N/A	<0.5"	A + 3" to A + 4"	N/A
PCI down[2]	Layout 4	N/A	<0.5"	A + 8.5" to A + 14"	N/A
PCI slot[2]	Layout 1	N/A	<0.5"	A + 5" to A + 11"	

NOTES:
1. Length "A" has been simulated up to 6 inches. The length must be matched between SDRAM MCLK lines by ±100 mils.
2. All PCI clocks must be within 6 inches of the ICH2 PCICLK route length. Routing on PCI add-in cards must be included in this length. In the presented solution space, ICH2 PCICLK was considered to be the shortest in the 6 inches trace routing range, and other clocks were adjusted from there. The system designer may choose to alter the relationship of PCI device and slot clocks, as long as all PCI clock lengths are within 6 inches. Note that the ICH2 PCICLK length is fixed to meet the skew requirements of ICH2 PCICLK to ICH2 HUBCLK.
3. 22 pF Load cap should be placed 0.5 inch from GMCH Pin.

General Clock Layout Guidelines

- All clocks should be routed 5 mils wide with 15 mil spacing to any other signals.

- It is recommended to place capacitor sites within 0.5 inch of the receiver of all clocks. They are useful in system debug and AC tuning.

- Series resistor for clock guidelines: 22 Ω for GMCH SCLK and SDRAM clocks. All other clocks use 33 Ω.

- Each DIMM clock should be matched within ±10 mils.

Clock Decoupling

Several general layout guidelines should be followed when laying out the power planes for the CK815 clock generator, as follows:

- Isolate power planes to the each of the clock groups.

- Place local decoupling as close as possible to power pins, and connect with short, wide traces and copper.

- Connect pins to appropriate power plane with power vias (larger than signal vias).

- Bulk decoupling should be connected to a plane with 2 or more power vias.

- Minimize clock signal routing over plane splits.

- Do not route any signals underneath the clock generator on the component side of the board.

- An example signal via is a 14 mil finished hole with a 24 mil to 26 mil path. An example power via is an 18 mil finished hole with a 33 mil to 38 mil path. For large decoupling or power planes with large current transients, a larger power via is recommended.

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12.4 Clock Driver Frequency Strapping

An Intel CK-815-compliant clock driver device uses two of its pins to determine whether processor clock outputs should run at 133 MHz, 100 MHz or 66 MHz. The pin names are SEL0 and REF0. In addition, a third strapping pin is defined (SEL1), which must be pulled High for normal clock driver operation.

SEL0 and REF0 are driven by either the processor, which depends on the processor populated in pull-up resistors on the motherboard. While SEL0 is a pure input to an Intel CK-815-compliant clock driver, REF0 is also the 14 MHz output that drives the ICH2 and other devices on the platform. In addition to sampling BSEL[1:0] at reset, Intel CK-815-compliant clock drivers are configured by the BIOS via a two-wire interface to drive SDRAM clock outputs at either 100 MHz (default) or 133 MHz (if all system requirements are met).

12.5 Clock Skew Assumptions

The clock skew assumptions in are used in the system clock simulations.

Table 36. Simulated Clock Skew Assumptions

Skew Relationships	Target	Tolerance (±)	Notes
HCLK @ GMCH to HCLK @ processor	0 ns	150 ps	Assumes ganged clock outputs will allow max of 50 ps skew
HCLK @ GMCH to SCLK @ GMCH	0 ns	600 ps	500 ps pin-to-pin skew 100 ps board/package skew
SCLK @ GMCH to SCLK @ SDRAM	0 ns	630 ps	250 ps pin-to-pin skew 380 ps board + DIMM variation
HLCLK @ GMCH to SCLK @ GMCH	0 ns	900 ps	500 ps pin-to-pin skew 400 ps board/package skew
HLCLK @ GMCH to HCLK @ GMCH	0 ns	700 ps	500 ps pin-to-pin skew 200 ps board/package skew
HLCLK @ GMCH to HLCLK @ ICH	0 ns	375 ps	175 ps pin-to-pin skew 200 ps board/package skew

Table 36. Simulated Clock Skew Assumptions

Skew Relationships	Target	Tolerance (±)	Notes
HLCLK @ ICH to PCICLK @ ICH	0 ns	900 ps	500ps pin-to-pin skew 400 ps board/package skew
PCICLK @ ICH to PCICLK @ other PCI devices	0 ns	2.0-ns window	500 ps pin-to-pin skew 1.5 ns board/add-in skew
HLCLK @ GMCH to AGPCLK @ connector			Total electrical length of AGP connector + add-in card is 750 ps (according to AGP2.0 spec and AGP design guide 1.0). Motherboard clock routing must account for this additional electrical length. Therefore, AGPCLK routed to the connector must be shorter than HLCLK to the GMCH, to account for this additional 750 ps.

12.6   Intel® CK-815 Power Gating On Wake Events

Special handling of wake events is required. When a wake event is triggered, the GMCH and the Intel CK-815 must not sample BSEL[1:0] until the signal VTTPWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the Intel CK-815-compliant clock driver until schematic signal VTTPWRGD12 is asserted.

2. Clocks to the ICH2 stabilize before the power supply asserts PWROK to the ICH2. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus it is necessary to gate PWROK to the ICH2 from the power supply while the Intel CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.

3. ICH2 takes the GMCH out of reset.

4. GMCH samples BSEL[1:0]. Intel CK-815 will have sampled BSEL[1:0] much earlier.

Refer to Section 4.3 for full implementation details.

Power Delivery   **13**

This chapter contains power delivery guidelines. Table 37 provides definitions fro power delivery terms used in this chapter.

Table 37. Power Delivery Definitions

Term	Description
Suspend-To-RAM (STR):	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board (CRB) to satisfy the S3 ACPI power management state.
Full-power operation:	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (processor stop-grant state) state.
Suspend operation:	During suspend operation, power is removed from some components on the motherboard. The CRB supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Power rails:	An ATX power supply has 6 power rails: +5 V, –5 V, +12 V, –12 V, +3.3 V, 5 VSB. In addition to these power rails, several other power rails are created with voltage regulators on the CRB.
Core power rail:	A power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are: ±5 V, ±12 V and +3.3 V.
Standby power rail:	A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5 VSB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail:	A *derived* power rail is any power rail that is generated from another power rail. For example, 3.3 VSB is usually derived (on the motherboard) from 5 VSB using a voltage regulator (on the CRB, 3.3 VSB is derived from 5 V_DUAL).
Dual power rail:	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

Figure 100 shows the power delivery architecture for an example system based on the Intel 815E platform. This power delivery architecture supports the "Instantly Available PC Design Guidelines" via the *suspend-to-RAM* (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH2 resume well, PCI wake devices (via 3.3 Vaux), AC'97, and optionally USB. (USB can be powered only if sufficient standby power is available.) To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *full-power*. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions in this design guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 92. Power Delivery Map
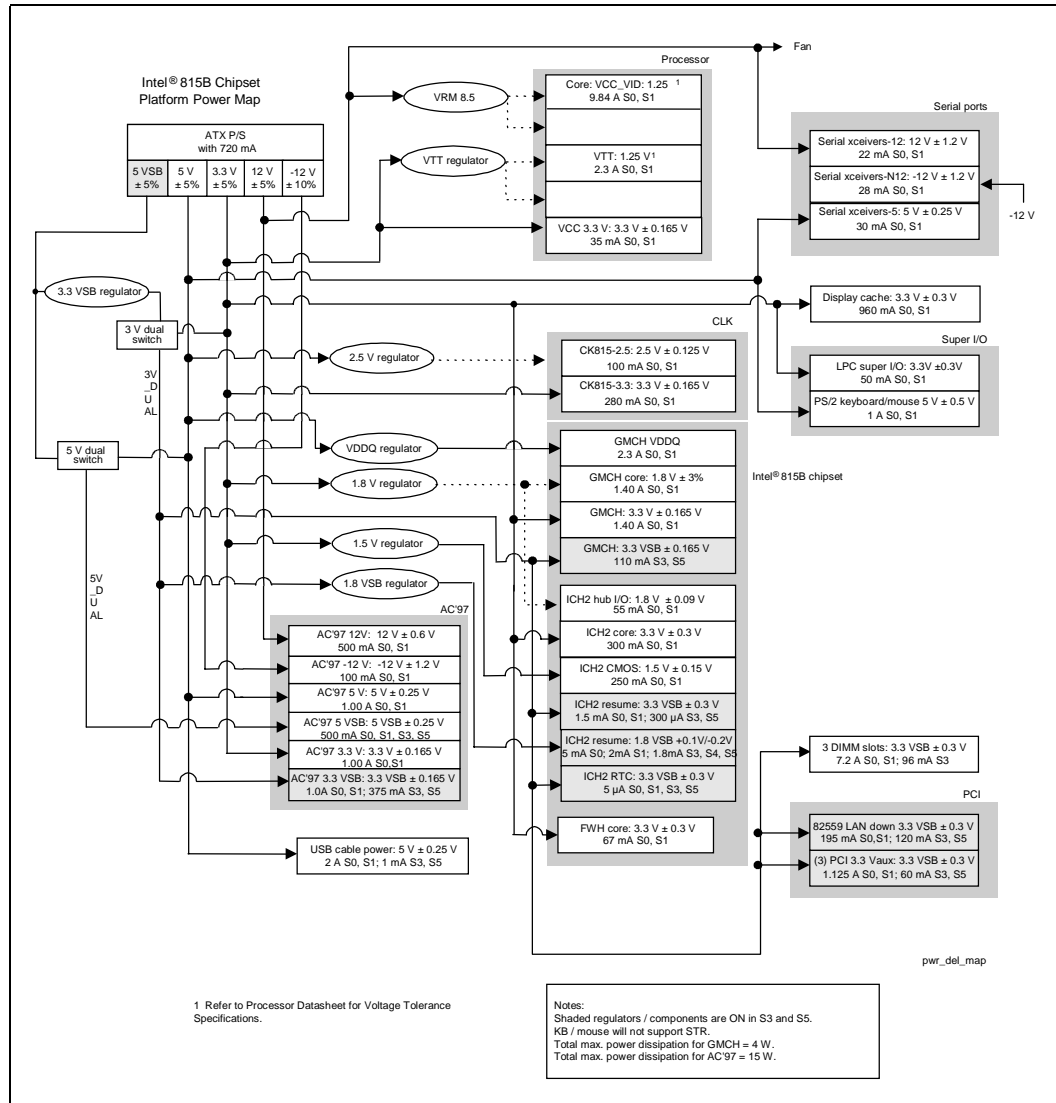
In addition to the power planes provided by the ATX power supply, an *instantly available* Intel 815 platform (using *Suspend-to-RAM)* requires six power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the CRB will have a *5 V Dual Switch*.

5 V Dual Switch

This switch will power the *5 V Dual plane* from the 5 V core ATX supply during *full-power* operation. During *Suspend-to-RAM,* the *5 V Dual plane* will be powered from the 5 V Standby power supply. Note: the voltage on the 5 V Dual plane is not 5 V! There is a resistive drop through

the *5 V Dual Switch* that must be considered. Therefore, NO COMPONENTS should be connected directly to the 5 V Dual plane. On the CRB, the only devices connected to the 5 V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in an Intel®815 platform that does not support Suspend-to-RAM (STR).

VTT

This power plane is used to power the AGTL termination resistors. Refer to the latest revisions of:

- Low Voltage Intel® Pentium® III Processor 512K LP/ULP (DP) Electrical, Mechanical and Thermal Specification

Note: This regulator is required in ALL designs.

1.85 V

The 1.85 V plane powers the GMCH core and the ICH2 hub interface I/O buffers. This power plane has a total power requirement of approximately 1.7A. The 1.85 V plane should be decoupled with a 0.1 µF and a 0.01 µF chip capacitor at **each** corner of the GMCH, and with a single 1 µF and 0.1 µF capacitor at the ICH2.

Note: This regulator is required in ALL designs.

VDDQ

The VDDQ plane is used to power the GMCH AGP interface and the graphics component AGP interface. Refer to the AGP Interface Specification Revision 2.0 (http://www.agpforum.org) and ECR#43 and ECR#44 for specific VDDQ delivery requirements.

For the consideration of component long-term reliability, the following power sequence is strongly recommended while the AGP interface of GMCH is running at 3.3 V. If the AGP interface is running at 1.5 V, the following power sequence recommendation is no longer applicable. The power sequence recommendations are:

- During the power-up sequence, the 1.85 V must ramp up to 1.0 V BEFORE 3.3 V ramps up to 2.2 V

- During the power-down sequence, the 1.85 V cannot ramp below 1.0 V BEFORE 3.3 V ramps below 2.2 V

- The same power sequence recommendation also applies to the entrance and exit of S3 state, since MCH power is compete off during the S3 state.

Refer to Figure 13.3.2 for more information on the power ramp sequence requirement between 3.3 V and 1.85 V. System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply. For further details on the voltage sequencing requirements, refer to the *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet.*

Note: This regulator is required in **all** designs (unless the design does not support 1.5 V AGP, and therefore does not support 4X AGP).

3.3 VSB

The 3.3 VSB plane powers the I/O buffers in the resume well of the ICH2 and the PCI 3.3 Vaux suspend power pins. The 3.3 Vaux requirement state that during suspend, the system must deliver 375 mA to each *wake-enabled* card and 20 mA to each *non wake-enabled* card. During *full-power* operation, the system must be able to supply 375 mA to *EACH* card. Therefore, the total current requirement is:

- *Full-power Operation:* 375 mA * number of PCI slots

- *Suspend Operation:* 375+20 mA* (number of PCI slots – 1)

In addition to the PCI 3.3 Vaux, the ICH2 suspend well power requirements must be considered as shown in Figure 92.

Note: This regulator is required in **all** designs.

1.85 VSB

The 1.85 VSB plane powers the logic to the resume well of the ICH2. This should not be used for VCMOS.

VCMOS

The VCMOS plane is used to power the processor CMOS signals. Given that VTT is 1.25 V, it is necessary to provide VCMOS as its own separate plane.

13.1   Thermal Design Power

The Thermal Design power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP of the GMCH component is 5.1W.

The TDP of the ICH2 is 1.5 W ±15%.

13.1.1   Pull-Up and Pull-Down Resistor Values

The pull-up and pull-down values are system dependent. The appropriate value for a system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, the input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high-voltage/low-voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be performed to determine the minimum/maximum values usable on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, and other considerations.

A simplistic DC calculation for a pull-up value is:

Equation 3. $R_{MAX} = (VCC_{PU} MIN - V_{IH} MIN) / I_{LEAKAGE} MAX$

Equation 4. $R_{MIN} = (VCC_{PU} MAX - V_{IL} MAX) / I_{OL} MAX$

Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} also is determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including the input capacitance of the devices to be driven, the output capacitance of the driver, and the line capacitance. This calculation yields the largest pull-up resistor allowable to meet the rise time t.

Equation 5. $R_{MAX} = -t / (C * ln(1-(V_{IH} MIN / VCC_{PU} MIN)))$

Figure 93. Pull-Up Resistor Example
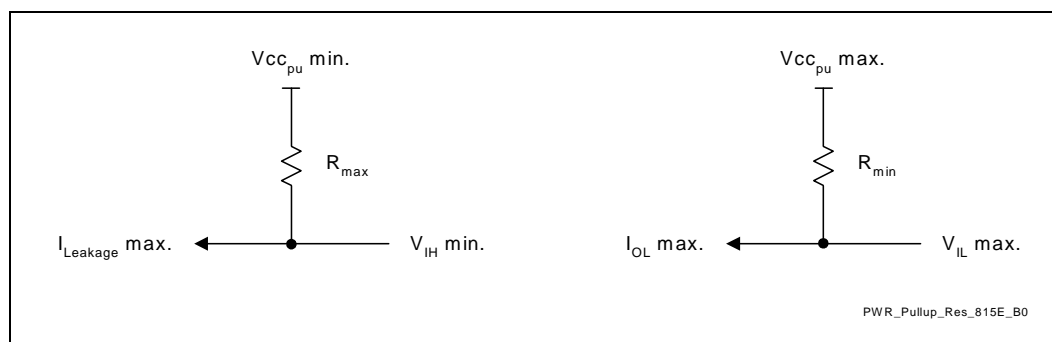
13.2   ATX Power Supply PWRGOOD Requirements

The PWROK signal must be glitch free for proper power management operation. The ICH2 sets the PWROK_FLR bit (ICH2 GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at offset A2h). If this bit is set upon resume from S3 power-down, the system will reboot and control of the system will not be given to the program running when entering the S3 state. System designers should insure that PWROK signal designs are glitch free.

13.3   Power Management Signals

- A power button is required by the ACPI specification.

- PWRBTN# is connected to the front panel on/off power button. The ICH2 integrates 16 ms debouncing logic on this pin.

- AC power loss circuitry has been integrated into the ICH2 to detect power failure.

- It is recommended that the ATXPWROK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity. It should not be connected directly to logic on the board.

- PWROK logic from the power supply connector can be powered from the core voltage supply.

- RSMRST# logic should be powered by a standby supply, while making sure that the input to the ICH2 is at the 3 V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).

- It is recommended that 3.3 V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.

- The PWROK signal to the chipset is a 3 V signal.

- The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms.

- PWROK to the chipset must be deasserted after RSMRST#.

- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V, using a 330 Ω resistor. It also has a 1.8 KΩ pull-down to ground.

- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH2 suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.

- SLP_S3# from the ICH2 must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.

- For an ATX power supply, when PSON is Low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

13.3.1   Power Button Implementation

The following items should be considered when implementing a power management model for a desktop system. The power states are as follows:

- S1 – Stop Grant – (processor context not lost)
- S3 - STR (Suspend to RAM)
- S4 - STD (Suspend to Disk)
- S5 - Soft-off

Note the following:

1. *Wake:* Pressing the power button wakes the computer from S1–S5.

2. *Sleep:* Pressing the power button signals software/firmware in the following manner:

   a. If SCI is enabled, the power button will generate an SCI to the OS.

   — The OS will implement the power button policy to allow orderly shutdowns.

   — Do not override this with additional hardware.

   b. If SCI is not enabled:

   — Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.

— Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.

— Always install an SMI handler for the power button that operates until ACPI is enabled.

3. *Emergency Override:* Pressing the power button for 4 seconds goes directly to S5.

   a. This is only to be used in EMERGENCIES when system is not responding.

   b. This will cause the user data to be lost in most cases.

4. Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off. This violates ACPI.

5. To be compliant with the latest PC9x specification, machines must appear to the user to be off when in the S1–S4 sleeping states. This includes:

   — All lights, except a power state light, must be off.

   — The system must be inaudible: silent or stopped fan, drives off.

Note: Contact Microsoft for the latest information concerning PC9x and Microsoft Logo programs.

13.3.2   1.85 V/3.3 V Power Sequencing

The ICH2 has two pairs of associated 1.85 V and 3.3 V supplies. These are {VCC1_85, VCC3_3} and {VCCSus1_85, VCCSus3_3}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.85 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.85 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violation of the 2 V Rule is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.85 V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.85 V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.85 V supply is not.

Figure 94 shows an example power-on sequencing circuit that ensures the 2 V Rule is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.85 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.85 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.85 V plane, current will not flow from the 3.3 V supply into 1.85 V plane when the 1.85 V plane reaches 1.85 V.

Figure 94. Example 1.85 V/3.3 V Power Sequencing Circuit
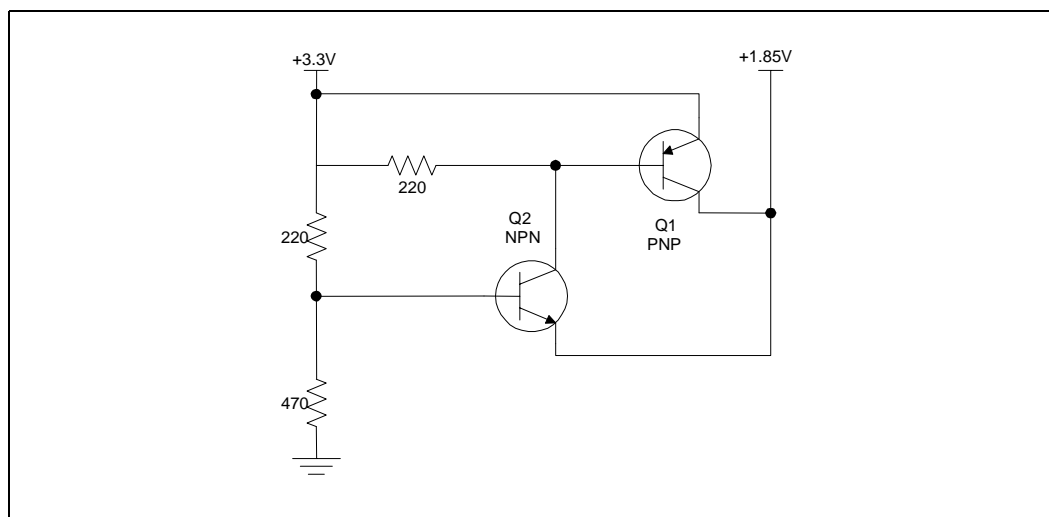
When analyzing systems that may be "marginally compliant" to the 2 V Rule, pay close attention to the behavior of the ICH2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.

- PWROK controls isolation between the Resume wells and Main wells

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

13.3.3   3.3 V/V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH2. V5REF must be powered up before or simultaneously to VCC3_3. It must also power down after or simultaneous to VCC3_3. The rule must be followed to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 95 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VCCSus3_3 rail is derived from the VCCSus5 and therefore, the VCCSus3_3 rail will always come up after the VCCSus5 rail. As a result, V5REF_Sus will always be powered up before VCCSus3_3. In platforms that do not derive the VCCSus3_3 rail from the VCCSus5 rail, this rule must be comprehended in the platform design. As an additional consideration, during suspend the only signals that are 5V tolerant are USBOC. If these signals are not needed during suspend, V5REF_Sus can be hooked to the VCCSus3_3 rail.

Figure 95. 3.3V/V5REF Sequencing Circuitry
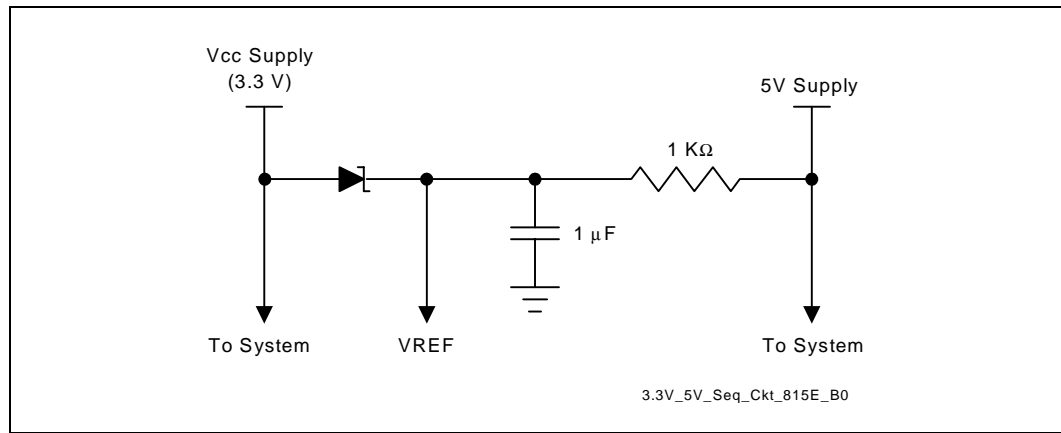
13.4   Power Plane Splits

Figure 96. Power Plane Split Example
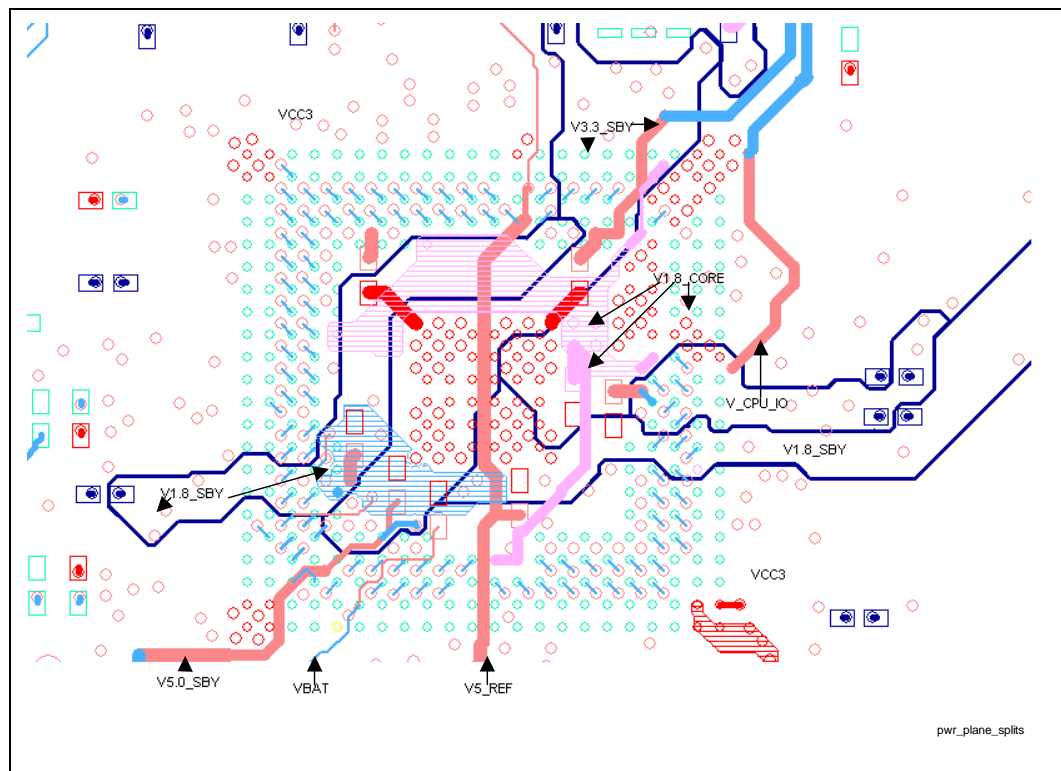
13.5   Glue Chip 3 (ICH2 Glue Chip)

To reduce the component count and BOM cost of the ICH2 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The Glue Chip 3 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- PWROK signal generation
- Control circuitry for Suspend To RAM
- Power Supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for suspend to RAM
- 5 V reference generation
- Flash FLUSH# / INIT# circuit
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for Audio MIDI signal
- Audio-disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test

More information regarding this component is available from the following vendors.

Vendor	Contact	Contact Information
Fujitsu Microelectronics	Customer Response Center	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 *phone:* 1-800-866-8600 *fax:* 1-408-922-9179 *email:* fmicrc@fmi.fujitsu.com
Mitel Semiconductor	Greg Kizik Regional Business Manager	1735 Technology Drive Suite 240 San Jose, CA 95110 *phone:* 408-451-4723 *fax*: 408-451-4710 *e-mail:* greg_kizik@mitel.com http://www.mitelsemi.com

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 intel®

System Design Checklist 14

14.1 Design Review Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an Intel 815E chipset platform for use with the Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor. This is not a complete list and does not guarantee that a design will function properly.

The following set of tables provides design considerations for the various portions of a design. Each table describes one of those portions and is titled accordingly. Contact your Intel Field Representative in the event of questions or issues regarding the interpretation of the information in these tables.

14.2 Processor Checklist

14.2.1 GTL Checklist

Checklist Items	Recommendations
A[35:3]# [1]	• Connect A[31:3]# to GMCH. Leave A[35:32]# as No Connect (not supported by chipset).
BNR#, BPRI#, DBSY#, DEFER#, DRDY#, D[63:0]#, HIT#, HITM#, LOCK#, REQ[4:0]#, RS[2:0]#, TRDY#	• Connect to GMCH.
ADS#	• Resistor site for 56 Ω pull-up to VTT placed within 150 mils of GMCH for debug purpose. Connect to GMCH.
BREQ[0]# (BR0#)	• 33 Ω pull-down resistor to ground
RESET# (B15)	• Terminate to VTT through 56 Ω resistor. Connect to GMCH. For ITP, also connect to ITP pin 2 (RESET#) with 240 Ω series resistor. Terminate at GMCH 56 Ω to VTT.

14.2.2 CMOS Checklist

Checklist Items	Recommendations
IERR#	• 150 Ω pull-up resistor to VCC_{CMOS} if tied to custom logic, or leave as No Connect (not used by chipset)
PREQ#	• 200–300 Ω pull-up resistor to VCC_{CMOS} / Connect to ITP or else leave as No Connect.
THERMTRIP#	• See Section 5.3.1.

Checklist Items	Recommendations
A20M#, IGNNE#, INTR, NMI, SLP#, SMI#, STP-CLK#	• Connect to ICH2. External pull-ups are not needed.
INIT#	• Requires 1K Ω pull-up to 1.5 VCC$_{CMOS}$/Connect to ICH2.
FERR#	• Requires 150 Ω pull-up to VCC$_{CMOS}$/Connect to ICH2.
FLUSH#	• Requires 150 Ω pull-up to VCC$_{CMOS.}$ (Not used by chipset.)
PWRGOOD	• 330 Ω pull-up to VCC2_5 /830Ω pull-down resistor to ground /Connect to POWERGOOD logic.

14.2.3   TAP Checklist

Checklist Items	Recommendations
TCK	• 39 Ω pull-down resistor to ground / Connect to ITP.
TMS	• 39 Ω pull-up resistor to VCMOS / Connect to ITP
TDI	• 200–330 Ω pull-up resistor to VCMOS / Connect to ITP.
TDO	• 150 Ω pull-up resistor to VCMOS / Connect to ITP.
TRST#	• 500-680 Ω pull-down resistor to ground / Connect to ITP.
PRDY#	• Pull-up resistor that matches GTL characteristic impedance to VTT / 240 Ω series resistor to ITP.

Note: Resistors need to be placed within 1 inch of the TAP connector.

14.2.4 Miscellaneous Processor Checklist

Checklist Items	Recommendations
BCLK	• Connect to clock generator. / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the GMCH and processor.
BSEL0 BSEL1	The table below shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the Low Voltage Intel® Pentium® III processor 512K (1.15 V) is 133 MHz. The Ultra Low Voltage Intel® Celeron® (1.10 V or 0.95 V) processor supports only a 100 MHz bus frequency. If another frequency is used, the processor is not guaranteed to function properly. See table below.

BSEL[1:0]	System Bus	Pin Connection
11	133 MHz	For single ended clocking pull both signals up to 3.3 V with a 1 KΩ resistor at the clock generator. NC on processor 0 and 1.
01	100 MHz	For single ended clocking pull BSEL0 up to 3.3 V with a 1K Ω resistor and pull BSEL1 to GND at the clock generator. NC on processor 0 and 1.

Checklist Items	Recommendations
CLKREF	• Connect to divider on VCC2.5 or VCC3.3 to create 1.25 V reference with a 4.7 µF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. Do not use VTT as source voltage for this reference!
PICCLK	• 130 Ω pull-down to GND to generate a 2.0 V clock signal. Connect to clock generator with a 33 Ω series resistor.
PICD[1:0]	• 150 Ω pull-up resistor to VCC_{CMOS}/Connect to ICH2.
PLL1, PLL2	• Low-pass filter on VTT provided on motherboard. Typically a 4.7 µH inductor in series with VTT is connected to PLL1, and then through a series 33 µF capacitor to PLL2.
RTTCTRL	• 56 Ω ±1 % pull-down resistor to ground.
SLEWCTRL	• 110 Ω ± 1% pull-down resistor to ground.
STPCLK#	• Connect to ICH2.
THERMDN, THERMDP	• No Connect if not used. Otherwise, connect to thermal sensor using vendor guidelines.
VCMOS_REF	• Connect to a 1.0 V voltage divider derived from VCC_{CMOS}.
VCCCORE	Connect to core voltage regulator. Provide low frequency decoupling. Guidelines: Place twenty-six 0.47-µF X5R 0603 capacitors directly under the package on the bottom side of the motherboard using at least two vias per capacitor node. Ten 10-µF X7R 6.3 V 1206-size ceramic capacitors should be placed around the package periphery near the balls. Trace lengths to the vias should be designed to minimize inductance. Avoid bending traces to minimize ESL.
VID[25mV, 3:0]	• Connect to on-board VR or VRM. 25mV should connect to VID25mV. For on-board VR, 10 kΩ pull-up resistor to power solution-compatible voltage is required (usually pulled up to input voltage of the VR). Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.
VTTPWRGD	• Pull up to VTT through 1 kΩ resistor and connect to VTTPWRGD circuitry.

Checklist Items	Recommendations
VREF[7:0]	• Connect to VREF voltage divider made up of 75 Ω and 150 Ω 1% resistors connected to VTT. Processor VREF must be able to be separate from chipset VREF. • Decoupling Guidelines: • 4 ea. (min.) 0.1 µF in 0603 package placed within 500 mils of VREF pins
VTT	Connect A26, C5, C7, C9, C11, C13, C15, C17, C19, C21, D5, E4, E6, G4, G23, J4, J23, L4, L23, N23, R23, U23, V4, W23, AA4, AA23, AC4, AC23, AD6, AD8, AD12, AD14, AD18, AD20, AE3, AE18, AF1, AF2 to 1.25 V regulator. Provide high and low frequency decoupling. Guidelines: Place twelve 1-µF X7R 0603 and four 4.7-µF X5R 1206 ceramic capacitors close to the package. Via and trace guidelines are the same as above.
NO CONNECTS	A2, A5, A11, B1, C1, C22, D1, D26, E1, F1, L5, N4, N24, P1, P4, P5, P26, AD4, AD13, AD23, AE8, AF17, AF18
NCHCTRL (N37)	• 14 Ω pull-up resistor to VTT.

14.3 GMCH Checklist

14.3.1 AGP Interface 1X Mode Checklist

Checklist Items	Recommendations
RBF#, WBF#, PIPE#, GREQ#, GGNT#, GPAR, GFRAME#, GIRDY#, GTRDY#, GSTOP#, GDEVSEL#, GPERR#, GSERR#, ADSTB0, ADSTB1, SBSTB	• Pull up to VDDQ through 8.2 kΩ
ADSTB0#, ADSTB1#, SBSTB#	• Pull down to ground through 8.2 kΩ
PME#	• Connect to PCI connector 0 device Ah. / Connect to PCI connector 1 device Bh. / Connect to Intel 82559 LAN (if implemented).
TYPEDET#	• Connect to AGP voltage regulator circuitry / AGP reference circuitry.
PIRQ#A, PIRQ#B	• Pull up to 5 V through 2.7 kΩ. / Follow ref. schematics (other device connections).

14.3.2 Designs That Do Not Use the AGP Port

Any external graphics implementation not using the AGP port should terminate the GMCH AGP control and strobe signals in the following way:

Table 38. Recommendations for Unused AGP Port

Signal	Pull up / Pull Down
FRAME#	Pull-up to +VDDQ
TRDY#	Pull-up to +VDDQ
IRDY#	Pull-up to +VDDQ
DEVSEL#	Pull-up to +VDDQ
STOP#	Pull-up to +VDDQ
SERR#	Pull-up to +VDDQ
PERR#	Pull-up to +VDDQ
RBF#	Pull-up to +VDDQ
WBF#	Pull-up to +VDDQ
INTA#	Pull-up to +VDDQ
INTB#	Pull-up to +VDDQ
PIPE#	Pull-up to +VDDQ
REQ#	Pull-up to +VDDQ
GNT#	Pull-up to +VDDQ
GPAR	Pull-down to Ground using a 100 kΩ resistor
AD_STB[1:0]	Pull-up to +VDDQ
SB_STB	Pull-up to +VDDQ
AD_STB[1:0]#	Pull-down to Ground
SB_STB#	Pull-down to Ground
ST[2:0]	Pull-up to +VDDQ

14.3.3 System Memory Interface Checklist

Checklist Items	Recommendations
SMAx(7:4)	• 10 Ω series reisitor at the GMCH.

14.3.4 Hub Interface Checklist

Checklist Items	Recommendations
HUBREF	• Connect to HUBREF generation circuitry.
HL_COMP	• Pull up to VCC1.85 through 40 Ω (both GMCH and ICH2 side).

14.3.5   Digital Video Output Port Checklist

Checklist Items	Recommendations
DVI Input Reference Circuit	• See reference schematics in the documentation of the third party vendor of the device of choice in your design. The Third-Party Vendor information is a part of this design guide and its associated design guide updates.

14.4   ICH2 Checklist

14.4.1   PCI Interface

Checklist Items	Recommendations
All	• All inputs to the ICH2 must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources. See Section 0 for recommendations.
PERR#, SERR# PLOCK#, STOP# DEVSEL#, TRDY# IRDY#, FRAME# REQ[4:0] #, GPIO[1:0], THRM#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3.3 or a 2.7 kΩ ohm pull-up resistor to VCC5. See PCI 2.2 Component Specification for pull-up recommendations for VCC3.3 and VCC5.
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal. • 33 Ω series resistor to IDE connectors.
PCIGNT#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to VCC3.3.
PME#	• No extra pull-up resistors This signal has an integrated pull-up resistor of 24 kΩ.
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to VCC3.3 is recommended.
GNT[A]#, /GPIO[16], GNT[B]/ GNT[5]#/ GPIO[17]	• No extra pull-up needed. These signals have integrated pull-ups of 24 kΩ. • GNT[A] has an added strap function of "top block swap". The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.

14.4.2   Hub Interface

Checklist Items	Recommendations
HL11	• No pull-up resistor required. Use a no-stuff or a test point to put the ICH2 into NAND chain mode testing
HL_COMP	• Tie the COMP pin to a 40Ω 1% or 2% (or 39 Ω 1%) pull-up resistor (to VCC1.85) via a 10 mil wide, very short (~0.5 inch) trace. ZCOMP No longer supported.

14.4.3 LAN Interface

Checklist Items	Recommendations
LAN_CLK	• Connect to LAN_CLK on Platform LAN Connect Device.
LAN_RXD[2:0]	• Connect to LAN_RXD on Platform LAN Connect Device. ICH2 contains integrated 9 kΩ pull-up resistors on interface.
LAN_TXD[2:0] LAN_RSTSYNC	• Connect to LAN_TXD on Platform LAN Connect Device.

NOTES:
1. LAN connect interface can be left NC if not used. Input buffers internally terminated.
2. In the event of EMI problems during emissions testing (FCC Classifications) you may need to place a decoupling cap (~470 pF) on each of the 4 LED pins. Reduces emissions attributed to LAN subsystem.

14.4.4 EEPROM Interface

Checklist Items	Recommendations
EE_DOUT	• Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector. • Connected to EEPROM data input signal (input from EEPROM perspective and output from ICH2 perspective).
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector. ICH2 contains an integrated pull-up resistor for this signal. • Connected to EEPROM data output signal (output from EEPROM perspective and input from ICH2 perspective).

14.4.5 FWH/LPC Interface

Checklist Items	Recommendations
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	• No extra pull-ups required. ICH2 Integrates 24 kΩ ohm pull-up resistors on these signal lines.

14.4.6　Interrupt Interface

Checklist Items	Recommendations
PIRQ#[D:A]	• These signals require a pull-up resistor. The recommendation is a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3. • In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the ICH2 datasheet. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19.
PIRQ#[G:F]/ GPIO[4:3]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3. • In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the ICH2 datasheet. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23.
PIRQ#[H] PIRQ#[E]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3. • Since PIRQ[H]# and PIRQ[E]# are used internally for LAN and USB controllers, they cannot be used as GPIO(s) pin.
APIC	• If the APIC is used: 150 Ω pull-up resistors on APICD[0:1] Connect APICCLK to CK133 with a 20–33 Ω series termination resistor. • If the APIC is not used on UP systems: The APICCLK can either be tied to GND or connected to CK133, but not left floating. Pull APICD[0:1] to GND through 10 kΩ pull-down resistors. Use pull-downs for each APIC signal. Do not share resistor to pull signals up.

14.4.7　GPIO Checklist

Checklist Items	Recommendations
All	• Ensure ALL unconnected signals are OUTPUTS ONLY!
GPIO[7:0]	• These pins are in the Main Power Well. Pull-ups must use the VCC3.3 plane. Unused core well inputs must either be pulled up to VCC3.3 or be pulled down. Inputs must not be allowed to float. These signals are 5 V tolerant. • GPIO[1:0] can be used as REQ[A:B]#. GPIO[1] can also be used as PCI REQ[5]#.
GPIO[8], [13:11]-	• These pins are in the Resume Power Well. Pull-ups must use the VCCSUS3.3 plane. These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register. Unused **resume** well inputs must be pulled up to VCCSUS3.3. These signals are not 5 V tolerant. • These are the only GPIs that can be used as ACPI compliant wake events.
GPIO[23:16]	• Fixed as output only. Can be left NC. In Main Power Well. GPIO22 is open drain.
GPIO[24,25,27,28]	• These I/O pins can be NC. These pins are in the resume power well.

14.4.8   USB

Checklist Items	Recommendations
USBP[3:0]P USBP[3:0]N	• See Figure 97 for circuitry needed on each differential pair.
VCC USB (Cable power)	• It should be powered from the 5 V core instead of the 5 V standby, unless adequate standby power is available.
Voltage drop considerations	• The resistive component of the fuses, ferrite beads and traces must be considered when choosing components, and power and GND trace widths. Minimize the resistance between the VCC5 power supply and the USB ports to prevent voltage drop. • Sufficient bypass capacitance should be located near the USB receptacles to minimize the voltage drop that occurs during the hot plugging a new device. For more information, see the USB specification.
Fuse	• A fuse larger than 1A can be chosen to minimize the voltage drop.

Figure 97. USB Data Line Schematic
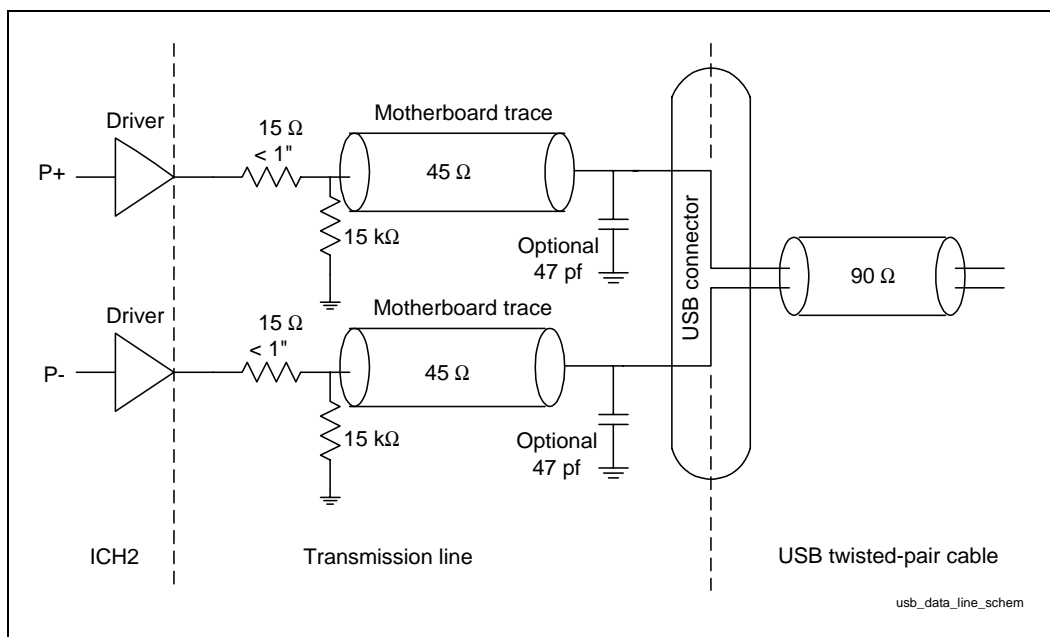
14.4.9   Power Management

Checklist Items	Recommendations
THRM#	Connect to temperature Sensor. Pull-up if not used.
SLP_S3# SLP_S5#	No pull-up/down resistors needed. Signals driven by ICH2.
PWROK	This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and VCC1_8 have reached their nominal voltages.
PWRBTN#	No extra pull-up resistors. This signal has an integrated pull-up of 24 kΩ.
RI#	RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to resume well. If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	Connect to power monitoring logic, and should go high no sooner than 10 ms after both VccSu3_3 and VccSus1_8 have reached their nominal voltages. Requires weak pull-down. Also requires well isolation control.

14.4.10   Processor Signals

Checklist Items	Recommendations
A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#	Internal circuitry has been added to the ICH2, external pull-up resistors are not needed.
FERR#	Requires Weak external pull-up resistor to VCC$_{CMOS}$.
RCIN# A20GATE	Pull-up signals to VCC3.3 through a 10 kΩ resistor.
CPUPWRGD	Connect to the processor's CPUPWRGD input. Requires weak external pull-up resistor.

14.4.11   System Management

Checklist Items	Recommendations
SMBDATA SMBCLK	Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.) Value of pull-up resistors determined by line load. Typical value used is 8.2 kΩ.
SMBALERT#/ GPIO[11]	See GPIO section if SMBALERT# not implemented
SMLINK[1:0]	Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.) Value of pull-up resistors determined by line load. Typical value used is 8.2 kΩ.
INTRUDER#	Pull signal to VCCRTC (VBAT), if not needed.

14.4.12   RTC

Checklist Items	Recommendations
VBIAS	The VBIAS pin of the ICH2 is connected to a .047 μF capacitor. See Figure 98.
RTCX1 RTCX2	Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling capacitors (assuming crystal with C_{LOAD} = 12.5 pF) at each signal. The ICH2 implements a new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in Figure 98 will be required to maintain the accuracy of the RTC. The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds. RTCX1 may optionally be driven by an external oscillator instead of a crystal. These signals are 1.85 V only, and must not be driven by a 3.3 V source.
RTCTST#	Ensure 10–20 ms RC delay (8.2 k and 2.2 μF). Figure 71.

Figure 98. ICH2 Oscillator Circuitry
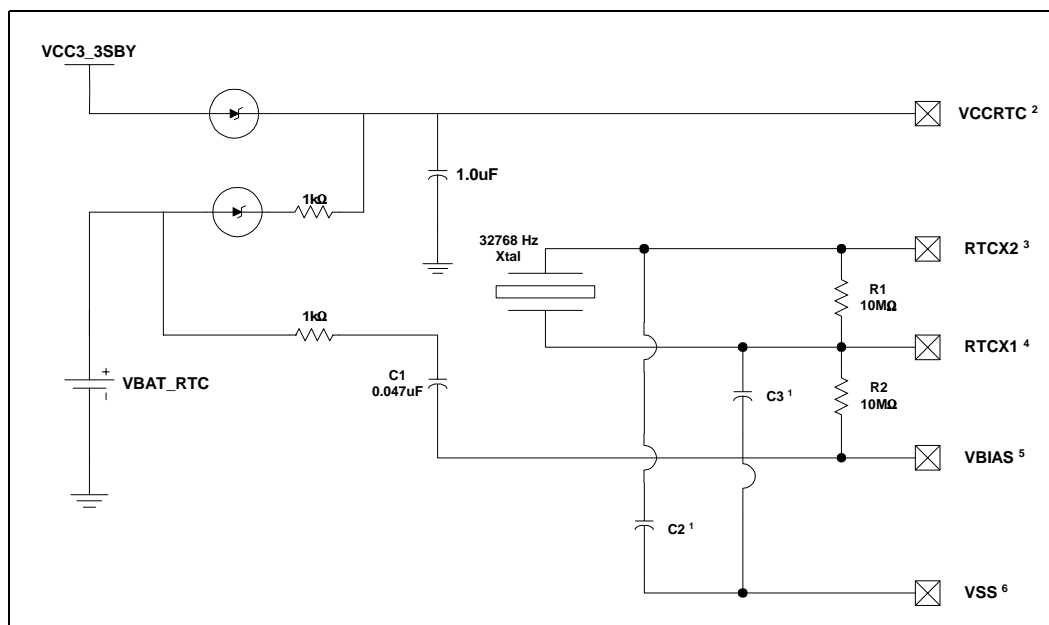
> *Note:*   Capacitors C2 and C3 are crystal dependent

14.4.13   AC'97

Checklist Items	Recommendations
AC_BITCLK	No extra pull-down resistors required. When nothing is connected to the link, BIOS must set a shut off bit for the internal keeper resistors to be enabled. At that point, you do not need pull-ups/pull-downs on any of the link signals.
AC_SYNC	No extra pull-down resistors required. Some implementations add termination for signal integrity. Platform specific.
AC_SDOUT	Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation. This pin has a weak internal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down.
AC_SDIN[1], AC_SDIN[0]	Requires pads for weak 10 kΩ pull-downs. Stuff resistor for unused AC_SDIN signal or AC_SDIN signal going to the CNR connector. AC_SDIN[1:0] are inputs to an internal OR gate. If a pin is left floating, the output of the OR gate will be erroneous. If there is no codec on the system board, then both AC_SDIN[1:0] should be pull-down externally with resisters to ground.
CDC_DN_ENAB#	If the primary codec is down on the motherboard, this signal must be low to indicate the motherboard codec is active and controlling the AC'97 interface.

14.4.14   Miscellaneous Signals

Checklist Items	Recommendations
SPKR	No extra pull-up resistors. Has integrated pull-up of between 18 kΩ and 42 kΩ. The integrated pull-up is only enabled at boot/reset for strapping functions; at all other times, the pull-up is disabled. A low effective impedance may cause the TCO Timer Reboot function to be erroneously disabled. Effective Impedance due Speaker and Codec circuitry must be greater than 50 kΩ or a means to isolate the resistive load from the signal while PWROK is low be found. See Figure 99.
TP[0]	Requires external pull-up resistor to VCCSUS3.3
FS[0]	Rout to a test point. ICH2 contains an integrated pull-up for this signal. Test point used for manufacturing appears in XOR tree.

Figure 99. SPKR Circuitry
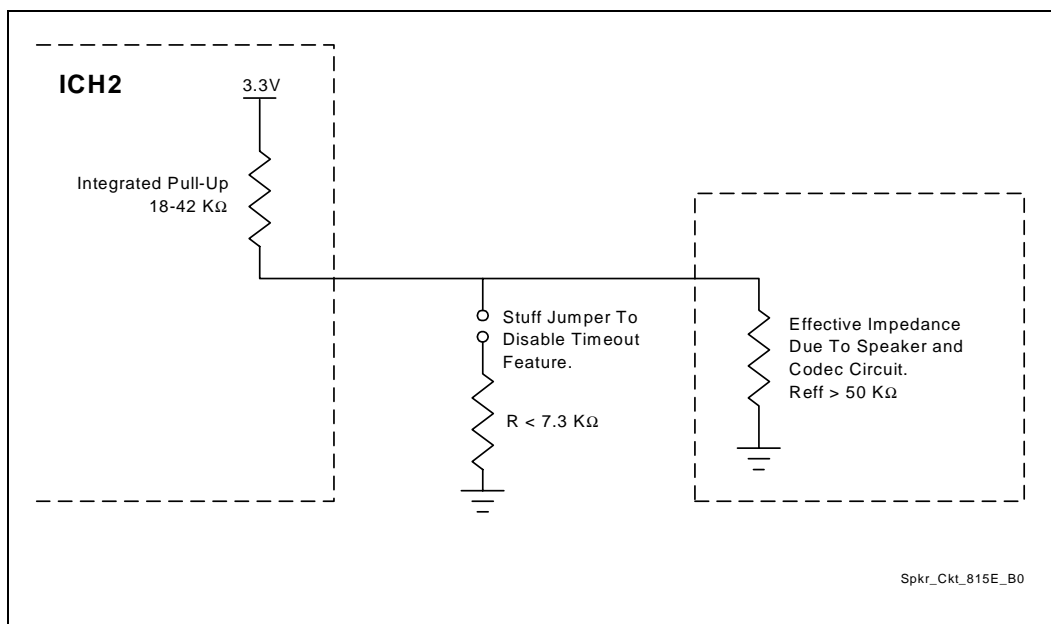
14.4.15   Power

Checklist Items	Recommendations
V_CPU_IO[1:0]	The power pins should be connected to the proper power plane for the processor's CMOS Compatibility Signals. Use one 0.1 μF decoupling capacitor.
VCCRTC	No clear CMOS jumper on VCCRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS
VCC3.3	Requires six 0.1 μF decoupling capacitor
VCCSus3.3	Requires one 0.1 μF decoupling capacitor.

Checklist Items	Recommendations
VCC1.85	Requires two 0.1 μF decoupling capacitor s.
VCCSus1.85	Requires one 0.1 μF decoupling capacitor.
5V_REF SUS	Requires one 0.1 μF decoupling capacitor. V5REF_SUS only affects 5 V tolerance for USB OC[3:0] ins and can be connected to VCCSUS3_3 if 5 V tolerance on these signal is not required.
5V_REF	5VREF is the reference voltage for 5 V tolerant inputs in the ICH2. Tie to pins VREF[2:1]. 5VREF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. Refer to Figure 100 for an example circuit schematic that may be used to ensure the proper 5VREF sequencing.
VCMOS	VCMOS power source must supply 1.5 V and be generated by circuitry on the motherboard. Do not connect to VTT. See Appendix A: Customer Reference Board CRB).

Figure 100. V5REF Circuitry
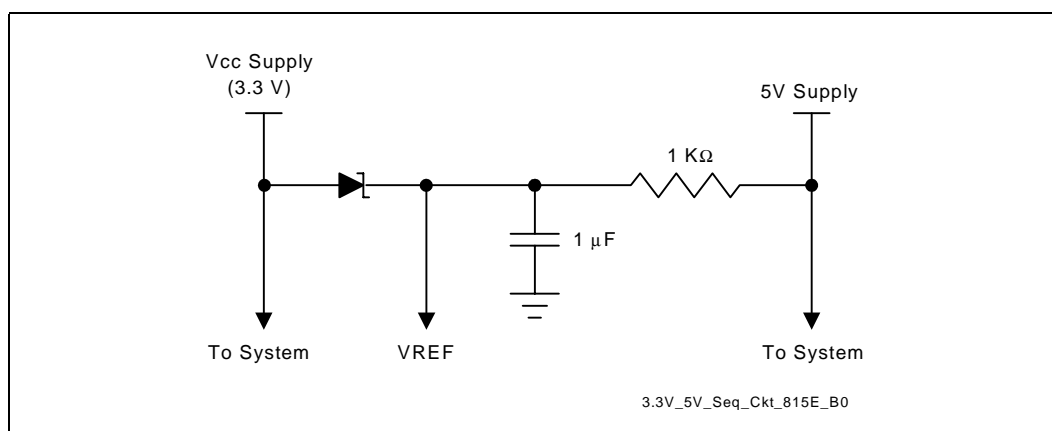
14.4.16 IDE Checklist

Checklist Items	Recommendations
PDD[15:0], SDD[15:0]	No extra series termination resistors or other pull-ups/pull-downs are required. These signals have integrated series resistors. Note that simulation data indicates that the integrated series termination resistors can range from 31 Ω to 43 Ω. PDD7/SDD7 does not require a 10 kΩ pull-down resistor. Refer to ATA ATAPI-4 specification.
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. These signals have integrated series resistors. Note that simulation data indicates that the integrated series termination resistors can range from 31 Ω to 43 Ω.
PDREQ SDREQ	No extra series termination resistors. No pull-down resistors needed. These signals have integrated series resistors in the ICH2. These signals have integrated pull-down resistors in the ICH2.
PIORDY SIORDY	No extra series termination resistors. These signals have integrated series resistors in the ICH2. Pull-up to VCC3.3 via a 4.7 kΩ resistor.

Checklist Items	Recommendations
IRQ14, IRQ15	Recommend 8.2 kΩ∇10 kΩ pull-up resistors to VCC3.3. No extra series termination resistors.
IDERST#	The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.
Cable Detect:	Host Side/Device Side Detection: Connect IDE pin PDIAG/CBLID to an ICH2 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. Device Side Detection: Connect a 0.047 µF capacitor from IDE pin PDIAG/CBLID to GND. No ICH2 connection. Note that all ATA66/ATA100 drives will have the capability to detect cables

Note: The maximum trace length from the ICH2 to the ATA connector is 8 inches.

Figure 101. Host/Device Side Detection Circuitry
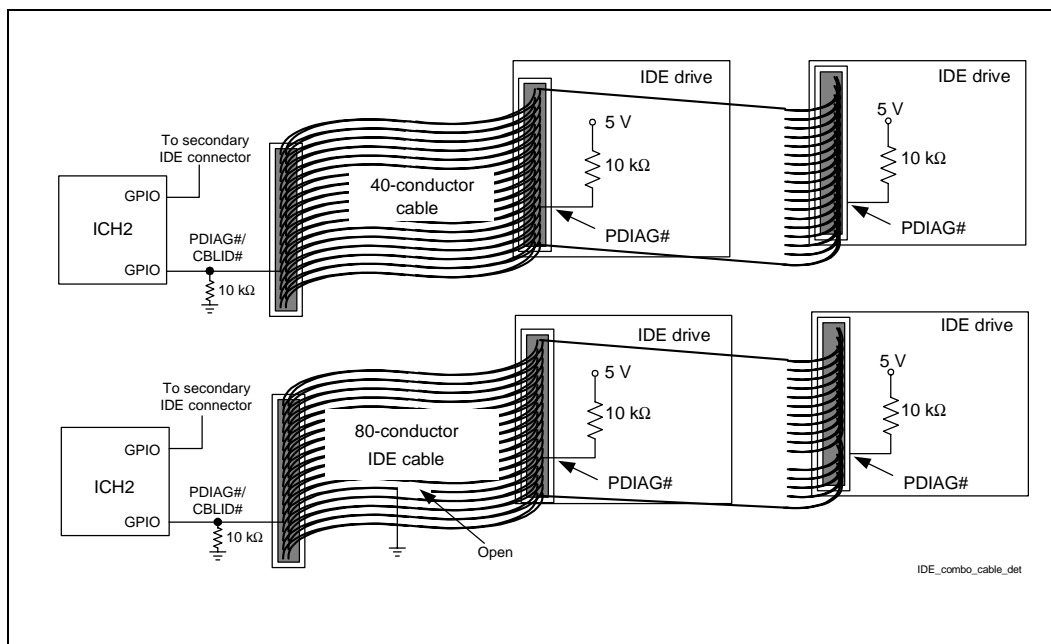
Figure 102. Device Side Only Cable Detection
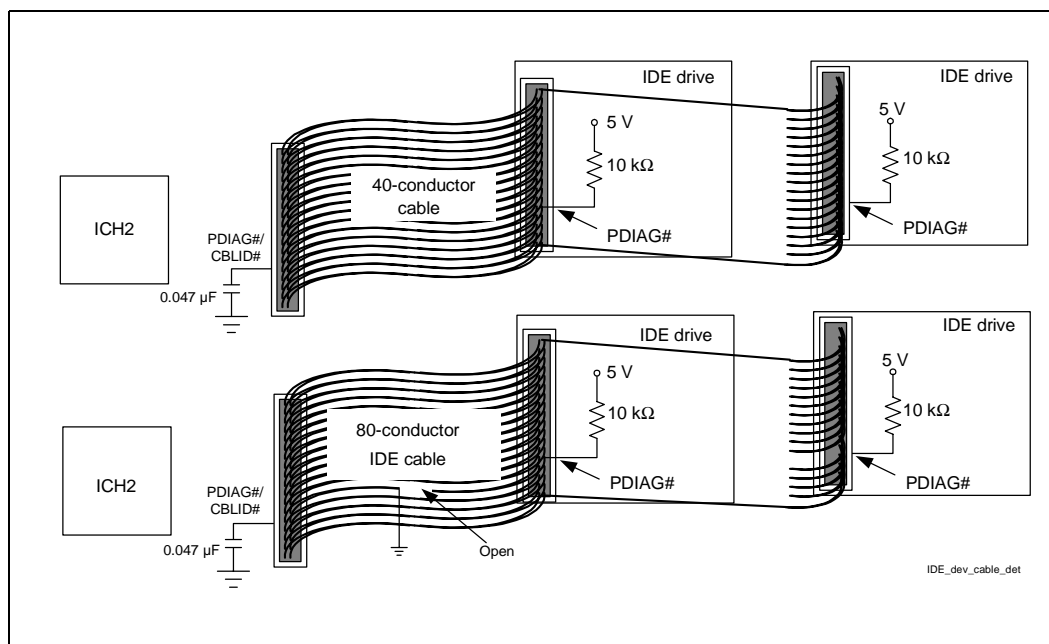
14.5   LPC Checklist

Checklist Items	Recommendations
RCIN#/KBRST#	• Pull up through 8.2 kΩ resistor to VCC3_3.
LPC_PME#	• Pull up through 8.2 kΩ resistor to VCC3_3. Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH2.
J1BUTTON1, J2BUTTON2, J2BUTTON1, J2BUTTON2	• Connect through 1 kΩ series resistor / decouple through 1000 pF capacitor to GND, followed by 4.7 kΩ pull-up to VCC5 / decouple through 470 pF capacitor to GND.
JOY1X, JOY2X, JOY1Y, JOY2Y	• Connect through 1 kΩ series resistor / decouple through 22 pF capacitor to GND, followed by 4.7 kΩ pull-up to VCC5 / decouple through 470 pF capacitor to GND.
A20GATE	• Pull up through 8.2 kΩ resistor to VCC3_3.
CASEOPEN#	• Pull up through 10 MΩ resistor to VCCRTC / connect to switch to GND.
KEYLOCK#	• Pull up through 10 kΩ resistor to VCC5.
MCLK, MDAT, KCLK, KDAT	• Pull up through 4.7 kΩ resistor to VCC5_Dual.
MIDI_IN, MIDI_OUT	• Pull up through 4.7 kΩ resistor to VCC5, followed by 47 Ω series resistor / decouple through a 470 pF capacitor to GND.

Checklist Items	Recommendations
RI#1, CTS#0, RXD1, RXD0, RI#0, DCD#1, DSR#1, DSR#0, DTR#1, DTR#0, DCD#0, RTS#1, RTS#0, CTS#1, TXD1, TXD0	• Decoupled using 100 pF capacitor to GND.
SERIRQ	Pull up through 8.2 kÙ resistor to VCC3_3.
LFRAME#	No required pull-up resistor
LDRQ#0	No required pull-up resistor

14.6   System Checklist

Checklist Items	Recommendations
KEYLOCK#	• Pull up through 10 kΩ resistor to VCC3_3.
PBTN_IN	• Connects to PBSwitch and PBin.
PWRLED	• Pull up through a 220 Ω resistor to VCC5.
R_IRTX	• Signal IRTX after it is pulled down through 4.7 kΩ resistor to GND and passes through 82 Ω resistor.
IRRX	• Pull up to 100 kΩ resistor to VCC3_3. • When signal is input for SI/O decouple through 470 pF capacitor to GND
IRTX	• Pull down through 4.7 kΩ to GND. • Signal passes through 82 Ω resistor. • When signal is input to SI/O decouple through 470 pF capacitor to GND
FP_PD	• Decouple through a 470 pF capacitor To GND. • Pull up 470 Ω to VCC5.
PWM1, PWM2	• Pull up through a 4.7 kΩ resistor to VCC3_3.

14.7 FWH Checklist

Checklist Items	Recommendations
No floating inputs	• Unused FGPI pins must be tied to a valid logic level.
WP#, TBL#	• Connect to ICH2.
VPP	• Pulled up to VCC3_3 and decoupled with a 0.1 μF capacitor to GND.
FGPI0, FGPI1, FGPI2, FPGI3, FPGI4, IC	• Pull down through a 8.2 kΩ resistor to GND.
INIT#	• FWH INIT# must be connected to processor INIT#.
RST#	• FWH RST# must be connected to PCIRST#.
ID[3:0]	• For a system with only one FWH device, tie ID[3:0] to ground.

Note: These recommendations are only valid for the Intel® Firmware Hub.

14.8 Clock Synthesizer Checklist

Checklist Items	Recommendations
REFCLK	• Connects to R-RefCLK, USB_CLK, SIO_CLK14, and ICHCLK14.
ICH_3V66/3V66_0, DOTCLK	• Passes through 33 Ω resistor. • When signal is input for ICH, it is pulled down through a 18 pF capacitor to GND.
DCLK/DCLK_WR	• Passes through 33 Ω resistor. • When signal is input for GMCH, it is pulled down through a 22 pF capacitor to GND.
CPUHCLK/CPU_0_1	• Passes through 33 Ω resistor. • When signal is input for Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor, decouple through a 18 pF capacitor to GND.
R_REFCLK	• REFCLK passed through 10 kΩ resistor. • When signal is input for Low Voltage Intel® Pentium® III processor 512K and Ultra Low Voltage Intel® Celeron® processor, pull up through 1 kΩ resistor to VCC3_3 and pass through 10 kΩ resistor.
USB_CLK, ICH_CLK14	• REFCLK passed through 10 Ω resistor.
XTAL_IN, XTAL_OUT	• Passes through 14.318 MHz oscillator. • Pulled down through 18 pF capacitor to GND.
SEL1_PU	• Pulled up via MEMV3 circuitry through 8.2 kΩ resistor.
FREQSEL	• Connected to clock frequency selection circuitry through 10 kΩ resistor. (See CRB schematic)
L_VCC2_5	• Connects to VDD2_5[0…1] through ferrite bead to VCC2_5.

Checklist Items	Recommendations
GMCHHCLK/CPU_1, ITPCLK/CPU_2, PCI_0/ PCLK_OICH, PCI_1/PCLK_1, PCI_2/PCLK_2, PCI_3/ PCLK_3, PCI_4/PCLK_4, PCI_5/PCLK_5, PCI_6/ PCLK_6, APICCLK_CPU/ APIC_0, APICCLK)ICH/ APIC_1, USBCLK/USB_0, GMCH_3V66/3V66_1, AGPCLK_CONN	• Passes through 33 Ω resistor.
MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7	Pass through 10 Ω resistor.
SCLK	Pass through 22 Ω resistor.
VCC3.3	Connected to VTTPWRGD gating circuit according to information in Section 4.6.1.

14.9   System Memory Checklist

Checklist Items	Recommendations
SM_CSA#[0:3, SM_CSB#[3:0, SMAA[11:8,3:0], SM_MD[0:63], SM_CKE[0:3], S_DQM[0:7]	• Connect from GMCH to DIMM0, DIMM1.
SM_MAA[7:4], SM_MAB[7:4]#	• Connect from GMCH to DIMM0, DIMM1 through 10 Ω resistors.
SM_CAS#	• Connected to R_REFCLK through 10 kΩ resistor.
SM_RAS#	• Jumpered to GND through 10 kΩ resistor.
SM_WE#	• Connected to R_BSEL0# through 10 kΩ resistor.
CKE[5…0] (For 3-DIMM implementation)	• When implementing a 3-DIMM configuration, all six CKE signals on the GMCH are used. (0,1 for DIMM0; 2, 3 for DIMM1; 4,5 for DIMM2)
REGE	• Connect to GND (since this Intel® 815E chipset platform does not support registered DIMMs).
WP (Pin 81 on the DIMMS)	• Add a 4.7 kΩ pull-up resistor to 3.3 V. This recommendation write-protects the DIMMs EEPROM.
SRCOMP	• Needs a 40 Ω resistor pulled up to 3.3 V standby.

14.10   Power Delivery Checklist

Checklist Items	Recommendations
All voltage regulator components meet maximum current requirements.	• Consider all loads on a regulator, including other regulators.
All regulator components meet thermal requirements.	• Ensure the voltage regulator components and dissipate the required amount of heat.
VCC1_8 pins	• These power pins must be supplied by a 1.85 V source and be between (1.795 V to 1.905 V).
If devices are powered directly from a dual rail (i.e., not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET.	• "Dual" voltage rails may not be at the expected voltage.
Dropout voltage	• The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage.
Voltage tolerance requirements are met.	• See the individual component specifications for each voltage tolerance.

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Third-Party Vendor Information **15**

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the Intel 815E chipset platform. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

Super I/O (Vendors Contact Phone)

SMSC	Dave Jenoff (909) 244-4937
National Semiconductor	Robert Reneau (408) 721-2981
ITE	Don Gardenhire (512) 388-7880
Winbond	James Chen (02) 27190505 - Taipei office

Clock Generation (Vendors Contact Phone)

Cypress Semiconductor	John Wunner 206-821-9202 x325
ICS	Raju Shah 408-925-9493
IMI	Elie Ayache 408-263-6300, x235
PERICOM	Ken Buntaran 408-435-1000

Memory Vendors

http://developer.intel.com/design/motherbd/se/se_mem.htm

Voltage Regulator Vendors (Vendors Contact Phone)

Analog Devices	Richard Carlson (408) 382-3258
On Semiconductor	Tod Shift (503) 203-7920
Semtech	Jason Bowles (408) 566-8729
Interisel	Gary Wiggins (360) 921-4421
Fairchild Semiconductor	Ron Lenk (408) 822-2546

Firmware Hub Vendors (Vendors Contact Phone)

Silicon Storage Technology	TBD
STMicroelectronics	TBD

GPA (a.k.a. AIMM) Card (Vendors Contact Phone)

Kingston **JK_TSAI@kingston.com**
 Richard_Kanadjian@kingston.com

Smart Modular **James.Lee@smartm.com**
 Arthur.SAINIO@smartm.com

Micron Semiconductor TBD

TMDS Transmitters

Silicon Images John Nelson (408) 873-3111

Texas Instrument Greg Davis [gdavis@ti.com] (214) 480-3662

Chrontel Chi Tai Hong [cthong@chrontel.com] (408) 544-2150

TV Encoders

Chrontel Chi Tai Hong [cthong@chrontel.com] (408)544-2150

ConexantEileen Carlson [eileen.carlson@conexant.com] (858) 713-3203

Focus Bill Schillhammer [billhammer@focusinfo.com] (978) 661-0146

Philips Marcus Rosin [marcus.rosin@philips.com]

Texas Instrument Greg Davis[gdavis@ti.com] (214) 480-3662

Combo TMDS Transmitters/TV Encoders

Chrontel Chi Tai Hong [cthong@chrontel.com] (408) 544-2150

Texas Instrument Greg Davis[gdavis@ti.com] (214) 480-3662

LVDS Transmitter

National Semiconductor 387R Jason Lu [Jason.Lu@nsc.com] (408) 721-7540

intel®

Support for the Ultra Low Voltage Intel® Celeron® Processors (650 MHz and 400 MHz)   *A*

The ULV Intel Celeron Processor and the LV Intel Pentium III Processor 512K are both pin-for-pin compatible in a 479-pin Micro-FCBGA package. This section contains guidelines for support of the ULV Intel Celeron 650 and 400 processors (CPUID = 06Bxh) in addition to the already supported LV Intel Pentium III 512K.

A.1   BSEL[1:0] Implementation

The ULV Intel Celeron 650 and 400 processors operate at a system bus speed of 100 MHz. In comparison the LV Intel Pentium III 512K operates at a system bus speed of 133 MHz. To indicate 100 MHz operation to the system, BSEL1 must be pulled low by populating R156 in the customer reference schematics. Alternatively, if the platform supports the dynamic VTTPWRGD sequencing by gating power to the system clock generator and core voltage regulator then the platform can allow the populated processor to drive the BSEL[1:0] bits to the appropriate level.

A.2   Voltage Regulator Requirements

One main feature that distinguishes the ULV Intel Celeron from the LV Intel Pentium III 512K is the VID specification that each follows. Unlike the LV Intel Pentium III 512K that follows the VRM8.5 VID code specification (Table 40), the ULV Intel Celeron 650 and 400 processors follow the IMVP-II VID code specification (Table 39). Due to the differences in VID codes, certain considerations will need to be made based on which combination of processors the platform will be targeted at supporting.

A.2.1   No Support for ULV Intel® Celeron 400

If the platform will not be supporting the ULV Intel Celeron 400 processor then a VRM8.5 compatible voltage regulator solution can be used. This implementation will require strapping options of the voltage regulator VID bits to set the appropriate VRM8.5 VID code that corresponds to that of the ULV Intel Celeron 650 core voltage (1.10 V).

A.2.2   Support for the ULV Intel® Celeron 400

To support the ULV Intel Celeron 400 processor the platform requires an IMVP-II voltage regulator solution. Since VRM8.5 VID spec only supports down to a minimum voltage of 1.05 V it is not compatible with the ULV Intel Celeron 400 core voltage of 0.95 V. Strapping options on the VID bits will be required for proper core voltage levels supplied to the LV Intel Pentium III 512K processor.

Table 39. ULV Intel® Celeron® Processor VID Values (IMVP-II)

VID[4:0]	V$_{CC}$ (V)	VID[4:0]	V$_{CC}$ (V)	VID[4:0]	V$_{CC}$ (V)	VID[4:0]	V$_{CC}$ (V)
00000	1.750	01000	1.350	10000	0.975	11000	0.775
00001	1.700	01001	1.300	10001	0.950	11001	0.750
00010	1.650	01010	1.250	10010	0.925	11010	0.725
00011	1.600	01011	1.200	10011	0.900	11011	0.700
00100	1.550	01100	1.150	10100	0.875	11100	0.675
00101	1.500	01101	1.100	10101	0.850	11101	0.650
00110	1.450	01110	1.050	10110	0.825	11110	0.625
00111	1.400	01111	1.000	10111	0.800	11111	0.600

Table 40. LV Intel® Pentium® III Processor 512K VID Values (VRM8.5)

VID[4:0]	V$_{CC}$ (V)	VID[4:0]	V$_{CC}$ (V)	VID[4:0]	V$_{CC}$ (V)	VID[4:0]	V$_{CC}$ (V)
10101	1.825	11001	1.625	11101	1.425	10001	1.225
00101	1.800	01001	1.600	01101	1.400	00001	1.200
10110	1.775	11010	1.575	11110	1.375	10010	1.175
00110	1.750	01010	1.550	01110	1.350	00010	1.150
10111	1.725	11011	1.525	11111	1.325	10011	1.125
00111	1.700	01011	1.500	01111	1.300	00011	1.100
11000	1.675	11100	1.475	10000	1.275	10100	1.075
01000	1.650	01100	1.450	00000	1.250	00100	1.050

Customer Reference Board   B

This appendix provides a set of customer reference board (CRB) schematics for the Intel 815E chipset platform. Schematics are provided for the following items below:

Note: These drawings contain information that has not been verified for manufacturing as an end-user product.

- Block Diagram
- CPU Part 1 and 2
- CPU Part 3 and VTT Decoupling
- Clock Generator
- GMCH Part 1 and 2
- DIMM 1 and 2
- DIMM 3
- AGP
- ICH Part 1 and 2
- PCI 1 and 2
- PCI 3
- Video Bus and Connector
- FWH & UDMA100 IDE 1-2
- USB 0-3
- AC97 CODEC
- Audio I/O
- LPC I/O Controller and FDCL
- WOR, WOL and 2SIP
- KB, MS, Game and IR
- Front Panel and CNR
- ATX Power and H/W Monitor
- VREGS: VDDQ: VCC1_8 and VTT
- VREGS: VCCVID, V1_8SB
- VREGS: Duals, 3.3 SB, 2.5, VCMOS
- PU/PDR and Unused Gates
- Decoupling Capacitors
- Thermtrip

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INTEL(R) LV PENTIUM(R) III 512K
AND ULV CELERON(R)/815E CHIPSET
PLATFORM CUSTOMER REFERENCE
BOARD SCHEMATICS

FAB A
REV 1.0

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATION
2. RESISTORS ARE IN OHM UNLESS OTHERWISE SPECIFIED.
3. VCC= +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

4. VCCP = +1.05 VOLTS UNLESS OTHERWISE SPECIFIED.

3. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.

INTEL(R) LV PENTIUM(R) III PROCESSOR
OR INTEL(R) ULV CELERON(R) PROCESSOR AND 815E CHIPSET

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POWER SUPPLY CONNECTOR

VREG

PROCESSOR (UFCBGA)

CLOCK

FSB (133MHZ)

100/133MHZ CLK

STUFFING OPTION

VGA CONNECTOR

AIMM OR AGP CARD

STUFFING OPTION

DVO HEADER

GMCH

544 PIN BGA

82815

SDRAM 100/133MHZ

100/133MHZ

DIMM 1
DIMM 2
DIMM 3

STUFFING OPTION

HARDWARE MONITOR

SMBUS_AUX

HUB LINK (66MHZ)

SMBUS

STUFFING OPTION

LAN

STUFFING OPTION

WOL HEADER

I/O CONTROLLER HUB (ICH2)

IDE CONNECTOR 1
IDE CONNECTOR 2

PCI BUS (33MHZ)

PCI SLOT 1
PCI SLOT 2
PCI SLOT 3

SMBUS

FLOPPY CONNECTOR

LPC SUPER I/O

LPC BUS

FIRMWARE HUB (4MB FWH, FWHX)

AC LINK

CNR CONN

STUFFING OPTION

RJ-45

STUFFING OPTION

INTEL 815E CHIPSET

PS2 MOUSE/ KEYBOARD CONNECTORS

PARALLEL (1) SERIAL (2) CONNECTORS

USB PORT 1, MJ
USB PORT 2, MJ

AC '97 V2.1 AUDIO CODEC (ADI 1885) (CS 4297)

STUFFING OPTION

10/100MBPS ETHERNET

FP USB PORT 3
FP USB PORT 4 STUFFING OPTION

USB PORT B
USB PORT 4

AMP

STUFFING OPTION

ATAPI CD-ROM
ATAPI AUX IN
ATAPI TELEPHONY

BP CONN LINE IN LINE OUT MIC IN

FP CONN LINE OUT MIC IN

STUFFING OPTION

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CHANDLER, AZ 85226

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[PAGE_TITLE=BLOCK_DIAGRAM]

NOTE :-
USE CYPRESS CY28301 (A44583-001) AS
ALTERNATIVE TO ICS 9250AF-50 (A50310-001)

3CB< 9C1> IN VCC3_CLOCK

BOM=CORE
A50310-001
U2G1
ICS9250-50

BOM=CORE 2 BOM=CORE
R2H14   R2H13
10K   10K
5%   5%
EMPTY   CH
603   603

BOM=CORE
630770-003
Y2G1
14.318MHZ
SM XTAL

Pin	Signal		Pin	Signal	Net
2	X1	24_48MHZ/FS2	35	CK_48M_DOTCLKR	4B4<
3	X2	48MHZ/FS3	34	CK_48M_ICHR	4B4<
22	PD*	REF0/FS4	56	CK_14M_REFR	4C4<
23	SCLK	PCICLK0/FS0	11	CK_P_33M_0R	4D8<
24	SDATA	PCICLK1/FS1	12	CK_P_33M_1R	4D8<

I_P5_U2G1_P2
I_P5_U2G1_P3

9B1 IN CK_PD
BI ICH_SMB_CLK
IN ICH_SMB_DATA

PCI CLKS

PCICLK<2>	13	CK_P_33M_2R	4D8<
PCICLK<3>	15	CK_P_33M_3R	4C8<
PCICLK<4>	16	CK_P_33M_4R	4C8<
PCICLK<5>	17	CK_P_33M_5R	4C8<
PCICLK<6>	19	CK_P_33M_6R	4C8<
PCICLK<7>	20	CK_P_33M_7R	4C8<

1	VDDMAINPLL
9	VDD3V66
10	VDDPCI
18	VDDPCI
25	VDDSDR
32	VDDSDR
37	VDDSDR
45	VDDSDR
33	VDD48PLL
53	VDDLCPU
55	VDDLAPIC

SDRAM CLKS

SDRAM<0>	48	CK_M_1XXM_SDRAM11R	5C7<
SDRAM<1>	47	CK_M_1XXM_SDRAM10R	5C7<
SDRAM<2>	46	CK_M_1XXM_SDRAM9R	5C7<
SDRAM<3>	44	CK_M_1XXM_SDRAM8R	5C7<
SDRAM<4>	43	CK_M_1XXM_SDRAM7R	5C7<
SDRAM<5>	42	CK_M_1XXM_SDRAM6R	5C7<
SDRAM<6>	40	CK_M_1XXM_SDRAM5R	5C7<
SDRAM<7>	39	CK_M_1XXM_SDRAM4R	5C7<
SDRAM<8>	31	CK_M_1XXM_SDRAM1R	5B7<
SDRAM<9>	30	CK_M_1XXM_SDRAM2R	5B7<
SDRAM<10>	27	CK_M_1XXM_SDRAM3R	5B7<
SDRAM<11>	26	CK_M_1XXM_SDRAM0R	5B7<

50	GNDLCPU
36	GND48PLL
4	GNDMAINPLL
5	GND3V66
14	GNDPCI
21	GNDPCI
28	GNDSDR
29	GNDSDR
41	GNDSDR
49	GNDSDR

MISC CLKS

SDRAM_F	38	CK_M_1XXM_DCLKWR	5B7<
IOAPIC	54	CK_33M_APICCPUR	
CPUCLK<1>	51	CK_H_1XXM_CPU_GMCHR	4A8<
CPUCLK<0>	52		
3V66<0>	6	CK_HL_66M_ICHR	4B8<
3V66<1>	7	CK_HL_66M_GMCHR	4A8<
3V66<2>	8	CK_G_66M_AGPR	4B8<

IC

300 OHM, SIZE 1206
BOM=CORE
FB1H1
FB
651080-007

3D7< 9C1> IN VCC3_CLOCK

BOM=CORE
R2G9
0
603 1A
108506-004

I_CK_VCC3_PLL

BOM=CORE
C2G4
2.2UF
10%
X5R
1206
644066-005

BOM=CORE
C2G5
2.2UF
10%
X5R
1206

BOM=CORE
R1H6
10
603 CH
5%
202285-001

I_CK_VCC3_48PLL

BOM=CORE
C1H17
1UF
10%
X7R
603

BOM=CORE
C1H11
10.0UF
20%
25V
1206
108426-120

BOM=CORE
C1H8
10UF
10%
X5R
603
603269-020

41B6< 8D4< 8C2< 43D2>
42AB< IN V_2P5

BOM=CORE
R1G12
0
603 1A CH

I_CK_2P5

BOM=CORE
C1G2
10UF
10%
X5R
1206
644066-005

BOM=CORE
C1G4
10UF
10%
X5R
603

BOM=CORE
C1G3
10UF
10%
X5R
603

BOM=CORE
C1G5
10UF
10%
X5R
603

I_CK_3P3_PCI

BOM=CORE
C1H8
1UF
5%
16V
603

BOM=CORE
C1G12
10.0UF
20%
6.3V
1206
108426-120

BOM=CORE
C1H20
10UF
5%
16V
603

BOM=CORE
C1H19
1UF
5%
16V
603

BOM=CORE
C1H10
1UF
5%
16V
603

BOM=CORE
C1H14
1UF
5%
16V
603

BOM=CORE
C1H18
1UF
5%
16V
603

BOM=CORE
C1H1
1UF
5%
16V
603

BOM=CORE
C1H11
1UF
5%
16V
603

NOTE : NET CK_M_1XXM_SDRAM1R IS COMING FROM PIN 31 OF CLOCK CHIP
       NET CK_M_1XXM_SDRAM3R IS COMING FROM PIN 27 OF CLOCK CHIP

CAD NOTE:
ANY SIGNALS THAT CROSS PLANE
SPLITS WILL REQUIRE STITCHING CAP
ON BOARD CORE DECOUPLING PAGES.

3D PIN CK_P_33M_0R
3D PIN CK_P_33M_1R
3C PIN CK_P_33M_2R
3C PIN CK_P_33M_3R
3C PIN CK_P_33M_4R
3C PIN CK_P_33M_5R
3C PIN CK_P_33M_6R
3C PIN CK_P_33M_7R

1 R2H3 2 BOM=CORE
33 5% 603 CH
CK_P_33M_ICH2 OUT 20B7<> 4D4<

RP2H1 BOM=CORE
8   1
33 5% 063W
SM   IC
CK_P_33M_S1 OUT 4D4< 27C2< 4D4<

RP2H1 BOM=CORE
7   2
33 5% 063W
SM   IC
CK_P_33M_FWH OUT 4D4< 31C5<

1 R2H5 2 BOM=CORE
33 5% 603 CH
CK_P_33M_SIO OUT 32C6<

RP2H1 BOM=CORE
6   3
33 5% 063W
SM   IC
CK_P_33M_S3 OUT 29C2<

RP2H1 BOM=CORE
5   4
33 5% 063W
SM   IC
CK_P_33M_S4 OUT

1 R2H6 2 BOM=CORE
33 5% 603 CH
CK_P_33M_S5 OUT

1 R2H7 2 BOM=CORE
33 5% 603 CH
CK_P_33M_GLUE OUT 40B6<

1 R2H8 2 BOM=CORE
33 5% 603 CH
CK_P_33M_S2 OUT 28C2<

IN CK_P_33M_ICH2 1 R2H1 2 BOM=CORE 10K 5% 603 CH
IN CK_P_33M_S1 1 R2H2 2 BOM=CORE 10K 5% 603 CH
IN CK_P_33M_FWH 1 R2H4 2 BOM=CORE 10K 5% 603 CH

BOM=CORE 1 C2H9 10PF 2 50V EMPTY 603
BOM=CORE 1 C2H4 10PF 2 50V EMPTY 603
BOM=CORE 1 C2H2 10PF 2 50V EMPTY 603

BOM=CORE 1 C2H5 10PF 2 50V EMPTY 603
BOM=CORE 1 C2H3 10PF 2 50V EMPTY 603

BOM=CORE 1 C2H10 10PF 2 50V EMPTY 603
BOM=CORE 1 C2H6 10PF 2 50V EMPTY 603
BOM=CORE 1 C2H13 10PF 2 50V EMPTY 603

BOM=AUD_1885_CK_14M
1 R1G2 2 10 603 EMPTY
CK_14M_AUD OUT 50D1<

3D PIN CK_14M_REFR
RP2G1 BOM=CORE
5   4
33 5% 063W IC
CK_14M_SIO OUT 32A7<

1 R2G4 2 BOM=CORE
10K 5% 603 CH
H_BSEL1 IN

RP2G1 BOM=CORE
2   7
33 5% 063W IC
CK_14M_ICH2 OUT 21B7<

3B PIN CK_33M_APICCPUR
RP2G1 BOM=CORE
6   3
33 IC
CK_APIC_33M_ICH2 OUT 20D5<

RP2G1 BOM=CORE
1   8
33 5% 063W IC
CK_33M_CPU_APIC OUT 9A3<

3D PIN CK_48M_ICHR
1 R1H5 2 BOM=USB_SIO_NOXTAL
22 603 EMPTY
CK_48M_USB OUT 32A8<

1 R2H10 2 BOM=CORE
10K 5% 603 CH
H_BSEL0 IN

1 R1H4 2 BOM=CORE
22 5% 603 CH
CK_USB_48M_ICH2 OUT 21B7<

3D PIN CK_48M_DOTCLKR
1 R1H3 2 BOM=CORE
33 5% 603 CH
CK_V_48M_DOTCLK OUT 11A8<

1 R1H2 2 BOM=CORE
10K 5% 603 CH

3A PIN CK_G_66M_AGPR
1 R2G8 2 BOM=CORE
10 603 CH
CK_G_66M_AGP OUT 17C4<

3A PIN CK_HL_66M_ICHR
1 R2G6 2 BOM=CORE
22 603 CH
CK_HL_66M_ICH2 OUT 21B7<

3A PIN CK_HL_66M_GMCHR
1 R2G7 2 BOM=CORE
22 603 CH
CK_HL_66M_GMCH OUT 13B8<

3B PIN CK_H_1XXM_CPU_GMCHR
1 R1G4 2 BOM=CORE
33 603 CH
CK_H_1XXM_GMCH OUT 13B8<

1 R1G3 2 BOM=CORE
33 603 CH
CK_H_133M_CPU OUT 6A5<

BOM=CORE 1 C2G8 10PF 2 50V EMPTY 603
BOM=CORE 1 C2G6 10PF 2 50V EMPTY 603
BOM=CORE 1 C2G11 10PF 2 50V EMPTY 603
BOM=CORE 1 C2G9 10PF 2 50V EMPTY 603

BOM=CORE 1 C2G3 10PF 2 EMPTY
BOM=CORE 1 C1H3 10PF 2 EMPTY
BOM=CORE 1 C1H 10PF 2 50V

CAD NOTE:
GMCH AND CPU FROM
CLOCK TO RESISTORS
SHOULD BE LESS THAN
200 MILS.

CAD NOTE:
CLOCK TO RESISTORS
SHOULD BE LESS THAN
500 MILS.

NOTE:
DO NOT R-PACK GMCH HOST CLK,
CPU HOST CLK, HUB CLKS,
48MHZ CLKS, OR DCLK

CAD NOTE:
ALL CLOCKS ARE 5 MILS WIDE
AND 15 MILS SPACING

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[PAGE_TITLE=CLOCK]

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

D

C

3C IN CK_M_1XXM_SDRAM11R
3C IN CK_M_1XXM_SDRAM10R
3C IN CK_M_1XXM_SDRAM9R
3C IN CK_M_1XXM_SDRAM8R
3C IN CK_M_1XXM_SDRAM7R
3B IN CK_M_1XXM_SDRAM6R
3B IN CK_M_1XXM_SDRAM5R
3B IN CK_M_1XXM_SDRAM4R
3B IN CK_M_1XXM_SDRAM3R
3B IN CK_M_1XXM_SDRAM2R
3B IN CK_M_1XXM_SDRAM1R
3B IN CK_M_1XXM_SDRAM0R
3B IN CK_M_1XXM_DCLKWR

RP1G1 BOM=CORE
1   8
10 5% 063W
RP1G1 BOM=CORE   IC
2   7
10 5% 063W
RP1G1 BOM=CORE
3   6
10 5% 063W
RP1G1 BOM=CORE   IC
4   5
10 5% 063W
IC

RP1H1 BOM=CORE
1   8
10 5% 063W
RP1H1 BOM=CORE   IC
2   7
10 5% 063W
RP1H1 BOM=CORE
3   6
10 5% 063W
RP1H1 BOM=CORE   IC
4   5
10 5% 063W
SM   IC

1 R2H12 2 BOM=CORE_DIMM0
603 5%
10 CH
1 R1H9 2 BOM=CORE_DIMM0
603 5%
10 CH
1 R1H8 2 BOM=CORE_DIMM0
603 5%
10 CH
1 R2H11 2 BOM=CORE_DIMM0
603 5%
10 CH
1 R1H1 2 BOM=CORE
22 5%
603 CH
BOM=CORE

CK_M_1XXM_DIMM3C OUT 16B6
CK_M_1XXM_DIMM2C OUT 16A6
CK_M_1XXM_DIMM1C OUT 16B7
CK_M_1XXM_DIMM0C OUT 16B7
CK_M_1XXM_DIMM3B OUT 15B4
CK_M_1XXM_DIMM2B OUT 15A4
CK_M_1XXM_DIMM1B OUT 15C4
CK_M_1XXM_DIMM0B OUT 15B4
CK_M_1XXM_DIMM3A OUT 15B8
CK_M_1XXM_DIMM2A OUT 15A8
CK_M_1XXM_DIMM1A OUT 15C8
CK_M_1XXM_DIMM0A OUT 15B8
CK_M_1XXM_DCLKW OUT 12D8

B

BOM=CORE
3 CP1G1
22PF
10%
6 50V
NPO
SM

BOM=CORE
3 CP1H1
22PF
10%
6 50V
NPO
SM

1 C1H14
22PF
CH
2 50V
NPO
B03

1 C1H3
10PF
CH
2 50V
NPO
B03

BOM=CORE
2 CP1G1
22PF
10%
7 50V
NPO
SM

BOM=CORE
4 CP1G1
22PF
10%
5 50V
NPO
SM

BOM=CORE
2 CP1H1
22PF
10%
7 50V
NPO
SM

BOM=CORE
4 CP1H1
22PF
10%
5 50V
NPO
SM

1 C1H15
22PF
CH
2 50V
NPO
B03

1 C2H15
22PF
CH
2 50V
NPO
B03

BOM=CORE
1 CP1G1
22PF
10%
8 50V
NPO
SM

BOM=CORE
1 CP1H1
22PF
10%
8 50V
NPO
SM

BOM=CORE
1 C2H16
22PF
CH
2 50V
NPO
B03

A

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H_D<63..0>*

H_A<31..3>*

H_PWRGD

VCCP

VTT

J3C1
PENTIUM(R)III_LV_UBGA

J3C1
TUAL_LP_UBGA

J3C1
PENTIUM(R)III_LV_UBGA

H_BSEL1
H_BSEL0

PWRGOOD
BSEL<1>
BSEL<0>

ADS*
RP*
AP1*
AP0*
AERR*
HIT*
HITM*
DEFER*

H_ADS*

H_CPURST*
H_INIT*

RESET*
INIT*

H_HITM*
H_DEFER

H_INTR
H_NMI
H_FLUSH_CPU
H_SMI*

INTR/LINT0
NMI/LINT1
FLUSH*
SMI*

TRDY*
RS*<2>
RS*<1>
RS*<0>
RSP*

H_TRDY*

H_APICD1
H_APICD0

PICD<1>
PICD<0>
PICCLK

H_RS<2..0>*

CK_33M_CPU_APIC_2A0V

PD_H_BREQ0*

BREQ1*
BREQ0*

DEP*<7>
DEP*<6>
DEP*<5>
DEP*<4>
DEP*<3>
DEP*<2>
DEP*<1>
DEP*<0>

H_BPRI*
H_BNR*
H_LOCK*

BPRI*
BNR*
LOCK*

H_DBSY*

H_REQ<4..0>*

REQ*<4>
REQ*<3>
REQ*<2>
REQ*<1>
REQ*<0>
DBSY*
DRDY*
VTTPWRGD
THERMTRIP*

H_DRDY*

THERMTRIP_R*

PWRGD_VTT

BINIT*
BERR*
IERR*

H_A20M*

A20M*
FERR*
IGNNE*

H_FERR*

H_IGNNE*

BP*<3>
BP*<2>
BPM*<1>
BPM*<0>

J3C1
TUAL_LP_UBGA

TCK
TDI
TDO
TMS
TRST*

H_SLP*

DPSLP*

RTTIMPEDP

RTTCTRL

V_1P0_CMOS_REF

VCMOS_REF<1>
VCMOS_REF<0>

PLL<2>
PLL<1>

PLL2_C
PLL1_C

H_TESTHI<1>
H_TESTHI<0>
H_TESTLO<1>
H_TESTLO<0>

TESTHI<1>
TESTHI<0>
TESTLO<1>
TESTLO<0>

PREQ*
PRDY*

STPCLK*

CK_H_133M_CPU

CPU_CLKREF

BCLK
BCLK*

VID<4>
VID<3>
VID<2>
VID<1>
VID<0>

H_VID<4>
H_VID<3>
H_VID<2>
H_VID<1>
H_VID<0>

SLEWCTRL
H_TEMP_RET
H_TEMP_SRC

EDGECTRLP
THERMDA
THERMDC

VREF<8>
VREF<7>
VREF<6>
VREF<5>
VREF<4>
VREF<3>
VREF<2>
VREF<1>

NCHCTRLP_R

NCTRL

V_CPU_GTLREF

GND=A25,B2,B4,B6,B8,B10,B12,B14,B16,B18,B20,B22,B26,C23,
C25,D2,D4,D7,D9,D11,D13,D15,D17,D19,D21,E8,E10,E12,E14,
E16,E18,E20,E22,E25,F2,F4,F5,F7,F9,F11,F13,F15,F17,F19,
F21,F23,G6,G22,G25,H2,H4,H5,H21,H23,J6,J22,J25,K2,K4,
K5,K21,K23,L6,L22,L25,M2,M3,M4,M21,M23,N6,N22,N25,P2,
P21,P23,R4,R6,R22,R25,T2,T5,T21,T23,U4,U6,U22,U25,V2,
V5,V21,V23,W4,W6,W22,W25,Y2,Y5,Y21,Y23,AA6,AA8,AA10,AA12,
AA14,AA16,AA18,AA20,AA22,AA25,AB2,AB5,AB7,AB9,AB11,AB13,
AB15,AB17,AB19,AB21,AB23,AC6,AC8,AC10,AC12,AC14,AC16,AC18,
AC20,AC22,AC25,AD2,AE1,AE5,AE7,AE9,AE11,AE13,AE15,AE17,
AE19,AE21,AE23,AE26,AF25,AF26

NC=A2,A5,A11,B1,C1,C22,D1,D26,E1,F1,L5,N4,N24,P1,P4,P5,
P26,AD4,AD13,AD23,AE8,AF17,AF18

1 OF 4
IC

2 OF 4
IC

3 OF 4
IC

4 OF 4
IC

H_TCK
H_TDI
H_TDO
H_TMS
H_TRST*
H_PREQ*
H_PRDY*
H_STPCLK*

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D

22D3< 21D2<
7B8< 8A5>
8D8< 8D2<
40A8<

IN V_1P5_CMOS

BOM=CORE_CPU
R1E1
150
5%
CH
603

BOM=CORE_CPU
R1E4
1K
5%
CH
603

BOM=CORE_CPU
R1D11
150
5%
CH
603

BOM=CORE_CPU
R1C9
150
5%
CH
603

BOM=CORE_CPU
R1D4
150
5%
CH
603

VCCP MUST BE DONE WITH
TRACE (2 INCHES, 5 MIL WIDE)

BOM=CORE_CPU
L1D1
4.7UH
IND
721891-008

6B PIN PLL1_C

VCCP IN

42D2> 43B4> 6D2< 41B5< 45D5<

+ 1C1D1
100.0UF
20V
TANT
DFP

6B OUT PLL2_C

6D5< 40A3> IN H_FLUSH_CPU*
6D5< 40A3> IN H_INIT*
20D4< 6B5> OUT H_FERR*
20B2<> 6C5< BI H_APICD0
20B2<> 6D5< BI H_APICD1

C

RTTCTRL OUT 6B2< 13D2< 9D8< 9C5< 8B7< 8A4< 7B2< 7A8< 6D1< 43C1<
61D7< 45D8< 43B8<

SLEWCTRL OUT 6A5<

PD_H_BREQ0* OUT 6C5<>

IN VTT

BOM=CORE_CPU
R1D6
56.2
1%
CH
603

BOM=CORE_CPU
R2C2
110
1%
CH
603

BOM=CORE_CPU
R1E8
33
5%
CH
603

PLACE CLOSE
TO CPU

BOM=CORE_CPU
R3D3
150
5%
CH
603

BOM=CORE_CPU
R1D5
14
1%
CH
603

NCHCTRLP_R OUT 6A5<

8B3< 6D5< 13C1> OUT H_CPURST*

B

40A8< 22D3<
8D2< 7D8< 6A5>
21D2< 8D8<

IN V_1P5_CMOS

R1D1
220
5%
CH
603

R1
39
5%
CH
603

R5
220
5%
CH
603

R6
150
5%
CH
603

VTT IN

43C1> 6D1< 7A8< 7C4< 8A4< 8B7<
9C5< 9D8< 13D2< 43B8< 45D8< 61D7<

6A5< 8A1> OUT H_PREQ*
6A5< 8B3> OUT H_TMS
6A5< 8A1> OUT H_TDI
8A1> 6A5< IN H_TDO

13C1< 9B7> OUT V_GMCH_GTLREF

BOM=CORE
R3D2
63.4
603

I_V_GMCH_GTLREF

BOM=CORE
FB3D1
FB
693286-001

6A5< 8A1> OUT H_TRST*

R4
470
603

BOM=CORE
C3D3
10%
X5R
603

BOM=CORE
FB1C1
FB
693286-001

SECONDARY SIDE CAP

I_V_CPU_GTLREF

A

8A4< 7C4< 7B2< 6D1< 43C1<
43B8< 13D2< 9D8< 9C5< 8B7<

IN VTT

BOM=CORE
C4D2
10%
X5R
805

BOM=CORE
C4D4
10%
X5R
603

BOM=BACKSIDE_GMCH
C4B1
1UF
10%
EMPTY
603

BOM=CORE
R4D1
150
1%
CH
603

BOM=CORE
R1C3
150
CH
603

BOM=CORE
C1C0
1UF
10%
X5R
603

8A1> 6A5< IN H_PRDY*

BOM=CORE_CPU
R1C4
56
603

5%
CH

V_CPU_GTLREF OUT 6A2<

13C8<> 6D2< OUT H_ADS*

BOM=CORE_CPU
R4E3
56
603

5%
EMPTY

BOM=CORE
C0C4
1UF
10%
X5R
603

BOM=CORE
R2C3
150
1%
CH
603

BOM=CORE
C0D2
1UF
10%
X5R
603

BOM=CORE
C0D43
1UF
10%
X5R
603

BOM=CORE
C0D43
1UF
10%
X5R
603

BOM=CORE
C0D44
1UF
10%
EMPTY
603

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

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V_1P5_CMOS
40A8<
21D2<
7D8<
8A5<
7B8<
8D2<
22D3<

BOM=CORE_CPU
C1F2
1UF
100
X7R
603

BOM=CORE_CPU
C1F1
1UF
100
X7R
603

BOM=CORE_CPU
R1F2
75
1%
CH
603

42A8< 41B6< 8C2< 3B8< 43D2>

V_2P5

BOM=CORE_CPU
R1C7
0
1A
CH
603

21D2< 8D8< 7D8< 7B8< 8A5<
40A8< 22D3>

V_1P5_CMOS

BOM=CORE_CPU
R1F9
150
5%
603

I_V_PU

V_1P0_CMOS_REF   OUT 6B5<

BOM=CORE_CPU
C1F5
1UF
100
X7R
603

BOM=CORE_CPU
R1F1
150
1%
CH
603

BOM=CORE_CPU
R1C8
332
1%
603
202286-147

BOM=CORE_CPU_T
R1C6
330
5%
EMPTY
603

BOM=CORE_CPU_T
Q1C1
EMPTY
SOT23
201924-001

THERMTRIP_R*   6C OUT

1_012R4_3

VCC3

H_PWRGD   6D5< 20C4<

BOM=CORE_CPU
R1F6
150
1%
CH
603
202286-114

CPU_T_HI   IN

BOM=CORE_CPU
C1F6
1UF
500
EMPTY

4D5>
9A3<
9A5<
43C8<

42A8< 41B6< 8D4< 3B8< 43D2>

V_2P5

BOM=CORE_CPU
R1D9
100
1%
CH
603

BOM=CORE_CPU
R3G3
1K
5%
CH
603

BOM=CORE_CPU
R2G3
1K
5%
CH
603

H_TCK   6A5< 8B2< OUT

R8
0   1A
603   CH

UNSTUFF R8
TO USE
ITP

BOM=CORE_CPU
R1F5
590
5%
CH
603
202285-045

CPU_CLKREF   6A OUT

BOM=CORE
C1D4
4.7UF
100
X5R
1206

BOM=CORE
C1D3
1UF
16V
603

BOM=CORE_CPU
R1D8
100   1%
603

H_BSEL0   4B1< 12B1<> 6D5<

R15
30
5%
EMPTY
603

STUFF R15
TO USE
ITP

H_BSEL1   4C1< 12A1<> 6D5<

BOM=CORE_CPU
R2G2
0
1A
EMPTY
603

BSEL1	BSEL0	BUS FREQ
0	0	RSVD (66MHZ)
0	1	RSVD (100MHZ)
1	0	RSVD (200MHZ)
1	1	133MHZ

4B8< 47D7< 47A4< 45C7< 43A8< 41D6< 40D2< 40C2< 40B2<
27D8< 22C7< 22C3< 21A1< 20C1< 20B8< 20B1< 20A6< 49B3<
40A7< 39D3< 39C8< 39D4< 39B3< 39D8< 39A7< 32A1< 29D8<
62C2< 61D4< 61B2< 59C8< 59B7< 59B2< 59B1< 56D8< 48C7<

V_3P3_STBY

R19
240
5%
CH
603

H_TMS   OUT 7B8< 6A5<

H_TCK   OUT 8C6< 6A5<

DBRESET* OUT 39B5<

H_CPURST* IN 7B4< 13C1> 6D5<

R12
240
5%
CH
603

J3
CONN_ITP

VTT   IN
13D2< 9D8< 9C5< 8A4< 7C4< 7B2< 7A8< 6D1< 43C1>
61D7< 45D8< 43B8<

BOM=VREG_VTT_1P5
R1E11
0
1A
EMPTY
805

100 MA MAX NEEDED

VCC

BOM=VREG_1P5_CMOS
305143-001
U1F1
LM317L

IN   OUT 2
     OUT 3
     OUT 5
     OUT 6
ADJ
NC=5,8
IC
4

BOM=VREG_1P5_CMOS
C1F4
22U
20%
16V

I_V_1P5_CMOS

BOM=VREG_1P5_CMOS
R1F3
100
1%
CH
603

BOM=VREG_1P5_CMOS
C1F3
10.0UF
20%
TANT
24MM_3528

V_1P5_CMOS   OUT

7B8< 7D8< 8D2< 8D8< 21D2< 22D3< 40A8<

VTT   IN
43B8< 13D2< 9D8< 9C5< 8B7< 7C4< 7B2< 7A8< 6D1< 43C1>
61D7< 45D8<

BOM=VREG_1P5_CMOS
R1E10
20
1%
CH
603

RESET*   GND
DBRESET*   GND
TCK   GND
TMS   TDI
POWERON   TDO
DBINST*   TRST*
GND   BSEN*
GND   PREQ0*
GND   PRDY0*
GND   PREQ1*
GND   PRDY1*
GND   PREQ2*
GND   PREQ3*
GND   PRDY2*
GND   PRDY3*

R9
1.5K
5%
603

R11
10K
5%
CH
603

FEMALE_1.5V
CONN

H_TDI   OUT 7A8< 6A5<
H_TDO   IN   6A5< 7A8<
H_TRST* IN   7A8< 6A5<
H_PREQ* OUT 7B8< 6A5<

R13
240
5%
CH
603

H_PRDY* IN   6A5< 7A8<

CR-9 : @ECHOBAY_LIB.ECHOBAY(SCH_1):PAGE9
8
7
6
5
4
3
2
1
D
C
B
A
55C5< 49B8< 48B7< 47B8< 46C7< 44D4<
36B2< 35B1< 35A8< 26D8< 26D2< 39A4>
43D2< 43B6< 40C2< 40B2< 39D3<
62D2<
IN
V_5P0_STBY
43B8< 13D2<
8A4< 7C4<
6D1< 43C1>
7B2< 7A8<
9C5< 8B7<
61D7< 45D8<
IN
VTT
R1E2
1K
5%
CH
603
FROM THE PREVIOUS DESIGN THE
VOLTAGE AT THIS NODE WAS
DETERMINED BY THE CPU.
C1E4
.1UF
20%
25V
EMPTY
603
C1E5
.1UF
20%
25V
EMPTY
603
R1E6
2.7K
5%
CH
603
SOT23
I_Q46R4_1
Q1E2
MMBT3906
XSTR
101421-601
R1E5
10K
5%
CH
603
SOT23
R1E3
220
603
5%
CH
202285-033
I_Q4602_1
Q1F1
MMBT3904
XSTR
108969-001
R1E7
10K
5%
CH
603
C1C8
.1UF
20%
25V
EMPTY
603
C1F7
.1UF
20%
25V
EMPTY
603
CPU_T_HI*
OUT
9A7<
CPU_T_HI
OUT
8C4< 9A3< 9A5< 43C8<
THIS NODE HELD
IN HIGH STATE
+12V
R3H3
4.7K
5%
CH
603
43B8< 42A8< 43B2>
PWRGD_VTT_5V*
IN
R1F4
10K
603
5%
CH
C1F7
.1UF
20%
25V
EMPTY
603
SOT23
Q1F1
MMBT3904
XSTR
I_Q1904V_1
108969-001
VCC3
SI2302DS-T1
Q1H1
EMPTY
SOT23
A50095-001
0.3 OHM
300 MA
C1H9
.1UF
10%
16V
X7R
603
C1H5
4.7UF
10%
10V
EMPTY
1206
644066-005
R1H7
0
1A
CH
603
VCC3_CLOCK
OUT
3C8< 3D7<
C1H13
.1UF
10%
16V
X7R
603
C1H16
10.0UF
20%
16V
AL_TANT
4MM_3528
R1H10
10K
5%
EMPTY
603
VCC3
I_PWRGD_VTT_5V
Q2H2
FET
SOT23
201924-001
CK_PD
OUT
3D6<
FOR CLOCK CHIP SPIN EVAL
VCC3
R2
1K
5%
CH
603
RP1
1K
5%
25W
IC
SM
43B8< 13D2< 9D8< 8B7< 8A4< 7C4< 7B2< 7A8< 6D1< 43C1>
61D7< 45D8<
J1
2X5HDR
HDR
6A8
IN
H_VID<4>
H_VID<3>
H_VID<2>
H_VID<1>
H_VID<0>
G_VID<4>
G_VID<3>
G_VID<2>
G_VID<1>
G_VID<0>
OUT
41A6< 42C8<
J2
2X5HDR
HDR
IN
VTT
6B8
OUT
H_TESTHI<1>
R3D4
1K
603
5%
CH
H_TESTHI<0>
R3E5
1K
603
5%
CH
H_TESTLO<1>
R3E4
1K
603
5%
CH
H_TESTLO<0>
R3E2
1K
603
5%
CH
13C1< 7B5>
IN
V_GMCH_GTLREF
R3D1
390
5%
EMPTY
603
I_Q11U1
9D5
IN
CPU_T_HI*
Q4D1
EMPTY
SOT23
201924-001
C4D10
.1UF
20%
EMPTY
603
2.0 MAX, 1.6 MIN HI ON TU 2V SIGNAL
2.5 SIGNAL
4B1
IN
CK_33M_CPU_APIC
R1D3
0
603
1A
CH
108506-004
CK_33M_CPU_APIC_2P0V
OUT
6C5<
R1D2
130
5%
CH
603
I_Q12R2_3
IN
CPU_T_HI
Q1D1
FET
SOT23
201924-001
M_MAA<12>
OUT
12A8< 15C5< 15D8< 16C7<
43C8< 9A5< 8C4< 9D5>
R4E2
10K
5%
CH
603
SOT23
I_Q46R3_3
43C8< 9A3< 8C4< 9D5>
IN
CPU_T_HI
R3F1
220
603
5%
CH
202285-033
I_Q46R3_1
Q3F1
MMBT3904
XSTR
108969-001

VID SETTINGS

MIN	TYP	MAX	VID
1.039	1.050	1.061	00100
1.064	1.075	1.086	10100
1.089	1.100	1.111	00011
1.113	1.125	1.137	10011
1.138	1.150	1.162	00010
1.163	1.175	1.187	10010
1.188	1.200	1.212	00001

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

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D

C

BOM=DIAGLED_DELL
RP5A1
DIAG_THIRD_LED_Y_R   2 —/\/\/— 7
150   5% 063W
SM   EMPTY

BOM=DIAGLED_DELL
RP5A1
DIAG_TOP_LED_Y_R   1 —/\/\/— 8
150   5% 063W
SM   EMPTY

BOM=DIAGLED_DELL
100650-180
U5A2
74HC164

BOM=DIAGLED_DELL
725905-001
DS5A1
1X4 LED ARRAY

20A1 >IN GPIO_DIAGLED_DATA   1 A   Q1 3
                               2 B   Q2 4   DIAG_TOP_LED_G   2 G►|►Y 1 DIAG_TOP_LED_Y
                                     Q3 5
                                     Q4 6   DIAG_THIRD_LED_G 4 G►|►Y 3 DIAG_THIRD_LED_Y
31D7< 21C6< 40A3> >IN PWRGD_3V 9 CLR Q5 10
20A1 >IN GPIO_DIAGLED_STB   8 CLK Q6 11   DIAG_SECOND_LED_G 6 G►|►Y 5 DIAG_SECOND_LED_Y
                                     Q7 12
                                     Q8 13   DIAG_BOTTOM_LED_G 8 G►|►Y 7 DIAG_BOTTOM_LED_Y

VCC3 < 14 VCC GND 7
                     EMPTY   EMPTY

1
BOM=DIAGLED_DELL
CR5A5
20K
2 EMPTY
603

BOM=DIAGLED_DELL
RP5A1
DIAG_BOTTOM_LED_Y_R   4 —/\/\/— 5
150   5% 063W
SM   EMPTY

BOM=DIAGLED_DELL
RP5A1
DIAG_SECOND_LED_Y_R   3 —/\/\/— 6
150   5% 063W
SM   EMPTY

B

ON POWER UP, THIS WILL BE OFF - NO LIGHTS

A

STATUS LED OPTION

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82815E-B (GRAPHICS)   #A08347-006 (S-SPEC) USED IN BOM

NOTE:
10-12 MILS TO GET 37.5 OHMS
SEPERATE BY 25 MILS TO DIGITAL SIGNALS

U4E1

G_AD<31..0>   17DB<>

LTVDATR<11..0>   19B1<>

BOM=CORE
A08347-005

VCC3

V_1P85   IN

61A4< 62D4<
44C1< 13B1< 14A7< 14BB<
19CB< 20C1< 22C3< 22D7<

CORE_RED
CORE_GREEN
CORE_BLUE

82815
PART 1 OF 4
REV 1.1

HSYNC_3V

VSYNC_3V

CAD NOTE:
IREFC 25 MILS MIN.
2 VIAS TO GND MIN
SHORT AS POSSIBLE

DISPLAY CACHE I/F

I_DC_RCLK

DDCSCL_3V
DDCSDA_3V

CK_V_48M_DOTCLK

VCC3

STUFF FOR 815EP

LTVHSYNC   19A4>
LTVVSYNC   19A4>
LTVBLNKR*   19A2<>
LTVCLKIN   19A6>
LTVCLKOUT0R   19A2>
LTVCLKOUT1R   19A2>

LTVCL_3V   19B4<>
LTVDA_3V   19B4<>

G_CBE<3..0>*   17BB<>
G_WBF*   17C1>
G_RBF*   17C1>
G_PIPE*   17C1>
G_TRDY*   17C1<>
G_STOP*   17C1<>
G_REQ*   17C1>
PU_G_RCOMP*
G_PAR   17C1<>
G_IRDY*   17C1<>
G_GNT*   17C1<
G_FRAME*   17C1<
G_DEVSEL*   17C1<>
VREF_AGP_MCH   17B4> 18A4>
G_AD_STB1*   17AB<>
G_AD_STB1   17AB<>
G_AD_STB0*   17AB<>
G_AD_STB0   17AB<>
G_SBSTB*   17AB>
G_SBSTB   17AB>

G_SBA<7..0>   17B8>
G_ST<2..0>   17B8>

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CK_M_1XXM_DCLKW

5B IN

#PLACE CAP WITH 500 MILS
OF PIN F7 ON THE GMCH

BOM=CORE
C2E2
10PF
2 REV
603

U4E1

82815
MEMORY I/F
REV 1.1
PART 2 OF 4

BOM=CORE
A08347-005

IC

M_DATA<63..0>   BI   15D7<> 16D7<>

M_CKE<5..0>   OUT   15A8< 16A7<

I_SRCOMP

CAD NOTE:
ROUTE 10 MIL TRACE TO R4E1.
PLACE AS CLOSE AS POSSIBLE
TO BGA. MAX OF 500 MILS.

1 R4E1 2   V_3P3_STR   IN
40.2   1%
603   CH

62C4<
46C2> 14B1< 15B5< 15C8<
16B7< 46B2< 48D4< 61B8<

M_MAC<7..4>*   16C7< OUT

RP4E2 BOM=CORE
7 4
10   5% 063W
6 SM 5 IC   RP4E2 BOM=CORE
   3 6
RP4E2 BOM=CORE   10   5% 063W
2 1 SM   IC
10   5% 063W   RP4E2 BOM=CORE
4 SM 5 IC   1 8
   10   5% 063W

M_MACR7*
M_MACR6*
M_MACR5*
M_MACR4*

M_MAB<7..4>*   15D8< OUT

RP5E1 BOM=CORE
7 4
10   5% 063W
6 SM 5 IC   RP5E1 BOM=CORE
   3 6
RP5E1 BOM=CORE   10   5% 063W
5 1 SM   IC
10   5% 063W   RP5E1 BOM=CORE
4 SM 5 IC   1 8
   10   5% 063W

M_MABR7*
M_MABR6*
M_MABR5*
M_MABR4*

M_WE*   OUT   15D5< 15D7< 16D7<

BOM=CORE
1 R5F1 2   H_BSEL0   BI   6D5> 4B1< 8C8<
10K   5%
603   CH

BOM=CORE
1 R5F2 2   H_BSEL1   BI   6D5> 4C1< 8B8<
10K   5%
603   CH

BOM=CORE
1 R5E6 2
10K   5%
603   CH

M_BS<1..0>   16C7< 15D8< 15D5<   OUT

M_MAA<12..8>   15D8< 15C5< 9A3< 16C7<   OUT

M_MAA<7..4>   15C8< OUT

RP4E1 BOM=CORE
7
10   5% 063W
6 SM   RP4E1 BOM=CORE
10   5% 063W
RP4E1 BOM=CORE SM   IC
5
10   5% 063W   RP4E1 BOM=CORE
4 SM   IC
10   5% 063W
SM   IC

M_MAA7R*
M_MAA6R*
M_MAA5R*
M_MAA4R*

M_SCAS*   OUT   15D5< 15D7< 16D7<
M_SRAS*   OUT   15D5< 15D7< 16D7<
M_CSB<5..0>*   OUT   15A8< 16B7<
M_CSA<5..0>*   OUT   15A8< 16B7<

M_MAA<3..0>   16C7< 15A8<   OUT

M_DQM<7..0>   16C7< 15A8<   OUT

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CAD NOTE:
MIN LENGTH = 2.0"
MAX LENGTH = 4.0"

U4E1

H_D<63..0>* BI 6D8<>

VTT IN 61D7<
43C1< 6D1< 7A8< 7B2< 7C4< 8A4<
8B7< 9C5< 9D8< 43B8< 45D8<

R3
50
5%
CH
603

PLACE CLOSE
TO GMCH

BOM=CORE
A08347-005

82815
CPU I/F
REV 1.1
PART 3 OF 4

H_CPURST* OUT 8B3<
7B4<
6D5<

7A8> 6D2> BI H_ADS*   G1 ADS
6C> BI H_BNR*   N4 BNR
6C> BI H_DBSY*   J3 DBSY
6C> BI H_DRDY*   J1 DRDY
6D> BI H_HIT*   K1 HIT
6D> BI H_HITM*   L3 HITM
6C> OUT H_LOCK*   L4 MLOCK
6D> BI H_TRDY*   K3 HTRDY
                          H1 RS2
                          L1 RS1
                          K2 RS0
6C> BI H_RS<2..0>*

CPURST AA5
BPRI   M5
DEFER   M3

H_BPRI* OUT 6C5<
H_DEFER* OUT 6D2<
H_REQ<4..0>* BI 6C5<>

HREQ4 N3 4
HREQ3 L5 3
HREQ2 M2 2
HREQ1 N1 1
HREQ0 M1 0

GTLREF0 U5
GTLREF1 AA10

V_GMCH_GTLREF IN 7B5> 9B7<

HUB I/F

IC

TP_GMCH_G10
6D> BI H_A<31..3>*

32C6< 22B5> IN P_RST*

4A> PIN CK_H_1XXM_GMCH

4A> PIN CK_HL_66M_GMCH
20C> BI HL_PSTRB*
20C> BI HL_PSTRB
20C> BI HL<10..0>

V_1P85 IN 22C3< 22D7< 61A4<
44C1< 11D1< 14A7<
14B8< 19C8< 20C1<
62D4<

BOM=CORE
R5E4
40.2
1%
CH
603

BOM=CORE
R5E4
150
1%
CH
603

I_HUB_RCOMP

V_0P9_HUBREF OUT 20B4<>

BOM=CORE
R5E6
150
1%
CH
603

BOM=CORE
C5E8
20pF
95V
603

BOM=CORE
C7L3
20pF
95V
603

BOM=CORE
C5E1
20pF
95V
603

BOM=CORE
C5E10
4.7pF
50V
EMPTY
603

CAD NOTE:
PLACE C5E10 NEAR PIN AA7.
PLACE C5E9 NEAR PIN F22.

BOM=CORE
C5E9
20pF
50V
EMPTY
603

8 7 6 5 4 3 2 1

U4E1 A28347-005

BOM=CORE

82815
POWER/GND
REV 1.1
PART 4 OF 4

IC

THESE CAPS SHOULD BE
40 MILS FROM PACKAGE
AND PERPENDICULAR TO
BGA EDGE

V_1P85

BOM=VGA
L5D1
22UH IND
R5D12
0   1A
1210 EMPTY
BOM=815EP   DFP

I_GMCH_VCCDA_AF25

V_1P85

V_3P3_STR   IN

* SECONDARY SIDE CAPS

BOM=VGA
L5C1
4.7UH IND
721891-008
R5C32
0   1A
805 EMPTY
BOM=815EP   DFP

I_GMCH_VCCDA_C

* SECONDARY SIDE CAPS

V_1P85

V_AGP_VDDQ   IN

V_1P85

NOTE : STUFF 0 OHM RESISTORS TO BYPASS THE INDUCTORS FOR GRAPHICLESS SKUS

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DIMM 0   DIMM 1

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DIMM 2

15D7<> 12D1< **BI** M_DATA<63..0>

VCC=V_3P3_STR

732426-001 J6G1
BOM=CORE

CONN
DIMM 168P SYNC

15D7< 15D5< 12B1> **IN**	M_WE*	27 WE0*
15D7< 15D5< 12A1> **IN**	M_SRAS*	115 RAS*/DU
15D7< 15D5< 12A1> **IN**	M_SCAS*	111 CAS*/DU

132	A13/DU
12 126	A12/DU
11 123	A11/A13
39	BA1/A12
1 122	BA0/A11
0 38	A10
10 121	A9
9 37	A8
8 120	A7
7 36	A6
6 119	A5
5 35	A4
4 118	A3
3 34	A2
2 117	A1
1 33	A0
0	

15D8< 15D5< 12A8> **IN** M_BS<1..0>
12C8 **IN** M_MAC<7..4>*

15D8< 15C5< 12A8> 9A3> **IN** M_MAA<12..8>

15A8< 12A8> **IN** M_MAA<3..0>

7 131	DQMB7/CAS7*
6 130	DQMB6/CAS6*
5 113	DQMB5/CAS5*
4 112	DQMB4/CAS4*
3 47	DQMB3/CAS3*
2 46	DQMB2/CAS2*
1 29	DQMB1/CAS1*
0 28	DQMB0/CAS0*

15A8< 12A8> **IN** M_DQM<7..0>

15A8< 12A1> **IN** M_CSB<5..0>*
15A8< 12A1> **IN** M_CSA<5..0>*

5 129	CS3*/RAS3*
4 45	CS2*/RAS2*
5 114	CS1*/RAS1*
4 30	CS0*/RAS0*

5C **IN** CK_M_1XXM_DIMM1C
5C **IN** CK_M_1XXM_DIMM0C

125	CLK1/DU
42	CLK0/DU

4 128 CKE0/DU

56B7< 15B8< 15B4< 57B7<> 21C6< 3D7<>
3C7< 57B2<> 56B7<> 21C6<> 15B8<> 15B4<>

IN ICH_SMB_CLK
BI ICH_SMB_DATA

83	SCL
82	SDA
167	SA2
166	SA1
165	SA0

62C4<
15B5< 14B1< 12B2< 46C2>
61B8< 48D4< 46B2< 15C8<

IN V_3P3_STR

TP_DIMM2_146 146 VREF1
TP_DIMM2_62 62 VREF0

5C **IN** CK_M_1XXM_DIMM3C

TP_DIMM2_164 164	RFU
163	CLK3/DU
147	RFU
TP_DIMM2_145 145	RFU
TP_DIMM2_137 137	CB7
TP_DIMM2_136 136	CB6
TP_DIMM2_135 135	RFU
TP_DIMM2_134 134	RFU
TP_DIMM2_109 109	RFU
TP_DIMM2_108 108	RFU
TP_DIMM2_106 106	CB5
TP_DIMM2_105 105	CB4

15A8< 15A4< 15C7> **IN** CORE_SPD_WE*
5C **IN** CK_M_1XXM_DIMM2C

81	RFU
TP_DIMM2_80 80	RFU
79	CLK2/DU
63	CKE1/DU
TP_DIMM2_61 61	RFU
TP_DIMM2_53 53	CB3
TP_DIMM2_52 52	CB2
TP_DIMM2_51 51	RFU
TP_DIMM2_50 50	RFU
TP_DIMM2_25 25	RFU
TP_DIMM2_24 24	RFU
TP_DIMM2_22 22	CB1
TP_DIMM2_21 21	CB0

DQ63	161	63
DQ62	160	62
DQ61	159	61
DQ60	158	60
DQ59	156	59
DQ58	155	58
DQ57	154	57
DQ56	153	56
DQ55	151	55
DQ54	150	54
DQ53	149	53
DQ52	144	52
DQ51	142	51
DQ50	141	50
DQ49	140	49
DQ48	139	48
DQ47	104	47
DQ46	103	46
DQ45	101	45
DQ44	100	44
DQ43	99	43
DQ42	98	42
DQ41	97	41
DQ40	95	40
DQ39	94	39
DQ38	93	38
DQ37	92	37
DQ36	91	36
DQ35	89	35
DQ34	88	34
DQ33	87	33
DQ32	86	32
DQ31	77	31
DQ30	76	30
DQ29	75	29
DQ28	74	28
DQ27	72	27
DQ26	71	26
DQ25	70	25
DQ24	69	24
DQ23	67	23
DQ22	66	22
DQ21	65	21
DQ20	60	20
DQ19	58	19
DQ18	57	18
DQ17	56	17
DQ16	55	16
DQ15	20	15
DQ14	19	14
DQ13	17	13
DQ12	16	12
DQ11	15	11
DQ10	14	10
DQ9	13	9
DQ8	11	8
DQ7	10	7
DQ6	9	6
DQ5	8	5
DQ4	7	4
DQ3	5	3
DQ2	4	2
DQ1	3	1
DQ0	2	0

WE2*	48	TP_DIMM2_48
OE2*	44	TP_DIMM2_44
OE0*	31	TP_DIMM2_31

15A8< 12C1> **IN** M_CKE<5..0>

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8   7   6   5   4   3   2   1

18C6< 18B7< 17CB< 17BB< 17A4< 14A1< 44A1>

IN V_AGP_VDDQ

BOM=CORE_AGP
RP7E1 6.80K 5% .063W IC SM
BOM=CORE_AGP RP7E1 6.80K 5% .063W IC SM
BOM=CORE_AGP R6C12 6.8K 5% CH 603
BOM=CORE_AGP R7E3 6.8K 5% CH 603
BOM=CORE_AGP R6E2 6.8K 5% CH 603
BOM=CORE_AGP R7E1 6.8K 5% CH 603
BOM=CORE_AGP R6C11 6.8K 5% CH 603

BOM=CORE_AGP R6D1 6.80K 5% CH 603
BOM=CORE_AGP R6C13 6.8K 5% CH 603
BOM=CORE_AGP RP7E1 6.80K 5% .063W IC SM
BOM=CORE_AGP RP7E1 6.80K 5% .063W IC SM
BOM=CORE_AGP RP7C1 6.80K 5% .063W IC SM

G_AD<31..0>
11D7 B1

PU.G_SERR_R*
PU_G_PERR_R*

BOM=CORE_AGP
656617-132
J6C1
UCONNAGP

Pin	Signal		Pin	Signal
31 B26	GAD31		B50	GSERR
30 B27	GAD30		B48	GPERR
29 B27	GAD29		A41	GIRDY
28 A27	GAD28		A46	GTRDY
27 A29	GAD27		A41	GFRAME
26 A29	GAD26		A47	GSTOP
25 B30	GAD25		A50	GPAR
24 A30	GAD24		B46	GDEVSEL
23 B33	GAD23			
22 A35	GAD22		A14	WBF
21 B35	GAD21		B12	RBF
20 A36	GAD20			
19 B36	GAD19		A12	PIPE
18 A38	GAD18		B8	GREQ
17 B38	GAD17		A8	GGNT
16 A39	GAD16		B7	AGPCLK
15 A51	GAD15		A7	PCIRST
14 B53	GAD14		A5	INTA
13 A53	GAD13		B6	INTB
12 B54	GAD12		A48	PME
11 A54	GAD11		B1	OVRCNT
10 B56	GAD10		A2	TYPEDET
9 A56	GAD9		B4	USB+
8 B57	GAD8		A4	USB-
7 A60	GAD7		A66	VREFG_C
6 B60	GAD6		B66	VREFC_G
5 A62	GAD5		B42	3.3V_AUX2
4 B62	GAD4		B24	3.3V_AUX1
3 B63	GAD3		A1	12V
2 A63	GAD2		B64	VDDQ
1 B65	GAD1		A64	VDDQ
0 A65	GAD0		B58	VDDQ
			A58	VDDQ
3 A33	GC_BE3		B52	VDDQ
2 B39	GC_BE2		B47	VDDQ
1 B51	GC_BE1		A40	VDDQ
0 A57	GC_BE0		B40	VDDQ
	B11	ST2	A34	VDDQ
	A10	ST1	B34	VDDQ
	B10	ST0		

G_IRDY* 11A2<>
G_TRDY* 11B2<>
G_FRAME* 11A2<>
G_STOP* 11B2<>
G_PAR 11A2<>
G_DEVSEL* 11B2<>

G_WBF* OUT 11B2<>
G_RBF* OUT 11B2<>

G_PIPE* OUT 11B2<>
G_REQ* OUT 11B2<>
G_GNT* IN 11A2>

CK_G_66M_AGP IN 4B5>
P_RST_SLOTS B1   40C6< 19A6< 27C7< 28C7<
P_INTA* B1   20B4> 30DB>
P_INTB* B1   20B4> 27C2> 28C7> 29C2> 30DB>
P_PME* B1   20BB<> 27C7> 28C7> 29C7>
TP_OVRCNT_B1
G_TYPEDET* OUT   18A6< 44BB<
PD_USB_AGP_P0
PD_USB_AGP_P0*
VREF_AGP_MC OUT 11A2> 18A4>
V_0P75_AGPREF4 IN 18B7>
V_3P3_PCIAUX IN
+12V
V_AGP_VDDQ IN

REF1 100K 5% EMPTY 603
BOM=CORE_AGP

BOM=CORE_AGP R6C9 15K 5% EMPTY 603
BOM=CORE_AGP R6C7 15K 5% EMPTY 603
4BC1> 27DB< 28DB> 29D7>
S7C2> 62BB<

44A1> 14A1< 17BB< 17CB< 17D6< 18B7< 18C6<

V_AGP_VDDQ IN
18C6<
17D6<
17A4<
44A1<
14A1<
17BB<
18B7<

BOM=CORE_AGP RP7C1 6.80K 5% .063W IC SM
BOM=CORE_AGP RP7C1 6.80K 5% .063W IC SM

G_CBE<3..0>* 11B2 B1

G_ST<2..0> 11A? IN
G_SBA<7..0> 11A? OUT

	Pin	Signal
7	A21	SBA7
6	B21	SBA6
5	B20	SBA5
4	B20	SBA4
3	A17	SBA3
2	B17	SBA2
1	A15	SBA1
0	B15	SBA0

18B7< 17D6< IN V_AGP_VDDQ
14A1< 44A1<
17CB< 17A4<
18C6<

BOM=CORE_AGP R6D5 6.8K 5% CH 603
BOM=CORE_AGP R6D7 6.8K 5% CH 603
BOM=CORE_AGP R6E3 6.8K 5% CH 603

G_AD_STB0   B59 GAD_STB0
G_AD_STB0*   A59 GAD_STB0
G_AD_STB1   B32 GAD_STB1
G_AD_STB1*   A32 GAD_STB1
G_SBSTB   B18 SB_STB
G_SBSTB*   A18 SB_STB

BOM=CORE_AGP R6D3 6.8K 5% CH 603
BOM=CORE_AGP R6D8 6.8K 5% CH 603
BOM=CORE_AGP R6E5 6.8K 5% CH 603

NOTE: VCC=B2,B3 CONN

GND=A5,B5,A13,B13,A19,B19,A23,A31,B31,A37,B37,A43,B43,A49,B49,A55,B55,A61,B61
NC=A3,A11,B14,A22,A24,A42,A44,B44
VCC=B2;B3

CAD PLACEMENT NOTE:
ENSURE STUB LENGTH
RES. IS MAX=100MI

CAD PLACEMENT NOTE:
PLACE RESISTORS NEAR AGP CONN

AGP

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+12V   VCC

VCC3

1 BOM=CORE_AGP
C9GB
470PF
2 10%
50V
603

1 BOM=CORE_AGP
C2A12
470PF
2 10%
50V
603

1 BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP
C4H3 C7D3 C7G5 C7H4
1UF   1UF   1UF   1UF
2 20% 20% 20% 20%
25V   25V   25V   25V
603   603   603   603

HMB HAS 2 X 4.7UF

18B7< 17D6< 17C8< 17BB< 17A4< 14A1< 44A1>   IN V_AGP_VDDQ

1 BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP BOM=CORE_AGP
C7D6 C6E6 C6E6 C6D2 C6D4 C6D2 C7E2 C7E4 C6E2 C7DJ
1UF   1UF   1UF   1UF   1UF   1UF   1UF   1UF   1UF   4.7UF
2 20% 20% 20% 20% 20% 20% 20% 20% 20% 10%
25V   25V   25V   25V   25V   25V   25V   25V   25V X5R
603   603   603   603   603   603   603   603   603 1206

CAD NOTE:
PLACE NEAR AGPCONN

17B< OUT V_0P75_AGPREF4X

PROVIDES AGP REF FOR
A 4X CARD

17D6< 17C8< 17BB< 17A4< 14A1< 44A1>   IN V_AGP_VDDQ
18C6<

1 BOM=CORE_AGP
R5E3 2
1K 1%
603 CH

1 BOM=CORE_AGP
C5F11
1UF
2 10%
16V
X7R
603

1 BOM=CORE_AGP
R5E2 2
1K 1%
603 CH

1 BOM=CORE_AGP
C5F11
1UF
2 10%
16V
X7R
603

2 BOM=CORE_AGP
R6F2 1
150 1%
603 CH

2 BOM=CORE_AGP
R6F1 1
100 1%
603 CH

DESIGN NOTE:
STATIC DRAIN-SOURCE ON-RESISTANCE
( )VGS=10V, ID=200MA) 5.0 OHM

- 2X AGP VREF FOR GMCH
- FOR 4X, AGP VREF SUPPLIED
  BY THE AGP CARD

I_VDO_4OF10_VDDQ   2 VREF_AGP_MCH OUT 11A2> 17B4>

Q5F1
FET
201924-001
1 BOM=CORE_AGP

1 BOM=CORE_AGP
C6F10
1UF
2 10%
16V
X7R
603

SPEC. NOTE:
$V_{GS} = +/-20$

CAD NOTE:
PLACE 0.1UF (VREF) CAP TO GROUND
AS CLOSE AS POSSIBLE TO GMCH.
PLACE RESISTOR DIVIDER CIRCUIT
AS CLOSE AS POSSIBLE TO GMCH.

44B8< 17B2>   IN G_TYPEDET*

DESIGN NOTE:
WHEN TYPEDET IS GND, MODE IS 4X
WHEN TYPEDET IS FLOATING, MODE IS 2X

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VGA & DVI CONNECTOR

NOTE: FILTER TARGETED FOR -3DB @ 105MHZ

NO STUBS ON CAPS, DIODES ON ESD EMI TRACES

CAPS MUST BE NEXT TO DIODES

CAD NOTE : PLACE THESE RESISTORS CLOSE TO VGA CONN

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NOTE : ICH2X #A51241-001

CK_APIC_33M_ICH2
H_STPCLK*

BOM=CORE_ICH2
A51241-001
U7F1
ICH2_360

BOM=CORE_ICH2
A51241-001
U7F1
ICH2_360
PART 3 OF 3

P_AD<31..0>

PCI

HUB

IRQ

PCI

LAN

GPIO

VCC

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NOTE : STUFF FOR LAN
SKU ONLY.
UNSTUFF FOR CNR
AND EVAL SKUS.

V_3P3_STBY
V_3P3_STBY
H_SMI_SIO*
CDC_DWN_ENAB*

PART 1 OF 3

NOTE
VCCPU1/2 VOLTAGE IS:
FOR SLOT1= V_2P5_CMOS
FOR FC-PGA= VCC_CORE

NOTE : ICH2X #A51241-001

PLACE NEAR
PIN U21

NOTE:-
STUFF FOR FV
FAB F ONWARDS
NO SITE ON FV
FAB A - FAB E

ROUTE ON TOP WITH
GND FILL UNDER PARTS

V_3P0_BAT_VREG
V_BAT_VREG_R_CH
0.01UF ON HMB

J9H4
1X2HDR
HDR
107555-102

V_3P0_BAT_VREG
V_1P5_CMOS
V5REF_SUS
V_REF5V

SM XTAL
32.768KHZ

SPARE

U7F1
SYSTEM

GPIO_GRN_BLNK   W15   GPIO25
I_GPIO_FVT_SELV21   GPIO24
CPU_THRM_ALERT A13   THRM
SLP_S3*   W16   SLP_S3
SLP_S5*   AB18   SLP_S5
PWRGD_3V   R20   PWROK
GPIO_LAN_ENABLE16   RSM_PWROK
SW_ON*   W21   PWRBTN
WOL*   AA17   RI
RSMRST*   R21   RSMRST
TP_SUS_STAT*   Y17   SUSSTAT
SUSCLK   AA18   SUSCLK
ICH_SMB_DATA   AA16   SMBDATA
ICH_SMB_CLK   AB16   SMBCLK
PU_SMB_ALERT*   AB17   GPI11/SMBALERT
GPIO_DMA66_DETECTGPRI   GPI6
P_INTH*   M4   GPI5/PIRQH*
   T19   INTRUDER*
PU_INTRUDER*

PU_ICH2_RTCRST
I_VBIAS   T20   RTCRST
I_ICH2_RTCX1   T21   VBIAS
I_ICH2_RTCX2   U22   RTCX1
   T22   RTCX2

CK_HL_66M_ICH2   D4   CLK66
CK_14M_ICH2   M19   CLK14
CK_USB_48M_ICH2   P20   CLK48

AC97
AUD_LINK_RST*   V22   AC_RST
I_AUD_LINK_SYNC_ICH_R   P19   AC_SYNC
   R19   AC_BIT_CLK
   P21   AC_SDOUT
   Y22   AC_SDIN0
   W22   AC_SDIN1
   N22   SPKR

LPC
L_AD<3..0>   Y12   LAD0/FWH0
   W12   LAD1/FWH1
   AB13   LAD2/FWH2
   AB12   LAD3/FWH3
L_DRQ*   Y13   LDRQ0
   W13   LDRQ1
L_FRAME*   AB11   LFRAME*/FWH4
   AA12   FS_0
AUD_LINK_SDO_ICH_R

USB
ICH_USB_P0   W17   USBP0_P
ICH_USB_P0*   Y18   USBP0_N
ICH_USB_P1   AB19   USBP1_P
ICH_USB_P1*   AA19   USBP1_N
ICH_USB_P2   W18   USBP2_P
ICH_USB_P2*   Y19   USBP2_N
ICH_USB_P3   AB20   USBP3_P
ICH_USB_P3*   AA20   USBP3_N

ICH_U_OC1_2   W19   OC0
   Y20   OC1
   Y21   OC2
   W20   OC3

ICH2_EE_CS   K4   EE_CS
ICH2_EE_DINK3   EE_DIN
ICH2_EE_DOUT4   EE_DOUT
ICH2_EE_CLKJ3   EE_SHCLK

ICH2_360
PART 2 OF 3
IC

IDE
ICH_IDE_PDCS1   E21   PDCS1
ICH_IDE_SDCS1   C15   SDCS1
ICH_IDE_PDCS3   E19   PDCS3
ICH_IDE_SDCS3   D15   SDCS3

ICH_IDE_PDA<2..0>   F20   PDA0
   F19   PDA1
   E22   PDA2
   A16   SDA0
   D16   SDA1
ICH_IDE_SDA<2..0>   C17   SDA2

ICH_IDE_PDDREQ   G22   PDDREQ
ICH_IDE_SDDREQ   B18   SDDREQ
ICH_IDE_PDDACK   F22   PDDACK
ICH_IDE_SDDACK   B17   SDDACK
ICH_IDE_PDIOR   G19   PDIOR
ICH_IDE_SDIOR   D17   SDIOR
ICH_IDE_PDIOW   G21   PDIOW
ICH_IDE_SDIOW   D14   SDIOW
ICH_IDE_PIORDY   G20   PIORDY
ICH_IDE_SIORDY   A17   SIORDY

PDD0   H19   0
PDD1   H22   1
PDD2   J19   2
PDD3   J22   3
PDD4   K21   4
PDD5   K20   5
PDD6   M21   6
PDD7   M22   7
PDD8   L22   8
PDD9   L21   9
PDD10   K22   10
PDD11   K20   11
PDD12   J21   12
PDD13   J20   13
PDD14   H21   14
PDD15   H20   15
ICH_IDE_PDD<15..0>

SDD0   D18   0
SDD1   B19   1
SDD2   D19   2
SDD3   C20   3
SDD4   C20   4
SDD5   C21   5
SDD6   D22   6
SDD7   D21   7
SDD8   D21   8
SDD9   C22   9
SDD10   D22   10
SDD11   B20   11
SDD12   C19   12
SDD13   A19   13
SDD14   C18   14
SDD15   A18   15
ICH_IDE_SDD<15..0>

SMLINK0   U19   ICH_SMIB_CLK
SMLINK1   V20   ICH_SMIB_DATA
VRMPWRGD   B15   PU_PWRGD_ICH2
TP_0   U20   PU_ICH2_U20

VCC3
V_3P3_STBY

ALL USB PAIRS MUST BE ROUTED AS DIFFERENTIAL PAIRS
7.5 / 7.5 / 7.5, AND 10 TO 12 MILS TO ALL OTHERS

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V_1P85 ──[IN]   44C1> 11D1< 13B1< 14A7< 14B8<   VCC3
                 19C8< 20C1< 22C3< 61A4< 62D4<

1 BOM=CORE_ICH2
   R7F2
   40.2
   1%   1 BOM=CORE_ICH2
   CH   R8F2
2 603   10K
                                                  5%
   HLZCOMP ──[OUT] 20C4<   2 CH
                                                  603

                                                  CPU_THRM_ALERT* ──[OUT] 21C6<

BOM=CORE_ICH2
1 R8F9 2 V_3P3_STBY ──[IN]   56D8< 59B1< 59B2< 59B7< 59C8< 61B2< 61D4< 62C2<
   10K   CH   39D4< 39C8< 39D3< 40A7< 40B2< 40C2< 40D2<
   603   49B3< 8B4< 20A8< 20B1< 20B8< 20C1< 21A1<
                                 22C3< 27D8< 28D8< 32A1< 32A7< 32D8< 38B3<
                                 41D6< 43A8< 46C7< 47A4< 47D7< 48B7< 48C7<

   PU_SMB_ALERT* ──[OUT] 21C6<

                           I_P_PCIRST_P35*   BOM=CORE_PCI
                                             1 R9G1 02   P_RST_GLUE_FWH* ──[OUT]   31C6< 40B6<
                                                33 5%
                                                603 CH

20B7>[IN] P_PCIRST* 1 R9G9 2   1 R9H1 2   P_RST* ──[OUT]   13B8< 32C6<
                        0   1A   33 5%
                        603 CH   603 CH

           CAD NOTE: 1 BOM=CORE_PCI
           PLACE R9G9 & C9H1   C9H1
           AS CLOSE AS POSSIBLE   100PF
           TO ICH2 (SOURCE)   50V
                                      2 X7R
                                         603

VCC3
           BOM=CORE_ICH2
           RP8B2
        3   1   PU_P_INTE* ──[OUT] 20A7<
        8.2K   5% 063W
        BOM=CORE_ICH2 SM   IC
        RP8B2
        5   4   P_INTF* ──[OUT]   27C7> 28C2> 29C7> 20A7<
        8.2K   5% 063W
        BOM=CORE_ICH2 SM   IC
        RP8B2
        8   1   P_INTG* ──[OUT]   27C2> 28C7> 29C2> 20A7<
        8.2K   5% 063W
        BOM=CORE_ICH2 SM   IC
        RP8B2
        7   5   P_INTH* ──[OUT]   27C7> 28C2> 29C7> 21C6<
        8.2K   5% 063W
                 SM   IC

───

20C1< 49D3> [IN] V_1P8_STBY BOM=CORE_ICH2
                               C8F2
                            1   2
                               .1UF 10%
                               16V
                               X7R
                               603

21D2< 8D8< 8D2< 7D8< 7B8< 8A5<   [IN] V_1P5_CMOS BOM=CORE_ICH2
                       40A8<   C7F2
                                                 1   2
                                                    .1UF 10%
                                                    16V
                                                    X7R
                                                    603

27D8< 22C7< 62C2< 61D4< 61B2< 59C8< 59B7< 59B2< [IN] V_3P3_STBY BOM=CORE_ICH2
             43A8< 41D6< 40D2< 40C2< 40B2< 40A7< 39D3<   C7F2
             21A1< 20C1< 20B8< 20B1< 20A8< 8B4< 49B3<   1   2
             39C8< 39D4< 38B3< 32D8< 32A7< 32A1< 28D8<   .1UF 10%
             59B1< 56D8< 48C7< 48B7< 47D7< 47A4< 46C7<   16V
                                                                 X7R
                                                                 603
                                                              BOM=CORE_ICH2
                                                              C8C7
                                                           1   2
                                                              .1UF 20%
                                                              25V
                                                              603

20C1< 19C8< 14B8< 14A7< 13B1< 11D1< 44C1< [IN] V_1P85   BOM=CORE_ICH2
                  62D4< 61A4< 22D7<   C7F5
                                                      1   2
                                                         .1UF 10%
                                                         16V
                                                         X7R
                                                         603
                                                      BOM=CORE_ICH2
                                                         C7F8
                                                      1   2
                                                         .1UF 10%
                                                         16V
                                                         603
                                                      BOM=CORE_ICH2
                                                         C8E9
                                                      1   2
                                                         .1UF 10%
                                                         16V
                                                         603

VCC3   VCC3

      BOM=CORE_ICH2   BOM=CORE_ICH2
      C8F3   1   C8E6   2
   1   2   .1UF 20%
      .1UF 20%   25V
      25V   603
      603
      BOM=CORE_ICH2   BOM=CORE_ICH2
      C7C2   1   C9C8   2
   1   2   .1UF 20%
      .1UF 20%   25V
      25V   603
      603
      BOM=CORE_ICH2   BOM=CORE_ICH2
      C8F1   1   C9D2   2
   1   2   .1UF 20%
      .1UF 20%   25V
      25V   603
      603

PLACE AS CLOSE AS POSSIBLE TO ICH2 (< 50 MILS)

ICH PULLUPS & DECOUPLING

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8   7   6   5   4   3   2   1

SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS

21A BI ICH_IDE_SDD<15..0>
21B BI ICH_IDE_PDD<15..0>

DESIGN NOTE: HOST SIDE DETECTION

VCC3

40A PIN IDE_RST*

BOM=CORE_IDE
1 R6H1 2
33 5%
603 CH
I_IDE_PRI_RST*

BOM=CORE_IDE
J6H1 732441-001
2X20HDR_20

PRIMARY IDE
CONNECTOR
(BLACK)

BOM=CORE_IDE
1 R7G3 2
4.7K 5%
603 CH

21C OUT ICH_IDE_PDDREQ
21B PIN ICH_IDE_PDIOW*
21C PIN ICH_IDE_PDIOR*
21B OUT ICH_IDE_PIORDY
21C PIN ICH_IDE_PDDACK*

BOM=CORE_IDE
1 R7G1 2
8.2K 5%
603 CH

20A OUT ICH_IDE_IRQ14
21C PIN ICH_IDE_PDA<1>
21C PIN ICH_IDE_PDA<0>
21C PIN ICH_IDE_PDCS1*
21C PIN ICH_IDE_PDCS3*
21C PIN ICH_IDE_PDA<2>

HDR

TP_701I

GPIO_DMA66_DETECT_PRI OUT 21C6<

BOM=CORE_IDE
1 R4G1 2
15K 5%
603 CH

IDE_PRI_ACT* OUT 40B6<

BOM=CORE_IDE
1 R6G1 2
33 5%
603 CH
I_IDE_SEC_RST*

BOM=CORE_IDE
J6G2 A22253-001
2X20HDR_20

SECONDARY IDE
CONNECTOR
(WHITE)

BOM=CORE_IDE
1 R5G1 2
4.7K 5%
603 CH

21C OUT ICH_IDE_SDDREQ
21B PIN ICH_IDE_SDIOW*
21C PIN ICH_IDE_SDIOR*
21B OUT ICH_IDE_SIORDY
21C PIN ICH_IDE_SDDACK*

BOM=CORE_IDE
1 R5G2 2
8.2K 5%
603 CH

20B OUT ICH_IDE_IRQ15
21C PIN ICH_IDE_SDA<1>
21C PIN ICH_IDE_SDA<0>

TP_702I

GPIO_DMA66_DETECT_SEC OUT 20A7<

BOM=CORE_IDE
1 R5G3 2
15K 5%
603 CH

21C PIN ICH_IDE_SDCS1*
21C PIN ICH_IDE_SDCS3*
21C PIN ICH_IDE_SDA<2>

HDR

IDE_SEC_ACT* OUT 40A6<

NOTE : PLACE CAPS NEXT TO MAGJACK

25D5< 47C2> [IN] V_5P0_USB

PLACE NEAR CONN

NOTE : USE A14537-002 FOR SKU WITH LAN
USED IN ECHO BAY

USE 749193-001 FOR SKU WITHOUT LAN

ICH_USB_P0*

ICH_USB_P0

ICH_USB_P2*

ICH_USB_P2

I_USB_BP0_CR*

I_USB_BP0_CR

I_USB_BP1_CR*

I_USB_BP1_CR

USB_FP0_R* [OUT] 26CB<>

USB_FP0_R [OUT] 26CB<>

USB_FP2_R* [OUT] 26AB<>

USB_FP2_R [OUT] 26AB<>

ALL USB PAIRS MUST BE ROUTED AS DIFFERENTIAL PAIRS, 7.5 / 7.5, AND 10 TO 12 MILS TO ALL OTHERS

BACK PANEL PRIMARY USB / MAGJACK

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USB TRACE WIDTH = 7.5 MIL
ALL USB PAIRS MUST BE ROUTED AS DIFFERENTIAL PAIRS, 7.5 / 7.5, AND 10 TO 12 MILS TO ALL OTHERS
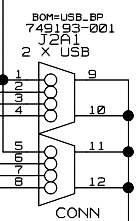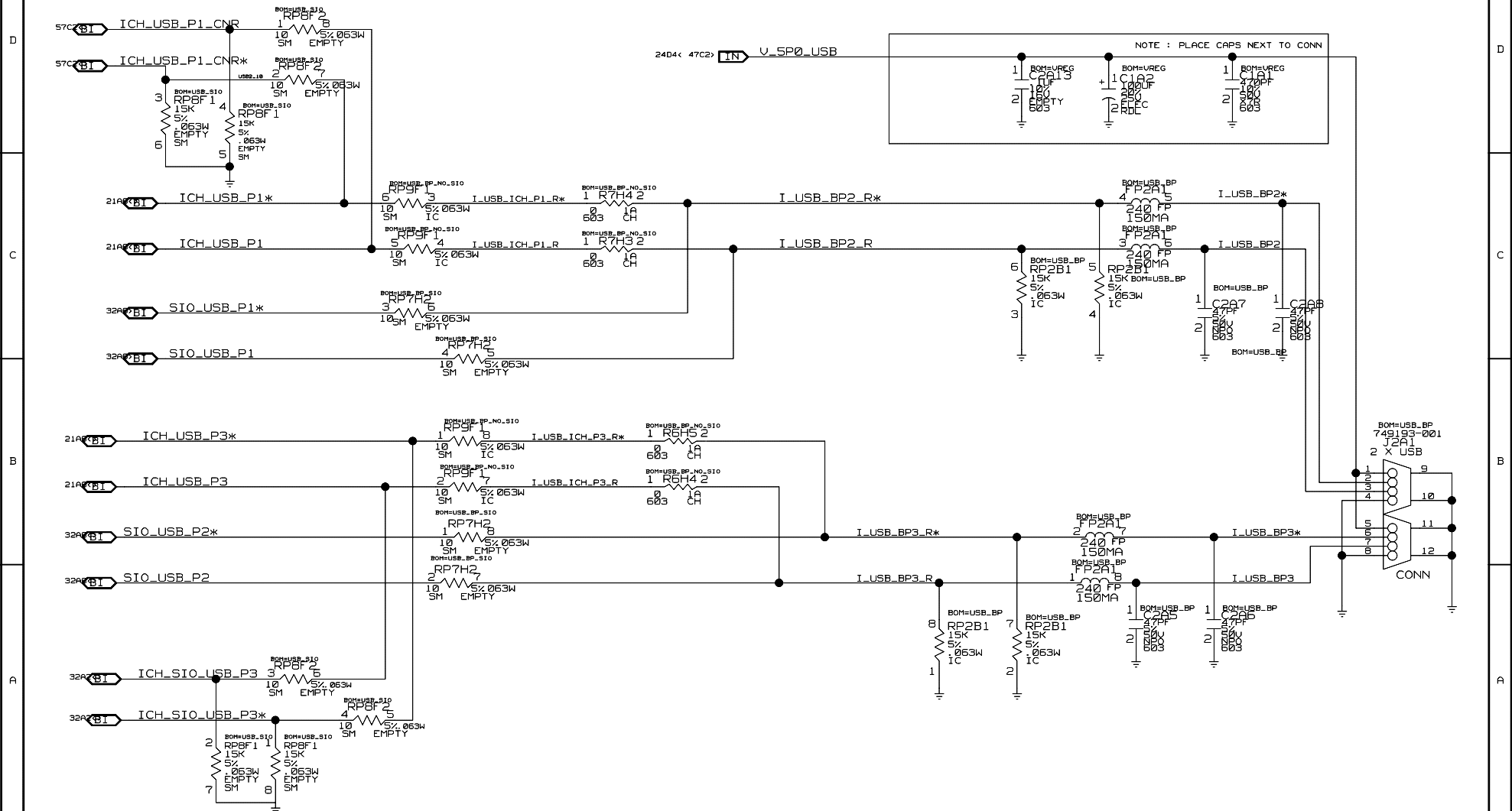
BACK PANEL SECONDARY USB

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XXXXXXXX	25	1.0

USB TRACE WIDTH = 7.5MIL

NOTE : SI4501DY #A03106-001
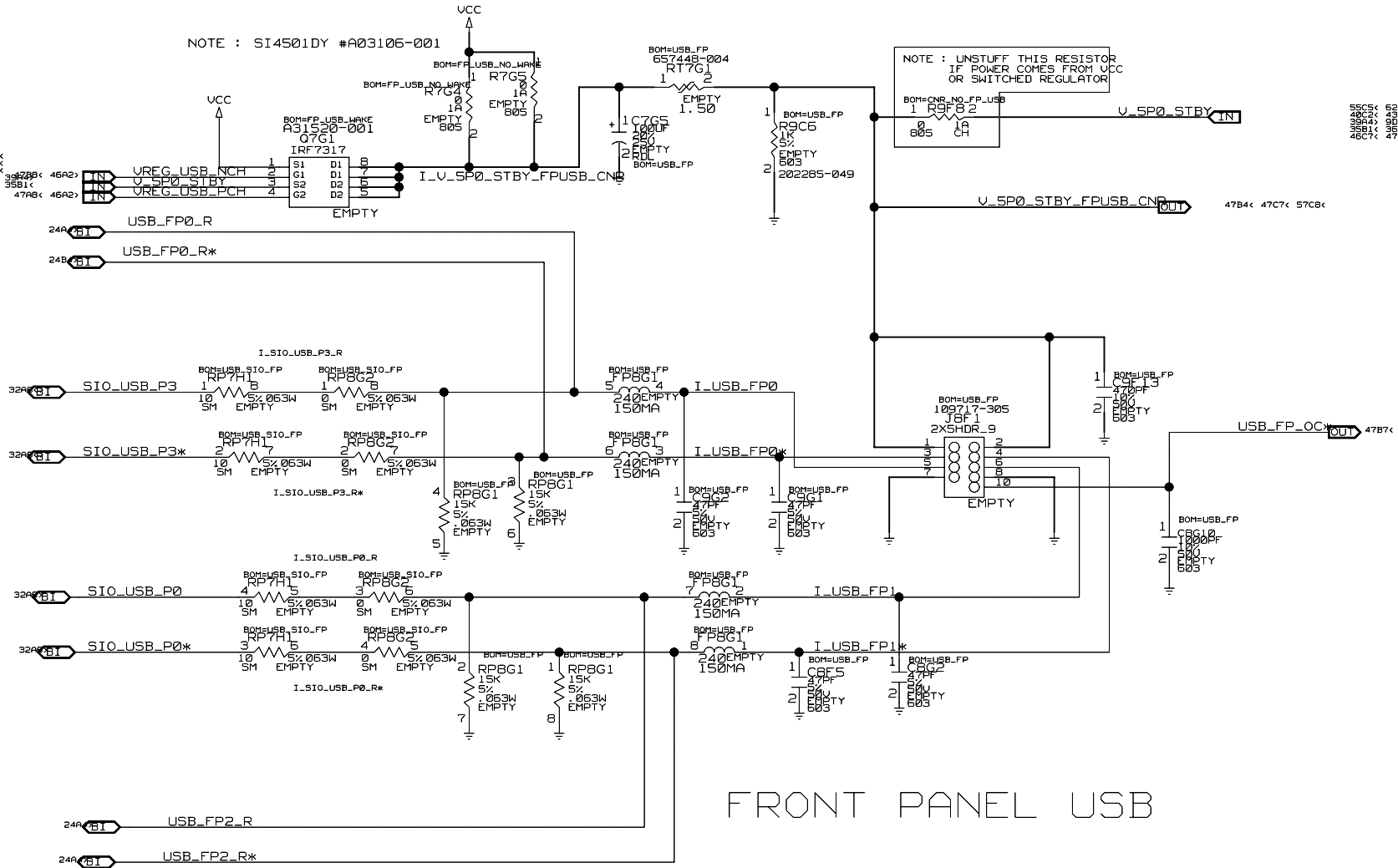
FRONT PANEL USB

ALL USB PAIRS MUST BE ROUTED AS DIFFERENTIAL PAIRS, 7.5 / 7.5, AND 10 TO 12 MILS TO ALL OTHERS

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PCI SLOT 1 (CLOSEST TO CPU)

NOTE : CONNECT V_3P3_STBY TO PIN A14 (3.3VAUX)
FOR WAKE FROM S5 SUPPORT IF V_3P3_PCIAUX
IS NOT SWITCHED

732431-002
BOM=CORE_PCI
J7B1
PCI CONN CONN

BOM=CORE_PCI
V_3P3_PCIAUX R7C22
0   1A
603   CH

BOM=CORE_PCI
V_3P3_STBY 1 R7C12   I_V_3P3_SLOT1
0   1A
603 EMPTY

NOTE : NO WAKE FROM S5 SUPPORT FOR PCI SLOT 1 BY DEFAULT

VCC3   VCC   +12V   -12V VCC   VCC3

P_INTF*
P_INTH*   P_INTG*
P_INTB*

TP_PCI1_A9
TP_PCI1_A11   TP_PCI1_B9
TP_PCI1_B10
TP_PCI1_B11

P_RST_SLOTS*   TP_PCI1_B14

P_GNT<0>*   CK_P_33M_S1

P_PME*   P_REQ<0>*

P_FRAME*   P_IRDY*
P_TRDY*   P_DEVSEL*
P_STOP*   P_PLOCK*
P_SDONE   P_PERR*
P_SBO*
P_PAR   P_SERR*

VCC   VCC

BOM=CORE_PCI   BOM=CORE_PCI
RP8E1   RP8E1
4   5   PU_P_REQ64A*   7   2
2.7K   5% 063W   2.7K   5% 063W
SM   IC   SM   IC

P_AD<31..0>
P_C/BE<3..0>*   P_ACK64*

NC=1,2

A1	TRST*	M12V_1	B1	
A2	P12V_1	TCK	B2	
A3	TMS	GND1	B3	
A4	TDI	TDO	B4	
A5	P5V_2	P5V_0	B5	
A6	INTA*	P5V_1	B6	
A7	INTC*	INTB*	B7	
A8	P5V_3	INTD*	B8	
A9	RSVD1	PRST1*	B9	
A10	P5V_4	RSVD2	B10	
A11	RSVD3	PRST2*	B11	
A12	GND10	GND2	B12	
A13	GND16	GND3	B13	
A14	3.3VAUX	RSVD5	B14	
A15	RST*	GND4	B15	
A16	P5V_6	CLK	B16	
A17	GNT*	GND7	B17	
A18	GND5	REQ*	B18	
A19	PME*	P5V_11	B19	
A20	AD30	AD31	B20	
A21	P3_3V	AD29	B21	
A22	AD28	GND8	B22	
A23	AD26	AD27	B23	
A24	GND6	AD25	B24	
A25	AD24	P3_3V	B25	
A26	IDSEL	C_BE3*	B26	
A27	P3_3V	AD23	B27	
A28	AD22	GND12	B28	
A29	AD20	AD21	B29	
A30	GND9	AD19	B30	
A31	AD18	P3_3V	B31	
A32	AD16	AD17	B32	
A33	P3_3V	C_BE2*	B33	
A34	FRAME*	GND14	B34	
A35	GND13	IRDY*	B35	
A36	TRDY*	P3_3V	B36	
A37	GND22	DEVSL*	B37	
A38	STOP*	GND15	B38	
A39	P3_3V	LOCK*	B39	
A40	SDONE	PERR*	B40	
A41	SBO*	P3_3V	B41	
A42	GND25	SERR*	B42	
A43	PAR	P3_3V	B43	
A44	AD15	C_BE1*	B44	
A45	P3_3V	AD14	B45	
A46	AD13	GND23	B46	
A47	AD11	AD12	B47	
A48	GND17	AD10	B48	
A49	AD09	GND24	B49	
	KEY	KEY		A50 B50
	KEY	KEY		A51 B51
A52	C_BE0*	AD08	B52	
A53	P3_3V	AD07	B53	
A54	AD06	P3_3V	B54	
A55	AD04	AD05	B55	
A56	GND21	AD03	B56	
A57	AD02	GND19	B57	
A58	AD00	AD01	B58	
A59	P5V_8	P5V_9	B59	
A60	REQ64*	ACK64*	B60	
A61	P5V_12	P5V_5	B61	
A62	P5V_10	P5V_7	B62	

PCI SLOT 2

NOTE : CONNECT V_3P3_STBY TO PIN A14 (3.3VAUX)
FOR WAKE FROM S5 SUPPORT IF V_3P3_PCIAUX
IS NOT SWITCHED

BOM=CORE_PCI
V_3P3_PCIAUX R8C22
0   1A
603 EMPTY

BOM=CORE_PCI
V_3P3_STBY 1 R8C12   1_V_3P3_SLOT2
0   1A
603 CA

NOTE : WAKE FROM S5 IS SUPPORTED BY DEFAULT

BOM=CORE_PCI
732431-002
J8B2
PCI CONN CONN

NC=1,2

BOM=CORE_PCI
RP8E1
3   6
2.7K   5% 063W
5M   1C

PU_P_REQ64B*

P_AD<31..0>
P_C/BE<3..0>*

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PCI SLOT 3

BOM=CORE_PCI
732431-002
J9B2
PCI CONN CONN

VCC3   VCC   +12V   -12V   VCC   VCC3

28D8< 27D8< 17B4< 48C1>
62B8< 57C2<   IN   V_3P3_PCIAUX

21C6< 28C2> 27C7> 22A6>   OUT   P_INTH*
20A7< 28C2> 27C7> 22A6>   OUT   P_INTF*

40B3 IN   PCI_SLOT3_5*
30A8> 20A3> IN   P_GNT<2>*
28C7> 27C7> 20B8> 17B4<> OUT   P_PME*

30C3> 28B7<> 27B7<> 20B7<>   BI   P_FRAME*
30D3> 28B7<> 27B7<> 20B7<>   BI   P_TRDY*
30C3> 28B7<> 27B7<> 20B7<>   BI   P_STOP*
56B3 BI   ICH_SMB_CLK_PCISLOT3
56B3 BI   ICH_SMB_DATA_PCISLOT3
28B7<> 27B7<> 20B7<>   BI   P_PAR

VCC
BOM=CORE_PCI
RP8L_1
1   8
2.7K   PU_P_REQ64C*
5% 063W
SM
IC

28A7<> 27A7<> 20D7<>   BI   P_AD<31..0>
28A7<> 27A7<> 20B8>   BI   P_C/BE<3..0>*

Pin	Signal		Pin	Signal
A1	TRST*		B1	M12V_1
A2	P12V_1		B2	TCK
A3	TMS		B3	GND1
A4	TDI		B4	TDO
A5	P5V_2		B5	P5V_0
A6	INTA*		B6	P5V_1
A7	INTC*		B7	INTB*
A8	P5V_3		B8	INTD*
A9	RSVD1		B9	PRST1*
A10	P5V_4		B10	RSVD2
A11	RSVD3		B11	PRST2*
A12	GND10		B12	GND2
A13	GND16		B13	GND3
A14	3.3VAUX		B14	RSVD5
A15	RST*		B15	GND4
A16	P5V_6		B16	CLK
A17	GNT*		B17	GND7
A18	GND5		B18	REQ*
A19	PME		B19	P5V_11
A20	AD30		B20	AD31
A21	P3_3V		B21	AD29
A22	AD28		B22	GND8
A23	AD26		B23	AD27
A24	GND6		B24	AD25
A25	AD24		B25	P3_3V
A26	IDSEL		B26	C_BE3*
A27	P3_3V		B27	AD23
A28	AD22		B28	GND12
A29	AD20		B29	AD21
A30	GND9		B30	AD19
A31	AD18		B31	P3_3V
A32	AD16		B32	AD17
A33	P3_3V		B33	C_BE2*
A34	FRAME*		B34	GND14
A35	GND13		B35	IRDY*
A36	TRDY*		B36	P3_3V
A37	GND22		B37	DEVSL*
A38	STOP*		B38	GND15
A39	P3_3V		B39	LOCK*
A40	SDONE		B40	PERR*
A41	SBO*		B41	P3_3V
A42	GND25		B42	SERR*
A43	PAR		B43	P3_3V
A44	AD15		B44	C_BE1*
A45	P3_3V		B45	AD14
A46	AD13		B46	GND23
A47	AD11		B47	AD12
A48	GND17		B48	AD10
A49	AD09		B49	GND24
	KEY			KEY
A50 B50		A51 B51		
A52	C_BE0*		B52	AD08
A53	P3_3V		B53	AD07
A54	AD06		B54	P3_3V
A55	AD04		B55	AD05
A56	GND21		B56	AD03
A57	AD02		B57	GND19
A58	AD00		B58	AD01
A59	P5V_8		B59	P5V_9
A60	REQ64*		B60	ACK64*
A61	P5V_12		B61	P5V_5
A62	P5V_10		B62	P5V_7

NC=1,2

TP_PCI3_B4
TP_PCI3_A9
TP_PCI3_A11
TP_PCI3_B9
TP_PCI3_B10
TP_PCI3_B11
TP_PCI3_B14

P_INTB*   OUT   17B4<> 20B4> 27C2> 28C7> 30D8>
P_INTG*   22A6> 27C2> 28C7> 20A7<

CK_P_33M_S3   IN 4C4<
P_REQ<2>*   OUT   20B3<> 30A3>

P_IRDY*   BI   20B7<> 27B2<> 28B2<> 30C3>
P_DEVSEL* BI   20B7<> 27B2<> 28B2<> 30D3>
P_PLOCK*   BI   20B7<> 27B2<> 28B2<> 30D3>
P_PERR*   OUT   20B7<> 27B2> 28B2> 30D3>
P_SERR*   OUT   20B7<> 27B2> 28B2> 30C3>

P_ACK64*   OUT   28A2> 27A1<

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VCC3

20B3> OUT PU_P_PCIREQA*

BOM=CORE_PCI
1 R8F1 2
10K 5%
603 CH

20B4> 17C4< OUT P_INTA*

BOM=CORE_PCI
1 R7C5 2
8.2K 5%
603 CH

28C7> 27C2> 20B4> 17B4<>
29C2>
OUT P_INTB*

BOM=CORE_PCI
1 R8C5 2
8.2K 5%
603 CH

20B3> OUT PU_P_INTC*

BOM=CORE_PCI
1 R8E3 2
8.2K 5%
603 CH

20B3> OUT PU_P_INTD*

BOM=CORE_PCI
1 R8E2 2
8.2K 5%
603 CH

1
BOM=CORE_PCI
R7F1
10K
5%
EMPTY
603
2

VCC3

BOM=CORE_PCI   BOM=CORE_PCI
3 RP7D1 2   2 RP7D1
  2.7K   2.7K
  5%   5%
  .063W   .063W
  IC   IC
6 SM   7 SM

SPARES

VCC3

4 BOM=CORE_PCI   BOM=CORE_PCI
  RP7D1 1   1 RP7D1
  2.7K   2.7K
  5%   5%
  .063W   .063W
  IC   IC
5   8

P_SDONE BI   27B7<> 56C1<> 56D1<>

P_SBO* BI   27B7<> 56C1<> 56D1<>

VCC3

BOM=PCI_NONCOMP
2 1 R8C6 2
8.2K 5%
603 EMPTY

5 BOM=PCI_NONCOMP
1 R8E1 2
8.2K 5%
603 EMPTY

VCC

1 BOM=PCI_NONCOMP
1 R8C4 2
2.7K 5%
603 EMPTY

0 BOM=PCI_NONCOMP
1 R7C3 2
2.7K 5%
603 EMPTY

27C7< 20A3<>
29C7< 28C7<
OUT P_GNT<5..0>*

BOM=PCI_ATX_NONCOMP
20A2> OUT P_S5_GNT<4>*
1 R9E3 2
2.7K 5%
603 EMPTY

BOM=PCI_ATX_NONCOMP
20A2> OUT P_S4_GNT<3>*
1 R9E5 2
2.7K 5%
603 EMPTY

THESE PARTS ARE FOR THE ATX FORM FACTOR SLOTS

VCC3

29B2> 28B2> 27B2> 20B7<> OUT P_PERR*
1 R8D7 2
8.2K 5%
603 CH

29B2<> 28B2<> 27B2<> 20B7<> OUT P_DEVSEL*
BOM=CORE_PCI
1 R9D10 2
8.2K 5%
603 CH

29B7<> 28B7<> 27B7<> 20B7<> OUT P_TRDY*
BOM=CORE_PCI
1 R8D5 2
8.2K 5%
603 CH

29B2> 28B2> 27B2> 20B7<> OUT P_PLOCK*
BOM=CORE_PCI
1 R9D15 2
8.2K 5%
603 CH

VCC

29B2<> 28B2<> 27B2<> 20B7<> OUT P_IRDY*
1 R9D8 2
2.7K 5%
603 CH

29B7<> 28B7<> 27B7<> 20B7<> OUT P_FRAME*
BOM=CORE_PCI
1 R9D1 2
2.7K 5%
603 CH

29B2> 28B2> 27B2> 20B7<> OUT P_SERR*
BOM=CORE_PCI
1 R9D16 2
2.7K 5%
603 CH

29B7<> 28B7<> 27B7<> 20B7<> OUT P_STOP*
BOM=CORE_PCI
1 R9D13 2
2.7K 5%
603 CH

VCC

20B3> OUT P_S5_REQ<4>*
BOM=CORE_PCI
1 R9E2 2
2.7K 5%
603 CH

20B3> OUT P_S4_REQ<3>*
BOM=CORE_PCI
1 R9E4 2
2.7K 5%
603 CH

THESE PARTS ARE FOR THE ATX FORM FACTOR SLOTS

2 BOM=CORE_PCI
1 R9C2 2
2.7K 5%
603 CH

1 BOM=CORE_PCI
1 R8C3 2
2.7K 5%
603 CH

0 BOM=CORE_PCI
1 R7C4 2
2.7K 5%
603 CH

VCC3

5 BOM=CORE_PCI
1 R8D15 2
8.2K 5%
603 CH

29C2> 28C2> 27C2> 20B3<> OUT P_REQ<5..0>*

PCI PULL-UPS

NOTE : FWHX (ST MICRO) # A36561-001 USED IN BOM

PWRGD_3V   21C6< 10B7< 40A3< IN

32C6<> 21B6<> BI L_AD<3..0>

HMB HAS 10PF CAPS ON PINS 7 AND 8   U8G1
FWH   723644-009

726841-001
BOM=CORE_FWH
J9A1
JUMPER

BOM=CORE_FWH
RP9G2
3 1K
5%
.063W
IC
6 SM
SPARES

102276-003
J9G2
BOM=CORE_FWH
1X3HDR
HDR
I_J9G2_2

+12V

BOM=CORE_FWH
1 R8H6 2   PU_WP 7   WP
4.7K 5%
603   CH

BOM=CORE_FWH
1 R8H7 2   PU_TBL 8 8   TBL
4.7K 5%
603   CH

BOM=CORE_FWH
1 R9G6 2   PD_FWH_29   29   IC
4.7K 5%
603 EMPTY

40B6< 22B5< IN   P_RST_GLUE_FWH*   2   RST

4D4< 4D4< IN   CK_P_33M_FWH   31   CLK

32C6< 21A6< IN   L_FRAME*   23   FWH4

BOM=CORE_FWH
8 RP9G2
1K
5%
.063W
IC
SM

BOM=CORE_FWH
201924-001
Q9G2
FET

VCC3

I_FWH_VPP   1   VPP

FWH3 17   3
FWH2 15   2
FWH1 14   1
FWH0 13   0

DQ4/RFU 18   TP_FWH_18
DQ5/RFU 19   TP_FWH_19
DQ6/RFU 20   TP_FWH_20
DQ7/RFU 21   TP_FWH_21
RY/BY/RFU 22   TP_FWH_22

FGPI4 30 I_FWH_GPI4
FGPI3 3 I_FWH_GPI3
FGPI2 4 PN_FWH_GPI2
FGPI1 5 PN_FWH_GPI1
FGPI0 6 PN_FWH_GPI0

INIT 24 H_FLUSH_FWH*

27 VCCA/NC
32 VCC
25 VCC

28 GNDA/NC
16 GND
26 GND

ID3 9   TP_FWH_9
ID2 10 TP_FWH_10
ID1 11 TP_FWH_11
ID0 12 TP_FWH_12

IC

BOM=CORE_FWH
2 C9G7
1UF
20%
Y5V
603
1

PLACE CAP RIGHT AT PIN 1

BOM=CORE_FWH
1 R9G7
4.7K
5%
603
2

BOM=CORE_FWH
7 RP9G2
1K
5%
.063W
SM

AUD_LINK_SDO_ICH_R   BI 21A6<

VCC3

BOM=CORE_FWH
1 R9H3 1
4.7K
5%
603
2

BOM=CORE_FWH
R9H2
4.7K
5%
603
2

BOM=CORE_FWH
R9H5
4.7K
5%
EMPTY
603
2

BOM=CORE_FWH
R8H5 4
1K
5%
.063W
IC
5 SM

BOM=CORE_FWH
RP9G2
EMPTY
603
2

IN 40A3>

BOM=CORE_FWH
1 R9H4
10K
5%
603
2

BOM=CORE_FWH
1 R9H7
10K
5%
603
2

BOM=CORE_FWH
R9H8
10K
5%
603
2

VCC3

J7A1 JUMPER	MODE
JUMPER 1-2	NORMAL
JUMPER 2-3	CONFIG
NO JUMPER	RECOVERY

FWH GPIO	LOW	HIGH
FGPI0	LAN DOWN	NO LAN DOWN
FGPI1	UATX (FV)	ATX (EA2)
FGPI2	VGA DOWN	NO VGA DOWN

DESIGN NOTE: WHEN AUD_LINK_SDO_ICH IS HIGH AT RESET, BOARD IS IN SAFE MODE.
WHEN PN_FWH_GPI4 IS HIGH AT RESET, BOARD IS IN NORMAL MODE.
WHEN PN_FWH_GPI4 AND AUD_LINK_SDO_ICH ARE BOTH LOW AT RESET, BOARD IS IN CONFIG MODE.

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BOM=CORE_SIO
U7H1
LPC47M14X

PQFP
A05620-002

FLOPPY

Signal	Pin	Name
SIO_FDD_DRVDEN0	1	DRVDEN0/GP40
SIO_FDD_DRVDEN1	2	DRVDEN1/GP41
SIO_FDD_MTR0*	3	MTR0
SIO_FDD_DS0*	5	DS0
SIO_FDD_DIR*	8	DIR
SIO_FDD_STEP*	9	STEP
SIO_FDD_WDATA*	10	WDATA
SIO_FDD_WGATE*	11	WGATE
SIO_FDD_HDSEL*	12	HDSEL
SIO_FDD_INDEX*	13	INDEX
SIO_FDD_TRK0*	14	TRK0
SIO_FDD_WRTPRT*	15	WRTPRT
SIO_FDD_RDATA*	16	RDATA
SIO_FDD_DSKCHG*	4	DSKCHG

JOY

Signal	Pin	Name
GP10/J1B1	32	TP_SIO_GAME_J1B1
GP11/J1B2	33	TP_SIO_GAME_J1B2
GP12/J2B1	34	TP_SIO_GAME_J2B1
GP13/J2B2	35	TP_SIO_GAME_J2B2
GP14/J1X	36	TP_SIO_GAME_J1X
GP15/J1Y	37	TP_SIO_GAME_J1Y
GP16/J2X	38	TP_SIO_GAME_J2X
GP17/J2Y	39	TP_SIO_GAME_J2Y
GP25/MIDI_IN	46	TP_SIO_GAME_MIDI_IN
GP26/MIDI_OUT	47	TP_SIO_GAME_MIDI_OUT

GPIO

Signal	Pin	Name
P17/GP20	41	I_FV_FVT_SEL
GP21/P16/DS1*	42	I_SIO_GP21
GP22/P12/MTR1*	43	TP_SIO_43
SYSOPT/GP24	45	TP_SIO_45
LED1/GP60	48	TP_SIO_48
LED2/GP61	49	TP_SIO_49
IOSMI*/GP27	50	M_SMI_SIO*
GP43/DDRC	28	TP_SIO_28

LPC

	Pin	Name
IOPME*/GP42	17	
0	20	AD0
1	21	AD1
2	22	AD2
3	23	AD3
L_FRAME*	24	FRAME
L_DRQ*	25	DRQ
P_RST*	26	PCI_RESET
PU_SUS_STAT*	27	PD
CK_P_33M_SIO	29	PCI_CLK
SER_IRQ	30	SER_IRQ

L_AD<3..0>

KEY/MOUSE

Signal	Pin	Name
KDAT	56	SIO_KBDATA
KCLK	57	SIO_KBCLOCK
MDAT	58	SIO_MSDATA
MCLK	59	SIO_MSCLOCK
GP36/KBDRST	63	KBRST*
GP37/A20M	64	A20GATE

SERIAL 1

Signal	Pin	Name
SIO_COM_RXD1	84	RXD1
SIO_COM_TXD1	85	TXD1
SIO_COM_DSR1*	86	DSR1
SIO_COM_RTS1*	87	RTS1
SIO_COM_CTS1*	88	CTS1
SIO_COM_DTR1*	89	DTR1
SIO_COM_RI1*	90	RI1
SIO_COM_DCD1*	91	DCD1

PARALLEL

Signal	Pin	Name
PD0	68	0
PD1	69	1
PD2	70	2
PD3	71	3
PD4	72	4
PD5	73	5
PD6	74	6
PD7	75	7

SIO_PD<7..0>

Signal	Pin	Name
INIT	66	SIO_INIT*
SLCTIN	67	SIO_SLCTIN*
SLCT	77	SIO_SLCT
PE	78	SIO_PE
BUSY	79	SIO_BUSY
ACK	80	SIO_ACK*
ERR	81	SIO_ERR*
ALF	82	SIO_ALF*
STROBE	83	SIO_STROBE*

SERIAL 2 /GPIO

Signal	Pin	Name
GP50/R12*	92	
GP51/DCD2*	94	
GP52/RXD2/IRRX	95	
GP53/TXD2/IRTX	96	
GP54/DSR2*	97	
GP55/RTS2*	98	
GP56/CTS2*	99	
GP57/DTR2*	100	

IR

Signal	Pin	Name
IRRX2/GP34	61	SIO_IRRX2
IRTX2/GP35	62	SIO_IRTX2

FAN

Signal	Pin	Name
GP32/FAN2	54	FAN3_PWM
GP33/FAN1	55	FAN2_PWM
FAN_TACH1/GP30	51	FAN1_TACH
FAN_TACH1/GP31	52	FAN2_TACH

CLOCK

Signal	Pin	Name
VREF	44	
USBAVTR	113	
VTR	18	
VTR	122	
AVSS	40	
CLOCKI	19	
SUSCLK	6	CLKI32
I_CK_48M_USBHUB*	123	ICLK
	124	OCLK

Signal	Pin	Name
USB+	103	ICH_SIO_USB_P3
USB-	104	ICH_SIO_USB_P3*
PWREN1	114	TP_SIO_114
PWREN2	115	TP_SIO_115
PWREN3	116	TP_SIO_116
PWREN4	117	TP_SIO_117
PWROK1	118	ICH_U_OC1_2*
PWROK2	119	
PWROK3	120	
PWROK4	121	
NSTRP0	126	TP_SIO_126
NSTRP1	127	TP_SIO_127
IC		

Signal	Pin	Name
SIO_USB_P0	105	PD1+
SIO_USB_P0*	106	PD1-
SIO_USB_P1	107	PD2+
SIO_USB_P1*	108	PD2-
SIO_USB_P2	109	PD3+
SIO_USB_P2*	110	PD3-
SIO_USB_P3	111	PD4+
SIO_USB_P3*	112	PD4-

VCC3=53,65,93,125
GND=7,31,60,76,101,128

I_FV_FVT_SEL
| HI | MENDOCINO/COPPERMINE |
| LO | COPPERMINE/TUALATIN |

STUFF WHEN COM2 IS EMPTY

SIO_COM_RI2*
SIO_COM_DCD2*
SIO_COM_RXD2
SIO_COM_TXD2
SIO_COM_DSR2*
SIO_COM_RTS2*
SIO_COM_CTS2*
SIO_COM_DTR2*

SPARES

NOTE : PLACE R7H1 CLOSE TO PIN 123 OF THE SIO

ALL USB PAIRS MUST BE ROUTED AS DIFFERENTIAL PAIRS
7.5 / 7.5 / 7.5, AND 10 TO 12 MILS TO ALL OTHERS

IO_PME*
V_3P3_STBY
SER_IRQ
CK_14M_SIO
CK_4BM_USB2
CK_4BM_USB
I_CK_48M_USBHUB

BOM=USB_SIO_XTAL
BOM=USB_SIO_NOXTAL
630770-018
24.000MHZ
Y7H1

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VCC

3 BOM=CORE_FLOPPY
RP6H1
1K
5%
.063W
IC

4 BOM=CORE_FLOPPY
RP6H1
1K
5%
.063W
IC

1 BOM=CORE_FLOPPY
R6H3
1K
5%
CH
603

6 BOM=CORE_FLOPPY

2 BOM=CORE_FLOPPY
RP6H1
1K
5%
.063W
IC

5 BOM=CORE_FLOPPY

1 BOM=CORE_FLOPPY
RP6H1
1K
5%
.063W
IC

BOM=CORE_FLOPPY
732440-001
J6H2
2X17HDR_5

SIO_FDD_DRVDEN0   2   320 PIN
SIO_FDD_DRVDEN1   320 PIN
SIO_FDD_INDEX*   320 OUT
SIO_FDD_MTR0*   320 PIN
SIO_FDD_DS0*   320 PIN
SIO_FDD_DIR*   320 PIN
SIO_FDD_STEP*   320 PIN
SIO_FDD_WDATA*   320 PIN
SIO_FDD_WGATE*   320 PIN
SIO_FDD_TRK0*   320 OUT
SIO_FDD_WRTPRT*   320 OUT
SIO_FDD_RDATA*   320 OUT
SIO_FDD_HDSEL*   320 PIN
SIO_FDD_DSKCHG*   320 OUT

TP_301S
TP_302S
TP_303S
TP_304S
TP_305S

P1   1
P2   2
P3   3
P4   4
KEY
P6   6
P7   7
P8   8
P9   9
P10 10
P11 11
P12 12
P13 13
P14 14
P15 15
P16 16
P17 17
P18 18
P19 19
P20 20
P21 21
P22 22
P23 23
P24 24
P25 25
P26 26
P27 27
P28 28
P29 29
P30 30
P31 31
P32 32
P33 33
P34 34

HDR

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V_5P0_PS2_FB

47R PIN

656554-010
FB1A1
FB

I_V_5P0_PS2_FB

PS2 KEYBOARD

BOM=CORE_SIO
RP1A1
2.7K
5%
.063W
1C

BOM=CORE_SIO
RP1A1
2.7K
5%
.063W
1C

BOM=CORE_SIO
RP1A1
2.7K
5%
.063W
1C

BOM=CORE_SIO
RP1A1
2.7K
5%
.063W
1C

BOM=CORE_PS2
C1A1
.1UF
20%
EMPTY
603

BOM=CORE_PS2
C1A2
470PF
10%
X7R
603

BOM=CORE_PS2
749231-001
J1A1
PS2 STACK

SIO_KBDATA
32C BI

BOM=CORE_PS2
FP1A1
60R
300MA

I_SIO_KBDATA_FB

TP_401S

P1
P2
P3
P4
P5
P6

SIO_KBCLOCK
32C BI

BOM=CORE_PS2
FP1A1
60R
300MA

I_SIO_KBCLOCK_FB

TP_402S

P13 13
P14 14
P15 15
P16 16
P17 17

SIO_MSDATA
32C BI

BOM=CORE_PS2
FP1A1
60R
300MA

I_SIO_MSDATA_FB

TP_403S

P7
P8
P9
P10
P11
P12

SIO_MSCLOCK
32C BI

BOM=CORE_PS2
FP1A1
60R
300MA

I_SIO_MSCLOCK_FB

TP_404S

CONN

MOUSE

BOM=CORE_PS2
C1A3
470PF
10%
X7R
603

BOM=CORE_PS2
C1A4
470PF
10%
X7R
603

BOM=CORE_PS2
C1A5
470PF
10%
X7R
603

BOM=CORE_PS2
C1A6
470PF
10%
X7R
603

BOM=CORE_PS2
CRP1A1
TVS6_2V
6.2V
DIO
671835-001

ATX DOUBLE-STACKED

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DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N

SERIAL PORT A

BOM=CORE_COM1
621111-103
U4B1
GD75232S

BOM=CORE_COM1
749218-001
J4A1
2 ROW

SIO_COM_DCD1*	19	RY1 RA1 2
SIO_COM_DSR1*	18	RY2 RA2 3
SIO_COM_RXD1	17	RY3 RA3 4
SIO_COM_CTS1*	14	RY4 RA4 7
	12	RY5 RA5 9
SIO_COM_RTS1*	16	DA1 DY1 5
SIO_COM_TXD1	15	DA2 DY2 6
SIO_COM_DTR1*	13	DA3 DY3 8
	1	VDD+ VDD- 10

I_SIO_COM_DCD1-232
I_SIO_COM_DSR1-232
I_SIO_COM_RXD1-232*
I_SIO_COM_RTS1-232
I_SIO_COM_TXD1-232*
I_SIO_COM_CTS1-232
I_SIO_COM_DTR1-232
I_SIO_COM_RI1-232

DSUB

NOTE DIRECTION
IC
VCC=I_5VSB_VCC
VCC=20
GND=11

+12V   -12V

V_5P0_STBY IN

SIO_COM_RI1* B1 32B6<

BOM=CORE_COM1
1 R4B3 2
10K   5%
603   CH

+12V   -12V

BOM=CORE_COM1   BOM=CORE_COM1   BOM=CORE_COM1
1 C4A17   1 C4A14   1 C5B9
.1UF   .1UF   EMPTY
2 25V   2 25V   2
603   603   603

COM1 & SIO-POWER SOURCES OPTION

VCC

BOM=CORE_COM1
1 R4B2 2
0   1A
603 EMPTY

PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY

IN V_5P0_STBY

BOM=CORE_COM1
1 R4B1 2
0   1A
603 CH

I_5VSB_VCC

E*

E*= COM1 POWER_GROUP

NOTE : CONNECT 5VSB_VCC TO V_5P0_STBY FOR WAKE FROM S5 SUPPORT
       CONNECT 5VSB_VCC TO VCC IF NO WAKE FROM S5 SUPPORT

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8   7   6   5   4   3   2   1

BOM=CORE_COM2
621111-103
VCC=V_5P0_STBY
U9H1
GD75232S

SIO_COM_DCD2* 19 RY1   RA1 2
SIO_COM_DSR2* 18 RY2   RA2 3
SIO_COM_RXD2 17 RY3   RA3 4
SIO_COM_CTS2* 14 RY4   RA4 7
SIO_COM_RI2* 12 RY5   RA5 9
SIO_COM_RTS2* 16 DA1   DY1 5
SIO_COM_TXD2 15 DA2   DY2 6
SIO_COM_DTR2* 13 DA3   DY3 8
   1 VDD+   VDD- 10

32B
32B
32B
32B
32B
32B
32B
32B

NOTE DIRECTION
IC

VCC=20
GND=11

+12V   -12V

SERIAL PORT B

BOM=CORE_COM2
109717-010
J8H1
SERIAL PORT
2X5HDR_10

I_DCD2*   P1
I_RXD22   P2
I_TXD23   P3
I_DTR2*   P4
        P5
I_DSR2*   P6
I_RTS2*   P7
I_CTS2*   P8
I_RI2*   P9
       KEY

HDR

BOM=CORE_COM2
C8H9 470PF 50V 603
BOM=CORE_COM2
C8H5 470PF 50V 603
BOM=CORE_COM2
C8H14 470PF 50V 603
BOM=CORE_COM2
C8H13 470PF 50V 603
BOM=CORE_COM2
C8H4 470PF 50V 603
BOM=CORE_COM2
C8H6 470PF 50V 603
BOM=CORE_COM2
C8H8 470PF 50V 603

+12V   -12V

V_5P0_STBY IN

BOM=CORE_COM2
C9H4 1UF 20% 25V 603
BOM=CORE_COM2
C9H9 1UF 20% 25V 603
BOM=CORE_COM2
C8H2 1UF 20% 25V 603

45C7< 47B8< 48B7<
39D3< 40B2< 40C2<
39A4> 90?7< 26D2<
26D8< 35A8< 35B1<
43B6< 43D2< 44D4<
49B8< 55C5< 62D2<

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VCC ◁

BOM=CORE_FNTPNL
R9H15
100K
5%
EMPTY
603

BOM=CORE_FNTPNL
R9H14
330 5%
603 CH

VCC ◁

I_VCC_HDLED_PWR

40B7< 47D7< 47A4< 45C7< 43A8< 41D6< 40D2< 40C2< 40B2<
22C7< 22C3< 21A1< 20C1< 20B8< 20B1< 20A8< 8B4< 49B3<
40A7< 39D3< 39C8< 38B3< 32D8< 32A7< 32A1< 20B8< 27D8<
62C2< 61D4< 61B2< 59C8< 59B7< 59B2< 59B1< 56D8< 40C7<

BOM=FP_PWR_LED
102276-304
J9H5
1X3HDR2
HDR

BOM=CORE_FNTPNL
639823-001
J9H3
2X8NSTDFP

IN ▷ V_3P3_STBY

BOM=CORE_FNTPNL
R9H111
220
5%
CH
603

BOM=CORE_FNTPNL
R9H10
220
5%
CH
603

40B8 IN ▷ HD_LED*

40DB< 41C6< OUT ▷ FP_RST*

32B2< OUT ▷ SIO_IRRX2

32B2 IN ▷ SIO_IRTX2

VCC ◁

TP_FP_SLP*

VCC ▷ VCC

HDR

GPIO_GRN_BLNK_HDR IN ▷ 40A3>
GPIO_YLW_BLNK_HDR IN ▷ 40A3>

VCC ◁

BOM=CORE_FNTPNL
C9H12
470PF
100
EMPTY
603

BOM=CORE_FNTPNL
C9H6
470PF
100
EMPTY
603

BOM=CORE_FNTPNL
C9H5
470PF
100
EMPTY
603

BOM=CORE_FNTPNL
C9H14
470PF
100
EMPTY
603

BOM=CORE_FNTPNL
C9H8
470PF
100
EMPTY
603

BOM=CORE_FNTPNL
C8H1
1UF
20%
X5R
603

BOM=CORE_FNTPNL
C9H10
470PF
100
EMPTY
603

BOM=CORE_FNTPNL
C9H11
470PF
100
EMPTY
603

BOM=CORE_FNTPNL
C9H3
470PF
100
EMPTY
603

22C7< 22C3< 21A1<
20A8< 8B4< 49B3>
20C1< 20B8< 20B1<
38D4< 32D8< 27D8>
40A7< 39D3< 39C8<
40D2< 40C2< 40B2>
46C7< 43A8< 41D6<
49B7< 47D7< 47A4<
59B1< 56D8< 40C7>
59C8< 59B7< 59B2>
62C2< 61D4< 61B2>

IN ▷ V_3P3_STBY

BOM=CORE_FNTPNL
R9H12
22K
5%
CH
603

VCC3

BOM=CORE_FNTPNL
R9H13
0 1A
603 CH

I_SW_ON_R*

SW_ON* OUT ▷ 21C6<

BOM=CORE_FNTPNL
C9H7
10UF
100
EMPTY
603

BOM=CORE_FNTPNL
R8D4
220
5%
EMPTY
603

BOM=CORE_FNTPNL
R8D3
220
5%
EMPTY
603

VCC

AUD_PC_BEEP
50D8< 21B8< IN

BOM=CORE_SPKR
R9F12
1K 5%
603 CH

I_AUD_PC_BEEP1
BOM=CORE_SPKR

108969-001
Q2H1
MMBT3904
XSTR

BOM=CORE_SPKR
201826-001
L52H1
XDCR

BOM=CORE_SPKR
R9E10
10K
5%
EMPTY
603

BOM=CORE_SPKR
C2H4
1000PF
CH
EMPTY

I_AUD_PC_BEEP_PWR 1
BOM=CORE_SPKR
R2H9
47
5%
EMPTY

AT-08
IN

59B7< 62C2< 61D4<
48B7< 59B2< 59B1<
40D2< 47D7< 47A4<
39B3< 40C2< 40B2<
22C7< 32D5< 32A7<
20A8< 22C3< 21A1<
20C1< 8B4< 49B3<
33A1< 20B8< 20B1<
40A7< 28D8< 27D8<
46C7< 39D3< 38D4<
56D8< 43A8< 41D6<
61B2< 48C<
59C6<

V_3P3_STBY
IN

BOM=CORE_BATT
201453-601
CR9G1
2

V_3P0_BAT_VREG
3 OUT
21D2< 21D8<

XBT4G1
3

I_V_BATT_MAIN
BOM=CORE_BATT
R9G132
1K 5%
603 CH

BAT54C
SOT23C
DIO

3PCOIN
A26460-001
BOM=CORE_BATT

V_BAT_VREG_R_CP
OUT 21D8<

NOTE : BATTERY #202168-001

20B8< 20B1< 20A6< 8B4< 49B3<
27D8< 22C7< 22C3< 21A1< 20C1<
38B3< 32D5< 32A7< 32A1< 20DA<
40C2< 40B2< 40A7< 39C8< 38D4<
47A4< 46C7< 43A8< 41D6< 40D2<
59B1< 56D8< 48C7< 48B7< 47D7<
61D4< 61B2< 59C8< 59B7< 59B2<
62C2<

55C5< 49B6< 48B7< 47B6< 46C7< 44D4<
35B1< 35A8< 26D8< 26D2< 9D7< 39A4<
43D2< 43B6< 40C2< 40B2< 36B2<
62D2<

V_3P3_STBY
IN

V_5P0_STBY
IN

BOM=WOL_HDR
665515-003
J9G1
1X3HDR
I_J9G1_33
HDR

BOM=CORE_ICH2
R9G2
10K
5%
CH
603

BOM=WOL_HDR
R9G4
10K
5%
CH
603

I_WOL*

BOM=WOL_HDR
R9G3
100K
5%
CH
603

WOL*
OUT 21C6<

Q9G1
MMBT3904
XSTR
BOM=WOL_HDR

ITP RESET CIRCUIT

-12V   VCC3   VCC +12V

BOM=CORE_PWRCONN
R4H2
22K
5%
EMPTY

BOM=CORE_PWRCONN
J4H1
2X10 PWR 1MH

PS_ON*
40A8 IN

VCC

TP_PWR_2112

BOM=CORE_PWRCONN
C4H0
470PF
10%
X7R

CONN
650520-021

8B3 IN
DBRESET*

U2
74LVC08
1
2
3
IC
VCC=V_3P3_STBY
GND=7

U1
74LVC14
1   2
IC
VCC=V_3P3_STBY
GND=7

U1
74LVC14
3   4
IC
VCC=V_3P3_STBY
GND=7

R16
0
1A
CH
603

R14
0
603 EMPTY
1   2
1A

PWRGD_PS
OUT 40A6< 40C2<

V_5P0_STBY
OUT

49B8< 55C5< 62D2<
9D7< 26D2< 26D8< 35A8< 35B1< 36B2< 39D3< 40B2<
40C2< 43B6< 43D2< 44D4< 46C7< 47B8< 48B7<

BOM=CORE_PWRCONN
C3H12
20%
Y5V

BOM=CORE_PWRCONN
C3H8
470PF
10%
X7R

VCC

BOM=VCC_LOAD
R1C5
30
5%
CH
2512
202153-012

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

VCC3

BOM=CORE_GLUE4
R9F7
1K
5%
EMPTY
603

SCSI ACTIVITY LED

BOM=SCSI_HDR
107555-102
J8H2
1X2HDR
HDR

I_SCSI_ACT*
TP_SCSI_ACT_PIN2 40B6>

41C6> 38D8> [IN] FP_RST*
BOM=CORE_GLUE4
R9F9 2
330 5%
603 CH
C9FB
20UF
10U
50V
603
I_GLUE_FP_RST_R* [OUT] 40A6<

V_3P3_STBY [IN]
BOM=CORE_GLUE4
R9F3
10K
5%
EMPTY
603

40B6< 20A7> [OUT] GPIO_FLUSH_CACHE*

40B [IN] I_P_RST_SLOTS_R*
BOM=CORE_GLUE4
R9F2 2
33 5%
603 CH
P_RST_SLOTS* [OUT]
BOM=CORE_GLUE4
C9F3
20PF
50V
603

V_3P3_STBY [IN]

V_5P0_STBY [IN]

40A6< 39A3> [IN] PWRGD_PS

40B [IN] I_PCI_SLOT_5R1*
BOM=CORE_GLUE4
R9F6 2
33 5%
603 CH
PCI_SLOT3_5* [OUT] 29C8<
BOM=CORE_GLUE4
C9F5
20PF
50V
603

17C4<> 19A6< 27C7< 28C7<

VCC
BOM=CORE_GLUE4
R9F4
10K
5%
CH
603 VCC3

BOM=CORE_GLUE4
R9E6
10K
5%
CH
603

BOM=CORE_GLUE4
C9F6
1UF
20%
EMPTY
603
BOM=CORE_GLUE4
C9F9
1UF
20%
25V
603
BOM=CORE_GLUE4
C9F4
1UF
20%
25V
603

V_5P0_STBY [IN]

V_3P3_STBY [IN]

BOM=CORE_GLUE4
A12878-002
U9F1
GLUECHIP4

Pin	Signal		Signal	Pin
40D3> 20A7> [IN]	GPIO_FLUSH_CACHE* 4	GPO_FLUSH_CACHE*/GP2_IN	VREF5IN	45	PU_GLUE_VREF5V
20D [IN]	ICH_H_INIT* 6	INIT/GP1_INA	VREF3IN	1	PU_GLUE_VREF3V
31C6> 22B5> [IN]	P_RST_GLUE_FWH* 12	PCIRST	V_5P0_STBY	3	
11B [IN]	DDCSCL_3V 17	3V_DDCSCL	V_3P3_STBY		
4C [IN]	CK_P_33M_GLUE 49	CLK_IN	REF5V	44	V_REF5V 21D2<>
	21	CPU_PRESENT	HD_LED	24	HD_LED* 38D8<
23C [IN]	IDE_PRI_ACT* 25	PRIMARY_HD	PCIRST_OUT	13	I_P_RST_SLOTS_R* [OUT] 40C8<
40C [IN]	I_SCSI_ACT* 26	SCSI	AUD_RST	15	I_PCI_SLOT3_SR1* [OUT] 40B8<
23A [IN]	IDE_SEC_ACT* 27	SECONDARY_HD	MUTE_AUD	46	
	I_AUD_EN 14	AUD_EN	SCK_BJT_GATE	35	TP_SCK_BJT_GATE_ENABLE
	TP_AUD_SHDN 47	AUD_SHDN	FLUSH_OUT_FWH		
	TEST_EN 41	TEST_EN	FLUSH_OUT_CPU/GP1_OUT	31	H_FLUSH_FWH* 31B1<
	TP_GLUE4_SEL_33.66* 10	SEL_33_66	INIT_OUT/GP2_OUT	7	H_FLUSH_CPU* 6D5< 7D8<
19C [IN]	DDCSDA_5V 20	5V_DDCSDA	IDE_RSTDRV	8	H_INIT* 6D5< 7D8<
40C2> 39A3> [IN]	PWRGD_PS 32	PWRGD_PS	PWRGD_3V	16	IDE_RST* 23D8<
11B [IN]	DDCSDA_3V 19	3V_DDCSDA	PS_ON	28	BACKFEED_CUT* 48A8<
40D [IN]	I_GLUE_FP_RST_R* 18	FPRST	RSMRST	30	VREG_BACKFEED_U4 46A8<
19C [IN]	DDCSCL_5V 5	5V_DDCSCL	YLW_LED	34	PWRGD_3V 45A8<
47C7> 21C6> [IN]	SLP_S5* 36	SLP_S5	GRN_LED	23	PS_ON* 39A8<
21C [IN]	SLP_S3* 22	SLP_S3	HSYNC_5V	42	RSMRST* 21C6<
21C [IN]	GPIO_GRN_BLNK 37	GRN_BLNK	VSYNC_5V	39	GPIO_YLW_BLNK_HDR 38D2<
20B [IN]	GPIO_YLW_BLNK 38	YLW_BLNK	STRAP	40	GPIO_GRN_BLNK_HDR 38D2<
	TP_CORE_HSYNC_3V 49	HSYNC_3V	GP3_OUT	51	TP_HSYNC_5V
	TP_CORE_VSYNC_3V 50	VSYNC_3V		52	TP_VSYNC_5V
6B5> 20D4> [IN]	H_A20M*	A20M/GP1_INB		54	TP_GLUE_STRAP
	VREF_5U5 48	REF5V_STBY		56	PWRGD_PS_BUF [OUT] 56C8<
	I_VCCP_VREF 53	VCCP_VREF	GND	11	
	GP3_IN 55	GP3_IN	GND	29	
			GND	43	

IC

V_3P3_STBY [IN]
BOM=CORE_GLUE4
R9F5 2
10K 5%
603 CH

7D8< 7B8< 22D3>
21D2< 8D8< 8D2> [IN] V_1P5_CMOS
BOM=CORE_GLUE4
R8E4 2
33 5%
603 CH
21D [OUT]
BOM=CORE_GLUE4
R9F9 1
C9F1
1UF
20%
25V
603
BOM=CORE_GLUE4
C9F9
1UF
20%
25V
603

GLUECHIP4

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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

```
4BB7< 47D7< 47A4< 45C7< 43A8< 40D2< 40C2< 40B2< 40A7<
22C7< 22C3< 21A1< 20C1< 20B8< 20B1< 20A8< 8B4< 49B3<
39D3< 39C8< 38D4< 38B3< 32D8< 32A7< 32A1< 28D8< 27D8<
62C2< 61D4< 61B2< 59C8< 59B7< 59B2< 59B1< 56D8< 48C7<
```

IN V_3P3_STBY

NOTE : TAKE CARE TO PULL UP FP_RST*
        IF THERE IS NO PULL UP HERE

BOM=HECETA
R1C1
1K
5%
CH
603
2

38D8> OUT FP_RST*   BOM=HECETA
40D8<   1 R9H162
                       0   1A
                       603   CH

BOM=HECETA
715969-002
U1C1
HECETA4

I_HEC_A0/NTEST_OUT 16   A0/NTEST_OUT   VDD/3.3VIN 4   BOM=HECETA
                                                              C1C3
56C8< B1 ICH_SMB_DATA_AUX   SDA   1   1UF
56C8< B1 ICH_SMB_CLK_AUX 2 SCL   20%
                                                              Y5V
ROUTE TEMP SIGNALS AS A DIFFERENTIAL PAIR   2   603
6A PIN H_TEMP_SRC   9   RMT_DIODE-
6A OUT H_TEMP_RET   10   RMT_DIODE+

42A8< 8D4< 8C2< 3B8< 43D2> IN V_2P5
                            43B4> 45D5<
                            7D2< 42D2<
                                  6D2<
                            IN VCCP   15 +VCCP_IN
                                         14 +2.5VIN
                                         12 +5VIN   GNDD 3
                                         13 +3.3V

+12V VCC3 VCC
                                         11 +12V/VID4
                                          8 VID3
                                          7 VID2
                                          6 VID1
                                          5 VID0   IC

BOM=HECETA
1 R1C112
0   1A
603 EMPTY

BOM=HECETA
1 R1C12
0
1A
CH
603
2

42C8< 9B6> IN G_VID<4..0>
                                          4 3 1 0
```

HECETA 4

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NOTE: HEAVY TRACE ON VREG.

| POWER FET | CPU FREQ GHZ | RES (MILLIOHMS) |
|-----------|--------------|------------------|
| 704895-002 | 1.6 | 7 |

VCC

BOM=VREG
700917-102
L4B1
10A 1.7UH
IND

4D5< 41B5< 7D2< 6D2< 43B4>

OUT VCCP

BOM=VREG
C4B1
10UF
10V
EMPTY
1210

BOM=VREG
C4C3
1UF
10%
50V
603

BOM=VREG
C4C1
3300UF
10V
2RDL

BOM=VREG
C5B15
3300UF
10V
2RDL

BOM=VREG
C4B4
1UF
10%
50V
603

BOM=VREG
C4B2
4.7UF
10V
1206

BOM=VREG
C4B5
4.7UF
10V
1206

I_VREG_VCC

PLACE THESE CAPS CLOSE TO SOCKET_C

BOM=VREG
C4F2
3300UF
10V
2ALUM

BOM=VREG
C1C1
1500UF
10V
2RDL

BOM=VREG
C2C3
1500UF
10V
2RDL

BOM=VREG
C2B3
3300UF
10V
2ALUM

BOM=VREG
C1B5
1500UF
10V
2RDL

BOM=VREG
C1B4
1500UF
10V
2RDL

BOM=VREG
R2P1
00HM
ETCH
EMPTY
SM

*2

VCC

BOM=VREG
201645-001
R5B6 1
10
805  CH
5%

C5B20
.1UF 10%
16V
X7R
603

*1

BOM=VREG
201645-609
R5B1 1
0
805  CH
5%

+12V

BOM=VREG
R5C8
10K
5%
EMPTY
603

BOM=VREG
C5B18
1UF
10%
16V
603

BOM=VREG
C5B23
10UF
10%
16V
EMPTY
805
644066-006

VCC3

BOM=VREG
R5B5
0
1A
CH
603

NOTE: FETS NEED 2 SQ IN. OF
COPPER TOGETHER WITH
270 DEGREES ACCESS

704895-002
BOM=VREG
Q3B1
DPAK

PLACE CLOSE TO FET

BOM=VREG
R3B2 2
4.7  5%
805  CH
201645-612

I_VREG_FETDRVA_R 1

BOM=VREG
A51396-002
U5B1
SC1187A

IC

I_SC1187_V5

I_SC1187_V12

I_SC1187_V3P3

IN G_VID<4..0>  9B5>
41A6<

| | | |
|---|---|---|
| VCC | CS+ | |
| VID0 | CS- | |
| VID1 | VOSENSE | |
| VID2 | LDOEN | |
| VID3 | BSTH | |
| VID25MV | DH | |
| EN | PGNDH | |
| NC_6 | DL | |
| AGND | BSTL | |
| PGNDL | LDOV | |
| GATE2 | GATE1 | |
| LDOS2 | LDOS1 | |

TP_SC1187_6

VREG_1P25_GATE  43D>  OUT

*1

VTT_SENSE  43C>  IN

BOM=VREG
C4B1
10
100
EMPTY
603

PLACE NEAR
PIN 4
OF SC1187

VREG_2P5_GATE  43D>  OUT

V_2P5  IN  41B5<
6C2<
43D2>
3B5<
6D4<

BOM=VREG
C5B22
10
100
EMPTY
603

PLACE NEAR
PIN 3
OF SC1187

PWRGD_VTT_5V*  IN  9C4< 43B2>
43B8<

BOM=VREG
R3C8
10K
5%
CH
603

I_COMP_VREG

BOM=VREG
Q3C2
MMBT3904
XSTR
108969-001

I_Q4SR2_1

I_VREG_FETDRVA

I_VREG_FETDRVB

I_VREG_VCCP_L

BOM=VREG
R3B1
0
CH
805

I_VREG_VCCP_PD

704895-002
BOM=VREG
Q3B2
DPAK

BOM=VREG
R3B3 2
0
805  CH
201645-609

I_VREG_FETDRVB_R 1

BOM=VREG
A15219-001
L3B1
1.2UH IND

I_VREG_VCCP_LR

DFP
BOM=VREG
712487-006
R2B2 2
.002  5% 1W
2512  CH

BOM=VREG
A04876-002
R2B5 2
.002  5% 2W
4527 EMPTY

BOM=VREG
R2B3
00HM
ETCH
EMPTY
SM

BOM=VREG
R2B4
00HM
ETCH
EMPTY
SM

BOM=VREG
C3B2
4700PF
10%
50V
603

I_VREG_CSP

BOM=VREG
C3P10
10
100
X7R
603

PLACE CLOSE
TO THE IC

BOM=VREG
R5C112
1K
603  CH

I_VREG_CSP_R

BOM=VREG
R5B4
2.2K
5%
EMPTY
603

BOM=VREG
R5B3 2
10
603 EMPTY

BOM=VREG
R5C13
0
1A
CH
603

I_VREG_CSN

I_VREG_VO_SENSE

BOM=VREG
C5B17
10
100
EMPTY
603

BOM=VREG
R5C12
0
1A
EMPTY
603

*1

NOTE *1 :
ALL ANALOG GND
ARE ROUTED WITH A
25 MIL TRACE TO NEAREST
OUTPUT BULK CAP GROUND
AT *2

# CPU REGULATION

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(815) LINEAR REGULATORS

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5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

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VTT SPEC +-9% FOR TRANSIENTS, +-3% FOR DC LEVEL
VTT: 1.25V FOR TU

NOTE :-
ADM1051    #745953-002
MC33567    #745953-003
ADM1051A   #745953-005

NOTE : IF ADM1051 OR MC33567 IS USED, SEQUENCING CIRCUIT MUST BE STUFFED

DESIGN NOTE:ASSUME(3)0.1@LOAD

CAD NOTE:
PLACE NEAR AGP SLOT

DESIGN NOTE: FOR VGA

CLOSE TO ADM1051

CLOSE TO ADM1051

STUFF FOR ADM1051
STUFF FOR MC33567
EMPTY FOR ADM1051A

EMPTY FOR ADM1051
EMPTY FOR MC33567
STUFF FOR ADM1051A

STUFF FOR ADM1051
STUFF FOR MC33567
EMPTY FOR ADM1051A

PLACE NEAR
20 OHM

PLACE NEAR
0 OHM

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

VTT

BB7< BA4< 7C4< 7B2< 7A8< 6D1< 43C
61D7< 43B8< 13D2< 9D8< 9C5<

41B5< 7D2< 6D2< 43B4> 42D2>

VCCP

**Column (VTT):**

C2D22 — 20% 1UF X5R 603
C3D1 — 20% 1UF X5R 603
C2D17 — 20% 1UF X5R 603
C2C1 — 20% 1UF X5R 603
C1D5 — 20% 1UF X5R 603
C2D30 — 20% 1UF X5R 603
C2D31 — 20% 1UF X5R 603
C2D35 — 20% 1UF X5R 603
C2D10 — 20% 1UF X5R 603
C2D11 — 20% 1UF X5R 603
C1 — 1UF 20% X5R EMPTY 603
C2 — 1UF 20% X5R EMPTY 603

**Column 1 (VCCP):**

C3E1 — .47UF 20% X5R 603
C1E2 — .47UF 20% X5R 603
C2F1 — .47UF 20% X5R 603
C2F2 — .47UF 20% X5R 603
C1E3 — .47UF 20% X5R 603
C2D43 — .47UF 20% X5R 603
C2E1 — .47UF 20% X5R 603
C2D15 — .47UF 20% X5R 603
C2D13 — .47UF 20% X5R 603
C2D3 — .47UF 20% X5R 603
C2D6 — .47UF 20% X5R 603
C2D7 — .47UF 20% X5R 603
C3 — .47UF 20% X5R EMPTY 603

**Column 2 (VCCP):**

C2D1 — .47UF 20% X5R 603
C2D12 — .47UF 20% X5R 603
C2D14 — .47UF 20% X5R 603
C2D38 — .47UF 20% X5R 603
C2D27 — .47UF 20% X5R 603
C2D37 — .47UF 20% X5R 603
C2D16 — .47UF 20% X5R 603
C2D5 — .47UF 20% X5R 603
C2D4 — .47UF 20% X5R 603
C2D25 — .47UF 20% X5R 603
C2D28 — .47UF 20% X5R 603
C3D4 — .47UF 20% X5R 603
C4 — .47UF 20% X5R EMPTY 603

**Column 3 (VCCP):**

C2D23 — 10UF 10% X7R 1206
C2D40 — 10UF 10% X7R 1206
C2D41 — 10UF 10% X7R 1206
C2D39 — 10UF 10% X7R 1206
C2D29 — 10UF 10% X7R 1206
C2D21 — 10UF 10% X7R 1206
C2D18 — 10UF 10% X7R 1206
C2D19 — 10UF 10% X7R 1206
C2D20 — 10UF 10% X7R 1206
C2D33 — 10UF 10% X7R 1206

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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

VCC3

BOM=VREG_NO_STR
1 R3G12
0    1A
805  EMPTY

BOM=VREG_NO_STR
1 R3G22
0    1A
805  EMPTY

BOM=VREG_STR
A31520-001
Q3G1
IRF7317

VCC3

IN   V_3P3_STBY

1  S1   D1  8
2  G1   D1  7
3  S2   D2  6
4  G2   D2  5

IC

NOTE : SI4501DY #A03106-001

V_3P3_STR   OUT

1        1        1
C4F3     CAF_4    CSF1
1UF      1UF      100UF
20%      20%      20%
2  16V   2  16V   2  EMPTY
603      603      RDL

IN   V_5P0_STBY

+12V

BOM=VREG_STR          BOM=VREG_STR
RP3H1                 RP3H1
3.3K        BOM=VREG_STR   3.3K
5%          1 R3H1    1   5%
.063W       R3H1          .063W
            10K           IC
IC          5%            SM
SM          EMPTY
            603

BOM=VREG_STR  1
4 R3H2
R3H2
1K
5%
CH
5       603      2      8

V_3P3_STR   IN

BOM=VREG_STBY_LED
1 R5E5
330
5%
CH
2   603

I_VREG_MAIN_STBY_LED_R

BOM=VREG_STBY_LED
2 716805-001
CR6E1
GREEN
1  LED

STR LED DISPLAY

BOM=VREG_STR
710127-001
Q3H1
MBT3904DUAL

BOM=VREG_STR
RP3H1
3.3K
5%
.063W
IC
SM

40A PIN   VREG_BACKFEED_U

BOM=VREG_STR
RP3H1
2
3.3K        I_VREG_SLP  5
SM   5% 063W
         IC

3    6

2    6

4

XSTR

I_P51_Q3H1_P2

VREG_USB_NCH   OUT   26D8< 47B8<

VREG_USB_PCH   OUT   26C8< 47A8<

STR

V_3P3_STBY

BOM=VREG
R9G1
10K
5%
CH
603

1 R9F132    I_SLP_S5A*
10K    5%
603    CH
202285-073

ICH_U_OC1_2*    OUT    21A6< 32A2<

SLP_S5*    40A6< 21C6<    IN

710127-001
BOM=VREG
Q9F1
MBT3904DUAL    3    6

1 R9F122    I_SLP_S5*
10K    5%
603    CH    5    2

4    1    XSTR

V_5P0_STBY_FPUSB_CNR    57C8< 47B4< 26C2<    IN

BOM=VREG
1 RT2A1
THRMSTR
2.60

V_5P0_USB    OUT    24D4< 25D5<

USB_FP_OC*    26B    IN
BOM=USB_FP
1 R8G122
10K    5%
603 EMPTY

VREG_USB MUST BE SPLIT
AMONSGT ALL USB CHANNELS.
DO NOT DAISY CHAIN

VCC

BOM=VREG_NO_WAKE_USB_PS2
R2B1
0
1A
EMPTY
805

BOM=VREG_NO_WAKE_USB_PS2
R1A2
0
1A
EMPTY
805

VCC

BOM=VREG_WAKE_USB_PS2
A31520-001
Q2B1
IRF7317

S1    D1    8
G1    D1    7
S2    D2    6
G2    D2    5

IC

VREG_USB_NCH    26D8< 45A2>    IN    2
V_5P0_STBY    3
VREG_USB_PCH    26C8< 45A2>    IN    4

I_VREG_USB_Q

NOTE : SI4501DY #A03106-001

1 BOM=VREG
R1A1
1%
CH
603

BOM=VREG
+ 1C2B4
100UF
20%
EEC
RDL

V_5P0_STBY_FPUSB_CNR    57C8< 47C7< 26C2<    IN

BOM=CNR
R9C5 2
10K    5%
603 EMPTY

BOM=CNR
VCC=V_3P3_STBY
U9D2
74LVC00A

CNR_OC*    62C2< 61D4< 61B2< 59C8< 57C    PIN
48C7< 48B7< 47D7< 46C7<
40B2< 40A7< 39D3< 39C8<
32A1< 2BDB< 27DB< 22C7<
20B1< 20A8< 8B4< 49B3<
22C3< 21A1< 20C1< 20B8<
3BD4< 3BB3< 32DB< 32A7<
43A6< 41D6< 40D2< 40C2<
59B7< 59B2< 59B1< 56D8<    12

13

11    I_CNR_OC

BOM=CNR
R9E12
10K    5%
603 EMPTY

1    I_CNR_OCA

3    BOM=CNR
100959-001
Q9F1
MMBT3904
EMPTY

V_3P3_STBY    IN

VCC3=14
GND=7
676294-102

THESE REFDES WILL CHANGE ON EASTON2.

BOM=CORE_PS2
RT1B1
1    2
THRMSTR
1.50

V_5P0_PS2_FB    OUT    34D8<

2 202285-049

# WAKE ON USB & PS2

8 7 6 5 4 3 2 1

V_3P3_STR
IN

46B2< 16B7< 15C8< 15B5< 14B1< 12B2< 45C2>
62C4< 61B8<

BOM=VREG_NO_PCIVAUX
R7E4
0
1A
CH
805

BOM=VREG_NO_PCIVAUX
R7E2
0
1A
CH
805

VCC3

V_3P3_PCIAUX
OUT

57C2< 52B8<
17B4< 27D8<
28D8< 29D7<

BOM=VREG
C7E1
.1UF
20%
16V
603

BOM=VREG
C7D5
.1UF
20%
16V
603

BOM=VREG
C8C4
100UF
25V
ELEC
RDL

BOM=VREG
C8C2
.1UF
20%
EMPTY
603

BOM=VREG_PCIVAUX
A31520-001
QBC2
IRF7317

I_VREG_PCIAUX_N_ON

S1  D1
G1  D1
S2  D2
G2  D2

EMPTY

NOTE :-
USE SI4501DY (A03106-001)
AS ALTERNATIVE PART

V_3P3_STBY
IN

47D7< 47A4< 45C7< 43A8< 41D6< 40D2< 40C2< 40B2< 40A7<
22C7< 22C3< 21A1< 20C1< 20B8< 20A8< 8B4< 49B3<
39D3< 39C8< 38D4< 38B3< 32D8< 32A7< 32A1< 28D8< 27D8<
62C2< 61D4< 61B2< 59C8< 59B7< 59B2< 59B1< 56D8< 48B7<

V_5P0_STBY
IN

40C2< 40B2< 39D3< 36B2< 35B1< 35A8< 26D8< 26D2< 9D7< 39A4>
62D2< 55C5< 49B8< 47B8< 46C7< 44D4< 43D2< 43B6<

+12V

BOM=VREG_PCIVAUX
RP8B3
2.7K
5%
.063W
EMPTY
SM

BOM=VREG_PCIVAUX
RP8B3
2.7K
5%
.063W
EMPTY
SM

I_VREG_PCIAUX_P_OFF

V_3P3_STBY
IN

62C2< 61D4< 61B2<
56D8< 48C7< 47D7< 47A4<
40C2< 40B2< 40A7< 39D3<
32A7< 32A1< 28D8< 27D8<
20B8< 20B1< 20A8< 8B4< 49B3<
39C8< 22C7< 22C3< 21A1< 20C1<
46C7< 43A8< 41D6< 40D2<
59C8< 59B7< 59B2< 59B1<

BOM=VREG_PCIVAUX
R9C1
1K
5%
EMPTY
603

BOM=VREG_PCIVAUX
710127-001
QBC1
MBT3904DUAL

BOM=VREG_PCIVAUX
RP8B1
2.7K 5% .063W
SM  EMPTY

I_VREG_BACKFEED

BOM=VREG_PCIVAUX
RP8B3
2.7K 5% .063W
SM  EMPTY

I_VREG_BACKFEED

I_VREG_BACKFEED_CUT

BOM=VREG_PCIVAUX
RP8B3
2.7K 5% .063W
SM  EMPTY

I_VREG_BACKFEED_CUT

BOM=VREG_PCIVAUX
RP8B1
2.7K 5% .063W
SM  EMPTY

EMPTY

BACKFEED_CUT
40A PIN

SPARE

BOM=VREG_PCIVAUX
RP8B1
2.7K 5% .063W
SM  EMPTY

BOM=VREG_PCIVAUX
RP8B1
2.7K 5% .063W
SM  EMPTY

PCI VAUX

BOM=VREG
305143-001
U9F2

LM317L
IN
OUT
ADJ
NC=5,8
IC

BOM=VREG
R9F10
100
1%
CH
603

V_1P8_STBY OUT 20C1< 22D3<

BOM=VREG
C9F2
1UF
20V
Y5V

BOM=VREG
C9F10
22UF
20V
ELEC
RDE

I_P54_U9F2_P4

BOM=VREG
R9F11
45.3
1%
CH
603

BOM=VREG
658916-101
U3H1
MC33269

IN    OUT
ADJ
EMPTY

45C7< 44D4< 43D2< 43B6< 40C2<
35A8< 26D8< 26D2< 9D7< 39A4<
40B2< 39D3< 36B2< 35B1<
62D2< 55C5< 48B7< 47B8<

V_5P0_STBY IN

V_3P3_STBY OUT

BOM=VREG
C3H5
22UF
20V
ELEC
RDE

BOM=VREG
C9G4
1UF
20V
EMPTY

BOM=VREG
C3H1
22UF
20V
ELEC
RDE

56D8< 59B1< 59B2< 59B7< 59C8< 61B2< 61D4< 62C2<
39D4< 39C8< 39D3< 40A7< 40B2< 40C2< 40D2<
8B4< 20A8< 20B1< 20B8< 20C1< 21A1< 22C3<
22C7< 27D8< 28D8< 32A1< 32A7< 32D8< 38B3<
41D6< 43A8< 46C7< 47A4< 47D7< 48B7< 48C7<

BOM=VREG
715453-002
U3H2
EZ1086

IN    OUT
ADJ   OUT
IC

NOTE:
EZ1086 = 1.5A
MC33269 = 0.7A

NOTE : ACTUAL PART USED IN
THE BOM IS 715453-001

715453-001 IS 3.45V

1.8V & 3.3V STANDBY

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AUD_LINK_SDO_ICH_CODEC `58C <IN>`

AUD_LINK_SYNC_ICH_CODEC `58C <IN>`

CDC_DWN_RST* `57A <IN>`

AUD_LINK_RST* `57A6< 21B7> <IN>`

AUD_PC_BEEP `39D8< 21B8< <IN>`

AUD_MONO_IN `52A <IN>`

AUD_LAUXIN `52D <IN>`
AUD_RAUXIN `52D <IN>`

AUD_SPDIF_SENSE1 `54D <IN>`

AUD_LCD `52C <IN>`
AUD_CDGND `52C <IN>`
AUD_RCD `52B <IN>`
AUD_MIC_IN `52B <IN>`
AUD_LLINEIN `52A <IN>`
AUD_RLINEIN `52B <IN>`

AUD_A_VREF `51D8< 50B3> <IN>`

V_5P0_AUD_ANALOG `50C1< 55C2> 53D1< 53B1< <IN>`

CK_14M_AUD `<IN> 4C1>`

AUD_LINK_BCLK_ICH_CODEC `<OUT> 58C5<`

V_5P0_AUD_ANALOG `<IN> 53B1< 53C2< 50AB< 53D1<`

AUD_LINK_SDI0_ICH_CODEC `<OUT> 58C5<`

AUD_SPDIF_OUT `<OUT> 54B8<`

AUD_CDC_LOUT_HP `<OUT> 54C8<`
AUD_CDC_ROUT_HP `<OUT> 54D8<`

AUD_MONO_OUT `<OUT> 52A2<`

AUD_A_REFFLT `<OUT> 51D8<`
AUD_A_VREF `<OUT>`
AUD_AFLT1 `<OUT> 51D8<`
AUD_AFLT2 `<OUT>`
AUD_AFLT3 `<OUT> 51C8<`
AUD_AFLT4 `<OUT> 51C8<`
AUD_3D_R `<OUT>`

AUD_3D_C `<OUT> 51B8<`

NOTE : CS4201  #A12325-002
NOTE : ADI1886 #A53991-001

NOTE :-
USE 0 OHM
(108506-004) WHEN
AUDIO CODEC CRYSTAL
IS NOT STUFFED

USE 33 OHM
(202285-013) FOR
CS4201

U9A2
A14470-001
AD1885
BOM=AUDIO

| pin | name | | name | pin |
|---|---|---|---|---|
| 2 | XTL_IN | | XTL_OUT | 3 |
| 5 | SDATA_OUT | | BIT_CLK | 6 |
| 10 | SYNC | | SDATA_IN | 8 |
| 11 | RESET | | | |
| 45 | ID0 | | JS1 | 48 |
| 46 | ID1 | | HP_OUT_L | 39 |
| 47 | EAPD/JS0 | | HP_OUT_R | 41 |
| 12 | PC_BEEP | | | |
| 13 | PHONE | | LINE_OUT_L | 35 |
| 14 | AUX_L | | LINE_OUT_R | 36 |
| 15 | AUX_R | | MONO_OUT | 37 |
| 16 | VIDEO_L | | | |
| 17 | VIDEO_R | | REFFLT | 27 |
| 18 | CD_L | | VREFOUT | 28 |
| 19 | CD_GND | | AFLT1 | 29 |
| 20 | CD_R | | AFLT2 | 30 |
| 21 | MIC1 | | HPCFG | 31 |
| 22 | MIC2 | | FLT3D | 32 |
| 23 | LINE_IN_L | | FLTI | 33 |
| 24 | LINE_IN_R | | AVDD3 | 43 |
| 34 | FLTO | | AVSS3 | 44 |
| 1 | DVDD1 | | AVSS2 | 40 |
| 9 | DVDD2 | | | |
| 4 | DVSS1 | | | |
| 7 | DVSS2 | | | |
| 25 | AVDD1 | | | |
| 38 | AVDD2 | | | |
| 26 | AVSS1 | | | |
| 42 | NC | | | |

NC=49    IC

I_1885_11
I_AUD_CK_24M_XTL_I
I_AUD_CK_24M_XTL_O
I_AUD_LINK_BCLK_CODEC_R
I_AUD_LINK_SDI_CODEC_R
I_1885_45
TP_1885_46
TP_1885_47
I_1885_12
I_AUD_MONO_IN_R
I_AUD_SPDIF_SENSE_R
TP_AUD_CDC_LOUT
TP_AUD_CDC_ROUT
I_AUD_AVSS3_43
I_AUD_AVSS3_44
I_AUD_AVSS2_40

Y9B1
630770-010
24.576MHZ
SM
XTAL

NOTE :-
*1 STUFF AND USE 22PF (603725-112) WHEN
CRYSTAL IS STUFFED
(BOTH ADI1885 AND CS4201)

UNSTUFF FOR ADI1885 AND NO CRYSTAL
CONFIGURATION.

STUFF AND CHANGE TO 220PF (602431-004)
FOR CS4201 AND NO CRYSTAL COMBINATION.

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KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC.✱✱✱✱✱✱✱✱

AUD_A_REFFLT

AUD_A_VREF

AUD_AFLT1

AUD_AFLT2

AUD_AFLT3

AUD_AFLT4

AUD_3D_R

AUD_3D_C

STUFF FOR
ANALOG DEVICE CRYSTAL AND
SIGMATEL CODECS

STUFF FOR
AD1885 ONLY

STUFF FOR
CS4201 ONLY

STUFF FOR
ANALOG DEVICE CODECS
AND CRYSTAL CODECS

STUFF FOR ANALOG
DEVICES CODECS

STUFF FOR
AD1885 ONLY

STUFF FOR
CS4201 ONLY

STUFF FOR
CS4201 ONLY

MULTI LAYOUT FOR
AD1885 AND CS4201

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AUX IN
ATAPI HEADER

BOM=AUDIO
663573-010
J6B4
1X4HDR

HDR
WHITE

I_AUD_LAUXIN_R

RP8A3
BOM=AUDIO
6.8K 5% .25W
SM     IC

BOM=AUDIO
RP8A3
6.8K 5% .25W
SM     IC

I_AUD_RAUXIN_R

BOM=AUDIO
RP8A3
6.8K
.25W
IC
SM

BOM=AUDIO
RP8A3
6.8K
.25W
IC
SM

I_AUD_LAUXIN_C

BOM=AUDIO
CBA11
1UF 10%
10V
X5R
B05

AUD_LAUXIN  OUT  50CB<

I_AUD_RAUXIN_C

BOM=AUDIO
CBA13
1UF 10%
10V
X5R
B05

AUD_RAUXIN  OUT  50CB<

CD IN
ATAPI HEADER

BOM=AUDIO
663573-001
J6B3
1X4HDR

HDR
BLACK

I_AUD_LCD_R

RP8A4
BOM=AUDIO
6.8K 5% .25W
SM     IC

BOM=AUDIO
RP8A4
6.8K 5% .25W
SM     IC

I_AUD_CDGND_R

BOM=AUDIO
RP8A4
6.8K 5% .25W
SM     IC

I_AUD_RCD_R

RP8A4
BOM=AUDIO
6.8K 5% .25W
SM     IC

BOM=AUDIO
RP8A2
6.8K
5%
.25W
IC
SM

BOM=AUDIO
RP8A2
6.8K
5%
.25W
IC
SM

BOM=AUDIO
RP8A2
6.8K
5%
.25W
IC
SM

BOM=AUDIO
RP8A2
6.8K
5%
.25W
IC
SM

I_AUD_LCD_C

BOM=AUDIO
CBA10
1UF 10%
10V
X5R
B05

AUD_LCD  OUT  50B8<

I_AUD_CDGND_C

BOM=AUDIO
CBA9
1UF 10%
10V
X5R
B05

AUD_CDGND  OUT  50B8<

I_AUD_RCD_C

BOM=AUDIO
CBA7
1UF 10%
10V
X5R
B05

AUD_RCD  OUT  50B8<

ALL AUDIO CON GND PINS SHOULD BE NO-SHAPE-CONNECT

LITE BLUE, TOP

BOM=AUDIO
A06125-001
J6A2
3 STACK AUDIOJACK

JACK

JACKSHIELD

54C2> 53CB> 53C1>  IN

BOM=AUD_LINEIN
FB6A5
FB

I_AUD_RLINEIN_R

BOM=AUD_LINEIN
RP8A1
6.8K 5% .25W
SM     IC

BOM=AUD_LINEIN
FB6A2
FB

I_AUD_LLINEIN_R

BOM=AUD_LINEIN
RP8A1
6.8K 5% .25W
SM     IC

BOM=AUD_LINEIN
CBA10
100PF
50V
X7R
B03

BOM=AUD_LINEIN
CBA7
100PF
10%
50V
X7R
B03

BOM=AUD_LINEIN
RP8A1
6.8K
5%
.25W
IC
SM

BOM=AUD_LINEIN
RP8A1
6.8K
5%
.25W
IC
SM

I_AUD_RLINEIN_C

BOM=AUD_LINEIN
CBA5
1UF 10%
10V
X5R
B05

AUD_RLINEIN  OUT  50B8<

I_AUD_LLINEIN_C

BOM=AUD_LINEIN
CBA6
1UF 10%
10V
X5R
B05

AUD_LLINEIN  OUT  50B8<

BOM=AUD_TELE
J8B1
1X4HDR

EMPTY
GREEN
NC=5
663573-011

TELEPHONY
ATAPI HEADER

BOM=AUDIO
R7A12
0
1A
EMPTY
603

BOM=AUDIO
R8A11
0
1A
EMPTY
603

BOM=AUDIO
R6A1
0
1A
CH
603

AUD_MONO_IN  OUT  50CB<

BOM=AUD_TELE
C8B14
1.0UF 10%
EMPTY
603

AUD_MONO_OUT  IN  50B2>

NOTE : CONNECT TO SOMEWHERE
NEAR CODEC GROUND

NOTE : CONNECT TO A MOUNTING HOLE
NEAR CODEC (MH6A1)
(ISOLATED GROUND)

NOTE : CONNECT TO THE NEAREST
MOUNTING HOLE (MH7A1)
NEXT TO JACK SHIELD

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ALL AUDIO CON GND PINS SHOULD BE NO-SHAPE-CONNECT

I_AUD_MIC_BIAS

MIC IN
PINK, BOTTOM
BOM=AUDIO
A06125-001
J6A2
3 STACK AUDIOJACK

PLACE NEAR MIC AMP
BOM=AUDIO
202285-051
R7A6
1.2K 5%
603 CH
NOTE : USE 2.2K (202285-057)
WHEN MIC AMP (LF353)
IS STUFFED.

BOM=AUD_NO_MIC_AMP STUFF FOR NO MIC AMP
R7A72
2.2K 5%
603 CH

U8A1
LF353

I_AUD_MIC_BIAS_REF

BOM=AUD_MIC_AMP
R7A9
10K 5%
EMPTY

V_5P0_AUD_ANALOG

NEAR
AMP

BOM=AUDIO
C7A4
1.0UF
100
EMPTY
603

I_AUD_MIC_BIAS_R

I_AUD_MIC_IN_FB

BOM=AUD_NO_MIC_AMP
C7A1
1.0UF STUFF FOR NO MIC AMP
10V
603

JACKSHIELD

I_AUD_MIC_PD

AUDIO FRONT PANEL

NOTE :
2-STACK AUDIO JACK
A06132-001

CUSTOM AUDIO FRONT PANEL HEADER

AUD_L_FNTOUT
AUD_R_FNTOUT

BOM=AUDIO_GW
109717-106
J6B1
2X3HDR_6

EMPTY

AUD_L_RETIN
AUD_R_RETIN

AUD_MIC_IN

NOTE :-
*1 STUFF WHEN AUDIO MIC AMP OR AUDIO FRONT PANEL OR BOTH ARE STUFFED
*2 STUFF WHEN THERE IS NO AUDIO MIC AMP BUT AUDIO FRONT PANEL IS STUFFED
*3 UNSTUFF WHEN AUDIO MIC AMP OR AUDIO FRONT PANEL OR BOTH ARE STUFFED
*4 UNSTUFF WHEN THERE IS NO AUDIO MIC AMP BUT AUDIO FRONT PANEL IS STUFFED

AUD_MIC_IN

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AUD_SPDIF_SENSE I36

50B OUT

AUD_CDC_ROUT_HP 50C IN

AUD_CDC_LOUT_HP 50C IN

NOTE :
USE 75 OHM
(202285-022)
FOR SPDIF

BOM=AUDIO
C8A12
100UF
20% 10V
ALUM
2525

BOM=AUDIO
R7A8 2
10    5%
603   CH
202285-001

BOM=AUDIO
C7B3
100UF
20% 10V
ALUM
2525

BOM=AUDIO
R7A1 2
10    5%
603   CH
202285-001

I_AUD_R7A8_1

I_AUD_R7A3_1

AUD_R_FNTOUT    OUT   53B3< 53B7<
AUD_R_RETIN     IN    53A8> 53B1>

BOM=AUDIO
FB6B1
FB

I_AUD_R_RETLINE

I_AUD_L_RETLINE

BOM=AUDIO
FB6A3
FB

AUD_L_RETIN    IN    53A8> 53B1>
AUD_L_FNTOUT   OUT   53B3> 53B7<

ALL AUDIO CON GND PINS SHOULD BE NO-SHAPE-CONNECT

LINE, MIDDLE
STEREO
LINE OUT

BOM=AUDIO
A06125-001
J6A2
3 STACK AUDIOJACK

25
24
23
22
1

JACK

JACKSHIELD              OUT   53C1> 53CB> 52A8<
I_AUD_L_GWSPK          OUT   54AB<
I_AUD_R_GWSPK          OUT   54AB<

BOM=AUDIO
R7A3
470
5%
CH
603

BOM=AUDIO
R7A10
470
5%
CH
603

BOM=AUDIO
C5A11
100PF
50V
X7R
603

BOM=AUDIO
C5A8
100PF
50V
X7R
603

AUD_SPDIF_OUT 50C IN

BOM=AUD_SPDIF
C7A2
4700PF 20%
50V
EMPTY
603

BOM=AUD_SPDIF
R7A2 2
330   5%
603   EMPTY

BOM=AUD_SPDIF
C9A23
470PF
50V
EMPTY
603

CUSTOM INTERNAL SPEAKER HEADER

VCC

BOM=AUDIO_GW
650287-001
J6A1
1X4HDR_ANCH

I_AUD_R_GWSPK 54C IN
I_AUD_L_GWSPK 54C IN

4
3
2
1

EMPTY

BOM=AUDIO_GW
C5A15
470PF
50V
EMPTY
603

BOM=AUDIO_GW
C5A16
470PF
50V
EMPTY
603

BOM=AUDIO_GW
C5A14
1UF
20%
EMPTY
603

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

ROUTE AWAY FROM NOISE

40C2< 40B2< 39D3< 36B2< 35B1< 35A8< 26D8< 26D2< 9D7< 39A4>
62D2< 49B8< 48B7< 47B8< 46C7< 44D4< 43D2< 43B6<

IN  V_5P0_STBY

BOM=AUDIO
1
R9A2
0
1A
CH
603
2

BOM=AUDIO
1  201005-018
L9A1
27UH
EMPTY
2

CURRENT DRAW 50 MA

V_5P0_AUD_ANALOG  OUT

50A8< 50C1< 53B1< 53D1<

BOM=AUDIO
1
C9A16
1UF
20V
25V
603
2

BOM=AUDIO
1
C9A7
10UF
10V
10V
25V
603
2

BOM=AUDIO
1  C9A21
+  10UF
10V
TBD
ALUM
2  4MM

AUDIO VOLTAGE REGULATOR

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| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

ALWAYS STUFFED

LAN SKU ONLY

IN V_3P3_STBY

P_SDONE BI 27B7<> 30B6<>
56C1<>

P_SB0* BI 27B7<> 30B6<>
56C1<>

1 BOM=SMBUS  1 BOM=SMBUS
R8F12      R8F11
5;7K       5;7K
CH         CH
2 603      2 603

LAN AND CNR SKUS

1 BOM=LAN  1 BOM=LAN
R8D1       R8F4
2;7K       5;
5%         5%
CH         CH
2 603      2 603

21A PIN ICH_SMIB_CLK

BOM=CNR_LAN
1 R8D6 2
0      1A
603    CH

1 BOM=PCI2_NO_SMBUS
R8D9 1 BOM=PCI2_NO_SMBUS
0     R8D12
1A    0
EMPTY 1A
2 603 EMPTY
      2 603

NOTE : STUFF THESE RESISTORS
FOR NO SMBUS SUPPORT
TO PCI SLOT 2

21A BI ICH_SMIB_DATA

BOM=CNR_LAN
1 R8F10 2
0       1A
603     CH

41C PIN ICH_SMB_CLK_AUX

BOM=PCI2_SMBUS
1 R8D2 2
0      1A
603    CH

ICH_SMB_CLK_PCISLOT2 OUT 28B7<>

41C BI ICH_SMB_DATA_AUX

BOM=PCI2_SMBUS
1 R8D8 2
0      1A
603    CH

ICH_SMB_DATA_PCISLOT2 BI 28B7<>

PCI CONN

+12V

P_SDONE BI 27B7<> 30B6<>
56D1<>

P_SB0* BI 27B7<> 30B6<>
56D1<>

1 BOM=SMBUS
R9E7
5;7K
CH
2 603

3 BOM=SMBUS
Q8F1
FET
2 201924-001

I_PWRGD_PS_BUFF_OC_R

1 BOM=PCI3_NO_SMBUS
R8D11  1 BOM=PCI3_NO_SMBUS
0      R8D14
1A     0
CH     1A
2 603  CH
       2 603

NOTE : STUFF THESE RESISTORS
FOR NO SMBUS SUPPORT
TO PCI SLOT 3

40A PIN PWRGD_PS_BUF

BOM=SMBUS
1 R9E8 2
10K 5%
603 CH

3 BOM=SMBUS
Q8F2
FET
2 201924-001

VCC3

1 BOM=SMBUS  1 BOM=SMBUS
R9C3         R9C4
2;7K         2;7K
5%           5%
CH           CH
2 603        2 603

BOM=PCI3_SMBUS
1 R8D10 2
0       1A
603 EMPTY CH

ICH_SMB_CLK_PCISLOT3 OUT 29B7<>

BOM=PCI3_SMBUS
1 R8D13 2
0       1A
603 EMPTY CH

ICH_SMB_DATA_PCISLOT3 BI 29B7<>

PCI CONN

15B4< 57B7<> 21C6<> 3D7<>
16B7<> 15B8<

IN ICH_SMB_CLK

16B7<> 15B8< 15B4<
3C7< 57B2<> 21C6<>

BI ICH_SMB_DATA

SMBUS ISOLATION
BLOCK DIAGRAM

P_SDONE/
P_SB0*

ICH_SMB_CLK_PCISLOT
ICH_SMB_DATA_PCISLOT

ICH_SMB_CLK_AUX
ICH_SMB_DATA_AUX

HECETA 4

ICH_SMIB_CLK
ICH_SMIB_DATA

POWERGD_PS ISOLATION

CLOCK

DIMM0
DIMM1
DIMM2

ICH2

ICH_SMB_CLK
ICH_SMB_DATA

NOTE : FOR SMBUS SUPPORT TO ALL PCI SLOTS,
STUFF COMPONENTS WITH BOM PROPERTY OF
PCI3_SMBUS, WITHOUT UNSTUFFING COMPONENTS
WITH BOM PROPERTY OF PCI3_NO_SMBUS.
NEED TO UNSTUFF PULL-UPS AT PAGE 34.

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ALL USB PAIRS MUST BE ROUTED AS DIFFERENTIAL PAIRS
7.5 / 7.5 / 7.5, AND 10 TO 12 MILS TO ALL OTHERS

+12V
VCC
VCC3

BOM=CNR
750073-002
J9B1
CNR60

| B1 | RESERVED | RESERVED | A1 |
| B2 | RESERVED | RESERVED | A2 |
| B3 | RESERVED | GND | A3 |
| B4 | GND | RESERVED | A4 |
| B5 | RESERVED | RESERVED | A5 |
| B6 | RESERVED | GND | A6 |
| B7 | GND | LAN_TXD2 | A7 |
| B8 | LAN_TXD1 | LAN_TXD0 | A8 |
| B9 | LAN_RSTSYNC | GND | A9 |
| B10 | GND | LAN_CLK | A10 |
| B11 | LAN_RXD2 | LAN_RXD1 | A11 |
| B12 | LAN_RXD0 | RESERVED | A12 |
| B13 | GND | USB+ | A13 |
| B14 | RESERVED | GND | A14 |
| B15 | +5VDUAL | USB- | A15 |
| B16 | USB_OC | GND | A16 |
| B17 | GND | +12V | A17 |
| B18 | -12V | +3.3VDUAL | A18 |
| B19 | +3.3VD | +5VD | A19 |
| B20 | GND | GND | A20 |
| B21 | EEDO | EEDI | A21 |
| B22 | EECK | RESERVED | A22 |
| B23 | GND | SMB_A1 | A23 |
| B24 | SMB_A0 | SMB_A2 | A24 |
| B25 | SMB_SCL | SMB_SDA | A25 |
| B26 | CDC_DWN_ENAB | AC97_RESET | A26 |
| B27 | RESERVED | RESERVED | A27 |
| B28 | AC97_SYNC | AC97_SDATA_IN1 | A28 |
| B29 | AC97_SDATA_OUT | AC97_SDATA_IN0 | A29 |
| B30 | AC97_BITCLK | GND | A30 |

EMPTY
-12V

NC_CNR_B1
NC_CNR_B2
NC_CNR_B3
NC_CNR_B5
NC_CNR_B6
58C2 IN   ICH2_LAN_TXD1_CNR
58B2 IN   ICH2_LAN_RST_CNR
58B2 OUT  ICH2_LAN_RXD2_CNR
58B2 OUT  ICH2_LAN_RXD0_CNR
NC_CNR_B14

NC_CNR_A1
NC_CNR_A2
NC_CNR_A4
NC_CNR_A5
ICH2_LAN_TXD2_CNR   IN 58C2
ICH2_LAN_TXD0_CNR   IN 58C2
ICH2_LAN_CLK_CNR    OUT 58B2
ICH2_LAN_RXD1_CNR   OUT 58B2
NC_CNR_A12
ICH_USB_P1_CNR      BI 25D8
ICH_USB_P1_CNR*     BI 25D8

47B4 26C2 IN  V_5P0_STBY_FPUSB_CNR
47C7
47A OUT   CNR_OC*

V_3P3_PCIAUX   IN
4BC1 17B4 27D8 28D8 29D7
62B8

BOM=CNR
C9B16
47UF
10%
EMPTY
I206

58D OUT   ICH2_EE_DIN_CNR
58D IN    ICH2_EE_CLK_CNR

ICH2_EE_DOUT_CNR   OUT 58D4
ICH2_EE_CS_CNR     IN 58D4

56B7 16B7 15B8 15B4 21C6 3D7  BI  ICH_SMB_CLK
ICH_SMB_DATA   BI   15B4 15B8 16B7 21C6 56B7 3C7

58D IN   AUD_LINK_SYNC_ICH_CNR
58D IN   AUD_LINK_SDO_ICH_CNR
58D OUT  AUD_LINK_BCLK_ICH_CNR

NC_CNR_A27
AUD_LINK_SDI1_ICH      OUT 21B8
AUD_LINK_SDI0_ICH_CNR  OUT 58D5

VCC3

| 1 R9D2 | 1 R9D4 | 1 R9D3 |
| BOM=CNR | BOM=CNR | BOM=CNR |
| 10K | 10K | 10K |
| 5% | 5% | 5% |
| EMPTY | EMPTY | EMPTY |
| 2 603 | 2 603 | 2 603 |

| 1 R9D5 | 1 R9D6 | 1 R9D7 |
| BOM=CNR | BOM=CNR | BOM=CNR |
| 10K | 10K | 10K |
| 5% | 5% | 5% |
| EMPTY | EMPTY | EMPTY |
| 2 603 | 603 | 2 603 |

PN_CNR_SMB_A0
PN_CNR_SMB_A1
PN_CNR_SMB_A2

CONNECT VCC FOR NAND
GATES TO A STANDBY SUPPLY.

BOM=CNR
676294-102
VCC=V_3P3_STBY
U9D2-CDC_DWN_ENAB
74LVC00A

BOM=CNR
VCC=V_3P3_STBY
U9D2
74LVC00A

BOM=CNR
VCC=V_3P3_STBY
U9D2
74LVC00A

| 1 R9D18 |
| BOM=CNR |
| 10K |
| 5% |
| EMPTY |
| 603 |

EMPTY
VCC3=14
GND=7

AUD_LINK_RST
VCC3=14
GND=7

VCC3=14
GND=7

STUFF FOR CNR AND CODEC DOWN

50D8 21B7 IN   AUD_LINK_RST*
20A OUT   CDC_DWN_ENAB*
50D OUT   CDC_DWN_RST*

THESE REFDES WILL CHANGE ON EASTON2.

COMM. NETWORKING RISER

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AUD_LINK_SYNC_ICH 21B PIN
RP9D1
BOM=CNR
8  0  5% 063W
SM  EMPTY
AUD_LINK_SYNC_ICH_CNR OUT 57B7<

AUD_LINK_SDO_ICH 21B PIN
RP9D1
BOM=CNR
7  0  5% 063W
SM  EMPTY
AUD_LINK_SDO_ICH_CNR OUT 57B7<

AUD_LINK_SDI0_ICH 21B OUT
RP9D1
5  4  0  5% 063W
SM  EMPTY
AUD_LINK_SDI0_ICH_CNR IN 57B1>

AUD_LINK_BCLK_ICH 21B OUT
RP9D1
BOM=CNR
6  3  0  5% 063W
SM  EMPTY
AUD_LINK_BCLK_ICH_CNR IN 57B7>

RP9D2
BOM=AUDIO
1  8  0  5% 063W
SM  IC
AUD_LINK_SYNC_ICH_CODEC OUT 50D8<

RP9D2
BOM=AUDIO
2  7  0  5% 063W
SM  IC
AUD_LINK_SDO_ICH_CODEC OUT 50D8<

RP9D2
BOM=AUDIO
4  5  0  5% 063W
SM  IC
AUD_LINK_SDI0_ICH_CODEC IN 50C1>

RP9D2
BOM=AUDIO
3  6  0  5% 063W
SM  IC
AUD_LINK_BCLK_ICH_CODEC IN 50D1>

## AC'97 STUFFING OPTION FOR AUDIO CODEC AND CNR

ICH2_EE_DIN_CNR 57C PIN
R9D1
BOM=CNR
108506-004
1  0  42  1A  603 EMPTY
ICH2_EE_DIN OUT 59A8> 21A6<

ICH2_EE_CLK_CNR 57C OUT
R9D1
108506-004
1  0  22  1A  603 EMPTY
ICH2_EE_CLK IN 21A6> 59A8<

ICH2_EE_DOUT_CNR 57C PIN
R9D9
BOM=CNR
108506-004
2  0  603 EMPTY
ICH2_EE_DOUT OUT 21A6> 59A8<

ICH2_EE_CS_CNR 57C OUT
R9D1
108506-004
1  0  12  1A  603 EMPTY
ICH2_EE_CS IN 21A6> 59A8<

NOTE : UNSTUFF THESE 4 RESISTORS FOR SKU WITH LAN DOWN
NOTE : UNSTUFF THESE 4 RESISTORS FOR EVAL SKU

NOTE : UNSTUFF THESE 2
R-PAKS FOR EVAL SKU

RP7E3
BOM=CNR
4  3  33  5% 063W
SM  EMPTY
ICH2_LAN_TXD0_CNR OUT 57C2<

RP7E3
BOM=CNR
2  7  33  5% 063W
SM  EMPTY
ICH2_LAN_TXD1_CNR OUT 57C6<

RP7E3
BOM=CNR
3  6  33  5% 063W
SM  EMPTY
ICH2_LAN_TXD2_CNR OUT 57C2<

RP7E2
BOM=CNR
5  4  33  5% 063W
SM  EMPTY
ICH2_LAN_RXD0_CNR OUT 57C6>

RP7E3
BOM=CNR
6  3  33  5% 063W
SM  EMPTY
ICH2_LAN_RXD1_CNR OUT 57C2>

RP7E2
BOM=CNR
8  1  33  5% 063W
SM  EMPTY
ICH2_LAN_RXD2_CNR OUT 57C6>

RP7E3
BOM=CNR
1  8  33  5% 063W
SM  EMPTY
ICH2_LAN_RST_CNR OUT 57C6<

RP7E2
BOM=CNR
7  2  33  5% 063W
SM  EMPTY
ICH2_LAN_CLK_CNR OUT 57C2>

JORDAN INTERFACE STUFFING OPTION FOR CNR

ICH2_LAN_TXD0_R 20A OUT
RP7E4
BOM=LAN
5  4  33  5% 063W
SM  IC
ICH2_LAN_TXD0 IN 59C7>

ICH2_LAN_TXD1_R 20A OUT
RP7E4
BOM=LAN
7  2  33  5% 063W
SM  IC
ICH2_LAN_TXD1 IN 59C7>

ICH2_LAN_TXD2_R 20A OUT
RP7E4
BOM=LAN
6  3  33  5% 063W
SM  IC
ICH2_LAN_TXD2 IN 59C7>

ICH2_LAN_RXD0_R 20A PIN
RP7E5
BOM=LAN
8  1  33  5% 063W
SM  IC
ICH2_LAN_RXD0 OUT 59C4<

ICH2_LAN_RXD1_R 20A PIN
RP7E5
7  2  33  5% 063W
SM  IC
ICH2_LAN_RXD1 OUT 59C4<

ICH2_LAN_RXD2_R 20A PIN
RP7E4
BOM=LAN
5  4  33  5% 063W
SM  IC
ICH2_LAN_RXD2 OUT 59C4<

ICH2_LAN_RST_R 20A OUT
RP7E4
BOM=LAN
8  1  33  5% 063W
SM  IC
ICH2_LAN_RST IN 59C7>

ICH2_LAN_CLK_R 20A OUT
RP7E5
BOM=LAN
6  3  33  5% 063W
SM  IC
ICH2_LAN_CLK IN 59C7>

JORDAN INTERFACE STUFFING OPTION FOR LAN

## THESE REFDES WILL CHANGE ON EASTON2.

R7B2, R7B1, R6B2, AND R6A3 ARE TUNING RESISTORS

BOM=LAN
2 R7B2 1
562    CH
603    1%

BOM=LAN
VCC=V_3P3_STBY
750285-005
U7B1
KINNERETH

BOM=LAN
2 R7B1 1
1%    590
CH    603

| | | |
|---|---|---|
| 5BA> OUT | ICH2_LAN_CLK 39 | JCLK |
| 5BB OUT | ICH2_LAN_TXD0 43 | JTXD0 |
| 5BB OUT | ICH2_LAN_TXD1 44 | JTXD1 |
| 5BB OUT | ICH2_LAN_TXD2 45 | JTXD2 |

JRXD0 34 ICH2_LAN_RXD0 IN 5BA2>
JRXD1 35 ICH2_LAN_RXD1 IN 5BA2>
JRXD2 37 ICH2_LAN_RXD2 IN 5BA2>

BOM=LAN
R6A3
1Ω
154
1%
603

BOM=LAN
1 R6B2 1
100
1%
CH
603

BOM=USB_LAN
A14537-002
NORES
JA5A1
RJ45_MJ2

5BA OUT  ICH2_LAN_RST 42  JRESET

RBIAS10 4 I_LAN_RBIAS10
RBIAS100 5 I_LAN_RBIAS100

TP_LAN_ADV1041 41  ADV10

TDP 10 I_LAN_TDP
TDN 11 I_LAN_TDM

TXP TXC1 13
TXN TXC2 12

I_LAN_JA5A1_12

I_KIN_22 21  TESTEN

RDP 15 I_LAN_RDP
RDN 14 I_LAN_RDM

RXP RXC 15
RXN GND 16

IO

GND=21,22,23,24,25,26,27,28

5BA OUT  I_LAN_CK_X1 46  X1
5BA IN   I_LAN_CK_X2 47  X2

LILED 27 I_LAN_LILED
SPEEDLED 31 I_LAN_SPEEDLED
ACTLED 32 I_LAN_ACT_LED_R

BOM=USB_LAN
NORES
JA5A1
YLW_LED

BOM=USB_LAN
NORES
JA5A1
GRN_LED

IN  V_3P3_STBY 1
BOM=LAN
R6A22
0    1A
603  CH

I_KIN_VCC_19

VCC 19
VCC 23

TOUT 26 PD_LAN_TOUT26
ISOL_TI 29 I_ISO_TI
ISOL_TEX 28 I_ISO_TEX
ISOL_TCK 30 I_ISO_TCK

BOM=LAN
1 R7A162
10K
603  EMPTY

19  20
IO

18  17
IO

V_3P3_STBY IN

BOM=LAN
L6A1 4.7UH
EMPTY
721891-008

IC

MUST BE RIGHT BY PINS

I_KINNERETH_DISABLE

* GPIO_LAN_ENABLE DEFAULT TO 1

IN  V_3P3_STBY

BOM=LAN
C7B4
1UF
603

VCC=V_3P3_STBY
U9D1
AT93C46A_66
109868-001

| | | |
|---|---|---|
| 5BD1> 21A6> IN | ICH2_EE_DOUT 3 | DI |
| 5BD1< 21A6< | ICH2_EE_CS 1 | CS |
| 5BD1< 21A6< | ICH2_EE_CLK 2 | SK |

DO 4
NC5 6 TP_LAN_6

VCC=8
GND=5
21A6< 58D1> OUT  ICH2_EE_DIN  NC=7

NOTE : PRE-PROGRAMMED EEPROM #A05441-002
FOR ATE PROGRAMMED, USE #A07262-002

SPARE
RP7A1
100  5% 063W
SM   IC

BOM=LAN
Q7A3
MMBT3904
XSTR
108969-001

BOM=LAN
1 R7A152
10K
CH
603

GPIO_LAN_ENABLE IN  20A7> 21C6<

BOM=CORE_ICH2
R8F7
10K
5%
CH
603

NOTE : IN FAB A, THIS FAN2 WAS NAMED FAN1

+12V    +12V

FAN 2          CHASSIS FAN

CAP MUST BE NEXT TO FAN CONN

NOTE : IN FAB A, THIS FAN3 WAS NAMED FAN2

+12V

FAN 3          ADDITIONAL STANDARD FAN

+12V

NOTE : IN FAB A, THIS FAN1 WAS NAMED FAN3

CAP MUST BE NEXT TO FAN CONN

FAN 1          CPU FAN

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## VCC ADDITIONAL DECOUPLING

IN VTT

9C5< 8B7< 8A4< 7C4< 7B2< 7A8< 6D1< 43C1<
45DB< 43B8< 13D2< 9D8<

VCC   VCC   VCC

VCC3

## LAN DECOUPLING

V_3P3_STBY   IN

46C7< 47A4< 47D7< 48B7< 48C7< 56D8<
39A7< 32D8< 39B3< 39D4< 39C8< 39D3<
49B3< 8B4< 20AB< 20B1< 20BB< 20C1<
21A1< 22C3< 22C7< 27D8< 28D8< 32A1<
40A7< 40C2< 40D2< 41D6< 41A6<
48B7< 40D7< 40C2< 40D2< 41D6< 43A6<
59B1< 59B2< 59B7< 59C8< 61B2< 62C2<

## POWER CONNECTOR DECOUPLING

VCC   VCC3   +12V

-12V

## DIMM DECOUPLING

46B2<
15C8<
14B1<
46C2<
12B2<
15B7<
48D4<
62C4<

IN   V_3P3_STR

## GENERIC

VCC3   VCC

## EXTRA DECOUPLING

22D7< 22C3<
19C8< 14BB<
11D1< 44C1<
14A7< 13B1<
20C1<
62D4<

VCC3

IN   V_1P85

## SIO DECOUPLING

32A1< 28D8< 27D8< 22C7<
20B1< 20A8< 8B4< 49B3<
22C3< 21A1< 20C1< 20BB<
39D4< 39B3< 32B< 32A7<
40A2< 40A7< 39D3< 39C8<
43A6< 41D6< 40D2< 40C2<
48B7< 40D7< 47A4< 46C7<
59B2< 59B1< 56D8< 48C7<
62C2< 61D4< 59C8< 59B7<

VCC3

IN   V_3P3_STBY

*PLACE NEAR SIO
PINS 113,122,18

VCC

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PCI_CONN DECOUPLING

+12V
BOM=CORE_PCI
C9C1
.1UF 20%
65V
603

BOM=CORE_PCI
C8BB
.1UF 20%
65V
603

BOM=CORE_PCI
C3H5
22UF
25V 20%
RDL
ELEC

BOM=CORE_PCI
C7B9
.1UF 20%
65V
603

BOM=CORE_PCI
C7C4
.1UF 20%
EMPTY
603

-12V
BOM=CORE_PCI
C9B7
.1UF 20%
65V
603

BOM=CORE_PCI
C8B6
.1UF 20%
65V
603

BOM=CORE_PCI
C8B7
22UF
25V 20%
ELEC
RDL

BOM=CORE_PCI
C7B8
.1UF 20%
65V
603

V_3P3_PCIAUX
29D7<
17B4<  48C1<
28D8<  27D8<
       57C2<

BOM=CORE_PCI
C8C2
.1UF 20%
65V
603

BOM=CORE_PCI
C7C1
22UF
25V 20%
ELEC
RDL

BOM=CORE_PCI
C7C2
.1UF 20%
65V
603

VCC
BOM=CORE_PCI
C3A13
.1UF 20%
65V
603

BOM=CORE_PCI
C7E2
.1UF 20%
65V
603

BOM=CORE_PCI
C3H7
.1UF 20%
65V
603

BOM=CORE_PCI
C9E3
.1UF 20%
65V
603

BOM=CORE_PCI
C8E2
.1UF 20%
65V
603

BOM=CORE_PCI
C8E3
.1UF 20%
65V
603

BOM=CORE_PCI
C8B9
.1UF 20%
65V
603

BOM=CORE_PCI
C3H9
.1UF 20%
65V
603

BOM=CORE_PCI
C8H3
.1UF 20%
65V
603

BOM=CORE_PCI
C8C1
22UF
25V 20%
ELEC
RDL

BOM=CORE_PCI
C9F2
100UF
25V 20%
EMPTY
RDL

VCC3
BOM=CORE_PCI
C7F10
.1UF 20%
65V
603

BOM=CORE_PCI
C9E1
.1UF 20%
65V
603

BOM=CORE_PCI
C2G10
.1UF 20%
65V
603

BOM=CORE_PCI
C9G8
.1UF 20%
65V
603

BOM=CORE_PCI
CBD2
.1UF 20%
65V
603

BOM=CORE_PCI
C7C7
.1UF 20%
65V
603

BOM=CORE_PCI
C8C6
100UF
25V 20%
ELEC
RDL

BOM=CORE_PCI
C7D6
.1UF 20%
65V
603

BOM=CORE_PCI
C7D7
.1UF 20%
65V
603

BOM=CORE_PCI
C7D2
.1UF 20%
65V
603

BOM=CORE_PCI
C8E1
.1UF 20%
65V
603

BOM=CORE_PCI
C8D1
100UF
25V 20%
EMPTY
RDL

## STITCH CAPS

V_1P85
22D7< 22C3< 20C1<
13B1< 11D1< 44C1<
19C8< 14B6< 14A7<
61A4<

BOM=CORE
C6E7
470PF 10%
90V
EMPTY

BOM=CORE
C7F4
470PF 10%
90V
EMPTY

BOM=CORE
C6F2
470PF 10%
90V
603

VCC3    VCC
BOM=CORE
C8H11
.1UF 20%
65V
603

V_3P3_STRL
61B8<
46B2<
15C6<
14B1<
46C2<
12B2<
15B5<
16B7<
48D4<

BOM=CORE
C6F3
470PF 10%
90V
603

## STANDBY DECOUPLING

V_5P0_STBY
46C7< 44D4< 43D2< 43B6< 40C2<
9SA8< 2SD8< 2SD2< 9D7< 9SA4<
40B2< 39D3< 36B2< 9SB1<
55C5< 49B8< 4BB7< 47B8<

BOM=CORE_GLUE4
C2B2
470PF 10%
90V
603

BOM=CORE_SIO
C3H2
470PF 10%
87V
603

V_3P3_STBY
61D4< 61B2< 59C8< 59B7<
4BB7< 47D7< 47A4< 46C7<
40B2< 40A7< 39D3< 39C8<
32A1< 2BD8< 27D8< 22C7<
20B1< 20A8< 8B4< 49B3<
22C3< 21A1< 20C1< 20B8<
38D4< 36B3< 33D2< 32A7<
43A8< 41D6< 40D2< 40C2<
59B2< 59B1< 56D8< 48C7<

BOM=CORE_GLUE4
C3C2
.1UF 20%
65V
603

BOM=CORE
C3G8
1.0UF 10%
10V
603

BOM=VREG_STR
C4H2
1.0UF 10%
EMPTY
603

## FWH DECOUPLING

VCC3
BOM=CORE_FWH
C8C5
.1UF 20%
65V
603

BOM=CORE_FWH
C8G11
.1UF 20%
65V
603

BOM=CORE_FWH
C9G6
.1UF 20%
65V
603

## MISC DECOUPLING

VCC
BOM=CORE
C8C3
.1UF 20%
65V
603

BOM=CORE
C8E4
10UF
20% 16V
ALUM
4MM

BOM=202341-002
C4C4
.1UF 20%
EMPTY
603

VCC3
BOM=CORE_SIO
C7G1
.1UF 20%
65V
603

BOM=CORE
C3G6
470PF 10%
EMPTY
603

BOM=CORE
C3H1
470PF 10%
65V
603

BOM=CORE
C2H21
.1UF 20%
EMPTY
603

VCC
BOM=CNR
C9F12
1UF
20%
16V
603

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

# MOUNTING HOLES

## TEST SITE

BOM=MTG_HOLE
MH7A1
MTG_HOLE
| NC9 | 9 NC_MH1 |
EMPTY
GND=1,2,3,4,5,6,7,8

BOM=MTG_HOLE
MH7G1
MTG_HOLE
| NC9 | 9 NC_MH3 |
EMPTY
GND=1,2,3,4,5,6,7,8

BOM=MTG_HOLE
MH9G1
MTG_HOLE
| NC9 | 9 NC_MH5 |
EMPTY
GND=1,2,3,4,5,6,7,8

MH8A1
MTG_HOLE
| NC9 | 9 NC_MH2 |
EMPTY
GND=1,2,3,4,5,6,7,8
BOM=MTG_HOLE

MH1G1
MTG_HOLE
| NC9 | 9 NC_MH4 |
EMPTY
GND=1,2,3,4,5,6,7,8
BOM=MTG_HOLE

MH1B1
MTG_HOLE
| NC9 | 9 NC_MH6 |
EMPTY
GND=1,2,3,4,5,6,7,8
BOM=MTG_HOLE

TP_ATE_1

1 BOM=ATE
C7G9
15PF
50V
N50
603
2

TP_ATE_2

TP_ATE_3

1 BOM=ATE
C3G5
62PF
50V
N50
603
2

TP_ATE_4

TP_ATE_5

1 BOM=ATE
C3G4
47PF
50V
N50
603
2

TP_ATE_6

TP_ATE_7

1 BOM=ATE
C7G8
10PF
50V
N50
603
2

TP_ATE_8

# DFM

4 BOM=CORE
RP9A1
10K
5%
.063W
EMPTY
5 5M

3 BOM=CORE
RP9A1
10K
5%
.063W
EMPTY
6 5M

2 BOM=CORE
RP9A1
10K
5%
.063W
EMPTY
7 5M

1 BOM=CORE
RP9A1
10K
5%
.063W
EMPTY
8 5M

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# REVISION HISTORY

REV 1.0
_____

FROZEN SCHEMATIC TAPEOUT ON 10-22-01

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