AP-933

APPLICATION NOTE

Flexible Motherboard Power Distribution and Control for the Pentium® III Xeon™ Processor

January 2000

Order Number 245245-002

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1. INTRODUCTION

The intent of this application note is to familiarize the reader with the power requirements of Pentium® III Xeon™ processors, and to show several simulation models and power implementation techniques. This guideline will discuss methods to allow support for all Pentium III Xeon processors including the Pentium III Xeon Processor at 600 MHz+, hence the term "Flexible Motherboard".

Only specific power distribution and control issues pertaining to Pentium III Xeon processors are discussed in this document. It is assumed the reader is familiar with power distribution issues of the Pentium® II Xeon™ processor. For a complete explanation of the detailed electrical theory assumed in this application note, please read the *Pentium® II Xeon™ Processor Power Distribution Guidelines.*

1.1 TERMINOLOGY

"Pentium III Xeon Processor at 600 MHz+", refers to Pentium III Xeon processors which utilize On Cartridge Voltage Regulator technology, or ***"OCVR"***. The OCVR regulates V_{CC_CORE} (the appropriate cartridge input voltage) to the required processor core voltage (V_{CC_CPU}). The OCVR was developed to provide the necessary regulation to guarantee the highest possible frequency of operation for the Pentium III Xeon Processor at 600 MHz+.

There are two variants of the Pentium® III Xeon™ Processor at 600 MHz+, one powered by 2.8 Volts, and one powered by either 5 or 12 Volts. The processor powered by 2.8 Volts is referenced in this document as the ***"2.8 Volt Pentium III Xeon processor"***. The processor powered by either 5 or 12 Volts is referenced in this document as the ***"5/12 Volt Pentium III Xeon processor"***. ***"Pentium III Xeon processor"*** refers to Pentium III Xeon processors specified at operating frequencies of 500 and 550 MHz.

"SC 330 processor" refers to the Pentium II Xeon processor, Pentium III Xeon processor, or Pentium III Xeon Processor at 600 MHz+. ***"SC 330.1"*** refers to the added cartridge pin functionality of the Pentium III Xeon Processor at 600 MHz+. The SC 330.1 interface is an electrical enhancement of the SC 330 interface, and supports up to four processors utilizing a 100 MHz system bus, or up to two processors utilizing a 133MHz system bus. The SC 330.1 interface adds the required flexibility to accommodate control and monitoring signals for the OCVR.

"Power-Good" or ***"PWRGOOD"*** is an active high signal that indicates that all of the system clocks and voltage supplies are stable. PWRGOOD should be asserted at a predetermined time after system voltages are stable, and should be de-asserted as soon as any of these voltages fail their specifications. The time constant should be set such that all clocks and other supply levels have reached a stable condition before PWRGOOD is asserted. The PWRGOOD signal(s) from onboard VRM(s) are sometimes used to generate a system-wide PWRGOOD signal. If this is the case, the VRM must continue to assert PWRGOOD even when the VID bits instruct the VRM to disable its output. The VRM providing voltage to the L2 of the Pentium III Xeon Processor at 600 MHz+ will encounter this situation (see Section 3.3).

"V_{CC_L2}" refers to the Pentium III Xeon processor's L2 cache supply voltage. ***"V_{CC_CORE}"*** and ***"AGTL+"*** refer to the SC 330 processor core's V_{CC} and Assisted Gunning Transceiver Logic+ supply voltage. V_{CC_CORE} for the Pentium III Xeon Processor at 600 MHz+ also supplies the L2 cache voltage, since the L2 is integrated into the processor's core. "AGTL+" is the bus between the processor and its chipset. The terms "AGTL+ bus" and "System Bus" are synonymous.

"Flexible Motherboard" refers to a motherboard that supports any SC 330 processor, and implements a Voltage Regulation Module (VRM).

"Pentium III Xeon Processor at 600 MHz+ only", refers to a system design that supports only Pentium III Xeon Processors at 600 MHz+. It likely powers the processors from the 5 or 12 Volt system power supply output, and does not require VRM(s). This design is not compatible with other SC 330 processors.

1.2 REFERENCES

This document contains references to the following documents:

- *AP-828, Pentium® II Xeon™ Processor Power Distribution Guidelines, order number 243772* http://developer.intel.com/design/pentiumii/xeon/applnots.
- *Pentium® II Xeon™ Processor at 400 and 450 MHz, order number 243770* http://developer.intel.com/design/pentiumii/xeon/datashts.
- *Pentium® III Xeon™ Processor at 500 and 550 MHz, order number 245094*
- http://developer.intel.com/design/pentiumiii/xeon/datashts.
- *Pentium® III Xeon™ Processor at 600, 667, 733 and 800 MHz, order number 245305* http://developer.intel.com/design/pentiumiii/xeon/datashts.
- *Pentium® III Xeon™ Processor Bus Terminator Design Guidelines, order number 245149* http://developer.intel.com/design/pentiumii/xeon/designgd/index.htm.
- *VRM 8.3 DC-DC Converter Design Guidelines, order number 243870* http://developer.intel.com/design/pentiumii/xeon/designgd/index.htm.

2. TYPICAL POWER DISTRIBUTION

Power distribution is generally thought of as *supplying power to the components that require it*. Printed circuit board (PCB) designers attempt to create an ideal power supply with power planes within the PCB or by using large width traces to distribute power. High frequency noise, created when high-speed logic gates switch, is typically controlled with high frequency ceramic capacitors, which are recharged from lower frequency bulk capacitors. Various *rule of thumb* methods exist for determining the amount of each type of capacitance that is required. The system designer needs to design beyond the rule of thumb and architect a power distribution system that meets processor specifications.

Figure 1 shows the ideal power model. However, a more realistic power distribution scheme is shown in Figures 2 and 3.

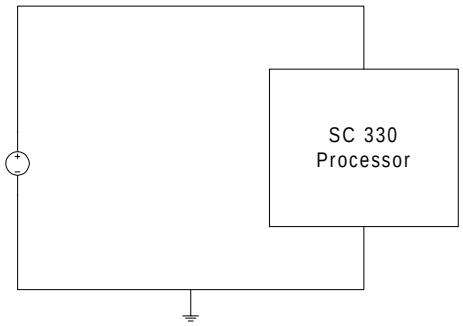

Figure 1. Ideal SC 330 Processor Power Supply Scheme

Note that in an SC 330 processor-based system, there is a "built-in" capability to support up to four processors on the system bus. Figure 2 shows the recommended flexible motherboard solution using local voltage regulator modules.

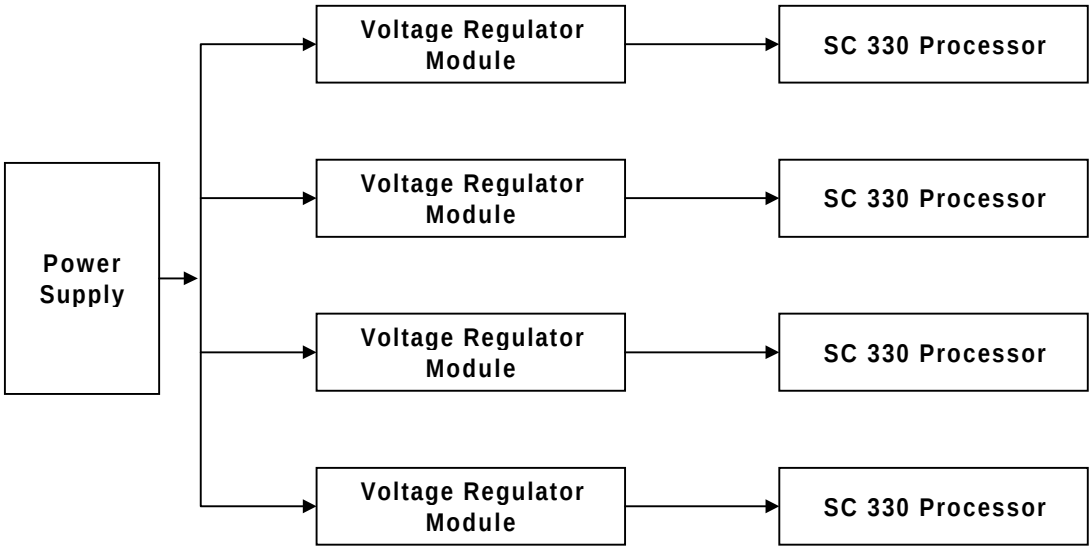

Figure 2. Power Distribution of a Flexible Motherboard System

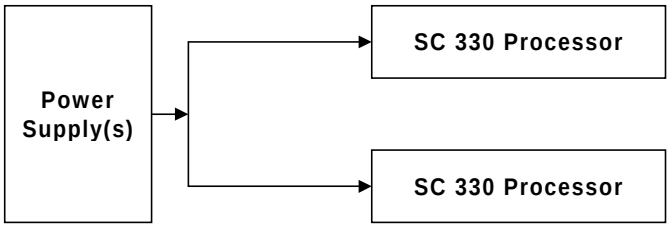

Figure 3. Power Distribution of Pentium III Xeon Processor at 600 MHz+-only System

To completely model the flexible motherboard system, one must include the inductance and resistance from the cables, connectors, PCB, the pins and body of components (such as resistors and capacitors), and the edge fingers and contacts of the processor and voltage regulator module. To model the Pentium III Xeon Processor at 600 MHz+-only system, the Voltage Regulator section is removed. A detailed model showing these effects is provided in Figures 4 and 5.

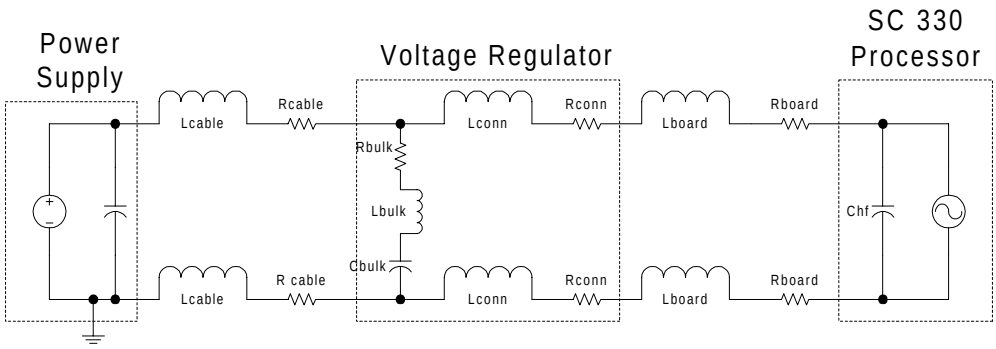

Figure 4. Detailed Power Distribution Model for Flexible System

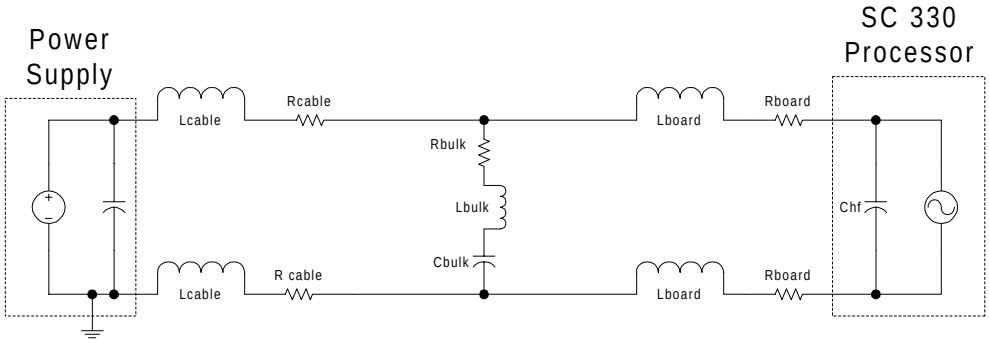

Figure 5. Detailed Power Distribution Model for Pentium III Xeon Processor at 600 MHz+-only System

3. PROCESSOR POWER REQUIREMENTS

This section describes the issues related to supplying power to the processor. Refer to the Pentium II Xeon processor datasheet, and the Pentium III Xeon processor datasheet for detailed electrical specifications.

The Pentium III Xeon Processor at 600 MHz+ typically operates on +2.8V for flexible motherboard designs, and +5V or +12V for Pentium III Xeon Processor at 600 MHz+-only motherboard designs. All other SC 330 processor cores typically operate on 2.0V and require a separate power supply for the L2 cache.

SC 330 processors allow the use of Auto HALT, Stop-Grant and Sleep states to reduce power consumption. This is accomplished by stopping the clock to specific internal sections of the processor, depending on each particular state. There is no Deep Sleep State on SC 330 processors.

A recommended termination for the AGTL+ bus is shown in the Figure 6. All AGTL+ bus lines should be terminated to the V_{TT} supply through 150-ohm resistors. Any unused processor slots must be terminated using System Bus Termination cards. This bus implementation allows up to 6 loads and may be run at speeds up to 100 MHz. The *Pentium® III Xeon™ Processor Bus Terminator Design Guidelines* document describes termination card design requirements.

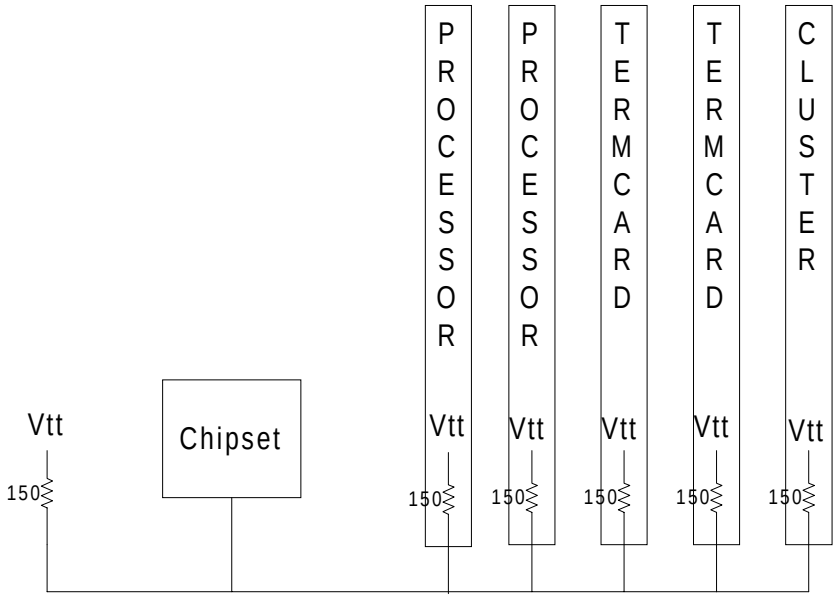

Figure 6. AGTL+ Bus Termination Layout

3.1 VOLTAGE TOLERANCE

SC 330 processors with the exception of the 5/12 Volt Pentium III Xeon processor require ±85 mV static (including noise & ripple) tolerance and a ±130 mV transient tolerance at the connector edge fingers. Failure to meet these specifications on the low-end tolerance results in transistor slow down, and the processor not meeting timing specifications. Not meeting the specifications on the high-end tolerance can induce electro-migration, causing damage or reducing the life of the processor.

3.2 MULTIPLE VOLTAGES

The VRM 8.3 module, which may provide the V_{CC_CORE} supply voltage to SC 330 processors, has the capability of supplying voltages from +1.8V to +2.8V. The typical Pentium III Xeon processor V_{CC_CORE} is 2V. Similarly, the VRM 8.3 module, which provides V_{CC_L2} supply to the Pentium III Xeon processor L2 caches, has the capability of supplying voltages from +1.8V to +2.8V. The typical Pentium III Xeon processor V_{CC_L2} is 2.0 or 2.7V.

The external voltage source, which provides the V_{CC_CORE} supply voltage to the Pentium III Xeon Processor at 600 MHz+, must supply one of three voltages to the V_{CC_CORE} pins (+2.8V, +5V, or +12V). The V_{CC_CORE} supply to the Pentium III Xeon Processor at 600 MHz+ is used as the input voltage to the processor's OCVR. The V_{CC_CPU} output from the OCVR then powers the Pentium III Xeon Processor at 600 MHz+ core and integrated L2 cache. The V_{CC_L2} pins of the Pentium III Xeon Processor at 600 MHz+ are not connected on the cartridge substrate, and therefore may be left floating at the processor cartridge connector.

The VRM 8.3 module can provide adequate power for all planned core frequencies of the 133 MHz system bus 2.8 Volt Pentium III Xeon processors. 5/12 Volt Pentium III Xeon processors are intended for use in systems that do not require Pentium III Xeon processor compatibility, and are powered directly from a +5V or +12V system power source. Reference Table 5 and/or the *VRM 8.3 DC-DC Converter Design Guidelines* document for available voltage details.

Figure 7 shows the Pentium III Xeon processor cartridge, with its processor core and L2 cache component(s). The typical voltages required are: V_{CC_CORE} = 2.0V, V_{CC_L2} = 2.0V or 2.7V, V_{TT} = 1.5V, V_{CC_TAP} = +2.5V and V_{CC_SM} = +3.3V.

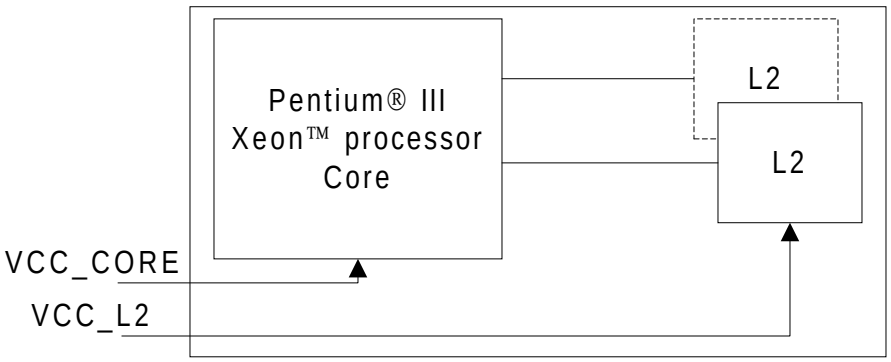

Figure 7. Pentium® III Xeon™ processor Cartridge Block Diagram

Figure 8 shows a Pentium III Xeon Processor at 600 MHz+ cartridge, with its processor core and on-die L2 cache. The 133 MHz system bus version of the Pentium III Xeon Processor at 600 MHz+ is limited to a two processor configuration, and is available in either a 2.8 Volt version or a 5/12 Volt version. 2.8 Volt Pentium III Xeon processors are intended for use in systems that also support Pentium III Xeon processors (generally employing a VRM 8.3 compliant regulator). 5/12 Volt Pentium III Xeon processors are intended to be powered directly from a system power supply, eliminating the need for VRM(s).

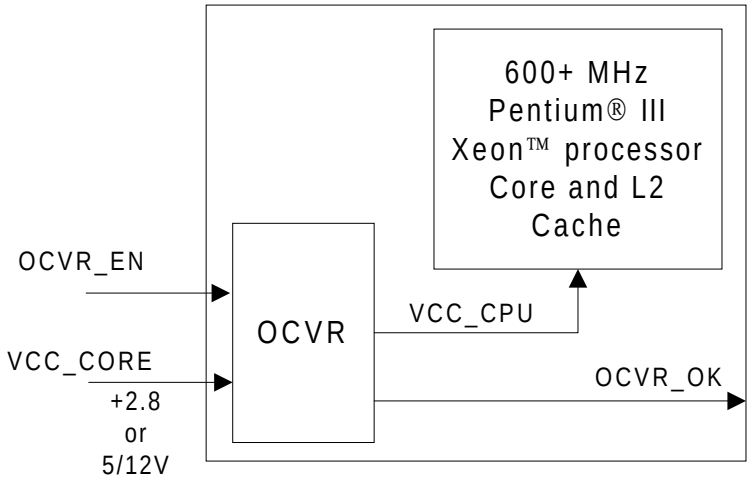

Figure 8. Pentium III Xeon Processor at 600 MHz+ Cartridge Block Diagram

Typical voltages required for a Pentium III Xeon Processor at 600 MHz+-based system are: V_{CC_CORE} = +2.8V (VRM 8.3) or either +5V or +12V (direct power supply), V_{TT} = 1.5V, V_{CC_TAP} = +2.5V and V_{CC_SM} = +3.3V.

3.3 CORE AND L2 VOLTAGE ID (VID) CODES [1]

Processor Pins[2]					V_{CC}	**CORE**[4]	**L2**[4]
VID4	**VID3**	**VID2**	**VID1**	**VID0**			
00110b - 01111b (these levels are defined in VRM 8.3)					Reserved[3]		
0	0	1	0	1	**1.80**	**x**	**x**
0	0	1	0	0	**1.85**	**x**	**x**
0	0	0	1	1	**1.90**	**x**	**x**
0	0	0	1	0	**1.95**	**x**	**x**
0	0	0	0	1	**2.00**	**x**	**x**
0	0	0	0	0	**2.05**	**x**	**x**
1	1	1	1	0	**2.1**	**x**	**x**
1	1	1	0	1	**2.2**		**x**
1	1	1	0	0	**2.3**		**x**
1	1	0	1	1	**2.4**		**x**
1	1	0	1	0	**2.5**		**x**
1	1	0	0	1	**2.6**		**x**
1	1	0	0	0	**2.7**		**x**
1	0	1	1	1	**2.8**	**x**[5]	**x**
1	0	1	1	0	2.9		
1	0	1	0	1	3.0		
1	0	1	0	0	3.1		
1	0	0	1	1	3.2		
1	0	0	1	0	3.3		
1	0	0	0	1	3.4		
1	0	0	0	0	3.5		
1	1	1	1	1	**NO CPU**	**x**[7]	**x**[6]

Table 1. Flexible Motherboard Core and L2 Identification Code

NOTES:

1. This table included as reference only. For design decisions, please refer to the latest Pentium III Xeon processor datasheet.
2. 0 = Processor pin connected to V_{SS}, 1 = Open on processor; may be pulled up to TTL V_{IH} on motherboard. See the *VRM 8.3 DC–DC Converter Design Guidelines*.
3. VRM output should be disabled for V_{CC} values less than 1.80V (these levels are defined in VRM 8.3), and for "NO CPU" selection. See section 5.3.2 for more details.
4. **x =** a required voltage that must be supported by the VRM.
5. VID_CORE pattern for 2.8 Volt Pentium III Xeon processors.
6. VID_L2 pattern for Pentium III Xeon Processors at 600 MHz+, since its L2 cache is integrated onto the processor core and draws power from V_{CC_CORE}.
7. VID_CORE pattern for 5/12 Volt Pentium III Xeon processors.

3.4 VOLTAGE SPECIFICATIONS

3.4.1 VOLTAGE SPECIFICATIONS FOR 133 MHZ PROCESSOR BUS SYSTEM DESIGNS[8]

Symbol	Parameter	Min	Typical	Max	Unit	Notes
V_{CC_CORE}	2.8 Volt Pentium III Xeon processor operating voltage	2.67	2.8	2.95	V	2, 3, 4
V_{CC_CORE}	5/12 Volt Pentium III Xeon processor operating voltage	4.75	5.0	5.25	V	2, 7
		11.4	12.0	12.6	V	2, 7
V_{CC_CORE} Static Tolerance	2.8 Volt Pentium III Xeon processor Static Tolerance at edge fingers	-0.085		0.085	V	6
V_{CC_CORE} Transient Tolerance	2.8 Volt Pentium III Xeon processor Transient Tolerance at edge fingers	-0.130		0.130	V	6
V_{TT}	AGTL+ bus termination voltage	1.47	1.50	1.53	V	5
V_{CC_SMBUS}	SMBus supply voltage	3.135	3.3	3.465	V	+3.3V±5%
V_{CC_TAP}	TAP supply voltage	2.375	2.50	2.625	V	+2.5V±5%

Table 2. Voltage Specifications at Processor Cartridge Pins for 133 MHz Processor Bus Designs

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. V_{CC_CORE} supplies the OCVR, which, in turn, supplies the processor core and the integrated L2 cache.
3. A variable voltage source such as a VRM should exist on systems in the event that a different voltage is required.
4. Use the Typical Voltage specification along with the Tolerance specifications to provide correct voltage regulation to the processor.
5. V_{TT} must be held to 1.5V ± 2%. This parameter is measured across the processor edge fingers. The processor cartridge connector is specified to have a pin self-inductance of 6.0 nH maximum, a pin-to-pin capacitance of 2 pF (maximum at 1 MHz), and an average contact resistance over the 6 V_{TT} pins of 15 mΩ maximum.
6. These are the tolerance requirements at the processor edge fingers of 2.8 Volt Pentium III Xeon processors, and are consistent with the VRM 8.3 Specification. The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. Voltage must return to within the static voltage specification within 100 μS after the transient event. The processor cartridge connector is specified to have a pin self-inductance of 6.0 nH maximum, a pin-to-pin capacitance of 2 pF (maximum at 1 MHz), and an average contact resistance of 15 mΩ maximum in order to function with the Intel specified voltage regulator module (VRM 8.3). Contact Intel for testing details of these parameters. Not 100% tested. Specified by design characterization.
7. The min/max specification includes all forms of voltage excursion from the nominal system DC design target.
8. This table included as reference only. For design decisions, please refer to the latest Pentium III Xeon processor datasheet.

3.4.2 VOLTAGE SPECIFICATIONS FOR 100 MHZ PROCESSOR BUS SYSTEM DESIGNS[8]

Symbol	Parameter	Min	Typical	Max	Unit	Notes
V_{CC_CORE}	Pentium® III Xeon™ processor operating voltage		1.8-2.1		V	2, 3, 4
V_{CC_CORE} Static Tolerance	Pentium® III Xeon™ processor static tolerance at edge fingers	-0.085		0.085	V	7
V_{CC_CORE} Transient Tolerance	Pentium® III Xeon™ processor transient tolerance at edge fingers	-0.130		0.130	V	7
V_{CC_L2}	V_{CC} for second level cache of Pentium® III Xeon™™ processor		1.8-2.8		V	3, 5
V_{CC_L2} Static Tolerance	Pentium® III Xeon™ processor Static Tolerance of second level cache supply	-0.085		0.085	V	7
V_{CC_L2} Transient Tolerance	Pentium® III Xeon™ processor Transient Tolerance of second level cache supply	-0.125		0.125	V	7
V_{TT}	AGTL+ bus termination voltage	1.365	1.50	1.635	V	6
V_{CC_SMBUS}	SMBus supply voltage	3.135	3.3	3.465	V	+3.3V±5%
V_{CC_TAP}	TAP supply voltage	2.375	2.50	2.625	V	+2.5V±5%

Table 3. Voltage Specifications at Processor Cartridge Pins for 100 MHz Processor Bus Designs

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. V_{CC_CORE} supplies the processor core
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
4. Use the Typical Voltage specification along with the Tolerance specifications to provide correct voltage regulation to the processor.
5. V_{CC_L2} supplies the L2 cache for Pentium® III Xeon™ processors. This parameter is measured at the processor edge fingers.
6. V_{TT} must be held to 1.5V **± 9%.** This parameter is measured across the processor edge fingers. The processor cartridge connector is specified to have a pin self-inductance of 6.0 nH maximum, a pin-to-pin capacitance of 2 pF (maximum at 1 MHz), and an average contact resistance over the 6 V_{TT} pins of 15 mΩ maximum.
7. These are the tolerance requirements **at the processor edge fingers**, and are consistent with the VRM 8.3 Specification**.** The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. Voltage must return to within the static voltage specification within 100 μS after the transient event. The processor cartridge connector is specified to have a pin self-inductance of 6.0 nH maximum, a pin-to-pin capacitance of 2 pF (maximum at 1 MHz), and an average contact resistance of 15 mΩ maximum in order to function with the Intel specified voltage regulator module (VRM 8.3). Contact Intel for testing details of these parameters. Not 100% tested. Specified by design characterization.
8. This table included as reference only. For design decisions, Refer to the latest Pentium® III Xeon™ processor datasheet for information affecting design decisions.

3.5 VOLTAGE SEQUENCING

No new voltage sequencing issues exist on the Pentium III Xeon processor. All voltage sequencing issues prevalent to Pentium II Xeon processors apply to Pentium III Xeon processors. Please reference the *Pentium® II Xeon™ Processor Power Distribution Guideline*. The OCVR circuitry of the Pentium III Xeon Processor at 600 MHz+ introduces a new voltage sequencing issue, described below.

3.5.1 PWRGOOD AND OCVR_OK

PWRGOOD should be inactive anytime that V_{CC_CORE} is invalid. ***The OCVR_OK signal is not guaranteed to be valid until 0.5 milliseconds (maximum) after Vin to the OCVR reaches 90 percent of its nominal value.*** Prior to this time, it is possible that the OCVR_OK signal may be falsely asserted high. This is because the OCVR is not yet powered, yet an on-cartridge pull-up resistor on the OCVR_OK output is tied to V_{CC_SMB}, a supply which may be valid and stable prior to power being applied to the OCVR. ***For this reason, care should be exercised in generation of a system-wide PWRGOOD which uses OCVR_OK in its derivation.*** OCVR_OK will become active a maximum of 13mS after the OCVR input voltage reaches 90% of its nominal value. Intel recommends that there be enough delay between the valid PWRGOOD (SC 330 pin A21) and the release of the RESET# signal from the chipset. Intel also recommends that the minimum PWRGOOD inactive pulse width (10 BCLKs) and the minimum RESET# pulse width (1mS) are within compliance as shown in the timing diagram below (Figure 9).

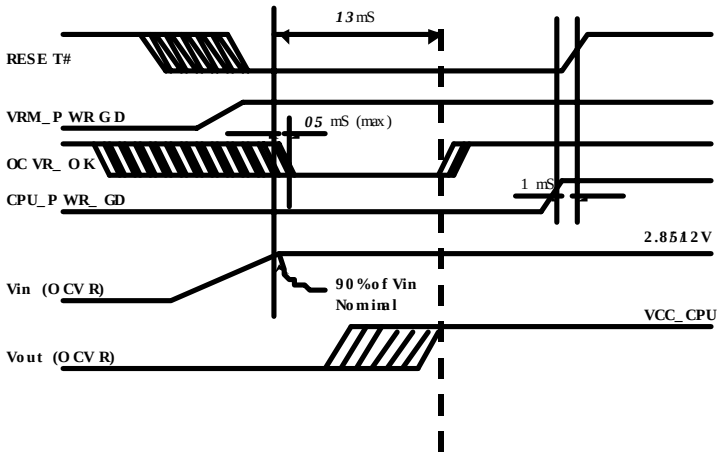

Figure 9. Timing Diagram of Power Control & processor Reset Pins

The PWRGOOD signal(s) from onboard VRM(s) may be used to generate a system-wide PWRGOOD signal. If this is the case, the VRM must continue to assert VRM_PWRGD even when the VID bits instruct the VRM to disable its output. The L2 VRM in a Pentium III Xeon Processor at 600 MHz+-based system will encounter this situation (see Section 3.3).

4. MEETING PROCESSOR POWER REQUIREMENTS

Intel recommends using local regulation (VRM 8.3 modules) for flexible motherboard designs, where support is required for all SC 330 processors. For Pentium III Xeon Processor at 600 MHz+ support only, the processor may be directly powered from the system power supply. To accommodate the differing power budgets of various system power supplies, 5/12 Volt Pentium III Xeon processors will connect directly to either +5V or +12V.

4.1 SUPPLYING POWER

In order to maintain power supply tolerance with relatively high current requirements, SC 330 processors require either local regulation or a power supply with remote sense capabilities. A DC loss occurs over the power distribution system due to the resistance of cables, power planes and connectors.

Intel recommends local regulation (the use of a supply or regulator near the load) to create the voltage needed where support for all SC 330 processors is required. For example, a local DC-to-DC converter, placed close to the load, converts a higher DC voltage to a lower DC voltage using either a linear or a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted resistive losses. More importantly, a discrete regulator regulates the voltage locally which processor voltage DC line losses by eliminating R_{CABLE} and reducing R_{BOARD}. The system designer must consider finding a representative load point that applies for all processors in a multi-processor system.

Remote sensing is recommended if the processor is powered directly from the system power supply. A power supply typically regulates the voltage at its terminals before cabling to the board. Distribution losses based on the current demand make it difficult to hold a tight tolerance at the load. A remote sense, shown in Figure 10, may solve this problem by running a separate connection from the load to the feedback loop of the power supply. The impedance of the feedback loop is quite high, and has very low current draw (in the μamp range) which significantly reduces the resistive losses described above. This allows the supply to regulate its output based on the voltage at the load and compensate for resistive losses. Remote-sense supplies suffer from added inductance due to cabling to a power supply and noise induced in the remote sense feedback signal.

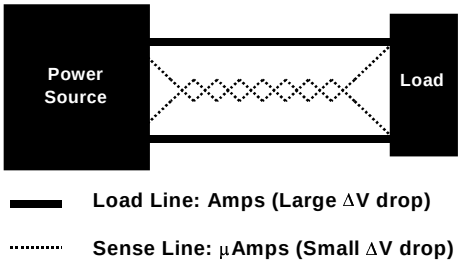

Figure 10. Remote Sense

Either method of regulation can maintain ±2% accuracy, plus a small ripple and noise budget. The large current transients of the processor means that the system designer must exercise extreme care to eliminate noise coupling and ringing when using remote sense feedback.

5. RECOMMENDATIONS

5.1 SIMULATION

Intel recommends using simulation to design and verify system design and layout. With the model of the power source, and the model of the processor provided in Section 6, system developers can begin analog modeling.

5.2 V_{CC_CORE} AND V_{CC_L2}

When designing a flexible motherboard that will accommodate any SC 330 processor, Intel recommends using a socketed local Voltage Regulator Module (VRM 8.3) DC-to-DC converter, as shown in Figure 11, for both V_{CC_CORE} and V_{CC_L2} for the Pentium III Xeon processor, and for V_{CC_CORE} for the Pentium III Xeon Processor at 600 MHz+.

The VRM design approach removes cable inductance from the distribution, and reduces board inductance. These modules should be capable of accepting 5 signals, used to indicate the voltage required by the individual processor unit. Table 1 lists the Core and L2 Voltage Identification Codes. Refer to VRM 8.3 DC-DC Converter Design Guidelines documents for actual specifications. The processor's VID_CORE and VID_L2 lines must be pulled high through 10KΩ (or greater) resistors on the motherboard. Note that the processor's V_{CC_L2} lines are "no connects" on the Pentium III Xeon Processor at 600 MHz+.

5.3 PROCESSOR UNDER/OVER VOLTAGE DAMAGE PREVENTION

To differentiate between two voltage versions of the Pentium III Xeon Processors at 600 MHz+, the HV_EN# signal (processor cartridge pin A3) is grounded on 5/12 Volt processors, and is a "no-connect" on 2.8 Volt processors. This pin is reserved (also a "no connect") on the Pentium III Xeon processor. This allows a fail-safe mechanism to prevent the risk of processor damage if the wrong voltage version is installed in a system.

5.3.1 PROCESSORS INCORRECTLY INSTALLED IN A 5/12 VOLT PENTIUM III XEON PROCESSOR SYSTEM

To prevent damage to Pentium III Xeon or 2.8 Volt Pentium III Xeon processors that might accidentally be installed in a system that only supports 5/12 Volt Pentium III Xeon processors, Intel recommends utilizing a voltage delivery mechanism as shown in Figure 13. In this example, the HV_EN# pin left floating, drives a logic '1' to the input of the inverter, which turns off the FET switch, preventing the +5 or +12 volt source from being applied to the V_{CC_CORE} pins of the Pentium III Xeon or 2.8 Volt Pentium III Xeon processor.

5.3.2 PROCESSORS INCORRECTLY INSTALLED IN A 2.8 VOLT PENTIUM III XEON PROCESSOR SYSTEM

To prevent damage to 5/12 Volt Pentium III Xeon processors that might accidentally be installed in a flexible motherboard system, the processor's VID lines will be programmed to all opens (NO CPU). By requesting “NO CPU”, the VRM 8.3 compliant delivery system turns off its output and no voltage will be applied to the processor's V_{CC_CORE} pins. See Figure 12.

Intel recommends checking with the VRM 8.3 vendor to verify that the module will not output a voltage if a reserved or invalid setting is requested. If this cannot be guaranteed, or if a custom VRM is being utilized

which is not fully VRM 8.3 compliant, Intel recommends a VRM by-pass circuit as shown in Figure 12. This circuit example allows full compatibility with all SC 330 processors.

5.4 FLEXIBLE MOTHERBOARD TOPOLOGY

The V_{CC_CORE} VRM can be used for all SC 330 processors. The V_{CC_L2} VRM is optional when using Pentium III Xeon Processors at 600 MHz+, since the cache is integrated onto the processor core; If the V_{CC_L2} VRM is present on the flexible motherboard while using the Pentium III Xeon Processor at 600 MHz+, the processor's V_{CC_L2} VID lines will program the VRM for no CPU. See Figure 11 below.

NOTE: If one V_{CC_L2} VRM is shared between two Pentium III Xeon processors, Intel recommends implementing logic on the motherboard that verifies both processors are requesting the same programmed voltage via their VID signal lines. If different voltages are being requested, then the L2 VRM must be left disabled or damage to one of the processors could occur.

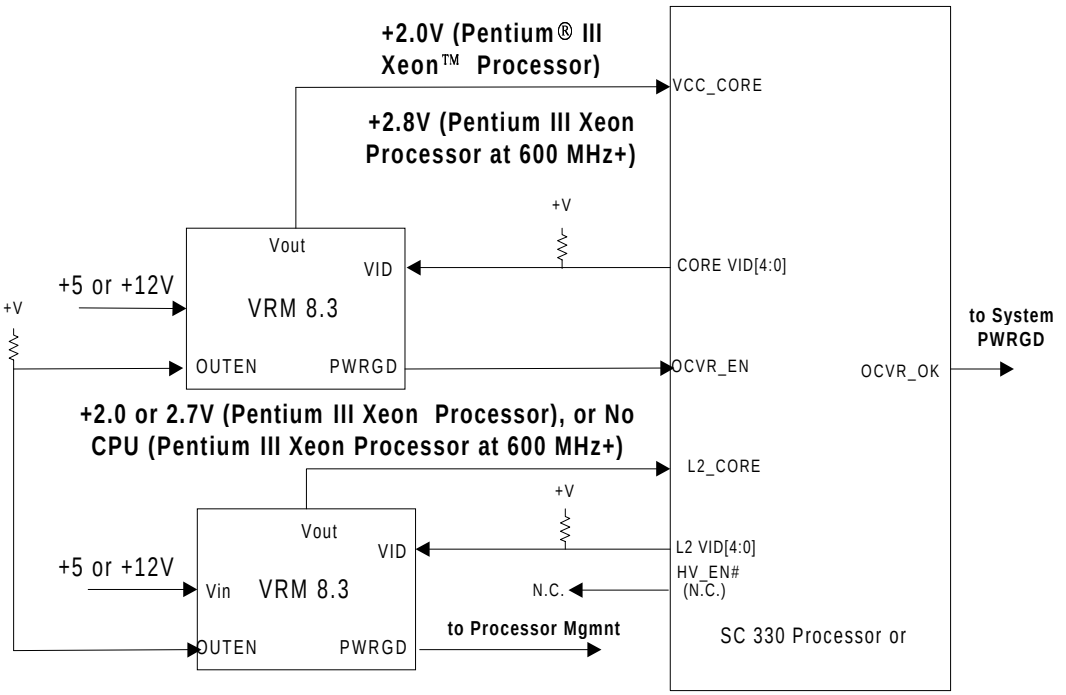

Figure 11. Flexible motherboard VRM configuration

5.5 FLEXIBLE MOTHERBOARD WITH VRM BYPASS TOPOLOGY

For the greatest flexibility, a VRM bypass circuit may be implemented to allow the use of any SC 330 processor. If a Pentium III Xeon processor or a 2.8 Volt Pentium III Xeon processor is installed, the HV_EN# signal is open, enabling FET Q1, connecting the VRM output to V_{CC_CORE} input at the voltage selected by the VID lines. When a 5/12 Volt Pentium III Xeon processor is installed, the HV_EN# line is grounded, which disables FET Q1 (and enables FET Q2), connecting either +5 or +12V to the processors V_{CC_CORE} input. See Figure 12.

NOTE: Intel recommends the use of the VRM sense lines to compensate for the small voltage drop across the FET due to its internal drain to source resistance. Provisions need to be added to the VRM sense line to open this line when the 5/12 volt CPU is installed. This protects the VRM from damage if 5/12 volts backfeeds the VRM. This can be accomplished by installing a small signal FET in series and driving the gate with the same signal as the gate input to Q1 shown in Figure 12.

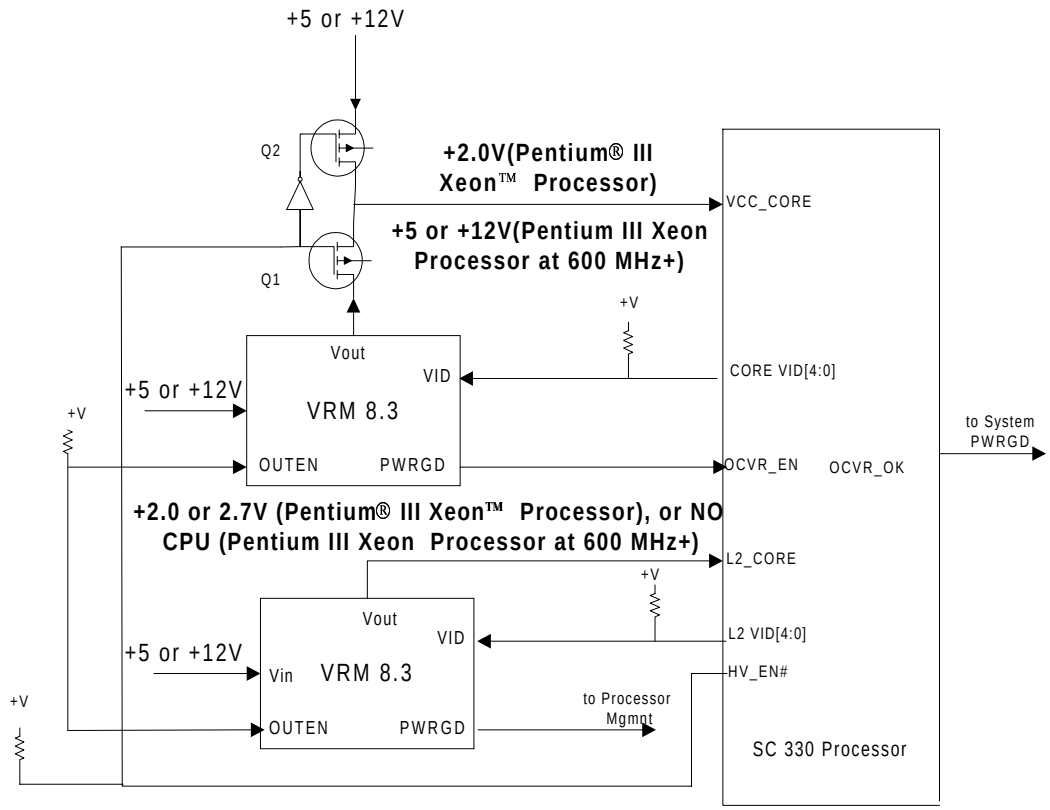

Figure 12. Flexible motherboard with VRM bypass configuration

5.6 PENTIUM III XEON PROCESSOR AT 600 MHz+ MOTHERBOARD TOPOLOGY

If full SC 330 processor support is not required, the exclusive support of Pentium III Xeon Processors at 600 MHz+ may be implemented. In this event, several issues require careful consideration.

Since the 5/12 Volt Pentium III Xeon processor's OCVR input can accept two discrete input voltages, it can be powered directly from the either the +5V or +12V outputs of the system power supply, eliminating the need for the VRM(s). However, special precautions must be made to ensure that OCVR DC and AC input specifications are strictly adhered to at the processor cartridge connector (see Table 3). See Figure 13.

Mixing 5/12 Volt Pentium III Xeon processors with 2.8 Volt Pentium III Xeon processors within a system is not allowed. Two 5/12 Volt Pentium III Xeon processors could be used with one processor operating at +5V and the other at +12V, allowing for system power supply output balancing.

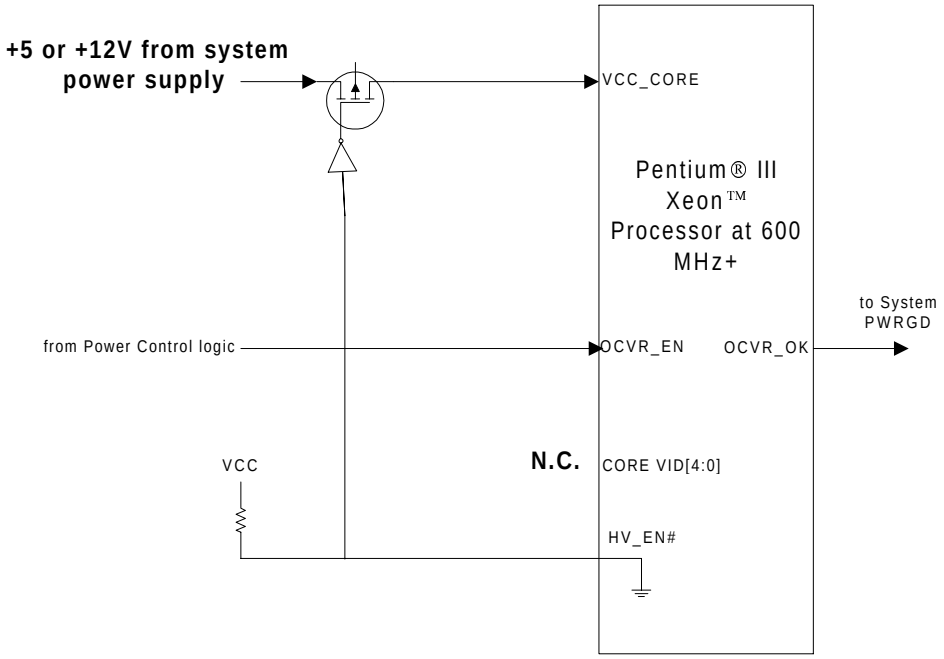

Figure 13. "Pentium III Xeon Processor at 600 MHz+ only" direct power supply configuration

5.7 POWER CONTROL

For flexible motherboard designs that support all SC 330 processors, Intel recommends the following design guidelines, as shown in Figure 14.

A 10KΩ (or greater) pull-up resistor must be placed between the OCVR_OK signal and the 3.3 Volt supply to properly support Pentium III Xeon processors. This will pull the OCVR_OK signal output high when a Pentium III Xeon processor is installed.

The VRM_PWRGD and the OCVR_OK signals should be logically ANDed. In the example below, this is accomplished with two open collector buffers whose outputs are combined in a wired-or fashion.

Note that the OCVR_EN signal has an internal pull-up resistor on the processor cartridge OCVR to 5V, so any external logic used with this signal must be 5V tolerant.

The wired-or outputs also serve to translate the resulting output signal to a 5 Volt level for system compatibility. The wired-or output can be used as an input to the system-wide PWRGOOD generation logic (taking care to account for the behavior of OCVR_OK prior to power being applied to the OCVR). For Pentium III Xeon processors, in the event of a faulty VRM (the VRM_PWRGD signal remains low) the wired-or output ensures that the Pentium III Xeon processor will remain reset by de-asserting the PWR_GD_PS signal.

Proper power-on control signal sequencing must be considered in order to prevent a race condition between the Pentium III Xeon Processor at 600 MHz+ OCVR_OK signal and the CPU_RESET# signal from the chipset, see Figure 9.

See Section 3.5.1 for OCVR_OK behavior prior to the application of power to the OCVR

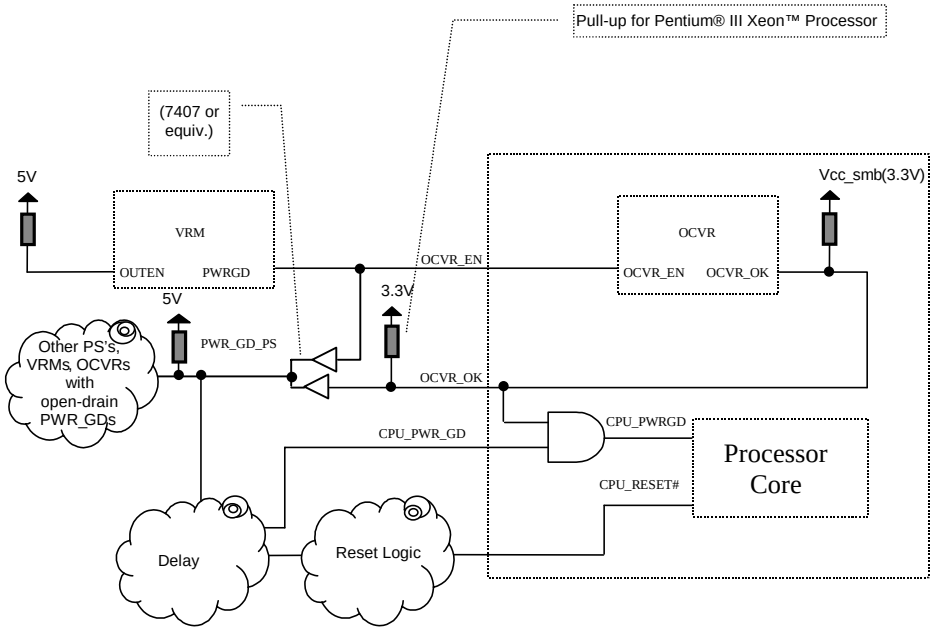

Figure 14. Flexible motherboard control recommendations

5.8 BULK AND HIGH FREQUENCY DECOUPLING

5.8.1 BULK DECOUPLING

For flexible motherboard designs, Intel recommends placing the bulk decoupling on the DC-to-DC converter module.

For Pentium III Xeon Processor at 600 MHz+-only motherboard designs, bulk decoupling capacitors are required on the V_{CC_CORE} lines as close as possible to the processor cartridge connector (no more than 1.0 inch maximum). The slew rate for V_{CC_CORE} on the Pentium III Xeon Processor at 600 MHz+ is 10 A/μS. Table 4 lists the recommended bulk capacitance parameters for all versions of Pentium III Xeon Processors at 600 MHz+.

Pentium III Xeon Processor at 600 MHz+	***Bulk Capacitance***	***ESR***	***RMS Current Rating***
2.8V	N/A (on VRM)	N/A	N/A
5.0V	≥ 2000μF	≤40mΩ	≥ 2.6A
12.0V	≥ 2000μF	≤40mΩ	≥ 1.1A

Table 4. Pentium III Xeon Processor at 600 MHz+ bulk capacitance recommendations

5.8.1 HIGH FREQUENCY DECOUPLING

The SC 330 processor cartridge contains all of the high frequency decoupling required for a properly designed system.

5.9 LAYOUT CONSIDERATIONS

System boards should include a sense input trace for each VRM 8.3. The trace resistance should be less than 1.0 Ohm.

5.9.1 REMOTE SENSE LINES

The VIN_SENSE line is provided on Pentium III Xeon Processors at 600 MHz+ to accurately compensate for losses and ensure adequate voltage delivery at the OCVR input. Intel recommends sense feedback to the VRM, either from a location on the processor cartridge connector, or through the VIN_SENSE line.

CORE_AN_SENSE is an analog representation of the output of the OCVR. This pin can be monitored to check the CORE voltage. The voltage seen at this pin is the actual operating voltage of the core (including the integrated L2 Cache) minus IR drops due to trace routing on the processor cartridge.

This L2_SENSE line is provided for system backward compatibility with systems that may want to monitor delivery of V_{CC_L2} voltage at the L2 cache device. Some legacy systems sample the L2 voltage to determine it is valid before asserting PWRGOOD.

NOTE: Intel recommends minimal loading of the sense lines to maintain accurate voltage sensing.

The following two sections explain sense trace routing.

5.9.2 FLEXIBLE SYSTEM DESIGN USING VRM 8.3

- Route a sense trace from VIN_SENSE (processor cartridge pin A56) to pin B5 on the VRM.
- If two Pentium III Xeon processors share an L2 VRM, route a sense trace from the mid-point of the V_{CC_L2} island to pin B5 on the L2 VRM.
- If each Pentium III Xeon processor has its own L2 VRM, route a sense trace from the L2_SENSE pin (processor cartridge pin B57) to pin B5 on the L2 VRM.

5.9.3 PENTIUM III XEON PROCESSOR AT 600 MHZ+-ONLY DESIGN USING DIRECT SYSTEM POWER SUPPLY

- Route sense trace from V_{IN_SENSE} pin to system power supply sense pin.

NOTE: If remote voltage sensing is not possible with the existing system power supply, then special care must be taken to ensure the V_{CC_CORE} DC and AC input specifications are met at the processor cartridge edge fingers. Cable, connector, and motherboard trace impedance drops must be compensated for. The compensation technique chosen for implementation is left to the system designer

5.9.4 OPTIONS FOR MEETING V_{CC} TOLERANCES

V_{CC_CORE} and V_{CC_L2} static and transient tolerances (and the corresponding VRM tolerances) of the SC 330 processor assume power distribution paths with resistance no greater than 0.5 mΩ and inductance no greater than 0.2 nH. Layout constraints may make these limits challenging. This section introduces two layout options for system board developers to consider in order to meet the required V_{CC} tolerances; first using VRM 8.3 for all SC 330 processors (flexible motherboard approach), and then without a VRM for Pentium III Xeon Processor at 600 MHz+-only designs.

NOTE: The addition of bulk capacitors as mentioned in Section 5.8, can be used to achieve the required voltage tolerances if the specified trace impedance's can not be met.

It may be possible to meet the 0.5 mΩ and 0.2 nH limits by placing the VRMs at the end of the processors closest to the V_{CC_CORE} and V_{CC_L2} pins, as shown in Figure 15. Either one plane of 2 oz. copper, or two planes of 1 oz. copper in parallel should be used.

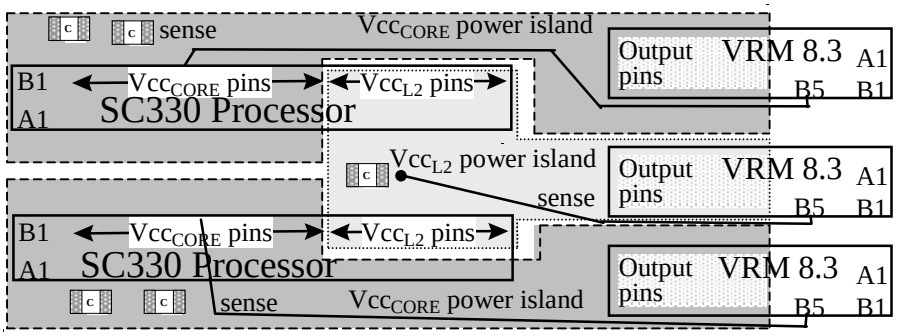

Figure 15. Flexible Motherboard with VRM's Layout option

As a second option, power the Pentium III Xeon Processor at 600 MHz+-only design directly from the system power supply, as shown in Figure 16. Two independent power islands are shown for use with 5/12 Volt Pentium III Xeon processors, allowing them to be powered from different voltages (e.g., one from +5 Volts, one from +12 Volts) if desired. Add on-board "bulk" capacitors as recommended in section 5.3.

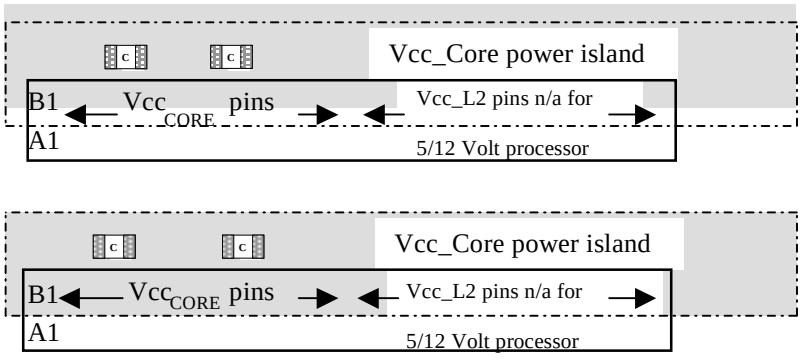

Figure 16. 5/12 Volt Pentium III Xeon processor-only with direct Power Supply Layout option

5.10 THE MAIN POWER SUPPLY

In a flexible motherboard design the main supply must provide power to the DC-to-DC converter as well as to the rest of the system. One should ensure that the input voltage to the DC-to-DC converter is within specifications, and is adequately decoupled in order to guarantee that it remains within specifications.

Similarly, in Pentium III Xeon Processor at 600 MHz+-*only* designs, care should be taken to ensure that the input voltage to the processor meets the voltage specifications outlined in the appropriate processor datasheet. The processor should also be adequately decoupled to guarantee that its input voltage remains within specifications.

5.11 COMPONENT MODELS

Designers should acquire component models from the selected component manufacturers. Intel cannot guarantee the specifications of another manufacturer's components. Table 5 contains some of the model parametric data developed by Intel for its simulations. AC transient models for V_{CC_CORE}, V_{CC_L2}, and V_{TT} of SC 330 processors are located in Section 6.

Component of Simulation	ESR (Ω)	ESL (nH)	ESL+ Trace + Via (nH)
0.1 μF Ceramic 0603 package	0.100	1.60	3.0
1.0 μF Ceramic 1206 package	0.120	0.47	1.9
100 μF MLC (2.05"x0.71")	0.005	0.30	1.7
47 μF, 16V Tantalum D Case	0.100	0.602	2.0
330 μF, 16V Aluminum Electrolytic	0.143	2.37	3.8
1000 μF, 10V Aluminum Electrolytic (20mm)	0.053	N/A	N/A
1000 μF, 25V Aluminum Electrolytic (25mm)	0.031	N/A	N/A
L_{BOARD}. One used for V_{SS}, one for V_{CC_CORE}. This estimate accommodates traces to vias, planes and the socket connections to the plane.	0.000	0.40	N/A

Table 5. Various Component Models Used at Intel (Not Vendor Specifications)

6. PROCESSOR POWER DISTRIBUTION NETWORK MODELING

Intel provides the AC electrical models shown in Figure 17, Figure 18, Figure 19 and Figure 20 for use in the simulation of the AC transient response of processor power delivery systems. Due to tool capability limitations, these models have been greatly simplified and are provided as a rough illustration of the processor cartridge power delivery systems.

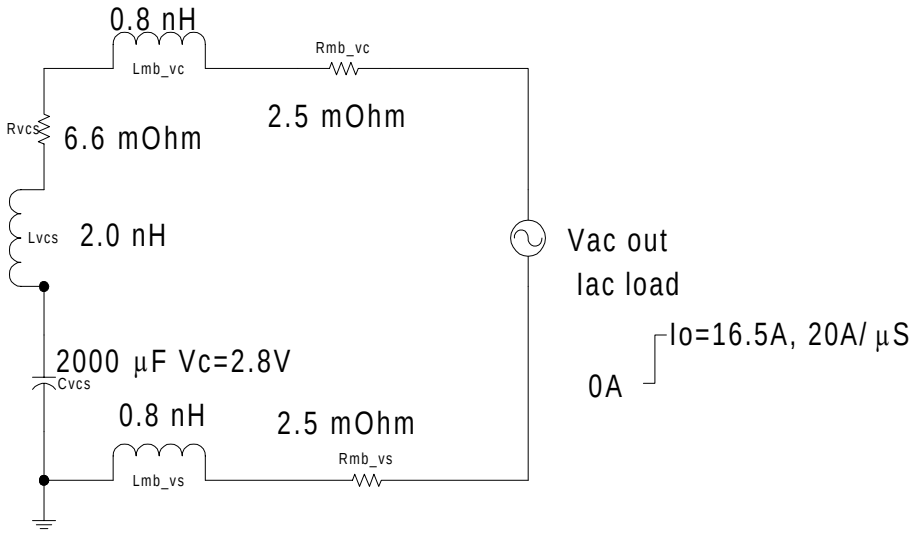

Figure 17. Flexible motherboard V_{CC_CORE} Power Delivery Model for AC Transient Response

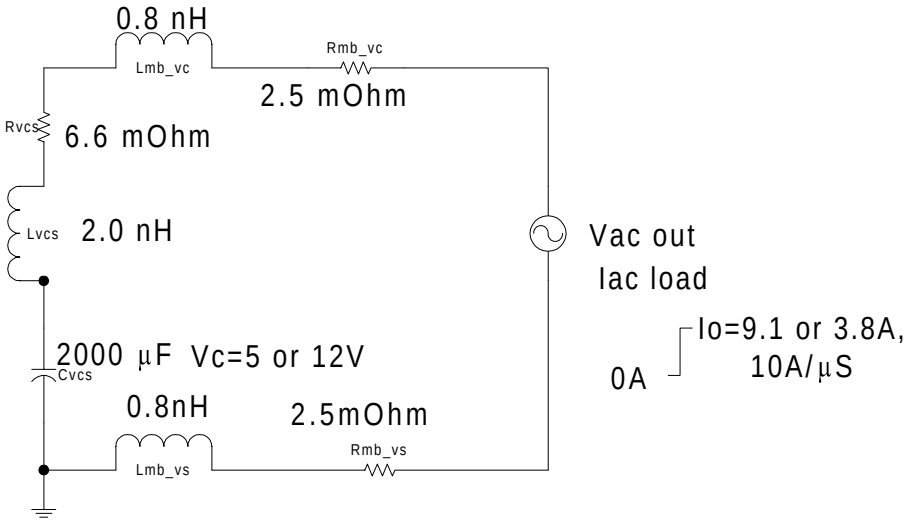

Figure 18. Pentium III Xeon Processor at 600 MHz+ only V_{CC_CORE} Power Delivery Model for AC Transient Response

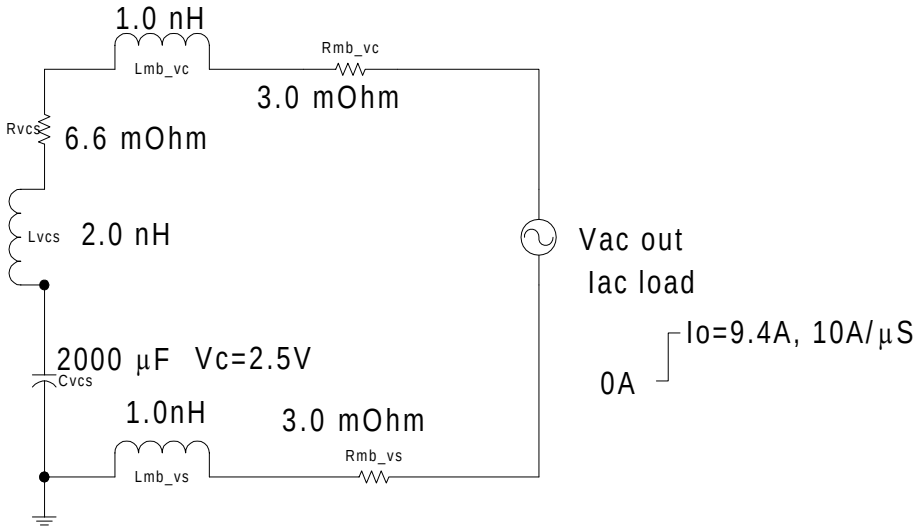

Figure 19. Pentium® III Xeon™ V_{CC_L2} Power Delivery Model for AC Transient Response

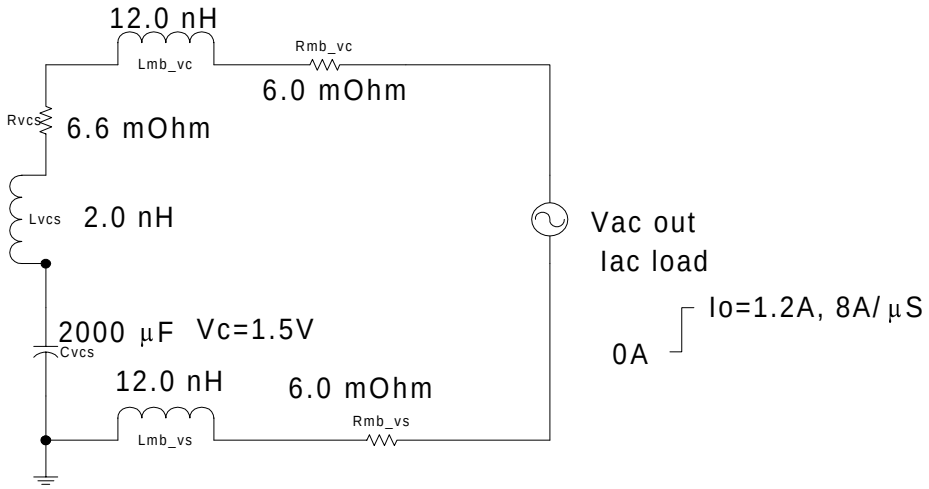

Figure 20. SC 330 processor V_{TT} Power Delivery Model for AC Transient Response

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