Intel® NetStructure™ ZT 5090

4U General Purpose Packet Switched Platform

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Revision History

Revision Number	Revision Date	Revision History
001	December 2001	Initial Release
002	January 2002	Added caution about using third party boards with alignment pins that insert into tapped screw holes in the chassis.
003	February 2002	Added information about only operating the system with compatible boards or blank filler panels in every slot.
004	January 2003	Added warranty information and air management information.
005	June 2003	Updated warranty information and customer support information.

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Document Organization

This Technical Product Specification describes the operation and use of the Intel® NetStructure™ ZT 5090 4U General Purpose Packet Switched Platform. The following summarizes the focus of each chapter in this manual.

Chapter 1, "Introduction," introduces the key features of the ZT 5090. This chapter includes a product definition and a list of product features. This chapter is useful for comparing the features of the ZT 5090 against the needs of a specific application.

Chapter 2, "Getting Started," provides installation and configuration information for the ZT 5090. This chapter should be read before attempting to use the system.

Chapter 3, "Field Replaceable Units," details the information needed for service and maintenance of the ZT 5090 system and its modular components.

Appendix A, "Specifications," contains the electrical, environmental, and mechanical specifications for the ZT 5090. It also provides connector pin assignments and a connector locations illustration.

Appendix B, "Power Supplies and Hot Swap Circuitry," addresses the relationship between hot swap performance and power supply loads, detailing minimum power supply start-up load and guaranteed regulation load requirements for proper hot swap configuration.

Appendix C, "Data Sheet Reference," provides data sheet links for technologies and devices used in the ZT 5090.

Appendix D, "Agency Approvals," presents UL, CE, and FCC agency approval and certification information for the ZT 5090.

Appendix E, "Customer Support," provides technical and sales assistance information.

1. Introduction

This chapter provides an overview of the ZT 5090 system. It includes a product definition and summaries of the system's hardware and software features. This chapter is useful for comparing the features of the ZT 5090 to the needs of a specific application.

User Documentation

The latest Intel NetStructure product information and manuals are available on the Intel NetStructure Website at http://www.intel.com/network/csp/products/cpci_index.htm. Refer to the following manuals and Technical Product Specifications for more information about the components that may be in your system.

- Intel® NetStructure™ ZT 5504 System Processor Board with Intel® Pentium® III Processor Hardware Manual
- The appropriate rear-panel I/O board hardware manual (ZT 4807)
- Intel® NetStructure™ ZT 8101 Fast Ethernet Switch Technical Product Specification
- Intel® NetStructure™ ZT 7101 Chassis Management Module Technical Product Specification
- Intel® NetStructure™ Embedded BIOS Software Manual
- Hot Swap Kit for Windows* 2000 CompactPCI* Systems Software Manual

Product Definition

The ZT 5090 is a 4U, rack-mount, 8-slot (seven node slots and one fabric slot) CompactPCI system for telecom and Internet applications built around the PICMG 2.16 V1.0 Packet Switching Backplane specification. The system features a transversely mounted backplane that accepts 6U cards at the front and rear. The backplane includes dual PCI buses and Dual H.110 buses.

Slot 1, at the top of the enclosure, contains the system's dedicated 2.16 fabric board slot, allowing communication between slots 2-8 via a fast Ethernet switch such as the Intel NetStructure ZT 8101. This topology connects link ports 'a' and 'b' from each node to the same fabric. This provides better utilization of Ethernet link ports on the fabric board and increased bandwidth to node slots in a compact 4U chassis.

Slots 3 and 7 provide support for two System Master processor boards such as the Intel NetStructure ZT 5504. Slots 2, 4-6 and 8 allow loading of up to five peripheral boards.

The Chassis Management Module (CMM) slot at the lower left of the enclosure provides a location for a PICMG 2.9 compliant System Management/IPMI module such as the Intel NetStructure ZT 7101 Chassis Management Module. The CMM is required for the ZT 5090 to power up unless BD_SEL# is jumpered to ground.

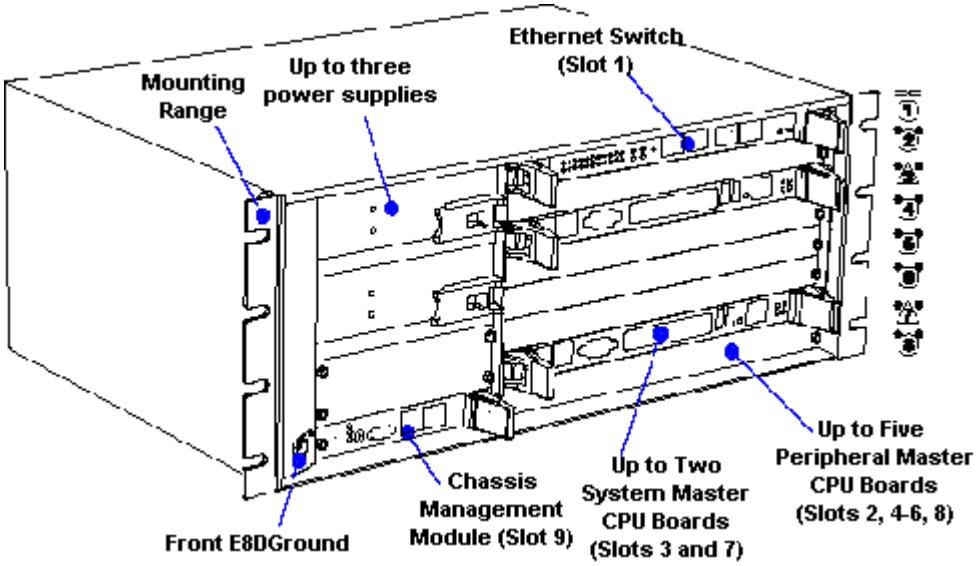
The ZT 5090 also features support for three 250W power supplies, a replaceable fan tray with two high-efficiency blowers, and optional rear panel I/O.

Your system may differ from the configurations depicted in this manual. Please contact Intel for available system configurations (see "Customer Support" for contact information).

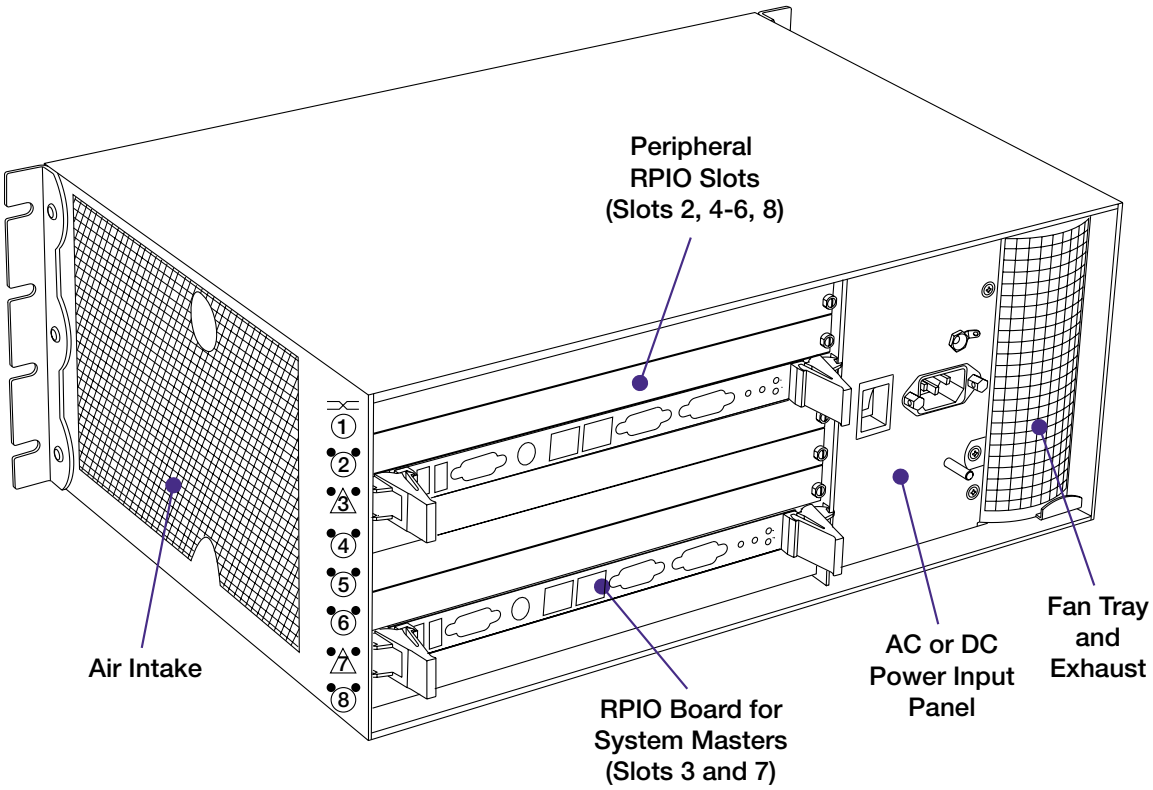
ZT 5090 Features

- Low profile 4U height, 19-inch rack-mount enclosure
- 8-slot (total) PICMG 2.16 Compliant CompactPCI backplane accepts 6U boards
- Dual independent CompactPCI segments of four and 3 slots, respectively
- Dual H.110 computer telephony bus (PICMG* 2.5 R1.0)
- Fan-tray mounted blowers provide side-to-rear cooling
- Support for up to three 250W power supplies
- Support for a dedicated 2.16 fabric board
- Support for two System Master processor boards featuring Intel® Pentium® processors
- Support for a Chassis Management Module
- Choice of Rear Panel I/O boards to compliment processor boards

ZT 5090 Features (Front)



ZT 5090 Features (Rear)



Functional Considerations

The following topics briefly discuss the key functional areas of the ZT 5090 platform. Refer to Appendix A, "Specifications," for mechanical, electrical, and environmental specifications.

Mechanical Considerations

The ZT 5090 is a 19" EIA rack-mount system compliant with the 4U Eurorack height standard. Mounting flanges are included with the system and can be positioned for front- or mid-mounting.

The ZT 5090 platform is compatible with front-mounted IEEE* 1101.10 compliant boards, rear-mounted IEEE 1101.11 transition boards, and 3U modular power supplies. See the "Mechanical Specifications" topic in Appendix A for system dimensions.

Electrical Considerations

The ZT 5090 system is compliant with

- CompactPCI Specification, PICMG 2.0, R3.0
- CompactPCI Hot Swap Specification, PICMG 2.1, R1.0
- CompactPCI Packet Switching Backplane Specification, PICMG 2.16, R1.0
- CompactPCI Computer Telephony Specification, PICMG 2.5, R1.0
- CompactPCI System Management Specification, PICMG 2.9, R1.0

The system is factory configured for either AC or DC power input. The power input panel configuration must match the power supply input voltage (AC or DC). The power input panel incorporates a power standby/off switch, a grounding stud (CHASSIS GROUND), and an ESD grounding jack (ESD GROUND). An additional ESD grounding jack is provided at the front of the system. See the "Electrical Specifications" topic in Appendix A for more information.

The ZT 5090 features a universal backplane that can be configured for 3.3V or 5V V(I/O) CompactPCI device support. As shipped from the factory, the backplane is jumpered for 5V operation and the CompactPCI connector mating keys allow only 5V boards to be installed. See the “Setting V(I/O)” topic for details.

Environmental Considerations

The ZT 5090 system, as configured by Intel, is designed to withstand the shock and vibration levels found in most industrial environments. Due to the modular construction of the system, components could be added that change the system’s environmental constraints. Board level components and power supply modules have their own operating temperature ratings. Refer to component-specific product manuals for operational details that may affect system performance. See "Environmental Specifications" in Appendix A for more information.

This product contains materials that may be regulated upon disposal. Please dispose of this product in accordance with local rules and regulations. For disposal or recycling information, please contact your local authorities or the Electronic Industries Alliance: http://www.eia.org.

2. Getting Started

This chapter describes the steps necessary to install and set up the ZT 5090 system. It includes instructions on unpacking, rack mounting, and making power connections.

Unpacking the System

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Intel for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to Intel. Refer to the "Customer Support" section for assistance information.

CAUTION: Intel has designed special packing material to protect the system during shipping. It is critical that the packing material be saved after unpacking the enclosure. Shipping the unit without the original packing material may void the warranty. Replacement packing material can be purchased from Intel.

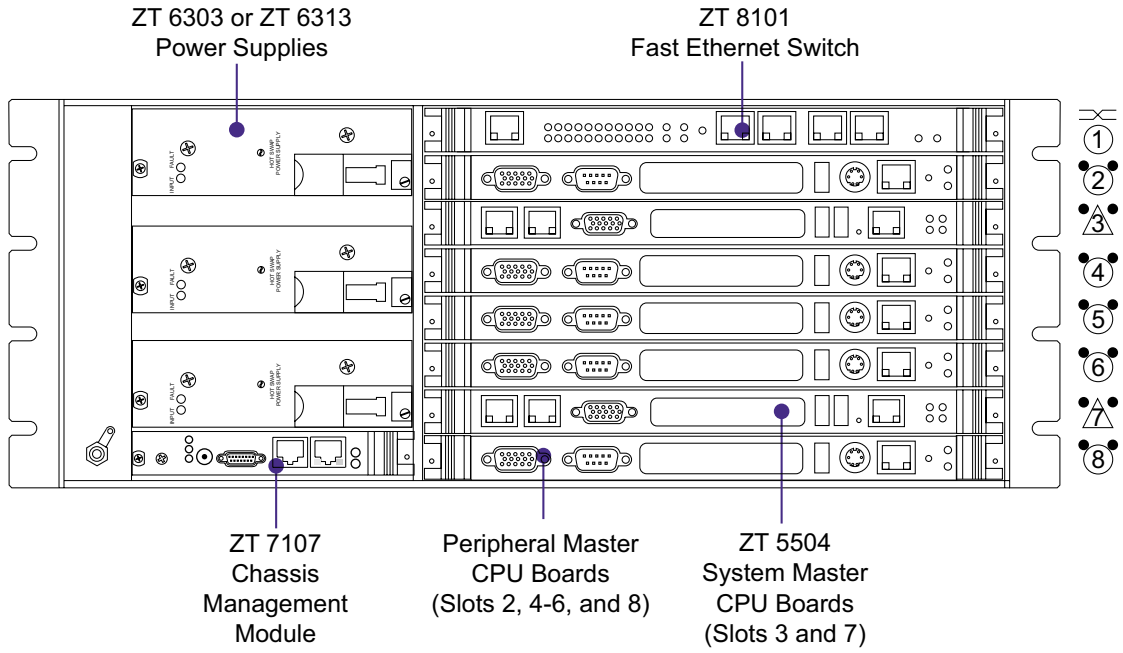
CAUTION: This system contains board-level components that must be protected from static discharge and physical shock. Wear a wrist strap grounded through one of the system's ESD Ground jacks when handling system components.

Shipping Contents

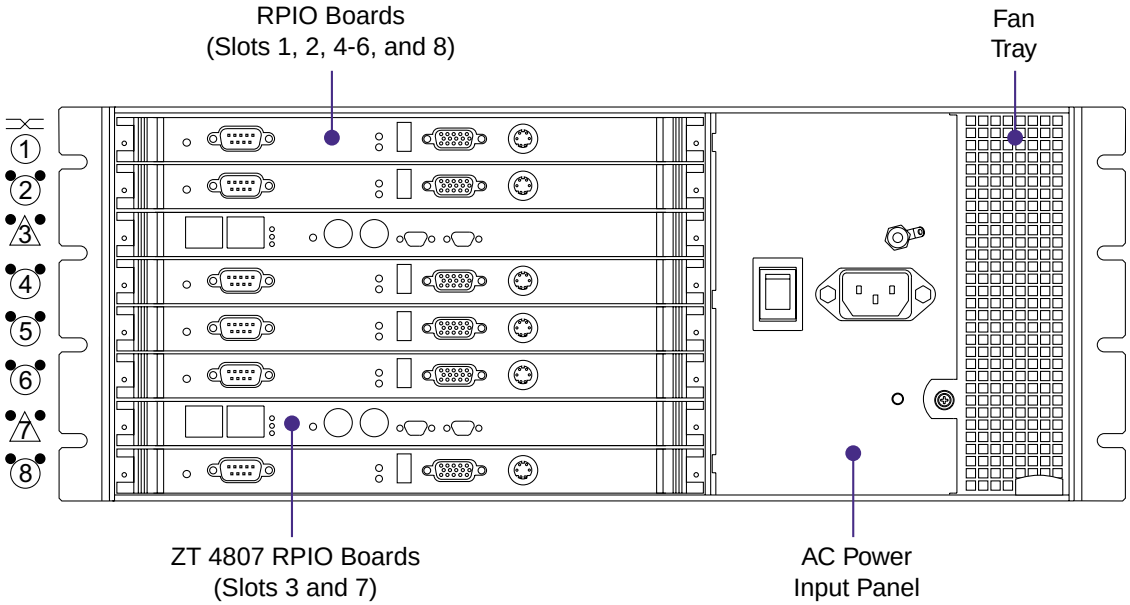
The ZT 5090 may be ordered with many options. The system is shipped fully assembled and tested and may be accompanied by several accessories. The basic system configuration and most common options and accessories are listed below. Your system may differ from the system illustrated in this manual.

- Basic configuration:
  - 4U 19" rack-mount enclosure with mounting flanges attached
  - 8-Slot (total) PICMG 2.16 V1.0 packet switching backplane (with dual H.110 bus)
  - AC or DC power input panel
  - Up to three AC input or DC input modular power supplies
  - Fan tray with two blowers
- Board-level options:
  - ZT 5504 System Master processor board
  - ZT 8101 Fast Ethernet Switch
  - ZT 7101 Chassis Management Module
  - ZT 4807 Rear Panel I/O board (for System Master processor board)
- Accessories:
  - AC power cord (with AC-configured system)
  - Safety and compliance literature
  - Optional software support packages and development kits

Fully Loaded Example (Front)



Fully Loaded Example (Rear)



Installing the System

Before installing and using the ZT 5090, ensure that all cover panels are in place and that all component slots are populated with a component, filled with an air management board (front), or covered with a blank filler panel (rear). Use CompactPCI industry standard blank filler panels with EMI gaskets for the rear panel. Air management boards may be purchased from APW Electronic Solutions or equivalent. Blank filler panels may be purchased from Intel. Refer to the following part numbers.

- To fill a single slot, use panels that are 6U x 4HP (horizontal pitch=0.2") (Intel PN 835022).
- To fill a double slot, use panels that are 6U x 8HP (Intel PN 844131).
- To fill a front slot, use an EMC air management board, 6U X 160 (APW PN AMB-EHD160 or APW PN AMB-EHD161).

WARNING: Failure to cover open slots could cause overheating of power supplies, boards, or other components, and could damage the system.

The ZT 5090 system fits standard 19" EIA racks. Mounting flanges are attached to the front of the enclosure to facilitate front mounting. The flanges can be repositioned for center-mounting the enclosure.

WARNING: This unit is intended for installation in restricted access locations.

CAUTION: To prevent damage to the components, never use component handles or cables to lift or move the system.

This system is intended for stationary mounting in a rack designed to meet the physical strength requirements of NEBS GR-63-CORE and NEBS GR 487. Be sure to mount the system in a way that ensures even weight distribution in the rack. Uneven mechanical loading can result in a hazardous condition. Secure all mounting bolts when installing the enclosure to the frame/rack.

The maximum ambient temperature at which a factory-configured ZT 5090 system should operate is 40°C at 5% to 85% relative humidity (see Appendix A, "Environmental Specifications" for details). If the system is installed with its ventilation intakes near another system's exhaust or in a closed or multi-unit rack assembly, the operating ambient temperature inside the enclosure may be greater than the room's ambient temperature. Install the system in an environment compatible with this recommended maximum ambient temperature. Due to the modular design of the system, components may be installed that alter the system's operating requirements. Please refer to product-specific documentation for the maximum recommended ambient temperature for individual components.

Safe operation of the ZT 5090 is dependent on the 200LFM/slot of forced-air cooling provided by the system's cooling fans. Be sure to install the system in an environment that does not compromise this recommended minimum air flow requirement.

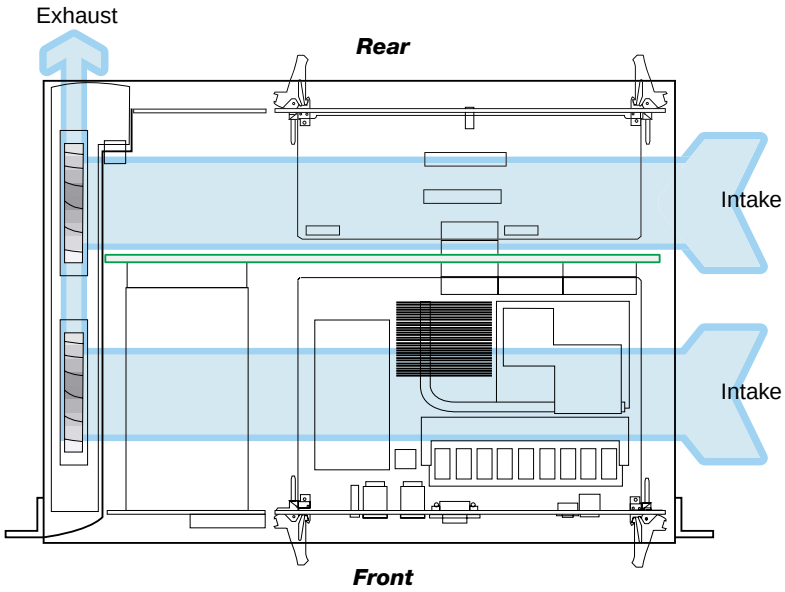
The following topics discuss installing the ZT 5090 step-by-step.

Rack Mounting the System

1. Disconnect all power sources and external connections/cables prior to installing or removing the system from a rack.
2. Select a position in the rack that does not interfere with other equipment and that provides safe weight distribution.

3. For efficient cooling, the area around the ZT 5090's intake and exhaust vents should be clear of obstructions. The intake should be away from another system's exhaust (refer to the following “Air Flow” illustration).
4. Secure the mounting flanges to the front or middle of the enclosure.
5. Place the enclosure in its intended location and line up the mounting holes on the ZT 5090's flanges with the rack's mounting holes.
6. Bolt the enclosure to the rack (rack hardware is not included).

Air Flow



Grounding the System

Before making any connections to the system, the enclosure must be properly grounded.

- Attach a grounded strap or cable, with a #10 ring terminal, to the Chassis Ground post on the ZT 5090's power input panel (refer to the “Power Input Panel” illustration).
- ESD ground jacks are located at the front and rear of the system. To protect components from static shock when handling system components, wear a wrist strap plugged into the most convenient ESD jack. Refer to the “ZT 5090 Features (Front)” Illustration in Chapter 1 and the following “Power Input Panel” illustration for ESD ground jack locations.

Providing Power

The power input panel at the rear of the enclosure allows AC or DC power to be connected to the system. The power input panel configuration must match the voltage input configuration of the power supplies intended for use with the system. See the “Power Input Panel” illustration for connector locations.

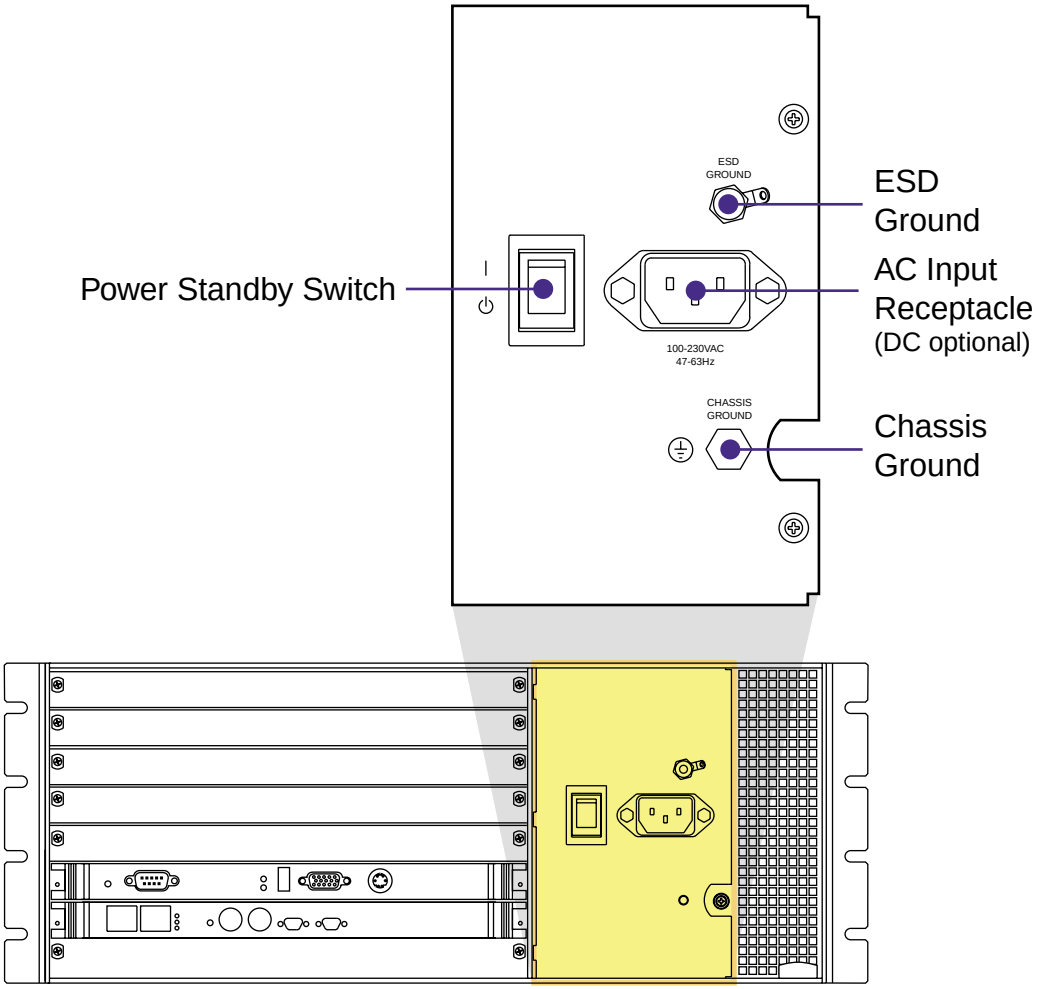
The ZT 5090 must be connected to a properly rated supply. For permanently connected equipment, a readily accessible disconnect device should be incorporated in the building wiring installation.

This product relies on the building's wiring installation for short-circuit (overcurrent) protection. Ensure that a listed and certified fuse or circuit breaker no larger than 72 VDC, 15 A is used on all current-carrying conductors.

WARNING: Always use a grounded outlet to supply power to the system. Always use a power cable with a grounded plug, such as the one supplied with the system.

When the system is plugged in, high voltages are present on the backplane. Do not reach into the enclosure.

Power Input Panel (AC System)



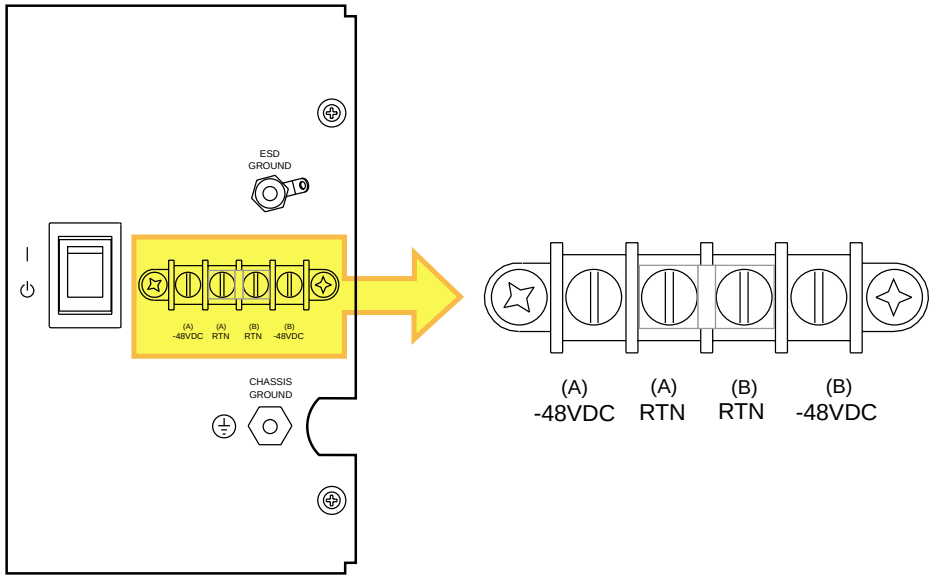
Connecting AC Power (P1 Option)

1. Ensure that the power standby switch is in the “standby” (⏻) position. See the “Power Input Panel” illustration for switch location.
2. Connect the supplied power cord to the AC power receptacle at the back of the enclosure and engage the cable retention device.
3. Plug the power cord into a grounded AC outlet capable of supplying 100 to 230VAC @ 50 to 60Hz @15A.

4. Once power is connected, the power standby switch may be used to turn on the system.

WARNING: The power standby switch does not turn off power to the system. The system must be disconnected from the power source.

DC Terminal Block



Connecting DC power (P2 Option)

1. Ensure that the power standby switch is in the “standby” (⏻) position. See the “DC Terminal Block” illustration for switch location.
2. Remove the protective cover from the DC terminal block.
3. The **(A) RTN** and **(B) RTN** terminals should be tied together with a suitable jumper. A jumper comes pre-installed on the terminal block.
4. Connect the DC supply terminals to the terminal block. Connections should be made with 18-14AWG wire with #8 ring terminals (use copper conductors only). To provide DC input power redundancy, connect both the (A) and (B) inputs. See the “DC Terminal Block” illustration for terminal assignments.
5. Replace the protective cover on the terminal block.
6. Complete the connection to the DC power source.
7. Once power is connected, the power standby switch may be used to turn on the system.

WARNING: The power standby switch does not turn off power to the system. The system must be disconnected from the power source.

Connecting I/O Devices

The front and rear board-level components in the ZT 5090 system offer connections for many different I/O devices such as a monitor, keyboard, mouse, and serial devices. Rear panel connectors are for added cabling flexibility and should not be used to connect extra devices to a given processor board. Unpredictable behavior may occur if the same front and rear panel connectors are used simultaneously (i.e., connecting two keyboards).

Refer to Intel's board-specific manuals for connectivity options and limitations.

Connecting to a Network

Most Intel NetStructure System Master and Peripheral Master processor boards support two channels of 10/100 Mbps Ethernet. Your system may include both front- and rear-panel Ethernet connectors for channels A and B. Each channel can be independently routed for connection at the front of the system (on the processor board) or at the rear of the system (on the RPIO board). Refer to board-specific hardware manuals for additional Ethernet connectivity information.

IMPORTANT: Connection to a 100BASE-TX hub for 100 Mbps operation requires Category 5 unshielded twisted-pair (UTP) cable. The maximum length from the 100BASE-TX hub to the adapter is 100 meters. Connection to a 10BASE-T hub for 10 Mbps operation requires a Category 3, 4, or 5 UTP cable.

Setup and Configuration

The following topics present a brief introduction to the setup and configuration of the ZT 5090.

BIOS Configuration

For detailed information about BIOS configuration and diagnostics, see the *Intel NetStructure Embedded BIOS Software Manual* and specific Intel NetStructure processor board manuals located at http://www.intel.com/network/csp/products/cpci_index.htm.

Operating System Installation

If it is necessary to install an operating system on the processor boards included with your ZT 5090, refer to specific Intel NetStructure processor board manuals. For OS-specific information, refer to the documentation provided by the OS vendor or visit the appropriate Internet web site.

Other Setup Considerations

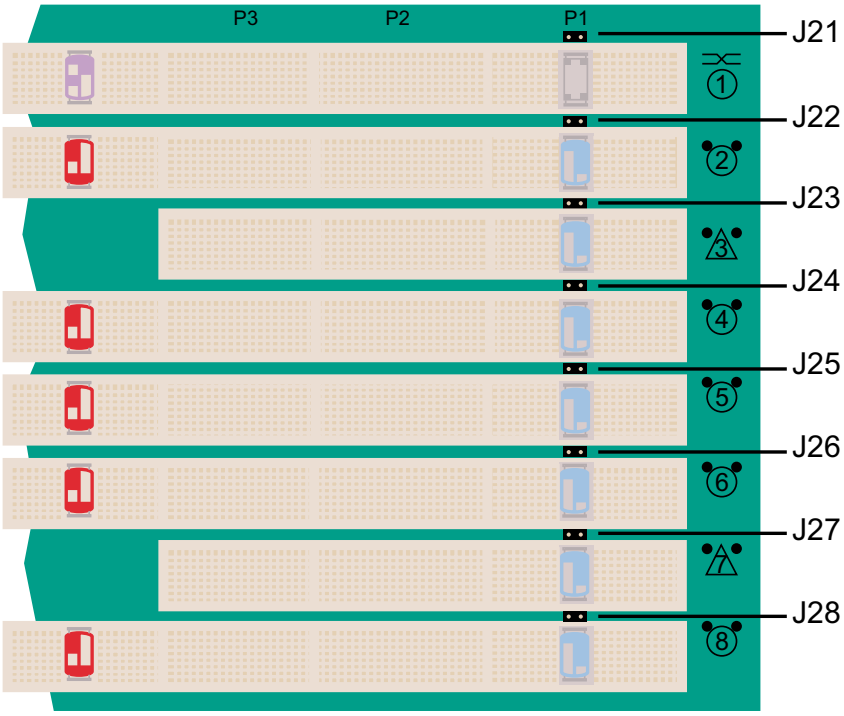
The ZT 5090's backplane has several features that can be used to tailor the system for use in a specific environment. The following topics address BD_SEL# signals, shelf enumeration, slot assignments, and setting V(I/O).

BD_SEL# Signals

The BD_SEL# signal must be asserted (grounded) to boards inserted in slots 1-8 for the boards to power up. A Chassis Management Module (CMM) operating in slot 9 controls

BD_SEL# assertion to slots 1-8. The ZT 5090's backplane provides eight standard, two-post jumper locations that allow assertion of BD_SEL# to slots 1-8 in the absence of a CMM (refer to the "Jumper Locations (Front)" illustration). Systems operating without a CMM must have jumpers installed in all eight locations. Systems operating with a CMM should have jumpers removed from all eight locations. The factory default configuration does not install jumpers in these locations. See the "Working with the Chassis Management Module" topic for more information.

Jumper Locations (Front)



J21-J28 Position		Operation
	All In	System with no CMM
Default	All Out	System with CMM

Shelf Enumeration

Assign a unique address to the ZT 5090 for use with other systems by configuring cuttable traces CT1-CT10. See the "Shelf Enumeration" topic in Appendix A for more information.

Slot Assignments

The ZT 5090's backplane supports geographic addressing; each slot is individually addressed to match its slot number. See the "CompactPCI Slot Connectors" table for physical to logical slot relationships.

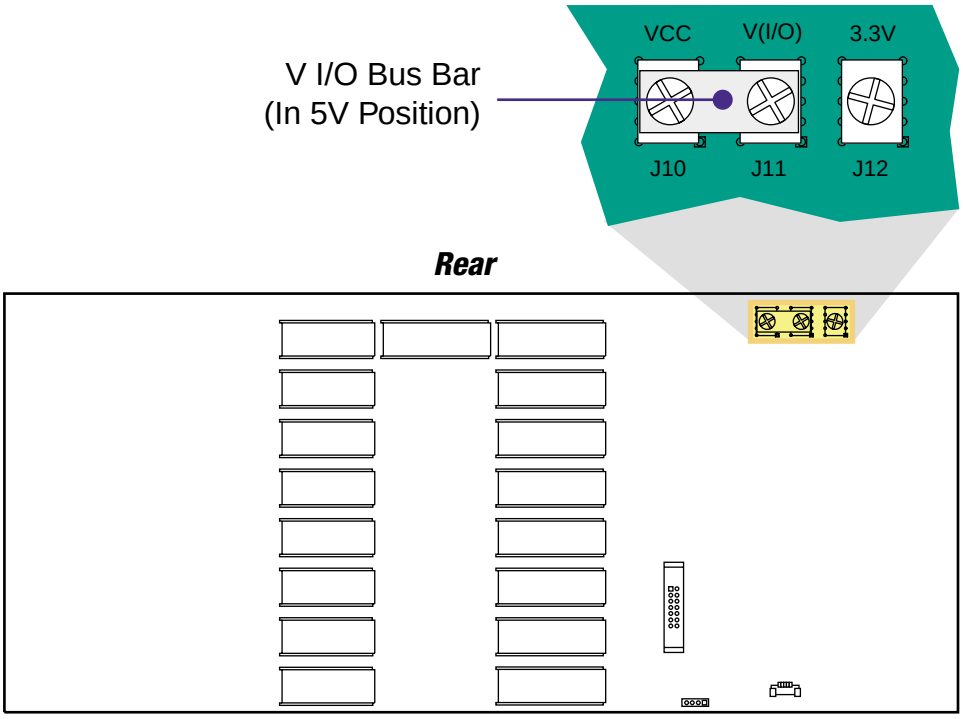
The backplane is fully hot swap compliant and buses individual clocks from the System Slot (slots 3 and 7) to each of the peripheral slots (slots 2, 4-6, and 8). Refer to the *CompactPCI Specification, PICMG 2.0, R3.0* for additional information on slot addressing and signal assignment.

Setting V(I/O)

The ZT 5090 incorporates a "universal" backplane, allowing V(I/O) to be changed for use with either 5V or 3.3V boards. A jumper bus bar at the rear of the backplane controls V(I/O) provided to the CompactPCI slots. See the "V(I/O) Selection" illustration below. Connect J10 to J11 for +5V operation, or J11 to J12 for +3.3V operation. The factory default setting is for 5V operation (terminals J10 and J11 are jumpered).

CompactPCI boards are designed for use in 5V or 3.3V systems. Boards incorporate a color-coded mechanical key (in the J1 CompactPCI connector) that prevents a 3.3V board from inserting into a 5V backplane and vice versa. Since the ZT 5090's backplane is configured for use with 5V boards, the jumper and the CompactPCI keys must be changed for use with 3.3V boards.

V(I/O) Selection



3. Field Replaceable Units

Field Replaceable Units (FRUs) are modular components that can be quickly and easily serviced without disturbing other components in the system. Some FRUs are hot swappable and can be serviced without turning the system off. The following topics discuss working with the ZT 5090's modular components including the Chassis Management Module, board-level components, power supplies, and the fan tray. For details about specific board products, refer to the appropriate board-level hardware manuals.

WARNING: When the system is plugged in, high voltages are present on the backplane. Do not reach into the enclosure.

WARNING: Static electricity can damage electronic components. Wear a wrist strap grounded through one of the system's ESD Ground jacks when servicing system components.

Working with the Chassis Management Module

The Chassis Management Module (CMM) affects power to slots 1-8 in accordance with the PICMG 2.1 specification. PICMG 2.1 defines the power control (BD_SEL# signals) as pulled up on general-purpose boards. This means that the BD_SEL# signals must be asserted (grounded) for the boards to power up. A CMM operating in slot 9 controls BD_SEL# assertion to slots 1-8.

Jumpers at locations J21-J27 on the ZT 5090 backplane allow assertion of BD_SEL# to slots 1-8 in the absence of a system CMM (See the topic BD_SEL# Signals for more information). Check that jumpers are removed from all eight locations if the system is intended for use with a CMM. Installed jumpers may cause unpredictable behavior from the chassis management software. The factory default configuration does not install jumpers in these locations.

Installing the CMM

The following instructions cover the mechanical aspects of installing the ZT 7101 CMM in a ZT 5090 system.

1. System power does not need to be off to install a CMM. The CMM must only be inserted in slot 9 (refer to the "ZT 5090 Features (Front)" illustration for slot identification.
2. Remove the filler-panel or existing CMM (see "Removing the CMM" for removal instructions).
3. Prepare the new/replacement CMM by opening its injector/ejector handle (refer to the "Injector/Ejector Operation" illustration).
4. Carefully align the edges of the board with the card guides in the CMM slot. It may be helpful to look into the enclosure to verify correct alignment of the rails in the guides.
5. Taking care to keep the board aligned in the guides, slide the board in until the injector/ejector mechanism engages the retention bar.

6. Simultaneously push in the board and rotate the injector/ejector handle to its closed position (rotate inward) to seat the backplane connectors.
7. If system power is on, the CMM boots and its Status LED lights green (active CMM) or blinks green (standby CMM).
8. Screw in the board retention screw to anchor the board in the chassis. This screw is located at the opposite end of the faceplate from the ejector handle.
9. Use the CMM's Command Line Interface (CLI) to configure the CMM. Refer to the *ZT 7101 Chassis Management Module Hardware Manual* for more information.

Removing the CMM

The following instructions cover the mechanical aspects of removing the ZT 7101 CMM from a system.

NOTE: Because the CMM controls the power to every slot in the system (via BDSEL#), if the system's CMM is removed all the boards in the system will lose power. When removing a CMM from a powered system, the CMM performs a controlled shutdown of itself but not the other boards in the system. Therefore, you should ensure that the entire system is in a "safe" state before removing the CMM.

1. System power does not need to be off to remove a CMM board.
2. Unscrew the board retention screw that fastens the board to the enclosure. This screw is located at the opposite end of the faceplate from the ejector handle.
3. If system power is off or the CMM's blue hot swap LED is on, proceed to step six. If not, the CMM needs to be in a "safe" state before it can be removed. Signal the CMM that it is about to be removed by partially unlatching its ejector. Do not fully open the ejector as this levers the board out of the enclosure and breaks its backplane connection before the board can shut down properly.
4. Wait for the blue hot swap LED to light. This shouldn't take more than a few seconds.
5. Open the ejector handle fully, rotating it outward until the board disengages from the backplane (refer to the "Injector/Ejector Operation" illustration).
6. Slide the board evenly out of the enclosure.
7. Install a replacement CMM or cover the empty slot with a filler panel to maintain the system's shielding and cooling performance. If no replacement CMM is installed, ensure that BD_SEL# jumpers are installed for all populated slots.

Working with Board-Level Components

The ZT 5090 has slots for up to nine board-level components at the front of the enclosure (see the "ZT 5090 Features (Front)" illustration). Slots are numbered 1 through 9, with slot 1 being at the top right of the enclosure, slot 8 at the bottom right, and slot 9 at the bottom left. Slots are defined as follows:

Slot 1	Fabric Slot; supports PICMG 2.16-compliant Ethernet switch boards.
Slots 2, 4-6, 8	Peripheral Slots; support Peripheral Master processor boards and other peripheral boards.
Slots 3 and 7	System Slots; support System Master processor boards.
Slot 9	CMM Slot; supports a Chassis Management Module.

Boards installed at the front of the ZT 5090 may be paired with Rear Panel I/O (RPIO) boards accessible from the rear of the system (see the "ZT 5090 Features (Rear)" illustration).

CAUTION: Some third party CompactPCI boards use latches with alignment pins that insert into tapped screw holes in the chassis. Intel highly recommends removing the alignment pins prior to insertion of these boards into the chassis. Insertion of alignment pins into tapped screw holes can generate metal particles, resulting in product failure. Failures resulting from use of this latch type are not covered under the Intel warranty.

The following instructions cover the removal and installation of System Master processor boards, Peripheral Master processor boards, and RPIO boards. There are additional considerations to working with the Chassis Management Module. This component is therefore covered in a separate topic.

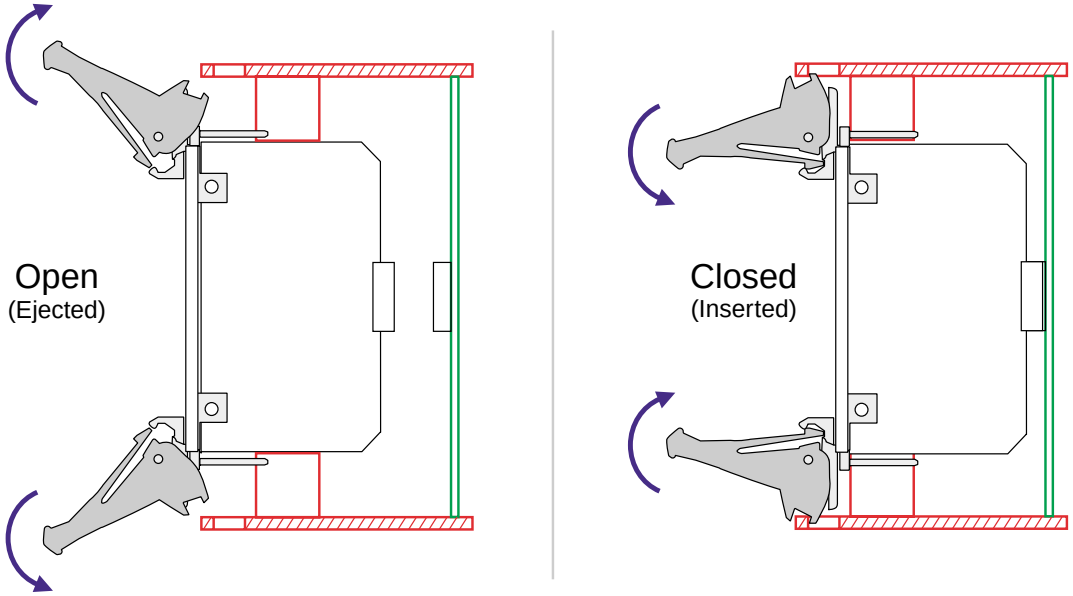
CAUTION: Processor boards may contain a socketed lithium battery. This battery is not a field-replaceable unit. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions. Return the processor board to the manufacturer for battery service.

Installing a Processor Board

The following steps cover the mechanical aspects of installing an Intel NetStructure System Master processor board in a System Slot (slots 3 and 7) or a Peripheral Master in a Peripheral Slot (slots 2, 4-6, and 8).

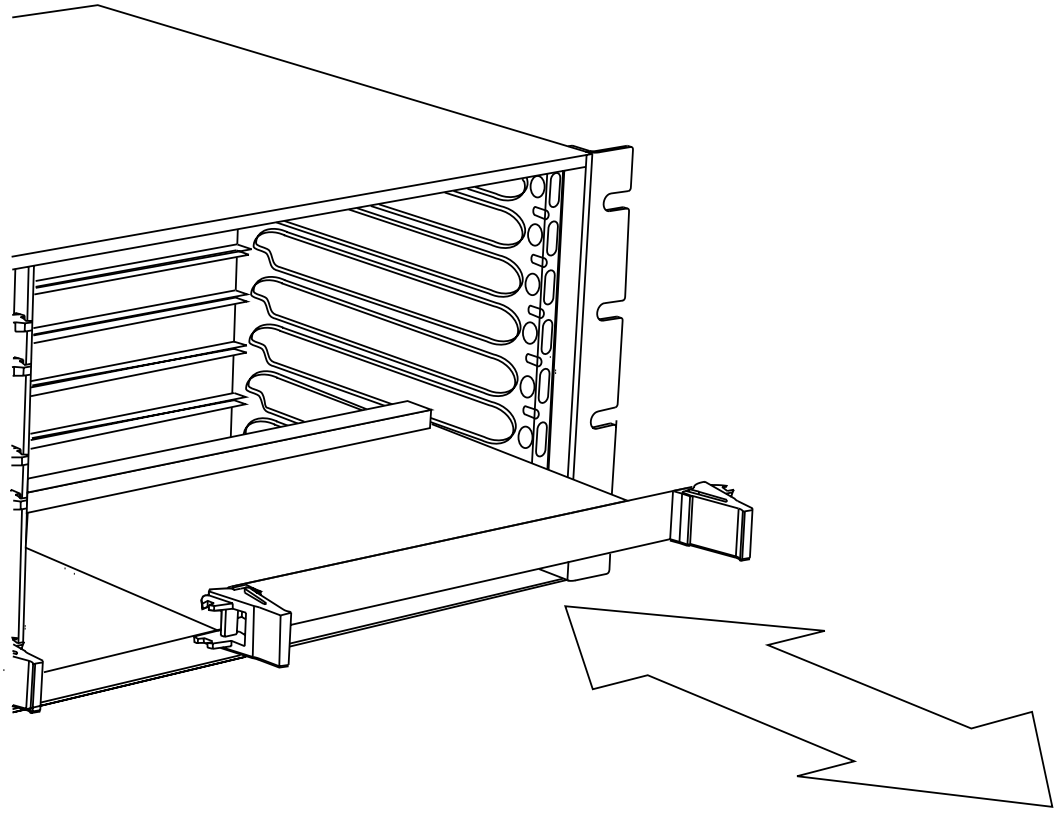
1. System power does not need to be off to insert a ZT 5504 System Master or a hot-swappable Peripheral Master processor board. The System Master processor board must only be inserted in slot 3 or slot 7 (refer to the "ZT 5090 Features (Front)" illustration for slot identification. Peripheral Master processor boards must only be inserted in peripheral slots 2, 4-6, and 8.
2. Prepare the board by opening the injector/ejector mechanisms (refer to the "Injector/Ejector Operation" illustration).

Injector/Ejector Operation (Board-Level Components)



3. Carefully align the edges of the board with the left and right card guides in the appropriate slot (refer to the "Board Alignment in the Enclosure Card Guides" illustration). It may be helpful to look into the enclosure to verify correct alignment of the rails in the guides.

Board Alignment in the Enclosure Card Guides



4. Taking care to keep the board aligned in the guides, slide the board in until the injector/ejector mechanisms engage the retention bars (refer to the "Injector/Ejector Operation" illustration).
5. Simultaneously push in the board and rotate the injector/ejector mechanisms to their closed positions (rotate inward) to seat the backplane connectors. When the processor board is in place and system power is on, the status light on the board turns green, and the board boots.
6. Make the desired connections at the faceplate and configure the processor board.

Removing a System Master Processor Board

The following steps cover the mechanical aspects of removing an Intel NetStructure System Master processor board from a System Slot (slots 3 and 7).

The processor board may be accompanied by a media expansion board, such as a CD-ROM drive carrier. In this case, the processor board and expansion board must be removed/installed together. Ejector/injector handles on the boards are ganged (connected together) and operate as one.

1. System power does not need to be off to remove a ZT 5504 processor board. The System Master processor board(s) can reside in slots 3 and 7.
2. Disconnect connections at the faceplate (Ethernet, VGA, keyboard, etc.).
3. Unscrew any retention screws that fasten the board to the enclosure. If the processor board has an attached media expansion board, unscrew the retention screws that fasten it to the enclosure.
4. Open the ejectors fully, rotating the handles outward until the board disengages from the backplane (refer to the "Injector/Ejector Operation" illustration).
5. Slide the board evenly out of the enclosure. If the processor board has a media expansion board attached to it, the boards will slide out together.
6. Install a replacement board or cover the empty slot with a filler panel to maintain the enclosure's shielding and cooling performance.

Removing a Peripheral Master Processor Board

The following steps cover the mechanical aspects of removing an Intel NetStructure Peripheral Master processor board from slots 2, 4-6, or 8.

1. System power does not need to be off to remove a hot-swappable Peripheral Master processor board.
2. Disconnect connections at the faceplate (Ethernet, VGA, keyboard, etc.).
3. Unscrew any retention screws that fasten the board to the enclosure.
4. The board should be in a "safe" state to be removed or data may be lost. Signal the system that a board is about to be removed by partially unlatching the ejectors on the board to be removed. Do not fully open the ejectors, as this levers the board out of the enclosure and prematurely breaks its backplane connection.
5. Wait for the blue hot swap LED on the board's faceplate to light; this indicates that board processes have finished and the board is safe to extract. If the hot swap LED fails

to light after 30 seconds, re-latch the ejectors and unlatch them again. In this case, the board is safe to extract (though the hot swap LED may not light).

6. Once the hot swap LED lights, open the injector/ejector mechanisms fully, rotating the handles outward until the board disengages from the backplane (refer to the "Injector/Ejector Operation" illustration).
7. Slide the board evenly out of the enclosure.
8. Install a replacement board or cover the empty slot with a filler panel to maintain the enclosure's shielding and cooling performance.

Removing a Rear Panel I/O Board

These instructions cover the mechanical aspects of removing an Intel NetStructure Rear Panel I/O (RPIO) board from a ZT 5090 system. RPIO boards may be installed at the rear of the ZT 5090 system in slots 1-8.

1. Shut down system operations and move the standby power switch to the standby (⏻) position.
2. Disconnect connections at the RPIO's faceplate.
3. Unscrew the retention screws that fasten the board to the enclosure.
4. Open the injector/ejector mechanisms, rotating the handles outward until the board disengages from the backplane (refer to the "Injector/Ejector Operation" illustration).
5. Begin to slide the board evenly out of the enclosure.
6. Before pulling the board out entirely, check for internal cabling attached to the board that may become snagged or that needs to be disconnected before the board can be fully removed.
7. Detach internal cables if necessary.
8. Remove the board from the enclosure.
9. Install a replacement board or cover the empty slot with a filler panel to maintain the enclosure's shielding and cooling performance.

Installing a Rear Panel I/O Board

These instructions cover the mechanical aspects of installing an Intel NetStructure Rear Panel I/O (RPIO) board. RPIO boards may be installed at the rear of the ZT 5090 system in slots 1-8.

1. Shut down system operations and move the standby power switch to the standby (⏻) position.
2. Choose an appropriate slot for the RPIO board. RPIO boards must be installed in-line behind their companion processor boards. For instance, if the System Master is installed in slot 3, it's RPIO board must be installed at the back of the system in slot 3.
3. Prepare the board by opening the injector/ejector mechanisms (refer to the "Injector/Ejector Operation" illustration).

4. Connect any internal system cabling, such as an IDE device, to the appropriate headers on the PCB. Route the cabling so that it doesn't become snagged or kinked when the board is inserted.
5. Carefully align the edges of the board with the left and right card guides in the appropriate slot. It may be helpful to look into the enclosure to verify correct alignment of the rails in the guides.
6. Taking care to keep the board aligned in the guides, slide the board in until the injector/ejector mechanisms engage the retention bars.
7. Simultaneously push in the board and rotate the injector/ejector mechanisms to their closed positions (rotate inward) to seat the backplane connectors.
8. Make the desired connections at the faceplate and configure the board.

Working with Power Supplies

The ZT 5090 accommodates up to three 250W, CompactPCI, modular power supplies. The power supplies are load sharing, hot swappable, and plug directly into the backplane (see the "Power Supply Orientation" illustration for power supply location).

The number of power supplies needed in any given system depends on the load in that system. It is recommended that three power supplies be used in every ZT 5090.

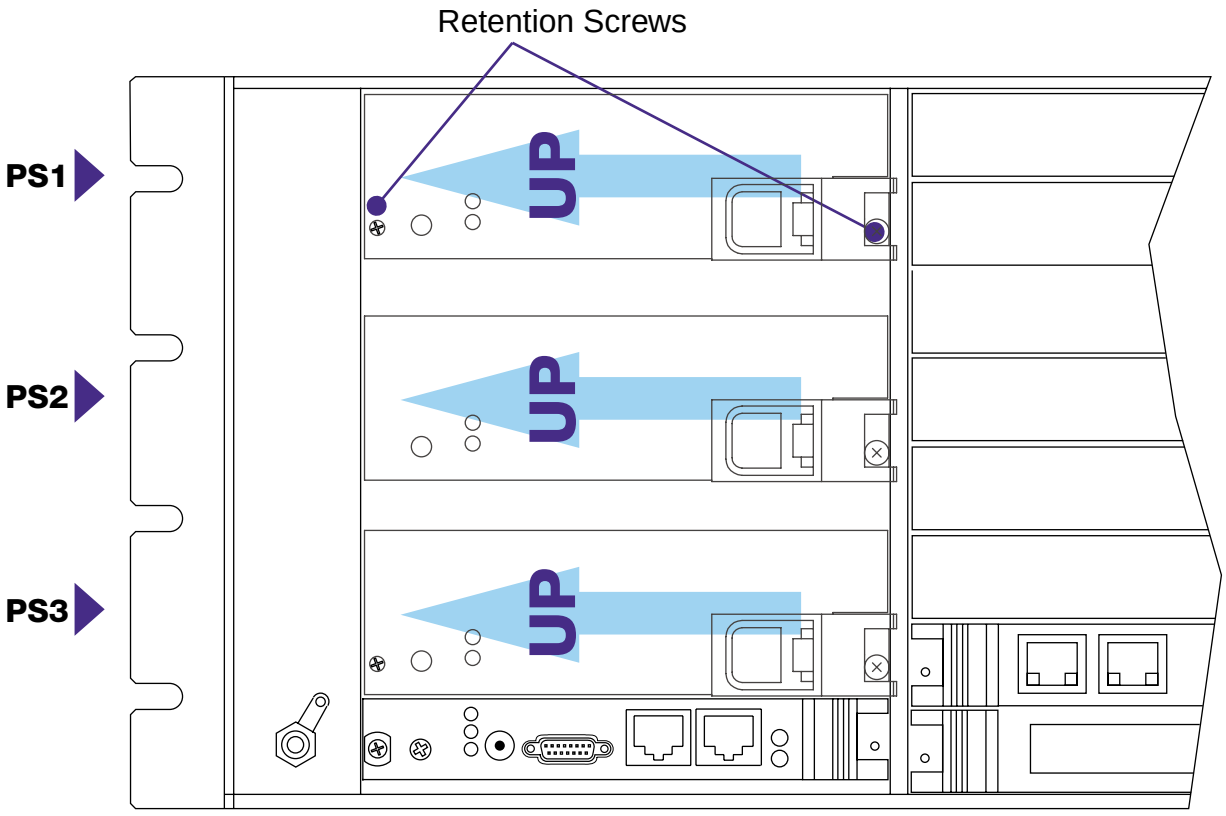
WARNING: The ZT 5090 is configured for either AC or DC input. The system's power input configuration (AC or DC) must match the power supply input voltage (AC or DC). **DO NOT INSTALL A DC INPUT POWER SUPPLY IN A ZT 5090 CONFIGURED FOR AC INPUT.**

WARNING: Power supply maintenance should only be performed by trained personnel. When the system is plugged in, high voltages are present on the backplane. Do not reach into the enclosure.

Installing a Power Supply

1. System power does not need to be off to install a power supply.
2. Select an empty power supply bay.
3. Align the rails on the power supply with the guides in the bay. It may be helpful to look into the enclosure to verify correct alignment of the rails in the guides.
4. Slide the power supply in the guides and press firmly to seat the connector. Refer to the "Injector/Ejector Operation (Power Supplies)" illustration.
5. Tighten the two retention screws on the front panel of the power supply. Refer to the "Power Supply Orientation" illustration for the location of power supply retention screws.

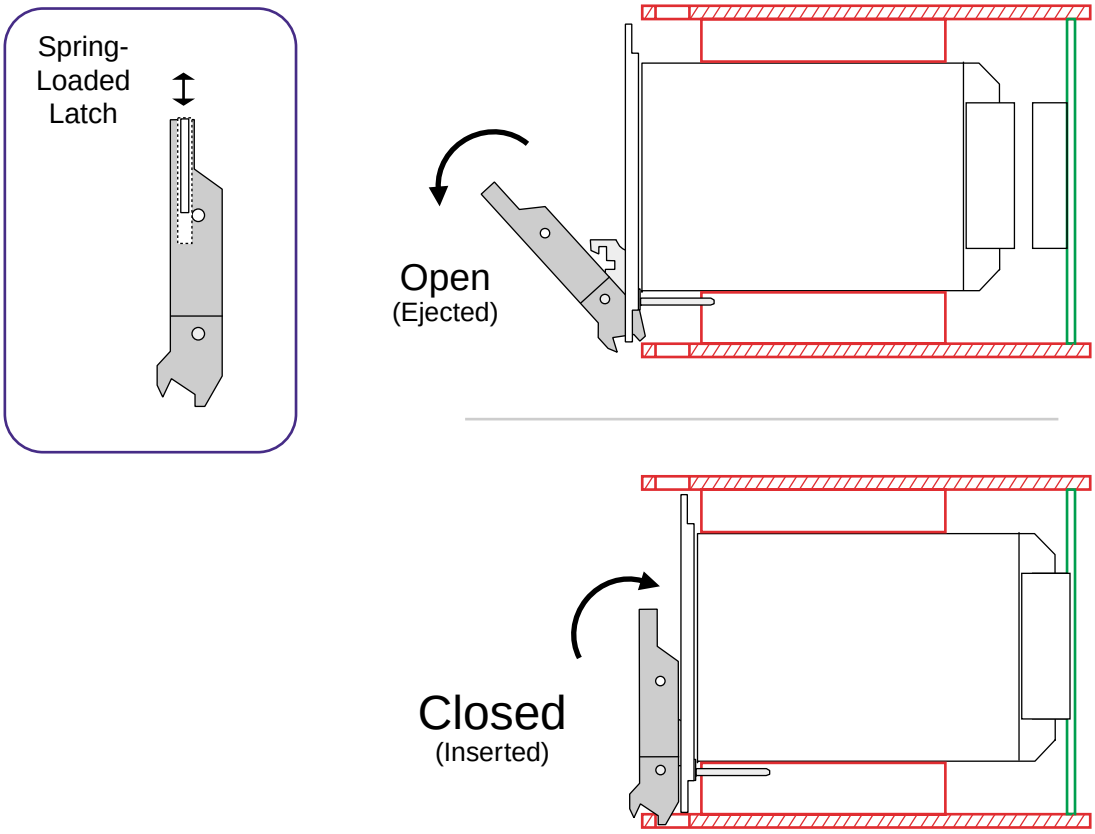
Power Supply Orientation



Removing a Power Supply

1. System power does not need to be off to remove a power supply.
2. Unscrew the two retention screws on the front of the power supply you wish to remove. Refer to the "Power Supply Orientation" illustration for the location of power supply retention screws.
3. Push down the spring-loaded latch on the ejector and rotate the ejector away from the power supply's faceplate. This levers the power supply away from the backplane. Refer to the "Injector/Ejector Operation (Power Supplies)" illustration.
4. Pull the power supply away from its backplane connection and slide it out of the enclosure.
5. Install a replacement power supply or cover the empty slot with a filler panel to maintain the enclosure's shielding and cooling performance.

Injector/Ejector Operation (Power Supplies)



Working with the Fan Tray

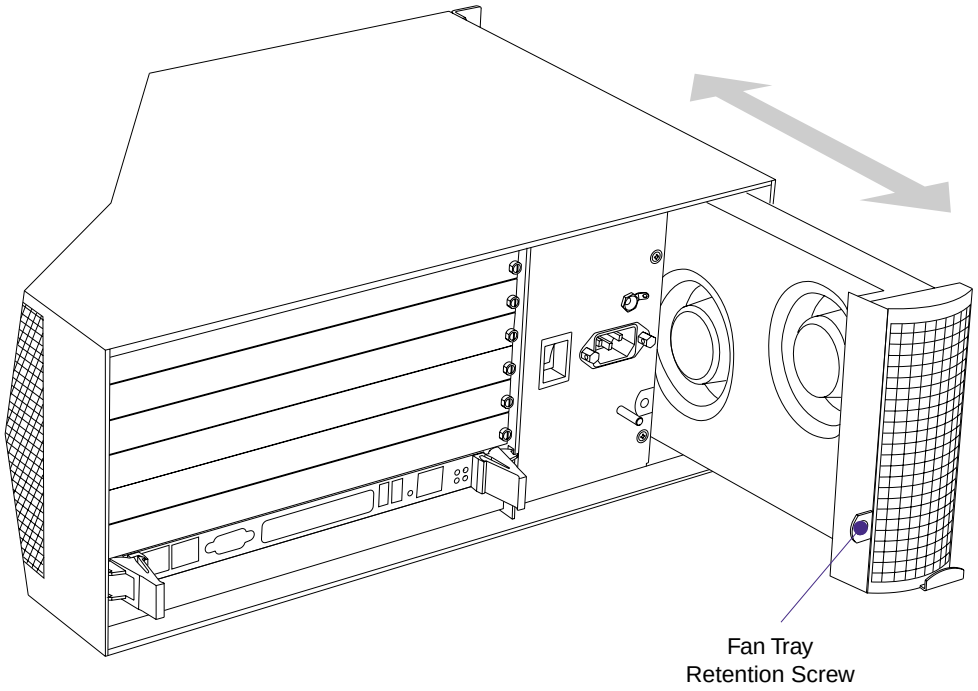
Two blowers housed in a removable fan tray occupy the right side of the enclosure (when viewed from the rear). The fan tray is secured by a captive screw and plugs into a blind mate receptacle in the enclosure (see the "Fan Tray Installation/Removal" illustration).

CAUTION: System cooling should not be absent for more than three minutes on an operating ZT 5090 system.

Removing the Fan Tray

1. A #2 Phillips screwdriver is required to remove the fan tray.
2. System power does not need to be turned off to remove the fan tray.
3. Loosen (turn counterclockwise) the captive retention screw on the fan tray grille until it releases the tray from the enclosure.
4. The grille and fan tray are one assembly. Use the handle at the bottom of the grille to pull the fan assembly out of the enclosure.
5. Perform the necessary maintenance or obtain a new fan tray.

Fan Tray Installation/Removal



Installing the Fan Tray

1. A #2 Phillips screwdriver is required to install the fan tray.
2. System power does not need to be turned off to install a fan tray.
3. The fan tray slides into the fan bay at the right rear of the enclosure. The fan tray should be oriented with the handle at the bottom.
4. Slide the fan tray into the enclosure.
5. Turn (clockwise) the captive screw to start the threads. When the threads engage properly, lightly tighten the screw.

A. Specifications

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 5090's enclosure and backplane. It includes a connector location illustration, connector descriptions, and connector pinouts.

Electrical Specifications

The ZT 5090's configuration options allow either an AC or DC power input panel.

AC input voltage:	100-230 VAC continuous, 50-60 Hz, 2.5-5.7A
DC input voltage:	36-75 VDC, 8-15A
Fan voltage:	12 VDC

WARNING: The ZT 5090 is configured for either AC or DC input. The system's power input configuration (AC or DC) must match the power supply input voltage (AC or DC). **DO NOT INSTALL A DC INPUT POWER SUPPLY IN A ZT 5090 CONFIGURED FOR AC INPUT.**

The following telecom voltages are bused through P4 connectors on slots 2, 4-6, and 8 (see the *CompactPCI Computer Telephony Specification, PICMG 2.5, Version 1.0* for more information):

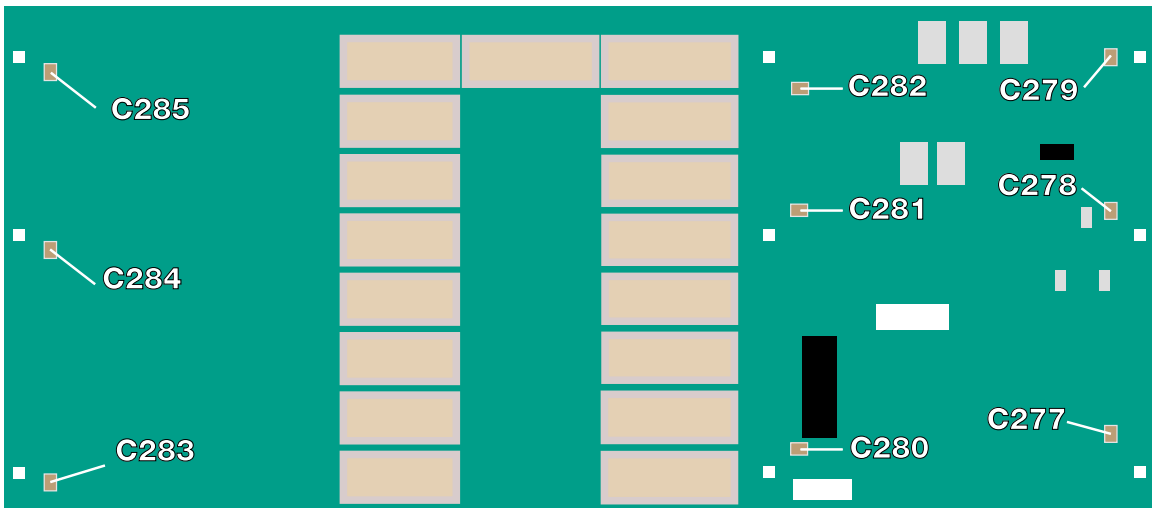
- **-Vbat** – telecom power source
- **-VbatRtn** – telecom power source return
- **-SELVbat** – short loop battery
- **-SELVbatRtn** – short loop battery return
- **VRG** – bused ringing voltage source
- **VRGRtn** – bused ringing voltage return

The ZT 5090 incorporates a universal backplane and can be jumpered to provide either 5V or 3.3V to the CompactPCI slots. See the "Setting V(I/O)" topic in Chapter 2 for information on changing V(I/O).

Logic Ground Isolation Capacitors

Logic ground can be isolated or connected to earth ground. Install capacitors C277-C285 on the rear of the backplane to isolate logic ground. Remove C277-C285 to tie logic ground to earth ground. See the "Logic Ground Isolation Capacitor Locations" figure.

Logic Ground Isolation Capacitor Locations



Environmental Specifications

The ZT 5090 platform (enclosure, fan tray, and backplane) is designed for harsh environments. The platform features sturdy steel and aluminum construction with a corrosion resistant finish.

- Min. Operating Temperature: 10° C
- Max. Operating Temperature: three power supplies, 400W total = 40° C
  three power supplies (n+1), 400W total = 25° C
  three power supplies (n+1), 280W total = 40° C
- Storage Temperature: -40° C to 66° C
- Non-Condensing Relative Humidity: 10% to 95%
- Cooling: 200LFM/slot
- Fan MTBF: 50,000 hrs (at 65º C)
- Operating Shock: 10 G per ASTM 0775
- Non-Operating Vibration: 5 to 300 Hz at 1.03 Gs
- Operating Vibration: 16 to 200 Hz at 0.25 G

Due to the modular construction of the system, components could be added that change the system's environmental constraints. Board-level components and power supply modules have their own operating temperature ratings. Refer to component-specific product manuals for operational details that may affect system performance.

Mechanical Specifications

The ZT 5090 is a 4U, 8-slot platform designed to fit standard 19" EIA racks. The system's mounting flanges may be positioned for front- or mid-mounting. The ZT 5090 accommodates IEEE 1101.10-compliant CompactPCI boards and IEEE1101.11-compliant rear panel I/O boards. The rear panel cards allow I/O connection to the rear of the enclosure using 80 mm deep, plug-in cards.

Chassis Dimensions:

Height: 6.94" (176 mm)

Width: 19.00" (483 mm), 17.20" (437 mm) excluding mounting flanges

Depth: 12.20" (310 mm)

Weight: 22 lbs. (10 kg) including chassis, backplane, and fan tray

Card slots are located on 0.8" (20.32 mm) centers.

The following topics provide connector information for the backplane.

Backplane Connectors and Devices

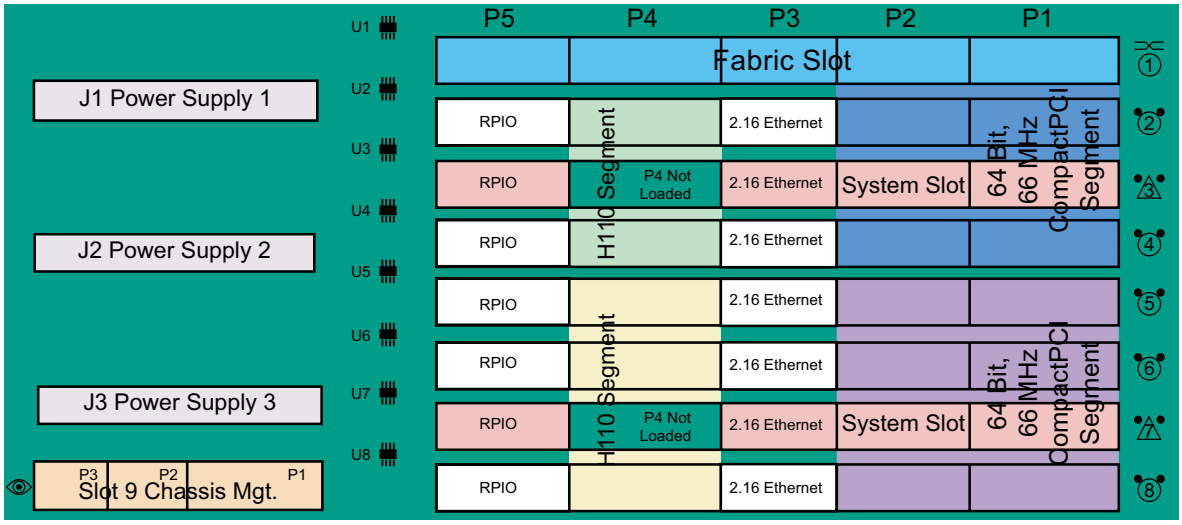
The ZT 5090 includes a hot swap-compatible 8-Slot CompactPCI backplane. The backplane is configured with a packet switched bus, two CompactPCI buses, and two H.110 TDM buses. Refer to the "Backplane Connector Locations (Front)" and "Backplane Connector Locations (Rear)" illustrations for connector locations.

Connector Assignments

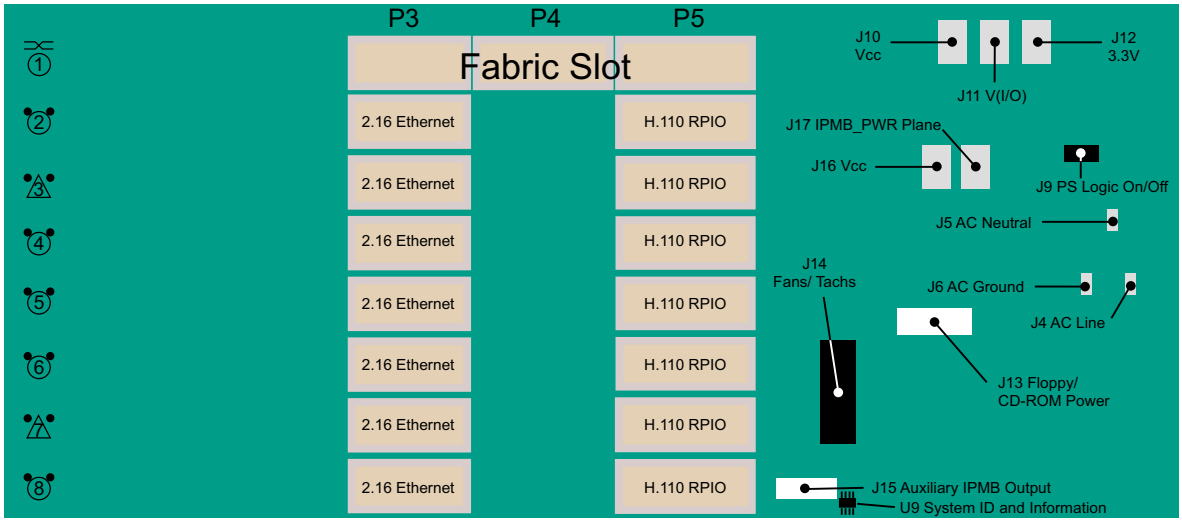
Connector	Function
P1-P5, Slot 1	PSB Fabric Interface (front)
P1-P5, Slots 3, 7	System Master Processor Board Interface (front)
P1-P5, Slots 2, 4-6, 8	Peripheral Board Interfaces (front)
P1-P3, Slot 9	Chassis Management Interface (front)
J1, J2, and J3	Modular Power Supply Connectors (front)
J4, J5, and J6	Power Spades (Rear)
J9	Power Supply Logic On/Off (rear)
J10, J11, and J12	V(I/O) Selection (rear)
J13	IDE/Floppy Drive Power Connector (rear)
J14	Fan Connector (rear)
J15	Auxiliary IPMB Output (rear)

Connector	Function
J16, J17	IPMB Power Plane (rear)
CT1-CT10	Shelf Enumeration (rear)
U1-U8	Temperature Sensors (front)
U9	System ID and Information (Rear)

Backplane Connector Locations (Front)



Backplane Connector Locations (Rear)



CompactPCI-Slot Connectors

Physical Slot	Logical Slot	Backplane Silkscreen	P1 Loading	P2 Loading	P3 Loading	P4 Loading	P5 Loading
Slot 1	4-A, Fabric	1APx	32-Bit	64-Bit	Fabric	Fabric	Fabric
Slot 2	2-A	2APx	32-Bit	64-Bit	Node	H.110	H.110 RPIO
Slot 3	1-A, System	3APx	32-Bit	64-Bit	Node	No	H.110 RPIO
Slot 4	3-A	4APx	32-Bit	64-Bit	Node	H.110	H.110 RPIO
Slot 5	3-B	5APx	32-Bit	64-Bit	Node	H.110	H.110 RPIO
Slot 6	2-B	6APx	32-Bit	64-Bit	Node	H.110	H.110 RPIO
Slot 7	1-B, System	7APx	32-Bit	64-Bit	Node	No	H.110 RPIO
Slot 8	4-B	8APx	32-Bit	64-Bit	Node	H.110	H.110 RPIO
Slot 9	—	9APx	CMM	CMM	CMM	No	No

32-Bit = 32-bit CompactPCI connector loaded
64-Bit = 64-bit CompactPCI connector loaded
Fabric = PICMG *2.16 PSB Fabric Slot connector*
Node = rows 14-19 provide links to fabric slot/all others available for RPIO
H.110 = ECTF H.110-compliant connector loaded
No = no connector loaded

Fabric Slot CompactPCI Connectors

On the front side of the backplane, slot 1 is reserved as the Fabric Slot. Slot 1 is compatible only with PICMG 2.16-compliant Ethernet switch boards. CompactPCI connectors are loaded in the P1-P5 locations at slot 1. See the "Backplane Connector Locations (Front)" illustration above for location information.

P1 at slot 1 is an un-keyed, 25-row CompactPCI connector. At slot 1, P1 buses between itself, 32-bit peripheral boards in slots 2 and 4, and P1 at the upper System Slot (slot 3). See the "P1 (at Slots 1-8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the *CompactPCI Hot Swap Specification, PICMG 2.1, R1.0* for more information.

P2 is an un-keyed, 22-row CompactPCI connector. At slot 1, P2 buses between itself, 64-bit peripheral cards in slots 2 and 4, and P2 at the upper System Slot (slot 3). Refer to the "P2 (at Slots 1-8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the *CompactPCI Specification, PICMG 2.0, R3.0* for more information.

P3 is an un-keyed, 19-row Standard Fabric Board CompactPCI connector. At slot 1, P3 provides links to Node boards in slots 5-8. Refer to the "P3 (at Slot 1) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the PICMG *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, R1.0* for more information.

P4 is a Lilac Blue keyed, 25-row Standard Fabric Board CompactPCI connector. Refer to the "P4 (at Slot 1) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the PICMG *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, R1.0* for more information.

P5 is an un-keyed, 22-row Standard Fabric Board CompactPCI connector. At slot 1, P5 provides links to Node boards in slots 2-4. See the "P5 (at Slot 1) CompactPCI Backplane Connector Pinout" table for pin information. Refer to the *CompactPCI Computer Telephony Specification, PICMG 2.5, R1.0* for more information.

P1 (at Slots 1- 8) CompactPCI 2.16 Backplane Connector Pinout

Pin#	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O) *(L)*	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V *(L)*	AD[2]	GND
22	GND	AD[7]	GND	3.3V *(L)*	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND *(L)*	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND *(L)*	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL# *(S)*	TRDY#	GND
14							
13			KEY	AREA			
12							
11	GND	AD[18]	AD[17]	AD[16]	GND *(L)*	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL *(S)*	AD[23]	GND *(L)*	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND *(L)*	AD[27]	GND
6	GND	REQ#	GND	3.3V *(L)*	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	PCI_RST#	GND *(L)*	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O) *(L)*	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V *(L)*	INTD#	GND
2	GND	TCK*	5V	TMS*	TDO*	TDI*	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Notes:

A color-coded (for V I/O) key plug occupies the KEY AREA—Brilliant Blue for 5V, Cadmium Yellow for 3.3V.

Designates a low true signal.

* Designates signals NOT bused

Pins are medium (Level 2) length except as follows:

(S) designates a short (Level 1) pin length.

(L) designates a long (Level 3) pin length.

Columns Z and F contain long (Level 3) pins.

P2 (at Slots 1- 8) CompactPCI Backplane Connector Pinout

Pin#	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	NC	GND	NC	NC	NC	GND
20	GND	NC	NC	NC	GND	NC	GND
19	GND	NC	GND	NC	NC	NC	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	NC	NC	NC	GND
16	GND	BRSVP2A16	BRSVP2B16	NC	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	NC	NC	NC	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	64EN#	V(I/O)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

Notes:

Designates a low true signal.

NC = No Connection

P3 (at Slot 1) CompactPCI 2.16 Fabric Slot Backplane Connector Pinout

Pin #	Z	A	B	C	D	E	F
19	GND	SGA4	SGA3	SGA2	SGA1	SGA0	GND
18	GND	LPf_DA+	LPf_DA-	GND	LPf_DC+	LPf_DC-	GND
17	GND	LPf_DB+	LPf_DB-	GND	LPf_DD+	LPf_DD-	GND
16	GND	LP8_DA+	LP8_DA-	GND	LP8_DC+	LP8_DC-	GND
15	GND	LP8_DB+	LP8_DB-	GND	LP8_DD+	LP8_DD-	GND
14	GND	LP7_DA+	LP7_DA-	GND	LP7_DC+	LP7_DC-	GND
13	GND	LP7_DB+	LP7_DB-	GND	LP7_DD+	LP7_DD-	GND
12	GND	LP6_DA+	LP6_DA-	GND	LP6_DC+	LP6_DC-	GND
11	GND	LP6_DB+	LP6_DB-	GND	LP6_DD+	LP6_DD-	GND
10	GND	LP5_DA+	LP5_DA-	GND	LP5_DC+	LP5_DC-	GND
9	GND	LP5_DB+	LP5_DB-	GND	LP5_DD+	LP5_DD-	GND
8	GND	LP4_DA+	LP4_DA-	GND	LP4_DC+	LP4_DC-	GND
7	GND	LP4_DB+	LP4_DB-	GND	LP4_DD+	LP4_DD-	GND
6	GND	LP3_DA+	LP3_DA-	GND	LP3_DC+	LP3_DC-	GND
5	GND	LP3_DB+	LP3_DB-	GND	LP3_DD+	LP3_DD-	GND
4	GND	LP2_DA+	LP2_DA-	GND	LP2_DC+	LP2_DC-	GND
3	GND	LP2_DB+	LP2_DB-	GND	LP2_DD+	LP2_DD-	GND
2	GND	LP1_DA+	LP1_DA-	GND	LP1_DC+	LP1_DC-	GND
1	GND	LP1_DB+	LP1_DB-	GND	LP1_DD+	LP1_DD-	GND

P4 (at Slot 1) CompactPCI 2.16 Fabric Slot Backplane Connector Pinout

Pin #	Z	A	B	C	D	E	F
25	GND	LP20_DA+	LP20_DA-	GND	LP20_DC+	LP20_DC-	GND
24	GND	LP20_DB+	LP20_DB-	GND	LP20_DD+	LP20_DD-	GND
23	GND	LP21_DA+	LP21_DA-	GND	LP21_DC+	LP21_DC-	GND
22	GND	LP21_DB+	LP21_DB-	GND	LP21_DD+	LP21_DD-	GND
21	GND	LP22_DA+	LP22_DA-	GND	LP22_DC+	LP22_DC-	GND
20	GND	LP22_DB+	LP22_DB-	GND	LP22_DD+	LP22_DD-	GND
19	GND	LP23_DA+	LP23_DA-	GND	LP23_DC+	LP23_DC-	GND
18	GND	LP23_DB+	LP23_DB-	GND	LP23_DD+	LP23_DD-	GND
17	GND	LP24_DA+	LP24_DA-	GND	LP24_DC+	LP24_DC-	GND
16	GND	LP24_DB+	LP24_DB-	GND	LP24_DD+	LP24_DD-	GND
15	GND	LPm_TX+	LPm_TX-	GND	LPm_RX+	LPm_RX-	GND
14	GND						GND
13	GND			KEY AREA			GND
12	GND						GND
11	GND	5V	5V	GND	3.3V	3.3V	GND
10	GND	RTS	CTS	TXD	RXD	SMBD	GND
9	GND	PWRGD	PWRGD	IPMB_PWR	SMBA	SMBC	GND
8	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND
7	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND
6	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND
5	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND
4	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND
3	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND
2	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND
1	GND	RESRVD	RESRVD	RESRVD	RESRVD	RESRVD	GND

Notes:

Fabric Slot key colors: Lilac Blue = Standard Fabric, Ochre Yellow = Extended Fabric

P5 (at Slot 1) CompactPCI 2.16 Fabric Slot Backplane Connector Pinout

Pin #	Z	A	B	C	D	E	F
22	GND	LP19_DA+	LP19_DA-	GND	LP19_DC+	LP19_DC-	GND
21	GND	LP19_DB+	LP19_DB-	GND	LP19_DD+	LP19_DD-	GND
20	GND	LP18_DA+	LP18_DA-	GND	LP18_DC+	LP18_DC-	GND
19	GND	LP18_DB+	LP18_DB-	GND	LP18_DD+	LP18_DD-	GND
18	GND	LP17_DA+	LP17_DA-	GND	LP17_DC+	LP17_DC-	GND
17	GND	LP17_DB+	LP17_DB-	GND	LP17_DD+	LP17_DD-	GND
16	GND	LP16_DA+	LP16_DA-	GND	LP16_DC+	LP16_DC-	GND
15	GND	LP16_DB+	LP16_DB-	GND	LP16_DD+	LP16_DD-	GND
14	GND	LP15_DA+	LP15_DA-	GND	LP15_DC+	LP15_DC-	GND
13	GND	LP15_DB+	LP15_DB-	GND	LP15_DD+	LP15_DD-	GND
12	GND	LP14_DA+	LP14_DA-	GND	LP14_DC+	LP14_DC-	GND
11	GND	LP14_DB+	LP14_DB-	GND	LP14_DD+	LP14_DD-	GND
10	GND	LP13_DA+	LP13_DA-	GND	LP13_DC+	LP13_DC-	GND
9	GND	LP13_DB+	LP13_DB-	GND	LP13_DD+	LP13_DD-	GND
8	GND	LP12_DA+	LP12_DA-	GND	LP12_DC+	LP12_DC-	GND
7	GND	LP12_DB+	LP12_DB-	GND	LP12_DD+	LP12_DD-	GND
6	GND	LP11_DA+	LP11_DA-	GND	LP11_DC+	LP11_DC-	GND
5	GND	LP11_DB+	LP11_DB-	GND	LP11_DD+	LP11_DD-	GND
4	GND	LP10_DA+	LP10_DA-	GND	LP10_DC+	LP10_DC-	GND
3	GND	LP10_DB+	LP10_DB-	GND	LP10_DD+	LP10_DD-	GND
2	GND	LP9_DA+	LP9_DA-	GND	LP9_DC+	LP9_DC-	GND
1	GND	LP9_DB+	LP9_DB-	GND	LP9_DD+	LP9_DD-	GND

System Slot CompactPCI Connectors

On the front side of the backplane, slots 3 and 7 are reserved as System Slots. CompactPCI connectors are loaded in the P1-P3 and P5 locations at slots 3 and 7. See the "Backplane Connector Locations (Front)" illustration above for location information.

P1 at slots 3 and 7 is a Brilliant Blue keyed for 5V operation, 25-row connector providing 32-bit CompactPCI busing between the System processors and the P1 connectors loaded at peripheral slots 2, 4-6, and 8. Refer to the "P1 (at Slots 1-8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the *CompactPCI Hot Swap Specification, PICMG 2.1, R1.0* for more information.

P2 at slots 3 and 7 is an un-keyed, 22-row connector providing 64-bit CompactPCI busing between the System processors and the P2 connectors loaded at peripheral slots 2, 4-6, and 8. Refer to the "P2 (at Slots 1-8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the PICMG *CompactPCI Specification, PICMG 2.0, R3.0* for more information.

P3 at slots 3 and 7 is an un-keyed, 19-row CompactPCI connector with signals on rows 14-19 providing links to the fabric slot and all other pins available for customer-defined I/O. Refer to the "P3 (at Slots 2-8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the PICMG *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, R0* for more information.

P4 at slots 3 and 7 is not loaded.

P5 at slots 3 and 7 is an un-keyed 22-row CompactPCI connector that is not bused. The connector’s "Z" and "F" columns are grounded and all other pins are available for customer-defined I/O.

P3 (at Slots 2-8) CompactPCI Connector Pinout

Pin#	Z	A	B	C	D	E	F
19	GND	ISO*	ISO*	ISO*	ISO*	ISO*	GND
18	GND	LPa_DA+	LPa_A-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPb_DA+	LPb_A-	GND	LPb_DC+	LPb_DC-	GND
15	GND	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
4	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
3	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
2	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
1	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND

Notes:

* = Used for Isolation

ISO row (row 19, pins A-E) may be at logic ground or may be at earth ground. A removable bypass capacitor to ground selects this option, as defined in the 2.16 specification. Refer to the “Logic Ground Isolation Capacitors” topic.

Peripheral Slot CompactPCI Connectors

On the front side of the backplane, slots 2, 4-6, and 8 are reserved for peripheral boards. CompactPCI connectors are loaded in the P1-P5 locations at slots 2, 4-6, and 8. See the "Backplane Connector Locations (Front)" illustration for location information.

P1 is a Brilliant Blue keyed for 5V operation, 25-row CompactPCI connector. At slots 1, 2, and 4, P1 buses between 32-bit peripheral boards and P1 at the upper system slot (slot 3). At slots 5, 6, and 8, P1 buses between 32-bit peripheral boards and P1 at the lower system slot (slot 7). See the "P1 (at Slots 1-8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the *CompactPCI Hot Swap Specification, PICMG 2.1, R1.0* for more information. Doesn't this really bus between slots 1-4 and also 5-8? Not

P2 is an un-keyed, 22-row CompactPCI connector. At slots 1, 2, and 4, P2 buses between 64-bit peripheral cards and P2 at the upper system slot (slot 3). At slots 5, 6, and 8, P2 buses between 64-bit peripheral cards and P2 at the lower System Slot (slot 7). Refer to the "P2 (at Slots 1-8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the *CompactPCI Specification, PICMG 2.0, R3.0* for more information.

P3 is an un-keyed, 19-row, CompactPCI node board Ethernet connector. At slots 2-4, P3 provides links to P5 at fabric slot 1. At slots 5-8, P3 provides links to P3 at fabric slot 1. P3 at slots 2, 4-6, and 8 also provides pins for through-backplane user-definable I/O. Refer to the "P3 (at Slots 2, 4-6, and 8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the PICMG *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, R1.0* for more information.

P4 at slots 2,4-6, and 8 is a Strawberry Red keyed, 25-row CompactPCI connector providing telephony signal busing among peripheral slots in the same CompactPCI bus segment. P4 at slots 2 and 4 route H.110 signals between each other. P4 at slots 5, 6 and 8 route H.110 signals between each other. Refer to the "P4 (at Slots 2, 4-6, and 8) CompactPCI Backplane Connector Pinout" table for pin definitions. Refer to the *CompactPCI Computer Telephony Specification, PICMG 2.5, R1.0* for more information.

P5 is an un-keyed, 22-row CompactPCI connector with staged pins for hot swap. The pins are specified for H.110 RPIO or through-backplane user-definable I/O. The backplane surrounding the P5 connectors is devoid of power planes, ground planes, and other signal routing on the inner and surface layers. See the "P5 (at Slots 2, 4-6, and 8) CompactPCI Backplane Connector Pin Staging" table for pin information. Refer to the *CompactPCI Computer Telephony Specification, PICMG 2.5, R1.0* for more information.

P3 (at Slots 2, 4-6, and 8) CompactPCI Backplane Connector Pinout

Pin #	Z	A	B	C	D	E	F
19	GND	ISO*	ISO*	ISO*	ISO*	ISO*	GND
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
15	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
4	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
3	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
2	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
1	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND

Notes:

* = Used for Isolation

ISO row (row 19, pins A-E) may be at logic ground or may be at earth ground. A removable bypass capacitor to ground selects this option, as defined in the 2.16 specification. Refer to the “Logic Ground Isolation Capacitors” topic.

P4 (at Slots 2, 4-6, and 8) CompactPCI Backplane Connector Pinout

Pin#	Z	A	B	C	D	E	F
25	NP	SGA4	SGA3	SGA2	SGA1	SGA0	FGND
24	NP	GA4	GA3	GA2	GA1	GA0	FGND
23	NP	+12V	/CT_Reset	/CT_EN *(S)*	-12V	CT_MC	FGND
22	NP	PFS0#	RSV	RSV	RSV	RSV	FGND
21	NP	-SELVbat *(L)*	PFS1#	RSV	RSV	-SELVbatRtn *(L)*	FGND
20	NP	NP	NP	NP	NP	NP	NP
19	NP	NP	NP	NP	NP	NP	NP
18	NP	VRG	NP	NP	NP	VRGRtn	NP
17	NP	NP	NP	NP	NP	NP	NP
16	NP	NP	NP	NP	NP	NP	NP
15	NP	-Vbat *(L)*	NP	NP	NP	-VbatRtn *(L)*	NP
14							
13			KEY AREA				
12							
11	NP	CT_D29	CT_D30	CT_D31	V(I/O) *(L)*	/CT_FRAME_A	GND
10	NP	CT_D27	+3.3V	CT_D28	+5V *(L)*	/CT_FRAME_B	GND
9	NP	CT_D24	CT_D25	CT_D26	GND *(L)*	/FR_COMP	GND
8	NP	CT_D21	CT_D22	CT_D23	+5V *(L)*	CT_C8_A	GND
7	NP	CT_D19	+5V	CT_D20	GND *(L)*	CT_C8_B	GND
6	NP	CT_D16	CT_D17	CT_D18	GND *(L)*	CT_NETREF_1	GND
5	NP	CT_D13	CT_D14	CT_D15	+3.3V *(L)*	CT_NETREF_2	GND
4	NP	CT_D11	+5V	CT_D12	+3.3V *(L)*	SCLK	GND
3	NP	CT_D8	CT_D9	CT_D10	GND *(L)*	SCLKx2	GND
2	NP	CT_D4	CT_D5	CT_D6	CT_D7	GND *(L)*	GND
1	NP	CT_D0	+3.3V	CT_D1	CT_D2	CT_D3	GND

Notes:

Designates a low true signal.

Pins are medium (Level 2) length except as follows:

(S) designates a short (Level 1) pin length.

(L) designates a long (Level 3) pin length.

Column F contains long (Level 3) pins.

P5 (at Slots 2, 4-6, and 8) H.110 Backplane Connector Pin Staging

Pin#	Z	A	B	C	D	E	F
22	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
21	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
20	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
19	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
18	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
17	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
16	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
15	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
14	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
13	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
12	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
11	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
10	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
9	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
8	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
7	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
6	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
5	NH	*(S)*	*(S)*	*(S)*	*(S)*	*(S)*	GND *(L)*
4	NH	*(M)*	*(M)*	*(M)*	*(M)*	*(M)*	GND *(L)*
3	NH	*(M)*	*(M)*	*(M)*	*(M)*	*(M)*	GND *(L)*
2	NH	*(M)*	*(M)*	*(M)*	*(M)*	*(M)*	GND *(L)*
1	NH	*(M)*	*(M)*	*(M)*	*(M)*	*(M)*	GND *(L)*

Notes:

Rows “A” through “E” pins 1-22 are open for user definition.

NH designates no hole in backplane.

(S) designates a short (Level 1) pin length.

(M) designates a medium (Level 2) pin length.

(L) designates a long (Level 3) pin length.

Chassis Management CompactPCI Connectors

On the front side of the backplane, slot 9 is reserved for the Chassis Management Module (CMM). P1, P2, and P3 connectors are loaded at slot 9 and are routed to assorted pins across the backplane. See the following P1, P2, and P3 pinout tables for pin definitions. See the "Backplane Connector Locations (Front)" illustration for location information.

P1 (at Slot 9) CompactPCI Backplane Connector

Pin #	Z	A	B	C	D	E	F
22	GND	PDEG0#	PDEG2#	GND	PDEG4#	PDEG6#	GND
21	GND	PDEG1#	PDEG3#	IPMB_PWR	PDEG5#	PDEG7#	GND
20	GND	PFAIL0#	PFAIL2#	GND	PFAIL4#	PFAIL6#	GND
19	GND	PFAIL1#	PFAIL3#	IPMB_PWR	PFAIL5#	PFAIL7#	GND
18	GND	PINH0#	PINH2#	GND	PINH4#	PINH6#	GND
17	GND	PINH1#	PINH3#	IPMB_PWR	PINH5#	PINH7#	GND
16	GND	PS_SCL0	PS_SDA0	GND	PRESI#	GA0	GND
15	GND	PS_SCL1	PS_SDA1	RES	FANP0#	FANP2#	GND
14	GND	FT_SCL	FT_SDA	GND	FANP1#	FANP3#	GND
13	GND	CS_SCL	CS_SDA	RES	FANPWM0	FANPWM2	GND
12	GND	CF_SCL0	CF_SDA0	GND	FANPWM1	FANPWM3	GND
11	GND	CF_SCL1	CF_SDA1	RES	FANTK0	FANTK8	GND
10	GND	PI_SCL	PI_SDA	GND	FANTK1	FANTK9	GND
9	GND	AC_SCL	AC_SDA	RES	FANTK2	FANTK10	GND
8	GND	STx	SRx	SRI	FANTK3	FANTK11	GND
7	GND	SCTS	SRTS	SCD	FANTK4	FANTK12	GND
6	GND	SDSR	SDTR	RES	FANTK5	FANTK13	GND
5	GND	RPMAC#	RPMIC#	RES	FANTK6	FANTK14	GND
4	GND	RPCR#	RPMAR#	RPMIR#	FANTK7	FANTK15	GND
3	GND	BP_5V	BP_N12V	BP_12V	BP_3.3V	VIO	GND
2	GND	SwTx+	SwTx-	GND	RpTx+	RpTx-	GND
1	GND	SwRx+	SwRx-	GND	RpRx+	RpRx-	GND

Note: # Designates a low true signal.

P2 (at Slot 9) Connector Pinout

Pin #	Z	A	B	C	D	E	F
11	GND	N_SCL0	N_SDA0	N_SCL9	N_SDA9	N_SCL17	GND
10	GND	N_SCL1	N_SDA1	N_SCL10	N_SDA10	N_SDA17	GND
9	GND	N_SCL2	N_SDA2	N_SCL11	N_SDA11	N_SCL18	GND
8	GND	N_SCL3	N_SDA3	N_SCL12	N_SDA12	N_SDA18	GND
7	GND	N_SCL4	N_SDA4	N_SCL13	N_SDA13	N_SCL19	GND
6	GND	N_SCL5	N_SDA5	N_SCL14	N_SDA14	N_SDA19	GND
5	GND	N_SCL6	N_SDA6	N_SCL15	N_SDA15	N_SCL20	GND
4	GND	N_SCL7	N_SDA7	N_SCL16	N_SDA16	N_SDA20	GND
3	GND	N_SCL8	N_SDA8	GND *(L)*	NGO	HLY#	GND
2	GND	R_SCL	IPMB_PWR	RES	IPMB_PWR *(L)*	HLYI#	GND
1	GND	GND *(L)*	R_SDA	BD_SEL# *(S)*	NGOI	GND *(L)*	GND

Notes:

Designates a low true signal.

Pins are medium (Level 2) length except as follows:

(S) designates a short (Level 1) pin length.

(L) designates a long (Level 3) pin length.

P3 (at Slot 9) Connector Pinout

Pin #	Z	A	B	C	D	E	F
11	GND	N_HLY0#	N_BDS0#	N_HLY9#	N_BDS9#	N_HLY17#	GND
10	GND	N_HLY1#	N_BDS1#	N_HLY10#	N_BDS10#	N_BDS17#	GND
9	GND	N_HLY2#	N_BDS2#	N_HLY11#	N_BDS11#	N_HLY18#	GND
8	GND	N_HLY3#	N_BDS3#	N_HLY12#	N_BDS12#	N_BDS18#	GND
7	GND	N_HLY4#	N_BDS4#	N_HLY13#	N_BDS13#	N_HLY19#	GND
6	GND	N_HLY5#	N_BDS5#	N_HLY14#	N_BDS14#	N_BDS19#	GND
5	GND	N_HLY6#	N_BDS6#	N_HLY15#	N_BDS15#	N_HLY20#	GND
4	GND	N_HLY7#	N_BDS7#	N_HLY16#	N_BDS16#	N_BDS20#	GND
3	GND	N_HLY8#	N_BDS8#	IPMB_PWR	PIMP0#	ACCMP#	GND
2	GND	PIMH0	GND	RES	GND	RES	GND
1	GND	IPMB_PWR	PIMH1	PRES#	PIMP1#	IPMB_PWR	GND

Note: # Designates a low true signal.

J1, J2, and J3 Power Supply Connectors

J1, J2, and J3 are 47-pin modular power supply connectors. Up to three AC or DC input, 200W power supplies can be plugged into the front side of the ZT 5090's backplane. See the following "J1, J2, and J3 Power Supply Connector Pinout" table for pin definitions. See the "Backplane Connector Locations (Front)" illustration for location information.

WARNING: The ZT 5090 is configured for either AC or DC input. The system's power input configuration (AC or DC) must match the power supply input voltage (AC or DC). **DO NOT INSTALL A DC INPUT POWER SUPPLY IN A ZT 5090 CONFIGURED FOR AC INPUT.**

J1, J2, and J3 Power Supply Connector Pinout

Pin#	Staging	Name	Function
1-4	M	V1	V1 Output (VCC, +5V)
5-12	M	RTN	V1 and V2 Return (GND)
13-18	M	V2	V2 Output (+3.3V)
19	M	RTN	V3 Return (GND)
20	M	V3	V3 Output (+12V)
21	M	V4	V4 Output (-12V)
22	M	RTN	Signal Return (GND)
23	M	RSV	Reserved
24	M	RTN	V4 Return (GND)
25	M	GA0	Geographic Address Bit 0
26	M	RSV	Reserved
27	S	EN#	Enable (Grounded)
28	M	GA1	Geographic Address Bit 1
29	M	V1ADJ	V1 Adjust
30	M	V1 SENSE	V1 Remote Sense
31	M	GA2	Geographic Address Bit 2
32	M	V2ADJ	V2 Adjust
33	M	V2 SENSE	V2 Remote Sense
34	M	S RTN	Sense Return
35	M	V1 SHARE	V1 Current Share
36	M	V3 SENSE	V3 Remote Sense
37	M	IPMB_SCL	Reserved for System Management Bus
38	M	DEG#	Degrade Signal
39	M	INH#	Inhibit (to Logic Power Switch)
40	M	IPMB_SDA	Reserved for System Management Bus
41	M	V2 SHARE	V2 Current Share
42	M	FAL#	Fail Signal
43	M	IPMB_PWR	Reserved for System Management Bus
44	M	V3 SHARE	V3 Current Share
45	L	CGND	Chassis Ground (safety ground)
46	M	ACN/+DC IN	AC Input – Neutral; +DC Input
47	M	ACL/-DC IN	AC Input – Line; -DC Input

Note: L designates a "long length" pin; M designates a "medium length" pin; S designates a "short length" pin.

J4, J5, and J6 Power Spades

These spade connectors, located on the rear of the backplane, allow connection of external power to the system power supplies. They supply line-level AC to the system power supplies if the external power source is AC, and line-level DC if the external power source is DC.

See the following "J4, J5, and J6 Power Spades" table for pin definitions. See the "Backplane Connector Locations (Rear)" illustration for location information.

J4, J5, and J6 Power Spades

Connector	Function
J4	AC/DC Line
J5	AC/DC Neutral
J6	Earth Ground

J9 Power Supply Logic On/Off

This 2-pin connector, located on the rear of the backplane, grounds the EN# signal for power supply connectors J1-J3. A wire attached to J9 leads to a switch on the rear of the system that “logically” turns the power supplies on and off.

See the "Backplane Connector Locations (Rear)" illustration for location information.

J10, J11, and J12 V(I/O) Selection

The ZT 5090 can be configured for use with 5 V or 3.3 V CompactPCI cards. On the rear of the backplane, three screw-down terminals determine V(I/O) for the CompactPCI connectors. See the "Backplane Connector Locations (Rear)" illustration for location information.

- For 5V operation (default setting), connect terminals J10 and J11 with the jumper/bus bar; J12 is not connected.
- For 3.3 V operation, connect terminals J11 and J12 with the jumper/bus bar; J10 is not connected.

See the "Setting V(I/O)" topic for additional location and setup information.

Be aware that CompactPCI connectors may be keyed for use in either 5 V or 3.3 V systems. A 3.3V board (with a yellow key) will not insert into a 5 V backplane (with a blue key). Since the ZT 5090’s backplane is configured for use with 5 V boards, the jumper *and* the CompactPCI keys must be changed for 3.3 V use.

J13 IDE/Floppy Drive Power Connector

The ZT 5090 system includes a power connector for an external IDE device, such as a CD-ROM drive, or a floppy drive. The device's power cable is connected to J13 at the rear of the backplane. See the following "J13 IDE/Floppy Drive Power Connector Pinout" table for pin definitions. See the "Backplane Connector Locations (Rear)" illustration for location information.

J13 IDE/Floppy Drive Power Connector Pinout

Pin#	Name
1	+12V
2	GND
3	GND
4	Vcc

J14 Fan Connector

The ZT 5090 system features an integrated fan tray. The fans (blowers) are cabled to connector J14 at the rear of the backplane. See the following "J14 Fan Connector Pinout" table for pin definitions. See the "Backplane Connector Locations (Rear)" illustration for location information.

J14 Fan Connector Pinout

Pin#	Name	Pin#	Name
1	FAN0	2	FAN3
3	FAN1	4	FAN4
5	FAN2	6	FAN5
7	12V	8	12V
9	12V	10	FANTRAYIN
11	GND	12	GND
13	GND	14	GND

J15 Auxiliary IPMB Signal Output

The ZT 5090 system makes IPMB power and signals available at connector J15 at the rear of the backplane. See the following "J15 Auxiliary IPMB Output Pinout" table for pin definitions. See the "Backplane Connector Locations (Rear)" illustration for location information.

J15 Auxiliary IPMB Output Pinout

Pin#	Name
1	PI_SCL
2	GND
3	PI_SDA
4	IPMB_PWR
5	NC

J16 and J17 IPMB Power Plane

The ZT 5090 is configured to provide IPMB power for the CMM. On the rear of the backplane, two screw-down terminals allow the IPMB power plane to be strapped to VCC. Set for 5V IPMB operation (default setting) as follows:

Connect terminals J16 and J17 with the jumper/bus bar ***or*** remove the jumper/bus bar from terminals J16 and J17 and connect a remote IPMB power source to J17.

See the "Backplane Connector Locations (Rear)" illustration for location information.

CT1-CT10 (Shelf Enumeration)

Cuttable traces CT1-CT10 allow the ZT 5090 to be assigned a unique address for use with other systems. Insert 0 Ω resistors at cuttable traces CT1-CT10 to set a unique address as described in the CT1-CT10 (Shelf Enumeration) table.

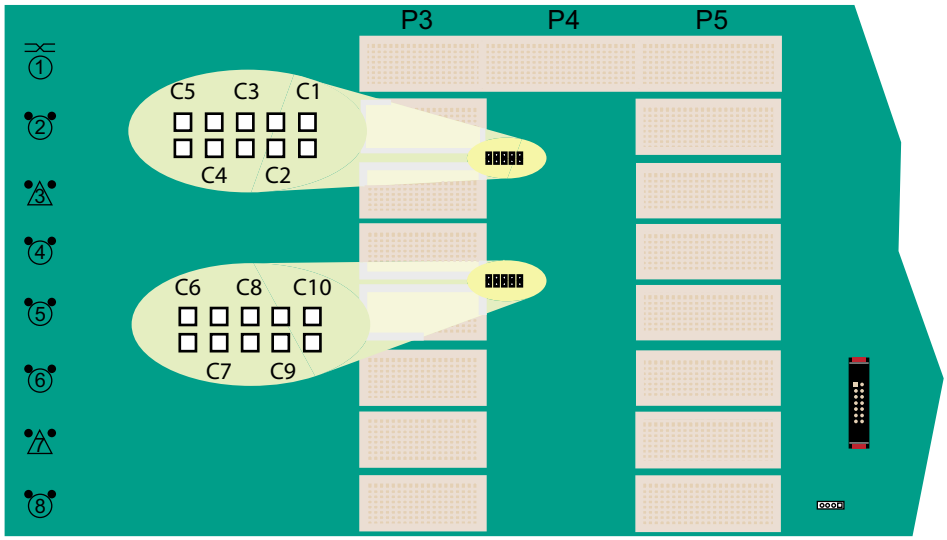
Each of the two H.100 buses is provided with a separate set of shelf enumeration address cuttable traces. Each H.110 bus can be set with the same or with a unique shelf enumeration address.

No 0 Ω resistors are pre-installed. The "Cuttable Trace Locations (Rear)" illustration shows the location of the cuttable traces.

CT1-CT10 (Shelf Enumeration)

CT	Address	CT	Address
1	SGA0	6	BSGA0
2	SGA1	7	BSGA1
3	SGA2	8	BSGA2
4	SGA3	9	BSGA3
5	SGA4	10	BSGA4

Cuttable Trace Locations (Rear)



U1-U8 Two-Wire Thermometers

Two-wire thermometers (DS75S) are loaded at U1-U8 on the front side of the ZT 5090's backplane. Temperature data is used by the CMM to monitor system performance. The following "U1-U8 Two-Wire Thermometer Locations" table lists the thermometers and their signals. See the "Backplane Connector Locations (Front)" illustration for location information.

U1-U8 Two-Wire Thermometer Locations

Slot Number	Device	Signal
1	U1	SENSOR 0
2	U2	SENSOR 1
3	U3	SENSOR 2
4	U4	SENSOR3
5	U5	SENSOR 4
6	U6	SENSOR 5
7	U7	SENSOR 6
8	U8	SENSOR 7

B. Power Supplies and Hot Swap Circuitry

Intel NetStructure hot swap products are essentially electrically isolated from the backplane when installed or removed. This prevents transients from corrupting backplane communication when a product is installed or removed while the system is operating.

When boards are powering up, this circuit monitors the power supply voltages available. Until the proper voltages are present, the board will not power up. This creates a concern when using power supplies that require a minimum load to start up.

The Power Supply Perspective

Power supplies typically have two minimum load requirements for the primary output to operate properly:

- The minimum start-up load requirement (typically 100-200mA).
- The minimum regulation load requirement. This requirement must be met to guarantee that the power supply's auxiliary outputs regulate properly when fully loaded, even if the primary output is not fully loaded. This is typically specified as 10% of the maximum output capability of the primary output.

In a pure hot swap system, the power supply essentially sees no load even after the input power to the system is applied because the hot swap circuitry remains disabled until the voltage levels reach the appropriate value. The power supply never generates the proper voltage until it sees a load. They both wait for each other and the system never powers up.

When configuring a pure hot swap system, minimum start up loads for the power supply must be considered. This can be accomplished in a number of ways. The most direct solution is to include a simple power resistor in the system to provide the start up load necessary for the supply.

Intel NetStructure Power Supplies

The Intel NetStructure power supplies that Intel currently provides have a minimum start up load and a minimum guaranteed regulation load:

- Start up load: +5 V @ 100 mA
- Regulation: +5 V @ 2.5 A

These requirements should be met for EACH SUPPLY in the system. In a hot swap system with three power supplies, a *minimum* load of 300 mA on the +5V output must be present to guarantee that the power supplies start up properly.

C. Data Sheet Reference

This appendix provides links to data sheets, standards, and specifications for the technology designed into the boards in your system.

Board Serial # ID

Refer to the Dallas Semiconductor *DS2401 Silicon Serial Number* data sheet for more information about the DS2401 device. The data sheet is in Adobe Acrobat* format (PDF) and available online at:

http://www.dalsemi.com/DocControl/PDFs/pdfindex.html

CompactPCI

Current CompactPCI Specifications can be purchased from PICMG (PCI Industrial Computers Manufacturers Group) for a nominal fee. Short form specifications in Adobe Acrobat format (PDF) are also available on PICMG's website at:

http://www.picmg.org/gcompactPCI.htm

Thermal

Refer to the Dallas Semiconductor *DS75 2-Wire Thermal Watchdog* data sheet for more information about the DS75 device. The data sheet is in Adobe Acrobat format (PDF) and available online at:

http://pdfserv.maxim-ic.com/arpdf/DS75.pdf

User Documentation

The latest Intel NetStructure product information and manuals are available on the Intel NetStructure Website at http://www.intel.com/network/csp/products/cpci_index.htm. Refer to the following manuals and Technical Product Specifications for more information about the components that may be in your system.

- Intel NetStructure ZT 5504 System Processor Board with Intel Pentium III Processor Hardware Manual
- The appropriate rear-panel I/O board hardware manual (ZT 4807)
- ZT 8101 Fast Ethernet Switch Technical Product Specification
- ZT 7101 Chassis Management Module Technical Product Specification
- Intel NetStructure Embedded BIOS Software Manual
- Hot Swap Kit for Windows 2000 CompactPCI Systems Software Manual

D. Intel® NetStructure™ Compute Boards & Platform Products

Limited Warranty

Intel warrants to the original owner that the product delivered in this package will be free from defects in material and workmanship for two (2) year(s) following the latter of: (i) the date of purchase only if you register by returning the registration card as indicated thereon with proof of purchase; or (ii) the date of manufacture; or (iii) the registration date if by electronic means provided such registration occurs within 30 days from purchase. This warranty does not cover the product if it is damaged in the process of being installed. Intel recommends that you have the company from whom you purchased this product install the product.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ANY WARRANTY OF INFRINGEMENT OF ANY OTHER PARTY'S INTELLECTUAL PROPERTY RIGHTS, OR ANY WARRANTY ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE.

This warranty does not cover replacement of products damaged by abuse, accident, misuse, neglect, alteration, repair, disaster, improper installation or improper testing. If the product is found to be otherwise defective, Intel, at its option, will replace or repair the product at no charge except as set forth below, provided that you deliver the product along with a return material authorization (RMA) number (see below) either to the company from whom you purchased it or to Intel. If you ship the product, you must assume the risk of damage or loss in transit. You must use the original container (or the equivalent) and pay the shipping charge. Intel may replace or repair the product with either a new or reconditioned product, and the returned product becomes Intel's property. Intel warrants the repaired or replaced product to be free from defects in material and workmanship for a period of the greater of: (i) ninety (90) days from the return shipping date; or (ii) the period of time remaining on the original two (2) year warranty.

This warranty gives you specific legal rights and you may have other rights which vary from state to state. All parts or components contained in this product are covered by Intel's limited warranty for this product. The product may contain fully tested, recycled parts, warranted as if new.

Returning a Defective Product (RMA)
Before returning any product, contact an Intel Customer Support Group to obtain either a Direct Return Authorization (DRA) or Return Material Authorization (RMA). Return Material Authorizations are only available for products purchased within 30 days.

Return contact information by geography:

For the Americas

Return Material Authorization (RMA) credit requests e-mail address: requests.rma@intel.com
Direct Return Authorization (DRA) repair requests e-mail address: uspss.repair@intel.com
DRA on-line form: http://support.intel.com/support/motherboards/draform.htm
Intel Business Link (IBL): www.intel.com/ibl
Telephone No.: 1-800-INTEL4U or 480-554-4904
Office Hours: Monday - Friday 0700-1700 MST Winter / PST Summer

For EMEA
Return Material Authorization (RMA) e-mail address - emea.fs@intel.com
Direct Return Authorization (DRA) for repair requests e-mail address: emea.fs@intel.com
Intel Business Link (IBL): http://intel.com/ibl
Telephone No.: 00 44 1793 403063

Fax No.: 00 44 1793 403109
Office Hours: Monday - Friday 0900-1700 UK time

For APAC
RMA/DRA requests email address: apac.rma.front-end@intel.com
Telephone No.: 604-859-3111 or 604-859-3325
Fax No.: 604-859-3324
Office Hours: Monday - Friday 0800-1700 Malaysia time

For IJKK
Return Material Authorization (RMA) requests e-mail address: rma.center.jpss@intel.com
Telephone No.: 81-298-47-0993 or 81-298-47-5417
Fax No.: 81-298-47-4264
Direct Return Authorization (DRA) for repair requests, contact the JPSS Repair center.
E-mail address: sugiyamakx@intel.co.jp
Telephone No.: 81-298-47-8920
Fax No.: 81-298-47-5468
Office Hours: Monday - Friday 0830-1730 Japan time

If the Customer Support Group verifies that the product is defective, they will have the Direct Return Authorization/Return Material Authorization Department issue you a DRA/RMA number to place on the outer package of the product. Intel cannot accept any product without a DRA/RMA number on the package. Limitation of Liability and Remedies

INTEL SHALL HAVE NO LIABILITY FOR ANY INDIRECT OR SPECULATIVE DAMAGES (INCLUDING , WITHOUT LIMITING THE FOREGOING, CONSEQUENTIAL, INCIDENTAL AND SPECIAL DAMAGES) ARISING FROM THE USE OF OR INABILITY TO USE THIS PRODUCT, WHETHER ARISING OUT OF CONTRACT, NEGLIGENCE, TORT, OR UNDER ANY WARRANTY, OR FOR INFRINGEMENT OF ANY OTHER PARTY'S INTELLECTUAL PROPERTY RIGHTS, IRRESPECTIVE OF WHETHER INTEL HAS ADVANCE NOTICE OF THE POSSIBILITY OF ANY SUCH DAMAGES, INCLUDING, BUT NOT LIMITED TO LOSS OF USE, BUSINESS INTERRUPTIONS, AND LOSS OF PROFITS. NOTWITHSTANDING THE FOREGOING, INTEL'S TOTAL LIABILITY FOR ALL CLAIMS UNDER THIS AGREEMENT SHALL NOT EXCEED THE PRICE PAID FOR THE PRODUCT. THESE LIMITATIONS ON POTENTIAL LIABILITIES WERE AN ESSENTIAL ELEMENT IN SETTING THE PRODUCT PRICE. INTEL NEITHER ASSUMES NOR AUTHORIZES ANYONE TO ASSUME FOR IT ANY OTHER LIABILITIES.

Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitations or exclusions may not apply to you.

E. Customer Support

This appendix offers technical and sales assistance information for this product, and information on returning an Intel NetStructure product for service.

Technical Support and Return for Service Assistance

For all product returns and support issues, please contact your Intel product distributor or Intel Sales Representative for specific information.

Sales Assistance

If you have a sales question, please contact your local Intel ® NetStructure ™ Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information is available at Intel's website, located at

http://www.intel.com/network/csp/sales/

Intel Corporation

Telephone (in U.S.) 1-800-755-4444

Telephone (Outside U.S.) 1-973-993-3030

FAX 1-973-967-8780

F. Agency Approvals

Intel NetStructure platforms have been demonstrated to show compliance with mandatory U.S. and international electromagnetic compatibility standards with all chassis slots either filled with compliant devices or covered by blank filler panels. In order to maintain this compliance, it is **mandatory** that all unused slots be filled with blank filler panels or compliant devices.

Use CompactPCI industry standard blank filler panels with EMI gaskets. Blank filler panels may be purchased from Intel (refer to the following part numbers).

To fill a single slot, use panels that are 6U x 4HP (horizontal pitch=0.2") (Intel PN 835022).

To fill a double slot, use panels that are 6U x 8HP (Intel PN 844131).

CE Certification

The ZT 5090 meets intent of Directive 89/336/EEC for Electromagnetic Compatibility and Low-Voltage Directive 73/23/EEC for Product Safety. The ZT 5090 has been designed for NEBS/ETSI compliance.

Safety

UL/cUL 60950	Safety for Information Technology Equipment (UL File # E179737)
EN/IEC 60950	Safety for Information Technology Equipment
CB Report Scheme	CB certificate and Report

Emissions Test Regulations

FCC Part 15, Subpart B

EN 55022

CISPR 22

Bellcore GR-1089

EN 50081-1 Emissions

GR-1089-CORE	Sections 2 and 3
EN 55022	Class A Radiated
EN 55022	Power Line Conducted Emissions
EN 61000-3-2	Power Line Harmonic Emissions
EN 61000-3-3	Power line Fluctuation and Flicker

EN 55024 Immunity

GR-1089-CORE	Sections 2 and 3

EN 61000 4-2	Electro-Static Discharge (ESD)
EN 61000 4-3	Radiated Susceptibility
EN 61000 4-4	Electrical Fast Transient Burst
EN 61000 4-5	Power Line Surge
EN 61000 4-6	Frequency Magnetic Fields
EN 61000 4-11	Voltage dips, Variations, and Short Interruptions

Regulatory Information

FCC (USA)

This product has been tested and found to comply with the limits for a Class A digital device pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This product generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Note: This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Caution: If you make any modification to the equipment not expressly approved by Intel, you could void your authority to operate the equipment.

Industry Canada (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadien des Communications.

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

Product Safety Information

Review the following precautions to avoid injury and prevent damage to this product, or any products to which it is connected. To avoid potential hazards, use the product only as specified.

Read all safety information provided in the component product user manuals and understand the precautions associated with safety symbols, written warnings, and cautions before accessing parts or locations within the unit. Save this document for future reference.

Caution: To Avoid Electric Overload: To avoid electrical hazards (heat shock and/or fire hazard), do not make connections to terminals outside the range specified for that terminal. See the product user manual for correct connections.

Caution: To Avoid the Risk of Electric Shock: When supplying power to the system, always make connections to a grounded main. Always use a power cable with a grounded plug (third grounding pin). Do not operate in wet, damp, or condensing conditions.

Caution: System Airflow Requirements: Platform components such as Single Board Computers, Ethernet Switches, etc., are designed to operate with external airflow. Components can be destroyed if they are operated without external airflow. External airflow is normally provided by chassis fans when components are installed in compatible chassis. Filler panels must be installed over unused chassis slots so that airflow requirements are met. Please refer to the product data sheet for airflow requirements if you are installing components in custom chassis.

Caution: Microprocessor Heatsinks May Become Hot During Normal Operation: To avoid burns, do not allow anything to touch processor heatsinks.

Caution: Do Not Operate Without Covers: To avoid electric shock or fire hazard, do not operate this product with any removed enclosure covers or panels.

Caution: To Avoid the Risk of Electric Shock: Do not operate in wet, damp, or condensing conditions.

Caution: Do Not Operate in an Explosive Atmosphere: To avoid injury, fire hazard, or explosion, do not operate this product in an explosive atmosphere.

Caution: If Your System Has Multiple Power Supply Sources: Disconnect all external power connections before servicing.

Warning: Power Supplies Must Be Replaced by Qualified Service Personnel Only.

Caution: Lithium Batteries Are Not Field-Replaceable Units: There is a danger of explosion if a battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions. Return the unit to Intel for battery service.

AC and/or DC Power Safety Warning (AC and/or DC Powered Units)

The AC and/or DC power cord is your unit's main AC and/or DC disconnecting device, and must be easily accessible at all times. Auxiliary AC and/or DC On/Off switches and/or circuit breaker switches are for power control functions only (NOT THE MAIN DISCONNECT).

For your safety, use only a power cord with a grounded plug. The enclosure is also provided with a separate earth ground connection/stud. The earth ground connection should be installed prior to the application of power or peripheral connections and should never be disconnected while power or peripheral connections exist.

To reduce the possibility of electric shock from a telephone or Ethernet system, plug your enclosure into the power source before making these connects. Disconnect these connections before unplugging your enclosure from the power source.

Warning: Verify Power Cord and Outlet Compatibility. Check to ensure you are using the appropriate power cords for your power outlet configurations. Visit the following website for additional information: http://kropla.com/electric2.htm.

Rack Mount Enclosure Safety

Your enclosure may be intended for stationary rack mounting. Mount in a rack designed to meet the physical strength requirements of NEBS GR-63-CORE and NEBS GR 487. Your system may have multiple power sources. Disconnect all power sources and external connections/cables prior to installing or removing your system from a rack frame.

Prior to mounting, Intel recommends you remove all hot-swappable equipment for optimum weight reduction. Be sure to mount your system in a way that ensures even loading of the rack. Uneven mechanical loading of weight can result in a hazardous condition. Secure all mounting bolts when installing the enclosure to the frame/rack.

Caution: Avoid Electric Overload. To avoid electric shock or fire hazard, only connect your system to an input voltage source as specified in the product user manual.