Modular Reference Design
System Electronics Board

History

Changes made to Revision E.

1. Removed CS_B#[5:0]. Tied CS_Bn# to CS_An# at DIMM connectors.
2. Changed WE_B#, SCAS_B# and SRAS_B# to WE_A#, SCAS_A#, SRAS_A# on J17
3. Changed WE_A#, SCAS_A# and SRAS_A# to WE_B#, SCAS_B# and SRAS_B# on J16.
4. Pin K25 of the CPU connector has been changed from reserved to VCC_CMOS.
5. A20M#, INIT, SLP, IGNNE NMI,INTR, STPCLK# and SMI are now pulled up to VCC_CMOS.
6. A20M#, INIT, SLP, IGNNE NMI,INTR, STPCLK# and SMI have series resistors and 680 ohm pullups from 2.7K pullups.
7. Removed Pullup on FERR#. Processor assembly or interposer cards must pull this signal up.
8. Modified Boot Block flash to support 28F004B5.
9. Removed Series resistor from MAB12#. Processor Assembly must configure BX FSB frequency.
10. Removed flash daughter card from schematics.
11. Changed MAB12#_R net to FQS.
12. Removed FQS pullups(formerly MAB12#_R).
13. Added R308 as series termination on BXDCLKO.
14. Update RTC Crystal section.
15. Removed speaker connector.
16. Pin names A01-A09 changed to A1-A9 on ISA and DIMM connectors

Changes made to Revision D.

1. Added Signals PWROK(A24) +12V(A33) MB12#_R(B33) to J19A.
2. Moved J20
3. Added C229 to -PCIRST

Changes made to Revision C.

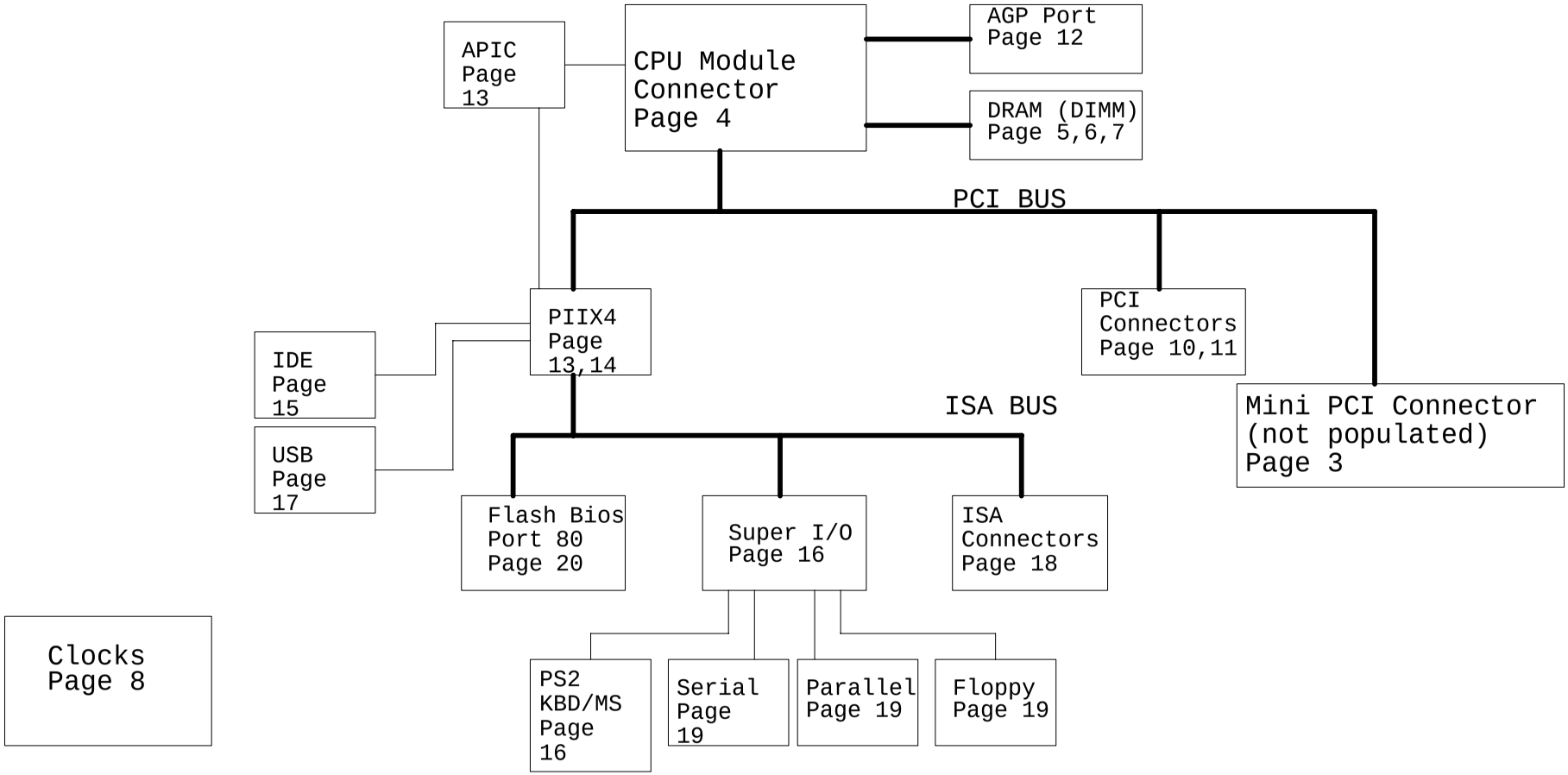
1. Tied VBAT (pin 65) to 3.3V on Super I/O.

Changes made to Revision B.

1. Swapped AD23 and AD19 on 400 pin connector.
2. Separated CSEL on IDE0 and IDE1
3. Swapped pins 1 and 3 (V5 with TP) on CPU-Fan connector.
4. Tied VBAT (pin 65) to 5.0V on Super I/O.
5. Changed RP48 to 4.7K. (Pullups for mouse and keyboard.)
6. Inverted POWERON# signal (SUSC#) from PIIX4 to control soft-on feature.
7. Changed Bulk decoupling on +12 and -12 to 2x220uF from 2x400uF.
8. Changed Bulk decoupling cap C154 from 10uF to 47uF to reduce BOM line items.

Revision E

Title: Changes		
Size: C	Document Number	Rev: E
Date: Tuesday, December 21, 1999	Sheet 1 of 22	



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: Block Diagram		
Size: C	Document Number: <Doc>	Rev: D
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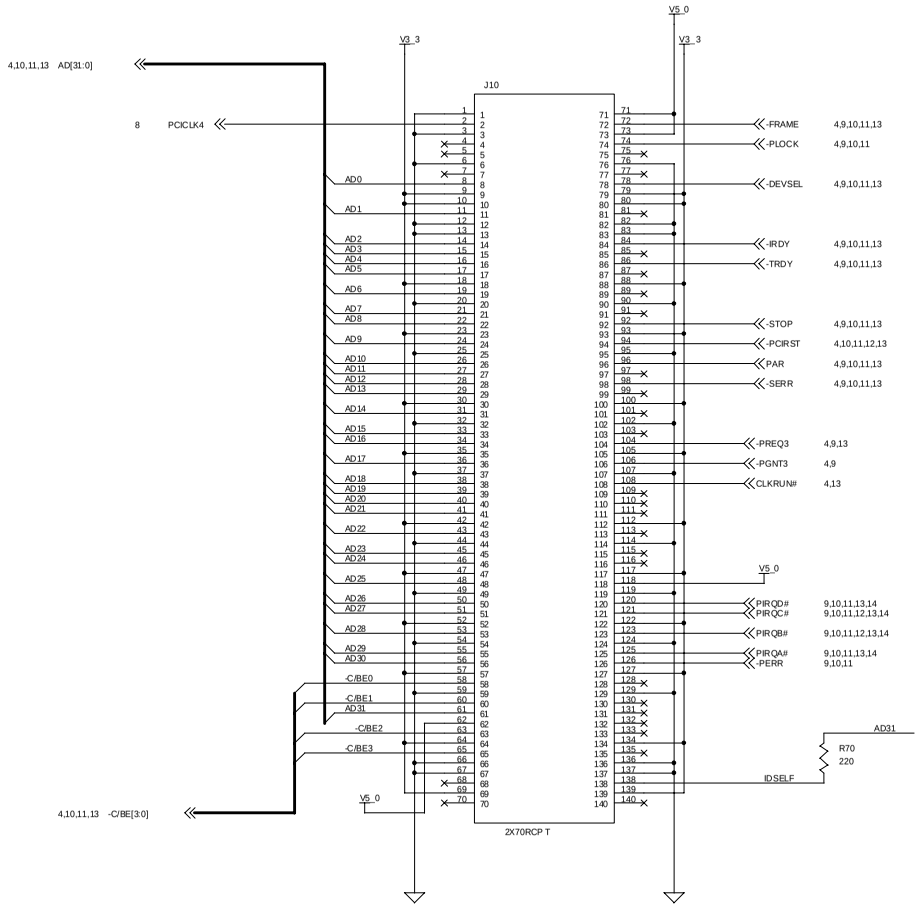
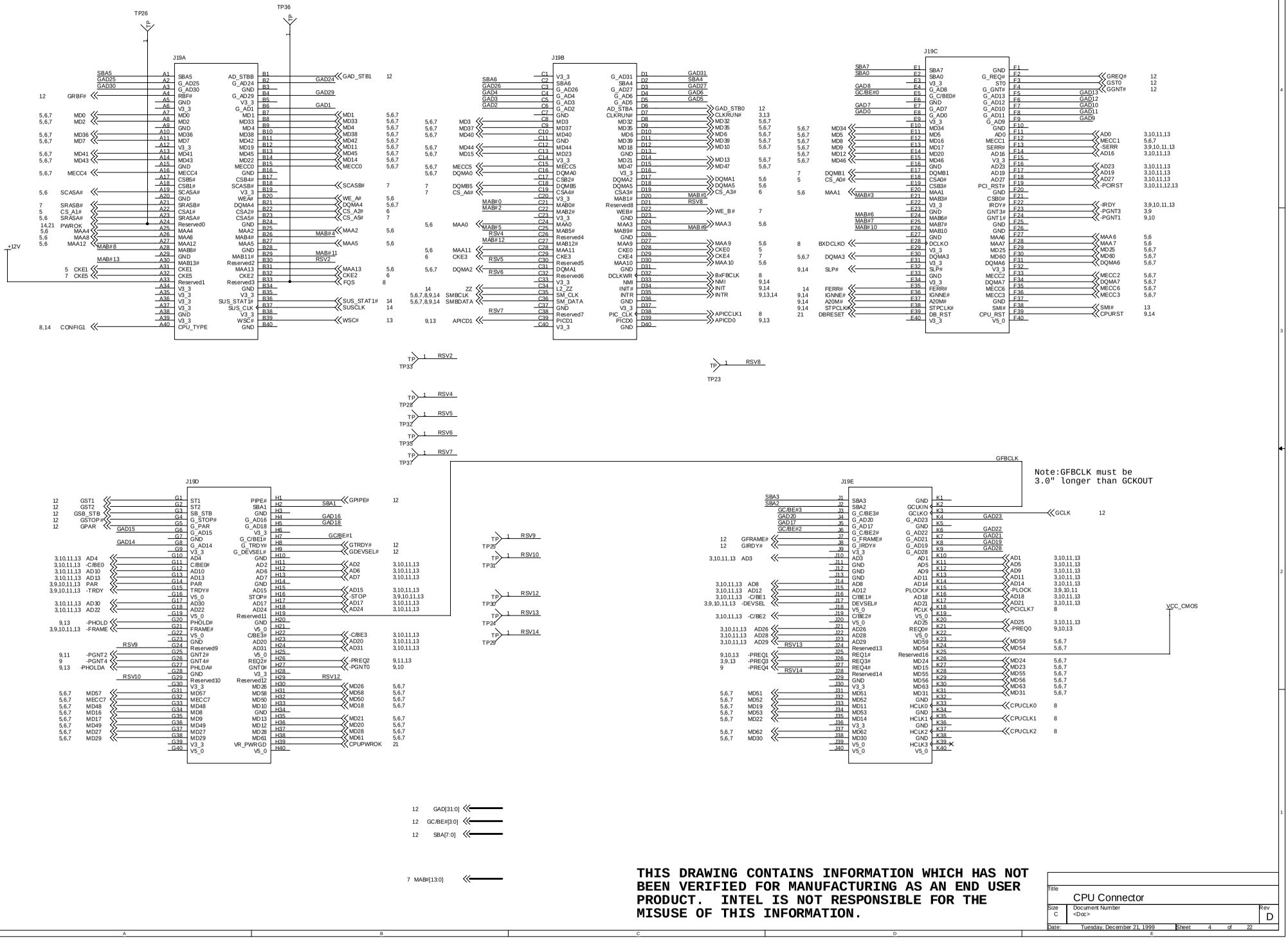
Do not populate J10



Title	Mini PCI Connector	
Size C	Document Number <Doc>	Rev D
Date: Tuesday, December 21, 1999	Sheet 3 of 22	


TP26
TP36
J19A
J19B
J19C
J19D
J19E
+12V
GFBCLK
Note:GFBCLK must be 3.0" longer than GCKOUT
VCC_CMOS
TP33 RSV2
TP23 RSV8
TP28 RSV4
TP32 RSV5
TP35 RSV6
TP37 RSV7
TP25 RSV9
TP31 RSV10
TP30 RSV12
TP24 RSV13
TP29 RSV14
12 GAD[31:0]
12 GC/BE#[3:0]
12 SBA[7:0]
7 MAB#[13:0]
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Title
CPU Connector
Size C
Document Number <Doc>
Rev D
Date: Tuesday, December 21, 1999
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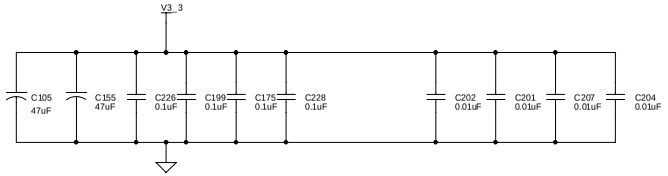
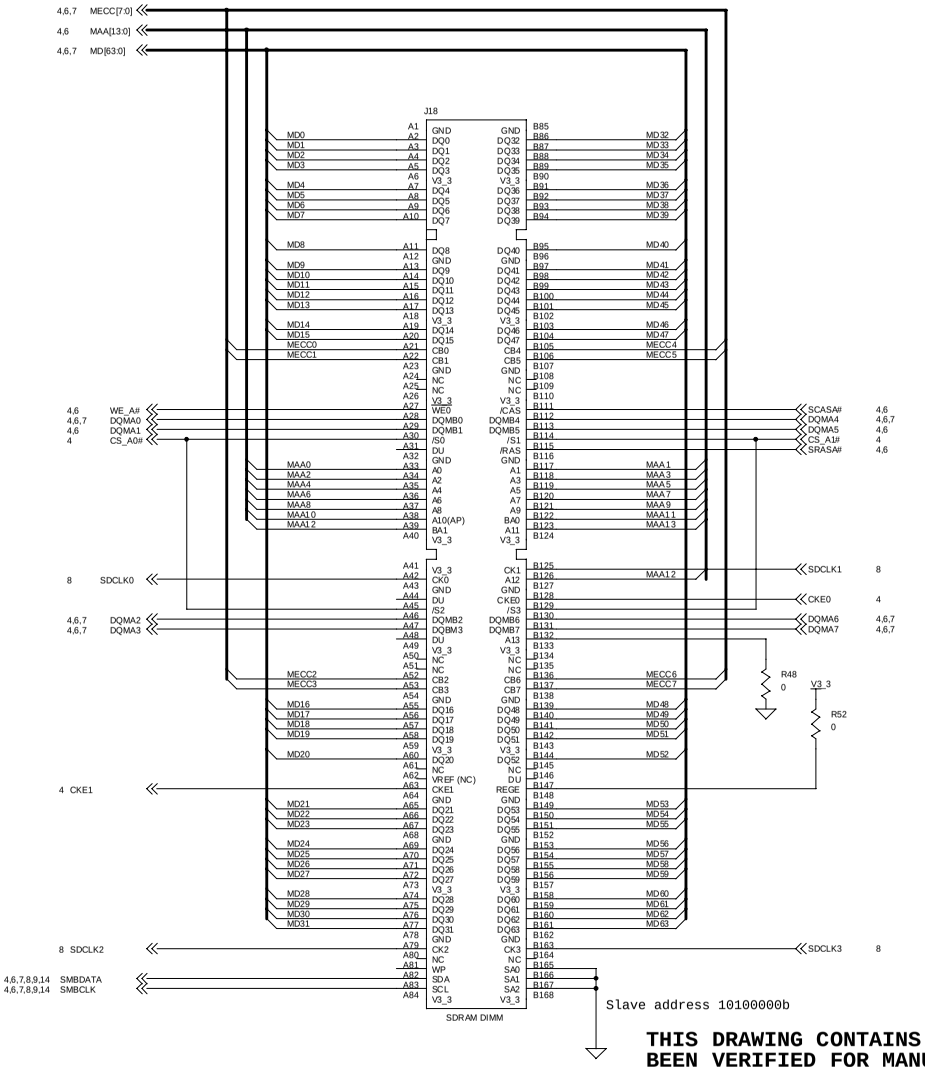


Socket 0



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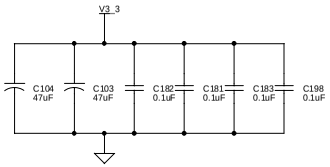
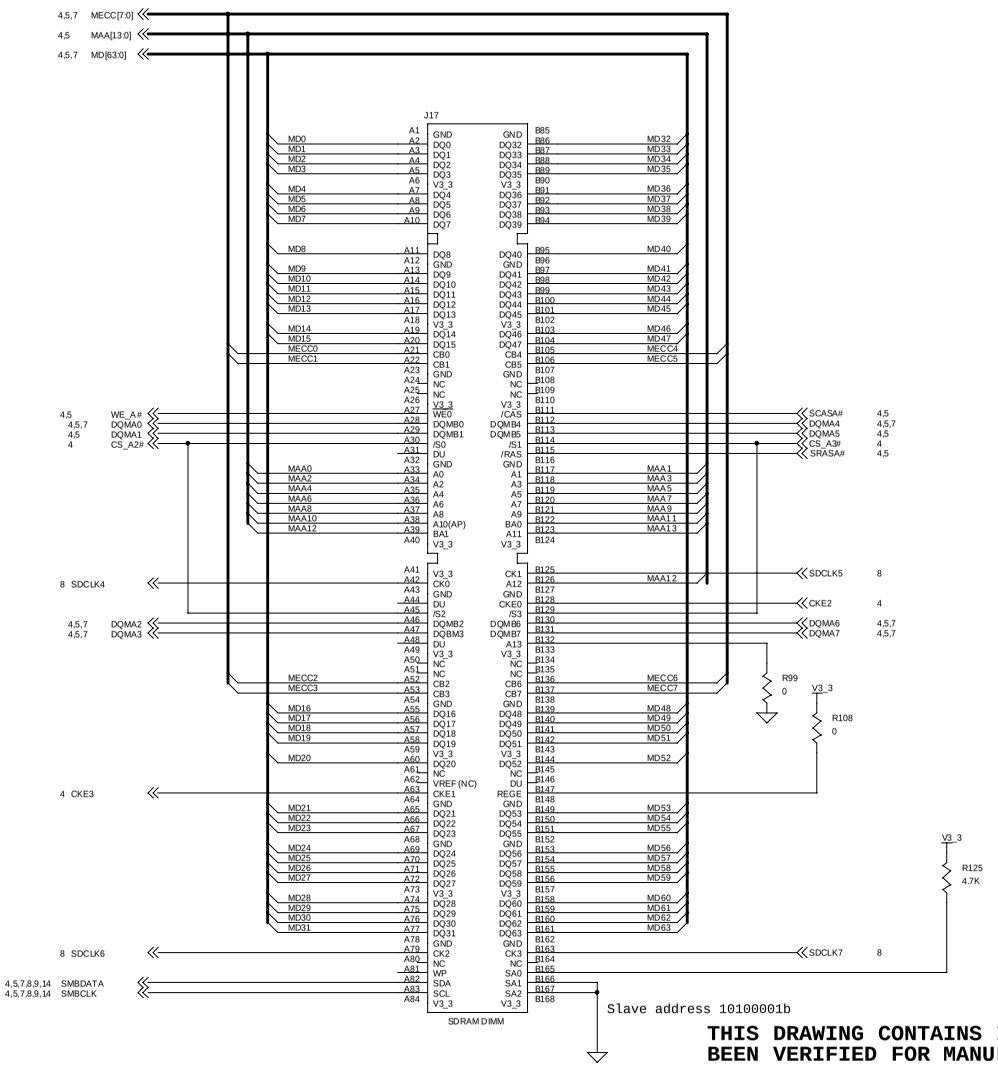
Title: DIMM0			
Size: C	Document Number: <Doc>		Rev: D
Date: Tuesday, December 21, 1999	Sheet 5 of 22		



Socket 1



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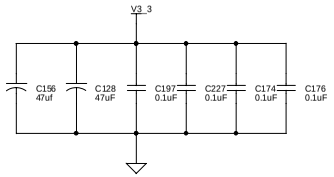
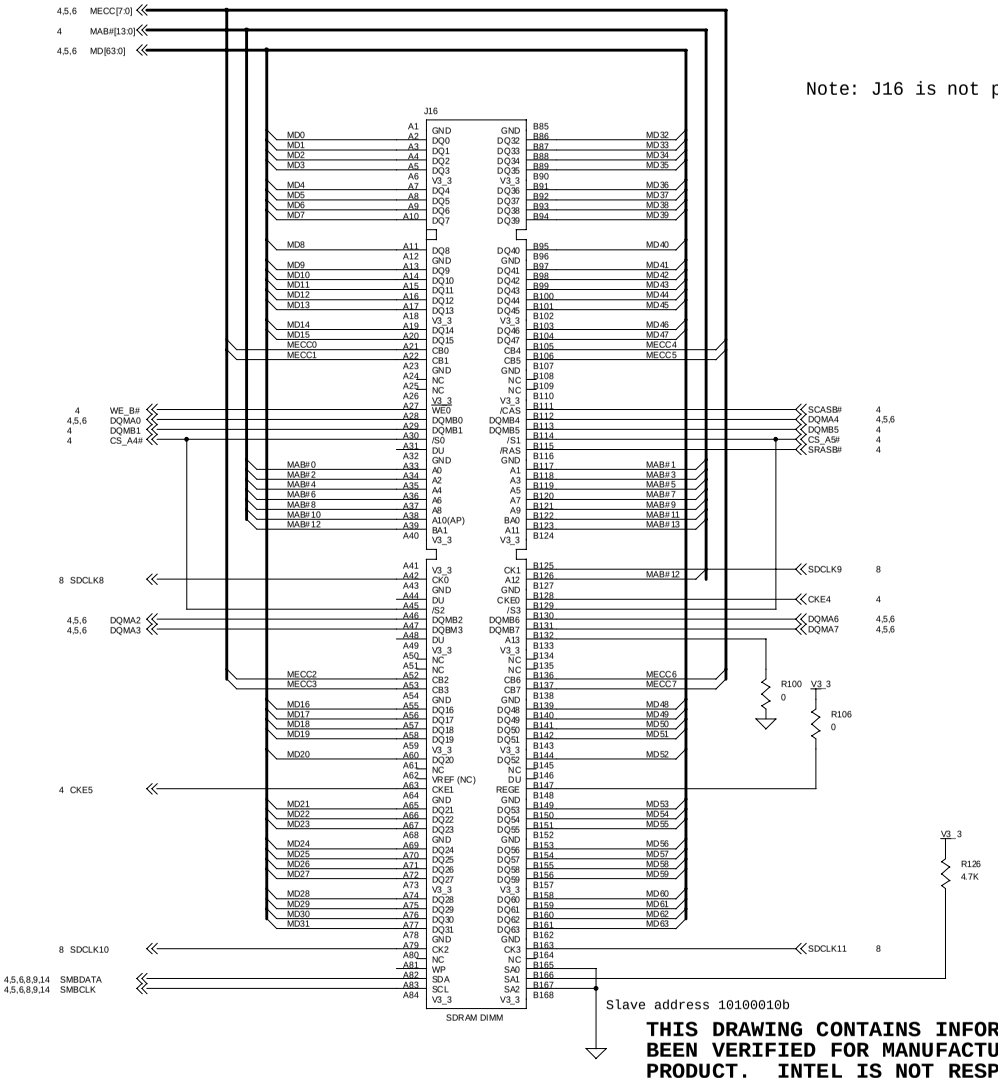
Title: DIMM1			
Size: C	Document Number: <Doc>		Rev: D
Date: Tuesday, December 21, 1999	Sheet 6 of 22		



Socket 2

Note: J16 is not populated



Slave address 10100010b

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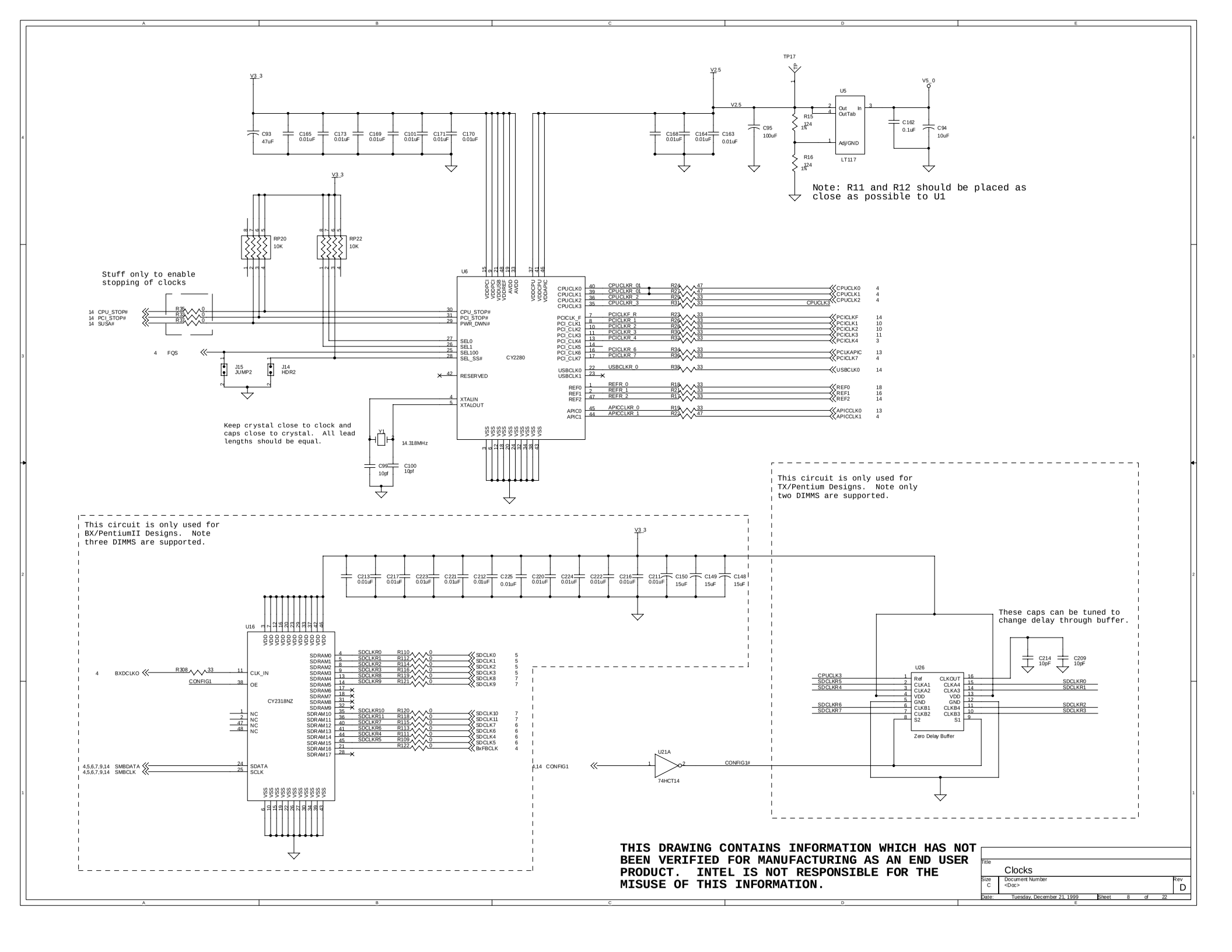
Title: DIMM2		
Size: C	Document Number: <Doc>	Rev: D
Date: Tuesday, December 21, 1999	Sheet 7 of 22	


V3_3
C93 47uF
C165 0.01uF
C173 0.01uF
C169 0.01uF
C101 0.01uF
C171 0.01uF
C170 0.01uF
V2.5
C168 0.01uF
C164 0.01uF
C163 0.01uF
C95 100uF
TP17
R15 124 1%
R16 124 1%
U5
Out
OutTab
In
Adj/GND
LT117
V5_0
C162 0.1uF
C94 10uF
Note: R11 and R12 should be placed as close as possible to U1
RP20 10K
RP22 10K
Stuff only to enable stopping of clocks
14 CPU_STOP#
14 PCI_STOP#
14 SUSA#
R35 0
R33 0
R37 0
4 FQS
J15 JUMP2
J14 HDR2
U6
CY2280
CPU_STOP#
PCI_STOP#
PWR_DWN#
SEL0
SEL1
SEL100
SEL_SS#
RESERVED
XTALIN
XTALOUT
CPUCLK0
CPUCLK1
CPUCLK2
CPUCLK3
CPUCLKR_01
CPUCLKR_01
CPUCLKR_2
CPUCLKR_3
PCICLK_F
PCI_CLK1
PCI_CLK2
PCI_CLK3
PCI_CLK4
PCI_CLK5
PCI_CLK6
PCI_CLK7
PCICLKF_R
PCICLKR_1
PCICLKR_2
PCICLKR_3
PCICLKR_4
PCICLKR_6
PCICLKR_7
USBCLK0
USBCLK1
USBCLK_0
REF0
REF1
REF2
REFR_0
REFR_1
REFR_2
APIC0
APIC1
APICCLKR_0
APICCLKR_1
Keep crystal close to clock and caps close to crystal. All lead lengths should be equal.
Y1
14.318MHz
C99 10pf
C100 10pf
This circuit is only used for TX/Pentium Designs. Note only two DIMMS are supported.
This circuit is only used for BX/PentiumII Designs. Note three DIMMS are supported.
C213 0.01uF
C217 0.01uF
C223 0.01uF
C221 0.01uF
C212 0.01uF
C225 0.01uF
C220 0.01uF
C224 0.01uF
C222 0.01uF
C216 0.01uF
C211 0.01uF
C150 15uF
C149 15uF
C148 15uF
U16
CY2318NZ
4 BXDCLKO
R308 33
CLK_IN
CONFIG1
OE
NC
SDRAM0
SDRAM1
SDRAM2
SDRAM3
SDRAM4
SDRAM5
SDRAM6
SDRAM7
SDRAM8
SDRAM9
SDRAM10
SDRAM11
SDRAM12
SDRAM13
SDRAM14
SDRAM15
SDRAM16
SDRAM17
SDCLKR0
SDCLKR1
SDCLKR2
SDCLKR3
SDCLKR8
SDCLKR9
SDCLKR10
SDCLKR11
SDCLKR7
SDCLKR6
SDCLKR4
SDCLKR5
SDCLK0
SDCLK1
SDCLK2
SDCLK3
SDCLK8
SDCLK9
SDCLK10
SDCLK11
SDCLK7
SDCLK6
SDCLK4
SDCLK5
BxFBCLK
4,5,6,7,9,14 SMBDATA
4,5,6,7,9,14 SMBCLK
SDATA
SCLK
14 CONFIG1
U21A
74HCT14
CONFIG1#
These caps can be tuned to change delay through buffer.
C214 10pF
C209 10pF
U26
Zero Delay Buffer
CPUCLK3
SDCLKR5
SDCLKR4
SDCLKR6
SDCLKR7
Ref
CLKA1
CLKA2
VDD
GND
CLKB1
CLKB2
S2
CLKOUT
CLKA4
CLKA3
VDD
GND
CLKB4
CLKB3
S1
SDCLKR0
SDCLKR1
SDCLKR2
SDCLKR3
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Title
Clocks
Size C
Document Number <Doc>
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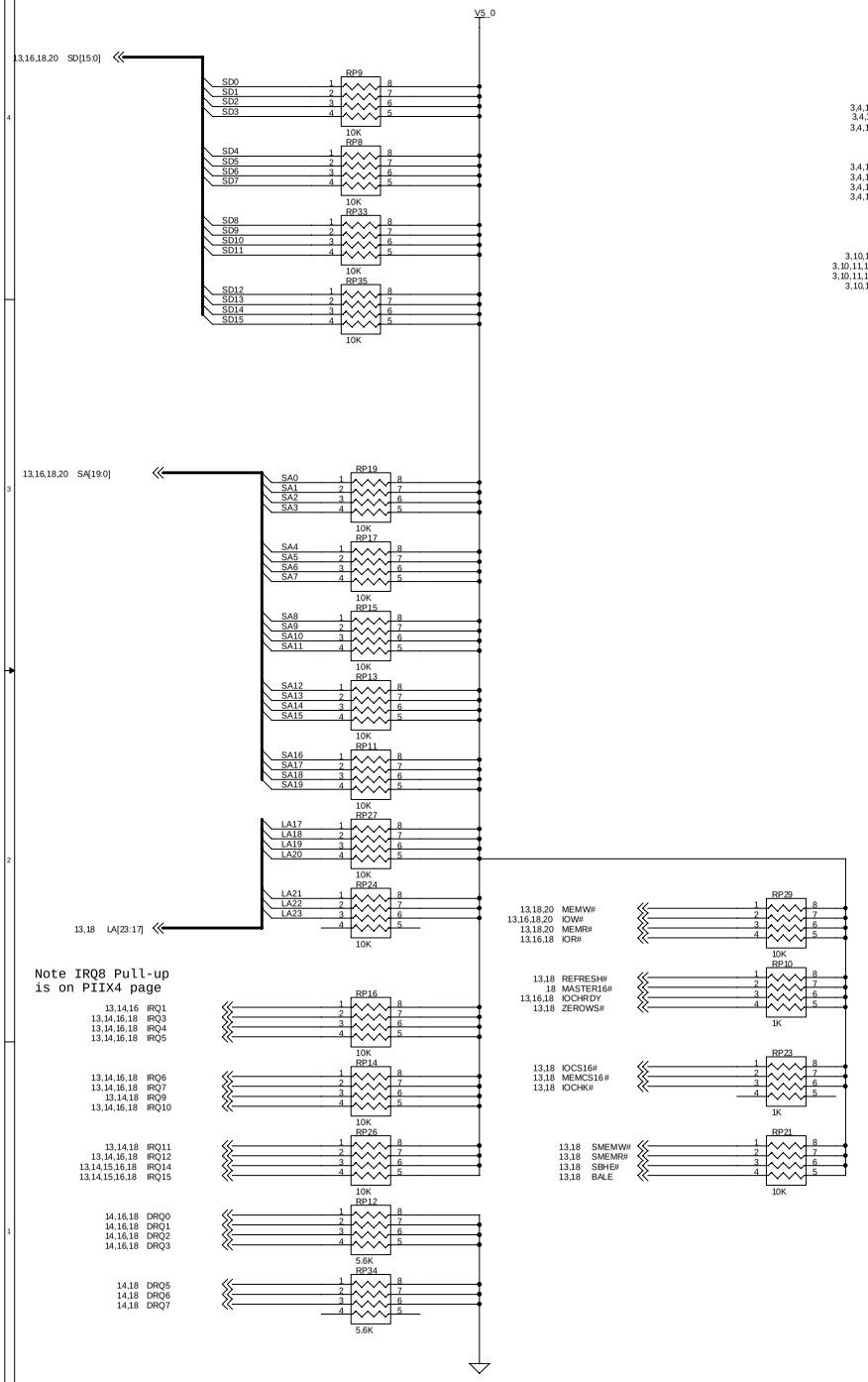
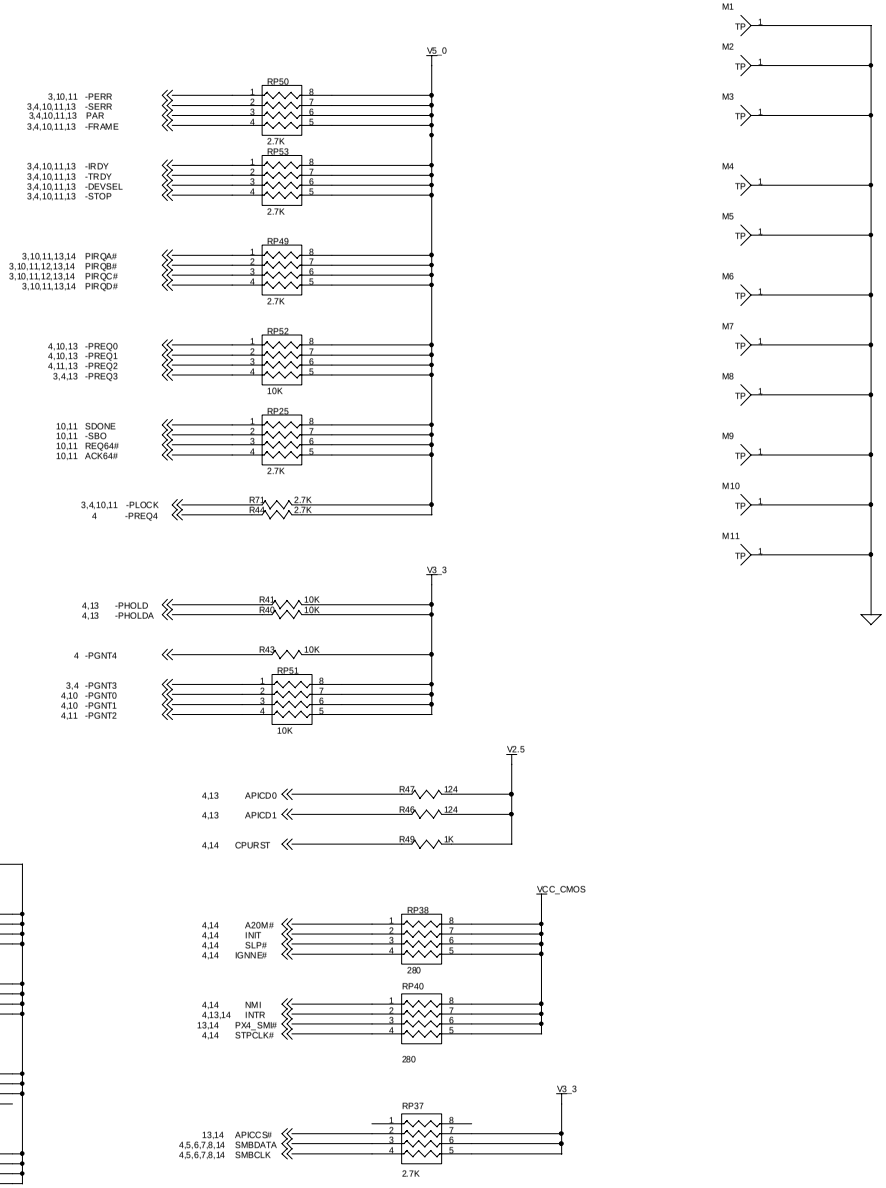
ISA Pullups



PCI Pullups



Title	ISA/PCI Pullups	
Size C	Document Number <Doc>	Rev D
Date: Tuesday, December 21, 1999	Sheet 9 of 22	

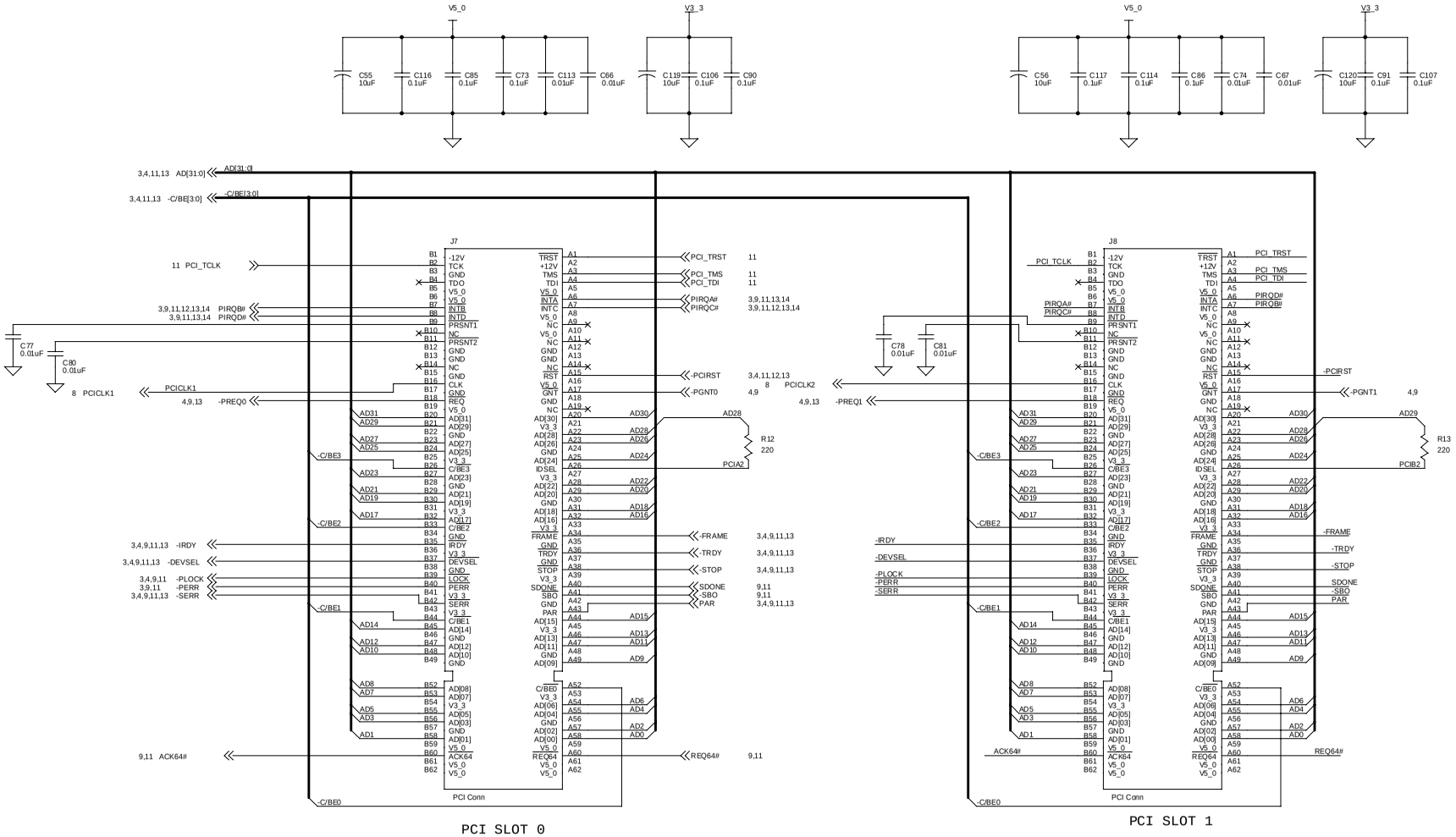
J7/J8 V5_0:
    A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
    B5, B6, B19, B22, B59, B61, B62

J7/J8 V3_3:
    A21, A27, A33, A39 A45, A53
    B25, B31, B36, B41, B43, B54

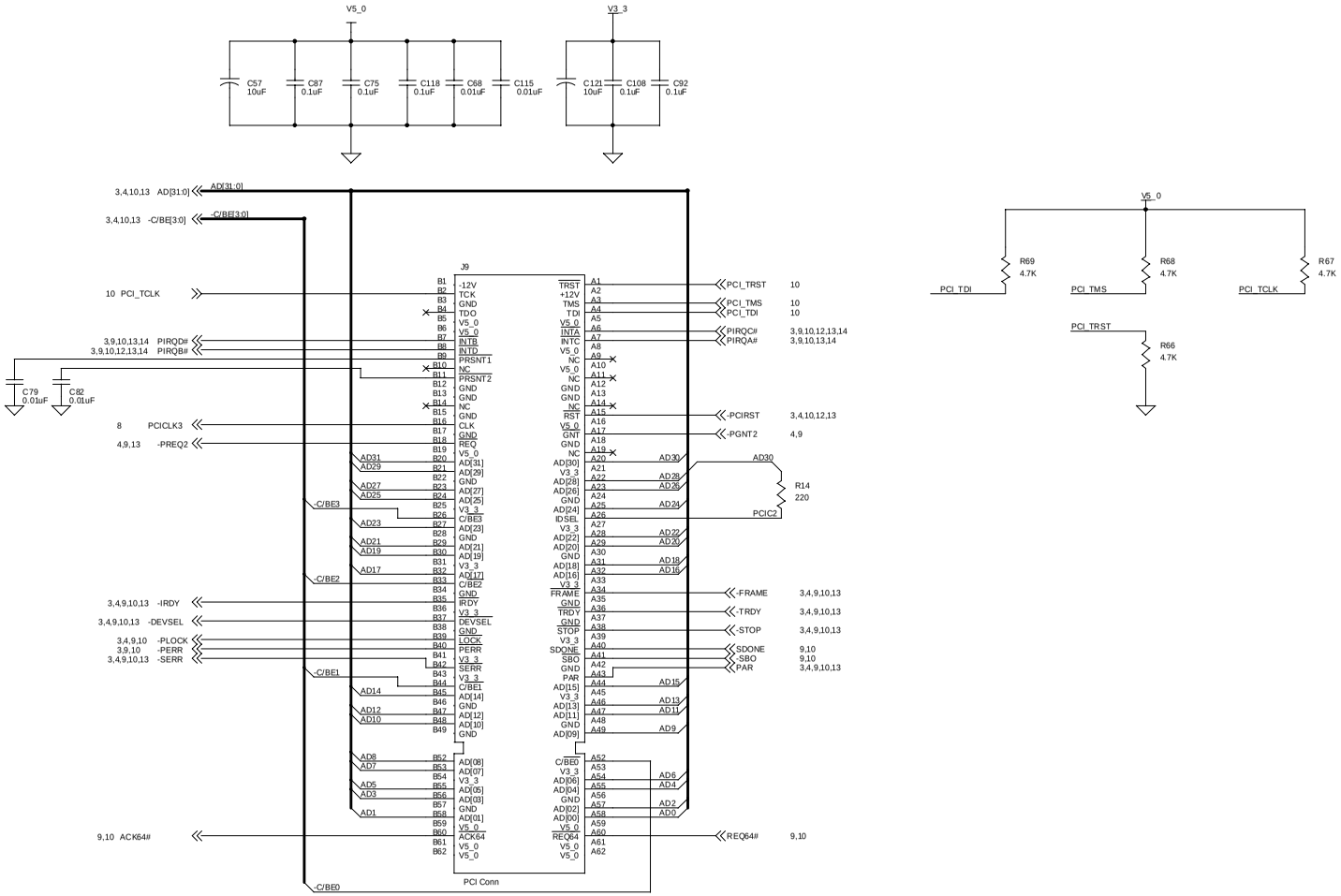
J7/J8 NC:
    A9, A11, A14, A19
    B10, B14

J7/J8 GND:
   A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
   B3, B12, B13, B15, B17, B28, B34, B38, B46, B49,
B57

J7/J8 +12V: A2
      -12V: B1



Title	PCI Slots 0 & 1	
Size: C	Document Number: <Doc>	Rev: D
Date: Tuesday, December 21, 1999	Sheet 10 of 22	



PCI SLOT 2

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Title: PCI Slot 2		
Size: C	Document Number: <Doc>	Rev: D
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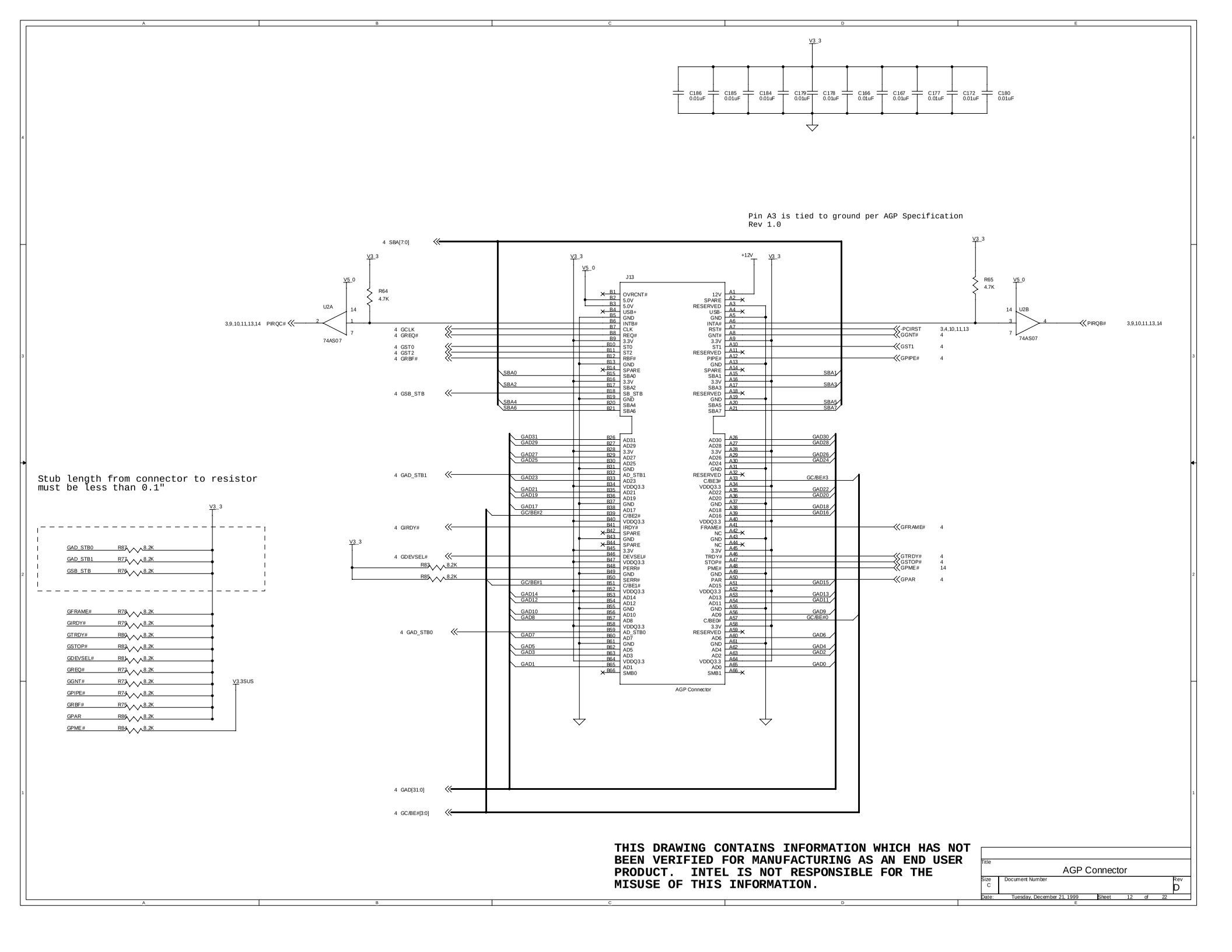
V3_3
C186 0.01uF
C185 0.01uF
C184 0.01uF
C179 0.01uF
C178 0.01uF
C166 0.01uF
C167 0.01uF
C177 0.01uF
C172 0.01uF
C180 0.01uF
Pin A3 is tied to ground per AGP Specification
Rev 1.0
4 SBA[7:0]
V3_3
V5_0
R64 4.7K
U2A
74AS07
3,9,10,11,13,14 PIRQC#
4 GCLK
4 GREQ#
4 GST0
4 GST2
4 GRBF#
4 GSB_STB
4 GAD_STB1
4 GIRDY#
4 GDEVSEL#
4 GAD_STB0
4 GAD[31:0]
4 GC/BE#[3:0]
+12V
J13
AGP Connector
R65 4.7K
U2B
74AS07
PIRQB#
3,9,10,11,13,14
-PCIRST
GGNT#
GST1
GPIPE#
GFRAME#
GTRDY#
GSTOP#
GPME#
GPAR
Stub length from connector to resistor must be less than 0.1"
GAD_STB0 R87 8.2K
GAD_STB1 R77 8.2K
GSB_STB R76 8.2K
GFRAME# R79 8.2K
GIRDY# R79 8.2K
GTRDY# R80 8.2K
GSTOP# R83 8.2K
GDEVSEL# R81 8.2K
GREQ# R72 8.2K
GGNT# R73 8.2K
GPIPE# R74 8.2K
GRBF# R75 8.2K
GPAR R86 8.2K
GPME# R84 8.2K
V3.3SUS
R83 8.2K
R85 8.2K
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Title
AGP Connector
Size C
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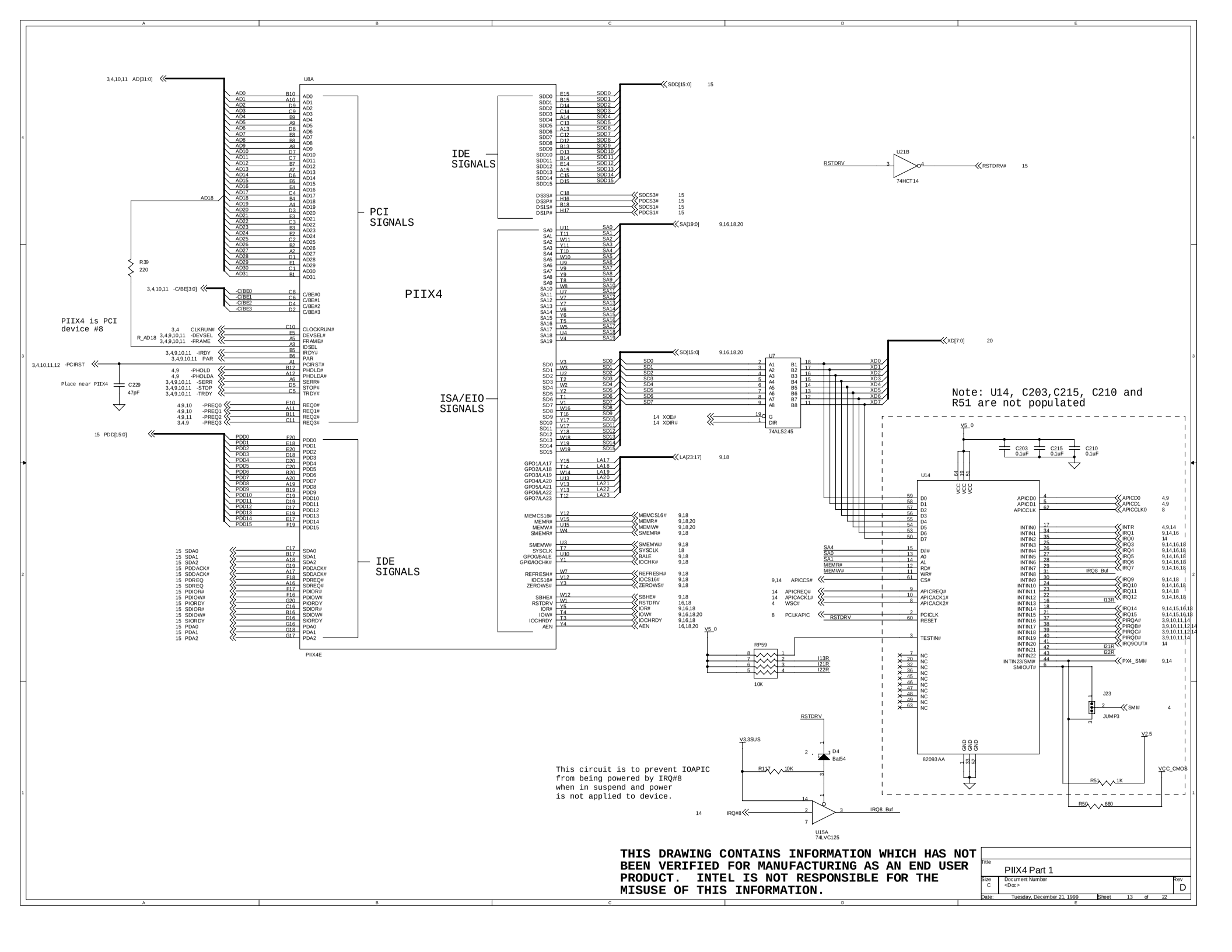
PIIX4 is PCI device #8
PCI SIGNALS
IDE SIGNALS
ISA/EIO SIGNALS
PIIX4
U8A
PIIX4E
U7
74ALS245
U14
82093AA
U21B
74HCT14
U15A
74LVC125
Note: U14, C203,C215, C210 and R51 are not populated
This circuit is to prevent IOAPIC from being powered by IRQ#8 when in suspend and power is not applied to device.
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PIIX4 Part 1
Document Number <Doc>
Rev D
Tuesday, December 21, 1999
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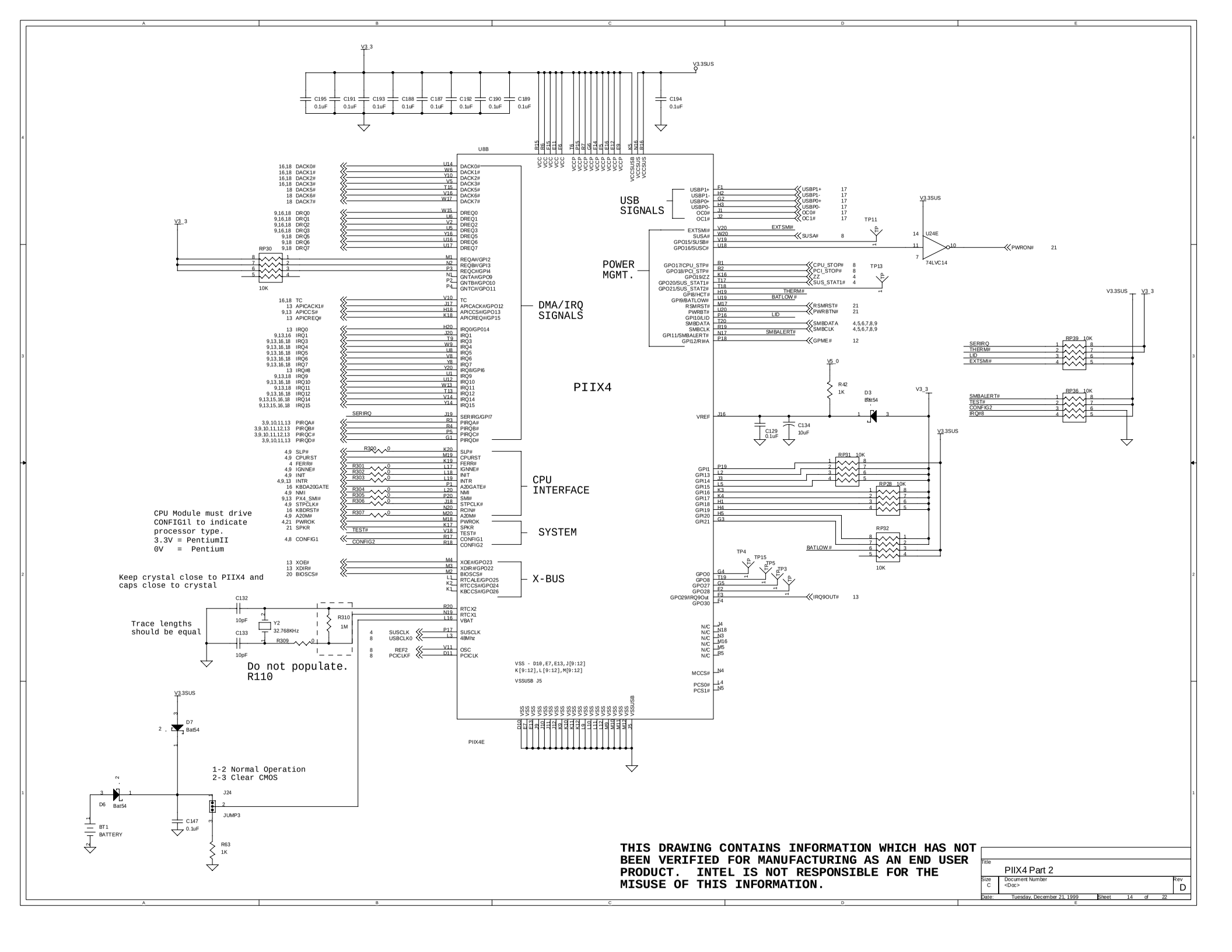
V3_3
V3.3SUS
C195 0.1uF
C191 0.1uF
C193 0.1uF
C188 0.1uF
C187 0.1uF
C192 0.1uF
C190 0.1uF
C189 0.1uF
C194 0.1uF
U8B
DMA/IRQ SIGNALS
PIIX4
CPU INTERFACE
SYSTEM
X-BUS
USB SIGNALS
POWER MGMT.
DACK0#
DACK1#
DACK2#
DACK3#
DACK5#
DACK6#
DACK7#
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
RP30
10K
TC
APICACK1#
APICCS#
APICREQ#
IRQ0
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
SERIRQ
PIRQA#
PIRQB#
PIRQC#
PIRQD#
R300 0
SLP#
CPURST
FERR#
IGNNE#
INIT
INTR
A20GATE#
NMI
SMI#
STPCLK#
RCIN#
A20M#
PWROK
SPKR
TEST#
CONFIG1
CONFIG2
XOE#
XDIR#
BIOSCS#
RTCALE/GPO25
RTCCS#/GPO24
KBCCS#/GPO26
RTCX2
RTCX1
VBAT
SUSCLK
48Mhz
OSC
PCICLK
USBP1+
USBP1-
USBP0+
USBP0-
OC0#
OC1#
EXTSMI#
SUSA#
GPO15/SUSB#
GPO16/SUSC#
CPU_STOP#
PCI_STOP#
ZZ
SUS_STAT1#
GPO20/SUS_STAT1#
GPO21/SUS_STAT2#
GPB/HCT#
GPB/BATLOW#
THERM#
BATLOW#
RSMRST#
PWRBTN#
LID
SMBDATA
SMBCLK
SMBALERT#
GPME#
PWRON#
74LVC14
U24E
RP39 10K
RP36 10K
RP31 10K
RP28 10K
RP32
10K
SERIRQ
THERM#
LID
EXTSMI#
SMBALERT#
TEST#
CONFIG2
IRQ#8
IRQ9OUT#
GPO0
GPO8
GPO27
GPO28
GPO29/IRQ9Out
GPO30
GPI1
GPI13
GPI14
GPI15
GPI16
GPI17
GPI18
GPI19
GPI20
GPI21
TP4
TP15
TP5
TP3
R42 1K
D3 Bat54
C129 0.1uF
C134 10uF
VREF
V5_0
C132 10pF
C133 10pF
Y2 32.768KHz
R309 0
R310 1M
Trace lengths should be equal
Do not populate. R110
Keep crystal close to PIIX4 and caps close to crystal
CPU Module must drive CONFIG1l to indicate processor type.
3.3V = PentiumII
0V = Pentium
D7 Bat54
D6 Bat54
BT1 BATTERY
C147 0.1uF
R63 1K
J24
JUMP3
1-2 Normal Operation
2-3 Clear CMOS
VSS - D10,E7,E13,J[9:12]
K[9:12],L[9:12],M[9:12]
VSSUSB J5
PIIX4E
N/C
MCCS#
PCS0#
PCS1#
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Title
PIIX4 Part 2
Size C
Document Number <Doc>
Rev D
Date: Tuesday, December 21, 1999
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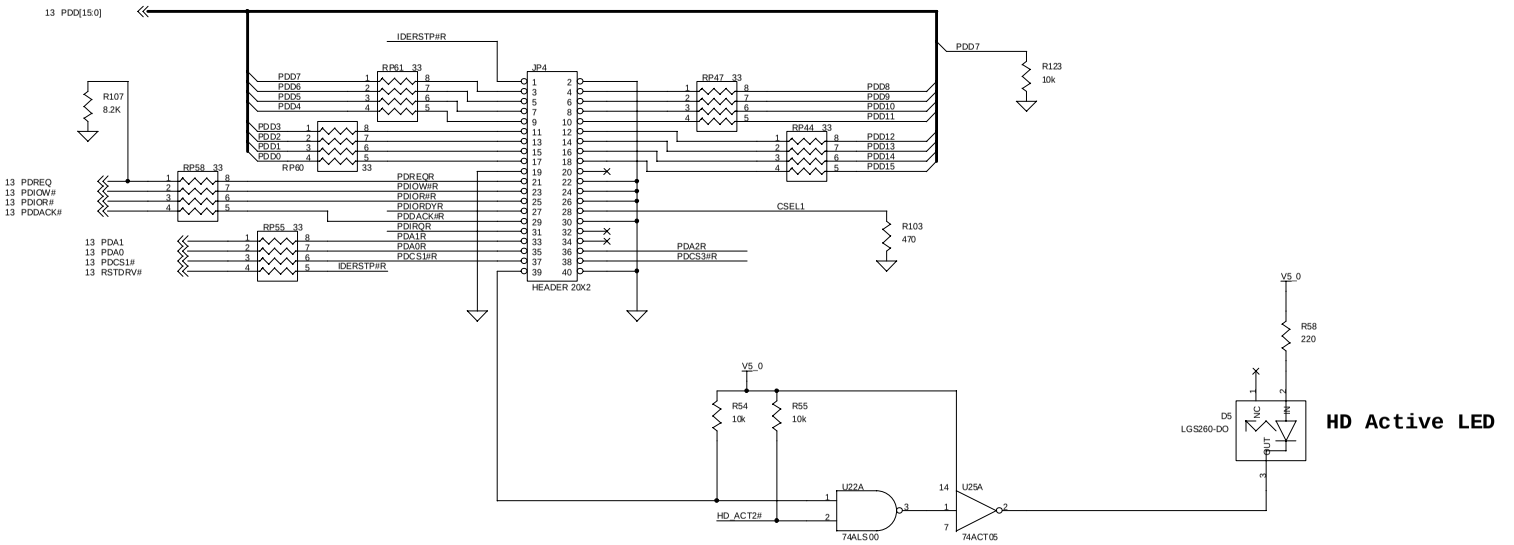
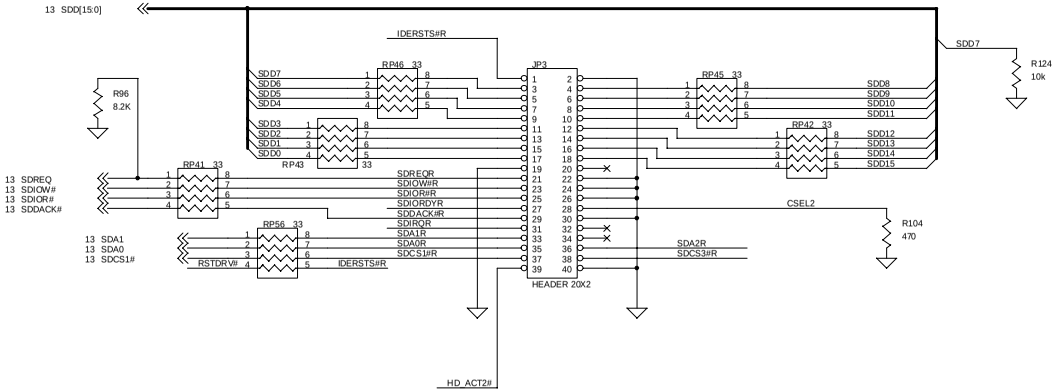
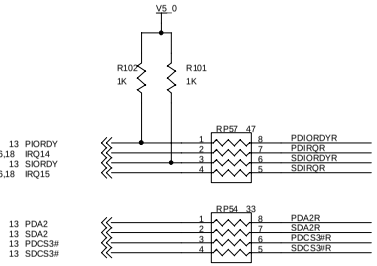
Primary IDE Connector



Secondary IDE Connector





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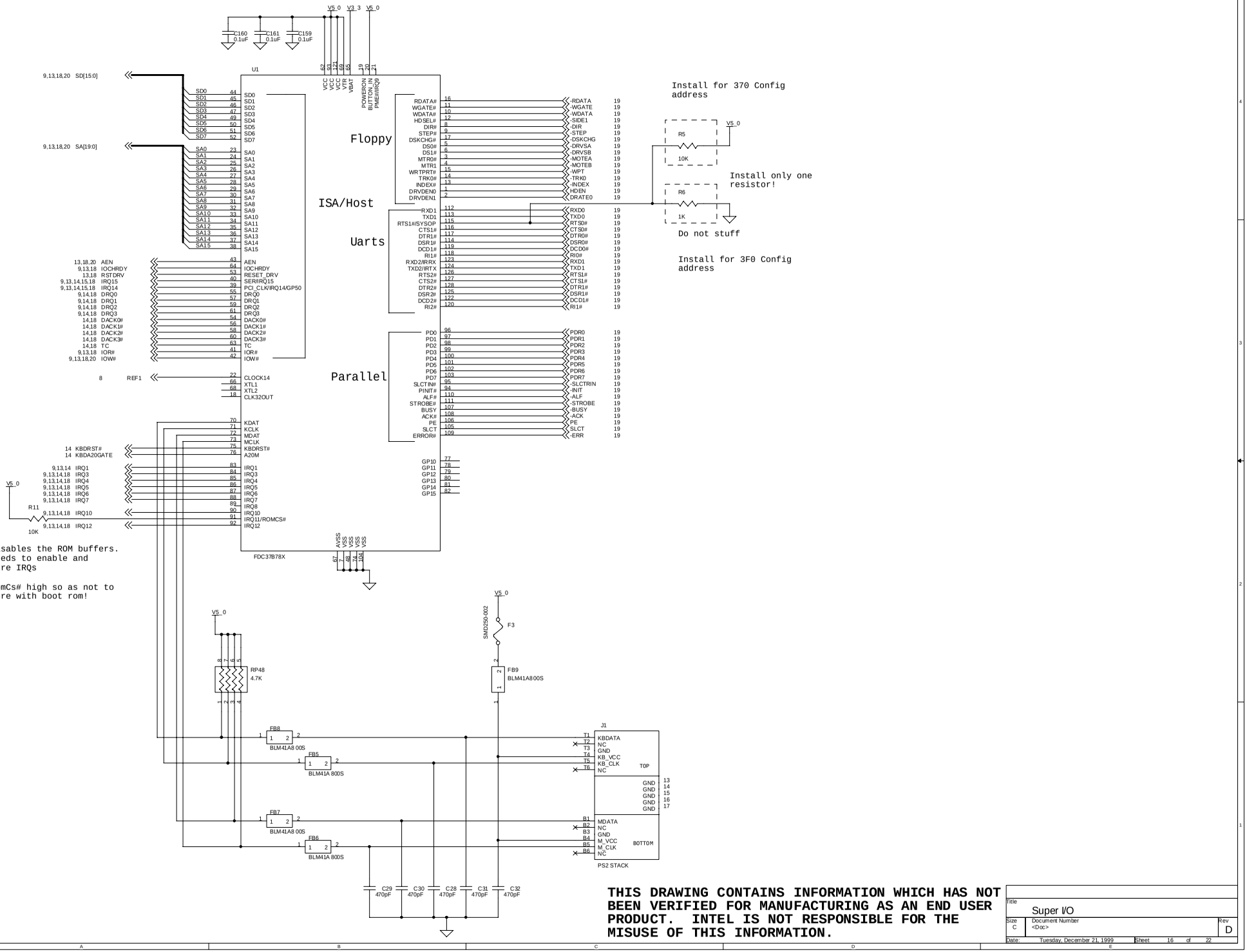
Title: IDE Connectors		
Size: C	Document Number: <Doc>	Rev: D
Date: Tuesday, December 21, 1999	Sheet 15 of 22	



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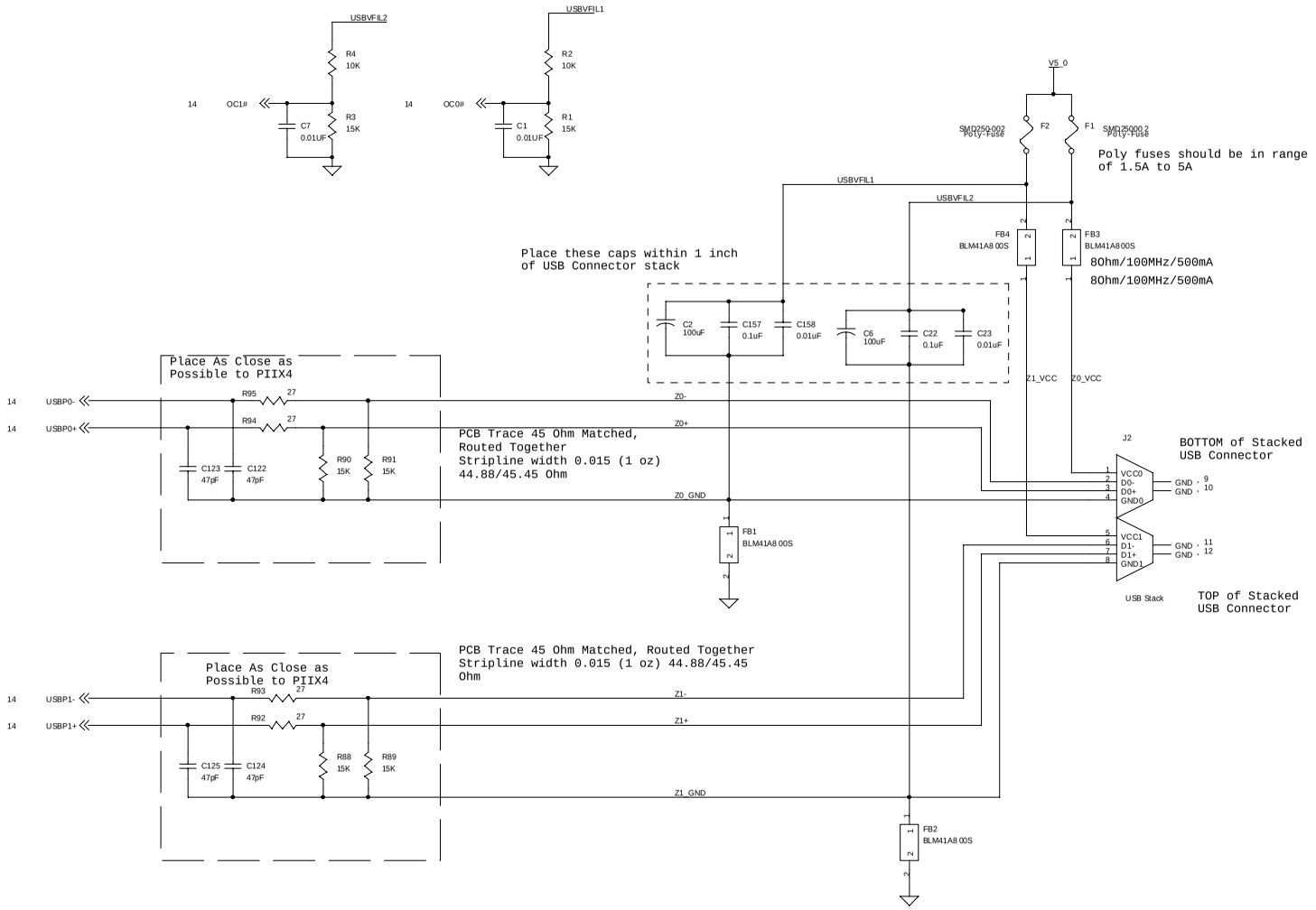
Title: Super I/O			
Size: C	Document Number: <Doc>		Rev: D
Date: Tuesday, December 21, 1999	Sheet 16 of 22		



NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or
double space to any other signal.

NOTE 3: Place ferrites at connector.

NOTE 4: Poly-fuse min 1.5A
max 5A.

Title	USB Connectors	
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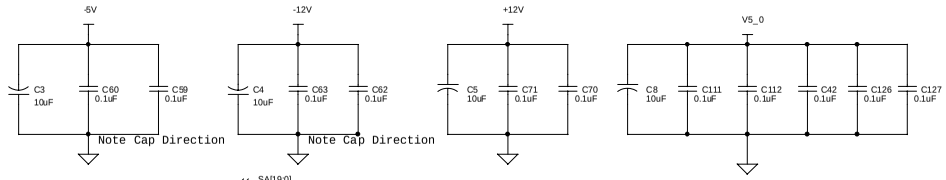
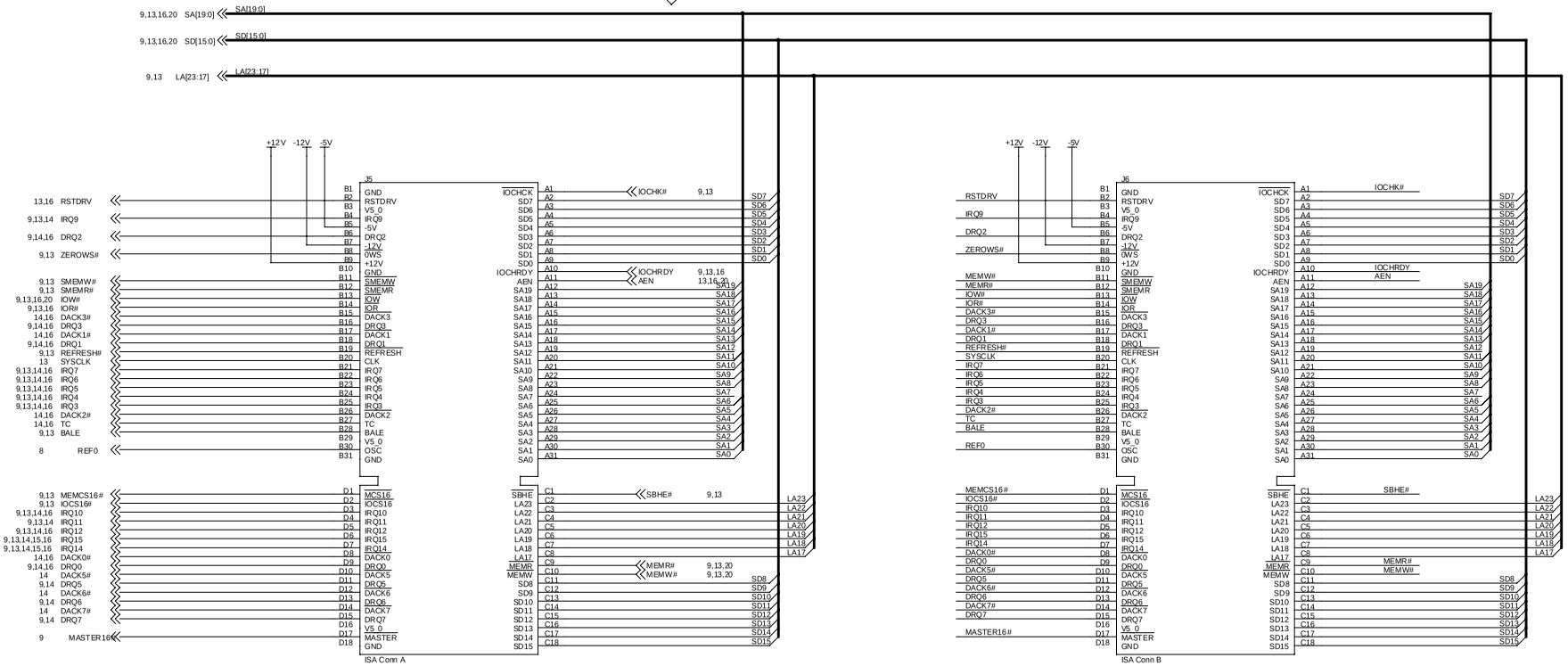
ISA Slots





J5/J6 V5_0:
B03, B29, B31, D16

J5/J6 GND:
B01, B10, D18

J5/J6: +12V B09
-12V B07
-5V B05

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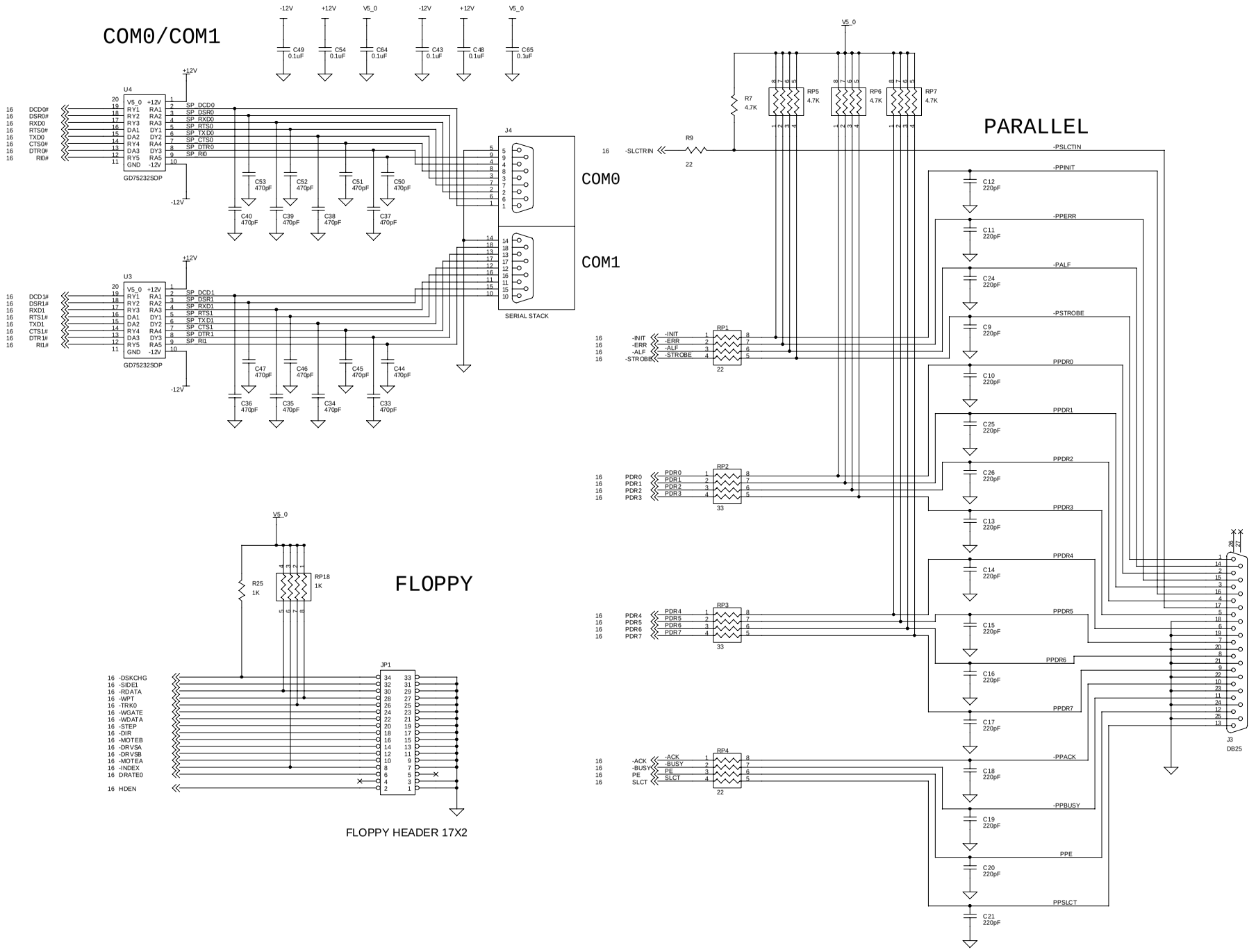
Title: ISA Connectors			
Size: C	Document Number: <Doc>		Rev: D
Date: Tuesday, December 21, 1999	Sheet 18 of 22		



THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	COMx, DB25, Floppy	
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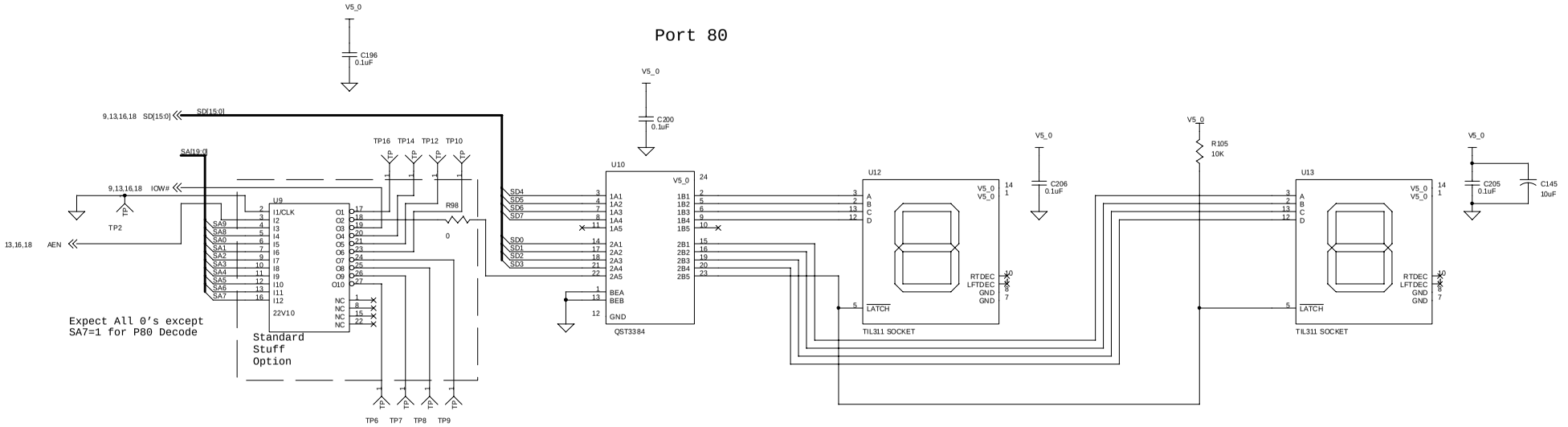
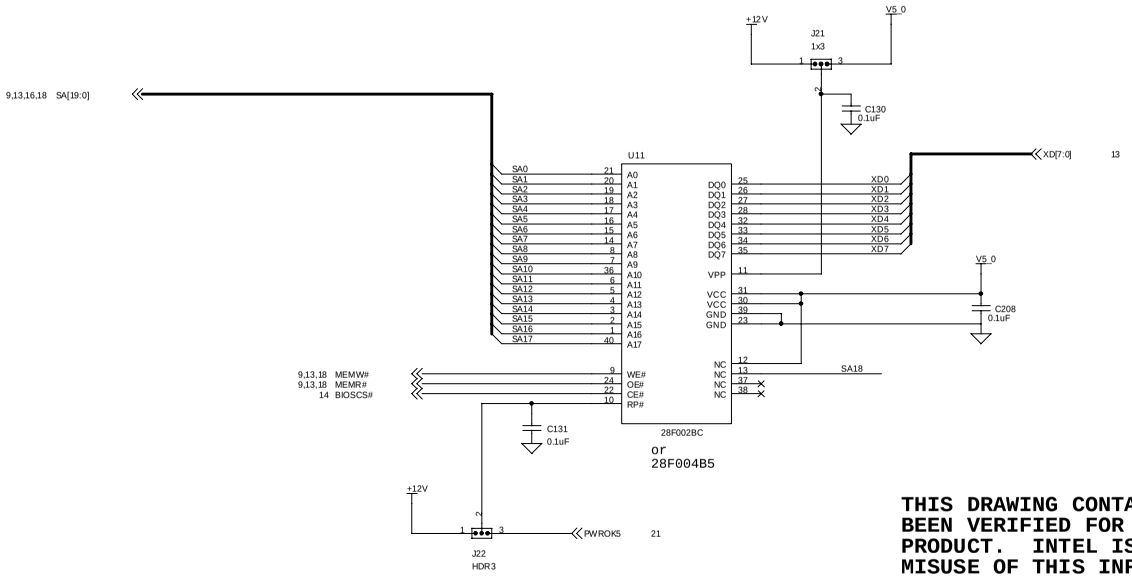
Port 80





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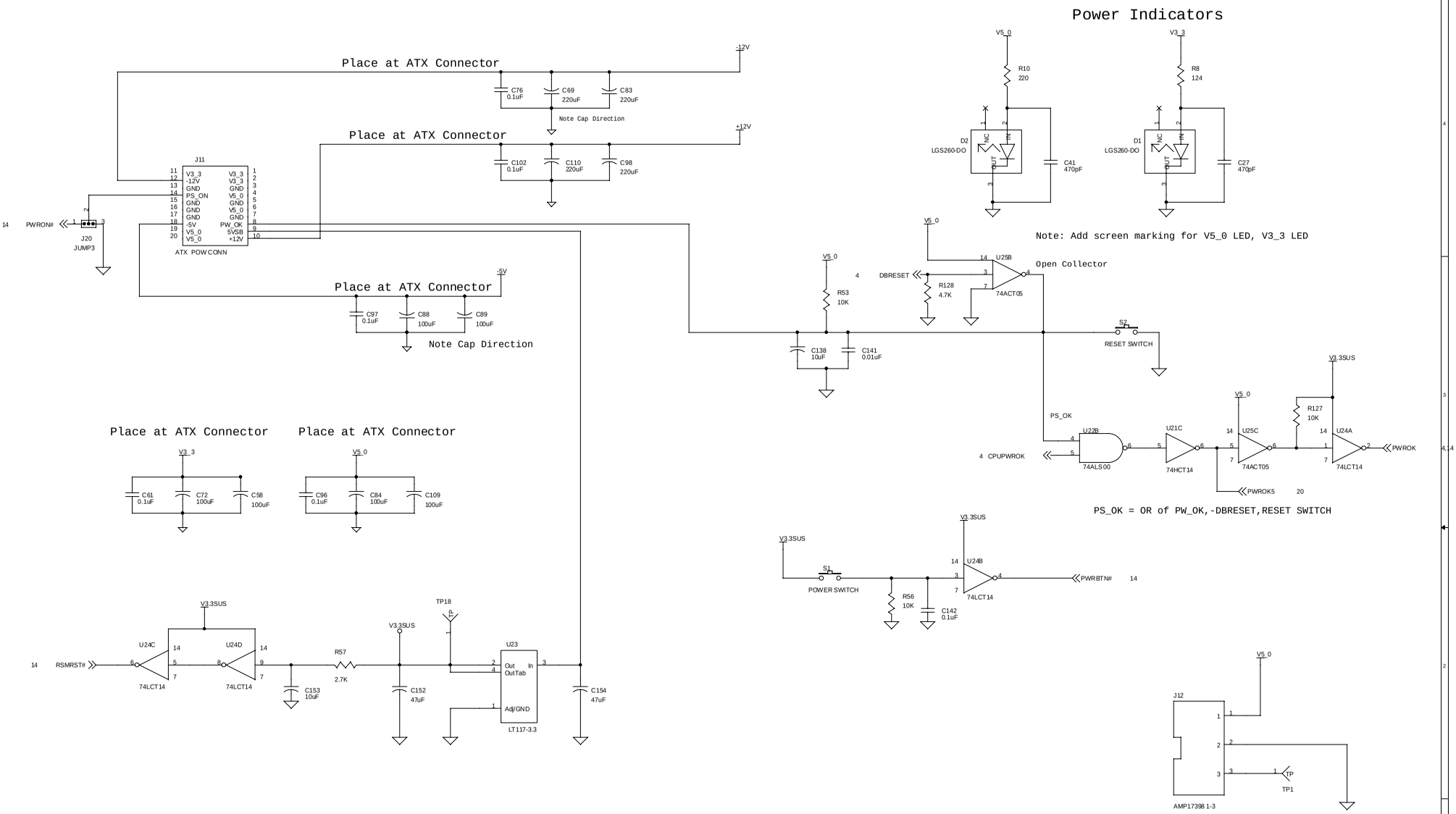
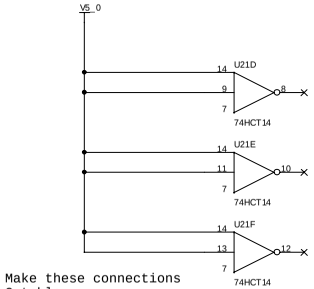
Title	BIOS/ Port 80	
Size C	Document Number <Doc>	Rev D
Date: Tuesday, December 21, 1999	Sheet 20 of 22	

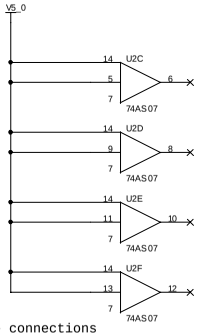


THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

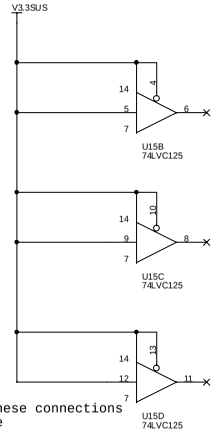
Title	ATX Power Connector	
Size C	Document Number <Doc>	Rev D
Date: Tuesday, December 21, 1999	Sheet 21 of 22	



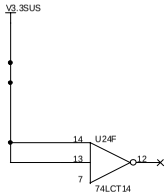
Make these connections
Cutable



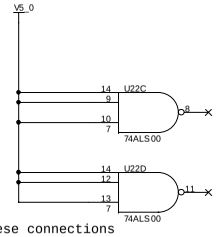
Make these connections
Cutable



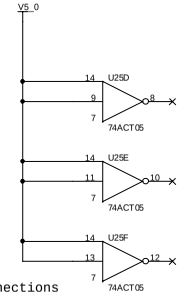
Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable

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Title: Unused Gates		
Size: C	Document Number: <Doc>	Rev: D
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PROJECT: LPM Interposer II

Revision C

HISTORY

Changes made on revision C.

1. Removed all reserved signals from Module Connector.
2. Added FQS signal from pin B34 on module connector to B33 on the baseboard connector
3. Changed value of FS PRDY# pullup to 56 ohms.
4. Removed all MAA signals, SRASB, SCASB, and WEB# singnals on Baseboard connector.
5. All CSA# signals from module Connector were routed to CSA# and CSB# signals on baseboard connector.
6. Added V_CPUPU to K25 on the baseboard Connector.
7. Added LC circuit betweet VDC an V5_0
8. Added pullups to PRDY signals on the ITP port
9. ITP connector changed to 104078-8.

Changes made on revision B.

1. Added PWROK signal to baseboard connector pin A-24
2. Inverted DBREST# signal
3. Moved pull up R14 to FS_PREQ# signal
4. Moved ITP connector to opposite side of board.
5. Removed JP2.

Title: Interposer II - TITLE_PAGE		
Size: C	Document Number: XXXX-XXX	Rev: C
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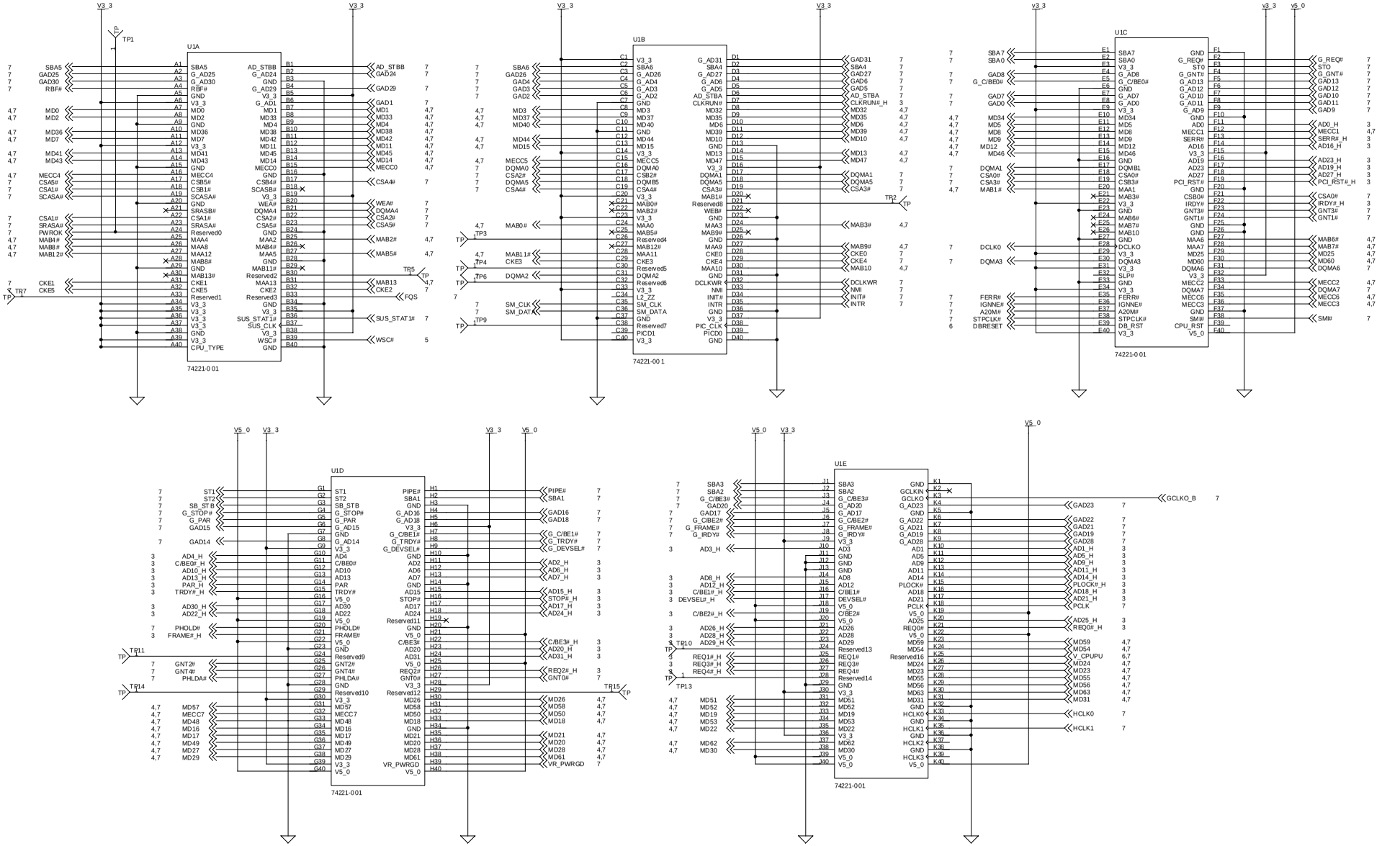
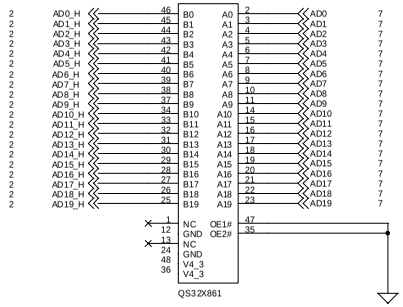
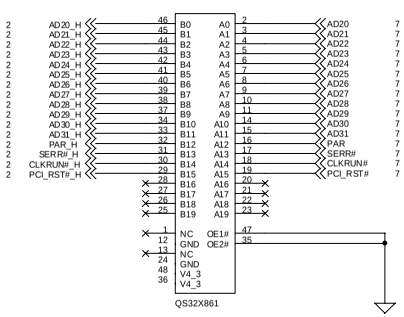
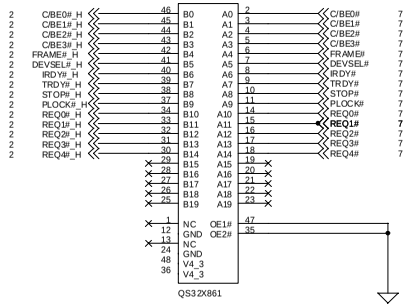
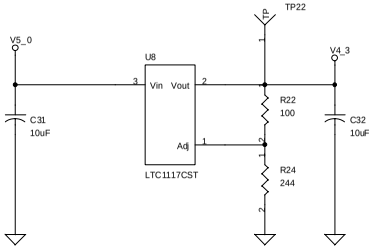
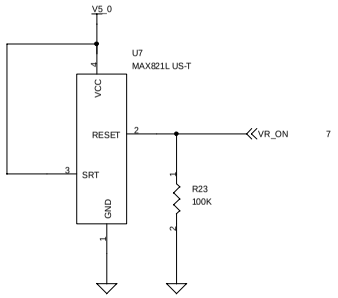

U1A
74221-0 01
U1B
74221-00 1
U1C
74221-0 01
U1D
74221-001
U1E
74221-001
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP9
TP10
TP11
TP12
TP13
TP14
TP15
V3_3
V5_0
Title
BASEBOARD CONNECTOR
Size
C
Document Number
<Doc>
Rev
C
Date:
Tuesday, December 21, 1999
Sheet
2
of
7



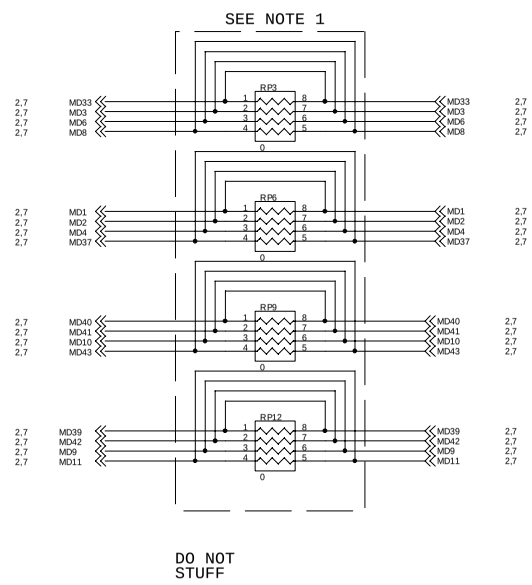


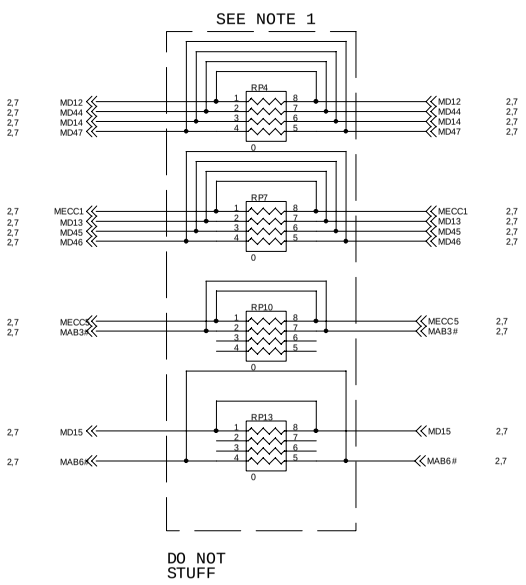


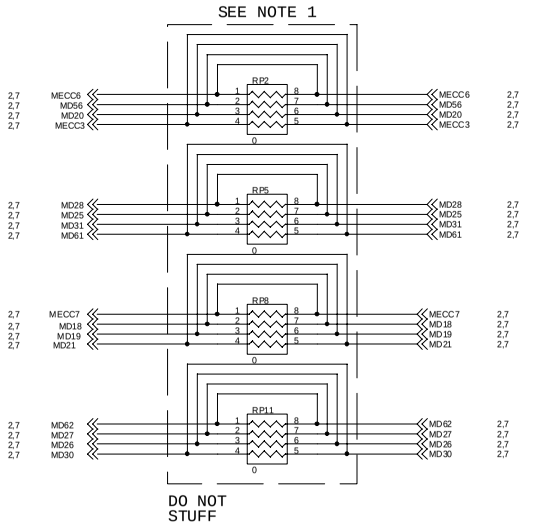


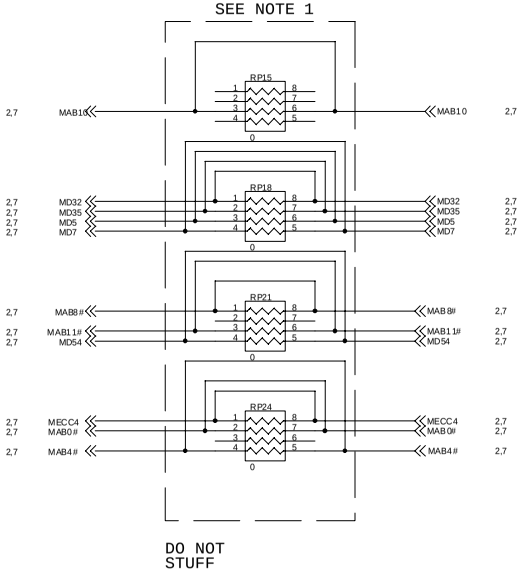


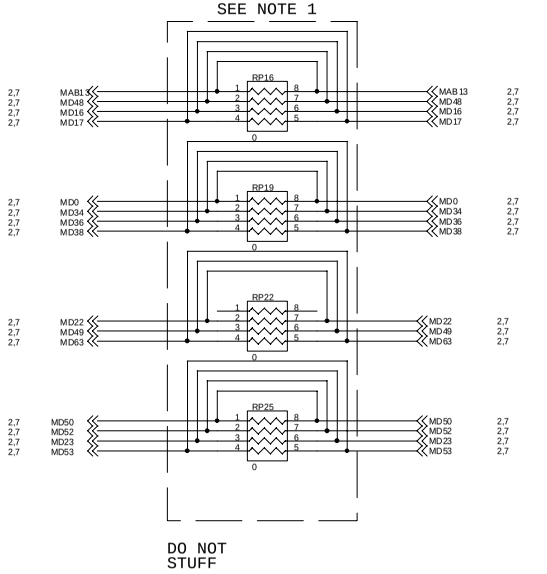
Title	Interposer II - Level Shifters/Power Sequencing	
Size C	Document Number XXXX-XXX	Rev C
Date: Monday, October 18, 1999	Sheet 3 of 7	

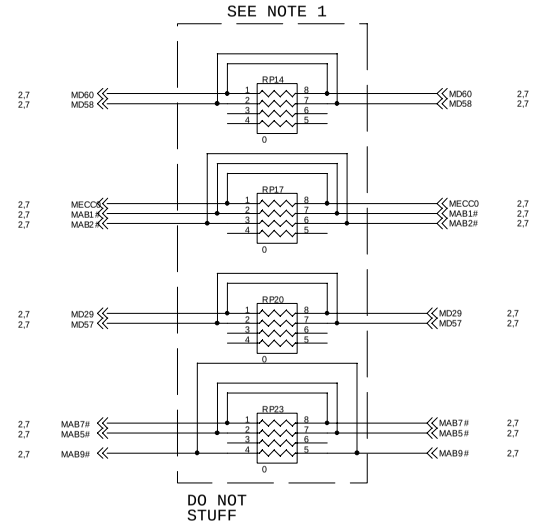


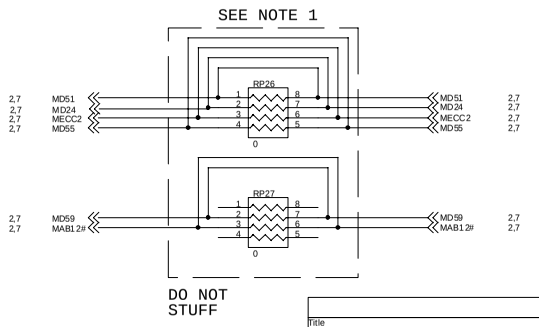












NOTE 1: Use R-PACK pad geometry. Shunt pads with trace. Route on surface (cuttable)

Title: SERIES TERMINATION		
Size: C	Document Number: <Doc>	Rev: C
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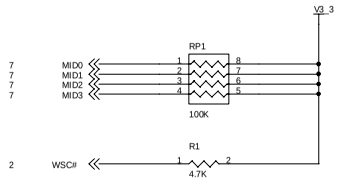
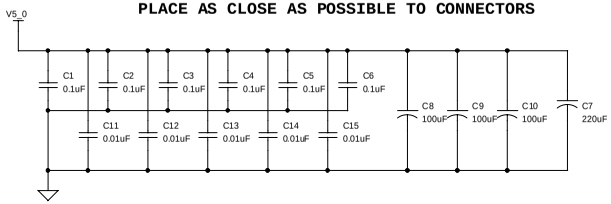
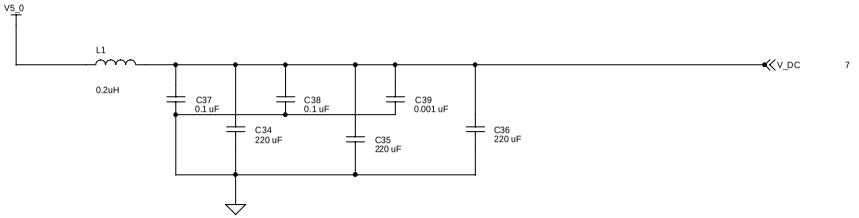
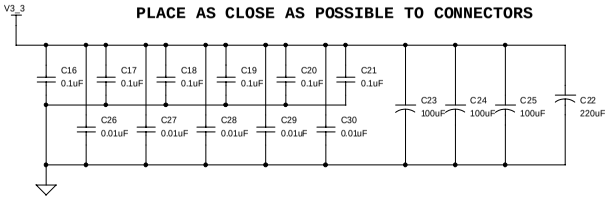


PLACE AS CLOSE AS POSSIBLE TO CONNECTORS





PLACE AS CLOSE AS POSSIBLE TO CONNECTORS



Title	DECOUPLING/PULLUPS	
Size C	Document Number <Doc>	Rev C
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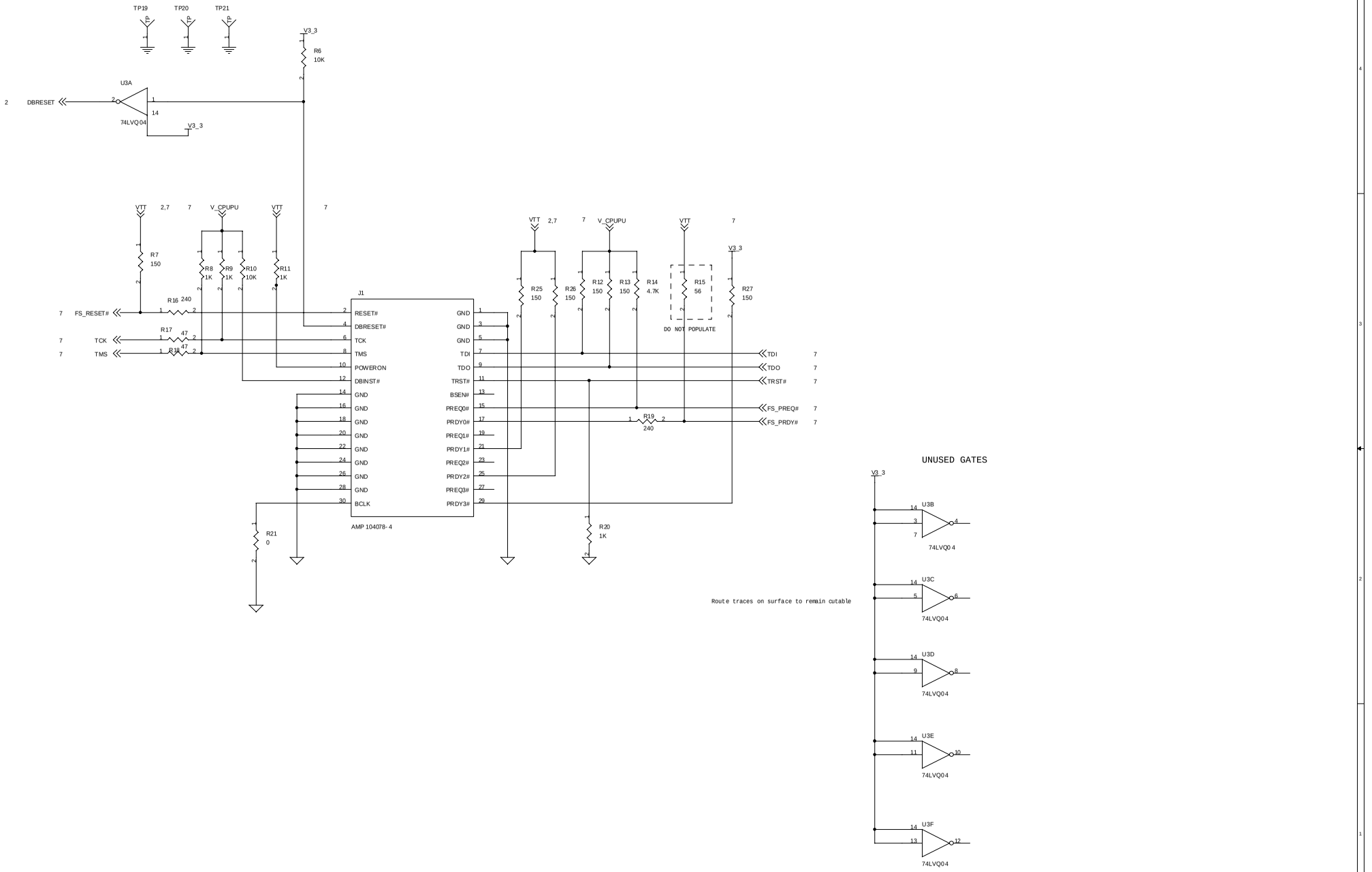
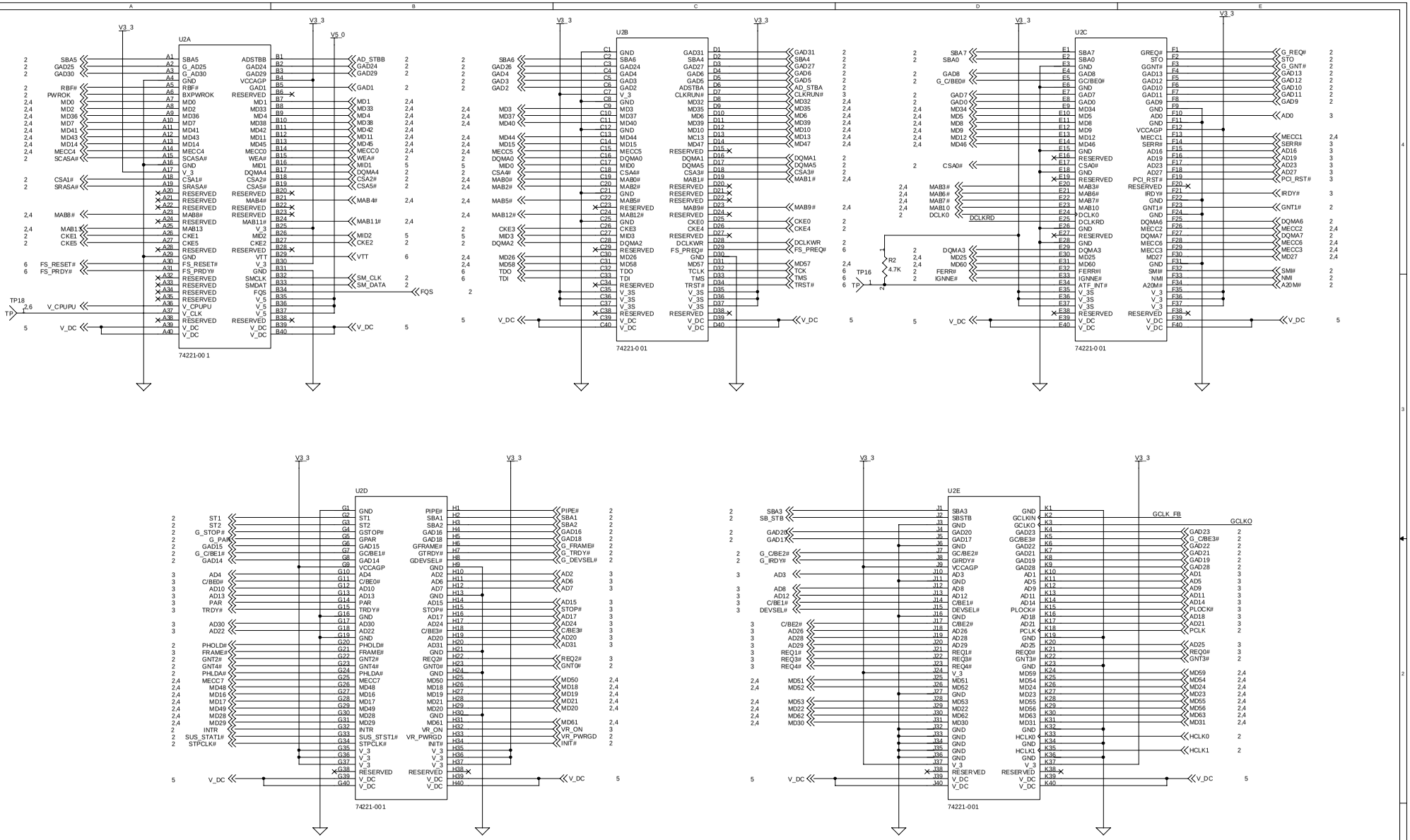


Title	ITP PORT	
Size C	Document Number <Doc>	Rev C
Date:	Sheet 6 of 7	


U2A
74221-00 1
U2B
74221-0 01
U2C
74221-0 01
U2D
74221-001
U2E
74221-001
No stub on DCLKWR pad of
R54 (place inline trace)
Do not populate
AGP clock signals
GCLK_FB length must
equal 10.77"
Place Near Module
connector
Title
Module connector
Size
C
Document Number
<Doc>
Rev
C
Date:
Monday, October 18, 1999
Sheet
7
of
7