

Pentium(r) II Processor - Low Power
Customer Reference Board
Revision C

History

from rev A to rev B

1. Changed AGP topology(GCLK0 on modular connector page)

These schematics only support the Intel Pentium(r) II Processor Mobile Module at 266MHz and 333MHz.

From Rev B to Rev C

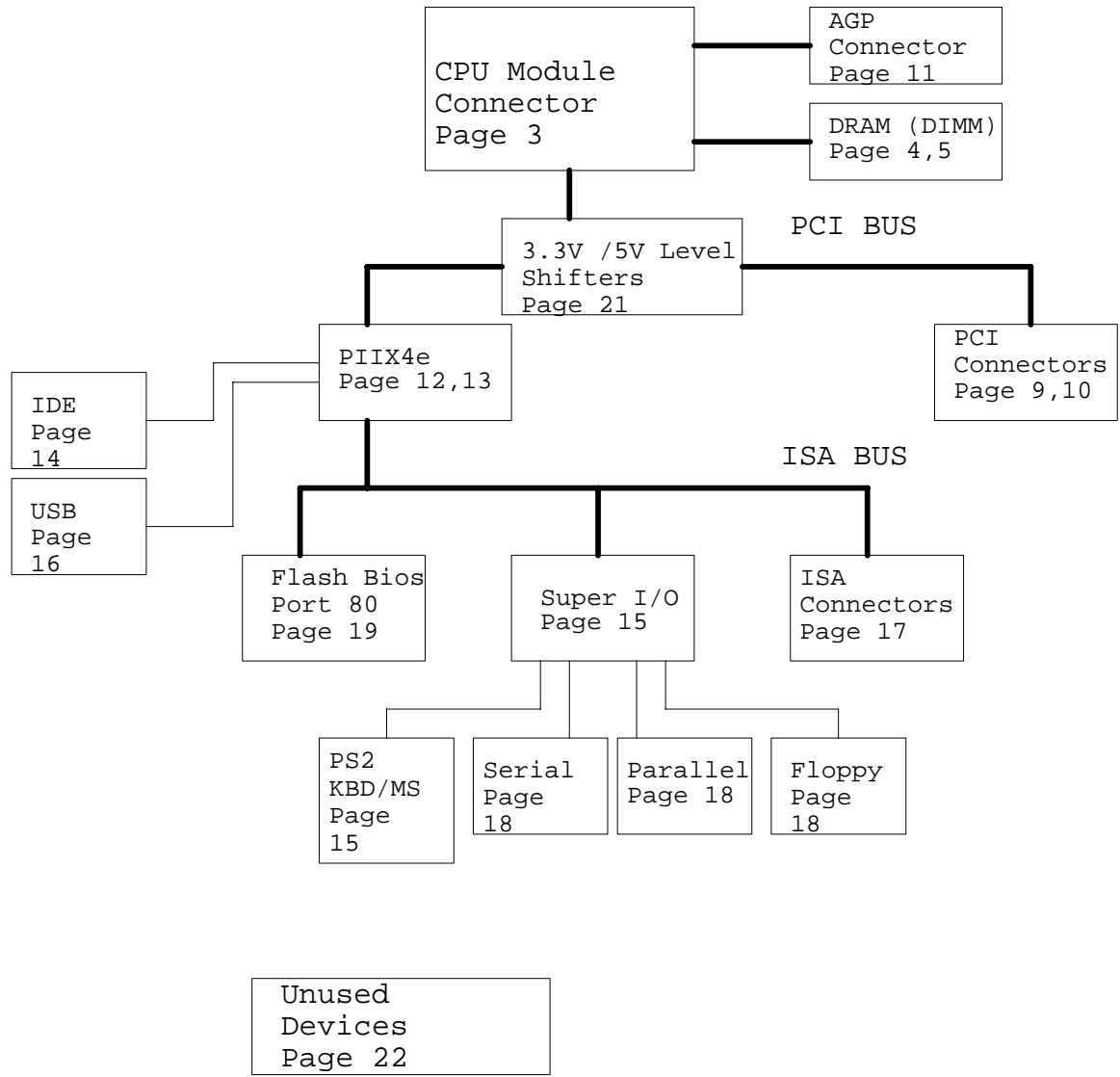
2. Removed 10K pullup on FQS signal page 8.
3. Added 10K pullup on SEL_SS signal page 8.

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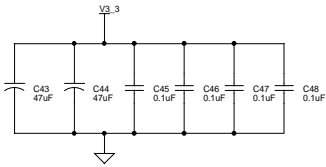
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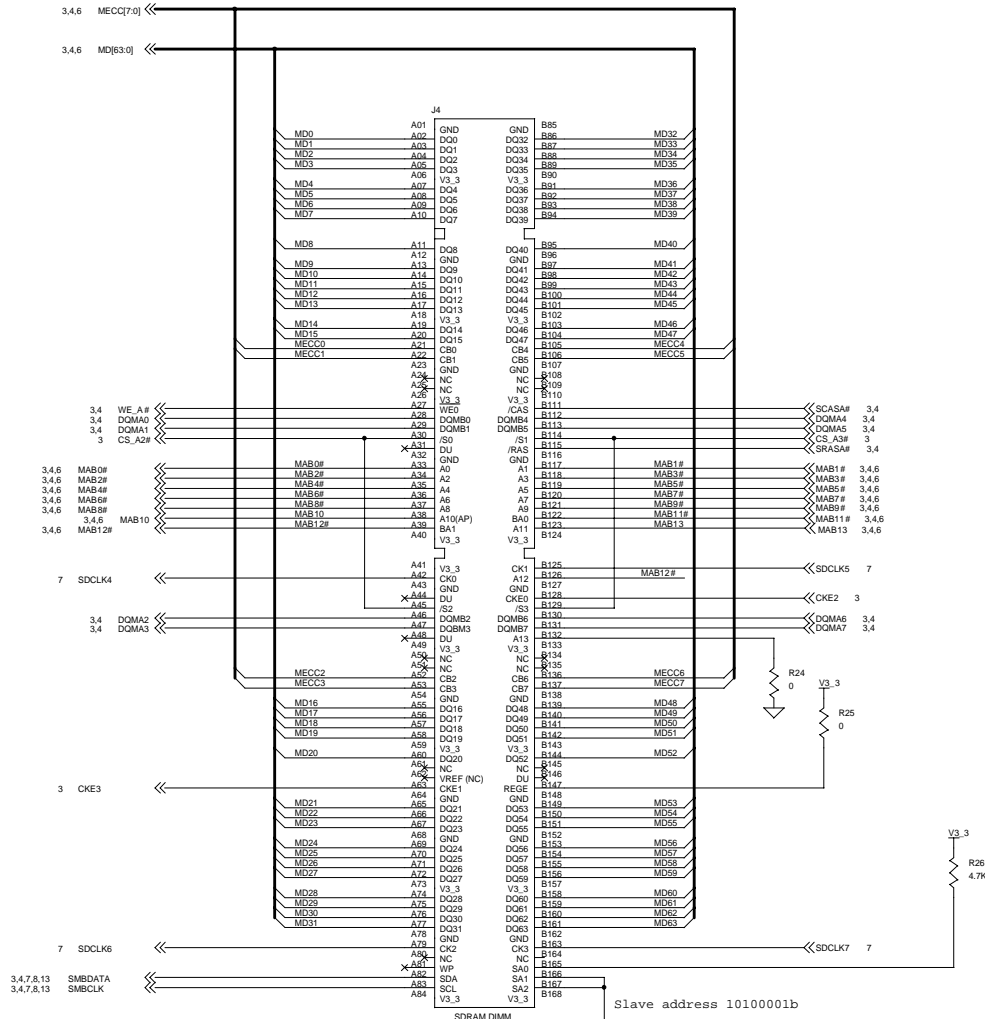


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Title			Block Diagram		
Size	Document Number	Rev			
C	<Doc>	B			
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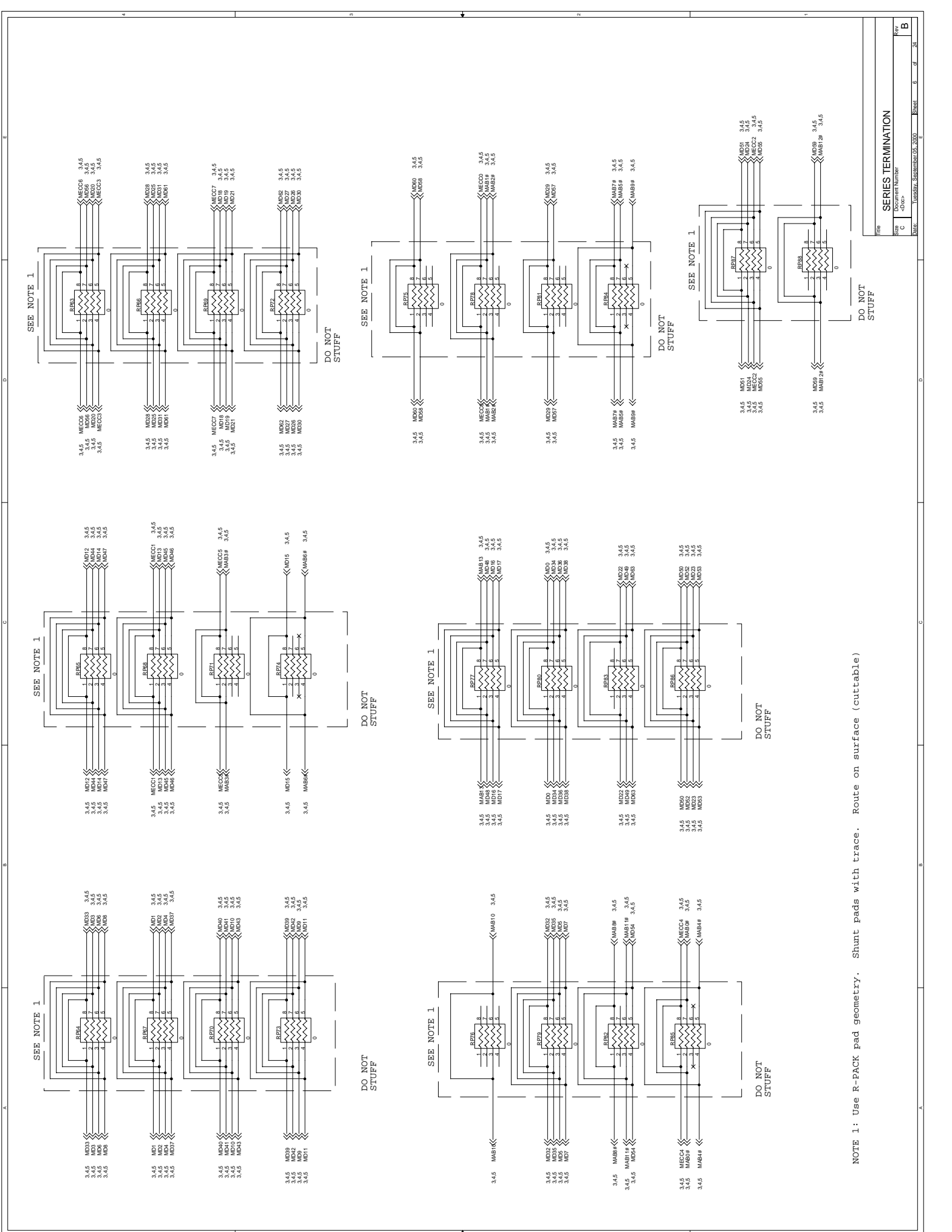


Socket 1



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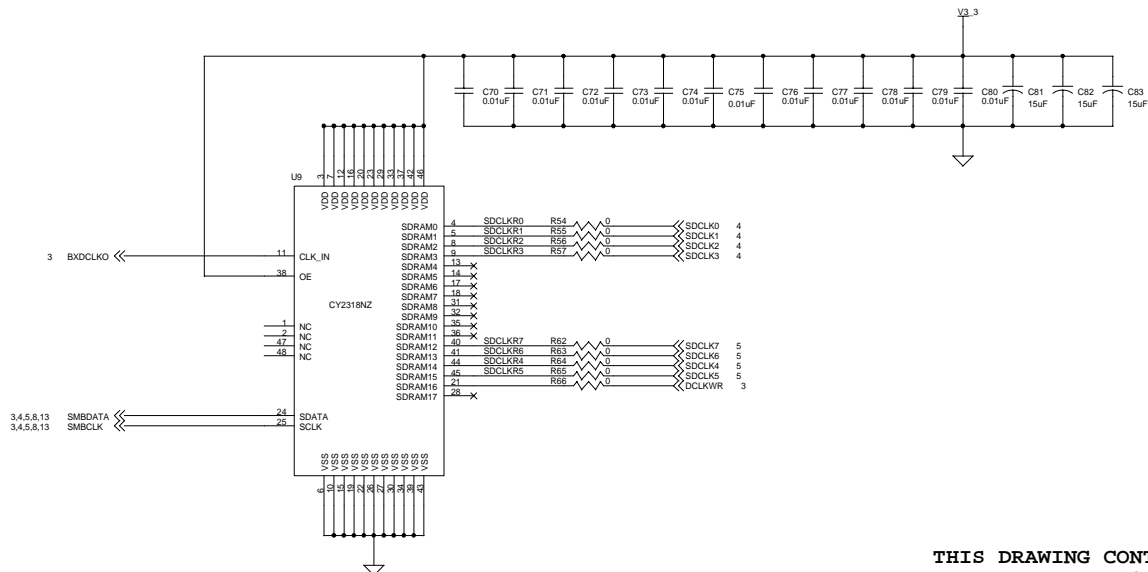
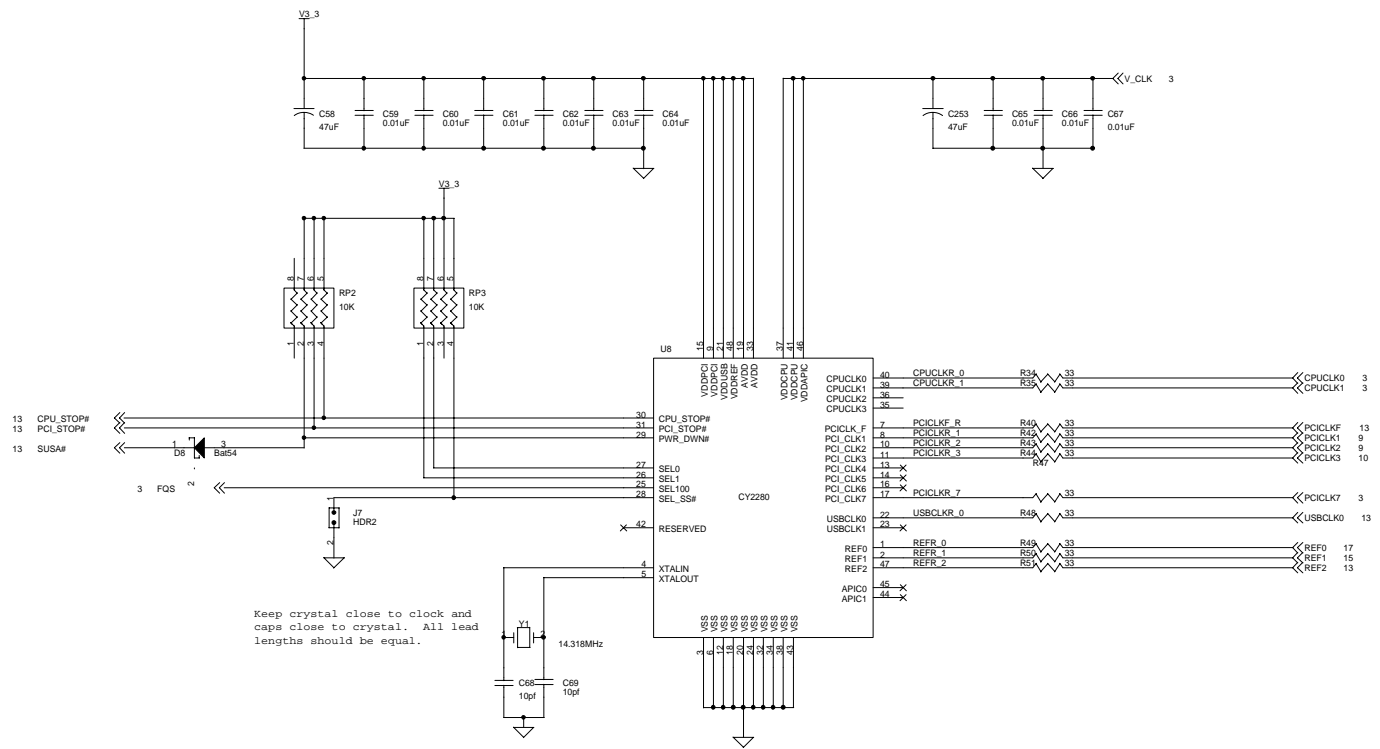
NOTE 1: Use R-PACK pad geometry. Shunt pads with trace. Route on surface (cuttable)

SERIES TERMINATION

Docuement Number
 01-001
 Rev: 0

Project: 01-001-001
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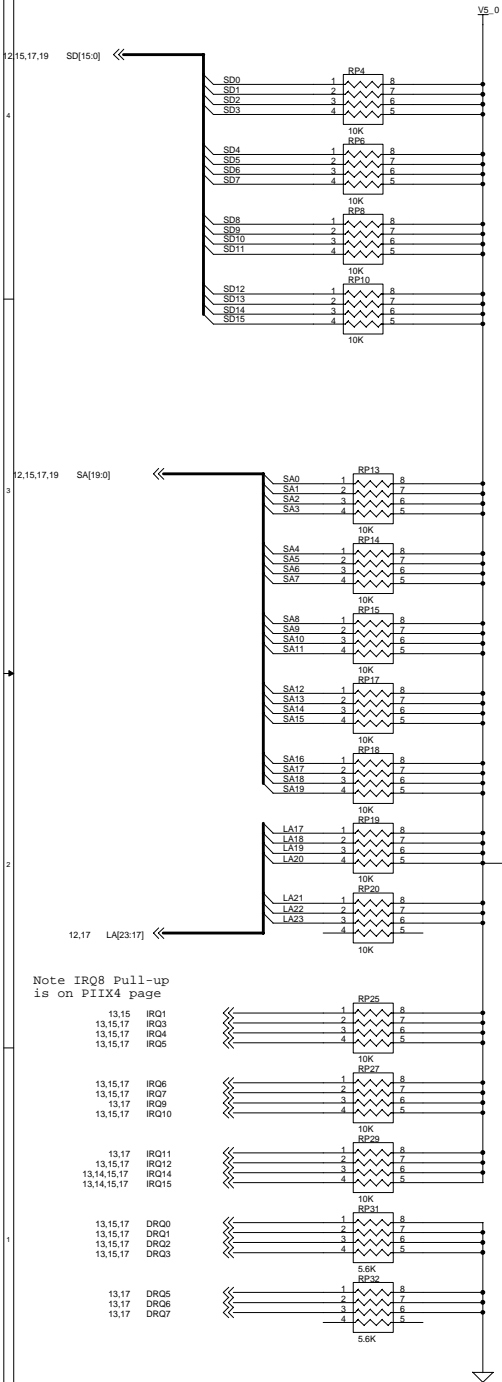
B



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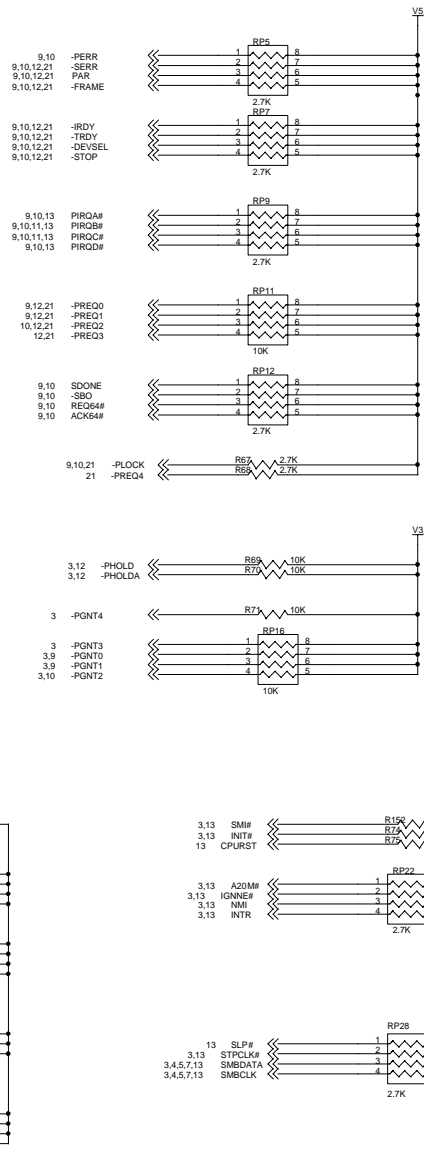
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ISA Pullups



Note IRQ8 Pull-up is on PIIX4 page

PCI Pullups



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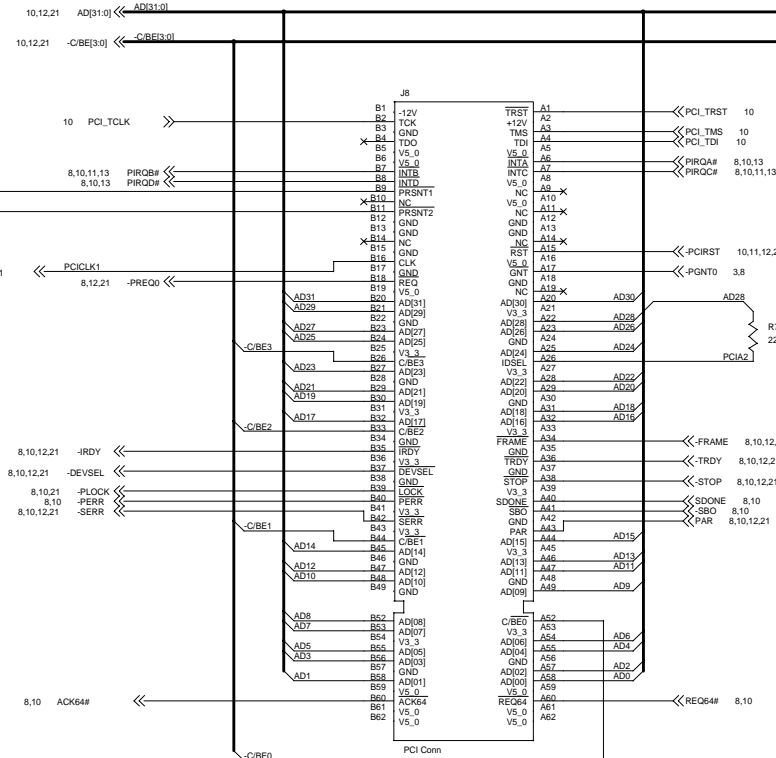
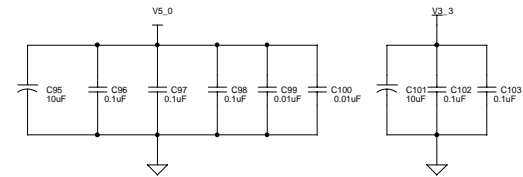
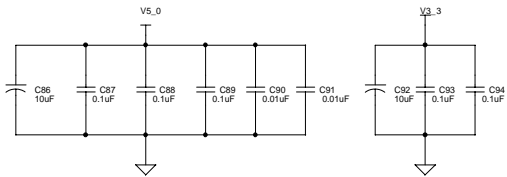
J8/J9 V5_0:
A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
B5, B6, B19, B22, B59, B61, B62

J8/J9 V3_3:
A21, A27, A33, A39, A45, A53
B25, B31, B36, B41, B43, B54

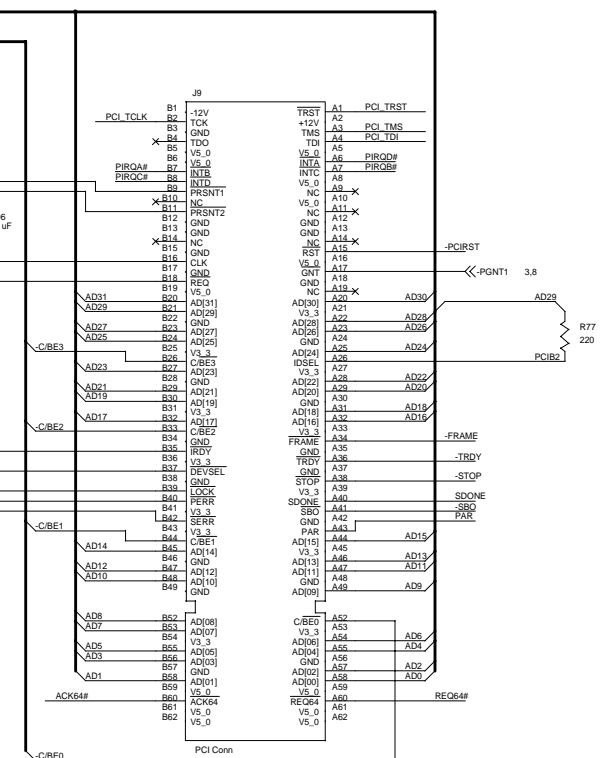
J8/J9 NC:
A9, A11, A14, A19
B10, B14

J8/J9 GND:
A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
B3, B12, B13, B15, B17, B28, B34, B38, B46, B49,
B57

J8/J9 +12V: A2
-12V: B1



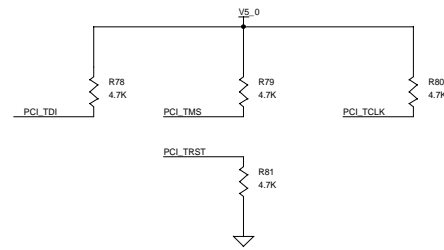
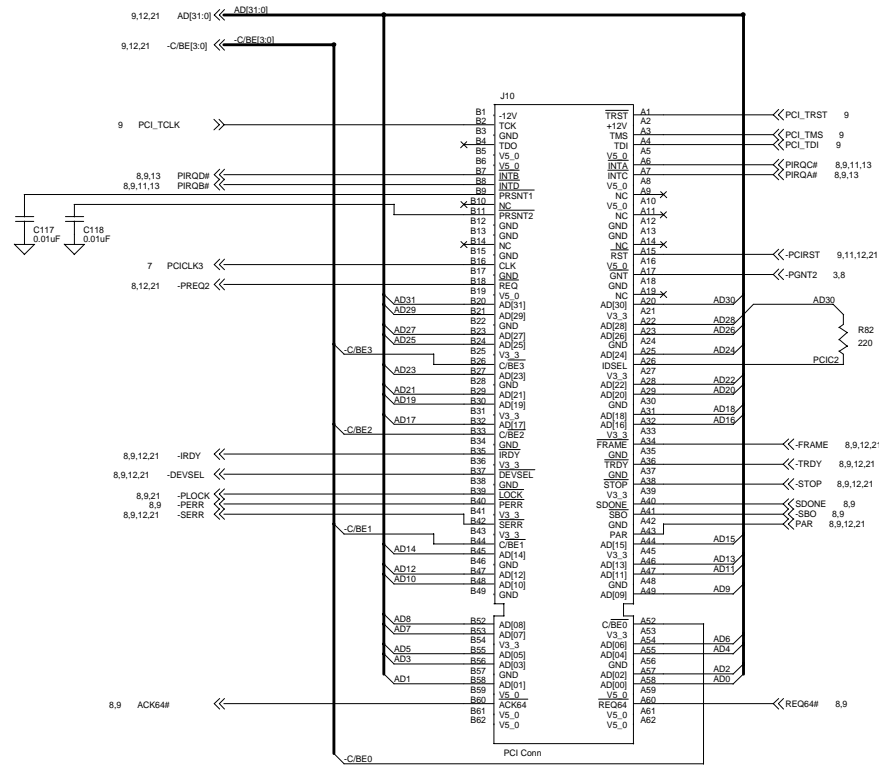
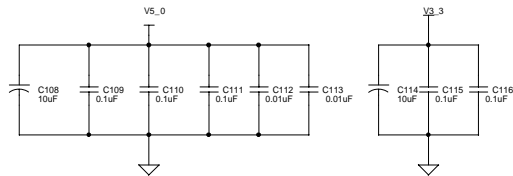
PCI SLOT 0



PCI SLOT 1

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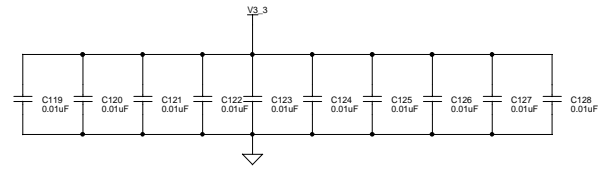
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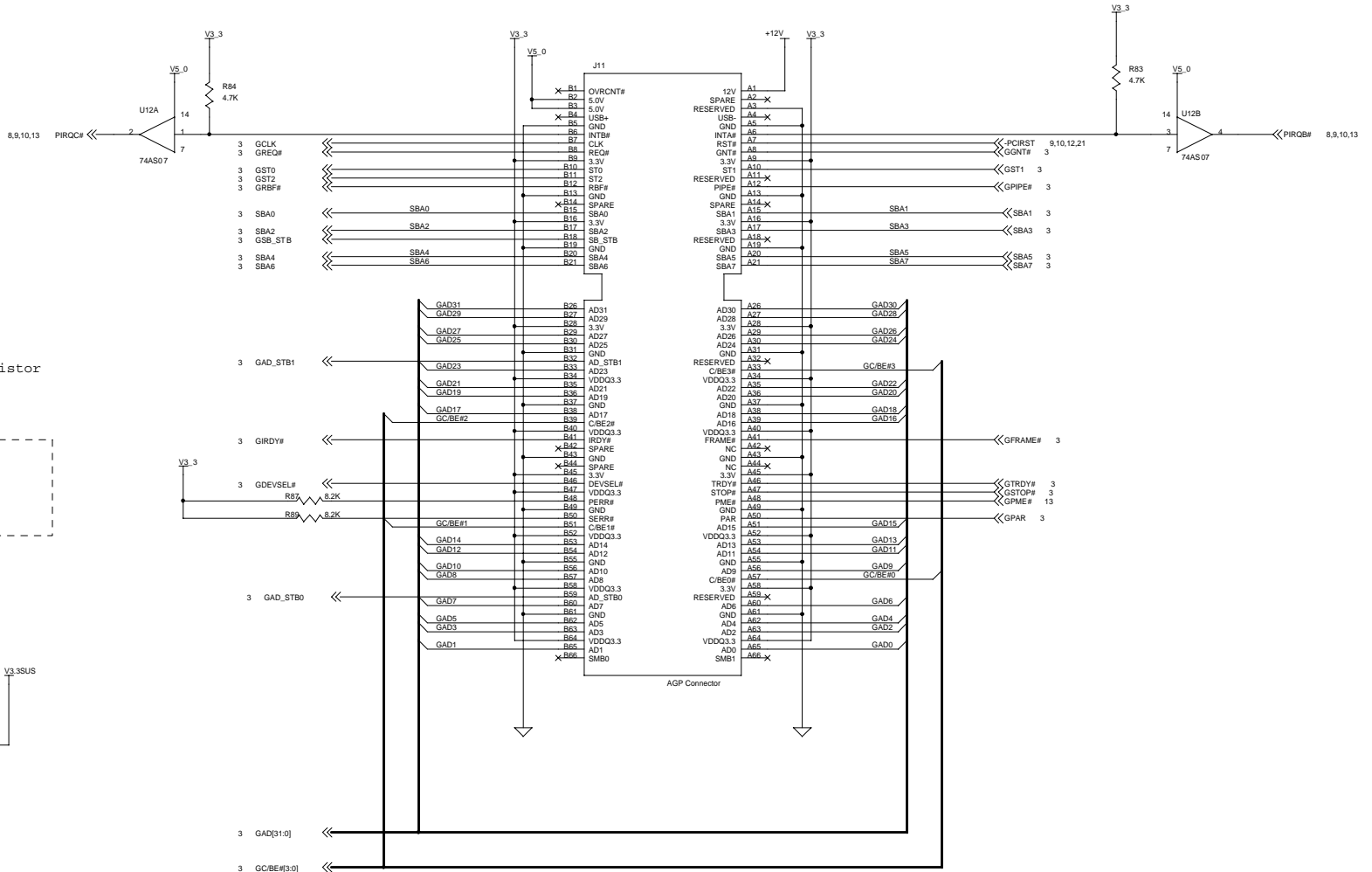
PCI SLOT 2

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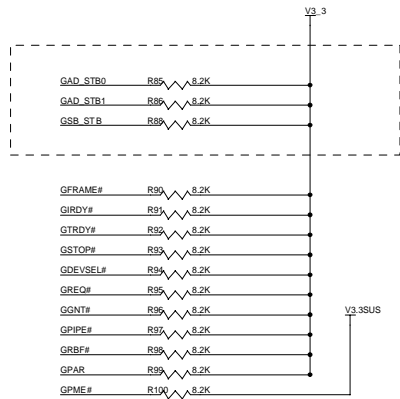
Title		PCI Slot 2	
Size	Document Number	Rev	
C	<Doc>	B	
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Pin A3 is tied to ground per AGP Specification Rev 1.0

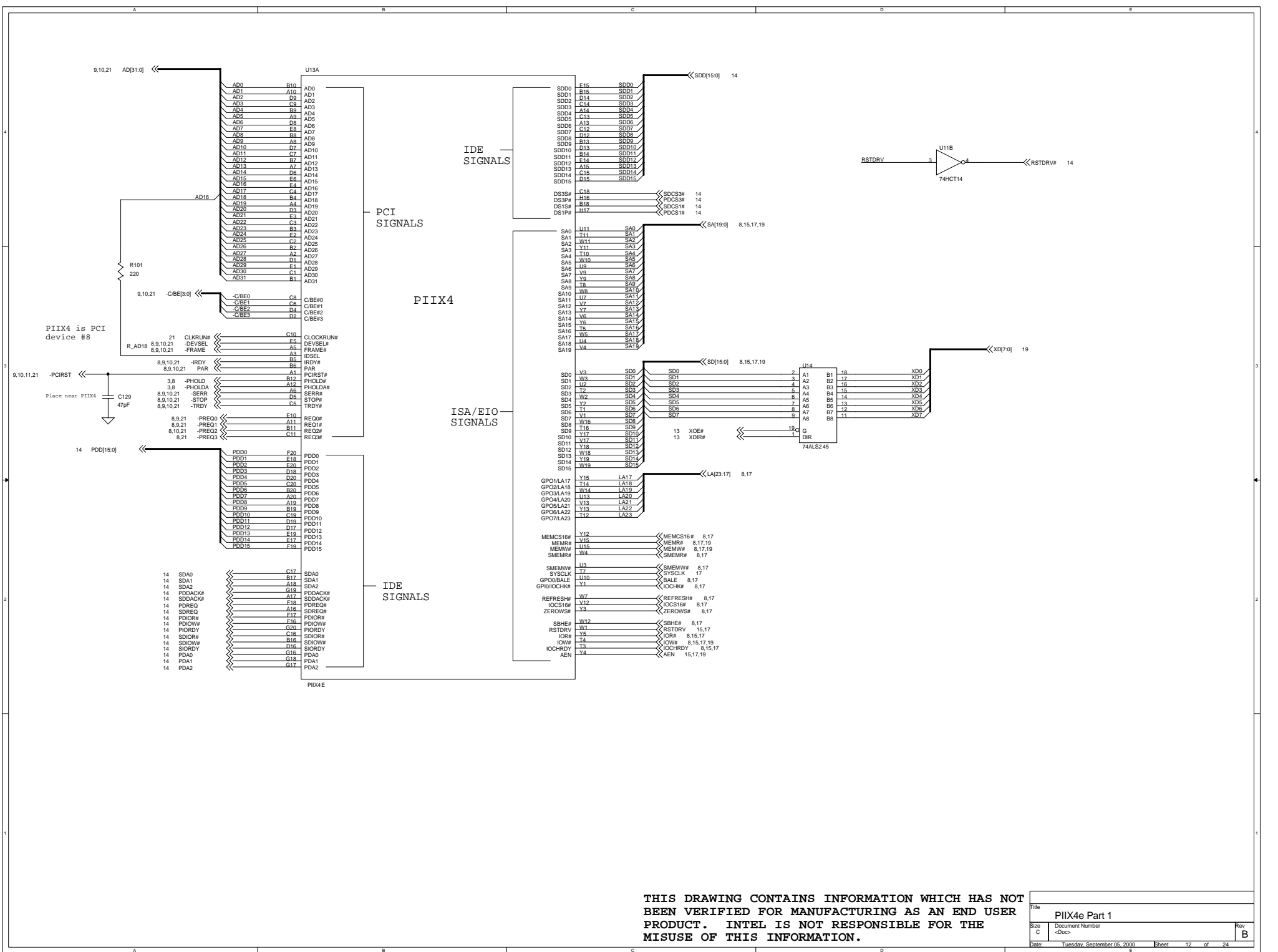


Stub length from connector to resistor must be less than 0.1"



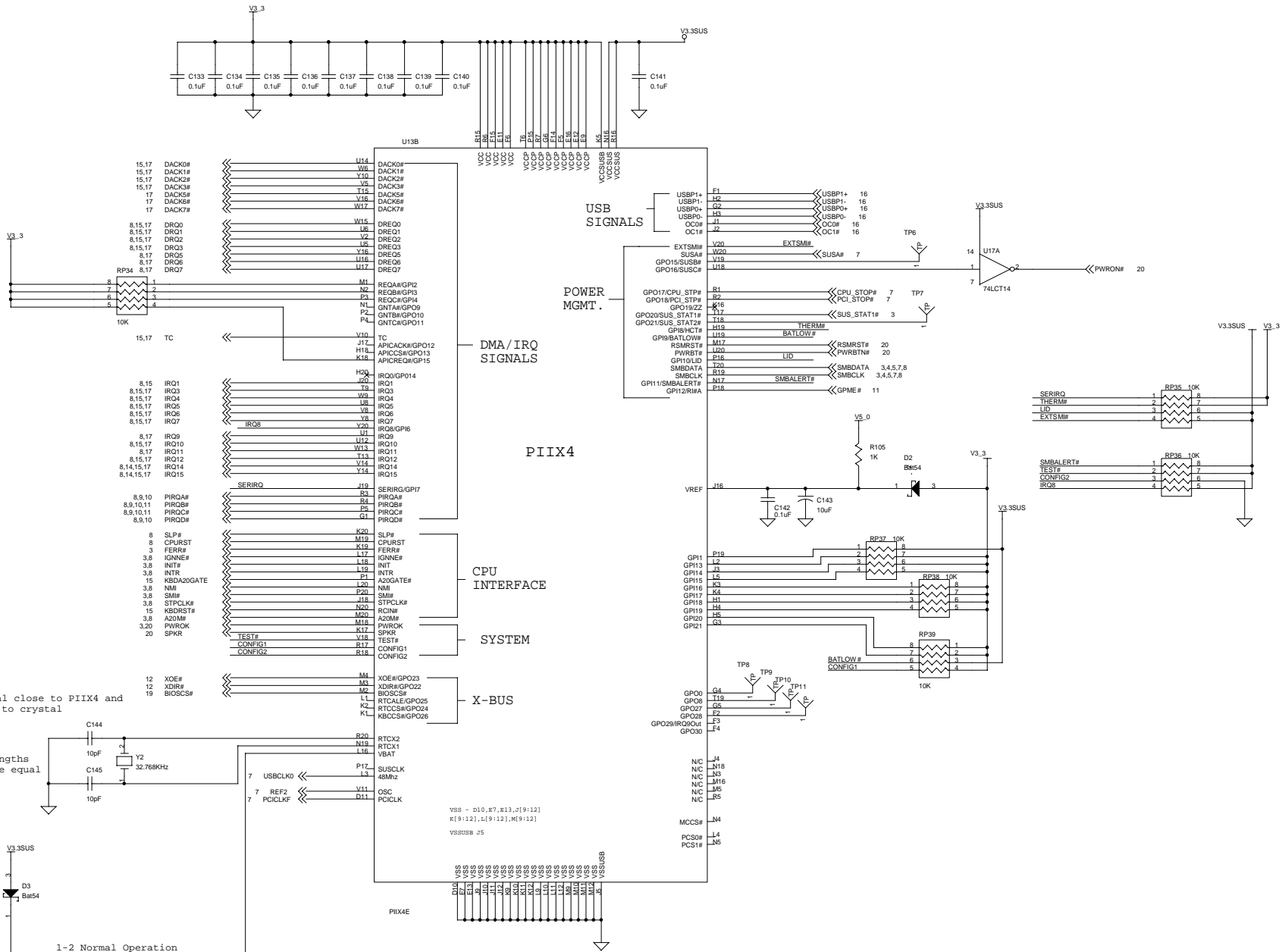
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Title		AGP Connector	
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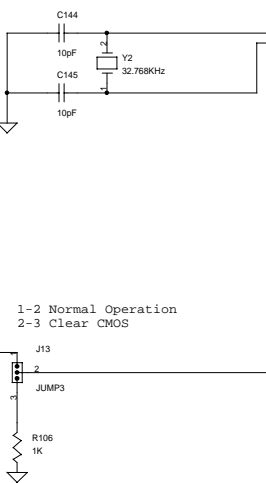
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Title		PIIX4e Part 1	
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Rev	B		



Keep crystal close to PIIx4 and caps close to crystal

Trace lengths should be equal

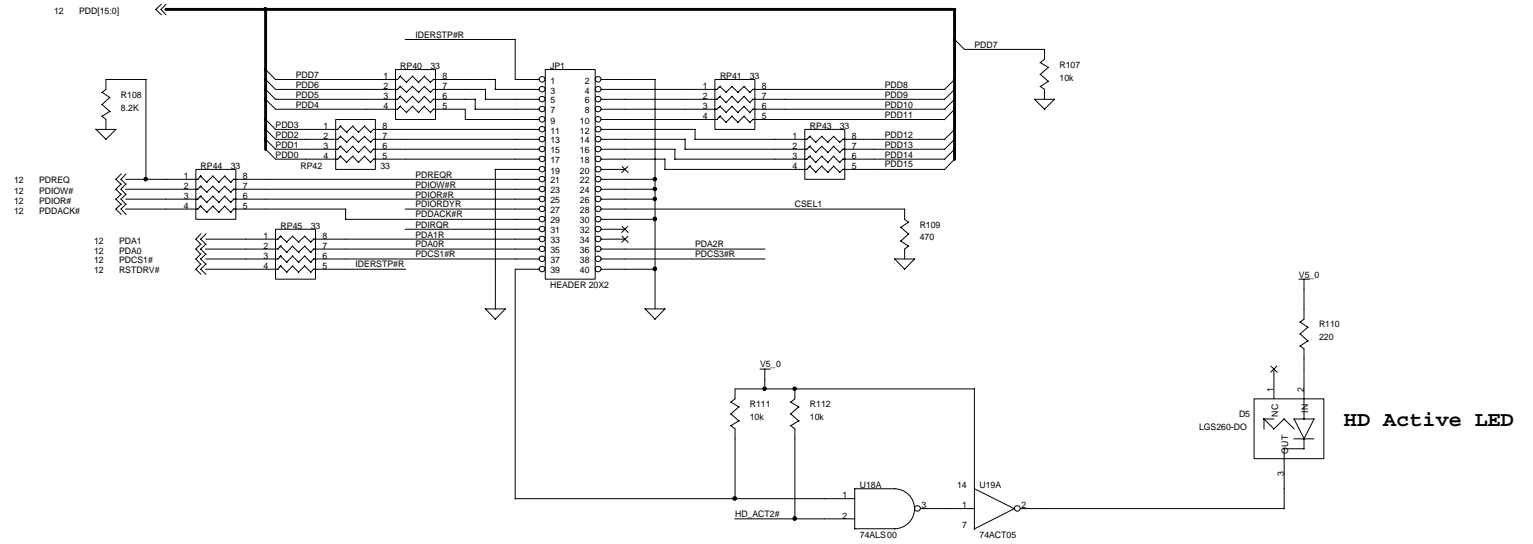


1-2 Normal Operation
2-3 Clear CMOS

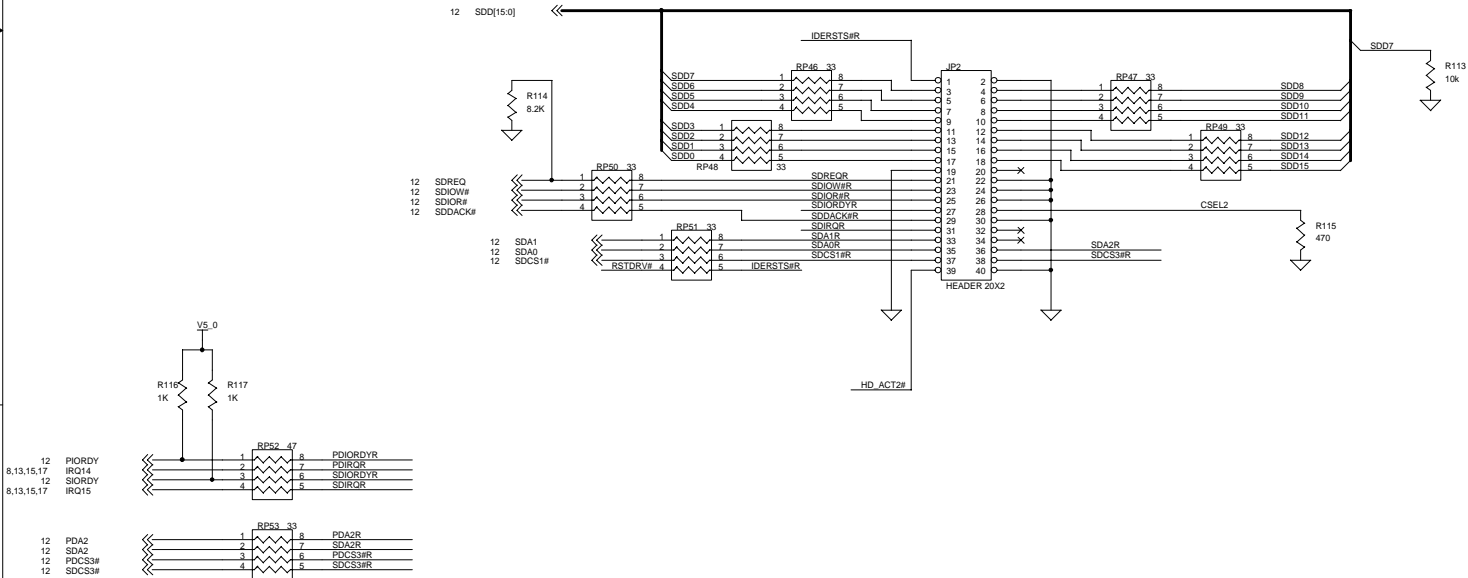
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Title	PiiX4e Part 2		Rev	B
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Primary IDE Connector

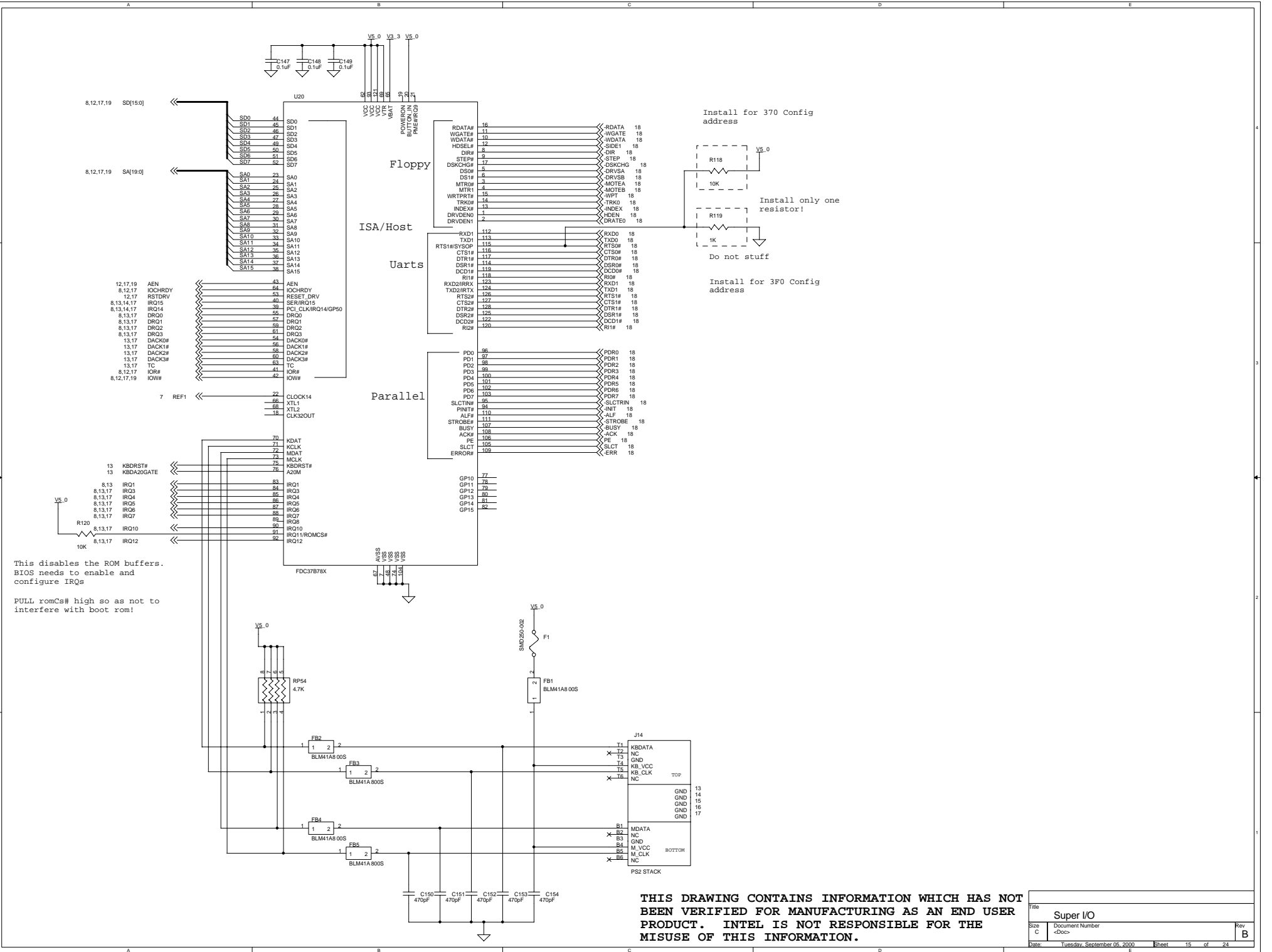


Secondary IDE Connector



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Title		IDE Connectors	
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Rev			B



This disables the ROM buffers. BIOS needs to enable and configure IRQs

PULL romCs# high so as not to interfere with boot rom!

Install for 370 Config address

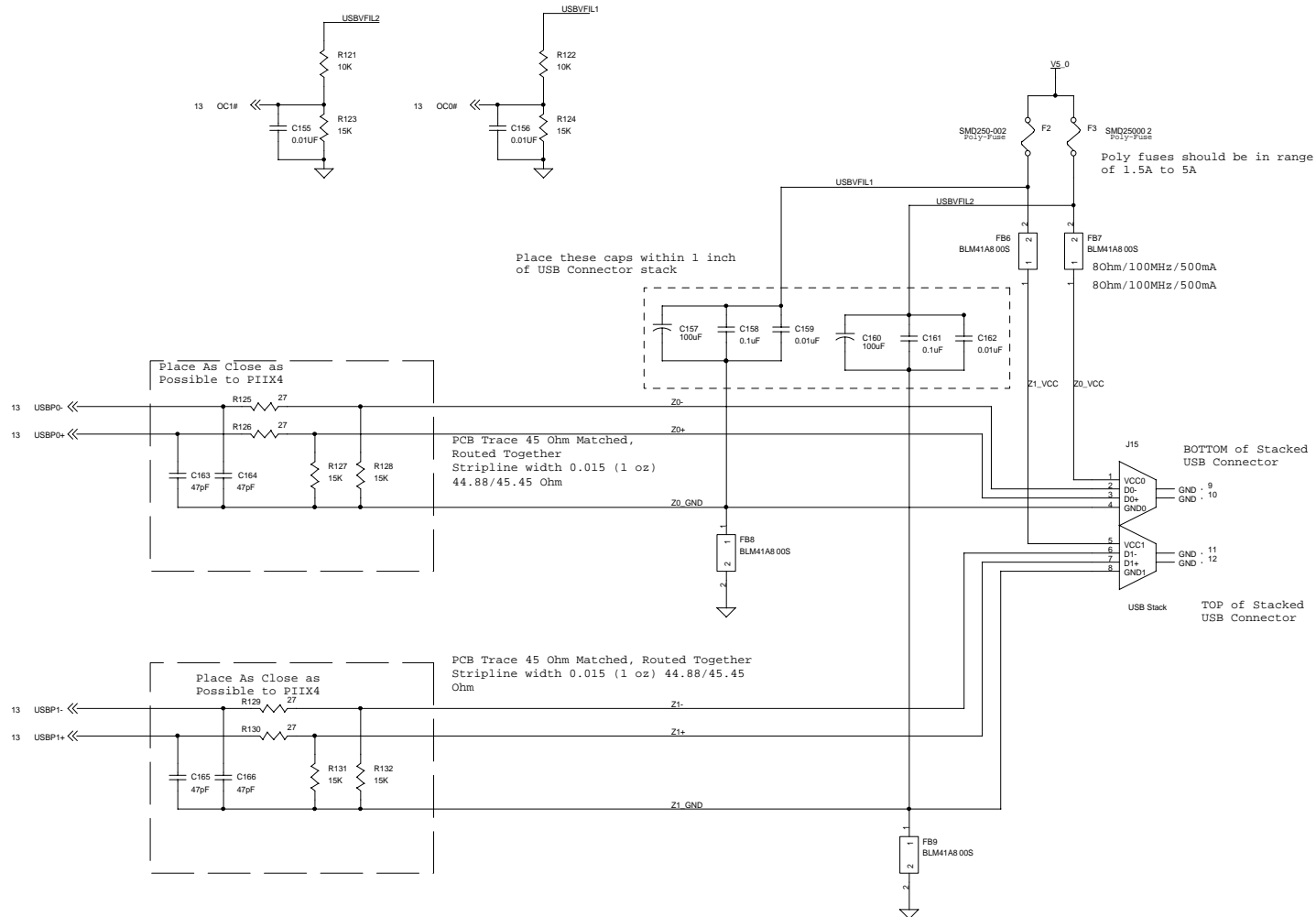
Install only one resistor!

Do not stuff

Install for 3F0 Config address

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Title		Super I/O	
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NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or double space to any other signal.

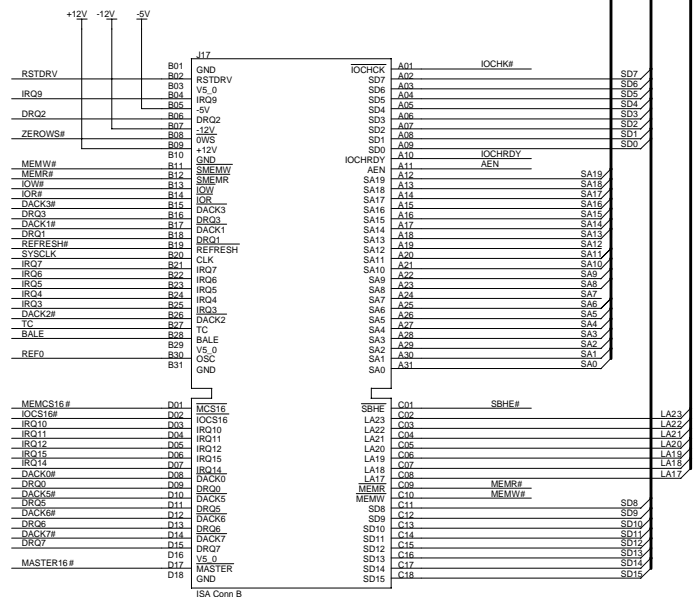
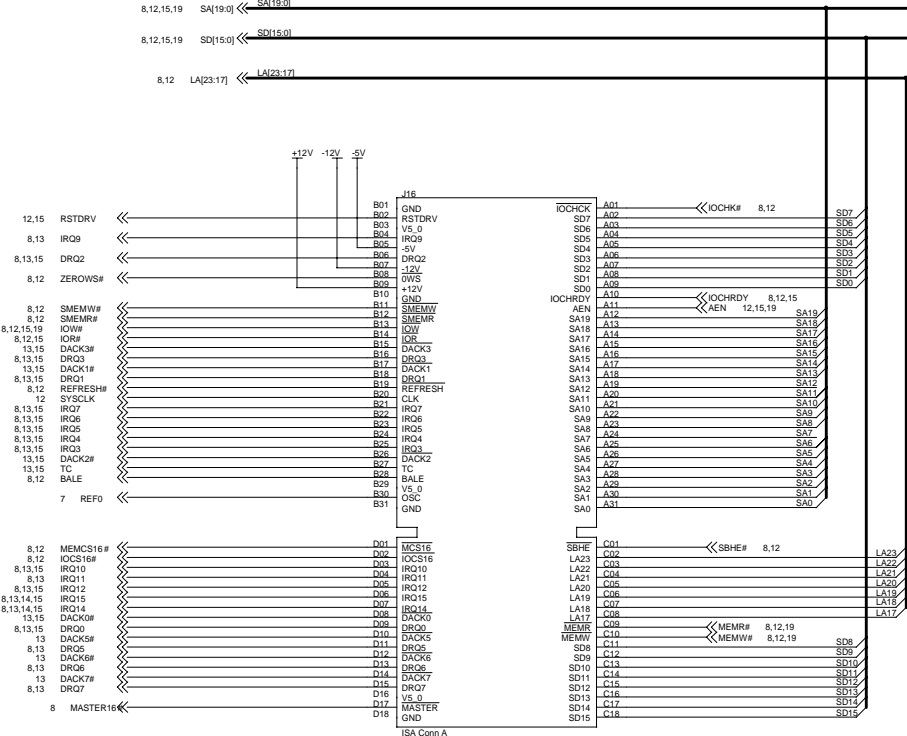
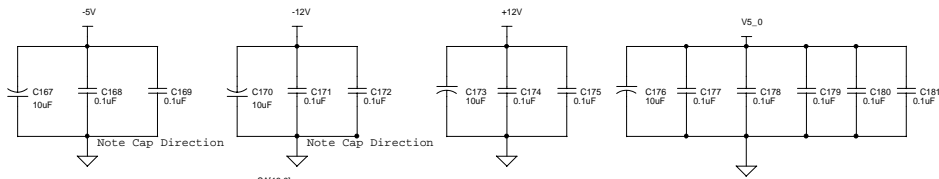
NOTE 3: Place ferrites at connector.

NOTE 4: Poly-fuse min 1.5A
max 5A.

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Title		USB Connectors	
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ISA Slots



J16/J17 V5_0:
B03, B29, B31, D16

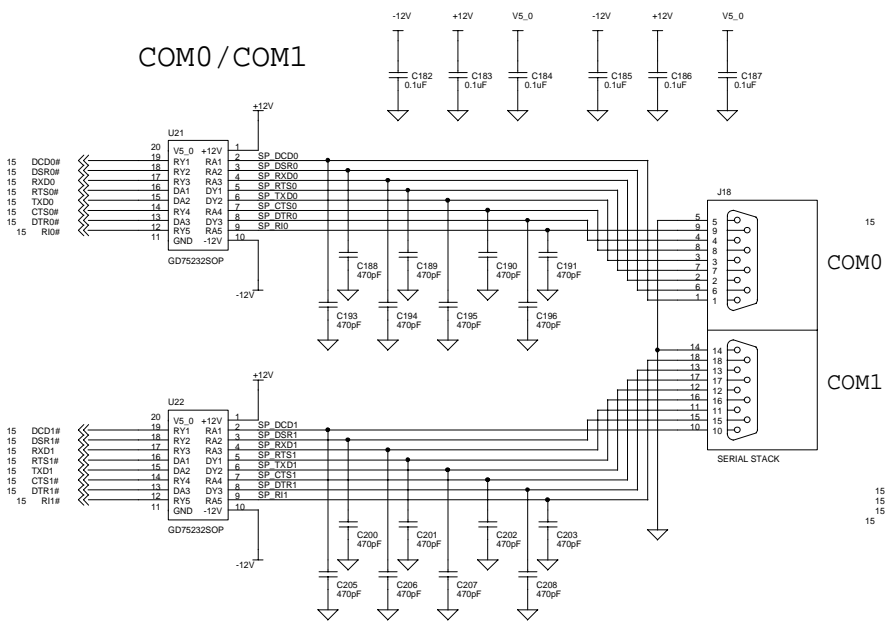
J16/J17 GND:
B01, B10, D18

J16/J17: +12V B09
-12V B07
-5V B05

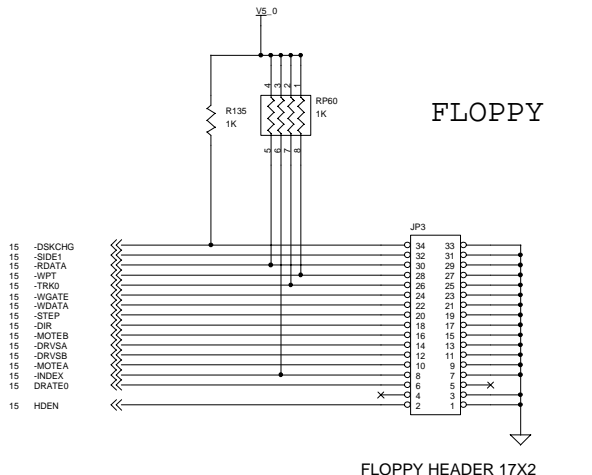
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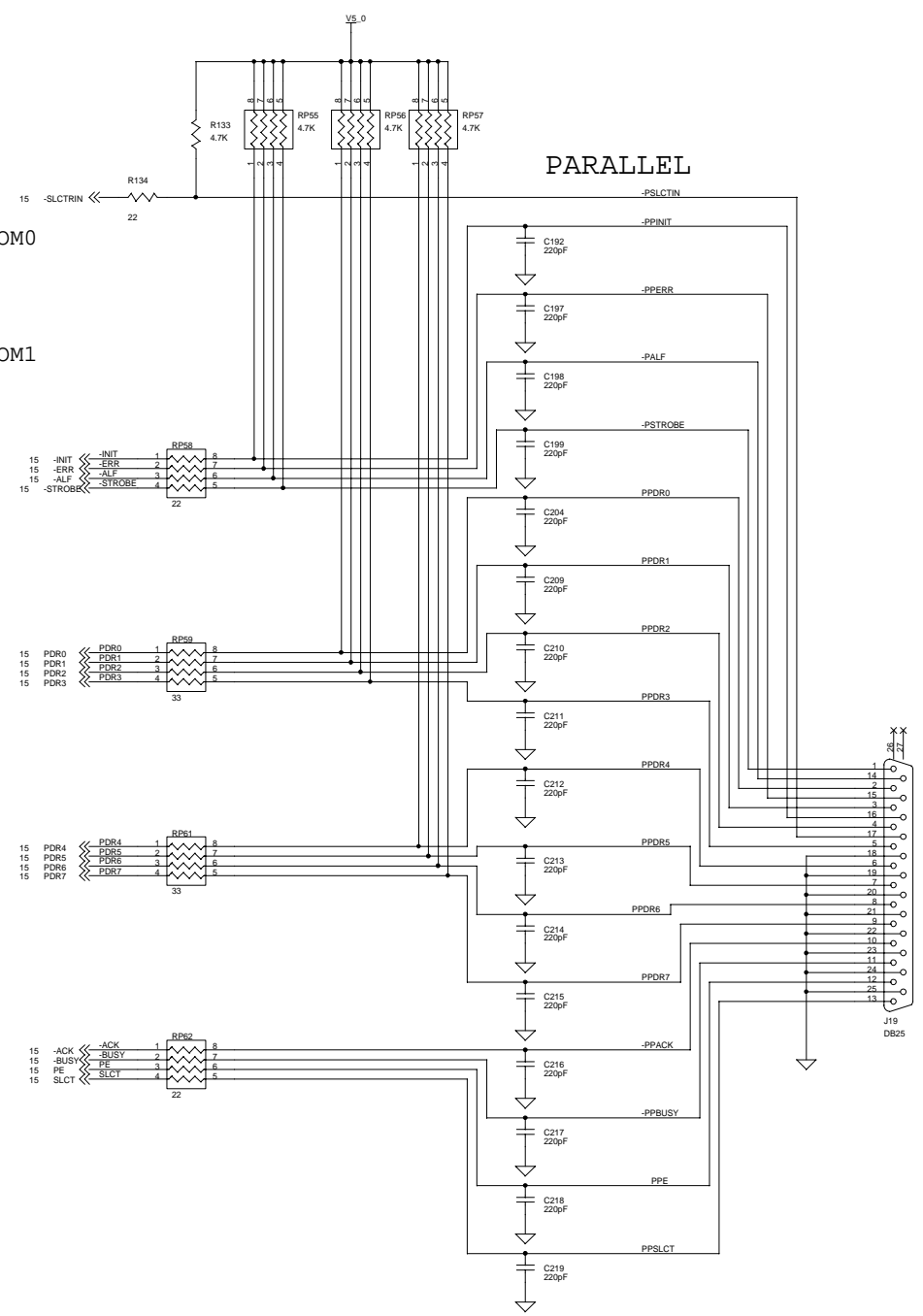
COM0 / COM1



FLOPPY

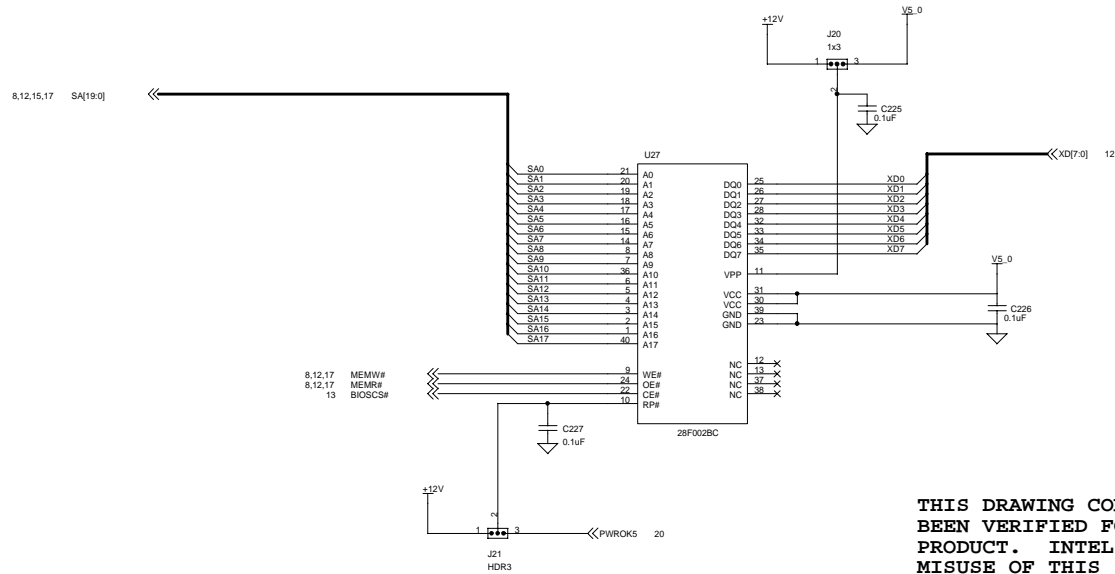
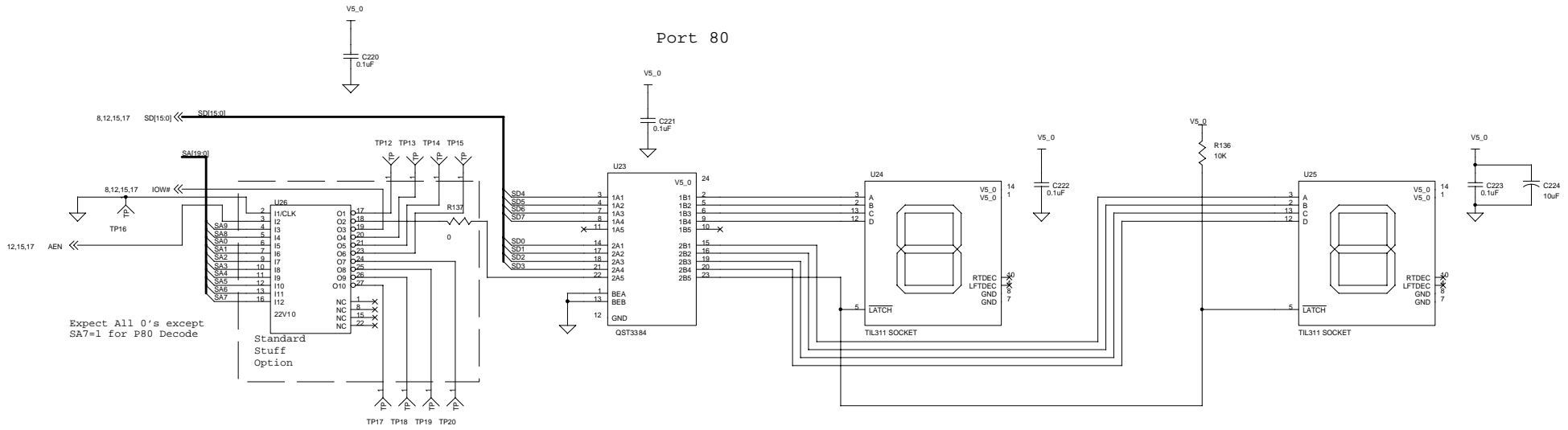


PARALLEL



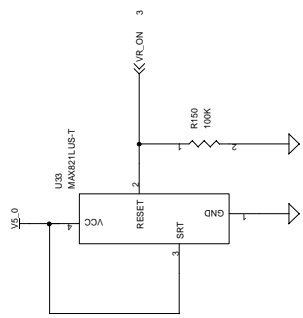
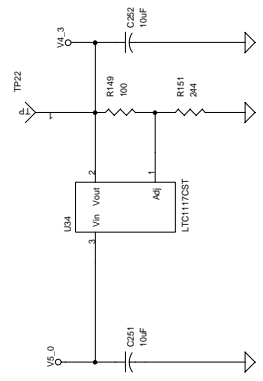
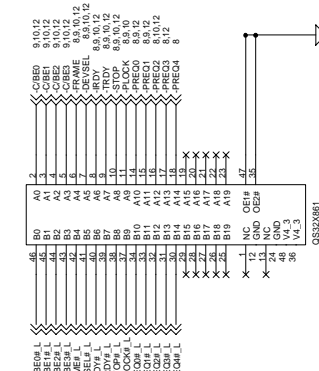
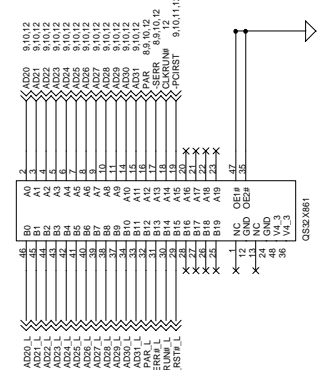
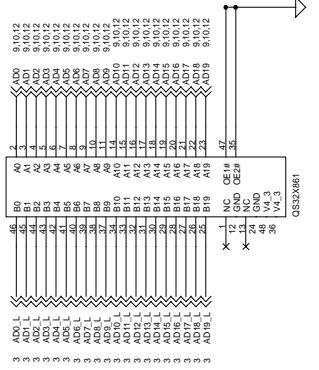
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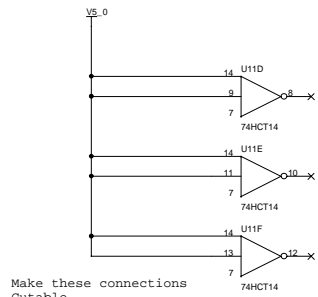
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Size	Document Number	Rev	
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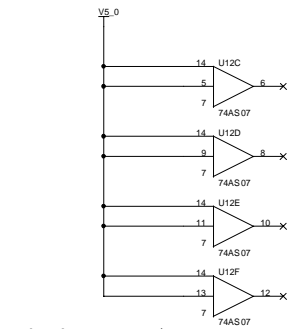
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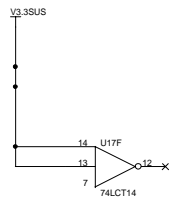




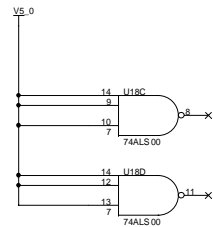
Make these connections
Cuttable



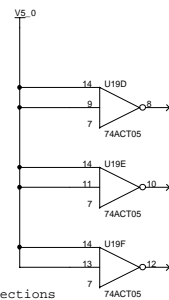
Make these connections
Cuttable



Make these connections
Cuttable



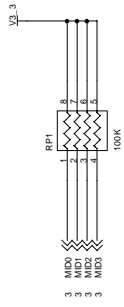
Make these connections
Cuttable



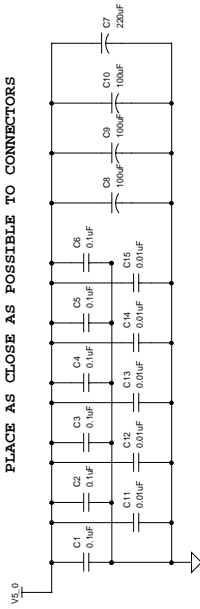
Make these connections
Cuttable

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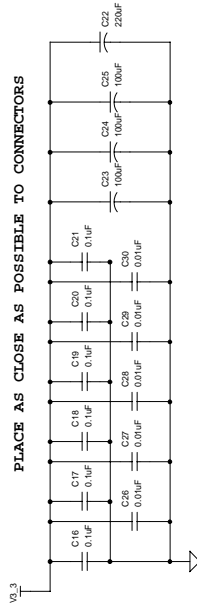
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Size C	Document Number «Doc»	Rev B
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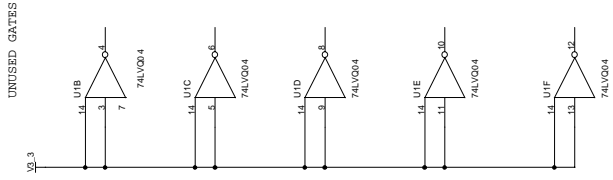
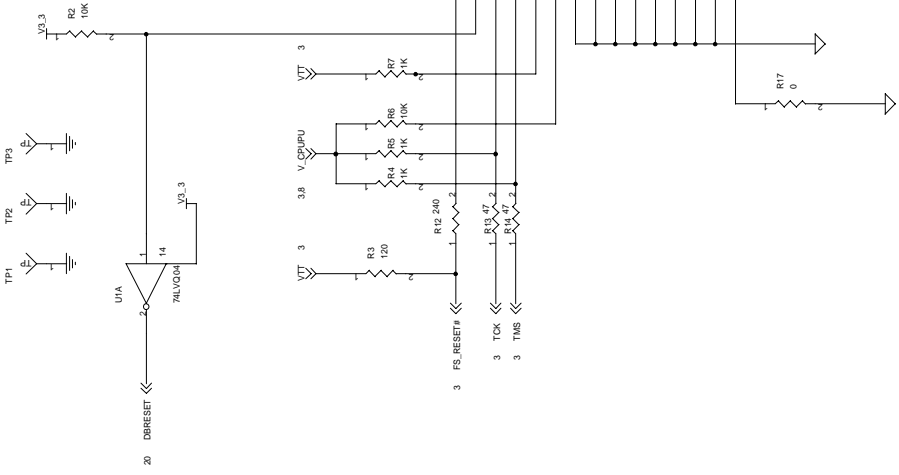


PLACE AS CLOSE AS POSSIBLE TO CONNECTORS



PLACE AS CLOSE AS POSSIBLE TO CONNECTORS





Route traces on surface to remain outable