Intel® 460GX Chipset

Specification Update

January 2002

Notice: The Intel® 460GX chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

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Revision History

Version Number	Description	Date
001	Initial release of this document.	June 2001
002	Added SAC erratum 2, MAC Specification Clarification 1, and WXB Specification Clarifications 2-3.	January 2002

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document #
Intel® 82460GX Chipset Datasheet	248703
Intel® 82460GX Chipset System Software Developer's Manual	248704

Nomenclature

Errata are design defects or errors. These may cause the product's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications for the Itanium processor. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Codes Used in Summary Table of Changes

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of this document.

Part 1: Specification Update for the 82461GX (SAC)

Identification Information

Type	Stepping	Revision ID	S-Spec
82461GX (SAC)	B-1	03h	SL54U

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82461GX (SAC) component. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	B-1			
1	X	13	NoFix	Strobe pair restrictions for boundary scan testing
2	X	13	NoFix	Chipset may livelock if loop claims exclusive ownership and does not modify data

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
			None for this revision of the specification update

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. Strobe pair restrictions for boundary scan testing

Problem: On the SAC component, there is a boundary scan 1149.1 specification violation on the Expander bus interface strobe pairs (HSTBN#, HSTBP#). The current implementation includes a boundary scan cell for each strobe in a differential pair. Because of this, a “01” or “10” pattern is the only valid pattern to load into the strobe boundary scan cells. If a “00” or a “11” pattern were scanned into the strobe pair boundary scan cells, the differential amplifier on the receiver could not deterministically resolve the signals to a known value.

Implication: For the Expander bus interface strobe pairs (HSTBN#, HSTBP#), only “01” or “10” may be scanned into the boundary scan cells.

Workaround: Automatic Test Pattern Generator software can be programmed to only create the “01” or “10” for each of the pairs. This could be done by defining the pair as a differential pair in the software.

Status: For the steppings affected, see the Summary Table of Changes.

2. Chipset may livelock if loop claims exclusive ownership and does not modify data

Problem: The ld.bias instruction provides a hint for a processor to acquire exclusive ownership of the accessed cache line. If a loop uses ld.bias to gain exclusive ownership of a cache line and does not actually modify the cache line, it is possible that the SAC will starve other processors trying to access the cache line, creating a chipset livelock condition.

Implication: The chipset may encounter a livelock in the situation described above resulting in a hang condition. However, in an operating system environment, any interrupt such as a timer interrupt may break the livelock.

Workaround: Firmware may contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

Part 2: Specification Update for the 82462GX (SDC)

Identification Information

Type	Stepping	Revision ID	S-Spec
82462GX (SDC)	B-1	03h	SL55G

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82462GX (SDC) component. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	B-1			
1	X	19	NoFix	Strobe pair restrictions for boundary scan testing
2	X	19	NoFix	PWRGD signal can disable boundary scan testing

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
			None for this revision of the specification update

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. Strobe pair restrictions for boundary scan testing

Problem: On the SDC component, there is a boundary scan 1149.1 specification violation on the system bus data strobe pairs (STBN[3:0]#, STBP[3:0]#), and the memory bus strobe pairs (MDSN#, MDSP#). The current implementation includes a boundary scan cell for each strobe in a differential pair. Because of this, a “01” or “10” pattern is the only valid pattern to load into the strobe boundary scan cells. If a “00” or a “11” pattern were scanned into the strobe pair boundary scan cells, the differential amplifier on the receiver could not deterministically resolve the signals to a known value.

Implication: For the system bus data strobe pairs (STBN[3:0]#, STBP[3:0]#), and the memory bus strobe pairs (MDSN#, MDSP#), only “01” or “10” may be scanned into the boundary scan cells.

Workaround: Automatic Test Pattern Generator software can be programmed to only create the “01” or “10” for each of the pairs. This could be done by defining the pair as a differential pair in the software.

Status: For the steppings affected, see the Summary Table of Changes.

2. PWRGD signal can disable boundary scan testing

Problem: If the PWRGD signal is driven to zero, all outputs are tristated, thus overriding the boundary scan chain logic.

Implication: If the PWRGD signal is not asserted, boundary scan testing cannot take place. This issue also prevents testing of the PWRGD connection on the board via boundary scan.

Workaround: The PWRGD signal must be kept asserted during boundary scan testing.

Status: For the steppings affected, see the Summary Table of Changes.

Part 3: Specification Update for the 82463GX (MAC)

Identification Information

Type	Stepping	Revision ID	S-Spec
82463GX (MAC)	B-1	03h	SL4DH

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82463GX (MAC) component. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	B-1			
1	X	25	NoFix	PWRGD signal can disable boundary scan testing
2	X	25	NoFix	SDRAM controller queue overflow during initialization
3	X	25	NoFix	General calls during chipset enumeration on the I2C bus are improperly handled

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
1	26	Doc	Memory bandwidth

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. PWRGD signal can disable boundary scan testing

Problem: If the PWRGD signal is driven to zero, all outputs are tristated, over-riding the boundary scan chain logic.

Implication: If the PWRGD signal is not asserted, boundary scan testing cannot take place. This issue also prevents testing of the PWRGD connection on the board via boundary scan.

Workaround: The PWRGD signal must be kept asserted during boundary scan testing.

Status: For the steppings affected, see the Summary Table of Changes.

2. SDRAM controller queue overflow during initialization

Problem: The MAC should be able to initialize all valid memory configurations. Due to this erratum, for systems populated with only one row of double-sided DIMM, the SDRAM controller is too quick and interferes with the memory refresh cycles causing the queue to overflow.

Implication: Due to the SDRAM controller queue overflow, system initialization does not complete and may cause the system to hang.

Workaround: Firmware may contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

3. General calls during chipset enumeration on the I2C bus are improperly handled

Problem: When a general call is issued by the SAC during chipset enumeration on the I2C bus, the MAC should return proper values from all valid locations and continue to function properly. This erratum will cause the first configuration read which targets the MAC after the general call to return invalid data. The general call is issued by default when function 2 or 3 of either device 5 or device 6 is accessed.

Implication: Invalid values from a valid location may result in unpredictable behavior.

Workaround: Firmware may contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

Specification Clarifications

1. Memory bandwidth

The memory bandwidth section in Section 5.3 of the *Intel® 460GX System Software Developer's Manual* will be clarified to say the following:

- Sustained bandwidth is a function of traffic patterns as well as the system design and configuration. Each memory port can transfer 16 bytes per clock. This is a peak of 2.13 GB/s per port.
- For maximum bandwidth, both stacks on each of the two memory cards should be evenly populated.
- For non-uniform memory configurations, as explained in Section 5.2.2, if one row of memory is populated on three stacks and two rows are populated on the fourth stack, accesses to the second row on the fourth stack will be slower since the second row will not be fully interleaved.

Part 4: Specification Update for the 82464GX (MDC)

Identification Information

Type	Stepping	Revision ID	S-Spec
82464GX (MDC)	B-2	04h	SL5L6

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82464GX (MDC) component. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	B-2			
1	X	31	NoFix	Strobe pair restrictions for boundary scan testing
2	X	31	NoFix	PWRGD signal can disable boundary scan testing
3	X	31	NoFix	General calls during chipset enumeration on the I2C bus are improperly handled

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
			None for this revision of the specification update

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. Strobe pair restrictions for boundary scan testing

Problem: On the MDC component, there is a boundary scan 1149.1 specification violation on the memory bus strobe pairs (MDSN#, MDSP#). The current implementation includes a boundary scan cell for each strobe in a differential pair. Because of this, a “01” or “10” pattern is the only valid pattern to load into the strobe boundary scan cells. If a “00” or a “11” pattern were scanned into the strobe pair boundary scan cells, the differential amplifier on the receiver could not deterministically resolve the signals to a known value.

Implication: For the memory bus strobe pairs (MDSN#, MDSP#), only “01” or “10” may be scanned into the boundary scan cells.

Workaround: Automatic Test Pattern Generator software can be programmed to only create the “01” or “10” for each of the pairs. This could be done by defining the pair as a differential pair in the software.

Status: For the steppings affected, see the Summary Table of Changes.

2. PWRGD signal can disable boundary scan testing

Problem: If the PWRGD signal is driven to zero, all outputs are tristated, over-riding the boundary scan chain logic.

Implication: If the PWRGD signal is not asserted, boundary scan testing cannot take place. This issue also prevents testing of the PWRGD connection on the board via boundary scan.

Workaround: The PWRGD signal must be kept asserted during boundary scan testing.

Status: For the steppings affected, see the Summary Table of Changes.

3. General calls during chipset enumeration on the I2C bus are improperly handled

Problem: When a general call is issued by the SAC during chipset enumeration on the I2C bus, the MDC should return proper values from all valid locations and continue to function properly. This erratum will cause the first configuration read which targets the MDC after the general call to return invalid data. The general call is issued by default when function 2 or 3 of either device 5 or device 6 is accessed.

Implication: Invalid values from a valid location may result in unpredictable behavior.

Workaround: Firmware may contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

Part 5: Specification Update for the 82465GX (GXB)

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82465GX (GXB) product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	B-0			
1	X	36	NoFix	Strobe pair restrictions for boundary scan testing
2	X	36	NoFix	GXB fails to ignore upper address bits with 4G enable cleared
3	X	37	NoFix	GXB component will not pass a Delayed Read Request or Memory Writes over a stalled I/O Write or Configuration Write
4	X	37	NoFix	GXB does not wait for FRAME# to go inactive for master abort

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
			None for this revision of the specification update

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. Strobe pair restrictions for boundary scan testing

Problem: On the GXB component, there is a boundary scan 1149.1 specification violation on the Expander bus interface strobe pairs (XSTBN#, XSTBP#). The current implementation includes a boundary scan cell for each strobe in a differential pair. Because of this, a “01” or “10” pattern is the only valid pattern to load into the strobe boundary scan cells. If a “00” or a “11” pattern were scanned into the strobe pair boundary scan cells, the differential amplifier on the receiver could not deterministically resolve the signals to a known value.

Implication: For the Expander bus interface strobe pairs (XSTBN#, XSTBP#), only “01” or “10” may be scanned into the boundary scan cells.

Workaround: Automatic Test Pattern Generator software can be programmed to only create the “01” or “10” for each of the pairs. This could be done by defining the pair as a differential pair in the software.

Status: For the steppings affected, see the Summary Table of Changes.

2. GXB fails to ignore upper address bits with 4G enable cleared

Problem: The 4G bit of the AGP Command Register, if set, allows the GXB to receive addresses of greater than 4 GB. When cleared, addressing above 4G is disabled; the GXB must ignore the upper address bits AD[63:32] from a dual address cycle in sideband mode, AD[47:36] from a Type 4 SBA access, and AD[35:32] from a Type 3 access. Due to this erratum, even when the 4G bit is cleared, the GXB fails to ignore the upper address bits.

Implication: Section 6.1.10 of the *Accelerated Graphics Port Interface Specification*, Rev 2.0, states that when the 4G bit is cleared, “the master is only allowed to access addresses in the low 4 GB of the address space.” However, when the 4G bit is cleared, if the AGP master illegally issues transactions directed above 4 GB, the GXB component will incorrectly accept those transactions and pass them along to memory. For sideband commands, the upper address bits are sticky. If the AGP master illegally accesses the higher address bits, the bits will be latched for Type 3 and Type 4 commands. That address will be used for all subsequent access until a similar type command is received. If the system has greater than 4 GB of memory, illegal transactions may corrupt data in memory.

If the AGP master correctly drives the upper address bits to zero when the 4G bit is cleared, this erratum will have no impact.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes.

3. GXB component will not pass a Delayed Read Request or Memory Writes over a stalled I/O Write or Configuration Write

Problem: Section E.4 of the *PCI Local Bus Specification*, Rev 2.2, defines the ordering of delayed transactions for PCI to PCI bridges. Row 1, Column 4 and Row 4, Column 4 of Table E-1 (Ordering rules for a Bridge) specify that Posted Memory Writes and Delayed Read Completions must be allowed to pass Delayed Write Requests. Due to this erratum, the GXB component will not pass a Posted Memory Write or Delayed Read Completion over a stalled Delayed Write Request (Configuration Write).

Implication: The following situation may result in a deadlock: the GXB retries an inbound Memory Read request from an AGP card or PCI-to-PCI bridge acting as an AGP master. The inbound Memory Read request is accepted by the GXB as a Delayed Read. Subsequently, GXB issues an outbound Configuration write which the AGP device acting as a target retries. The GXB receives the Delayed Read Completion (DRC) for the read request from the system bus and queues the DRC behind the Configuration Write. If the AGP device waits to receive the DRC for the read request before completing the Configuration Write, the system will deadlock.

The situation is the same if GXB has two out bound transactions: an Configuration Write followed by Memory Write. If the AGP device retries the Configuration Write indefinitely, the system will deadlock as GXB will not pass Memory Writes ahead of the stalled Configuration Write.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes.

4. GXB does not wait for FRAME# to go inactive for master abort

Problem: During inbound traffic from a PCI agent, if none of the targets (including GXB) decode the address to be in their address space (i.e. none of the targets assert DEVSEL# on the bus), the master will master abort and in response should transition to IDLE state. Due to this erratum, the GXB does not wait for the FRAME# from master to go inactive for a Master Abort cycle. Instead it assumes the master will remove FRAME# in the subtractive decoding phase.

Implication: If the master does not deassert FRAME# in the Subtractive Decode clock phase when it samples DEVSEL# inactive, the GXB may lock up.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes.

Part 6: Specification Update for the 82466GX (WXB)

Identification Information

Type	Stepping	Revision ID	S-Spec
82466GX (WXB)	B-2	07h	SL5HP

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82466GX (WXB) component. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	B-2			
1	X	43	NoFix	WXB minimum slew rate

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
1	44	Doc	Slot Enable, LED Control, and Slot Power Control read only if less than six hot-plug slots on a PCI bus

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
1	45	Doc	IHPC indicates SERR flag even when SERR output is disabled and SERR occurs
2	45	Doc	WXB PCI feedback clock
3	45	Doc	WXB does not set Received Master Abort (RMA) bit during configuration cycles

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. WXB minimum slew rate

Problem: The minimum slew rate of the WXB component's outgoing PCI clock (P(A,B)CLK[2:0]) may be as low as 1 V/ns which translates to an additional 220 ps of clock uncertainty for 66 MHz operation.

Implication: The WXB component does not meet the minimum clock slew rate for 66 MHz operation as specified in the *PCI Local Bus Specification*, Rev 2.2. In systems that are not able to tolerate an additional 220 ps of clock uncertainty, it is possible that parity, or protocol errors may occur resulting in a master abort.

Workaround: For 66 MHz operation, total system timing margins need to account for an additional 220 ps of clock uncertainty.

Status: For the steppings affected, see the Summary Table of Changes.

Specification Changes

1. Slot Enable, LED Control, and Slot Power Control read only if less than six hot-plug slots on a PCI bus

In Sections 7.5.2, 7.5.4, and 7.5.12 of the *Intel® 460GX Chipset System Software Developer's Manual*, if there are less than six hot-plug slots on a PCI bus, then the unused bits in Slot Enable, LED Control, and Slot Power Control will be read-only with a value of '0'.

Specification Clarifications

1. IHPC indicates SERR flag even when SERR output is disabled and SERR occurs

As described in Section 7.4.4 of the *Intel® 460GX Chipset System Software Developer's Manual*, the IHPC SERR enable bit in the PCICMD register must be programmed consistently with the WXB SERR enable bit. Software must ensure that the bits are both enabled or both disabled.

Additionally, the WXB may have all of its SERR sources suppressed by existing masks while leaving SERR enable asserted for the benefit of IHPC SERR reporting.

2. WXB PCI feedback clock

In Section 7.4 of the *Intel® 460GX Chipset Datasheet* the original text states:

- A series termination resistor near each PCI clock driver is also required. System measurements should be performed to determine the precise value in a particular system. Timing studies should be done on the feedback network to satisfy Table 7-9.

The following note will be added to the above paragraph:

- Note: The CLKFB signal in Figure 7-3 may be subject to noise and temperature and power supply variations, causing excessive clock jitter and PCI parity errors. The resistor and capacitor network values for a particular system should be optimized and verified experimentally.

3. WXB does not set Received Master Abort (RMA) bit during configuration cycles

When a master device terminates a transaction with a master abort, except during a special cycle, the *PCI Local Bus Specification*, Rev. 2.2, requires the device to set the Received Master Abort (RMA) bit in its PCI status register. Furthermore, so that firmware does not need to clear the RMA bit after Master Aborts that occur while searching configuration space for devices, the WXB will not set the RMA bit in its PCI status register during configuration cycle transactions. For all other transactions receiving a Master Abort, the RMA bit will be set.

Part 7: Specification Update for the 82467GX (PXB)

Identification Information

Type	Stepping	Revision ID	S-Spec
82467GX (PXB)	C-1	05h	SL482

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82467GX (PXB) component. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	C-1			
1	X	51	NoFix	PXB does not assert target abort; request submitted continuously
2	X	51	NoFix	Strobe pair restrictions for boundary scan testing
3	X	51	NoFix	XXSTBP# pin cannot be tri-stated

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
			None for this revision of the specification update

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. PXB does not assert target abort; request submitted continuously

Problem: The case arises when a device on one PCI bus generates an inbound read request targeting a PCI agent on another PCI bus and the targeted device responds with a target abort. In this case, it is possible that the target abort which is returned to the initiating PXB will hit a timing window such that the PXB treats the target abort as a retry. The PXB will retry the initiating PCI card instead of doing a target abort. The PCI card will re-issue this transaction later, the PXB will attempt the peer read and the targeted PXB may receive another target abort. It is possible that this cycle could continue indefinitely and is potentially a livelock.

Implication: The PXB may encounter a livelock in the situation described above, resulting in a PCI bus hang.

Workaround: None identified at this time. This erratum requires that the targeted agent do a target abort to each read. It also requires that there is no random traffic in the system to perturb the traffic patterns so that the one clock window which causes the problem is always hit.

Status: For the steppings affected, see the Summary Table of Changes.

2. Strobe pair restrictions for boundary scan testing

Problem: On the PXB component, there is a boundary scan 1149.1 specification violation on the Expander bus interface strobe pairs (XSTBN#, XSTBP#). The current implementation includes a boundary scan cell for each strobe in a differential pair. Because of this, a “01” or “10” pattern is the only valid pattern to load into the strobe boundary scan cells. If a “00” or a “11” pattern were scanned into the strobe pair boundary scan cells, the differential amplifier on the receiver could not deterministically resolve the signals to a known value.

Implication: For the Expander bus interface strobe pairs (XSTBN#, XSTBP#), only “01” or “10” may be scanned into the boundary scan cells.

Workaround: Automatic Test Pattern Generator software can be programmed to only create the “01” or “10” for each of the pairs. This could be done by defining the pair as a differential pair in the software.

Status: For the steppings affected, see the Summary Table of Changes.

3. XXSTBP# pin cannot be tri-stated

Problem: The XXSTBp# pin cannot be tri-stated on the PXB.

Implication: Since the XXSTBP# pin cannot be tri-stated, applying a voltage to this pin (for example, during JTAG Hi-Z testing) will cause a short between power and ground.

Workaround: None identified at this time.

Status: For the steppings affected see the Summary Table of Changes.

Part 8: Specification Update for the 82468FB (IFB)

Identification Information

Type	Stepping	Revision ID	S-Spec
FW82468GX (IFB)	A-0	01h	SL4GJ

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the FW82372FB (IFB) and FW82468GX (IFB) components. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	A-0			
1	X	57	NoFix	Daylight savings time errata
2	X	57	NoFix	USB dribble errata
3	X	57	NoFix	USB handshake

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
			None for this revision of the specification update

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. Daylight savings time errata

Problem: If the last Sunday in October is the 30th or 31st, and the daylight savings enable bit in the IFB is set, the IFB will not correctly adjust the time back one hour from 1:59:59 to 1:00:00am.

Implication: The system time may not be correct after the daylight savings time change. The first manifestation of this will be on October 31st 1999.

Workaround: The operating system or the system firmware can correctly detect the time change and correct the IFB's CMOS time settings.

Status: For the steppings affected, see the Summary Table of Changes.

2. USB dribble errata

Problem: The USB host controller may incorrectly interpret a USB receive packet and record an error. This situation occurs when a bitstuff follows the transmission of a cyclic redundancy check (CRC), coupled with a dribble bit. The dribble bit is due to prop delays through cables and HUBs.

Implication: The host controller response to this is a non-acknowledge with a CRC/Timeout status communicated to the software. If this condition persists the error count associated with this packet will be exceeded and an interrupt can be generated to software. This will stall the USB device. Current software reports a device error to the user via a pop-up window. Another implication is that the installed base may have limited USB expandability via HUBs.

Workaround: There are two possible workarounds:

1. Hardware: Try plugging the USB device into a USB port closer to the root hub.
2. Software: Detect the CRC/Timeout error and count exceeded and attempt to requeue the packets while changing the length of the packets. Changing the length of the packets will change the CRC and may remove the combination of the two events causing the failure.

Status: For the steppings affected, see the Summary Table of Changes.

3. USB handshake

Problem: The IFB UHCI will fail to provide a handshake if it receives an incoming data packet where CRC has five consecutive 1's in the least significant bit of CRC and is immediately followed by an EOP for Bulk, Interrupt, and Isoc transfers ONLY IF a K-state is being signalled on the other port at the time of this EOP. This behavior, to date, has only been observed during artificial testing procedures.

Implication: USB devices may stall. The OS will attempt to recover, but if it fails to do, an error message will be displayed. The user may have to unplug then re-install the USB device that has stalled.

Workaround: There are two possible workarounds to choose from:

1. Do not use the specific selective suspend feature of the IFB when there can be activity on the other bus. Global Suspend must be employed.
2. Do not allow USB peripherals to use remote wake feature (from selective suspend).

Status: For the steppings affected, see the Summary Table of Changes.

Part 9: Specification Update for the 82094AA (PID)

Identification Information

Type	Stepping	Revision ID	S-Spec
82094AA (PID)	A-0	01h	Q768

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 82094AA (PID) component. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated on page 7.

Errata

No.	Steppings	Page	Status	ERRATA
	A-0			
1	X	63	NoFix	PID stops responding under certain conditions when PCI bus is parked on it

Specification Changes

No.	Page	Status	SPECIFICATION CHANGES
			None for this revision of the specification update

Specification Clarifications

No.	Page	Status	SPECIFICATION CLARIFICATIONS
			None for this revision of the specification update

Documentation Changes

No.	Page	Status	DOCUMENTATION CHANGES
			None for this revision of the specification update

Errata

1. PID stops responding under certain conditions when PCI bus is parked on it

Problem: It is possible for the PID to stop responding when the following conditions are met:

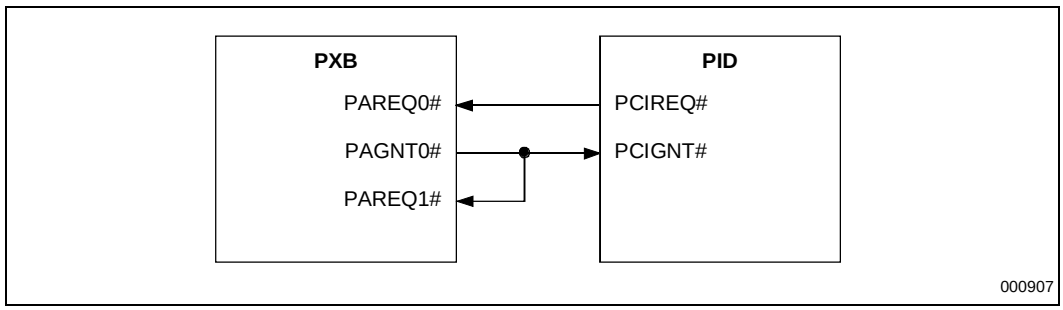
- The PCI bus is parked on the PID, and thus it's GNT# signal is asserted.
- The PID has an inbound SAPIC message it is about to send.
- The PID's GNT# signal is deasserted.

In this case it is possible that upon the assertion of the PID's GNT# signal, the PID will stop responding to any interrupt requests or PCI bus transactions targeting it.

Implication: If the PID stops responding, any interrupt requests routed to this PID will no longer be serviced and the system may hang.

Workaround: The workaround is to prevent the PCI bus from getting parked on the PID. With the PXB, it is accomplished by connecting the PID's PCI GNT# pin to an unused PCI REQ# input on the PXB that has the PID attached to it. See Figure 1.

Figure 1. Recommended Workaround for Erratum 1



If no unused REQ# input is available on the PXB, the PID's PCI GNT# signal can be ANDed with another REQ# input.

This workaround results in the PXB always seeing a REQ# being asserted when the PID has been granted the bus, thus keeping the PCI bus from being parked on the PID. When the PID's GNT# signal is deasserted by the PXB, the REQ# line tied to it is also deasserted. If there are not any other outstanding requests for the PCI bus, the bus will be parked on the PXB since the REQ# signal and PID's GNT# signal get deasserted in the same clock.

For systems which use the PID, but not a PXB, a similar workaround will have to be implemented using the REQ# and GNT# pins to again ensure that the PCI arbiter does not allow the PCI bus to be parked on the PID.

Status: For the steppings affected, see the Summary Table of Changes.