21153 PCI-to-PCI Bridge

Specification Update

August 1999

Notice: The 21153 may contain design defects or errors known as errata. Characterized errata that may cause the 21153's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278301-001

Contents

Revision History

Date	Version	Description
8/25/99	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
21153 PCI-to-PCI Bridge	278220-001

Nomenclature

Errata are design defects or errors. These may cause the 21153-AC's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 21153-AC product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	E	#	#			
1	X			10	Eval	Hold timing issues for all PCI signals (both bused and control) on the 21153-AC.

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	#	#			
					None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

Identification Information

Markings

21153

- This document contains errata for the 21153 PCI-to-PCI Bridge. The 21153 device revision affected by this erratum can be identified by marketing part number 21153AC (marked on the package as DC1041E). This device can be electrically identified in a PCI system by reading the REV_ID register (offset of 08h in PCI configuration space), which is a value of -04.
- While Intel believes the information included in this publication to be correct as of the date of publication, it is subject to change without notice.

Errata

1. Hold Time Issues for all PCI Signals (Both Bused and Control) on the 21153-AC

Problem: This problem exists for parts with REV_ID 4.

The *PCI Local Bus Specification, Revision 2.2*, specifies a Hold time of **0 ns** in Section 4.2.3.2. The 21153-AC requires a minimum hold time of **1.0 ns**.

Implication: Most PCI devices will function properly with this miss to the Hold time specification.

Workaround: There are no workarounds for this erratum.

Status: Eval.

Specification Changes

None for this revision of this specification update.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

None for this revision of this specification update.