AP-585

APPLICATION NOTE

Pentium® II Processor GTL+ Guidelines

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CONTENTS

1.0. INTRODUCTION

The Pentium® II processor is the next processor in the family of Intel Architecture microprocessors. The Pentium II processor extends the power of the Pentium Pro processor and adds the capability of MMX™ media enhancement technology. The Pentium II processor maintains binary compatibility with the 8086/88, 80286, Intel386™, Intel486™, Pentium and Pentium Pro processors. The design of the Pentium II processor system bus enables the Pentium II processor to be "multiprocessor ready." The Pentium II processor implements a synchronous, latched bus protocol that allows a full clock cycle for signal transmission and a full clock cycle for signal interpretation and generation. The Pentium II processor bus uses low-voltage-swing GTL+ I/O buffers, making high frequency signal communication between many loads easier.

The goal of this layout guideline is to provide a system designer with the information needed for the Pentium II processor and Intel 440 PCIset bus portion of the printed circuit board (PCB) layout. These guidelines are valid for the 440FX and future Intel Pentium II processor PCIsets. Other chassis requirements including cooling, mechanical stability, memory location, etc. may constrain the system topology and component placement location, therefore constraining the board routing. These issues are not directly addressed in this document. This document provides guidelines and methdologies that are to be used with good engineering practices. It does not provide hard and fast rules.

See the Pentium II processor datasheet and the applicable chipset specification for component specific electrical details. Intel strongly recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design.

2.0. ABOUT THIS DOCUMENT

The following sections describe the layout and usage of these guidelines as well as define many of the terms used throughout this document.

2.1. Document Organization

This section defines terms used in the document. Section 3 discusses specific system guidelines. This is a step-by-step methodology that Intel has successfully used to design Pentium II processor systems using the 440 PCIset components for validation and feasibility. Section 4 introduces the theories that are applicable to this Layout Guideline. Section 5 contains more details and insights. The items in Section 5 expand on some of the rationale for the recommendations in the step-by-step methodology. This section also includes equations that may be used for reference.

The actual guidelines start at Section 3 – *A Recommended GTL+ Design Guideline.*

2.2. Definition of Terms

Aggressor – a network that transmits a coupled signal to another network is called the aggressor network.

Bus Agent – a component or group of components that, when combined, represent a single load on the GTL+ bus.

Clock Adjustment Factor – an adjustment factor included in timing analysis calculations to account for effects of host clock trace routing from the processor edge fingers, through the substrate, to the processor core.

Corner – describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. The results in performance of an electronic component that may change as a result of this include, but are not limited to: clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the "slow" corner would mean having a component operating at it's slowest, weakest performance. Similar discussion of "fast" corner would mean having a component operating at its fastest, strongest performance. Operation or simulation of a component at it's slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance. The component packages, printed circuit boards and electrical connectors have corner characteristics that effect Pentium II processor based system designs.

Crosstalk – the reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.

- **Backward Crosstalk** – coupling which creates a signal in a victim network that travels in the opposite direction as the aggressor's signal.

- **Even Mode Crosstalk** – coupling from one or more aggressors when all the aggressors switch in the same direction that the victim is switching.

- **Forward Crosstalk** – coupling which creates a signal in a victim network that travels in the same direction as the aggressor's signal.

- **Odd Mode Crosstalk** – coupling from one or more aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Daisy Chain – a routing topology in which a network connects component to component without any intersections, or only short stubs.

Flight Time – the additional delay between the driver and receiver introduced by the printed circuit board interconnects and the component loading effects as compared to the data sheet specification load. Although the name implies that this is the time required for a signal to travel from one end of the interconnect to the other, a better definition of this term is simply that it is the total delay the layout (interconnects plus loads) adds to the component timings. (This is similar to the usage of the term "derating", but that term fails to acknowledge that transmission line effects are being included in the analysis.)

Flight time is therefore defined as the difference between when a signal at the input pin of a receiving agent crosses V_{REF} and the time that the output pin of the driving agent crosses the V_{REF} were it driving the test load used to specify that driver's AC timings. V_{REF} for the Pentium II processor is 1.0 V.

T_{REF} for the Pentium II processor driver is measured into an idealized 50Ω resistor pulled up to 1.5V. T_{REF} for the 440 PCIset component test load is measured into an idealized 25Ω resistor pulled up to 1.5 V. The difference between the T_{REF} test loads for the processor and PCIset is attributed to the GTL+ termination resistors included within the Pentium II processor. Component delays are measured to the V_{REF} value of 1.0 V for both the processor and the PCIset.

Flight time is defined as:

$$T_{FLIGHT} = T_{RECEIVER} - T_{REF}$$

Where:

T_{REF} = the reference delay discussed above, and $T_{RECEIVER}$ is the time at which the waveform has a valid V_{REF} crossing (as described in the *Pentium® II Processor Developer's Manual*).

Figure 1 shows the definition of flight time. Notice that determining flight time requires a minimum of two simulations, one in which the driver is driving the test load, and one in which it is driving the actual system load.

- **Maximum and Minimum Flight Time** – Flight time variations can be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of multiple signals switching and additional packaging affects.

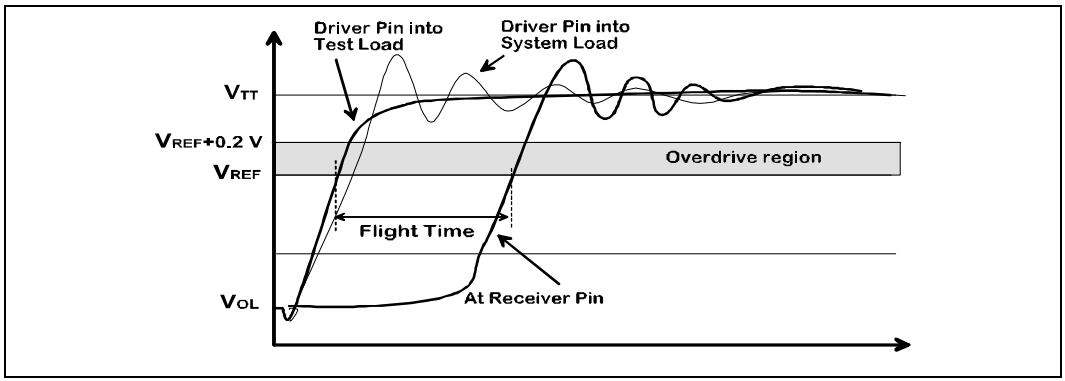

Figure 1. Definition of the Flight Time Criteria

- **Maximum Flight Time** – the largest flight time a network will experience under all variations of conditions.
- **Minimum Flight Time** – the smallest flight time a network will experience under all variations of conditions.

GTL+ – the bus technology used by the Pentium II processor. This is an incident wave switching, open drain bus with external pull-up resistors that provide both the high logic level and termination at each end of the bus. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See the Pentium II processor specification for more details of GTL+.

Network – the trace of a PCB that completes an electrical connection between two or more components.

Network Length – the distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors.

Overdrive Region – the voltage range, at a receiver, from V_{REF} +200 mV for a low to high going signal and V_{REF} –200 mV for a high to low going signal.

Overshoot – a voltage amplitude that exceeds the maximum voltage, V_{IH}, level as specified in the component specification.

Ringback – the re-crossing of a high or low input logic threshold after it has initially crossed that logic threshold.

Settling Limit – the maximum allowed peak to peak oscillation after a signal has transitioned to the correct logic level as specified in the component specification.

Setup Window – the time between the beginning of Setup to Clock (T_{SU_MIN}) and the clock input. This window may be different for each type of bus agent in the system.

Stub – the branch from the trunk terminating at the pad of an agent. All stubs should be short.

Trunk – the main connection, excluding interconnect branches, ending at the active agent pins. The trunk should be routed in a daisy chain fashion.

Undershoot – a voltage amplitude that negatively exceeds the minimum low voltage, V_{IL} level as specified in the component specification.

Victim – a network that receives a coupled crosstalk signal from another network is called the victim network.

3.0. A RECOMMENDED GTL+ DESIGN GUIDELINE

The following step-by-step guideline was developed for systems based on one or two Pentium II processors and one 440 PCIset load.

The methodology recommended in this section is based on experience developed at Intel while developing many different Pentium II processor-based systems for validation and feasibility studies. This methodology relies on spreadsheet type calculations for initial timing analysis and performing signal integrity/noise analysis. The analog simulations should be validated after actual systems become available. The validation portion of this section describes a method for determining the flight time in an actual system.

3.1. Determine Components

Determine which components will be used. Determine the number of Pentium II processors, which 440 PCIset components, and other GTL+ components to be used.

3.2. Initial Timing Analysis

An initial timing analysis of the system is required. To complete the timing analysis, values for the clock skew and clock jitter are needed, along with the component specifications. These values should be sufficient for determining the bounds for system flight times. Equation 1 and Equation 2 are the basis for the timing analysis.

Equation 1. Maximum Frequency

$$\text{Clock Period} \geq T_{FLIGHT\_MAX} + T_{CO\_MAX} + T_{SU\_MIN} + CLK_{SKEW} + CLK_{JITTER} + CLK_{ADJ} + T_{ADJ}$$

Equation 2. Hold Time

$$T_{CO\_MIN} + T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} + CLK_{ADJ}$$

Where (for Equation 1 and Equation 2):

T_{CO_MAX} = The maximum clock to output specification. (1)

T_{CO_MIN} = The minimum clock to output specification. (1)

T_{SU_MIN} = The minimum required time specified to setup before the clock. (1)

T_{HOLD} = The minimum specified input hold time.

T_{ADJ} = An empirical timing adjustment factor that accounts for timing "pushout" seen when multiple bits change state at the same time. The factors that contribute to the adjustment factor include crosstalk on the PCB, substrate, and packages, simultaneous switching noise, and edge rate degradation caused by inductance in the ground return path. (2)

CLK_{JITTER} = The maximum clock edge to edge variation.

CLK_{SKEW} = The maximum variation between components receiving the same clock edge.

CLK_{ADJ} = The host clock adjustment factor. (3)

T_{FLT_MAX} = The maximum flight time as defined in Section 2.2.

T_{FLT_MIN} = The minimum flight time as defined in Section 2.2.

Notes for Equation 1 and Equation 2:

1. The Clock to Output (T_{CO}) and Setup to Clock (T_{SU}) timings are both measured from the signals last crossing of V_{REF}, with the requirement that the signal does not violate the ringback or edge rate limits. See the *Pentium® II Processor Developer's* Manual for more details.
2. TADJ should be calculated for each individual system. A value of 0.7 ns is used throughout this document and may be used as a generic TADJ value during flight time calculations if an actual crosstalk flight time delay can not be calculated.
3. The CLKADJ clock adjustment factor is included in the timing calculations to adjust for BCLK skew differences between the Pentium II processor edge fingers and other component pins on the GTL+ network. The adjustment accounts for the effects of host clock trace routing from the processor edge fingers, through the substrate, to the processor core. Adding an adjustment constant to timing calculations between the processor and the PCIset guarantees host clock synchronization between the PCIset component and the processor core. See Table 2 for CLK_{ADJ} values and the Pentium II processor and 440 PCIset datasheets for details on host clock timing and signal quality requirements.

Solving these equations for flight time results in the following equations:

Equation 3. Maximum Flight Time

$$T_{FLIGHT\_MAX} = \text{Clock Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - CLK_{ADJ} - T_{ADJ}$$

Equation 4. Minimum Flight Time

$$T_{FLIGHT\_MIN} = T_{HOLD} + CLK_{SKEW} + CLK_{ADJ} - T_{CO\_MIN}$$

There are multiple cases to consider. Note that while the same trace connects two components, say A and B, the minimum and maximum flight time requirements for A driving B as well as B driving A must be met. The cases discussed in this document are:

- Pentium II processor driving a Pentium II processor
- Pentium II processor driving a PCIset component
- PCIset component driving a Pentium II processor

Designs using components other than those listed above require calculations for additional combinations of driver and receiver.

Table 1. Pentium® II Processor and Intel 440FX PCIset GTL+ Parameters (1)

IC Parameters	Pentium® II Processor (2)	Intel 440 PCIset
Clock to Output maximum (T_{CO_MAX}) ns	6.37	7.25
Clock to Output minimum (T_{CO_MIN}) ns	1.07	1.00
Setup time (T_{SU_MIN}) ns	2.53	5.00
Hold time (T_{HOLD}) ns	1.53	0.00

NOTES:

1. Timing analysis done using timing parameters for the Pentium® II processor and the 440FX PCIset. These timing parameters are subject to change. Please check the appropriate component datasheets for valid timing parameter values for the specific components used in the system design.
2. Pentium II processor timings are specified at the processor edge fingers.

Table 2. T_{FLT_MAX} Calculations (1, 2)

Driver	Receiver	CLK Period	T_{CO_MAX}	T_{SU_MIN}	CLK_{SKEW}	CLK_{JITTER}	CLK_{ADJ}	T_{ADJ}	T_{FLT_MAX}
Processor	Processor	15.00	6.37	2.53	0.40	0.25	0.00	0.70	4.75
Processor	440 PCIset	15.00	6.37	5.00	0.40	0.25	0.78	0.70	3.06
440 PCIset	Processor	15.00	7.25	2.53	0.40	0.25	0.78	0.70	3.09

Table 3. T_{FLT_MIN} Calculations (1, 2)

Driver	Receiver	T_{HOLD}	CLK_{SKEW}	CLK_{ADJ}	T_{CO_MIN}	T_{FLT_MIN}
Processor	Processor	1.53	0.40	0.00	1.07	0.86
Processor	440 PCIset	0.00	0.40	0.78	1.07	0.11
440 PCIset	Processor	1.53	0.40	0.78	1.00	0.15

NOTES FOR Table 2 AND Table 3:

1. All times in nanoseconds.
2. Timing calculations are to the Pentium® II processor edge fingers. The Slot 1 connector maximum and minimum delays should be included in calculations to determine trace routing lengths.

GTL+ trace lengths required to meet these timings can be calculated using the maximum and minimum flight time calculations, the effective board propagation constant (S_{EFF}) and Slot 1 connector characteristics. S_{EFF} is a function of:

- Dielectric constant (ε_r) of the PCB material.
- The type of trace connecting the components (stripline or microstrip).
- The length of the trace and the load of the components on the trace. (Note that the board propagation constant multiplied by the trace length is a **component** of the flight time but **not necessarily equal** to the flight time.)

Simulation should be used to accurately determine and verify signal length and flight time, see Section 3.6. The standard “textbook” equations used to calculate the expected signal propagation rate of a board are included in Section 5.1.

The BCLK input at the Pentium II processor edge fingers has a different reference voltage and signal integrity requirements than at the PCIset BCLK input pins. This difference is attributed to routing through the Pentium II processor's substrate before termination near the Pentium II processor core. For the electrical requirements at the Slot 1 connector edge fingers, refer the *Pentium® II Processor Developer's Manual*.

This extra trace routing introduces a clock delay factor between the Pentium II processor edge fingers and the processor core. Calculating the minimum and maximum signal flight times at the processor edge fingers requires incorporation of this BCLK timing delay. For AC timing analysis, this offset/adjustment value is fixed and is defined as, CLK_{ADJ} = 0.78 ns. This means that BCLK is seen at the Pentium II processor edge fingers 0.78 ns prior to being seen at the 440 PCIset components and the Pentium II processor core.

In addition to a timing delay factor, several BCLK edge finger parameters have been defined/updated to account for the edge finger to core differences. These parameters allow analysis of the BCLK signal integrity at the edge finger contacts. These specifications include:

- BCLK edge finger reference voltage
- Minimum and maximum BCLK edge finger ledge voltage
- Rise and fall time
- Ringback tolerance
- Overshoot and undershoot
- Minimum high and low time

See the *Pentium® II Processor Developer's Manual* for specification details.

3.3. Determine General Layout, Routing, and Topology Desired

Once the processor bus components have been selected, and the timing budget calculated, then determine their approximate location on the printed circuit board. Estimate the printed circuit board parameters from the placement and other information including the general layout and routing recommendations given in this section.

General recommendations for GTL+ bus topology, layout, and routing are given in the following list. Many of these recommendations are outlined in Figure 2.

- Daisy chain all GTL+ signals, keeping stubs to the Intel 440 PCIset components under 1.5 inches.
- The Pentium II processors need to be located at the end of the bus to terminate the GTL+ signals.
- If implementing a single Pentium II processor design, GTL+ termination resistors will need to be placed at the other end of the bus. To match the GTL+ termination of the Pentium II processor, termination resistor values should be 56Ω ±5%. Routing techniques such as those shown in Figure 3 can be used to overcome placement and space constraints.

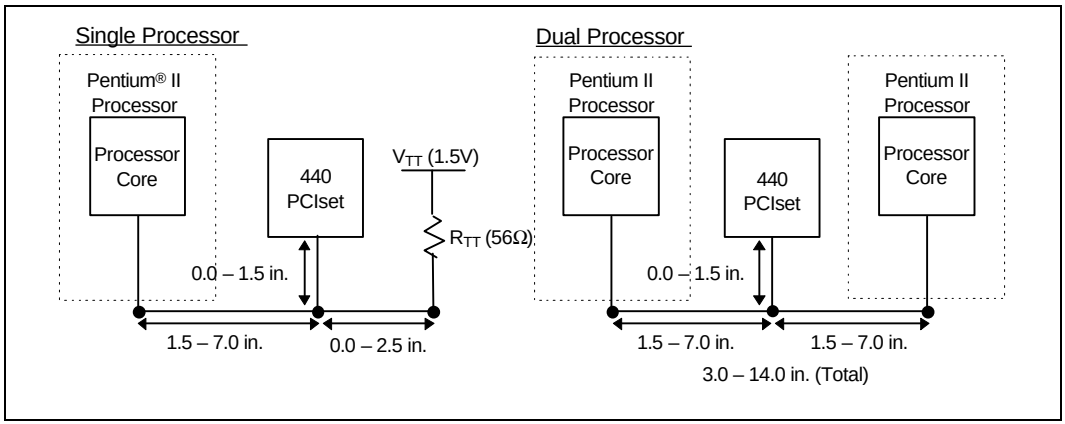

Figure 2. Pentium® II Processor General GTL+ Interconnect and Topology Guidelines

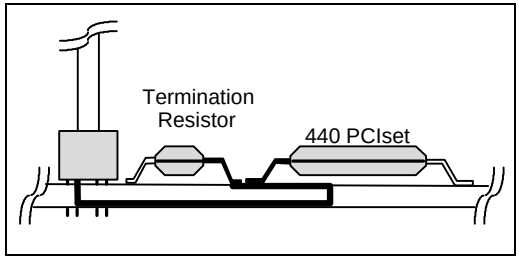

Figure 3. Single Processor Routing Example

- Locate the Pentium II processor(s) and 440 PCIset as required to meet timing. In dual Pentium II processor designs, the 440 PCIset should be placed electrically between the processors. Studies at Intel have shown that for most systems a trace routing length from 1.5 to 7.0 inches from Slot 1 connector to PCIset, and 3.0 to 14.0 inches from Slot 1 connector to Slot 1 connector prove to be valid routing solutions.
- Limit the trace routing length from the last agent on the GTL+ bus to the GTL+ termination to 2.5 inches in those systems requiring termination on the motherboard.
- Slot 1 connector characteristics must be included when determining trace routing lengths from flight times from the Pentium II processor edge fingers. Please check with your Slot 1 connector vendor for connector characteristics. For most Slot 1 connectors, Intel has found that slow corner values of 35Ω impedance and 150 ps delay, and fast corner values of 80Ω impedance and 110 ps delay appropriately model connector characteristics while connected to a 50Ω pull-up resistor test load to 1.5 V.
- Distribute V_{TT} with a wide trace. A 50 mil minimum width is recommended. Route the V_{TT} trace with the same topology as the GTL+ traces.
- Plan to place V_{REF} resistor divider pairs at the Intel 440 PCIset components. No V_{REF} divider is needed at the processors as V_{REF} is generated locally on the Pentium II processor from V_{TT}.
- Closely control the characteristic line impedance, Z_0 (50Ω to 80Ω).
- A PCB signal velocity of 1.6 to 2.2 ns/ft should be used.
- The total host clock skew should be designed to achieve an overall maximum value of 650 ps. This 650 ps includes 250 ps of host clock jitter, 250 ps of host clock driver pin-to-pin skew and 150 ps of host clock motherboard interconnect skew.
- Host clock trace lengths should be identical to all components on the GTL+ network (a tolerance of ±0.1 inch is allowed). The Pentium II processor I/O Buffer Models and Slot 1 connector specifications should be used to determine exact trace length adjustments required to account for host clock routing across the Slot 1 connector, through the processor substrate to the processor core. A generic adjustment factor of –4.0 inches may be used for most system designs of which 3.3 inches are host clock routing on the Pentium II processor substrate. The remaining 0.7 inches are attributed to the delay of a typical Slot 1 connector.
- Host clock traces should be routed before all other signals to guarantee length and skew requirements are met. Adding serpentines to clock traces to meet timing requirements is significantly easier before other signals have been routed.
- Plan to minimize crosstalk by:
  - Maximizing the line-to-line spacing (at least 10 mils between traces, except when routing between pins of components).
  - Minimizing the dielectric used in the system (4.2 to 4.8).
  - Minimize the cross sectional area of the traces, (5 mil lines with 1/2 ounce/ft^2 copper, but watch out for higher resistivity traces).
  - Eliminating parallel traces between layers not separated by a power or ground plane.
  - Isolate GTL+ signals from other signals (at least 25 mils from non GTL+ signals to GTL+ signals).
  - Route the same type of GTL+ I/O signals in isolated signal groups. That is route the data signals in one group, the address signals in another group. Keep at least 25 mils between each group of signals.

Using a custom ASIC or other component (with different timings than the Pentium II processor or 440 PCIset) on the Pentium II processor bus will require additional analog simulations to determine the optimum location of each agent along the bus.

Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.

3.4. Estimate Component to Component Spacing for GTL+ Signals

After determining the general layout do a more specific preliminary component placement. Estimate the number of layers that will be required. Then determine the expected interconnect distances between each of the components on the GTL+ bus. Be sure to consider the guidelines and recommendations discussed in Section 3.3. Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

Figure 4 shows one example of a single Pentium II processor based system component placement. With all single and dual Pentium II processor based systems, component placement and trace routing lengths should be designed to meet all system timing and signal quality requirements.

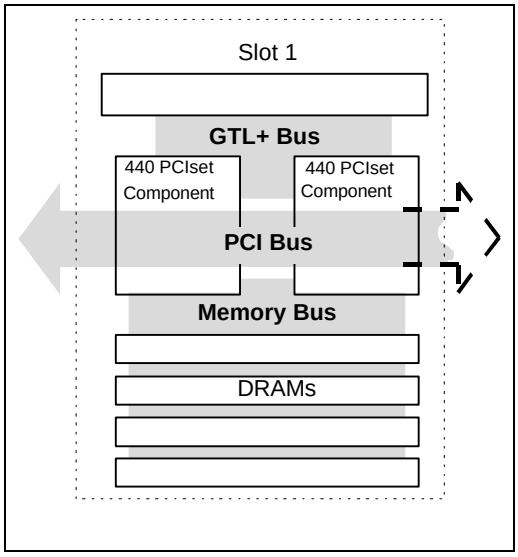

Figure 4. Single Pentium® II Processor Component Placement Example

The maximum network length between the bus agents is determined by the bus frequency and the maximum flight time propagation delay on the PCB. The minimum network length is independent of the required bus frequency. Table 2 and Table 3 assume values for CLK_{SKEW} and CLK_{JITTER} parameters that are controlled by the system designer. As noted in Section 4.2, these equations DO NOT allow for any change in the propagation of the signal due to ringback, crosstalk on the network/package or for any difference in buffer performance caused by driving actual loaded transmission lines instead of test loads that are used in the component specification. Intel suggests running analog simulations to ensure that each design has adequate noise and timing margin.

After the board layout is complete, extract real trace lengths and run analog simulations to verify the actual layout meets the timing and noise requirements.

Simulations and empirical testing done by Intel on systems following the guidelines and recommendations listed in Section 3.3 and the timing calculations and assumptions listed in Table 2 and Table 3 show that for most systems, 1.5 to 7.0 inches trace routing from processor to PCIset, and 3.0 to 14.0 inches trace routing from processor to processor are valid routing solutions (refer to Figure 2). As always, analog simulations are recommended for all system designs.

3.5. Route Board

Layout the board using the guidelines detailed in Section 3.3. Keep the estimated spacing and timing requirements in mind during the layout. If it becomes apparent that the placement and estimated spacing are not going to support the timing requirements, then revise the timing requirements estimates before the routing is complete.

After the GTL+ portion of the system is routed, extract the actual routed line lengths and verify that the actual routing provided acceptable timing.

3.6. Simulation

Intel strongly suggests running analog simulations for Pentium II processor designs. Intel provides the Pentium II processor I/O Buffer Models and the 440 PCIset I/O Buffer Models in IBIS 2.1 format. These models are available from your local Intel office.

Accurate simulations require that the actual range of parameters be used in the simulations. Intel has consistently measured the cross-sectional resistivity of the PCB copper to be in the order of 1 ohm * mil^2/inch, not the 0.662 ohm * mil^2/inch value for annealed copper as typically published in reference material.

Positioning drivers with faster edges closer to the middle of the network results in more noise than positioning them towards the ends. Intel has seen that the worst-case noise margin can be generated by drivers located in all positions (given appropriate variations in the other network parameters). Therefore, stimulating the networks from all driver locations, and analyzing each receiver for each possible driver is recommended.

Analysis has shown that increasing the value of R_{TT} results in decreased noise margin on the rising edge, and decreasing the value of R_{TT} results in decreased noise margin on the falling edge. Therefore it is not necessary to budget for R_{TT} variation if the selected value of R_{TT} +5% is used on the rising edge and R_{TT} –5% is used on the falling edge, since the simulation results will already include the extreme effects.

Faster edge rates cause increased ringback, which reduces the noise margin on the rising edge (Low to High); therefore only the fast corner (voltage, temperature, and process) I/O buffer model needs to be simulated for the Low to High transitions to evaluate signal quality.

Analysis has also shown that both fast and slow models must be run to verify signal quality on the falling edge (High to Low). The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum, causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. The slow corner I/O buffer model is used to check the maximum flight time.

Lengthening the stubs correlates to more (increased) ringback and a corresponding reduction in noise margin on the rising edge. Therefore it is acceptable to only simulate rising edges with all stubs at the maximum value on all bus agents.

Using maximum length package stubs can be pessimistic. Actual internal package stub lengths are provided with the I/O buffer models for the Pentium II processor or the Intel 440 PCIset devices. The internal package stub lengths may change slightly over time with new steppings of the components.

Intel has determined that, to properly model the effects of the "package stub" (connection between the die pad and the external pin), the package traces and pins should be represented using transmission line segments. The length, Z_0 and S_0 of each stub is given in IBIS compatible ".pkg" files. These files include the stub lengths, the package trace resistance, the substrate trace to the termination resistor and the substrate trace routing from the processor core pins to the Pentium II processor edge fingers. The packaging files are in an IBIS compatible format.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. This is generally done by editing your simulator's net description or topology file.

We have found wide variation in noise margins when we vary the stub impedance and the PCB's Z_0 and S_0. Our analysis has shown that extremes in impedance do **not** necessarily produce the extreme variations in noise margin. We therefore recommend that PCB parameters be controlled as tightly as possible, with a sampling of the allowable Z_0 and S_0 simulated. Intel recommends running uncoupled simulations using the Z_0 of the package stubs; and performing fully coupled simulations if increased accuracy is needed or desired.

There are six GTL+ signals that can be driven by more than one agent simultaneously. These signals may require more attention during the simulation, layout and validation portions of the design. When a signal is asserted (driven low) by two agents on the same clock edge, the two falling edge wave fronts will meet at some point on the bus and can sum to form a negative voltage. For most system designs, the ringback from this negative voltage should not cross into the overdrive region. The signals are AERR#, BERR#, BINIT#, BNR#, HIT# and HITM#.

3.6.1. EXTRACT INTERCONNECT INFORMATION

Extract the actual interconnect information for the board from the CAD layout tools.

3.6.2. RUN SIMULATIONS

For timing and signal integrity analysis at the Pentium II processor edge fingers, simulations need to be performed using the fast/slow buffer models, fast/slow connector mode, board impedance and the dielectric extreme values, and V_{TT} and R_{TT} extremes. As shown in

Equation 3 and Equation 4, both the minimum and maximum lengths need to be simulated.

For timing simulations use a V_{REF} voltage of 2/3 V_{TT} ±2% (nominal 1.0V) for both the Pentium II processor and 440 PCIset components. T_{REF} for the Pentium II processor is an idealized 50Ω resistor and an idealized 25Ω resistor for the 440 PCIset, each pulled up to 1.5 V. Flight times measured from the Pentium II processor edge fingers to other system components use the standard method of subtracting the reference delay with this load from the delay to the destination component at 1.0 V.

In addition to standard interconnect simulations for timing and signal quality, Monte Carlo style simulations should be conducted, allowing all the simulation parameters to vary at random within their respective ranges. The recommendations presented in Figure 2 and Table 4 were derived by a combination of standard interconnect and Monte Carlo style simulations.

3.7. Validation

The timing and signal behavior specifications in the *Pentium® II Processor Developer's Manual* are at the processor edge fingers. Signal and timing validation measurements need to be made as close to the Pentium II processor edge fingers as possible.

3.7.1. MEASUREMENTS

In actual systems, the Pentium II processor edge fingers are not easily accessible. In most instances, measurements must be taken at the motherboard solder connection of the Slot 1 connector. To effectively correlate measurements to values at the Pentium II processor edge fingers, the Slot 1 connector minimum or maximum delay must be incorporated. All timings measured at the Slot 1 connector motherboard connection should use a reference voltage of 1 V.

3.7.2. DETERMINING FLIGHT TIME

Flight time is defined as the difference between when a signal at the input pin of a receiving agent crosses V_{REF} and the time that the output pin of the driving agent crosses V_{REF} were it driving the test load used to specify that driver's AC timings. For system measurements, subtracting delay from the in-circuit driver to receiver at V_{REF} is **not** a correct measurement of flight time. To measure in-system flight time, the simulated delay to threshold with the T_{REF} test load pulled to V_{TT} should be subtracted from the delay from the driver to receiver at V_{REF}. It is difficult to define a methodology for determining in-system flight times, and system designers should be aware of the accuracy concerns with this flight time measurement method due to the use of empirical and simulated parameters.

Remember, if measurements are being made at the Slot 1 connector motherboard connection, flight times must be adjusted to incorporate signal delay across the connector. Flight times between a Pentium II processor and a 440 PCIset component should incorporate connector delays for one Slot 1 connector, while flight times between two Pentium II processors should incorporate delays for two Slot 1 connectors.

3.8. Summary of System Design Recommendations

A quick summary of the board design guidelines and recommendations presented in Section 3 are shown in Table 4.

Table 4. Summary of Board Design Guidelines

Parameter	Value	Units
Slot 1 to 440 PCIset trace length	1.5 – 7.0	inches
Slot 1 to Slot 1 trace length	3.0 – 14.0	inches
440 PCIset stub length	0.0 – 1.5	inches
440 PCIset to termination (single processor system)	0.0 – 2.5	inches
Trace line impedance	50 – 80	ohms
Trace line width	5	mils
Trace line spacing	>10	mils
Termination resistance (R_{TT})	56 ±5%	ohms
FR4 dielectric constant	4.2 – 4.8	
PCB signal velocity	1.6 – 2.2	ns/ft
Number of board layers (1)	2 Signal 1 Ground 1 Power	

NOTES:

1. In some dual processor based systems, 4 layers may not be sufficient to physically route the system bus traces. Those systems unable to be routed in 4 layers should use a 6 layer stackup with 4 signal routing layers.

4.0. THEORY

Section 4 presents much of the theory associated with designing a Pentium II processor based system.

4.1. GTL+

GTL+ is the electrical bus technology used for the Pentium II processor bus. GTL+ is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each end of the bus. The specification defines:

- Termination voltage (V_{TT})
- Termination resistance (R_{TT})
- Maximum output low voltage (V_{OL})
- Output driver edge rate under specific load conditions
- Maximum bus agent loading (capacitance and package stub length)
- Receiver high and low voltage level
- Receiver reference voltage (V_{REF}) as a function of termination voltage (V_{TT})
- Receiver ringback characterization

The complete GTL+ specification can be found in the *Pentium® II Processor Developer's Manual*. Layout recommendations for the GTL+ bus can be found in Section 3 of this document.

4.2. Timing Requirements

The system timing for GTL+ is dependent on many things. Each of the following elements combine to determine the maximum and minimum frequency the GTL+ bus can support:

- The range of timings for each of the agents in the system.
  - Clock to output [T_{CO}]. (Note that the system load is likely to be different from the "specification" load therefore the T_{CO} observed in the system may not be the same as the T_{CO} from the specification.)
  - The minimum required time to setup to clock [T_{SU_MIN}] for each receiving agent.
- The range of flight time between each component. This includes:
  - The velocity of propagation for the loaded printed circuit board [S_{EFF}].
  - The board loading impact on the effective T_{CO} in the system.
- The amount of skew and jitter in the system clock generation and distribution.
- Changes in flight time due to crosstalk, noise, and other effects (T_{ADJ}).

4.3. Noise Margin

The goal of these sections is to describe the total amount of noise that can be tolerated in a system (the noise budget), identify the sources of noise in the system, and recommend methods to analyze and control the noise so that the allowed noise budget is not exceeded.

There are several sources of noise which must be accounted for in the system noise budget, including:

- V_{REF} variation
- Variation in V_{TT}
- Crosstalk
- Ringback due to impedance variation along the network, termination mismatch, and/or stubs on the network
- Data pattern dependencies

The total noise budget is calculated by taking the difference in the worst case specified input level and the worst case driven output level.

Sections 4.3.1 and 4.3.2 discuss calculating noise margin. These sections do not discuss ringback tolerant receivers which can increase the effective noise margin. See the component datasheet(s) for information about ringback.

4.3.1. FALLING EDGE OR LOW LEVEL NOISE MARGIN

Equation 5. Low Level Noise Margin

$$\text{Noise Margin}_{\text{LOW LEVEL}} = V_{IL\_MAX} - V_{OL\_MAX} \Rightarrow (V_{REF\_MIN} - 200\text{ mV}) - V_{OL\_MAX}$$

Where:

V_{IL_MAX} = The maximum specified valid input low level from the component specification.

V_{OL_MAX} = The maximum output low level the component will drive.

V_{REF_MIN} = The minimum valid voltage reference used for the threshold reference.

V_{OL_MAX} for the Pentium II processor is 600 mV, and is specified into a 50Ω test load tied to 1.5V. This corresponds to the maximum output low current (I_{OL}) of 18 mA. This implies an effective maximum "on" resistance of 33.33Ω. This maximum condition corresponds to the slow corner components and models. Note that the processor core actually has an output low current of roughly 36 mA, corresponding to a maximum "on" resistance of roughly 16.67Ω. The load seen by the processor core is roughly 25Ω as the 50Ω test load is seen in parallel with the GTL+ termination resistance of 56Ω.

V_{REF_MIN} = $[2/3 (V_{TT\_MIN})] –2\%$

= $[2/3 (1.365 V)] –2\%$

= 892 mV

The output low current for V_{REF_MIN} can be calculated as shown below:

I = V / R

I = 1.365 / (50Ω +33.33Ω) = 16.4 mA

Then the

V_{OL_MAX} for V_{REF_MIN} is (16.4 * 33.33) = 547 mV

So from

Processor Driving Noise $Margin_{LOW\ LEVEL}$

= $(V_{REF\_MIN} –200 mV) –V_{OL\_MAX}$

= (892 mV –200 mV) –547 mV

= 145 mV

4.3.2. RISING EDGE OR HIGH LEVEL NOISE MARGIN

Equation 6. High Level Noise Margin

$$\text{Noise Margin}_{HIGH\ LEVEL} = V_{OH\_MIN} – V_{IH\_MIN} \Rightarrow V_{TT\_MIN} – (V_{REF\_MAX} + 200 mV)$$

Where:

V_{IH_MIN} = The minimum specified valid input high level from the component specification.

V_{OH_MIN} = The minimum output high level the component will drive.

V_{TT_MIN} = The minimum termination voltage.

V_{REF_MAX} = The maximum valid voltage reference used for the threshold reference.

V_{OH_MIN} for the GTL+ signals is V_{TT_MIN}. For the Pentium II processor this is 1.365 V. Since V_{REF} is defined as a function of V_{TT} the maximum V_{REF} when V_{TT} is 1.365 V is

= 2/3 * (1.365) +2% = 928 mV.

Then Noise $Margin_{HIGH\ LEVEL}$

= $V_{TT\_MIN} –(V_{REF\_MAX} +200 mV)$

= 1.365 V –928 mV –200 mV

= 237 mV

Note that while the high level noise margin is not sensitive to the value of the termination resistance, using larger value termination resistors would reduce the current in the line, slowing the rising edge rate and hence increasing the flight time.

4.3.3. RECOMMENDED NOISE BUDGET

The slow corner falling edge noise margin is reduced due to the increase in V_{OL} associated with the reduced drive capability of the worst case buffer, yielding the smallest margin. This requires a different budget than the fast corner falling edge or the rising edges. The slow corner edge rates are slowed by approximately 1/3, resulting in a maximum crosstalk length that is three times longer than those at the fast corner. Systems that are designed to minimize crosstalk with the fast corner edge rates, are not likely to have the maximum crosstalk lengths at the slow corner. Therefore, maximum coupled noise is unlikely to occur. In addition, the voltage swing is reduced by 15%, reducing the crosstalk budget to 60 mV. This leaves only 100 mV for the ringback portion of the noise budget which can be achieved with the slower edge and reduced voltage swing. The biggest concern for the slow corner signal quality is achieving a sufficiently low V_{OL}. Using 1 ounce copper or shortening the maximum network

length may be necessary to minimize the V_{OL} loss along the network. Adjusting R_{TT} to balance the noise margin could also be an option.

A representative noise budget (within the setup window, V_{TT} = 1.5V and V_{REF} –2/3 V_{TT}) for all rising edges and the typical falling edge is:

V_{REF} variation	20 mV
V_{TT} variation	20 mV
Crosstalk	110 mV
Ringback	150 mV
Total budget	300 mV

A representative noise budget (within the setup window, V_{TT} = 1.5V and V_{REF} –2/3 V_{TT}) for the slow corner falling edge is:

V_{REF} variation	20 mV
V_{TT} variation	20 mV
Crosstalk	60 mV
Ringback	100 mV
Total budget	200 mV

The V_{REF} variation is based on the ±2% tolerance in V_{REF}. The V_{TT} variation term is based on shifting V_{OL} closer to V_{REF} when V_{TT} is lowered (simple voltage divider effect). The required margin for these can both be reduced by holding tighter tolerances on V_{TT}.

The crosstalk budget comes from 5 mil lines with 10 mil spacing (5/10), using 1/2 ounce/ft^2 copper and a dielectric constant of 4.0. This budget also assumes that there is no doubling; see Sections 4.4 and 4.4.1. Using 1 ounce/ft^2 copper (1.4 mil thick) doubles the cross-sectional area of the traces and therefore doubles the crosstalk. Using a dielectric material with a constant higher than 4.0 will cause the signals to propagate at a slower rate. Using a higher dielectric constant material while maintaining the same impedance will cause the traces to be farther from their reference plane, increasing crosstalk. The total impact of using a higher dielectric material, while keeping the rest of the board parameters the same, is more noise from crosstalk.

Ringback is a function of the following parameters:

- R_{TT} value (and variation)
- Driver's edge rate
- Stubs along the network and their length (including internal package connection)
- Inter-agent spacing
- Total network length
- Bus agent position
- Impedance variations (PCB material and internal package stubs)

4.4. Crosstalk Theory

GTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies that have traditionally been used in personal computer designs. This requires that designers using GTL+ be more aware of crosstalk than they may have been in past designs.

Crosstalk is caused through capacitive and inductive coupling between networks. Crosstalk appears as both backward crosstalk and as forward crosstalk. Backward crosstalk creates an induced signal on a victim network that travels in a direction opposite that of the aggressor's signal. Forward crosstalk creates a signal that travels in the same direction as the aggressor's signal. On the GTL+ bus, a driver on the aggressor network is not at the end of the network, therefore it sends signals in both directions on the aggressor's network. The signal propagating in each direction causes crosstalk on the victim network. The maximum crosstalk occurs when all the aggressors are switching in the same direction at the same time. Figure 5 shows a driver on the aggressor network and a receiver on the victim network that are not at the ends of the network. There may be crosstalk internal to the component packages, which can also affect the signal quality/noise.

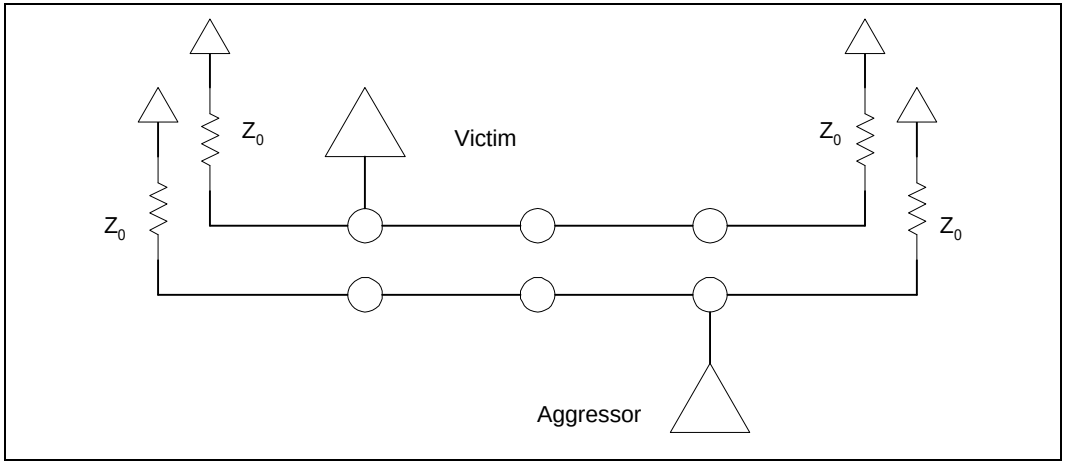

Figure 5. Driver on Aggressor Network: Receiver on Victim Network

Backward crosstalk is present in both stripline and microstrip geometries (see Figure 6). (A way to remember which geometry is stripline and which is microstrip is that a stripline geometry requires stripping a layer away to see the signal lines.) The backward coupled amplitude is proportional to the backward crosstalk coefficient, the aggressor's signal amplitude, and the coupled length of the network up to a maximum which is dependent on the rise time of the aggressor's signal. Backward crosstalk reaches a maximum (and remains constant) when the propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing, and the rise time on an unloaded coupled network, then:

*Length for Max. Backward Crosstalk = (1/2 * Rise Time) / Board Delay per Unit Length*

Agents on the GTL+ bus drive signals in each direction on the network. This will cause backward crosstalk from segments on two sides of a driver. The pulses from the backward crosstalk travel toward each other and will meet and add at certain moments and positions on the bus. This can cause the voltage (noise) from crosstalk to double. Backward crosstalk will transition in the same direction as the aggressor's edge.

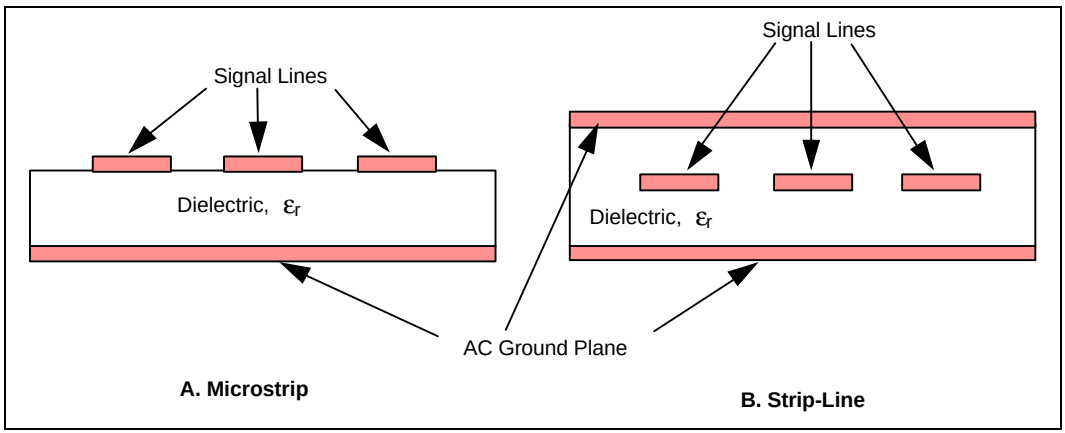

Figure 6. Transmission Line Geometries

Forward crosstalk is absent in stripline topologies, but present in microstrip. (This is for the ideal case with a uniform dielectric constant. In actual boards, forward crosstalk is nearly absent in stripline topologies, but more prevalent in microstrip.) The forward coupled amplitude is proportional to the forward crosstalk coefficient, the aggressor's signal edge rate (dv/dt), and the coupled network's electrical length. The forward crosstalk coefficient is also a function of the geometry. Unlike backward crosstalk, forward crosstalk can grow with coupled section length, and may transition in a direction similar to or opposite to that of the aggressor's edge.

Since forward coupled signals travel in the same direction as the aggressor's, an agent on the GTL+ bus that has coupled sections on both sides of itself will not run the risk of the two forward coupled signals meeting and adding. However, unlike backward crosstalk, each signal will continue to grow as it passes through more coupled length before the aggressor's wave front is absorbed by the termination.

4.4.1. CROSSTALK MANAGEMENT

To minimize crosstalk (and the "cost" of crosstalk) in terms of noise margin budget:

- Route adjacent trace layers in different directions (orthogonal preferred) to minimize the forward and backward crosstalk that can occur from parallel traces on adjacent layers. This reduces a source of crosstalk.
- Maximize the spacing between traces. Where traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between sections that have close spacing. Routing close together could occur where multiple signals have to route between a pair of pins. When this happens the signals should be spread apart where possible. As an example: Two traces at 5/5 (5 mil lines with 5 mil spaces) for two separate 2 inch sections that are spaced at least one half of the rise time apart is better than having a single 4 inch section at 5/5 spacing.
- Minimize the nominal board impedance (Z_0) within the GTL+ specification. For a given dielectric constant, this reduces the spacing between the traces and their reference plane, which reduces the backward and forward crosstalk coefficients. Having reduced crosstalk coefficients reduces the magnitude of the crosstalk.
- Minimize the dielectric constant used in the PCB fabrication. As above, all else being equal, this puts the traces closer to their reference planes and reduces the magnitude of the crosstalk.
- To avoid backward crosstalk at the extreme ends of the bus, connect the end bus agents to the termination resistors using microstrip traces of the same impedance as the rest of the GTL+ bus (this will have to be evaluated with other system constraints). This can be ignored in dual processor Pentium II systems since both ends of the bus are terminated on the processors.
- Watch out for voltage doubling at a receiving agent, caused by the adding of the backward crosstalk on either side of a driver. Minimize the total network length of signals that have coupled sections. If there has to be closely spaced/coupled lines, place them near the center of the net. This will cause the point in time that voltage doubling occurs to be before the setup window.
- Route synchronous signals that could be driven by different components in separate groups to minimize crosstalk between these groups. The Pentium II processor uses a split transaction bus. This implies, that in a given clock cycle, the address lines and corresponding control lines could be driven by a different agent than the data lines and their corresponding control lines. If these two agents are at the opposite process corner (one fast and one slow), then separating the signal types will support the budget assumptions in Section 4.3.3.
- Minimize the cross-sectional area of the trace. This can be done by using narrower traces and/or by using thinner copper (1/2 ounce/ft^2 or 0.7 mil thick rather than 1 ounce/ft^2 or 1.4 mil thick). Note that the trade-off for this smaller cross-sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the increased I*R loss along the trace.

Simulation shows that 5/5 technology (5 mil lines with 5 mil spaces) will have excessive crosstalk between networks on the Pentium II processor bus. This is due to the lower voltage swing of GTL+, high frequencies (even with the controlled edge rate buffers) and likely long parallel traces.

4.4.2. POTENTIAL TERMINATION CROSSTALK PROBLEMS

The use of standard "pull-up" resistor networks for termination may not be suitable. These networks have a common power or ground pin at the extreme end of the

package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks that have separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

5.0. MORE DETAILS AND INSIGHTS

5.1. Textbook Timing Equations

The textbook equations used to calculate the propagation rate of a signal in a PCB are the basis for spreadsheet calculations for timing margin. These equations are:

Equation 7. Intrinsic Impedance

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

Equation 8. Stripline Intrinsic Propagation Speed

$$S_{0\_STRIPLINE} = 1.017 * \sqrt{e_r}$$

Equation 9. Microstrip Intrinsic Propagation Speed

$$S_{0\_MICROSTRIP} = 1.017 * \sqrt{0.475 * e_r + 0.67}$$

Equation 10. Effective Propagation Speed

$$S_{EFF} = S_0 * \sqrt{1 + \frac{C_D}{C_0}}$$

Equation 11. Effective Impedance

$$Z_{EFF} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$

Equation 12. Distributed Trace Capacitance

$$C_0 = \frac{S_0}{Z_0}$$

Equation 13. Distributed Trace Inductance

$$L_0 = Z_0 * S_0$$

Where (for Equation 7 through Equation 13):

S_0 = The speed of the signal on an unloaded PCB. This is referred to as the board propagation constant.

S_0 MICROSTRIP and S_0 STRIPLINE
= The speed of the signal on an unloaded microstrip or stripline trace on the PCB.

Z_0 = The intrinsic impedance of the line and is a function of the dielectric constant (ε_r), the line width, line height and line space from the plane(s). The equations for Z_0 are not included in this document. See the *MECL System Design Handbook* by William R. Blood, Jr. for these equations.

C_0 = The distributed trace capacitance per unit length of the network.

L_0 = The distributed trace inductance per unit length of the network.

C_D = The sum of the capacitance of all devices and stubs divided by the length of the network's trunk, not including the portion connecting the end agents to the termination resistors.

S_{EFF} and Z_{EFF}
= The effective propagation constant and impedance of the PCB when the board is "loaded" with the components.

5.2. Reference Planes

Designs using the Pentium II processor require several different voltages. The following paragraphs describe some of the impact of three common methods used to distribute the required voltages. Refer to the *Pentium® II*

Processor Power Distribution Guidelines (Order Number 243332) for more information on power distribution.

The most desirable method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes are used for an “AC ground” reference for traces to control trace impedance on the board, then the plane needs to be well decoupled to the system ground plane. This method may require more total layers in the PCB than other methods.

A second method of power distribution is to use partial planes in the immediate area needing the power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing area that can be used to route traces. These partial planes may also change the impedance of adjacent trace layers. (For instance, the impedance calculations may have been done for a microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.)

The third method to distribute the power is to incorporate split power planes. This method is similar to the second method except that the multiple voltages share the conventional power plane layer. The power plane is split so that areas of the board needing separate voltages are divided to provide a separate voltage for each area. These areas still need to be properly decoupled, especially at the edges of each plane. The gap between the different power planes on a layer should be kept to a minimum. There will be a negligibly small impedance discontinuity in traces that cross the split and are using the power plane for a reference plane. It is very important when splitting planes that the GROUND plane not be split, as this could create significant length in the ground return path, adding noise in the system. Decoupling the different power planes, which are adjacent on the same layer may also be valuable for signals that use the split power planes for AC reference. The split plane method is not universally agreed upon as engineering good practice. If your company is not comfortable splitting planes, then you should use a different method.

5.3. PCB Stackup

The type and number of layers for the PCB need to be chosen to balance many requirements. Many of these requirements are technical and include:

- Providing enough routing channels to support the minimum and maximum timing requirements of the components.
- Providing stable voltage distribution for each of the components.
- Providing uniform impedance for the Pentium II processor bus and other signals as needed.
- Minimizing coupling/crosstalk between the networks.
- Minimizing RF emissions.
- Minimizing PCB cost.
- Minimizing cost to assemble PCB.

Design your PCB to meet these technical requirements.

6.0. CONCLUSION

GTL+ routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will allow a designer to avoid the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.