Design Recommendations for Display Compatibility on Intel® Integrated Graphics Chipsets

Application Note

October 2002

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Revision History

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251936	-001	Initial Release.	October 2002

1 Introduction

1.1 Terminology

Term	Description
DVO	Digital Video Out, multiplexed on the GMCH AGP port, this interface contains all data and side-band signals intended for a DVO translator device.
DVI	Digital Video Interface, generally regarded as the part of the interface between the DVO translator device and the Digital Flat Panel monitor.
DFP	Digital Flat Panel monitor
ADD card	AGP Digital Display card. The ADD card implementation only applies to the Intel® 845G chipset family.
I^2C	Two-wire serial interface intended for side-band communication between the GMCH and the DVO translator device, for configuration purposes.
MDVI / DDC	Two-wire serial interface intended for side-band communication between the GMCH and the Digital Flat Panel, for configuration purposes.

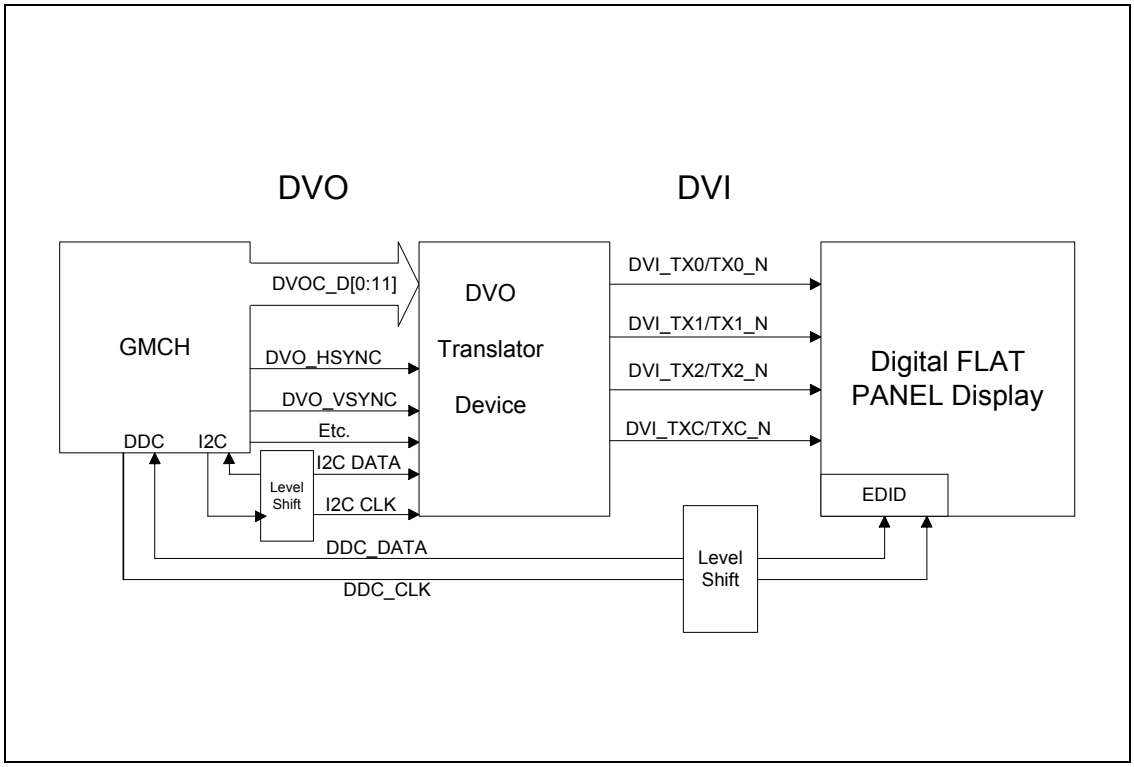
1.2 Overview

This document applies to all of Intel's integrated chipset products and describes the graphics & memory controller hub (GMCH) DVO/DVI implementation in order to enable robust Vil/Vol levels across a wide range of digital and analog displays. This document uses a case study example to illustrate the recommended implementation.

2 Background

Digital and analog monitors use a 5V interface, while the chipset uses a 1.5V interface. This requires the use of level-shifting circuitry, either down on the motherboard, or on the ADD card. This circuitry interfaces with the I^2C and MDVI/DDC channels that are used to read configuration data in the DVO translator and the DFP. The I^2C and MDVI/DDC channels use open-drain type driver circuits that only drive low, and therefore require external pull-up resistors to drive the signal high. If the DFP has weak driver circuitry, and the pull-up resistors used in the level shifter are strong pull-ups (low resistance), then the DFP may not be able to drive below the GMCH specified Vol(max). This can result in the GMCH not seeing the transition, thus not detecting the device or port, resulting in no video on the DFP display.

Figure 1 Simplified Block Diagram

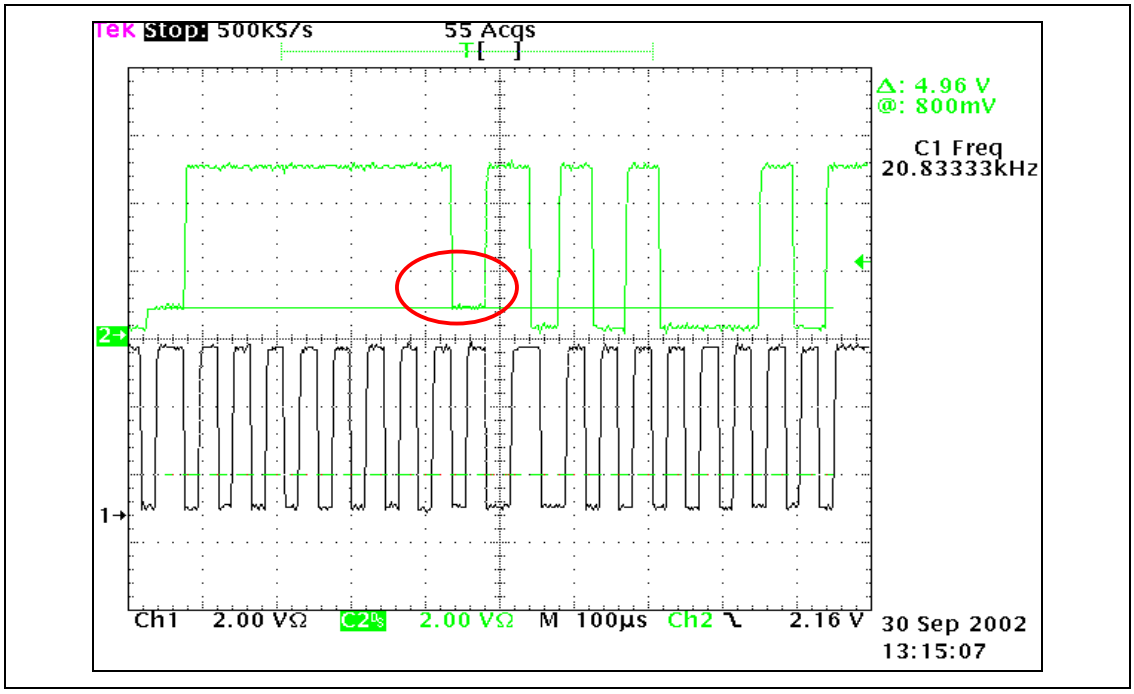


3 Detail

3.1 Case Study

The effect of weak driver circuitry on Digital Flat Panel monitors, in this case, can be easily seen by using an oscilloscope to look at the MDVI or DDC data line on the monitor-side of the level shifter. An example of a DFP monitor with insufficient drive strength can be seen in the Figure below:

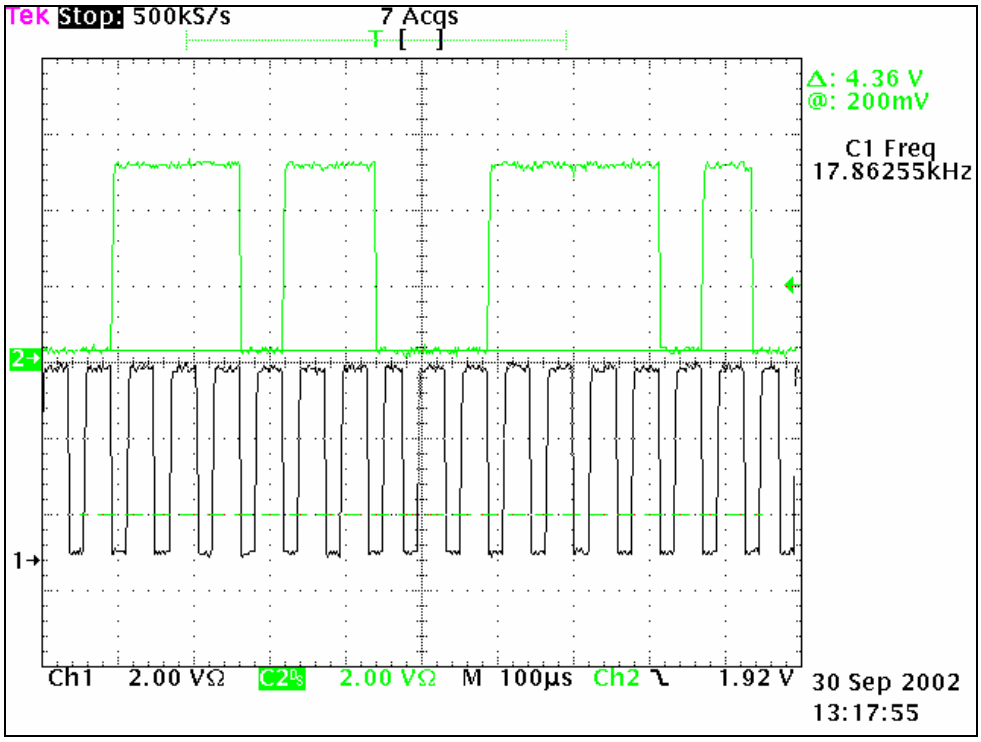
Figure 2. Scope capture of weak DDC drivers in a failing DFP



Note that this particular flat panel was driving back a Vol of 800mV. In this case, the level shifter being used was a GTL2010 voltage clamp. This device clamps its Voh/Vih with respect to the pull-ups used on its inputs and outputs, but leaves the low levels effectively the same. In this case, the monitor's ACK pulse (shown in green in Figure 2) was attenuated through the level shifter from a 5V swing to a 1.5V swing, but the 800mV low pulse was "passed through" and left unchanged. The result was that the GMCH did not recognize that a DFP was connected since the Vol(max) was not crossed, and the port was disabled, resulting in no display on the DFP.

An example of a DFP with stronger drivers, can be seen in Figure 3 below. :

Figure 3. Scope capture of a functioning DFP



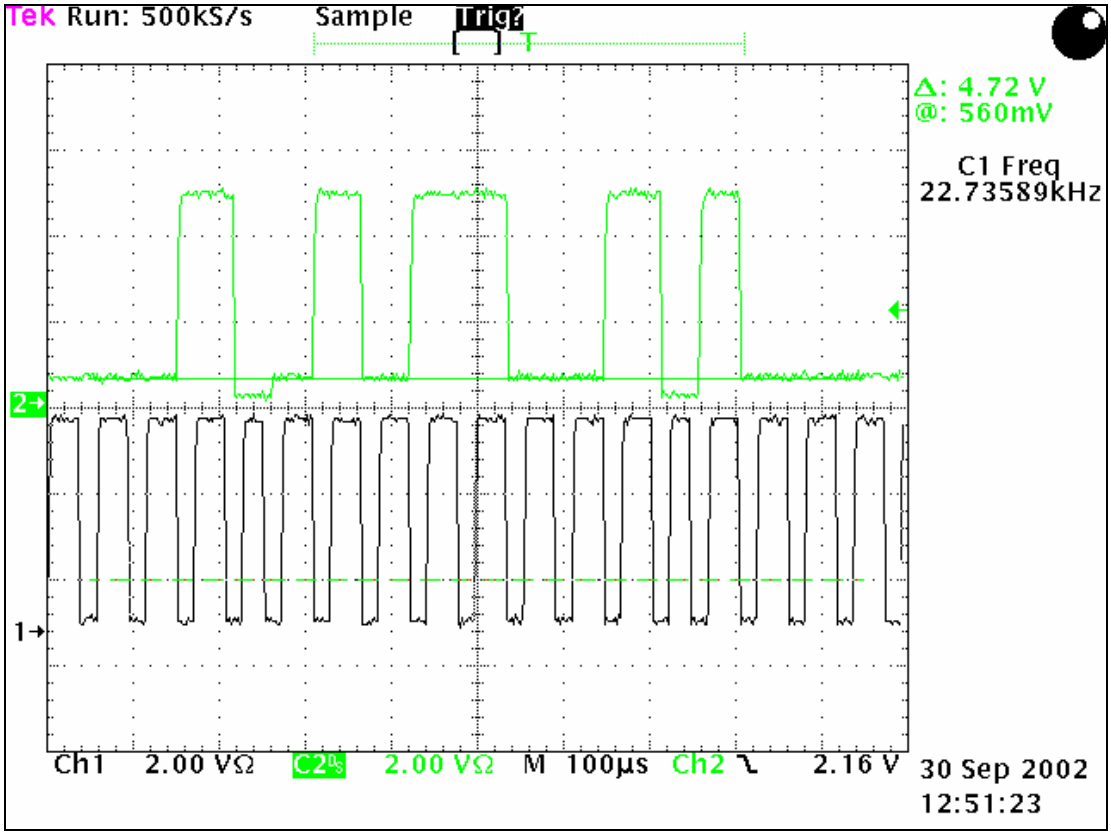
Note that the DFP in this case was driving back a Vol of 200mV, and worked consistently.

Both of these DFP monitors in the previous examples were using the same system and same ADD card. The ADD card contains the interface to the AGP slot, the DVO translator device, the level shifting circuitry and the connector for the DFP monitor. The DFP monitor that did not work (Figure 2) could not overcome the pull-up resistor on the DDC line. In this case, the pull-up resistor value used on this ADD card for the DDC_DATA line on the monitor side of the level shifter was 2.2K Ohms pulling up to 5V.

3.2 The Solution

Changing the pull-up resistor on the DDC_DATA line to 5.6K Ohms, resulted in a lower Vol, as shown in the Figure below.

Figure 4. DDC-Data line pull-up resistor change



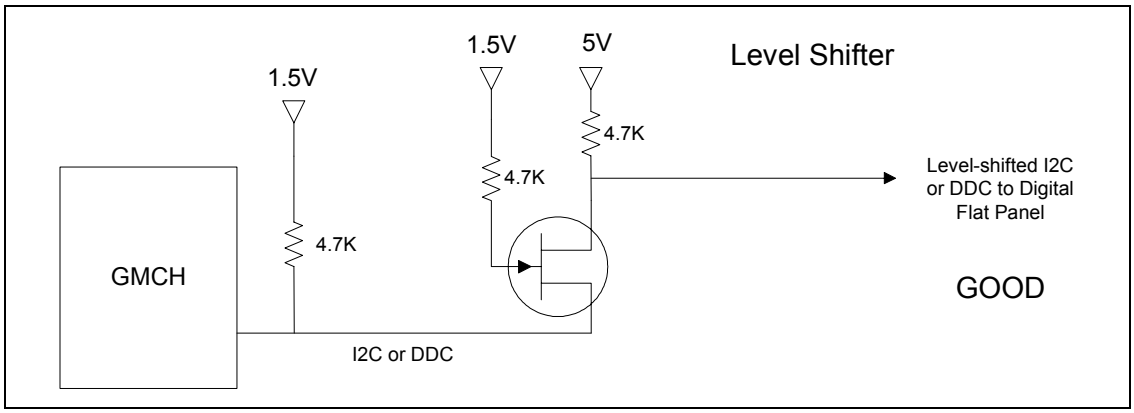
Note that this previously failing DFP can now drive down to 560mV (within specified GMCH Vol input range) and at this level the display became functional.

3.3 Conclusion

Specifications of load capacity for the I^2C and MDVI/DDC interface as defined by VESA do not meet current industry standards for low-voltage signaling. Therefore, the behavior of monitors that support this interface can vary widely. Although, most seem to support standard Vil/Vih, Vol/Voh specifications, it is recommended that the designer take into account that some monitors are weak in this area and design their level shifting circuitry accordingly. Weaker pull up resistors can help greatly.

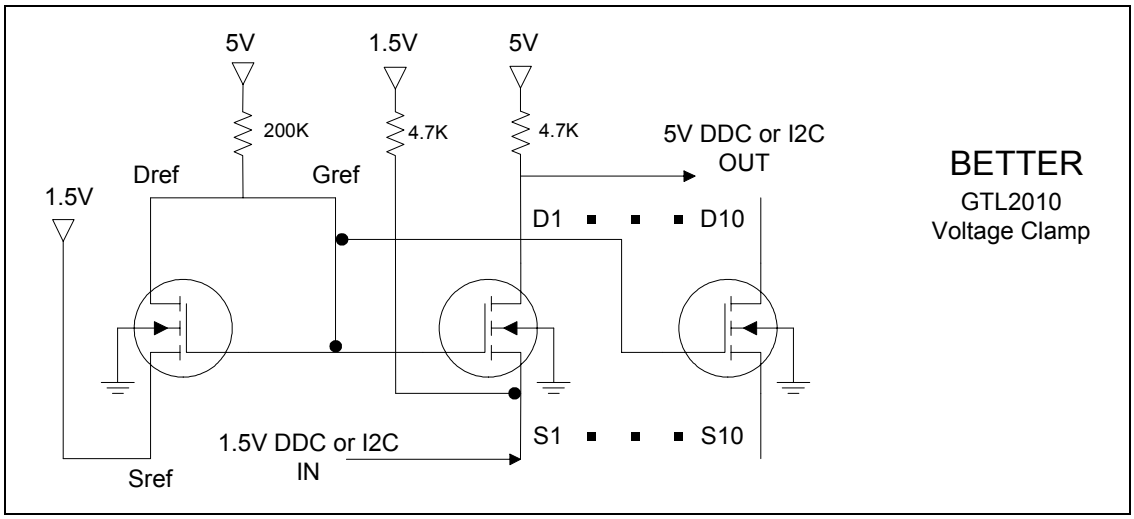
4 Level Shifter Examples

Figure 5. FET-based Level Shifter



NOTE:
Pull up resistor values may vary. Some flat panel displays have weak drivers and may require weaker pull-ups.

Figure 6. GTL2010 Voltage Clamp



NOTE:
Pull up resistor values may vary. Some flat panel displays have weak drivers and may require weaker pull-ups.