Controlled Impedance Design and Test

Intel Corporation

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Agenda

- Statement of Objective
- Background
- AC Timing and Signal Quality
- Impedance Fundamentals
- Design Guidelines
- Testing Board Impedance (TDR)
- Summary and Conclusions

Objective

The objective of this presentation is to provide information to assist OEMs and PCB vendors to design and test motherboards which will meet a 28 Ω (+/- 10%) impedance specification

Background

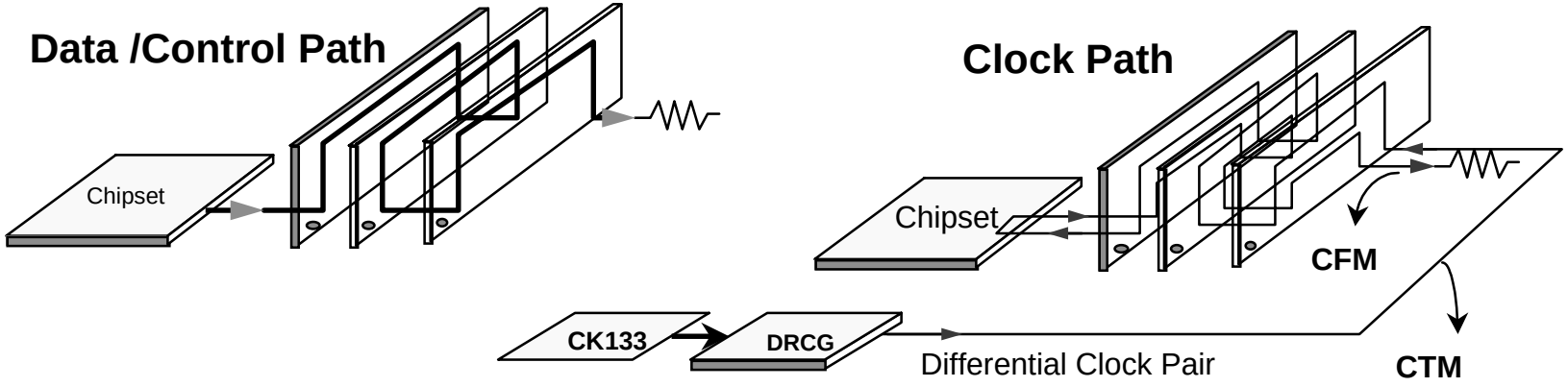
- Existing motherboards are designed around 65 Ω +/-15%
- The new 28 Ω +/-10% specification is required by the memory channel
- Exceeding the specification results in additional channel timing error and reduced signal margin
- Both effects may cause failures on the memory channel

Signal Quality and Timing

- RDRAM Channel is designed for 28 Ω
- Impedance mismatch causes signal reflections
- Reflections reduce voltage and timing margins
- AC Timings are tight!
  - 2X clock @ 400MHz Operation = 1.25ns window
  - Only 100 - 150 ps allowed for total channel timing error
  - PCB impedance is only one factor
- PCB process variation -> Z0 variation -> Channel error

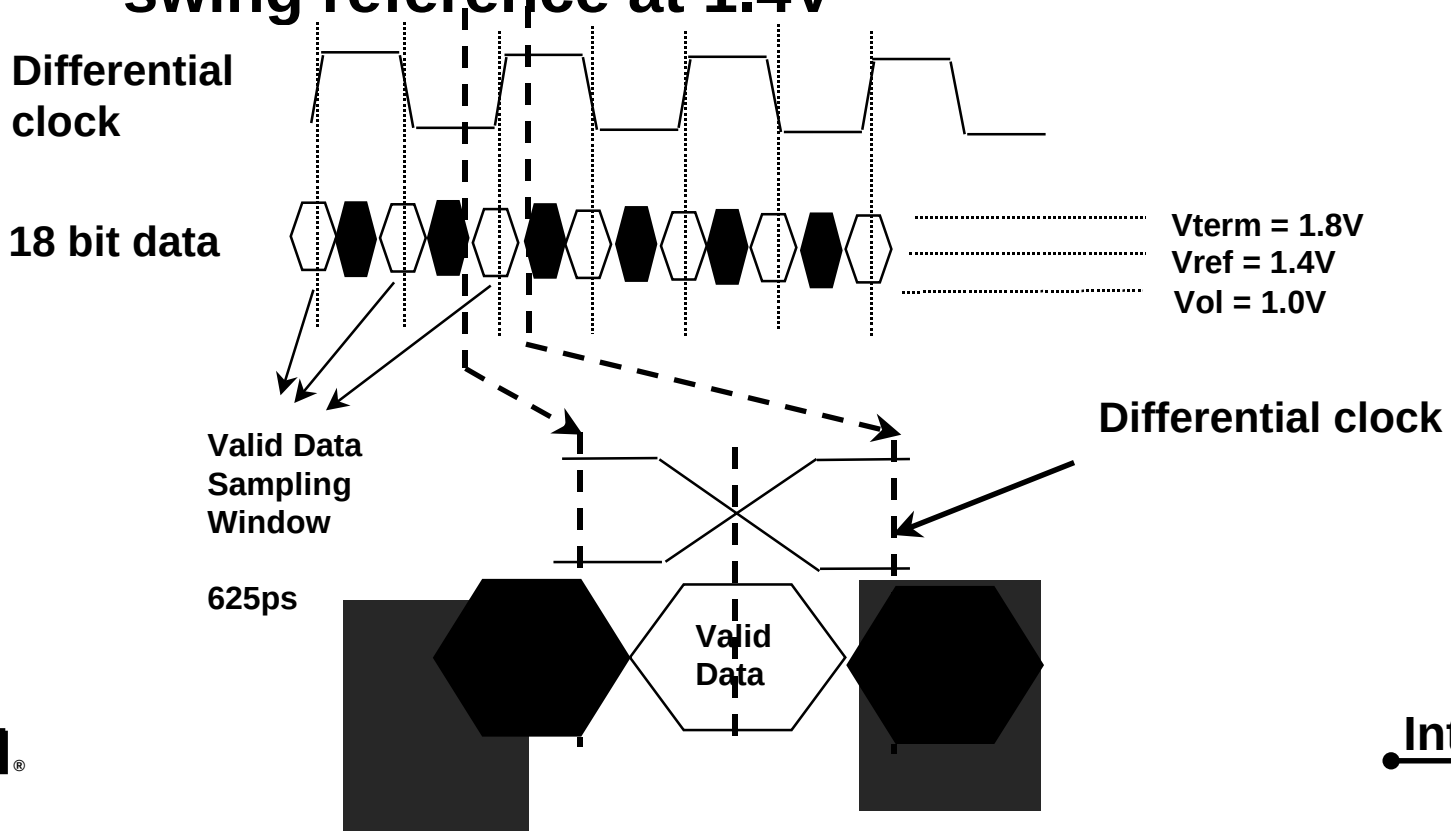
THIS IS WHY HITTING 28 Ω IS CRITICAL

RDRAM Signal Routing



Data Signal and Sampling

- Data is sampled on both edges of the clock
  - 625ps data window
- 0.8V low signal swing between logic 0 and 1, signal swing reference at 1.4V



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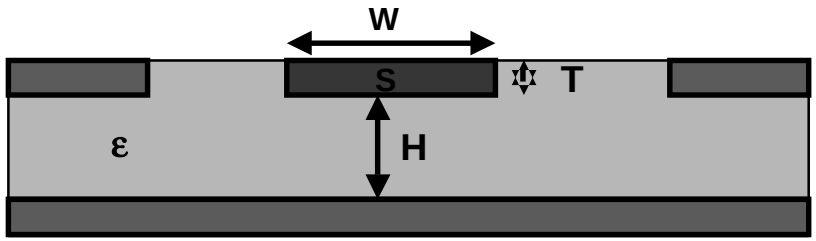
Impedance Fundamentals

- Microstrip vs Stripline
- PCB Parameters and Relationship to Impedance
- Simulation Tools (Field Solvers) and Impedance Calculators
- PCB Materials
- Chipset Example

Microstrip X-Section



Z0 = F(W,H,T,ε)

EQUATIONS FOR Z0 USED IN ZCAL PROGRAM

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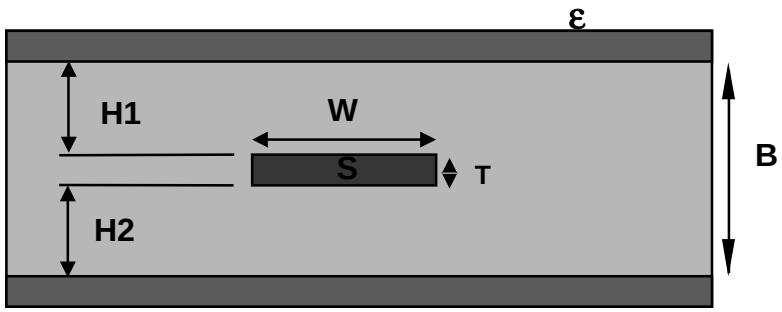
Stripline X-Section



Z0 = F(W,H1,H2,T,ε)

EQUATIONS FOR Z0 USED IN ZCAL PROGRAM

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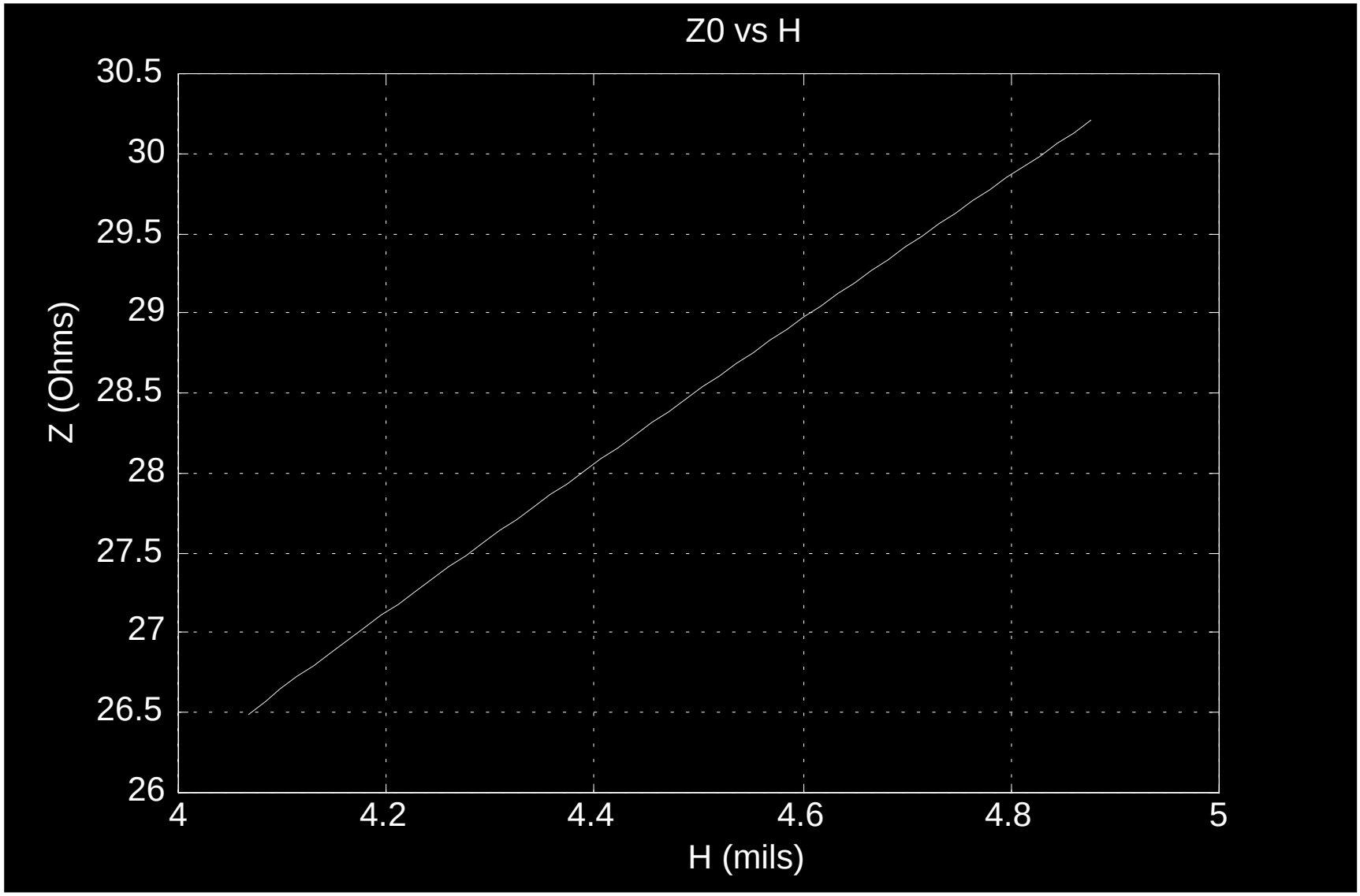
PCB Parameters

- H tolerance is hardest to control
- W & T has less impact due to wider trace
- Z0 can be calculated from geometries
  - Equations (like zcalc) are approximate
  - 3D Field Solvers also used to calculate impedance
- Plot of Z0 variation with various parameters (W, H, ε_r, T) shows impact
  - Also show what tolerances we need to hit for the various geometries

Z0 vs H (W=18mils, T=1.4mils, ε_r=4.5)



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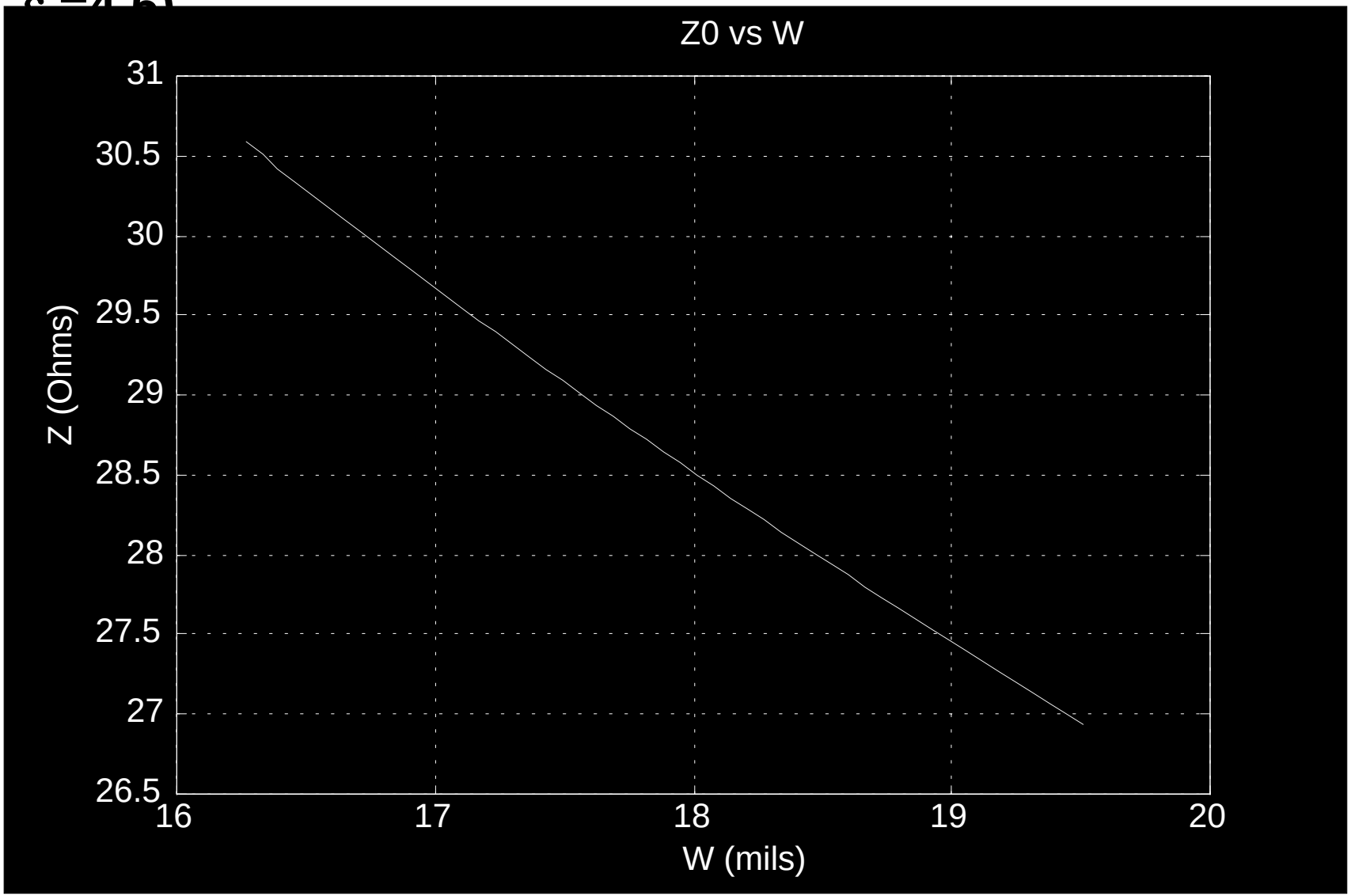
Z0 vs W (H=4.5mils, T=1.4mils, ε=4.5)



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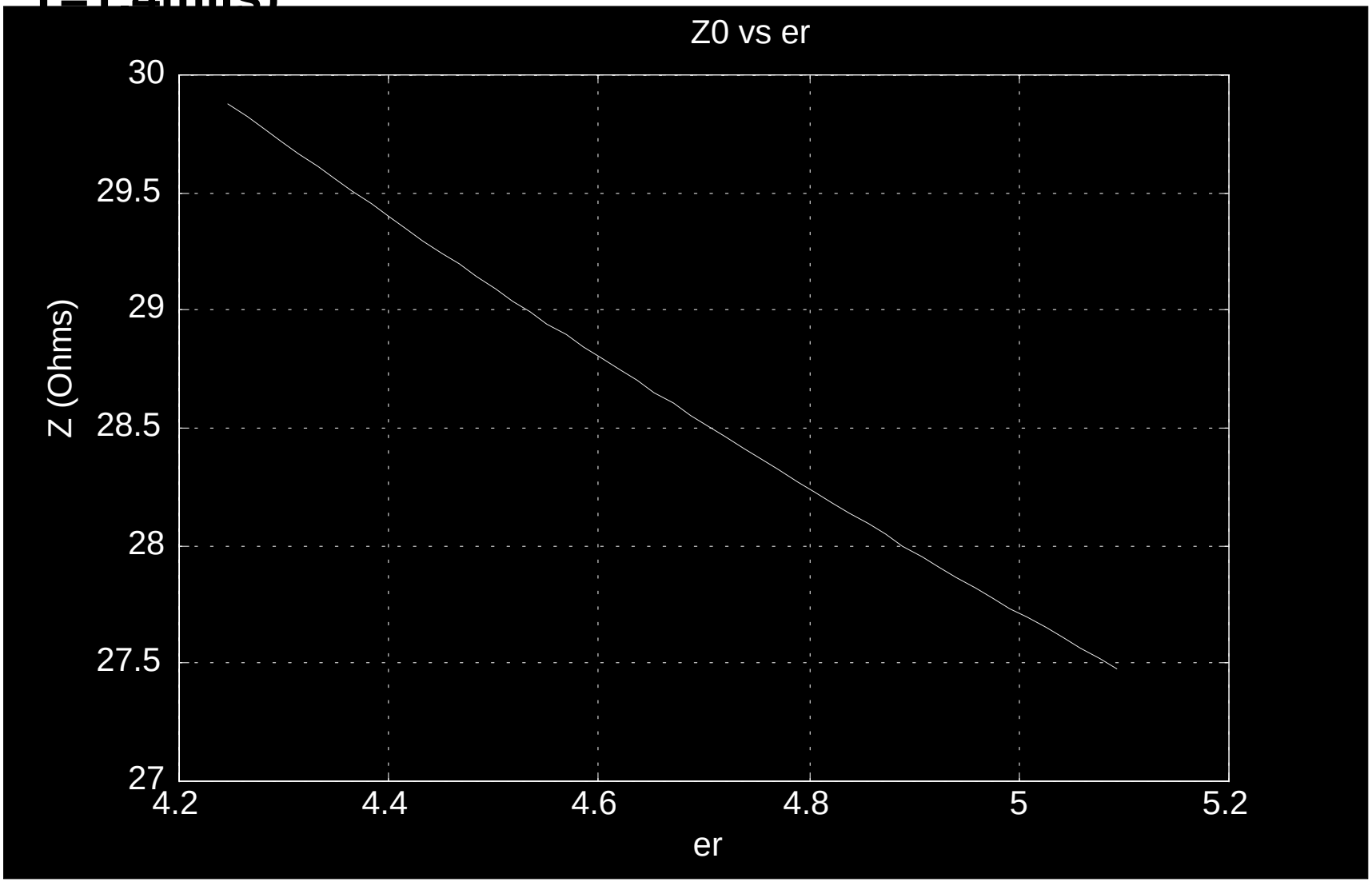
Z0 vs ε_r (H=4.5mils, W=18mils, T=1.4mils)



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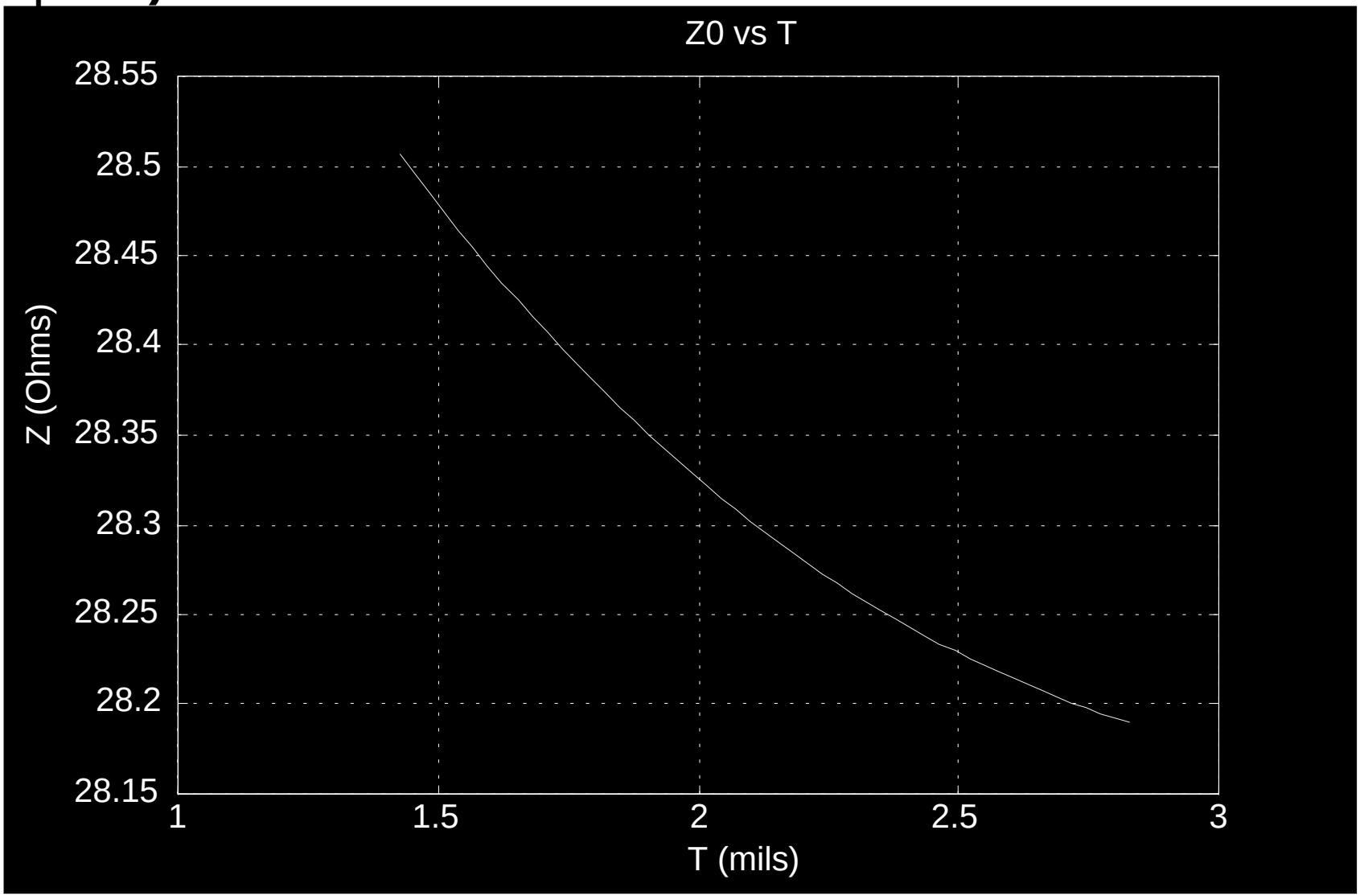
Z0 vs T (H=4.5mils, W=18mils, ε_r=4.5)



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Impedance Calculation

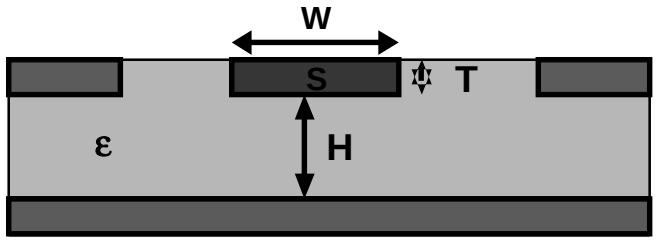
- 3D Field Solvers are most accurate
  - HP, Ansoft, Sonnet, Polar etc
- Z calculators based on equations are also pretty accurate

3D Field Solver vs ZCALC

	#1	#2	#3	#4	#5	#6
H	4.5	4.5	4.2	4.8	4.5	4.5
W	18	18	18	18	17	19
W1	18.1	18.1	18.1	18.1	17.1	19.1
T	1.4	2.8	1.4	1.4	1.4	1.4
εr	4.5	4.5	4.5	4.5	4.5	4.5
Z0 (3D)	29.0	28.4	27.6	30.4	30.2	27.9
Z0 (zcalc)	29.1	28.7	27.7	30.4	3.02	28.0

PCB Materials

- PCB tolerances determine Z0 variation
  - Dielectric thickness, trace width, plating thickness, dielectric constant and solder mask thickness
- Pre-preg style type and characteristics determine H variation
  - single ply vs. 2-ply
  - resin content and tolerance
  - flow tolerance



- Recommended material tolerances:
  - Dielectric height tolerance +/- 10% (~ 0.4mil)
  - Trace width tolerance +/- 3% (~ 0.5mil)
  - Pre-preg resin content tolerance +/- 3%
  - Pre-preg resin flow tolerance +/- 3%
  - e_r tolerance +/- 5% (~0.2) @ 1GHz

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Design Process

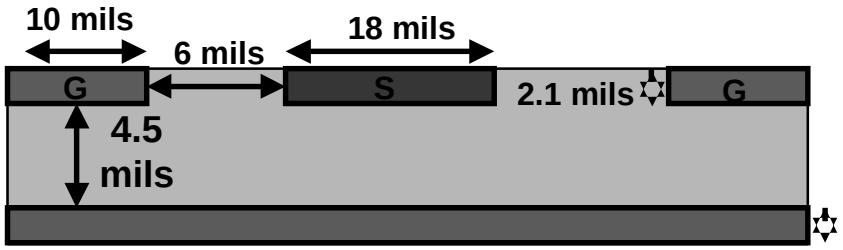
- Specify material to be used
- Calculate board geometries for desired impedance - or use example stackup
- Build test boards and coupons
- Measure board impedance using TDR
  - Need accurate data - follow TDR methodology
- Measure geometries with x-section
- Adjust design parameters and/or material as required
- Build new board and re-measure
  - May require one or two iterations

Design Guidelines

- Several reference stackups provided
- Test coupon should be included on panel
  - If possible, integrate test coupon pattern into board
  - Makes lot sampling easier, more accurate
  - Test coupon probe pattern
    - Must match probe type
  - Gerber file is available
- Don’t forget about other traces on PCB!
  - Need to adjust other trace widths to meet impedance requirements for different busses

Recommended Stackup

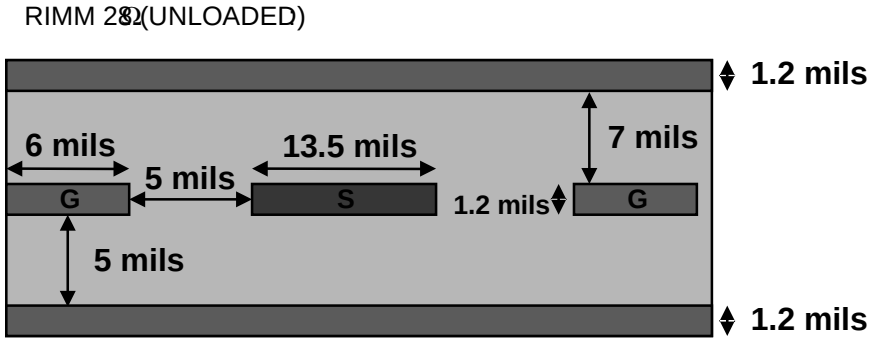
- Numerous variations are possible
- We used the following as a starting point:
  - W=18mil, H=4.5mil, T=2.0, 1 ply 2116 pre-preg



Don’t forget ground floods and stitching

Inner Layer Routing

- Also numerous possible stackups
- We used the following as a starting point:
  - W=13.5mil, H1=7mil, H2=5, T=1.2



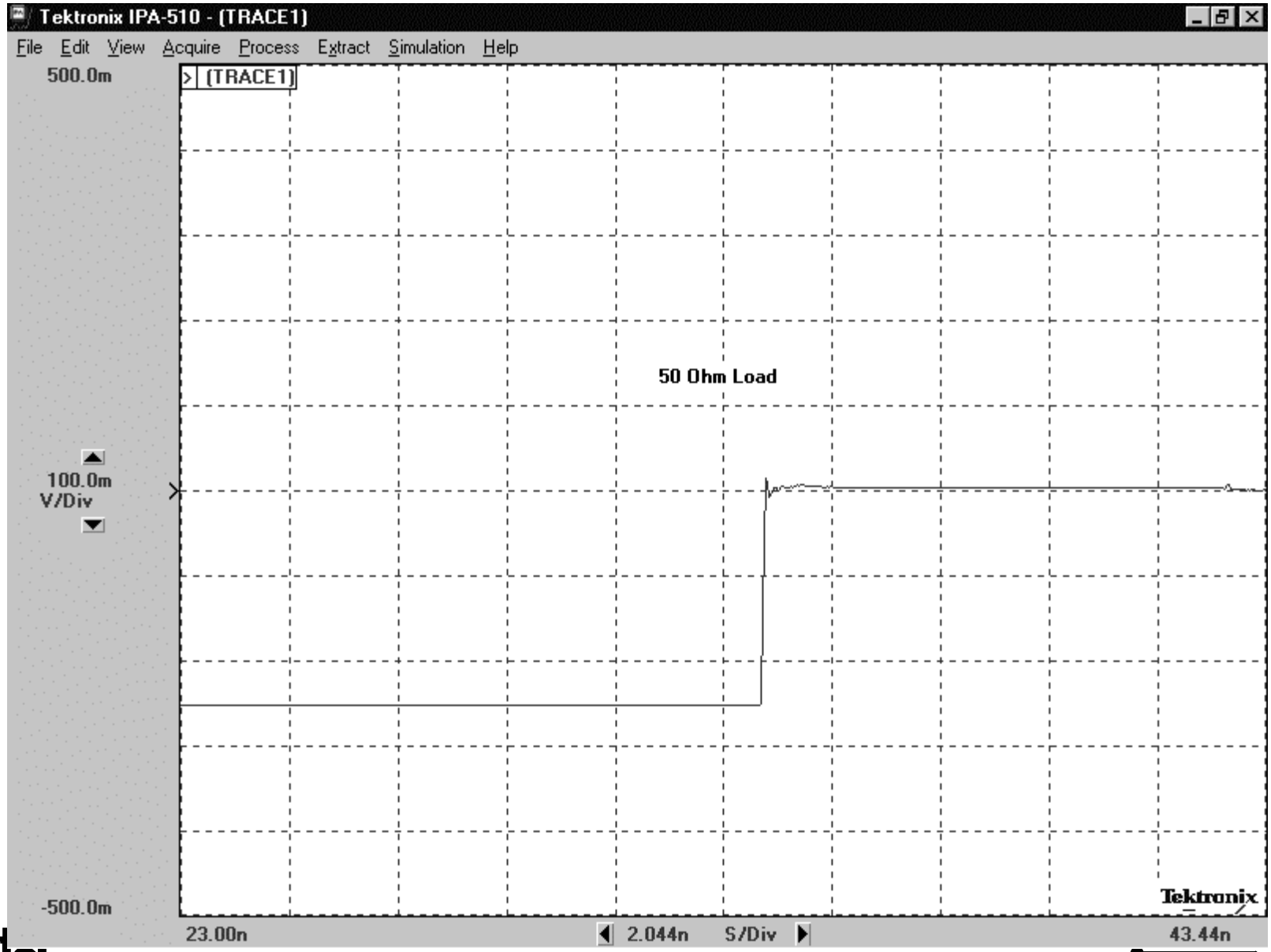
Testing Board Impedance

- TDR Basics
- Test Equipment
- Test Coupon
- Test Procedure
- HVM Testing
- Reference Collateral

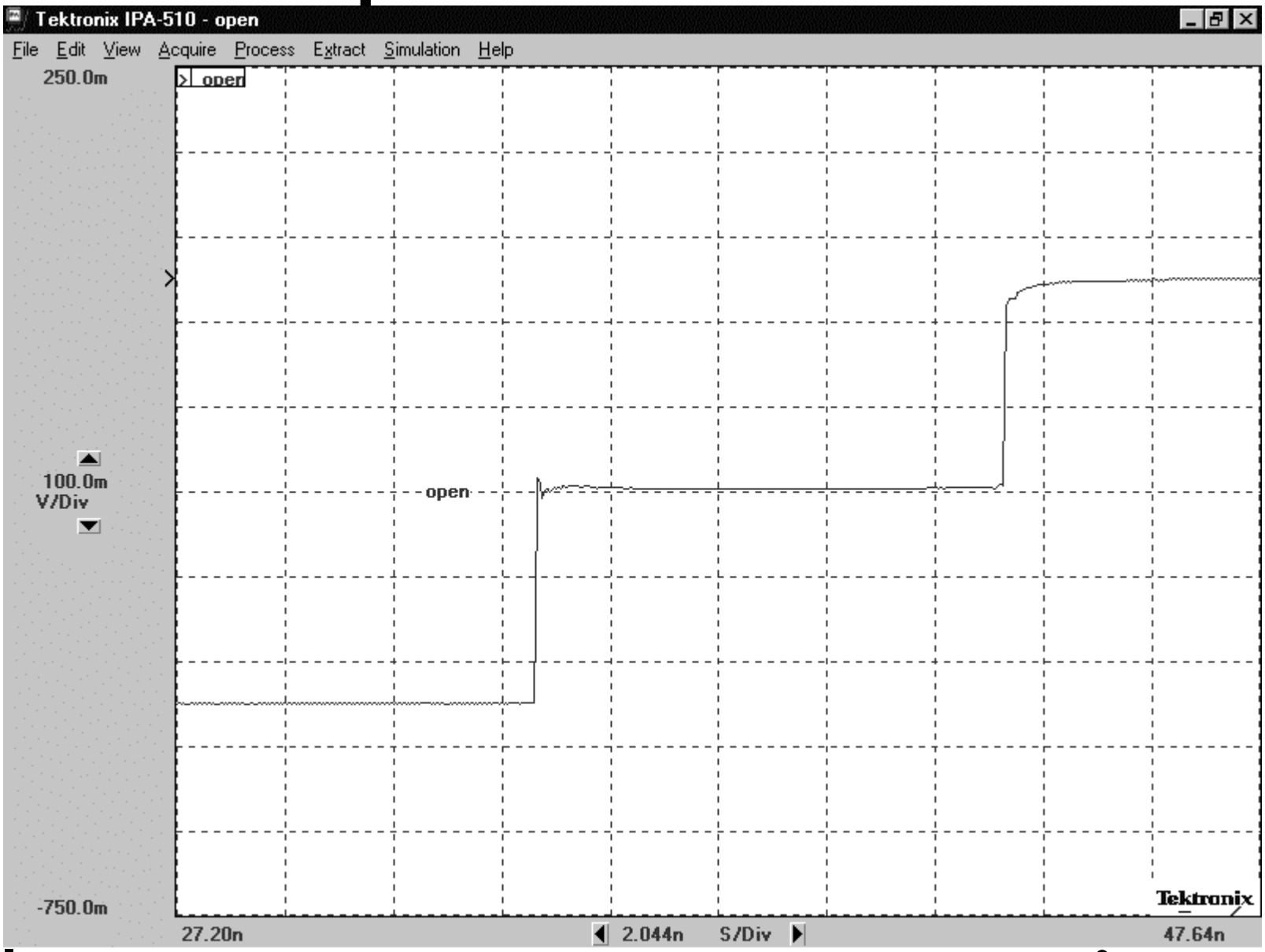
TDR Basics

- High-edge rate pulse transmitted to DUT
- DUT reflects wave
- Reflected wave measured by scope
- Impedance of DUT determines reflected voltage amplitude
- Scope and/or software calculates impedance based on reflected wave amplitude
  - PLOT OF TDR OF SHORT/OPEN/50 OHM
- Propagation delay can also be measured

TDR of 50 Ohm Load



TDR of Open


Tektronix IPA-510 - open
File Edit View Acquire Process Extract Simulation Help
250.0m
open
100.0m
V/Div
open
-750.0m
Tektronix
27.20n
2.044n S/Div
47.64n

TDR Test Equipment

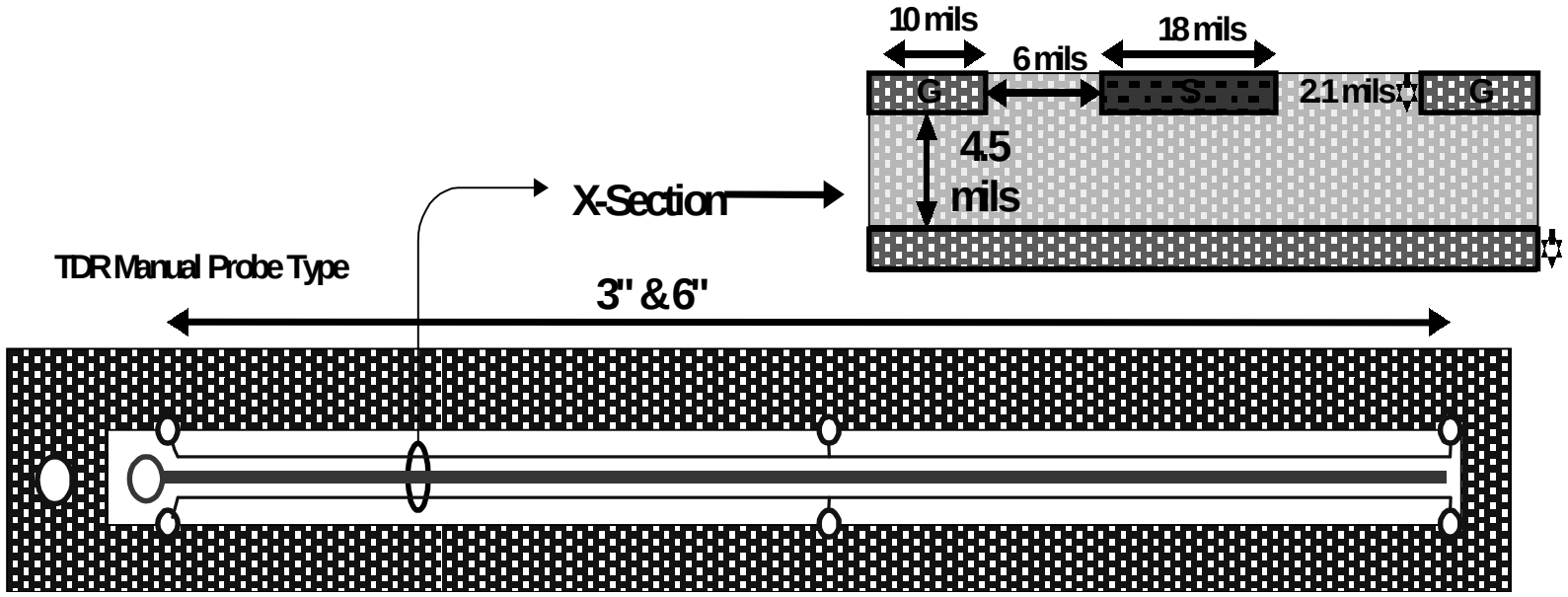
- Tektronix 11801C
  - using SD24 TDR test head
- HP54750A
  - HP54753A Single Ended TDR
  - HP54754A Differential TDR
- Polar CITS500S

Test Coupon

- Use test coupon for ease of testing
  - Gerbers for an example coupon are available
- Test coupon placement
  - Coupon can be designed as part of motherboard
  - Ideally located in memory section of board
  - Or have separate coupon somewhere on panel
- Test coupon probe pattern
  - Pattern depends on test equipment and probes
  - Land pattern must match test probe used

GND

Test Coupon



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Test Coupon Design

- Test coupon routing should match routing guidelines for RDRAM bus
  - Follow trace to trace spacing rules
  - Ground shields required to control etch and reduce coupling
  - Ground traces will affect trace impedance, so they must be included in test coupon
- Signal trace routing
  - Route straight (no bends) for best results
  - End of trace should be open - no pad or via
- Ground pads required for probing
  - Microstip - Signal and ground pad
  - Stripline - Signal and pad for each reference plane

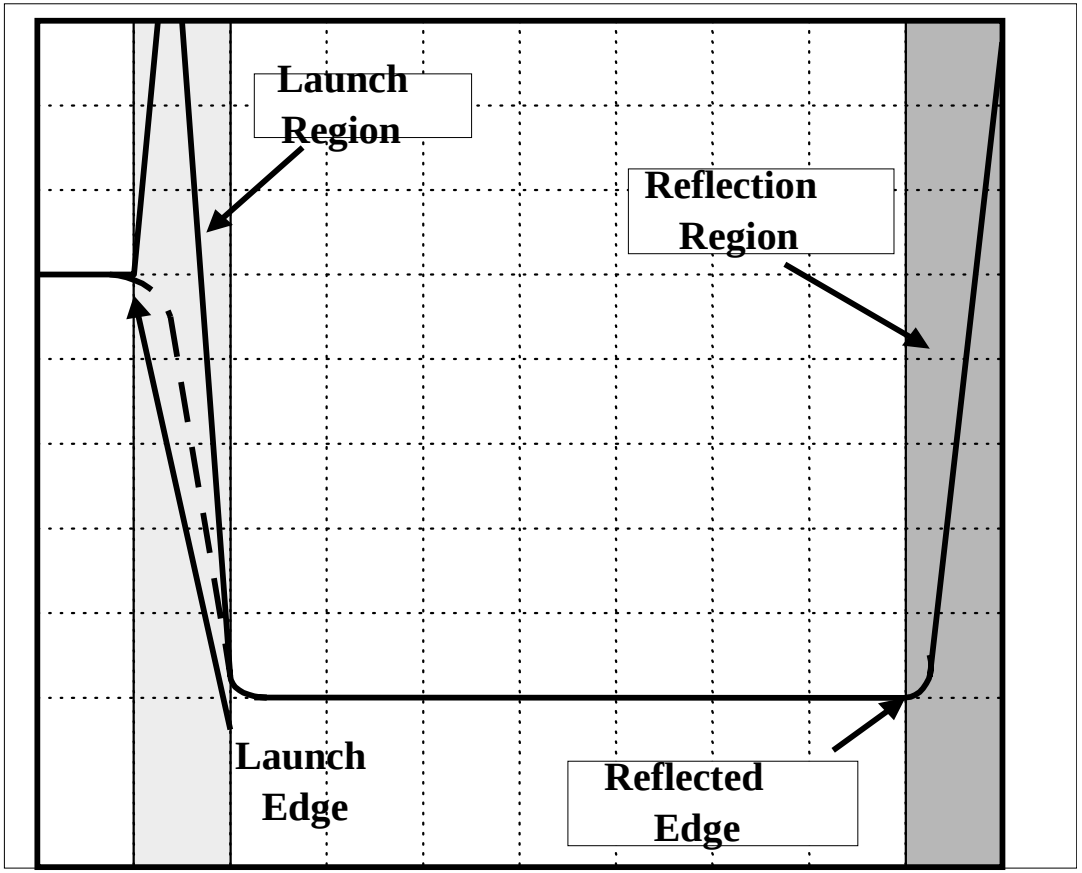
Test Procedure

- Equipment calibration is critical
  - Careful calibration is required for accurate results
  - Procedure is defined in TDR Methodology Doc
  - 28 Ohm standard should be used to verify test setup
- Probing techniques
  - Standard high-frequency probes are acceptable
  - Discontinuity at probe tip must be minimized
    - Minimize ground lead length
    - Probe ground pad should be near signal pad
- Reading the data
  - Impedance will vary along transmission line
  - Ringing will also affect measurement
    - (Beginning (near probe) of line will have more error

TDR Measurement

Maximize the display

- **Display Adjustment:**
  - **Line launch pt on first column.**
  - **Reflection on last column**
  - **Utilize vertical scaling to maximize screen**



Proper display adjustment is important

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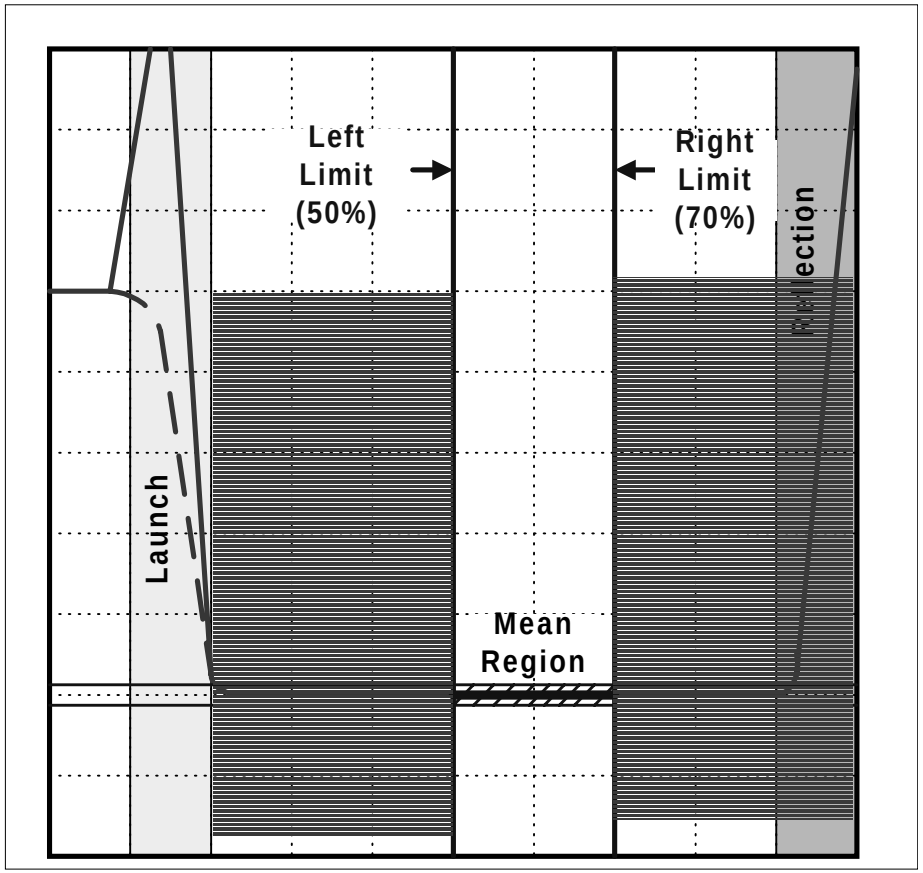
TDR Measurement

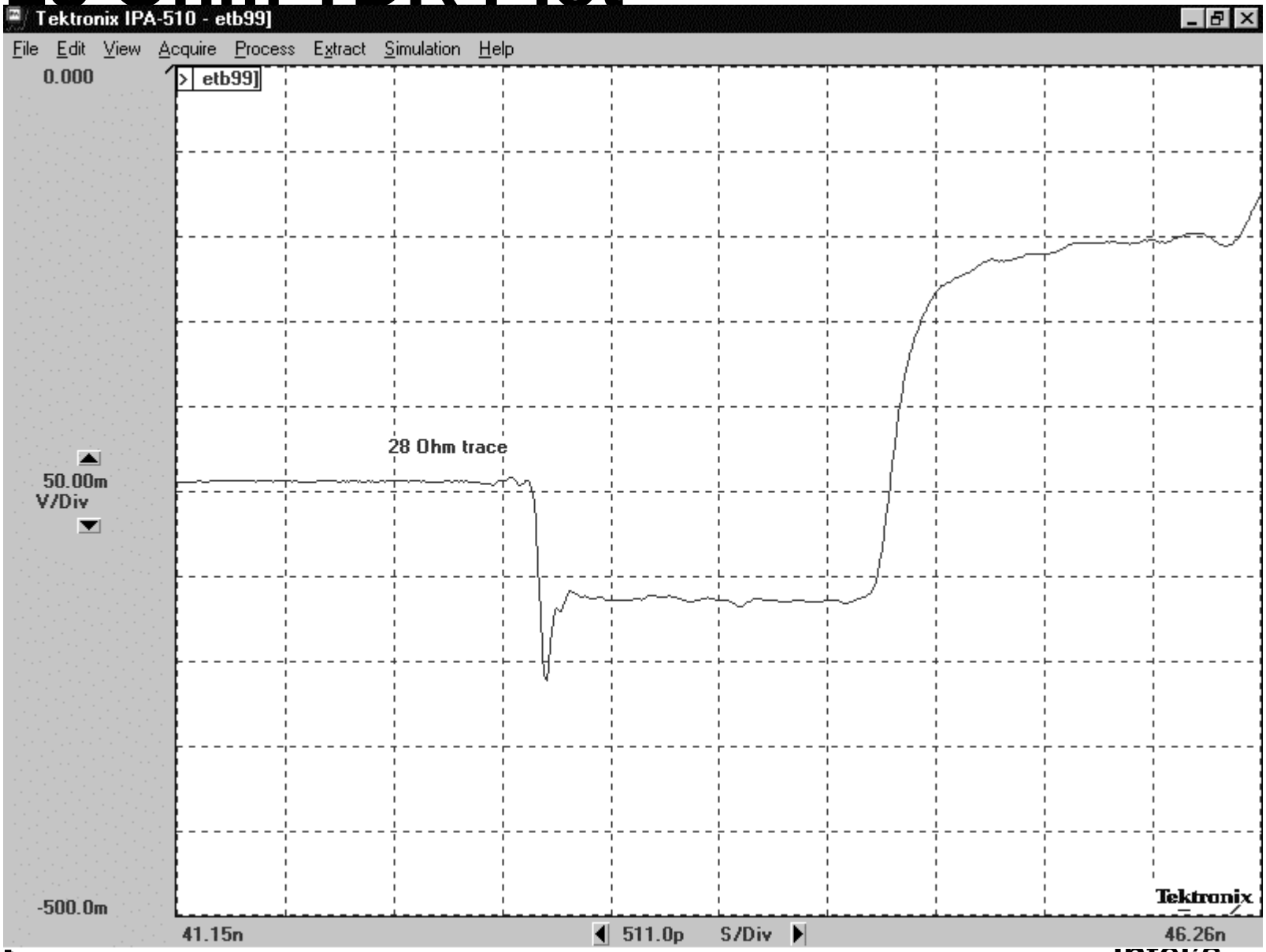
Measure the average mean

- **Measure the response correctly:**
  - **Region should be after midpoint slightly before reflection region**
  - **Take average impedance of the mean region**



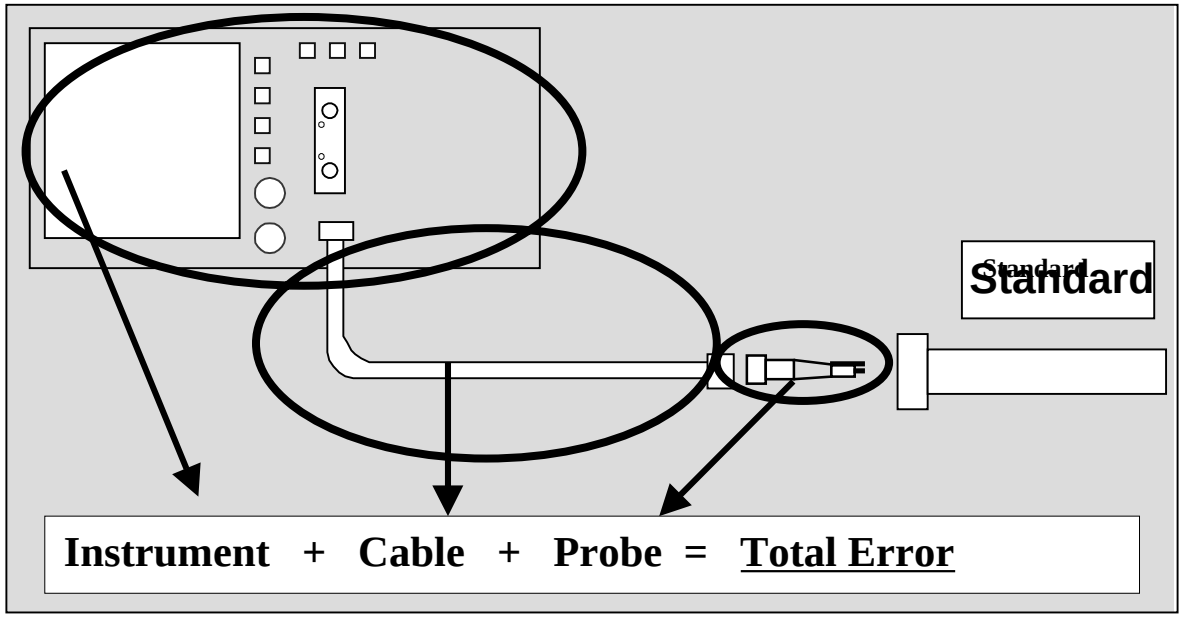
- **Measure the right region and take average**

28 Ohm TDR Plot



Rambus 28 Ω Measurement

Calibrate against a standard



- Determine equivalent error at probe tip

Standard can determine error

Rambus 28 Ω Measurement

Use error as an offset

- Compare standard value against measured value
  - ***Measure standard with cable connected***
- Use difference between measured and actual
- Shift spec window by that amount
- Example:
  - Calibrated value = 25 Ohms
  - Measured value = 27 Ohms
  - Difference = + 2 Ohms

Shift measurement window by error value

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Standards

Standard value must be close to spec

- **Option 1)*preferred**
  - **28 ohm airline**
    - 15 cm min length
- **Option 2)**
  - **Two 50 ohm airlines connected in parallel (25 Ohms)**
    - 15 cm min length

Airline standards provide best accuracy

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HVM Testing

- Test at 100% for early production
  - Avoid excursions on first production units
  - Use recommended TDR test probes
- Lot to Lot checks (sample)
  - Once stability of materials & process have been established
- Frequent calibration recommended
  - Use 28 Ohm calibration standard
  - Use Intel recommended calibration method for offset calculation
- Place coupon in middle of panel to minimize error
  - Or a minimum of 0.8” from edge of panel
- X-section data to check for process variations

Reference Collateral

Collateral	By	Available
PCB Test Methodology Doc	Intel	WWW
TDR Theory (AN 1304-2)	HP	WWW

URLs:

Company	URL
Intel Corporation	http://developer.intel.com/ial/home/sp/index.htm
Hewlett-Packard	www.tmo.hp.com/tmo/
Tektronix	www.tek.com/Measurement/scopes/
Polar	www.polar.co.uk

Summary and Conclusion

- Meeting 28 Ω +/-10% requirement is critical for a solid motherboard design
- Board and trace geometries can be calculated, or use reference design
- Material tolerances need to be analyzed using x-section measurements
- Test builds will be required to dial in process
- Accurate impedance measurements are required to verify design