Intel® 850 Chipset Family: 82850/82850E Memory Controller Hub (MCH)

Datasheet

October 2002

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Revision History

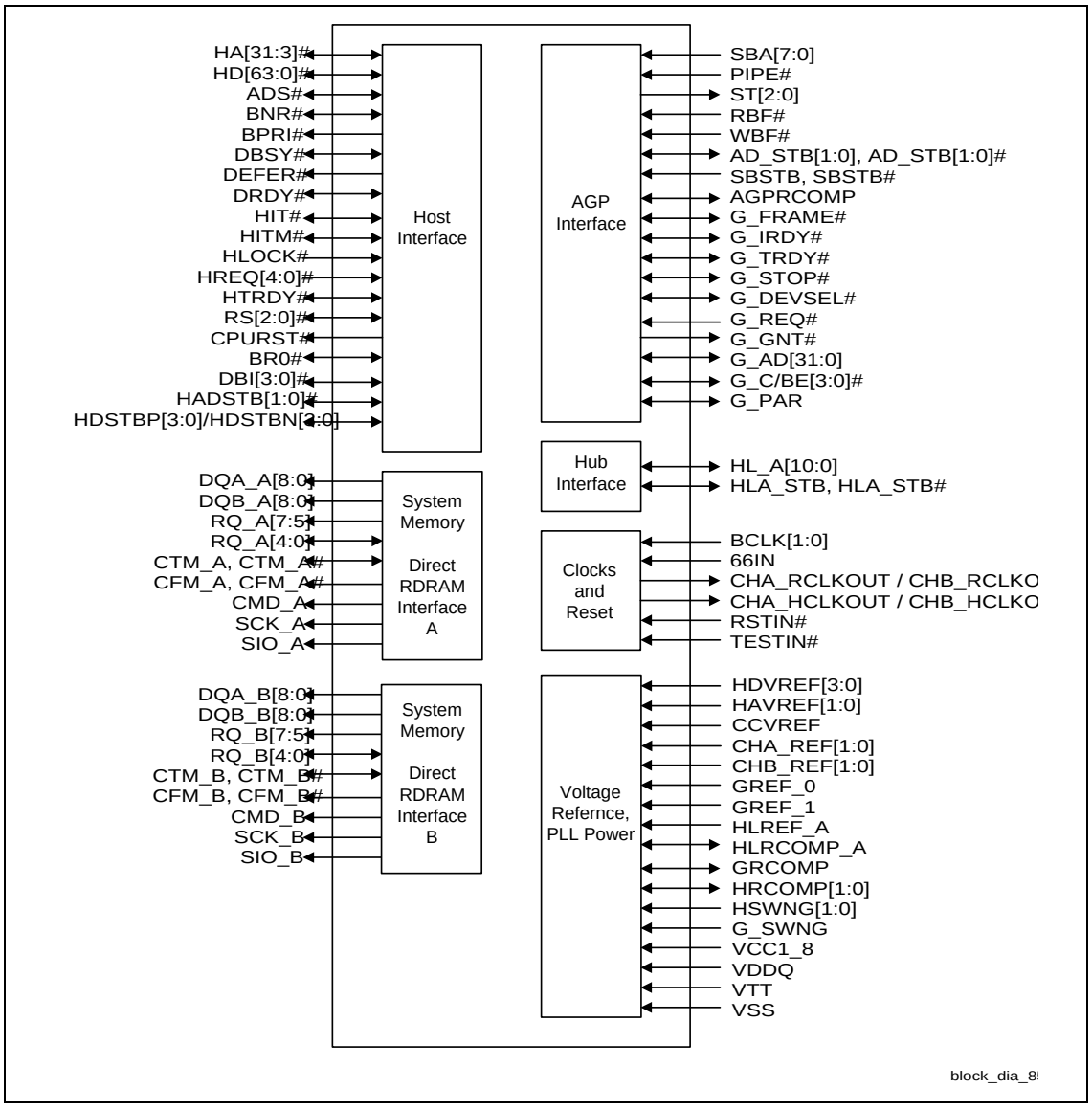
Rev.	Description	Date
-001	• Initial Release	November 2000
-002	• Renamed document title to 850 Chipset Family • Added 82850E MCH	May 2002
-003	• Added 1066 MHz RDRAM support for 82850E MCH	October 2002
-004	• Revised MCH Features	October 2002

Intel® 82850/82850E MCH Features

- Processor/Host Bus Support
  - Supports the Intel® Pentium® 4 processor in the 423 pin and 478-pin package
  - 2X Address, 4X Data
  - Pentium 4 processor system bus interrupt delivery
  - Intel® 82850 MCH supports Pentium 4 processor in the 423 or 478-pin package with a processor system bus of 100 MHz (400 MHz Data Bus)
  - Intel® 82850E MCH supports Pentium 4 processor in the 478 pin package with a processor system bus of 133 MHz (533 MHz Data Bus)
  - Supports system bus Dynamic Bus Inversion (DBI)
  - Supports 32-bit host bus addressing
  - 8 deep In-Order Queue
  - AGTL+ bus driver technology with integrated termination resistors
- Direct RDRAM Support
  - Directly supports two RDRAM Direct channels operating in lock-step.
  - 82850 MCH supports 300 MHz and 400 MHz RDRAM
  - 82850E MCH supports 400 MHz (PC800-40) and 533 MHz (PC1066-32) RDRAM
  - Maximum memory bandwidth 3.2 GB/s (82850 MCH), 4.2 GB/s (82850E MCH)
  - Supports 128-Mb, 256-Mb, and 288-Mb RDRAM densities
  - Supports up to 32 Direct RDRAM devices/channel for 300/400 MHz RDRAM, 24 devices/channel for 533 MHz RDRAM
  - Dual-Channel maximum memory array size is 1 GB using 128Mb RDRAM technology and up to 1.5 to 2 GB using 256Mb/288Mb RDRAM technology
  - Supports up to 8 simultaneous open pages; 1 KB page size for 128 Mb and 256 Mb RDRAM Devices; 2 KB page size for 256Mb/288Mb RDRAM Devices
  - Configurable optional ECC operation: ECC with single bit Error Correction and multiple bit Error Detection
- Hub Interface to ICH2
  - Private interconnect between MCH and I/O Controller Hub
- **Accelerated Graphics Port (AGP) Interface**
  - Supports a single AGP device (either via a connector or on the motherboard)
  - Supports AGP 2.0 including 4X AGP data transfers and 2X/4X fast write protocol
  - Supports only 1.5 V AGP signaling levels
  - 32 deep AGP request queue
  - AGP address translation mechanism with integrated fully associative 20 entry TLB
  - AGP semantic (PIPE# or SBA initiated) accesses to memory not snooped
  - PCI semantic (FRAME# initiated) accesses to memory are snooped
  - High priority access support
  - Hierarchical PCI configuration mechanism
  - Delayed transaction support for AGP-to-DRAM FRAME# semantic reads that can not be serviced immediately
  - 32-bit upstream address support for inbound AGP and PCI cycles
  - 32-bit downstream address support for outbound PCI and fast write cycles
- **System Interrupts**
  - Supports system bus interrupt delivery mechanism
- **Power Management**
  - SMRAM space remapping to A0000h (128 KB)
  - Supports extended SMRAM space above 256MB, additional 128K/256K/512K/1MB TSEG from Top of Memory, cacheable (cacheability controlled by Processor)
  - SMRAM accesses from AGP or hub interfaces are not allowed
  - ACPI Rev 1.0 compliant power management
  - APM Rev 1.2 compliant power management
- **Packaging**
  - 31x35mm 615 OLGA
- **I/O Device Support**
  - ICH2

The Intel® 82850 MCH / Intel® 82850E MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Simplified Block Diagram



1. Introduction

The Intel® 850 chipset family is a high-bandwidth chipset family designed for high-performance desktop and workstation platforms based on the Intel® Pentium® 4 processor. The chipset contains two main components—the Memory Controller Hub (MCH) and the I/O Controller Hub 2 (ICH2). The MCH provides the system bus interface, memory controller, AGP interface, and hub interface for I/O.

There are two chipsets in the 850 chipset family:

- Intel® 850 chipset: This chipset contains the 82850 (MCH) and the 82801BA (ICH2).
- Intel® 850E chipset: This chipset contains the 82850E (MCH) and the 82801BA (ICH2).

The difference between the 82850 MCH and the 82850E MCH is that the 82850 MCH supports a 400 MHz processor system bus, and the 82850E MCH supports either a 400 MHz or 533 MHz processor system bus. Additionally, the 82850 MCH supports 300 MHz or 400 MHz RDRAM, where the 82850E MCH supports 400 MHz or 533 MHz RDRAM.

This document describes the 82850 and 82850E Memory Controller Hubs (MCH). Section 1.3 *Intel® 850/850E Chipset System*, provides an overview of the components of the 850/850E chipset. Unless otherwise specified, references to the 850 chipset, 850 chipset system or MCH refer to both the 82850 MCH and 82850E MCH.

1.1. Related Documents

- *Intel® 82801BA I/O Controller Hub* (ICH2), Datasheet (Doc Ref: 290687)
- *Intel® 82802AB/AC Firmware Hub (FWH)*, Datasheet (Doc Ref: 290658)
- *Intel® Pentium 4 Processor in the 423 pin package / Intel® 850 Chipset* Design Guide (Doc Ref: 2098245
- *Intel® Pentium 4 Processor in the 478 pin package / Intel® 850 Chipset Family*, Design Guide (Doc Ref: 249888)
- *Intel® 850 Chipset: Thermal Considerations*, Application Note (AP-720) (Doc Ref: 292268)

1.2. Terminology

Term	Definition
MCH	The Memory Controller Hub component that contains the processor interface, DRAM controller, and AGP interface. It communicates with the I/O controller hub (ICH2) and other I/O controller hubs over proprietary interconnect called the hub interface.
Intel® ICH2	The I/O Controller Hub component that contains the primary PCI interface, LPC interface, USB, ATA-100, AC'97, and other I/O functions. It communicates with the MCH over a proprietary interconnect called "hub interface".
Host	This term is used synonymously with processor.
Core	The internal base logic in the MCH.
System Bus	Processor-to-MCH interface. The system bus runs at 400 MHz from a 100 MHz quad-pumped clock. It includes source synchronous transfers for address and data and system bus interrupt delivery enhancements.
Hub Interface	The proprietary hub interconnect that ties the MCH to the ICH2. In this document hub interface cycles originating from or destined for the primary PCI interface on the ICH2 is generally referred to as hub interface cycles.
Accelerated Graphics Port (AGP)	Refers to the AGP interface that is in the MCH. It supports AGP 2.0 compliant components only with 1.5 V signaling level. PIPE# and SBA addressing cycles and their associated data phases are generally referred to as AGP transactions. FRAME# cycles over the AGP bus are generally referred to as AGP/PCI transactions.
PCI_A	The physical PCI bus that is driven directly by the ICH2 component. It supports 5 V, 32-bit, 33 MHz PCI 2.2 compliant components. Communication between PCI_A and the MCH occurs over the hub interface. Note that even though it is referred to as PCI_A it is not PCI Bus 0 from a configuration standpoint.
RSL	RDRAM Signaling Level is the name of the signaling technology used by RDRAM.
RAC	RDRAM ASIC Cell. It is the embedded cell designed by Rambus* that interfaces with the RDRAM devices using RSL signaling. The RAC communicates to the RMC.
RMC	RDRAM Memory Controller. This is the logic that directly interfaces to the RAC.
Full Reset	A Full MCH Reset is defined in this document when RSTIN# is asserted.
GART	Graphics Aperture Re-map Table. Table in memory containing the page re-map information used during AGP aperture address translations.
GTLB	Graphics Translation Look-aside Buffer. A cache used to store frequently used GART entries.
UP	Uni-Processor
DBI	Dynamic Bus inversion
MSI	Message Signaled Interrupts. MSIs allow a device to request interrupt service via a standard Memory Write transaction instead of through a hardware signal.
IPI	Inter Processor Interrupt

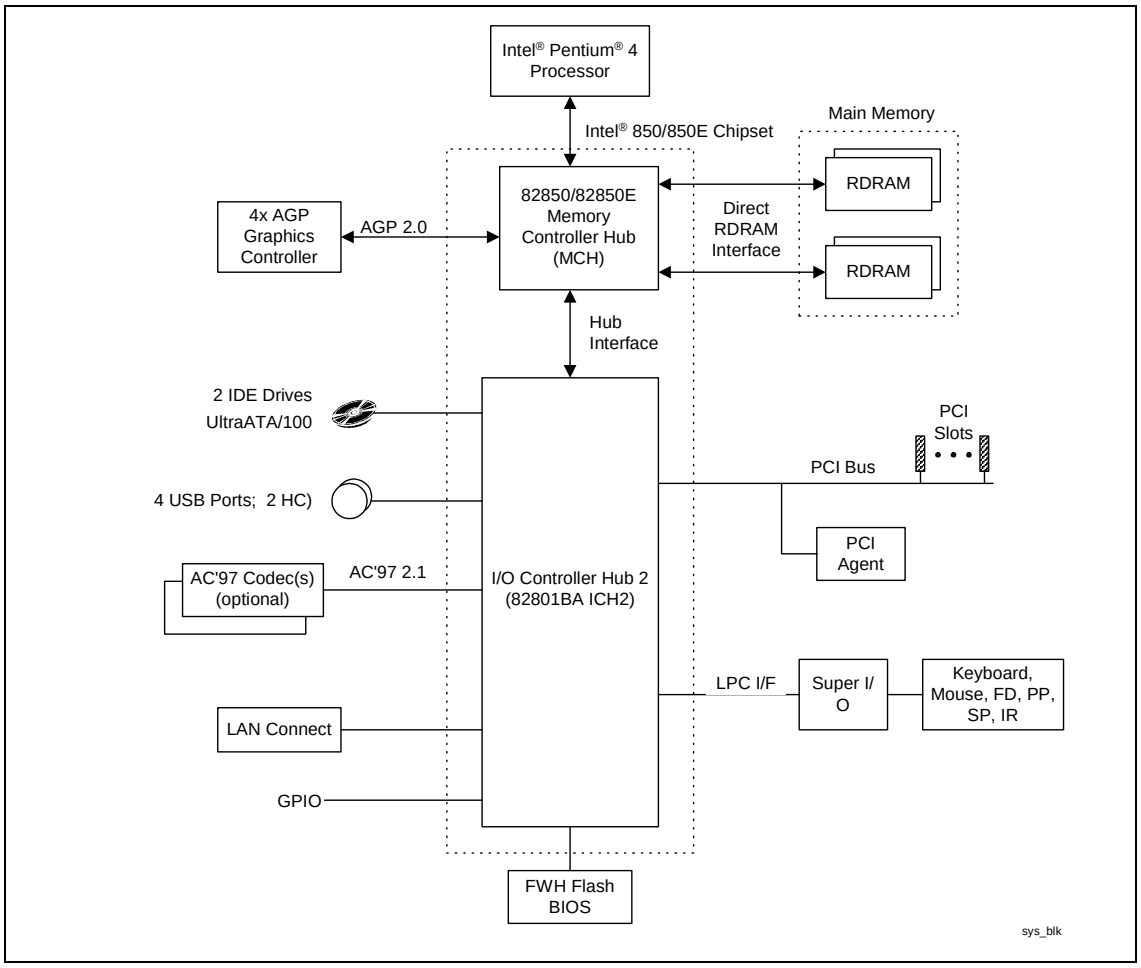
1.3. Intel® 850/850E Chipset Family System

Figure 1 shows a typical system block diagram based on the 850 chipset family. The 850 chipset uses a hub architecture with the MCH as the host bridge hub and the I/O Controller Hub as the I/O hub. The 82850 MCH supports a processor system bus frequency of 100 MHz (data bus quad-pumped to 400 MHz), and the 82850E MCH supports a processor system bus frequency of 133 MHz (data bus quad-pumped to 533 MHz) The I/O Controller Hub is highly integrated providing many of the functions needed in today's PC platforms; it also provides the interface to the PCI Bus. The MCH and I/O Controller Hub communicate over a dedicated hub interface.

82801BA ICH2 functions include:

- PCI Rev 2.2 compliant with support for 33 MHz PCI operations
- Supports up to 6 Req/Gnt pairs (PCI Slots)
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated IDE controller
  - Ultra ATA/100/66/33
- USB host interface
  - 2 host controllers
  - Supports 4 USB ports
- Integrated LAN controller
- System Management Bus (SMBus) compatible with most I^2C devices
  - ICH2 has both bus master and slave capability
- AC'97 2.1 compliant link for audio and telephony codecs
  - Up to 6 channels
- Low Pin Count (LPC) interface
- FWH Interface (FWH Flash BIOS support)
- Alert on LAN*
  - AOL and AOL2

Figure 1. Intel® 82850/82850E MCH Desktop System Block Diagram



1.4. Intel® 82850/82850E MCH Overview

The MCH provides the processor interface, memory interface, AGP interface, and hub interface in an 850/850E chipset platform. The MCH supports two channels of Direct RDRAM operating in lock-step. It also supports 4X AGP data transfers and 2X/4X AGP fast writes.

Intel® Pentium® 4 Processor Host Interface

The MCH is optimized for the Pentium 4 processor. The primary host-interface enhancements are:

- Source synchronous double pumped address
- Source synchronous quad pumped data
- System bus interrupt delivery

The MCH supports a 64-B cache line size. The 82850 MCH supports one processor at a system bus frequency of 100 MHz (400 MHz Data Bus) or a 1:1 Host-to-RDRAM frequency ratio (400 MHz data bus to 400 MHz RDRAM). The 82850E MCH supports one processor at a system bus frequency of 133 MHz (533 MHz Data Bus), with either a 4:3 Host-to-RDRAM frequency ratio (533 MHz data bus to 400 MHz RDRAM) or a 1:1 Host-to-RDRAM frequency ratio (533 MHz data bus to 533 MHz (PC1066)

RDRAM). The MCH integrates AGTL+ termination resistors on all of the AGTL+ signals. The MCH supports 32-bit host addressing, allowing the processor to access the entire 4 GB of the MCH's memory address space. The MCH has an 8-deep In-Order Queue to support up to eight outstanding pipelined address requests on the host bus. Host initiated I/O cycles are positively decoded to AGP or MCH configuration space. Host-initiated I/O cycles are subtractively decoded to the hub interface. Host-initiated memory cycles are positively decoded to AGP or RDRAM and are again subtractively decoded to the hub interface. AGP semantic memory accesses initiated from AGP to DRAM are not snooped on the host bus. Memory accesses initiated from AGP using PCI semantics and from the hub interface to DRAM are snooped on the system bus. Memory accesses whose addresses lie within the AGP aperture are translated using the AGP address translation table, regardless of the originating interface.

RDRAM Interface

The MCH directly supports two channels of Direct RDRAM memory operating in lock-step using RSL technology. The MCH RDRAM channels run at 300 MHz, 400 MHz and 533 MHz and support 128-Mb and 256-/288-Mb technology RDRAM Direct devices. These 128-Mb and 256-/288-Mb RDRAMs use page sizes of 1 KB, while 256-/288-Mb devices may also be configured to use 2 KB pages. For 82850 MCH and 82850E MCH PC800 RDRAM a maximum of 64 RDRAM devices are supported on the paired channels without external logic. For 82850E MCH PC1066 RDRAM a maximum of 24 RDRAM devices are supported on the paired channels. The following tables show the maximum RDRAM array size and the minimum increment size for the various RDRAM densities supported.

Table 1. RDRAM* Densities Supported

MCH Stepping	Device Tech	Device Qantity	No. of Banks	Page Size
A2, A3	128/144 Mbit	4,8,16	16d	1 KB
A2, A3	128/144 Mbit	4,8,16	2x16d	1 KB
A3	288 Mbit	4,8,16	16d	2 KB
A3	256/288 Mbit	2,4,8,16	2x16d	2 KB
A3	256/288 Mbit	4,8,16	32s	2 KB

Table 2. Maximum RDRAM* Array Size, Minimum Increment Size

RDRAM* Technology	Directly Supported		
	Increments	Maximum 400 MHz RDRAM	Maximum 533 MHz RDRAM
128 Mb	32 MB	1 GB	1 GB
256/288 Mb	64 MB	2 GB	1.5 GB

Table 3. RDRAM* Platform Configuration and Support

Topic	Intel® 82850 MCH			Intel® 82850E MCH	
System Bus (MHz)	400	400		533	
RDRAM (MHz)	300	400	400	400	533
RDRAM Type	PC600-40	PC800-40	PC800-45	PC800-40	PC1066-32
tRCD (clks)	7	7	9	7	9
tCAC (clks)	8	8	8	8	8
Register 50h, bit 11	0	1	1	0	1
Register BEh, bits [7:6]	01	01	10	01	10

The MCH provides optional ECC error checking for RDRAM data integrity. During DRAM writes, ECC is generated on a QWord (64-bit) basis. During RDRAM reads and the read of the data that underlies partial writes, the MCH supports detection of single-bit and multiple-bit errors, and will correct single bit errors when correction is enabled.

C-RIMM Placement Requirement:

- For 82850E/533 MHz RDRAM, if a C-RIMM is used, it must be placed in the #2 RIMM slot only – never in the #1 RIMM slot.

AGP Interface

A single AGP component or connector (not both) is supported by the MCH's AGP interface.

The AGP interface supports 1X/2X/4X AGP signaling and 2X/4X fast writes. AGP semantic cycles to DRAM are not snooped on the host bus. PCI semantic cycles to DRAM are snooped on the host bus. The MCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. Both upstream and downstream addressing is limited to 32-bit for AGP and AGP/PCI transactions. The MCH contains a 32-deep AGP requests queue. High priority accesses are supported. All accesses from the AGP interface that fall within the graphics aperture address range pass through an address translation mechanism with a fully associative 20 entry TLB. Accesses between AGP and the hub interface are limited to memory writes originating from the hub interface destined for the AGP bus.

The AGP interface is clocked from a dedicated 66 MHz clock (66IN). The AGP-to-host/core interface is asynchronous.

The AGP buffers operate only in 1.5 V mode. They are not 3.3 V safe.

Hub Interface

The 8-bit hub interface connects the MCH to the ICH2. Most communications between the MCH and the ICH2 occurs over this interface. The hub interface runs at 66 MHz / 266 MB/s.

The hub interface's supported traffic types include hub interface -to- AGP memory writes, hub interface-to-DRAM, processor-to-hub interface, Messaging (MSI Interrupt messages, Power Management state change, MI, SCI, and SERR error indication). In addition to these traffic types, the hub interface also supports, Interrupt related messages, Power management events as messages, and SMI, SCI, and SERR error indication messages.

It is assumed that the hub interface is always connected to an ICH2.

MCH Clocking

The MCH has the following clock input pins:

- Differential BCLK0/BCLK1 for the host interface
- 66 MHz clock input for the AGP and hub interface
- Differential CTM/CTM# and CFM/CFM# for each of the two RACs.

Clock synthesizer chip(s) are responsible for generating the system host clocks, AGP, and hub interface clocks, PCI clocks, and RDRAM clocks. The MCH provides two pairs of feedback signals to the Direct Rambus* Clock Generator (DRCG) chips to keep the host and RDRAM clocks aligned. The host speed is 100 MHz (82850 MCH) or 133 MHz (82850E MCH). The RDRAM speed is 300 MHz or 400 MHz for the 82850 MCH, and 400 MHz or 533 MHz for the 82850E MCH. The MCH does not require any relationship between the BCLK host clock and the 66 MHz clock generated for AGP and hub interfaces; they are totally asynchronous from each other. The AGP and hub interface run at a constant 66 MHz base frequency. The hub interface runs at 4X. AGP transfers may be 1X/2X/4X.

Table 4 indicates the frequency ratios between the various interfaces the MCH supports.

Table 4. MCH Processor-to-AGP/Hub Interface Relationship

AGP/Hub Interface Unit Frequency (MHz)	Intel® Pentium® 4 Processor 100 MHz (400 MHz Data Bus)
AGP: 66 MHz	Asynchronous
Hub Interface: 66 MHz	Asynchronous

System Interrupts

The MCH supports both 8259 and Pentium 4 processor system bus interrupt delivery mechanisms. The serial APIC bus interrupt mechanism is not supported. The 8259 support consists of flushing inbound hub interface write buffers when an Interrupt Acknowledge cycle is forwarded from the system bus to the hub interface.

The Pentium 4 processor and MCH support a new system bus interrupt delivery mechanism. IOxAPIC and PCI MSI interrupts are generated as memory writes. The MCH decodes upstream memory writes to the range 0FEE0_0000h–0FEEF_FFFFh from the hub interface as messaged-based interrupts. The MCH forwards these memory writes, along with the associated write data, to the system bus as an Interrupt Message transaction. Note that since this address does not decode as part of main memory, the write cycle and the write data does not get forwarded to DRAM via the write buffer. The MCH provides the response and TRDY# for all Interrupt Message cycles including the ones originating from the MCH. The MCH supports interrupt re-direction for inter-processor interrupts (IPIs) as well as upstream interrupt memory writes.

For message-based interrupts, system write-buffer coherency is maintained by relying on strict ordering of memory writes. The MCH ensures that all memory writes received from a given interface prior to an interrupt message memory write are delivered to the system bus for snooping in the same order that they occur on the given interface.

Powerdown Flow

Since the MCH will be powered down during STR, the MCH cannot maintain any state information when exiting STR. This means that the entire initialization process when exiting STR must be performed by the BIOS via accesses to the RICM register.

Entry into STR (ACPI S3) is initiated by the Operating System (OS) based on detecting a lack of system activity. The OS unloads all system device drivers as part of the process of entering STR. The OS then writes to the PM1_CNT I/O register in the ICH2 to actually trigger the transition into STR. The ICH2 will respond by eventually generating the Go C3 message to the MCH via the hub interface.

2. Signal Description

This section provides a detailed description of MCH signals. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during reset are provided in the Pin States During Reset section of this chapter.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin
s/t/s	Sustained Tri-state. This pin is driven to its inactive state prior to tri-stating.
As/t/s	Active Sustained Tri-state. This applies to some of the hub interface signals. This pin is weakly driven to its last driven value.

The signal description also includes the type of buffer used for the particular signal:

AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The MCH integrates AGTL+ termination resistors.
AGP	AGP interface signals. These signals are compatible with AGP 2.0, 1.5 V Signaling Environment DC and AC Specifications. The buffers are not 3.3 V tolerant.
CMOS	CMOS buffers.
RSL	RDRAM Signaling Level interface signal. Refer to the RDRAM Direct Specification for complete details

Note that system address and data bus signals are logically inverted signals. Thus, the actual values are inverted from what appears on the system bus. All processor control signals follow normal convention. A 0 indicates an active level (low voltage) if the signal is followed by # symbol and a 1 indicates an active level (high voltage) if the signal has no # suffix.

2.1. Host Interface Signals

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the system bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The MCH is the only priority agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions, unless the HLOCK# signal was asserted.
BR0#	I/O AGTL+	**Bus Request 0:** The MCH pulls the processor bus BR0# signal low during CPURST#. The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. BR0# should be tri-stated after the hold time requirement has been satisfied.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the MCH. The MCH asserts CPURST# while RSTIN# (PCIRST# from ICH2) is asserted and for approximately 1 ms after RSTIN# is deasserted. The CPURST# allows the processor to begin execution in a known state. Note that the ICH2 must provide processor frequency select strap setup and hold times around CPURST#. This requires strict synchronization between MCH CPURST# deassertion and ICH2 driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEEFER#	O AGTL+	**Defer:** This signal indicates that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
DBI[3:0]#	I/O AGTL+ 4X	**Dynamic Bus Inversion:** These signals are driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DBI[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DBI[x]# — Data Bits** DBI3# — HD[63:48]# DBI2# — HD[47:32]# DBI1# — HD[31:16]# DBI0# — HD[15:0]#
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+ 2X	**Host Address Bus:** HA[31:3]# connect to the system address bus. During processor cycles, HA[31:3]# are inputs. The MCH drives HA[31:3]# during snoop cycles on behalf of hub interface and AGP/Secondary PCI initiators. HA[31:3]# are transferred at 2X rate. Note that the address is inverted on the system bus. **Note:** After reset, the value on HA[7]# is sampled by all system bus agents, including the MCH on the rising edge of CPURST#. Its latched value determines the maximum IOQ depth mode supported on the system bus. If HA[7] is sampled low, the IOQ depth on the bus is one. If HA[7]# is sampled high, the IOQ depth on the bus is the maximum of 12. When the IOQ depth on the bus is set to 12, the MCH limits the number of queued transactions by asserting BNR# since the MCH has an IOQ of depth 8.

Signal Name	Type	Description
HADSTB[1:0]#	I/O AGTL+ 2X	**Host Address Strobe:** The source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at the 2X transfer rate. **Strobe** **Address Bits** HADSTB0# HA[16:3]#, HREQ[4:0]# HADSTB1# HA[31:17]#
HD[63:0]#	I/O AGTL+ 4X	**Host Data:** These signals are connected to the system data bus. In Enhanced Mode HD[63:0]# are transferred at 4X rate. Note that the data signals are inverted on the system bus.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+ 4X	**Differential Host Data Strobes:** The differential source synchronous strobes used to transfer HD[63:0]# and DBI[3:0]# at the 4X transfer rate. **Strobe** **Data Bits** HDSTBP3#, HDSTBN3# HD[63:48]#, DBI3# HDSTBP2#, HDSTBN2# HD[47:32]#, DBI2# HDSTBP1#, HDSTBN1# HD[31:16]#, DBI1# HDSTBP0#, HDSTBN0# HD[15:0]#, DBI0#
HIT#	I/O AGTL+	**Hit:** HIT# indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I AGTL+	**Host Lock:** All system bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e., *no hub interface or AGP snoopable access* to DRAM are allowed when HLOCK# is asserted by the processor).
HREQ[4:0]#	I/O AGTL+ 2X	**Host Request Command:** These signals define the attributes of the request. In Enhanced Mode HREQ[4:0]# are transferred at 2X rate. They are asserted by the requesting agent during both halves of the request phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** These signals indicates type of response according to the following the table: 000 = Idle state 001 = Retry response 010 = Deferred response 011 = Reserved (not driven by MCH) 100 = Hard Failure (not driven by MCH) 101 = No data response 110 = Implicit Write back 111 = Normal data response

2.2. Direct RDRAM* Interface A

Signal Name	Type	Description
DQA_A[8:0]	I/O RSL	**RDRAM Data (A):** Data signals used for read and write operations on RDRAM channel A.
DQB_A[8:0]	I/O RSL	**RDRAM Data (A):** Data signals used for read and write operations on RDRAM channel A.
RQ_A[7:5]	O RSL	**Row Access Control (A):** Three request package pins containing control and address information for row accesses. Note: RQ_A[7:5] are sometimes referred to as the “ROW_A[2:0]” signals.
RQ_A[4:0]	O RSL	**Column Access Control (A):** Five request package pins containing control and address information for column accesses. Note: RQ_A[4:0] are sometimes referred to as the “COL_A[4:0]” signals.
CTM_A	I RSL	**Clock To Master (A):** One of the two differential transmit clock signals used for RDRAM operations on RDRAM channel A. It is an input to the MCH and is generated from an external clock synthesizer.
CTM_A#	I RSL	**Clock To Master Compliment (A):** One of the two differential transmit clock signals used for RDRAM operations on RDRAM channel A. It is an input to the MCH and is generated from an external clock synthesizer.
CFM_A	O RSL	**Clock From Master (A):** One of the two differential receive clock signals used for RDRAM operations on RDRAM channel A. It is an output from the MCH.
CFM_A#	O RSL	**Clock From Master Compliment (A):** One of the two differential receive clock signals used for RDRAM operations on RDRAM channel A. It is an output from the MCH.
CMD_A	O CMOS	**Command (A):** Command output to the RDRAM devices used for power mode control, configuring the SIO daisy chain, and framing SIO operations.
SCK_A	O CMOS	**Serial Clock (A):** This signal provides clocking for register accesses and selects RDRAM channel A devices for power management.
SIO_A	I/O CMOS	**Serial Input/Output (A):** Bi-directional serial data signal used for device initialization, register operations, power mode control, and device reset.

2.3. Direct RDRAM* Interface B

Signal Name	Type	Description
DQA_B[8:0]	I/O RSL	**RDRAM Data (B):** Data signals used for read and write operations on RDRAM channel B.
DQB_B[8:0]	I/O RSL	**RDRAM Data (B):** Data signals used for read and write operations on RDRAM channel B.
RQ_B[7:5]	O RSL	**Row Access Control (B):** Three request package pins containing control and address information for row accesses. Note: RQ_B[7:5] are sometimes referred to as the “ROW_B[2:0]” signals.
RQ_B[4:0]	O RSL	**Column Access Control (B):** Five request package pins containing control and address information for column accesses. Note: RQ_B[4:0] are sometimes referred to as the “COL_B[4:0]” signals.
CTM_B	I RSL	**Clock To Master (B):** One of the two differential transmit clock signals used for RDRAM operations on RDRAM channel B. It is an input to the MCH and is generated from an external clock synthesizer.
CTM_B#	I RSL	**Clock To Master Compliment (B):** One of the two differential transmit clock signals used for RDRAM operations on RDRAM channel B. It is an input to the MCH and is generated from an external clock synthesizer.
CFM_B	O RSL	**Clock From Master (B):** One of the two differential receive clock signals used for RDRAM operations on RDRAM channel B. It is an output from the MCH.
CFM_B#	O RSL	**Clock From Master Compliment (B):** One of the two differential receive clock signals used for RDRAM operations on RDRAM channel B. It is an output from the MCH.
CMD_B	O CMOS	**Command (B):** Command output to the RDRAM devices used for power mode control, configuring the SIO daisy chain, and framing SIO operations.
SCK_B	O CMOS	**Serial Clock (B):** This signal provides clocking for register accesses and selects RDRAM channel B devices for power management.
SIO_B	I/O CMOS	**Serial Input/Output (B):** Bi-directional serial data signal used for device initialization, register operations, power mode control, and device reset.

2.4. Hub Interface Signals

Signal Name	Type	Description
HL_A[10:0]	I/O CMOS	**Hub Interface Signals:** Signals used for the hub interface.
HLA_STB	I/O CMOS	**Hub Interface Strobe:** One of two differential strobe signals used to transmit or receive packet data over the hub interface.
HLA_STB#	I/O CMOS	**Hub Interface Strobe Compliment:** One of two differential strobe signals used to transmit or receive packet data over the hub interface.

2.5. AGP Interface Signals

2.5.1. AGP Addressing Signals

Signal Name	Type	Description
PIPE#	I AGP	**Pipeline.** **During PIPE# Operation:** This signal is asserted by the AGP master to indicate a full width address is to be enqueued on by the target using the AD bus. One address is placed in the AGP request queue on each rising clock edge while PIPE# is asserted. When PIPE# is deasserted no new requests are queued across the AD bus. **During SBA Operation:** Not used. **During FRAME# Operation:** Not used. **Note:** Initial AGP designs may not use PIPE# (i.e., PCI only 66 MHz). Therefore, an 8 kΩ pull-up resistor connected to this pin is required on the motherboard.
SBA[7:0]	I AGP	**Side-band Addressing** **During PIPE# Operation:** Not used. **During SBA Operation:** These signals are used by the AGP master (graphics component) to place addresses into the AGP request queue. The SBA bus and AD bus operate independently. That is, transaction can proceed on the SBA bus and the AD bus simultaneously. **During FRAME# Operation:** Not used. **Note:** These signals implement internal pull-ups to a nominal value of 8 kΩ.

NOTES: The above table contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. The master may not switch methods without a full reset of the system. When PIPE# is used to queue addresses the master is not allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master continues to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism but rather a static decision when the device is first being configured after reset.

2.5.2. AGP Flow Control Signals

Signal Name	Type	Description
RBF#	I AGP	**Read Buffer Full.** **During PIPE# and SBA Operation:** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted, the MCH is not allowed to initiate the return low priority read data. That is, the MCH can finish returning the data for the request currently being serviced; however, it cannot begin returning data for the next request. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data, then it is not required to implement this signal. **During FRAME# Operation:** Not used.
WBF#	I AGP	**Write-Buffer Full.** **During PIPE# and SBA Operation:** WBF# indicates if the master is ready to accept fast write data from the MCH. When WBF# is asserted, the MCH is not allowed to drive fast write data to the AGP master. WBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data, then it is not required to implement this signal. **During FRAME# Operation:** Not used.

2.5.3. AGP Status Signals

Signal Name	Type	Description
ST[2:0]	O AGP	**Status Bus.** **During PIPE# and SBA Operation:** ST[2:0] provide information from the arbiter to an AGP Master on what it may do. ST[2:0] only have meaning to the master when its GNT# is asserted. When GNT# is deasserted, these signals have no meaning and must be ignored. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings. **During FRAME# Operation:** These signals are not used during FRAME#-based operation; except that a 111 indicates that the master may begin a FRAME# transaction.

2.5.4. AGP Strobes

Signal Name	Type	Description
AD_STB0	I/O (s/t/s) AGP	**AD Bus Strobe-0.** **During 1X Operation:** Not used. **During 2X Operation:** During 2X operation, this signal provides timing for the AD[15:0] and C/BE[1:0]# signals. The agent that is providing the data drives this signal. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals.
AD_STB0#	I/O (s/t/s) AGP	**AD Bus Strobe-0 Compliment.** **During 1X Operation:** Not used. **During 2X Operation:** Not used. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals. The agent that is providing the data drives this signal.
AD_STB1	I/O (s/t/s) AGP	**AD Bus Strobe-1.** **During 1X Operation:** Not used. **During 2X Operation:** During 2X operation, this signal provides timing for the AD[16:31] and C/BE[2:3]# signals. The agent that is providing the data drives this signal. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the AD[16:31] and C/BE[2:3]# signals. The agent that is providing the data drives this signal.
AD_STB1#	I/O (s/t/s) AGP	**AD Bus Strobe-1 Compliment.** **During 1X Operation:** Not used. **During 2X Operation:** Not used. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the AD[16:31] and C/BE[2:3]# signals. The agent that is providing the data drives this signal.
SB_STB	I AGP	**SBA Bus Strobe** **During 1X Operation:** Not used. **During 2X Operation:** During 2X operation, this signal provides timing for the SBA bus signals. The agent that is driving the SBA bus drives this signal. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the SBA bus signals. The agent that is driving the SBA bus drives this signal.
SB_STB#	I AGP	**SBA Bus Strobe Compliment.** **During 1X Operation:** Not used. **During 2X Operation:** Not used. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the SBA bus signals. The agent that is driving the SBA bus will drive this signal.

2.5.5. AGP/PCI Signals-Semantics

For transactions on the AGP interface carried using AGP FRAME# protocol, these signals operate similar to their semantics in the PCI 2.1 specification the exact role of all AGP FRAME# signals are defined below.

Signal Name	Type	Description
G_FRAME#	I/O s/t/s AGP	**FRAME.** **During PIPE# and SBA Operation:** G_FRAME# is not used by AGP SBA and PIPE#, but used during AGP FRAME#. **During Fast Write Operation:** G_FRAME# is used to frame transactions as an output from the MCH during fast writes. **During FRAME# Operation:** G_FRAME# is an output when the MCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the MCH to indicate the beginning and duration of an access. G_FRAME# is an input when the MCH acts as a FRAME- based AGP target. As a FRAME#-based AGP target, the MCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
G_IRDY#	I/O s/t/s AGP	**Initiator Ready.** **During PIPE# and SBA Operation:** G_IRDY# is not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when MCH acts as a FRAME#-based AGP initiator and an input when the MCH acts as a FRAME#-based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** G_IRDY# indicates the AGP compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait-states. The master is never allowed to insert a wait-state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait-states after each 32- byte block is transferred.
G_TRDY#	I/O s/t/s AGP	**Target Ready.** **During PIPE# and SBA Operation:** G_TRDY# is not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the MCH acts as an AGP initiator and an output when the MCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** G_TRDY# indicates the AGP compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait-states after each block (32 bytes) is transferred on write transactions.
G_STOP#	I/O s/t/s AGP	**Stop.** **During PIPE# and SBA Operation:** Not used. **During FRAME# Operation:** STOP# is an input when the MCH acts as a FRAME#-based AGP initiator and an output when the MCH acts as a FRAME#-based AGP target. STOP# is used for disconnect, retry, and abort sequences on the AGP interface.

Signal Name	Type	Description
G_DEVSEL#	I/O s/t/s AGP	**Device Select.** **During PIPE# and SBA Operation:** Not used. **During FRAME# Operation:** DEVSEL#, when asserted, indicates that a FRAME# based AGP target device has decoded its address as the target of the current access. The MCH asserts DEVSEL# based on the DRAM address range being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected. **During Fast Write Operation:** G_DEVSEL# is used when the transaction cannot complete during the block data transfer
G_REQ#	I AGP	**Request.** **During SBA Operation:** Not used. **During PIPE# and FRAME# Operation:** REQ#, when asserted, indicates that a FRAME# or PIPE# based AGP master is requesting use of the AGP interface. This signal is an input to the MCH.
G_GNT#	O AGP	**Grant.** **During SBA, PIPE# and FRAME# Operation:** GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings. This signal requires an external pull-up of 8.2 kΩ.
G_AD[31:0]	I/O AGP	**Address/Data Bus.** **During PIPE# and FRAME# Operation:** AD[31:0] are used to transfer both address and data information on the AGP interface. **During SBA Operation:** AD[31:0] are used to transfer data on the AGP interface.
G_C/BE[3:0]#	I/O AGP	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the C/Bex# signals during FRAME#-based AGP are the same C/BE# command described in the PCI 2.1 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/Bex# signals carry command information. Refer to the *AGP 2.0 Interface Specification, Revision 2.0* for the definition of these commands. The command encoding used during PIPE# based AGP is **Different** than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** Not used.
G_PAR	I/O AGP	**Parity.** **During FRAME# Operation:** MCH is driven by the MCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the MCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#. **During SBA and PIPE# Operation:** Not used.

NOTES:

1. PCIRST# from the ICH2 is connected to RSTIN# and is used to reset AGP interface logic within the MCH. The AGP agent will also use PCIRST# provided by the ICH2 as an input to reset its internal logic.
2. The **LOCK#** signal is **Not Supported** on the AGP interface (even for PCI operations)
3. The **PERR#** signal is **Not Supported** on the AGP interface.

2.6. Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
BCLK[1:0]	I CMOS	**Differential Host Clock In:** These signals receive a differential host clock from the external clock synthesizer. This clock is used by all of the MCH logic that is in the host clock domain.
66IN	I CMOS	**66 MHz Clock In:** This signal receives a 66 MHz clock from the clock synthesizer. This clock is used by AGP and hub interface clock domains. Note that this clock input is 3.3 V tolerant.
CHA_RCLKOUT/ CHB_RCLKOUT	O CMOS	**RDRAM Clock Out:** These signals provide divided down versions of the RDRAM clock as feedback to the RDRAM clock synthesizers for phase alignment. Note that this signal is only driven to 1.8 V.
CHA_HCLK0UT/ CHB_HCLKOUT	O CMOS	**Host Clock Out:** These signals provide divided down versions of the host clock as feedback to the RDRAM clock synthesizers for phase alignment. Note that this signal is only driven to 1.8 V.
RSTIN#	I CMOS	**Reset In:** When asserted, this signal asynchronously resets the MCH logic. This signal is connected to the PCIRST# output of the ICH2. All AGP output and bi-directional signals also tri-states compliant to PCI Rev 2.0 and 2.1 specifications. Note that this input needs to be 3.3 V tolerant.
TESTIN#	I CMOS	**Test Input:** This signal is used for manufacturing and board-level test purposes. It is internally pulled up to VDDQ.

2.7. Voltage References, PLL Power

Signal Name	Type	Description
HDVREF[3:0]	—	**Host Data Reference Voltage:** Reference voltage input for the 4X data signals of the Host AGTL+ interface. Connect to a 2/3 VTT with 2% tolerance.
HAVREF[1:0]	—	**Host Address Reference Voltage:** Reference voltage input for the 2X address signals of the host AGTL+ interface. Connect to a 2/3 VTT with 2% tolerance.
CCVREF	—	**Host Common Clock Reference Voltage:** Reference voltage input for the common clock signals of the Host AGTL+ interface. Connect to a 2/3 VTT with 2% tolerance.
CHA_REF[1:0]	—	**RDRAM* Channel A Reference:** Reference voltage input for the RDRAM Channel A RSL interface.
CHB_REF[1:0]	—	**RDRAM Channel B Reference:** Reference voltage input for the RDRAM Channel B RSL interface.
GREF_0	—	**AGP Reference:** Reference voltage input for the AGP interface. Comes from graphic card.
GREF_1	—	**AGP Reference:** Reference voltage input for the AGP interface. Comes from graphic card.
HLREF_A	—	**Hub Interface Reference:** Reference voltage input for the hub interface. Connected to 1/2 VCC1_8 with 2% tolerance.
HLRCOMP_A	I/O CMOS	**Compensation for Hub Interface:** This signal is used to calibrate the hub interface I/O buffers. Connected to a 40 Ω with 1% tolerance or a 39 Ω with a 2% tolerance pull-down.
GRCOMP	I/O CMOS	**Compensation for AGP:** This signal is used to calibrate buffers. Connected to a 40 Ω with a 1% tolerance or a 39 Ω with a 2% tolerance Pull-down.
HRCOMP[1:0]	I/O CMOS	**Compensation for Host:** This signal is used to calibrate the host AGTL+ I/O buffers. Connected to a 20.75 Ω with a 1% tolerance pull-down
HSWNG[1:0]	I CMOS	**Host Compensation Reference Voltage:** Reference voltage input for the compensation logic. Connected to a 1/3 VTT with a 2% tolerance.
G_SWNG	I CMOS	**AGP Compensation Reference Voltage:** Reference voltage input for compensation logic. Hooked to GREF_0.
VCC1_8	—	**1. 8V Power Input Pins:**
VDDQ	—	**Power Supply Input for the AGP I/O Supply (1.5 V):**
VTT	—	**AGTL+ Bus Termination Voltage Inputs:**
VSS	—	**Ground:**
VCC1_8RAC	—	**1.8 V RAC Power Pins.**

2.8. Pin States during Reset

Table 5 indicates the MCH signal pin states during reset assertion.

Z	Tristate Outputs
ISO	Isolate Inputs in Inactive State
S	Strap sampled on RSTIN# rising edge
H	Driven High
L	Driven Low
D	Drive Outputs to Functional Logic Level
I	Input Active
U	Undefined - Indeterminate

Table 5. Pin States during Reset

Signal Name	State during RSTIN# Assertion
Host Interface	
CPURST#	L
HA[35:8,6:3]#	Z/I
HA[7]#	Z/I/S
HADSTB[1:0]#	Z/I
HD[63:0]#	Z/I
HDSTBP[3:0]#	Z/I
HDSTBN[3:0]#	Z/I
DBI[3:0]#	Z/I
ADS#	Z/I
BNR#	Z/I
BPRI#	Z/I
DBSY#	Z/I
DEFER#	Z/I
DRDY#	Z/I
HIT#	Z/I
HITM#	Z/I
HLOCK#	Z/I
HREQ[4:0]#	Z/I
HTRDY#	Z/I
RS[2:0]#	Z/I
BR0#	Z/I
HDVREF[3:0]	I
HAVREF[1:0]	I
CCVREF	I
HRCOMP[1:0]	Z
HSWNG[1:0]	I
Rambus* A	
DQA_A[8:0]	Z
DQB_A[8:0]	Z
RQ_A[7:0]	Z
CTM_A	I
CTM_A#	I
CFM_A	Z
CFM_A#	Z
SCK_A	L
CMD_A	Z
SIO_A	Z
CHA_VREF[1:0]	I
Rambus* B	
CHB_DQA[8:0]	Z
CHB_DQB[8:0]	Z
CHB_RQ[7:0]	Z
CHB_CTM	I
CHB_CTM#	I
CHB_CFM	Z
CHB_CFM#	Z
CHB_SCK	L
CHB_CMD	Z
CHB_SIO	Z
CHB_VREF[B:A]	I

Signal Name	State during RSTIN# Assertion
AGP	
PIPE#	I
SBA[7:0]	ISO
RBF#	I
WBF#	I
G_REQ#	I
ST[2:0]	L
G_GNT#	H
AD_STB[1:0]	Z
AD_STB[1:0]#	Z
SB_STB	I
SB_STB#	I
G_AD[31:0]	L/I
G_C/BE[3:0]#	L/I
G_FRAME#	Z/I
G_IRDY#	S
G_TRDY#	Z/I
G_STOP#	Z/I

Signal Name	State during RSTIN# Assertion
G_DEVSEL#	Z/I
G_PAR	L/I
Hub Interface	
HL_A[7:4]	L/I
HL_A[3:0]	Z/I
HLA_STB	L/I
HLA_STB#	H/I
HLRCOMP_A	Z
HLREF_A	I
Clocks and Misc.	
BCLK[1:0]	I
66IN	I
CHA_HCLKOUT	D
CHB_HCLKOUT	D
CHA_RCLKOUT	D
CHB_RCLKOUT	D
RSTIN#	I
TESTIN#	I

3. Register Description

This chapter describes the MCH configuration registers. A detailed register bit description is provided. The MCH contains two sets of software accessible registers, accessed via the Host I/O address space:

1. Control registers I/O mapped into the host I/O space. These two registers control access to PCI and AGP configuration space (see section entitled I/O Mapped Registers)

2. Internal PCI configuration registers residing within the MCH are partitioned into two logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to Host-Hub Interface bridge functionality (controls PCI_A including DRAM configuration, other chip-set operating parameters, and optional features). The second register block is dedicated to Host-AGP bridge functions (controls AGP interface configurations and operating parameters).

The MCH supports PCI configuration space accesses using the mechanism denoted as Configuration Mechanism 1 in the PCI specification.

The MCH internal registers (I/O Mapped and PCI configuration registers) are accessible by the host. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONF_ADDR, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field).

3.1. Register Nomenclature, Definitions, and Access Attributes

Symbol	Description
RO	**Read Only**. If a register is read only, writes to this register have no effect.
R/W	**Read/Write**. A register with this attribute can be read and written.
R/W/L	**Read/Write/Lock**. A register with this attribute can be read, written, and Lock.
R/WC	**Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	**Read/Write Once.** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
L	**Lock.** A register bit with this attribute becomes Read Only after a lock bit is set.
Reserved Bits	Some of the MCH registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note that software does not need to perform read, merge, write operation for the Configuration Address (CONF_ADDR) register.

Symbol	Description
Reserved Registers	In addition to reserved bits within a register, the MCH contains address locations in the configuration space that are marked “Reserved”. When a “Reserved” register location is read, a random value is returned. (“Reserved” registers can be 8-, 16-, or 32-bit in size). Registers that are marked as “Reserved” must not be modified by system software. Writes to “Reserved” registers may cause system failure.
Default Value upon a Reset	Upon a Full Reset, the MCH sets all of its internal configuration registers to predetermined **default** states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the MCH registers accordingly.

3.2. PCI Configuration Space Access

The MCH and ICH2 are physically connected by the hub interface. From a configuration standpoint, the hub interface is logically PCI Bus 0. As a result, all devices internal to the MCH and ICH2 appear to be on PCI Bus 0. The system’s primary PCI expansion bus is physically attached to the ICH2 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge; therefore, it has a programmable PCI Bus number. **Note that the primary PCI bus is referred to as PCI_A in this document and is not PCI Bus 0 from a configuration standpoint.** The AGP and 16-bit hub interface ports appear to system software to be real PCI busses behind PCI-to-PCI bridges resident as devices on PCI Bus 0.

The MCH contains up to two PCI devices within a single physical component. The configuration registers for the devices are mapped as devices residing on PCI Bus 0.

- Device 0: Host-Hub Interface bridge/DRAM controller. Logically this appears as a PCI device residing on PCI Bus 0. Physically, Device 0 contains the standard PCI registers, DRAM registers, the Graphics Aperture controller, and other MCH specific registers.
- Device 1: Host-AGP bridge. Logically this appears as a “virtual” PCI-to-PCI bridge residing on PCI Bus 0. Physically, Device 1 contains the standard PCI-to-PCI bridge registers and the standard AGP configuration registers (including the AGP I/O and memory address mapping).

The following table shows the Device # assignment for the various internal MCH devices.

MCH Function	Bus 0, Device #	Function #
DRAM Controller/8-bit Hub Interface Controller	Device 0	Function 0
Host-to-AGP Bridge (virtual PCI-to-PCI)	Device 1	Function 0

Note that a physical PCI Bus 0 does not exist. The hub interface and the internal devices in the MCH and ICH2 logically constitute PCI Bus 0 to configuration software.

Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot-based “configuration space” that allows each device to contain up to 8 functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the MCH. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The MCH supports only Mechanism #1.

The configuration access mechanism makes use of the CONF_ADDR Register and CONF_DATA Register. To reference a configuration register a DWord I/O write cycle is used to place a value into CONF_ADDR that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONF_ADDR [31] must be 1 to enable a configuration cycle. CONF_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONF_ADDR. Any read or write to CONF_DATA results in the MCH translating the CONF_ADDR into the appropriate configuration cycle.

The MCH is responsible for translating and routing the processor’s I/O accesses to the CONF_ADDR and CONF_DATA registers to internal MCH configuration registers or AGP.

Routing Configuration Accesses

The MCH supports up to two bus interfaces—hub interface and AGP. PCI configuration cycles are selectively routed to one of these interfaces. The MCH is responsible for routing PCI configuration cycles to the proper interface. PCI configuration cycles to ICH2 internal devices and Primary PCI (including downstream devices) are routed to the ICH2 via the hub interface. AGP configuration cycles are routed to AGP. The AGP interface is treated as a separate PCI bus from the configuration point of view. Routing of configuration accesses to AGP is controlled via the standard PCI-to-PCI bridge mechanism using information contained within the Primary Bus Number, the Secondary Bus Number, and the Subordinate Bus Number registers of the corresponding PCI-to-PCI bridge device.

Logical PCI BUS 0 Configuration Mechanism

The MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONF_ADDR register. If the Bus Number field of CONF_ADDR is 0 the configuration cycle is targeting a PCI Bus 0 device.

- The Host-Hub Interface bridge entity within the MCH is hardwired as Device 0 on PCI Bus 0.
- The Host-AGP bridge entity within the MCH is hardwired as Device 1 on PCI Bus 0.

Configuration cycles to any of the MCH’s internal devices are confined to the MCH and not sent over the hub interface. Accesses to disabled MCH internal devices are forwarded over the hub interface as Type 0 configuration cycles.

Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONF_ADDR is non-zero, and is less than the values programmed into any of the internal MCH device's Secondary Bus Number registers or greater than the values programmed into the Subordinate Bus Number registers, the MCH generates a Type 1 hub interface configuration cycle. The ICH2 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI or a downstream PCI bus.

AGP Bus Configuration Mechanism

From the chipset configuration perspective, AGP is seen as PCI bus interfaces residing on a Secondary Bus side of the "virtual" PCI-to-PCI bridges referred to as the MCH Host-AGP bridge. On the Primary bus side, the "virtual" PCI-to-PCI bridge is attached to PCI Bus 0. Therefore, the Primary Bus Number register is hardwired to 0. The "virtual" PCI-to-PCI bridge entity converts Type 1 PCI Bus configuration cycles on PCI Bus 0 into Type 0 or Type 1 configuration cycles on the AGP interface. Type 1 configuration cycles on PCI Bus 0 that have a Bus Number that matches the Secondary Bus Number of one of the MCH's "virtual" PCI-to-PCI bridges are translated into Type 0 configuration cycles on the AGP interface.

If the Bus Number is non-zero, greater than the value programmed into the Secondary Bus Number register, and less than or equal to the value programmed into the Subordinate Bus Number register, the MCH generates a Type 1 PCI configuration cycle on AGP.

3.3. I/O Mapped Registers

The MCH contains a set of registers that reside in the Host I/O address space — CONF_ADDR register and CONF_DATA register. The CONF_ADDR register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.3.1. CONF_ADDR—Configuration Address Register

I/O Address:	0CF8h Accessed as a DWord
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

CONF_ADDR is a 32-bit register that can be accessed only as a DWord. Byte or Word reference "pass through" the Configuration Address Register and the hub interface onto the PCI bus as an I/O cycle. The CONF_ADDR register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CFGE).** This bit enables/disables access to PCI configuration space. 1 = Enable 0 = Disable
30:24	Reserved. These bits are read only and have a value of 0.

Bit	Descriptions
23:16	**Bus Number.** When the Bus Number is programmed to 00h, the target of the configuration cycle is a hub interface agent (MCH, ICH2, etc.). The configuration cycle is forwarded to the hub interface if the Bus Number is programmed to 00h and the MCH is not the target (the device number is ≥ 2). If the Bus Number is non-zero and matches the value programmed in the Secondary Bus Number Register of device 1, a Type 0 PCI configuration cycle is generated on AGP. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of device 1, and less than or equal to the value programmed into the Subordinate Bus Number Register of device 1, a Type 1 PCI configuration cycle is generated on AGP. If the Bus Number is non-zero and does not fall within the ranges enumerated by device 1's Secondary Bus Number or Subordinate Bus Number Register, then a hub interface Type 1 configuration cycle is generated.
15:11	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is 00, the MCH decodes the Device Number field. The MCH is always Device Number 0 for the Host-hub interface bridge entity and Device Number 1 for the Host-AGP entity. Therefore, when the Bus Number = 0 and the Device Number = 0–1, the internal MCH devices are selected. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register a Type 0 PCI configuration cycle is generated on AGP. The MCH decodes the Device Number field [15:11] and assert the appropriate GAD signal as an IDSEL. For PCI-to-PCI bridge translation, one of the 16 IDSELs is generated. When bit [15] = 0, bits [14:11] are decoded to assert a signal AD[31:16] IDSEL. GAD16 is asserted to access Device 0, GAD17 for Device 1, and so forth up to Device 15 for which will assert AD31. All device numbers higher than 15 cause a type 0 configuration access with no IDSEL asserted, which results in a Master Abort reported in the MCH's "virtual" PCI-to-PCI bridge registers. For Bus Numbers resulting in the hub interface configuration cycles, the MCH propagates the device number field as A[15:11]. For bus numbers resulting in AGP/PCI_B type 1 configuration cycles, the device number is propagated as GAD[15:11].
10:8	**Function Number.** This field is mapped to GAD[10:8] during AGP configuration cycles and A[10:8] during the hub interface configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The MCH ignores configuration cycles to its internal devices if the function number is not equal to 0.
7:2	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to GAD[7:2] during AGP Configuration cycles and A[7:2] during the hub interface Configuration cycles.
1:0	Reserved.

3.3.2. CONF_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

CONF_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONF_DATA is determined by the contents of CONF_ADDR.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If CONF_ADDR[bit 31] is 1, any I/O access to the CONF_DATA register will be mapped to configuration space using the contents of CONF_ADDR.

3.4. Host-Hub Interface Bridge Device Registers (Device 0)

Table 6 summarizes the MCH configuration space for Device 0. Address locations not shown are reserved. An “s” in the Default Value column means that a strap determines the power-up default value for that bit.

Table 6. Host-Hub Interface Bridge Register Address Map (Device 0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2530h	RO
04–05h	PCICMD	PCI Command	0006h	RO, R/W
06–07h	PCISTS	PCI Status	0090h	RO, R/WC
08h	RID	Revision Identification	02h	RO
09h	—	Reserved	—	—
0Ah	SUBC	Sub-Class Code	00h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch	—	Reserved	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0Fh	—	Reserved	—	—
10–13h	APBASE	Aperture Base Configuration	00000008h	RO, R/W
14–2Bh	—	Reserved	—	—
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO
30–33h	—	Reserved	—	—
34h	CAPPTR	Capabilities Pointer	A0h	RO
35–3Fh	—	Reserved	—	—
40–4Fh	GAR[0:15]	RDRAM Group Architecture Register [0:15]	80h	R/W
50–51h	MCHCFG	MCH Configuration	0000000000 000s00h	RO, R/W, R/WO
52–57h	—	Reserved	—	—
58h	FDHC	Fixed DRAM Hole Control	00h	R/W
59–5Fh	PAM[0:6]	Programmable Attribute Map [0:6]	00h	R/W
60–61h	GBA0	RDRAM Group Boundary Address 0	0001h	RO, R/W/L
62–63h	GBA1	RDRAM Group Boundary Address 1	0001h	RO, R/W/L
64–65h	GBA2	RDRAM Group Boundary Address 2	0001h	RO, R/W/L
66–67h	GBA3	RDRAM Group Boundary Address 3	0001h	RO, R/W/L
68–69h	GBA4	RDRAM Group Boundary Address 4	0001h	RO, R/W/L

Address Offset	Register Symbol	Register Name	Default Value	Access
6A–6Bh	GBA5	RDRAM Group Boundary Address 5	0001h	RO, R/W/L
6C–6Dh	GBA6	RDRAM Group Boundary Address 6	0001h	RO, R/W/L
6E–6Fh	GBA7	RDRAM Group Boundary Address 7	0001h	RO, R/W/L
70–71h	GBA8	RDRAM Group Boundary Address 8	0001h	RO, R/W/L
72–73h	GBA9	RDRAM Group Boundary Address 9	0001h	RO, R/W/L
74–75h	GBA10	RDRAM Group Boundary Address A	0001h	RO, R/W/L
76–77h	GBA11	RDRAM Group Boundary Address B	0001h	RO, R/W/L
78–79h	GBA12	RDRAM Group Boundary Address C	0001h	RO, R/W/L
7A–7Bh	GBA13	RDRAM Group Boundary Address D	0001h	RO, R/W/L
7C–7Dh	GBA14	RDRAM Group Boundary Address E	0001h	RO, R/W/L
7E–7Fh	GBA15	RDRAM Group Boundary Address F	0001h	RO, R/W/L
80–87h	—	Reserved	—	—
88h	RDPS	RDRAM Pool Sizing	10h	RO, WO, L
89–8Fh	—	Reserved	—	—
90–93h	DRD	RDRAM Device Register Data	00000000h	R/W
94–97h	RICM	RDRAM Initialization Control Management	00000000h	RO, R/W
98–9Ch	—	Reserved	—	—
9Dh	SMRAM	System Management RAM Control	02h	RO, R/W, L
9Eh	ESMRAMC	Extended System Management RAM Control	38h	RO, R/W, R/WC, L
9Fh	—	Reserved	—	—
A0–A3h	ACAPID	AGP Capability Identifier	00200002h	RO
A4–A7h	AGPSTAT	AGP Status Register	1F000217h	RO
A8–ABh	AGPCMD	AGP Command Register	00000000h	R/W
AC–AFh	—	Reserved	—	—
B0–B3h	AGPCTRL	AGP Control Register	00000000h	R/W
B4h	APSIZE	Aperture Size	00h	R/W
B5–B7h	—	Reserved	—	—
B8–BBh	ATTBASE	Aperture Translation Table	00000000h	R/W
BCh	AMTT	AGP MTT Control	00h	R/W
BDh	LPTT	AGP Low Priority Transaction Timer	00h	R/W
Beh	RDT	RDRAM Timing	00h	R/W
BF–C3h	—	Reserved	—	—
C4–C5h	TOM	Top of Low Memory	0000h	R/W
C6–C7h	—	Reserved	—	—
C8–C9h	ERRSTS	Error Status	0000h	RO, R/WC

Address Offset	Register Symbol	Register Name	Default Value	Access
CA–CBh	ERRCMD	Error Command	0000h	R/W
CC–CDh	SMICMD	SMI Command	0000h	R/W
CE–CFh	SCICMD	SCI Command	0000h	R/W
D0–DBh	—	Reserved	—	—
DC–DDh	DRAMRC	RDRAM Refresh Control	0000h	R/W
DE–DFh	SKPD	Scratchpad Data	0000h	R/W
E0–E1h	—	Reserved	—	—
E2–E3h	DERRCTL	DRAM Error Control	0000h	RO
E4–E7h	EAP	DRAM Error Address	00000000h	RO
E8–F3h	—	Reserved	—	—
F4–F7h	MISC_CNTL	Miscellaneous Control Register	0000F874h	R/W
F8–FFh	—	Reserved	—	—

3.4.1. VID—Vendor Identification Register (Device 0)

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number**. This is a 16-bit value assigned to Intel. Intel VID = 8086h.

3.4.2. DID—Device Identification Register (Device 0)

Address Offset: 02–03h
Default Value: 2530h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:10	**Device Identification Number**. This is a 16-bit value assigned to the MCH Host-Hub Interface bridge Function 0.

3.4.3. PCICMD—PCI Command Register (Device 0)

Address Offset: 04–05h
Default: 0006h
Access: Read/Write, Read Only
Size 16 bits

Since MCH Device 0 does not physically reside on PCI0, many of the bits are not implemented. Writes to bits that are not implemented have no affect.

Bit	Descriptions
15:10	Reserved.
9	**Fast Back-to-Back—RO.** Not Implemented; Hardwired to 0. This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented.
8	**SERR Enable (SERRE)—R/W.** This bit is a global enable bit for Device 0 SERR messaging. The MCH does not have an SERR# signal. The MCH communicates the SERR# condition by sending an SERR message to the ICH2. 1 = Enable. MCH is enabled to generate SERR messages over the hub interface for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. If SERRE is reset to 0, then the SERR message is not generated by the MCH for Device 0. 0 = Disable. **NOTE:** This bit only controls SERR message for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring on their respective devices.
7	**Address/Data Stepping—RO.** Not Implemented; Hardwired to 0.
6	**Parity Error Enable (PERRE)—R/W.** Not Implemented; Hardwired to 0.
5	**VGA Palette Snoop—RO.** (Not Implemented; Hardwired to 0).
4	**Memory Write and Invalidate Enable(MWIE)—RO.** Not Implemented; Hardwired to 0.
3	**Special Cycle Enable(SCE)—RO.** Not Implemented; Hardwired to 0.
2	**Bus Master Enable (BME)—RO.** Not Implemented; Hardwired to 1. The MCH is always enabled as a master on the hub interface.
1	**Memory Access Enable (MAE)—RO.** Not Implemented; Hardwired to 1. The MCH always allows access to main memory.
0	**I/O Access Enable (IOAE)—RO.** Not Implemented; Hardwired to 0.

3.4.4. PCISTS—PCI Status Register (Device 0)

Address Offset: 06–07h
Default Value: 0090h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device 0 on the hub interface. Since MCH Device 0 is the Host-to-hub interface bridge, many of the bits are not implemented. Writes to bits that are not implemented have no affect.

Bit	Description
15	Reserved
14	**Signaled System Error (SSE)—R/WC**. 1 = MCH Device 0 generates an SERR message over the hub interface for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or ERRSTS registers. 0 = Software sets SSE to 0 by writing a 1 to this bit.
13	**Received Master Abort Status (RMAS)—R/WC**. 1 = MCH generated a hub interface request that receives a Master Abort completion packet or Master Abort Special Cycle. 0 = Software clears this bit by writing a 1 to it.
12	**Received Target Abort Status (RTAS)—R/WC.** 1 = MCH generated a hub interface request that receives a Target Abort completion packet or Target Abort Special Cycle. 0 = Software clears this bit by writing a 1 to it.
11	**Signaled Target Abort Status (STAS)—RO.** Not Implemented; Hardwired to 0. The MCH will not generate a Target Abort hub interface completion packet or Special Cycle.
10:9	**DEVSEL Timing (DEVT)—RO**. hub interface does not comprehend DEVSEL# protocol. These bits are hardwired to 00.
8	**Master Data Parity Error Detected (DPD)—RO.** Not Implemented; Hardwired to 0. PERR signaling and messaging are not implemented.
7	**Fast Back-to-Back (FB2B)—RO**. Not Implemented; Hardwired to 1.
6:5	**Reserved**
4	**Capability List (CLIST)—RO.** 1 = Indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP Capability standard register resides.
3:0	Reserved.

3.4.5. RID—Revision Identification Register (Device 0)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the MCH Device 0.

Bit	Description
7:0	**Revision Identification Number**. This is an 8-bit value that indicates the revision identification number for the MCH Device 0. For the A-2 Stepping, this value is 02h. For the A-3 Stepping this value is 04h

3.4.6. SUBC—Sub-Class Code Register (Device 0)

Address Offset: 0Ah
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the MCH Device 0.

Bit	Description
7:0	**Sub-Class Code (SUBC)**. This is an 8-bit value that indicates the category of bridge into which the MCH falls. 00h = Host Bridge.

3.4.7. BCC—Base Class Code Register (Device 0)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the MCH Device 0.

Bit	Description
7:0	**Base Class Code (BASEC)**. This is an 8-bit value that indicates the Base Class Code for the MCH. 06h = Bridge device.

3.4.8. MLT—Master Latency Timer Register (Device 0)

Address Offset: 0Dh
Default Value: 00h
Access: Read Only
Size: 8 bits

The hub interface does not comprehend the concept of Master Latency Timer. Therefore this register is not implemented.

Bit	Description
7:0	These bits are hardwired to 0. Writes have no effect.

3.4.9. HDR—Header Type Register (Device 0)

Offset: 0Eh
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Description
7:0	This read only field always returns 0 when read and writes have no affect.

3.4.10. APBASE—Aperture Base Configuration Register (Device 0)

Offset: 10–13h
Default: 00000008h
Access: Read/Write, Read Only
Size: 32 bits

The APBASE is a standard PCI Base Address register that is used to set the base of the Graphics Aperture. The standard PCI configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to 0 or behave as hardwired to 0). To allow for flexibility (of the aperture), an additional register called APSIZE is used as a “back-end” register to control which bits of the APBASE will behave as hardwired to 0. This register is programmed by the MCH specific BIOS code that will run before any of the generic configuration software is run.

Note that bit 9 of the MCHCFG register is used to prevent accesses to the aperture range before this register is initialized by the configuration software and the appropriate translation table structure has been established in the main memory.

Bit	Description
31:28	**Upper Programmable Base Address bits—R/W.** These bits are used to locate the range size selected via lower bits 27:4. Default = 0000
27:22	**Lower "Hardwired"/Programmable Base Address bits—R/W.** These bits behave as a "hardwired" or as a programmable depending on the contents of the APSIZE register as defined below: **27 26 25 24 23 22 Aperture Size** r/w r/w r/w r/w r/w r/w 4 MB r/w r/w r/w r/w r/w 0 8 MB r/w r/w r/w r/w 0 0 16 MB r/w r/w r/w 0 0 0 32 MB r/w r/w 0 0 0 0 64 MB r/w 0 0 0 0 0 128 MB 0 0 0 0 0 0 256 MB Bits 27:22 are controlled by the bits 5:0 of the APSIZE register in the following manner: If bit APSIZE[5]=0, APBASE[27]=0; if APSIZE[5]=1, APBASE[27]=r/w (read/write). The same applies correspondingly to other bits. Default for APSIZE[5:0]=000000b forces default APBASE[27:22] =000000b (i.e., all bits respond as "hardwired" to 0). This provides a default to the maximum aperture size of 256 MB. The MCH specific BIOS is responsible for selecting smaller size (if required) before PCI configuration software runs and establishes the system address map.
21:4	**Hardwired to 0.** This forces minimum aperture size selected by this register to be 4 MB.
3	**Prefetchable—RO.** Hardwired to 1 to identify the Graphics Aperture range as a prefetchable (i.e., there are no side effects on reads, the device returns all bytes on reads, regardless of the byte enables, and the MCH may merge processor writes into this range without causing errors.)
2:1	**Type—RO.** These bits determine addressing type and they are hardwired to 00 to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space.
0	**Memory Space Indicator—RO.** Hardwired to 0 to identify aperture range as a memory range.

3.4.11. SVID—Subsystem Vendor ID (Device 0)

Offset: 2C–2Dh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Description
15:0	**Subsystem Vendor ID—R/WO.** The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

3.4.12. SID—Subsystem ID (Device 0)

Offset: 2E–2Fh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Description
15:0	**Subsystem ID—R/WO.** The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

3.4.13. CAPPTR—Capabilities Pointer (Device 0)

Offset: 34h
Default: A0h
Access: Read Only
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location where the AGP standard registers are located.

Bit	Description
7:0	**Pointer to Start of AGP Standard Register Block.** This pointer indicates to software where it can find the beginning of the AGP register block. The value in this field is A0h

3.4.14. GAR[0:15]—RDRAM* Group Architecture Register (Device 0)

Address Offset: 40–4Fh (GAR0–GAR15)
Default Value: 80h
Access: Read/Write
Size: 8 bits/register

This 8-bit register defines the #of banks and DRAM technology of each device group in the RDRAM channel. There are 16 GAR registers (GAR0–GAR15) that are used to define 16 groups for the Direct RDRAM channel.

Bit	Description
7:6	**Device Page Size (DPS)**. This field defines the page size of each device in the corresponding group. 00 = Reserved 01 = Reserved 10 = 1 KB 11 = 2 KB
5	**Reserved**
4	**Device Banks (DB).** This field defines # of bank architecture in each device in the group. 0 = 16 dependent Banks 1 = 32 dependent Banks arranged in two groups of 16 dependent banks (i.e., 2x16)
3	**Reserved**
2:1	**Device DRAM Technology (DDT).** This field defines the DRAM technology of each device in the group. 00 = Reserved 01 = 128/144Mbit 10 = 256/288Mbit 11 = Reserved
0	Reserved.

3.4.15. MCHCFG—MCH Configuration Register (Device 0)

Offset: 50–51h
Default: 0000_0000_ 0000_0s00b
Access: Read/Write Once, Read/Write, Read Only
Size: 16 bits

Bit	Description
15:12	**Reserved**
11	**Direct RDRAM Frequency—R/W.** These bits are written by the BIOS after polling the Direct RDRAMs, finding the least common denominator speed and comparing with the Host-to-RDRAM frequency ratio. 0 = 4:3 Host-to-RDRAM frequency ratio (configuration supports tRCD=7) 1 = 1:1 Host-to-RDRAM frequency ratio (configuration supports tRCD=7 or tRCD=9)
10	**Reserved**
9	**Aperture Access Global Enable—R/W.** This bit is used to prevent access to the graphics aperture from any port (host, hub interface, or AGP) before the aperture range is established by the configuration software and appropriate translation table in the main DRAM has been initialized. It must be set after system is fully configured for aperture accesses. 1 = Enable 0 = Disable (Default)
8:7	**DRAM Data Integrity Mode (DDIM)—R/W.** These bits select one of 3 DRAM data integrity modes. 00 = Non-ECC (Byte-Wise Writes supported, RDRAM Device only). (Default) 01 = Reserved 10 = ECC Mode (Generation and Error Checking/Correction) 11 = Reserved
6	**Reserved**
5	**MDA Present (MDAP)—R/W.** This bit works with the VGA Enable bit in the BCTRL register of device 1 and 5 to control the routing of host-initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set when the VGA Enable bit is not set in either device 1 or 5. If the VGA enable bit is set, accesses to IO address range x3BCh–x3BFh are forwarded to the hub interface. MDA resources are defined as the following: Memory: 0B0000h–0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the hub interface, even if the reference includes I/O locations not listed above. Refer to the System Address Map Chapter of this document for further information.
4:3	**Reserved**

Bit	Description
2	**In-Order Queue Depth (IOQD)—RO.** This bit reflects the value sampled on HA[7]# on the deassertion of the CPURST#. It indicates the depth of the host bus in-order queue (i.e., level of host bus pipelining). If IOQD is set to 1 (HA[7]# sampled 1; that is, not driven on the host bus), then the depth of the host bus in-order queue is configured to the maximum allowed by the host bus protocol (i.e., 12). Note that the MCH has an 8 deep IOQ and asserts BNR# on the bus to limit the number of queued bus transactions to 8. If the IOQD bit is set to 0 (HA[7]# is sampled asserted; i.e., 0), the depth of the host bus in-order queue is set to 1 (i.e., no pipelining support on the host bus). Note that HA[7]# is not driven by the MCH during CPURST#. If an IOQ size of 1 is desired, HA[7]# must be driven low during CPURST# by an external source.
1	**APIC Memory Range Disable (APICDIS)—R/W. Note that this bit should NOT be set to 1.** 1 = Disable. The MCH forwards accesses to the IOAPIC regions to the appropriate interface, as speciified by the memory and PCI configuration registers. 0 = Enable. The MCH sends cycles between 0_FEC0_0000h and 0_FEC7_FFFFh to the hub interface.
0	**Reserved**

3.4.16. FDHC—Fixed DRAM Hole Control Register (Device 0)

Address Offset: 58h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This 8-bit register controls a fixed DRAM hole: 15–16 MB.

Bit	Description
7	**Hole Enable (HEN).** This field enables a memory hole in DRAM space. Host cycles matching an enabled hole are passed on to ICH2 through the hub interface. The hub interface cycles matching an enabled hole will be ignored by the MCH. Note that a selected hole is not re-mapped. 0 = Disable. No hole 1 = Enable. 15 MB – 16 MB (1 MB hole)
6:0	Reserved.

3.4.17. PAM[0:6]—Programmable Attribute Map Registers (Device 0)

Address Offset: 59–5Fh (PAM0–PAM6)
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The MCH allows programmable memory attributes on 13 *Legacy* memory segments of various sizes in the 640 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to host initiator only access to the PAM areas. MCH forwards to main memory any AGP, PCI, or hub interface initiated accesses to the PAM areas. These attributes are:

RE - **Read Enable**. When RE = 1, the host read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI0.

WE - **Write Enable**. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI0.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions that are typically 16 KB. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 7.

Table 7. PAM Register Control Field Definitions

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
x	x	0	0	**Disabled.** DRAM is disabled and all accesses are directed to the hub interface. The MCH does not respond as a PCI target for any read or write access to this area.
X	x	0	1	**Read Only**. Reads are forwarded to DRAM and writes are forwarded to the hub interface for termination. This write protects the corresponding memory segment. The MCH responds as an AGP or the hub interface target for read accesses but not for any write accesses.
X	x	1	0	**Write Only**. Writes are forwarded to DRAM and reads are forwarded to the hub interface for termination. The MCH responds as an AGP or the hub interface target for write accesses but not for any read accesses.
X	x	1	1	**Read/Write**. This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by the MCH and forwarded to DRAM. The MCH responds as an AGP or the hub interface target for both read and write accesses.

At the time that a HL or AGP accesses to the PAM region may occur, the targeted PAM segment **must be programmed to be both readable and writeable**.

As an example, consider BIOS that is implemented on the expansion bus. During the initialization process, BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. Table 8 and Figure 2 show the PAM registers and the associated attribute bits.

Figure 2. PAM Registers and Attribute Bits

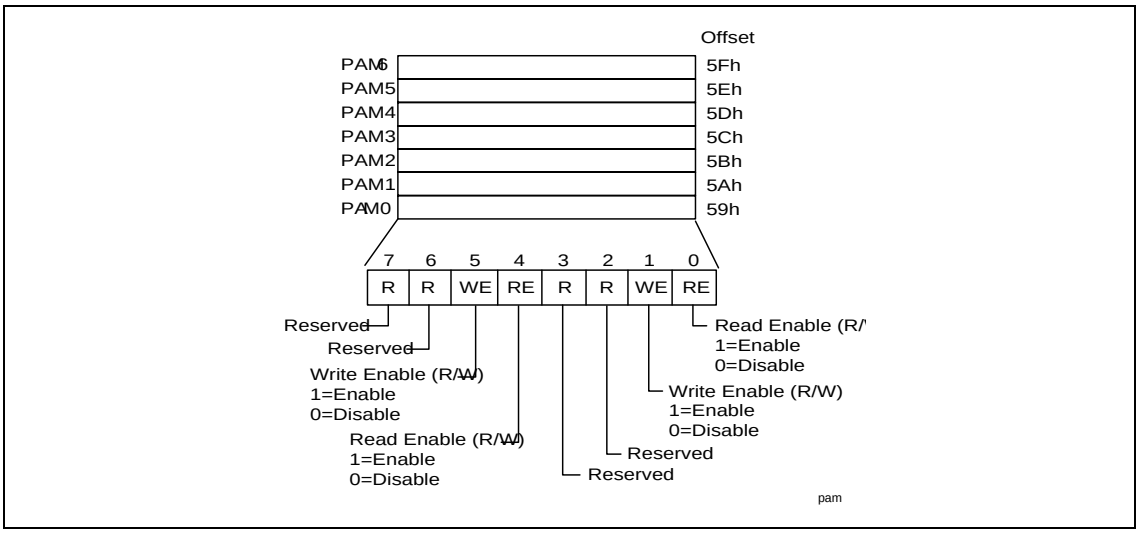


Table 8. PAM Registers and Attribute Bits

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h– 0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h– 0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h– 0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h– 0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h– 0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h– 0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h– 0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h– 0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h– 0EFFFFh	BIOS Extension	5Fh

For details on overall system address mapping scheme see the Address Map Chapter of this document.

- **DOS Application Area (00000h–9FFFh):** The 640 KB DOS area is divided into two parts. The 512 KB area at 0 to 7FFFFh is always mapped to the main memory controlled by the MCH. The 128 KB address range from 080000 to 09FFFFh can be mapped to PCI0 or to main DRAM. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI0) via MCH FDHC configuration register.
- **Video Buffer Area (A0000h–BFFFFh):** Attribute bits do not control this 128 KB area. The host - initiated cycles in this region are always forwarded to either PCI0 or AGP unless this range is accessed in SMM mode. Routing of accesses is controlled by the Legacy VGA control mechanism of the “virtual” PCI-to-PCI bridge device in the MCH.

  This area can be programmed as SMM area via the SMRAM register. When used as a SMM space, this range cannot be accessed from the hub interface or AGP.
- **Expansion Area (C0000h–DFFFFh):** This 128 KB area is divided into eight 16 KB segments, which can be assigned with different attributes via PAM control register as defined by the Table above.
- **Extended System BIOS Area (E0000h–EFFFFh):** This 64 KB area is divided into four 16 KB segments that can be assigned with different attributes via PAM control register as defined by the Table above.
- **System BIOS Area (F0000h–FFFFFh):** This area is a single 64 KB segment, which can be assigned with different attributes via PAM control register as defined by the Table above.

3.4.18. GBA[0:15]—RDRAM* Group Boundary Address Register (Device 0)

Address Offset:	60–7Fh (GBA0–GBA15)
Default:	0001h
Access:	Read/Write/Lock
Size	16 bits/register

This register is locked and becomes Read Only when the D_CLK bit in the SMRAM register is set. This is done to improve SMM security.

The RDRAM device-pairs are logically arranged into groups. There are eight groups when the MCH is configured for single-channel pair mode operation, and there are four groups for multiple channel-pair mode operation. Each group requires a separate GBA register. The GBA registers define group ID and the upper and lower addresses for each group in a channel-pair. Contents of bits 9:0 of this register represent the boundary addresses in 16-MB granularity.

For example, a value of 01h indicates that the programmed group applies to memory below 16 MB. Only the first eight GBA registers are used in single-channel pair mode. All 16 GBA registers are used in multiple channel-pair mode. Note that GBA15 must always contain the group boundary address that points to the top of memory, whether the MCH is being used in single-channel pair mode or multiple channel-pair mode.

60–61h	GBA0 = Total memory in group0 (in 16 MB)
62–63h	GBA1 = Total memory in group0 + group1 (in 16 MB)
64–65h	GBA2 = Total memory in group0 + group1 + group2 (in 16 MB)
66–67h	GBA3 = Total memory in group0 + group1 + group2 + group3 (in 16 MB)
....	
7E–7Fh	GBA15 = Total memory in group0 + group1 + group2 + … + group15 (in 16 MB)

Bit	Description
15:14	Reserved.
13:11	**Group ID (GID).** This 3-bit value is used to identify a logical group of Direct RDRAM devices. This value and appropriate address bits are used to generate the device RDRAM_D device ID. **Note:** All device-pairs populated in a group must be of the same memory technology.
10:0	**Group Boundary Address (GBA).** This 11-bit value is compared against address lines A[33:24] to determine the upper address limit of a particular group of devices (i.e., GBA minus previous GBA = group size).

3.4.19. RDPS—RDRAM* Pool Sizing Register (Device 0)

Address Offset: 88h
Default Value: 10h
Access: Read/Write
Size: 8 bits

Bit	Description
7	**Pool Lock (LOCK).** 1 = RDPS register is Read Only. 0 = RDPS register is Read/Write.
6	Reserved.
5	**Reinitialize RDRAM Pools (POOLINIT).** When the POOLINIT bit is set, the RDRAM pools are reinitialized to the default value contained in this register. As long as this bit is 0, the other fields in this register may be modified without changing the behavior of the pools. Only when this bit is set or when a thermal over-temperature condition occurs are the values programmed into this register re-examined by the pool logic. Following a write of 1 to this bit, the new pool sizes will take effect and the DRAM interface logic will perform any operations necessary to comply with the new pool constraints. When these compliance operations are completed and the MCH is operating with the new pool settings, the POOLINIT bit is cleared to 0. Software can poll the bit to check for completion of the pool mode transition prior to proceeding with test cases. **Note:** While over-temperature conditions (during current calibration) do cause new pool values to be loaded, they do not have any effect on the contents of this bit.
4	**Pool C Operating Mode (PCS).** 1 = All devices found neither in pool A nor in pool B are assumed to be in standby mode. 0 = All devices in pool C are assumed to be in standby mode. **Note:** Even though this bit defaults to 12 (which is Pool C Nap mode) the MCH functionally defaults to Pool C Standby mode (Nap mode is not supported by the 82850/82850E MCH).
3:2	**Pool A Capacity (PAC).** This field defines the maximum number of RDRAM devices that can reside in Pool A at a time. 00 = 1 01 = 2 10 = 4 11 = 8
1:0	**Pool B Capacity (PBC).** This field defines the maximum number of RDRAM devices that can reside in Pool B at a time. 00 = 1 01 = 4 10 = 8 11 = 16

3.4.20. DRD—RDRAM* Device Register Data Register (Device 0)

Address Offset: 90–93h
Default Value: 0000h
Access: Read/Write
Size: 32 bits

Bit	Description
31:0	**Register Data (RD).** Bits 31:0 contain the 32 bits of data to be written to a RDRAM register or the data read from a RDRAM register as a result of IOP execution. Data will be valid when the IIO bit of the RICM register has transitioned from 1 to 0. Bits 31:16 apply to Direct RDRAM interface A and bits 15:0 apply to Direct RDRAM interface B.

3.4.21. RICM—RDRAM* Initialization Control Management Register (Device 0)

Address Offset: 94–97h
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

Bit	Description
31	Reserved.
30	**RDRAM Interface B Stick Channel Swap.** 1 = The two stick channels of each MRH-R are swapped on the RDRAM interface B. 0 = Not swapped
29:28	**Time To PowerUp(TPU).** This field defines the total powerdown exit time for RDRAM devices and corresponds to the RDRAM device (PDNA + tPDNB) timing. 00 = 42.0 µs 01 = 34.5 µs 10 = 27.0 µs 11 = 19.5 µs
27	**Initialization Complete (IC).** This bit is for hardware use. 1 = BIOS sets this bit to 1 after the initialization of the RDRAM memory array is complete.
26:24	Reserved.
23	**Initiate Initialization Operation (IIO).** Software must check to see if this bit is 0 before writing to it. 1 = Execution of the initialization operation specified by IOP starts. 0 = After the execution is completed, the MCH sets this bit to 0. The operations that specify register data read from the Direct RDRAM will have the data valid in DRD register when this bit is 0.
22	Reserved.
21:20	**Channel ID (CID).** This field specifies the channel address that the initialization or the channel reset operation is initiated.

Bit	Description
19	**Broadcast Address (BA).** 1 = Initialization operation (IOP) is broadcast to all devices. When this bit is set to 1, the DSA field is don't care.
18:10	**Device Register Address (DRA).** This field specifies the register address for the register's read and write operations.
9:5	**Serial Device/Channel Address (SDCA).** This 5-bit field specifies the serial device ID of the Direct RDRAM that the initialization operation is targeted for the next SIO command to be sent by the MCH.
4:0	**Initialization Opcode (IOP).** This field specifies the initialization operation to be done on Direct RDRAM device. 00000 = RDRAM Register Read 00001 = RDRAM Register Write 00010 = RDRAM Set Reset 00011 = Reserved 00100 = RDRAM Set Fast Clock Mode 00101 = RDRAM Temperature Calibrate Enable 00110 = RDRAM Temperature Calibrate 00111 = Reserved 01000 = Reserved 01001 = Reserved 01010 = Reserved 01011 = RDRAM Clear Reset 01100 = Reserved 01101 = Reserved 01110 = Reserved 01111 = Reserved 10000 = RDRAM Current Calibration 10001 = RDRAM SIO Reset 10010 = RDRAM Powerdown Exit 10011 = RDRAM Powerdown Entry 10100 = RDRAM Nap Entry 10101 = RDRAM Nap Exit 10110 = RDRAM Refresh 10111 = RDRAM Precharge 11000 = Manual Current Calibration of MCH RAC 11001 = MCH RAC load RAC A configuration register 11010 = MCH RAC load RAC B configuration register 11011 = Initialize MCH RAC 11100 = MCH RAC Current Calibration 11101 = MCH RAC Thermal Calibration 11110 = Reserved 11111 = PowerUp All Sequence

3.4.22. SMRAM—System Management RAM Control Register (Device 0)

Address Offset: 9Dh
Default Value: 02h
Access: Read/Write, Read Only, Lock
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The open, close, and lock bits function only when G_SMRAME bit is set to a 1. Also, the open bit must be reset before the lock bit is set.

A system device can access the System Management Mode (SMM) space through the graphic aperture GTLB.

Bit	Description
7	Reserved.
6	**SMM Space Open (D_OPEN).** 1 = When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only. 0 = Not open
5	**SMM Space Closed (D_CLS).** 1 = Closed. SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This allows SMM software to reference “through” SMM space to update the display, even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. 0 = Not closed. **Note:** The D_CLS bit only applies to Compatible SMM space.
4	**SMM Space Locked (D_LCK).** 1 = When D_LCK is set to 1, D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become “Read Only”. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function. 0 = Can only be cleared by a Full Reset.
3	**Global SMRAM Enable (G_SMRAME).** 1 = Enable. Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has to be set to 1. 0 = Disable. **Note:** Once D_LCK is set, this bit becomes read only.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG)—RO.** This field indicates the location of SMM space. “SMM DRAM” is not remapped. It is simply “made visible” if the conditions are right to access SMM space; otherwise, the access is forwarded to the hub interface. C_BASE_SEG is hardwired to 010 to indicate that the MCH supports the SMM space at A0000h–BFFFFh.

3.4.23. ESMRAMC—Extended System Management RAM Control Register (Device 0)

Address Offset: 9Eh
Default Value: 38h
Access: Read Only, Read/Write, Read/Write Clear, Lock
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Description
7	**H_SMRAM_EN (H_SMRAME)—R/W.** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB). 1 = When G_SMRAME is 1 and H_SMRAME this bit is 1, the high SMRAM memory space is enabled. SMRAM accesses from FEDA_0000h to FEDB_FFFFh are remapped to DRAM address 000A0000h to 000BFFFFh. **Note:** Once D_LCK is set, this bit becomes read only.
6	**E_SMRAM_ERR (E_SMERR)—R/WC.** 1 = H ost accesses the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with D-OPEN = 0. 0 = It is software's responsibility to clear this bit. Software must write a 1 to this bit to clear it.
5	**SMRAM_Cache (SM_CACHE)—RO.** Hardwired to 1.
4	**SMRAM_L1_EN (SM_L1)—RO.** Hardwired to 1.
3	**SMRAM_L2_EN (SM_L2)—RO.** Hardwired to 1.
2:1	**TSEG_SZ[1–0] (T_SZ)—R/W.** This field selects the size of the TSEG memory block, if enabled (TSEG_EN=1). This memory is taken from the top of DRAM space (i.e., TOM - TSEG_SZ), which is no longer claimed by the memory controller (all accesses to this space are sent to the hub interface if TSEG_EN is set). This field decodes as follows: 00 = (TOM – 128 KB) to TOM 01 = (TOM – 256 KB) to TOM 10 = (TOM – 512 KB) to TOM 11 = (TOM – 1 MB) to TOM **Note:** Once D_LCK is set, this bit becomes read only.
0	**TSEG Enable (TSEG_EN)—R/W.** Enabling of SMRAM memory (TSEG, 128 KB, 256 KB, 512 KB or 1 MB of additional SMRAM memory) for Extended SMRAM space only. 1 = Enable. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. 0 = Disable **Note:** Once D_LCK is set, this bit becomes read only.

3.4.24. ACAPID—AGP Capability Identifier Register (Device 0)

Address Offset: A0–A3h
Default Value: 00200002h
Access: Read Only
Size: 32 bits

This register provides standard identifier for AGP capability.

Bit	Description
31:24	Reserved.
23:20	**Major AGP Revision Number.** These bits provide a major revision number of AGP specification to which this version of MCH conforms. This field is hardwired to a value of 0010b (i.e., implying Rev 2.x).
19:16	**Minor AGP Revision Number.** These bits provide a minor revision number of AGP specification to which this version of MCH conforms. This number is hardwired to a value of 0000 (i.e., implying Rev x.0). Note: Together with major revision number this field identifies MCH as an AGP REV 2.0 compliant device.
15:8	**Next Capability Pointer.** AGP capability is the first and the last capability described via the capability pointer mechanism and, therefore, these bits are hardwired to 0 to indicate the end of the capability linked list.
7:0	**AGP Capability ID.** This field identifies the linked list item as containing AGP registers. This field has a value of 0000_0010b assigned by the PCI SIG.

3.4.25. AGPSTAT—AGP Status Register (Device 0)

Address Offset: A4–A7h
Default Value: 1F000217h
Access: Read Only
Size: 32 bits

This register reports AGP device capability/status.

Bit	Description
31:24	**Requests (RQ).** This field is hardwired to 1Fh to indicate a maximum of 32 outstanding AGP command requests can be handled by the MCH. This field contains the maximum number of AGP command requests the MCH is configured to manage. Default =1Fh to allow a maximum of 32 outstanding AGP command requests.
23:10	Reserved.
9	**Side Band Addressing (SBA).** Hardwired to a 1.This bit indicates that the MCH supports side band addressing.
8:6	Reserved.
5	**Greater Than 4 GB Addressing (4GB).** Hardwired to 0. The MCH does not support addresses greater than 4 GB
4	**Fast Writes (FW).** Hardwired to a 1.This bit indicates that the MCH supports fast writes from the host to the AGP master.
3	Reserved.
2:0	**RATE.** After reset the MCH reports its data transfer rate capability. Bit 0 identifies if AGP device supports 1X data transfer mode, bit 1 identifies if AGP device supports 2X data transfer mode, bit 2 identifies if AGP device supports 4X data transfer mode. 111 = MCH supports 1X, 2X, and 4X data transfer modes (Default) **Note:** The selected data transfer mode applies to both AD bus and SBA bus. It also applies to fast writes, if they are enabled.

3.4.26. AGPCMD—AGP Command Register (Device 0)

Address Offset: A8–ABh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides control of the AGP operational parameters.

Bit	Description
31:10	Reserved.
9	**Side Band Addressing Enable (SBA_EN).** 1 = Enable 0 = Disable
8	**AGP Enable.** When this bit is 0, the MCH ignores all AGP operations, including the sync cycle. Any AGP operations received while this bit is set to 1 will be serviced, even if this bit is reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1X mode, the command will be issued. When this bit is 1, the MCH responds to AGP operations delivered via PIPE#, or to operations delivered via SBA (if SBA_EN=1) 1 = Enable 0 = Disable
7:6	Reserved.
5	**Greater Than 4 GB Addressing Enable (4GB_EN).** Hardwired to 0. The MCH as an AGP target does not support addressing greater than 4 GB.
4	**Fast Write Enable (FW_EN).** 1 = MCH uses fast write protocol for memory write transactions from the MCH to the AGP master. Fast writes will occur at the data transfer rate selected by the data rate bits (2:0) in this register. When this bit is cleared, or when the data rate bits are set to 1X mode, the memory write transactions from the MCH to the AGP master use standard PCI protocol. 0 = Disable
3	Reserved.
2:0	**Data Rate.** The settings of these bits determine the AGP data transfer rate. One (*and only one*) bit in this field must be set to indicate the desired data transfer rate. The same bit must be set on both master and target. Bit 0 = 1X Bit 1 = 2X Bit 2 = 4X Configuration software updates this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP masters' configuration space.) **Note:** This field applies to AD and SBA buses. It also applies to fast writes if they are enabled.

3.4.27. AGPCTRL—AGP Control Register

Address Offset: B0–B3h
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides for additional control of the AGP interface.

Bit	Description
31:8	Reserved.
7	**GTLB Enable (and GTLB Flush Control).** 1 = Enable. This selects normal operations of the Graphics Translation Lookaside Buffer. 0 = Disable. GTLB is flushed by clearing the valid bits associated with each entry. (Default)
6:0	Reserved.

3.4.28. APSIZE—Aperture Size (Device 0)

Address Offset: B4h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register determines the effective size of the Graphics Aperture used for a particular MCH configuration. This register can be updated by the MCH specific BIOS configuration sequence before the PCI standard bus enumeration sequence takes place. If the register is not updated, a default value selects an aperture of maximum size (i.e., 256 MB). The size of the table that corresponds to a 256 MB aperture is not practical for most applications; therefore, these bits must be programmed to a smaller practical value that will force adequate address range to be requested via the APBASE register from the PCI configuration software.

Bit	Description
7:6	Reserved.
5:0	**Graphics Aperture Size (APSIZE).** Each bit in APSIZE[5:0] operates on similarly ordered bits in APBASE[27:22] of the Aperture Base configuration register. When a particular bit of this field is 0, it forces the similarly ordered bit in APBASE[27:22] to behave as “hardwired” to 0. When a particular bit of this field is set to 1, it allows corresponding bit of the APBASE[27:22] to be read/write accessible. Only the following combinations are allowed: 11 1111 = 4 MB 11 1110 = 8 MB 11 1100 = 16 MB 11 1000 = 32 MB 11 0000 = 64 MB 10 0000 = 128 MB 00 0000 = 256 MB Default for APSIZE[5:0]=000000b forces default APBASE[27:22] =000000b (i.e., all bits respond as “hardwired” to 0). This provides a maximum aperture size of 256 MB. As another example, programming APSIZE[5:0]=111000b hardwires APBASE[24:22]=000b and while enabling APBASE[27:25] as read/write programmable.

3.4.29. ATTBASE—Aperture Translation Table Base Register (Device 0)

Address Offset: B8–BBh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table Base located in main memory (DRAM). This value is used by the MCH Graphics Aperture address translation logic (including the GTLB logic) to obtain the appropriate address translation entry required during the translation of the aperture address into a corresponding physical DRAM address. The ATTBASE register may be dynamically changed.

The address provided via ATTBASE is 4-KB aligned.

Bit	Description
31:12	**Aperture Translation Table Base Address (ATT_BA).** This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory. **Note:** This field should be modified only when the GTLB has been disabled.
11:0	Reserved.

3.4.30. AMTT—AGP Interface Multi-Transaction Timer Register (Device 0)

Address Offset: BCh
Default Value: 00h
Access: Read/Write
Size: 8 bits

AMTT is an 8-bit register that controls the amount of time that the MCH arbiter allows AGP master to perform multiple back-to-back transactions. The MCH AMTT mechanism is used to optimize the performance of the AGP master (using PCI protocol) that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers). The AMTT mechanism applies to the host-AGP transactions as well, and it guarantees to the processor a fair share of the AGP interface bandwidth.

The number of clocks programmed in the AMTT represents the guaranteed time slice (measured in 66 MHz clocks) allotted to the current agent (either AGP master or Host bridge) after which the AGP arbiter will grant the bus to another agent. The default value of AMTT is 00h and disables this function. The AMTT value can be programmed with 8-clock granularity. For example, if AMTT is programmed to 18h, the selected value corresponds to the time period of 24 AGP (66 MHz) clocks.

Bit	Description
7:3	**Multi-Transaction Timer Count Value.** The number programmed in these bits represents the guaranteed time slice (measured in eight 66 MHz clock granularity) allotted to the current agent (either AGP master or MCH) after which the AGP arbiter will grant the bus to another agent.
2:0	Reserved.

3.4.31. LPTT—Low Priority Transaction Timer Register (Device 0)

Address Offset: BDh
Default Value: 00h
Access: Read/Write
Size: 8 bits

LPTT is an 8-bit register similar in a function to AMTT. This register is used to control the minimum tenure on the AGP for low priority data transactions (both reads and writes) issued using PIPE# or SB mechanisms.

The number of clocks programmed in the LPTT represents the guaranteed time slice (measured in 66 MHz clocks) allotted to the current low priority AGP transaction data transfer state. This does not necessarily apply to a single transaction but it can span over multiple low-priority transactions of the same type. After this time expires, the AGP arbiter may grant the bus to another agent, if there is a pending request. The LPTT does not apply in the case of high-priority request where ownership is transferred directly to the high-priority requesting queue. The default value of LPTT is 00h and disables this function. The LPTT value can be programmed with 8-clock granularity. For example, if LPTT is programmed to 10h, the selected value corresponds to the time period of 16 AGP (66 MHz) clocks.

Bit	Description
7:3	**Low Priority Transaction Timer Count Value.** The number of clocks programmed in these bits represents the guaranteed time slice (measured in eight 66 MHz clock granularity) allotted to the current low priority AGP transaction data transfer state.
2:0	Reserved.

3.4.32. RDTR—RDRAM* Timing Register (Device 0)

Address Offset: BEh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This 8-bit register defines the timing parameters for all devices in the Direct RDRAM channel. BIOS programs this register with the "least common denominator" values after reading configuration registers of each device in the Direct RDRAM channel. This register applies to the entire DRAM array.

Bit	Description
7:6	**Row to Column Delay (tRCD).** This field defines the minimum interval between opening a row and column operation on that row in units of Direct Rambus* clocks. 00 = Reserved 01 = 7 Rclks 10 = 9 Rclks 11 = Reserved
5	Reserved.
4:0	**RDRAM Total CAS Access Delay (tRDRAM).** This field defines the minimum round trip propagation time of the RDRAM channel in units of RDRAM clocks. This value includes the CAS access time and the channel delay time. tRDRAM = tCAC + tRDLY • tRDRAM has a minimum value of 8 Rclks since the supported RDRAM tCAC = 8 Rclks. • tRDLY is the total channel delay time and should include the channel delay time of the RDRAM device in the MCH RDRAM interface.

Table 9. Valid tRCD and tCAC Combinations for 400 MHz System Bus (Intel® 82850 MCH)

RDRAM* Frequency (Rclk)	TRCD in Rclks	tCAC in Rclks
400 MHz	9	8
400 MHz	7	8
300 MHz	7	8

Table 10. Valid tRCD and tCAC Combinations for 533 MHz System Bus (Intel® 82850E MCH)

RDRAM* Frequency (Rclk)	TRCD in Rclks	tCAC in Rclks
533 MHz	9	8
400 MHz	7	8

3.4.33. TOM—Top of Low Memory Register (Device 0)

Address Offset: C4h
Default Value: 0100h
Access: Read/Write
Size: 16 bits

A memory hole is present under normal operating conditions from TOM to the 4 GB address where TOM is the Top Of Lower Memory register. This hole is used to access devices present behind the hub interface, the AGP bus, the memory-mapped APIC register, and the boot BIOS area just below 4 GB. If the total amount of main memory is less than 4 GB, the addresses (i.e., not their *'values'*) indicated by the TOM and GBA15 (or TOM and SRBA7) registers will be identical.

This register must be set to a value of 0100h (16 MB) or greater.

Bit	Description
15:4	**Top of Low Memory (TOLM).** This register contains the address that corresponds to bits 31:20 (1 MB granularity) of the maximum DRAM memory address that lies below 4 B. Configuration software should set this value to either the maximum amount of memory in the system or to the minimum address allocated for PCI memory or the graphics aperture, whichever is smaller. **Programming example:** C00h = 3 GB (assuming that GAR15 is set > 4 GB) • An access to 0_C000_0000h or above (but <4 GB) will be considered above the TOLM; therefore, not to DRAM. It will go to AGP or will be subtractively decoded to the hub interface. • An access to 0_BFFF_FFFFh and below will be considered below the TOLM and go to DRAM. **Note:** Locked accesses that cross TOM are illegal and should not be performed.
3:0	Reserved.

3.4.34. ERRSTS—Error Status Register (Device 0)

Address Offset: C8–C9h
Default Value: 0000h
Access: Read/Write Clear
Size: 16 bits

This register is used to report various error conditions via the hub interface messages to ICH2. An, SERR, SMI, or SCI error message may be generated via the hub interface on a zero to one transition of any of these flags when enabled in the PCICMD/ERRCMD, SMICMD, or SCICMD registers respectively. These bits are set regardless of whether or not the SERR is enabled and generated.

Bit	Description
15:12	Reserved.
11	**RDRAM Thermal Sensor Trip (RDTST).** 1 = MCH detected a tripped thermal sensor in a RDRAM device. 0 = Software must write a 1 to clear this bit.
10	Reserved.

Bit	Description
9	**LOCK to non-DRAM Memory Flag (LCKF).** 1 = A host initiated LOCK cycle targeting non-DRAM memory space occurred. 0 = Software must write a 1 to clear this bit.
8:7	Reserved.
6	**SERR on Hub Interface Target Abort (TAHLA).** 1 = MCH detected that an MCH originated hub interface cycle was terminated with a Target Abort completion packet or special cycle. 0 = Software must write a 1 to clear this bit.
5	**MCH Detects Unimplemented Hub Interface Special Cycle (HIAUSC).** 1 = MCH detected an Unimplemented Special Cycle on the hub interface. 0 = Software must write a 1 to clear this bit.
4	**AGP Access Outside of Graphics Aperture Flag (OOGF).** 1 = An AGP access occurred to an address that is outside of the graphics aperture range. 0 = Software must write a 1 to clear this bit.
3	**Invalid AGP Access Flag (IAAF).** 1 = An AGP access was attempted outside of the graphics aperture and either to the 640 KB – 1 MB range or above the top of memory. 0 = Software must write a 1 to clear this bit.
2	**Invalid Graphics Aperture Translation Table Entry (ITTEF).** 1 = An invalid translation table entry was returned in response to an AGP access to the graphics aperture. 0 = Software must write a 1 to clear this bit.
1	**Multiple-bit DRAM ECC Error Flag (DMERR).** 1 = A memory read data transfer had an uncorrectable multiple-bit error. The address, channel number, and device number that caused the error are logged in the EAP register. The EAP, CN, DN, and ES fields are locked until the processor clears this bit by writing a 1. Software uses bits [1:0] to detect whether the logged error address is for Single or Multiple-bit error. 0 = Once software completes the error processing, a value of 1 is written to this bit field to clear the value (back to 0) and unlock the error logging mechanism.
0	**Single-bit DRAM ECC Error Flag (DSERR).** 1 = A memory read data transfer had a single-bit correctable error and the corrected data was sent for the access. The address, channel number, and device number that caused the error are logged in the EAP register. The EAP, CN, DN, and ES fields are locked to further single bit error updates until the processor clears this bit by writing a 1. A multiple bit error that occurs after this bit is set will overwrite the EAP, CN, and DN fields with the multiple bit error signature and the MEF bit will also be set. 0 = Software must write a 1 to clear this bit and unlock the error logging mechanism.

3.4.35. ERRCMD—Error Command Register (Device 0)

Address Offset: CA–CBh
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register enables various errors to generate a SERR message via the hub interface. Since the MCH does not have an SERR# signal, SERR messages are passed from the MCH to the ICH2 over the hub interface. When a bit in this register is set, a SERR message will be generated on the hub interface when the corresponding flag is set in the ERRSTS register. *The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.*

An error can generate one and only one error message via the hub interface. It is software's responsibility to make sure that when an SERR error message is enabled for an error condition, SMI and SCI error messages are disabled for that same error condition.

Bit	Description
15:12	Reserved.
11	**SERR on RDRAM Thermal Sensor Trip (ETST).** 1 = Enable. MCH generates a hub interface SERR special cycle when a RDRAM thermal sensor is found tripped. 0 = Disable
10	Reserved.
9	**SERR on Non-DRAM Lock (LCKERR).** 1 = Enable. MCH generates a hub interface SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM. 0 = Disable
8:7	Reserved.
6	**SERR on Target Abort on Hub Interface Exception (TAHLA_SERR).** 1 = Enable. Hub interface SERR message is enabled when an MCH originated hub interface cycle is completed with "Target Abort" completion packet or special cycle status. 0 = Disable
5	**SERR on Detecting Hub Interface Unimplemented Special Cycle (HIAUSCERR).** 1 = Enable. MCH generates an SERR message over hub interface when an Unimplemented Special Cycle is received on the hub interface. 0 = Disable. MCH does not generate an SERR message for this event. SERR messaging for Device 0 is globally enabled in the PCICMD register.
4	**SERR on AGP Access Outside of Graphics Aperture (OOGF_SERR).** 1 = Enable. Hub interface SERR message is enabled when an AGP access occurs to an address outside of the graphics aperture. 0 = Disable

Bit	Description
3	**SERR on Invalid AGP Access (IAAF_SERR).** 1 = Enable. Hub interface SERR message is enabled when an AGP access occurs to an address outside of the graphics aperture and either to the 640 KB – 1 MB range or above the top of memory. 0 = Disable
2	**SERR on Invalid Translation Table Entry (ITTEF_SERR).** 1 = Enable. Hub interface SERR message is enabled when an invalid translation table entry is returned in response to an AGP access to the graphics aperture. 0 = Disable
1	**SERR Multiple-Bit DRAM ECC Error (DMERR_SERR).** 1 = Enable. Hub interface SERR message is enabled when the MCH detects a multiple-bit error. 0 = Disable. For systems not supporting ECC, this bit must be disabled.
0	**SERR on Single-bit ECC Error (DSERR).** 1 = Enable. Hub interface SERR message is enabled when the MCH detects a single bit error. 0 = Disable. For systems that do not support ECC, this bit must be disabled.

3.4.36. SMICMD—SMI Command Register (Device 0)

Address Offset: CC–CDh
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register enables various errors to generate a SMI message via the hub interface.

An error can generate one and only one error message via the hub interface. It is software's responsibility to make sure that when an SMI error message is enabled for an error condition, SERR and SCI error messages are disabled for that same error condition.

Bit	Description
15:2	Reserved.
1	**SMI on Multiple-Bit DRAM ECC Error (DMERR_SMI).** 1 = Hub interface SMI message is enabled when the MCH detects a multiple-bit error. 0 = For systems not supporting ECC, this bit must be disabled.
0	**SMI on Single-bit ECC Error (DSERR_SMI).** 1 = Hub interface SMI message is enabled when the MCH detects a single bit error. 0 = For systems that do not support ECC, this bit must be disabled.

3.4.37. SCICMD—SCI Command Register (Device 0)

Address Offset: CE–CFh
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register enables various errors to generate a SCI message via the hub interface. An error can generate one and only one error message via the hub interface. It is software's responsibility to make sure that when an SCI error message is enabled for an error condition, SERR and SMI error messages are disabled for that same error condition.

Bit	Description
15:2	Reserved.
1	**SCI on Multiple-Bit DRAM ECC Error (DMERR_SCI).** 1 = Hub interface SCI message is enabled when the MCHDRAM controller detects a multiple-bit error. 0 = For systems not supporting ECC, this bit must be disabled.
0	**SCI on Single-bit ECC Error (DSERR_SCI).** 1 = Hub interface SCI message is enabled when the MCH DRAM controller detects a single bit error. 0 = For systems that do not support ECC, this bit must be disabled.

3.4.38. DRAMRC—RDRAM* Refresh Control Register (Device 0)

Address Offset: DC–DDh
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register is loaded by configuration software with the refresh timings for all RDRAM channels present in the system. The value placed into this register should represent the least common denominator of all of the devices on the specified channel pair.

The refresh rate for a channel is programmed to that of the device with the fastest refresh rate on that channel. That is, if a channel has a mix of 128 Mbit (3.9 µs) and 256 Mbit (1.95 µs) technology devices, the refresh rate for the channel will be programmed to 1.95 µs.

Bit	Description
15:3	Reserved.
2:0	**DRAM Refresh Rate RDRAM channel pair #0 (DRR0).** The DRAM refresh rate is adjusted according to the frequency selected by this field. Note that refresh is also disabled via this field, and that disabling refresh results in the eventual loss of DRAM data. This field is programmed by BIOS after collecting configuration information from all Direct RDRAM devices in the channel and determining the least common denominator value for refresh. 000 = Refresh Disabled 001 = 1.95 µs 010 = 3.9 µs 011 – 111 = Reserved

3.4.39. SKPD—Scratchpad Data (Device 0)

Address Offset: DE–DFh
Default Value: 0000h
Access: Read/Write
Size: 16 bits

it	Description
15:0	**Scratchpad [15:0].** These bits are simply R/W storage bits that have no effect on the MCH functionality.

3.4.40. DERRCTL_STS—DRAM Error Control/Status Register (Device 0)

Address Offset: E2–E3h
Default Value: 0000h
Access: Read Only
Size: 16 bits

This register enables and reflects the status of various errors checking functions that the MCH supports on the DRAM interface.

Bit	Description
15:8	Reserved.
7:0	**DRAM ECC Syndrome (DECCSYN).** After a DRAM ECC error, hardware loads this field with a syndrome describing the set of bits found to be in error. This field is locked from the time it is loaded until the time when the error flag is cleared by software. If the first error was a single bit correctable error; then a subsequent multiple bit error overwrites this field. In all other cases, an error that occurs after the first error and before the error flag has been cleared by software will escape recording.

3.4.41. EAP—Error Address Pointer Register (Device 0)

Address Offset: E4–E7h
Default Value: 0000h
Access: Read Only
Size: 32 bits

This register stores the DRAM address when an ECC error occurs.

Bit	Description
31:11	**Error Address Pointer (EAP).** This field is used to store the 4 KB block of main memory of which an error (single bit or multi-bit error) has occurred. Note that the value of this field represents the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and does not change as a result of a new error.
10:1	Reserved.
0	**Error Address Segment (EAS).** This bit indicates whether the reported error was found on RDRAM channel 0 or on channel 1. 1 = RDRAM Channel 1 0 = RDRAM Channel 0

3.4.42. MISC_CNTL—Miscellaneous Control Register (Device 0)

Address Offset: F4–F7h
Default: 0000F874h
Default: R/W
Size 32 bits

Bit	Description
31:22	Reserved.
21	**Write Combining Disable (PCIBWCD).** 1 = Disable. Write combining is disabled for host bus writes targeting AGP (depends on configuration). Write combining should not be used. Bit 21 should be set to “1”. 0 = Enable.
20:0	Reserved.

3.5. AGP Bridge Registers (Device 1)

Table 11 below summarizes the MCH configuration space for device 1.

Table 11. AGP Bridge Register Address Map (Device 1)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	2532h	RO
04–05h	PCICMD1	PCI Command Register	0000h	RO, R/W
06–07h	PCISTS1	PCI Status Register	00A0h	RO, R/WC
08h	RID1	Revision Identification	02h	RO
09h	—	Reserved	—	—
0Ah	SUBC1	Sub-Class Code	04h	RO
0Bh	BCC1	Base Class Code	06h	RO
0Ch	—	Reserved	—	—
0Dh	MLT1	Master Latency Timer	00h	R/W
0Eh	HDR1	Header Type	01h	RO
0F–17h	—	Reserved	—	—
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	R/W
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh	SMLT1	Secondary Bus Master Latency Timer	00h	R/W
1Ch	IOBASE1	I/O Base Address Register	F0h	R/W
1Dh	IOLIMIT1	I/O Limit Address Register	00h	R/W
1E–1Fh	SSTS1	Secondary Status Register	02A0h	RO, R/WC
20–21h	MBASE1	Memory Base Address Register	FFF0h	R/W
22–23h	MLIMIT1	Memory Limit Address Register	0000h	R/W
24–25h	PMBASE1	Prefetchable Memory Base Address Reg.	FFF0h	R/W
26–27h	PMLIMIT1	Prefetchable Memory Limit Address Reg.	0000h	R/W
28–3Dh	—	Reserved	—	—
3Eh	BCTRL1	Bridge Control Register	00h	R/W
3Fh	—	Reserved	—	—
40h	ERRCMD1	Error Command	00h	R/W
41–FFh	—	Reserved	—	—

3.5.1. VID1—Vendor Identification Register (Device 1)

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number**. This is a 16-bit value assigned to Intel. Intel VID = 8086h.

3.5.2. DID1—Device Identification Register (Device 1)

Address Offset: 02–03h
Default Value: 2532h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number**. This is a 16-bit value assigned to the MCH Device 1. MCH Device 1 DID =2532h.

3.5.3. PCICMD1—PCI-PCI Command Register (Device 1)

Address Offset: 04–05h
Default: 0000h
Access: Read Only, Read/Write
Size 16 bits

Bit	Descriptions
15:10	Reserved.
9	**Fast Back-to-Back—RO.** Not Applicable. Hardwired to 0.
8	**SERR Message Enable (SERRE1)—R/W.** This bit is a global enable bit for Device 1 SERR messaging. The MCH does not have an SERR# signal. The MCH communicates the SERR# condition by sending an SERR message to the ICH2. 1 = The MCH is enabled to generate SERR messages over the hub interface for specific Device 1 error conditions that are individually enabled in the BCTRL register. The error status is reported in the PCISTS1 register. 0 = SERR message is not generated by the MCH for Device 1. **NOTE:** This bit only controls SERR messaging for the Device 1. Device 0 has its own SERRE bit to control error reporting for error conditions occurring on Device 0.
7	**Address/Data Stepping—RO.** Not applicable. Hardwired to 0.
6	**Parity Error Enable (PERRE1)—RO.** Hardwired to 0. Parity checking is not supported on the primary side of this device.
5	Reserved.
4	**Memory Write and Invalidate Enable—RO.** Hardwired to 0.
3	**Special Cycle Enable—RO.** Hardwired to 0.
2	**Bus Master Enable (BME1)—R/W.** This bit is not functional. It is a R/W bit for compatibility with compliance testing software.
1	**Memory Access Enable (MAE1)—R/W.** 1 = Enable. This bit must be set to 1 to enable the Memory and Prefetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers. 0 = Disable. All of Device 1's memory space is disabled.
0	**I/O Access Enable (IOAE1)—R/W.** 1 = Enable. This bit must be set to1 to enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers. 0 = All of Device 1's I/O space is disabled.

3.5.4. PCISTS1—PCI-PCI Status Register (Device 1)

Address Offset: 06–07h
Default Value: 00A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the "virtual" PCI-to-PCI bridge in the MCH. Since this device does not physically reside on PCI_A it reports the optimum operating conditions so that it does not restrict the capability of PCI_A.

Bit	Descriptions
15	**Detected Parity Error (DPE1)—RO.** Not Applicable. Hardwired to 0.
14	**Signaled System Error (SSE1)—R/WC.** 1 = MCH Device 1 generates an SERR message over the hub interface for any enabled Device 1 error condition. Device 1 error conditions are enabled in the ERRCMD, PCICMD1 and BCTRL1 registers. Device 1 error flags are read/reset from the ERRSTS and SSTS1 register. 0 = Software clears this bit by writing a 1 to it.
13	**Received Master Abort Status (RMAS1)—RO.** Not Applicable. Hardwired to 0.
12	**Received Target Abort Status (RTAS1)—RO.** Not Applicable. Hardwired to 0.
11	**Signaled Target Abort Status (STAS1)—RO.** Not Applicable. Hardwired to 0.
10:9	**DEVSEL# Timing (DEVT1).** This bit field is hardwired to "00b" to indicate that the Device 1 uses the fastest possible decode.
8	**Data Parity Detected (DPD1)—RO.** Not Applicable. Hardwired to 0.
7	**Fast Back-to-Back (FB2B1)—RO.** This bit is hardwired to 1 to indicate that the AGP port always supports fast back to back transactions.
6	Reserved.
5	**66 MHz Capability—RO.** This bit is hardwired to 1 to indicate that the AGP port is 66 MHz capable.
4:0	Reserved.

3.5.5. RID1—Revision Identification Register (Device 1)

Address Offset: 08h
Default Value: 02h
Access: Read Only
Size: 8 bits

This register contains the revision number of the MCH Device 1. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number**. This is an 8-bit value that indicates the revision identification number for the MCH Device 1. A-2 Stepping = 02h. Refer to the latest Specification Update for the most current information.

3.5.6. SUBC1—Sub-Class Code Register (Device 1)

Address Offset: 0Ah
Default Value: 04h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the MCH Device 1.

Bit	Description
7:0	**Sub-Class Code (SUBC1)**. This is an 8-bit value that indicates the category of bridge for the MCH. 04h = PCI-to-PCI Host Bridge.

3.5.7. BCC1—Base Class Code Register (Device 1)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the MCH Device 1.

Bit	Description
7:0	**Base Class Code (BASEC)**. This is an 8-bit value that indicates the Base Class Code for the MCH Device 1. 06h = Bridge device.

3.5.8. MLT1—Master Latency Timer Register (Device 1)

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to prevent standard PCI-to-PCI bridge configuration software from getting “confused”.

Bit	Description
7:3	**Not applicable but support read/write operations.** Reads return previously written data.
2:0	Reserved.

3.5.9. HDR1—Header Type Register (Device 1)

Offset: 0Eh
Default: 01h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	This read only field always returns 01h when read. Writes have no effect.

3.5.10. PBUSN1—Primary Bus Number Register (Device 1)

Offset: 18h
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies that “virtual” PCI-to-PCI bridge is connected to Bus 0.

Bit	Descriptions
7:0	**Bus Number.** Hardwired to 0.

3.5.11. SBUSN1—Secondary Bus Number Register (Device 1)

Offset: 19h
Default: 00h
Access: Read /Write
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” PCI-to-PCI bridge (i.e., to AGP). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	**Bus Number.** Programmable. Default = 00h.

3.5.12. SUBUSN1—Subordinate Bus Number Register (Device 1)

Offset: 1Ah
Default: 00h
Access: Read /Write
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	**Bus Number.** Programmable. Default = 0

3.5.13. SMLT1—Secondary Master Latency Timer Register (Device 1)

Address Offset: 1Bh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register controls the bus tenure of the MCH on AGP. MLT is an 8-bit register that controls the amount of time the MCH, as an AGP/PCI bus master, can burst data on the AGP Bus. The count value is an 8-bit quantity; however, MLT[2:0] are reserved and assumed to be 0 when determining the count value. The MCH's MLT is used to guarantee to the AGP master a minimum amount of the system resources. When the MCH begins the first AGP FRAME# cycle after being granted the bus, the counter is loaded and enabled to count from the assertion of FRAME#. If the count expires while the MCH's grant is removed (due to AGP master request), the MCH will lose the use of the bus, and the AGP master agent may be granted the bus. If MCH's bus grant is not removed, the MCH continues to own the AGP bus, regardless of the MLT expiration or idle condition. Note that the MCH must always properly terminate an AGP transaction with FRAME# negation prior to the final data transfer.

The number of clocks programmed in the MLT represents the guaranteed time slice (measured in 66 MHz AGP clocks) allotted to the MCH, after which it must complete the current data transfer phase and then surrender the bus as soon as its bus grant is removed. For example, if the MLT is programmed to 18h, the value is 24 AGP clocks. The default value of MLT is 00h and disables this function. When the MLT is disabled, the burst time for the MCH is unlimited (i.e., the MCH can burst forever).

Bit	Description
7:3	**Secondary MLT Counter Value.** Default=0 (i.e., SMLT disabled)
2:0	Reserved.

3.5.14. IOBASE1—I/O Base Address Register (Device 1)

Address Offset: 1Ch
Default Value: F0h
Access: Read/Write
Size: 8 bits

This register controls the host-to-AGP I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4 KB boundary.

BIOS must not set this register to 00h; otherwise, 0CF8h/0CFCh accesses will be forwarded to AGP.

Bit	Description
7:4	**I/O Address Base.** Corresponds to A[15:12] of the I/O address. Default=F0h
3:0	Reserved.

3.5.15. IOLIMIT1—I/O Limit Address Register (Device 1)

Address Offset: 1Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register controls the hosts to AGP I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4 KB aligned address block.

Bit	Description
7:4	**I/O Address Limit.** Corresponds to A[15:12] of the I/O address. Default=0
3:0	Reserved.

3.5.16. SSTS1—Secondary PCI-PCI Status Register (Device 1)

Address Offset: 1E–1Fh
Default Value: 02A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with the secondary side (i.e., AGP side) of the "virtual" PCI-to-PCI bridge in the MCH.

Bit	Descriptions
15	**Detected Parity Error (DPE1)—R/WC.** 1 = MCH detected a parity error in the address or data phase of AGP bus transactions. 0 = Software sets DPE1 to 0 by writing a 1 to this bit.
14	Reserved.
13	**Received Master Abort Status (RMAS1)—R/WC.** 1 = MCH terminated a Host-to-AGP with an unexpected master abort. 0 = Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS1)—R/WC.** 1 = An MCH-initiated transaction on AGP is terminated with a target abort. 0 = Software resets RTAS1 to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS1)—RO.** Hardwired to a 0. The MCH does not generate target abort on AGP.
10:9	**DEVSEL# Timing (DEVT1)—RO.** This 2-bit field indicates the timing of the DEVSEL# signal when the MCH responds as a target on AGP, and is hardwired to the value 01b (medium) to indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle.
8	**Master Data Parity Error Detected (DPD1)—RO.** Hardwired to 0. MCH does not implement G_PERR# signal.
7	**Fast Back-to-Back (FB2B1)—RO.** Hardwired to 1. MCH as a target supports fast back-to-back transactions on AGP.
6	Reserved.
5	**66 MHz Capable (CAP66)—RO.** Hardwired to 1. AGP bus is capable of 66 MHz operation.
4:0	Reserved.

3.5.17. MBASE1—Memory Base Address Register (Device 1)

Address Offset: 20–21h
Default Value: FFF0h
Access: Read/Write
Size: 16 bits

This register controls the host to AGP non-prefetchable memory accesses routing based on the following formula:

MEMORY_BASE1 ≤ address ≤ MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range is aligned to a 1 MB boundary.

Bit	Description
15: 4	**Memory Address Base 1 (MEM_BASE1).** Corresponds to A[31:20] of the memory address.
3:0	Reserved.

3.5.18. MLIMIT1—Memory Limit Address Register (Device 1)

Address Offset: 22–23h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register controls the host to AGP non-prefetchable memory accesses routing based on the following formula:

MEMORY_BASE1 ≤ address ≤ MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

The memory range covered by MBASE1 and MLIMIT1 registers are used to map non-prefetchable AGP address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE 1and PMLIMIT1 are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved host-AGP memory access performance.

Bit	Description
15: 4	**Memory Address Limit 1(MEM_LIMIT1).** Corresponds to A[31:20] of the memory address. Default=0
3:0	Reserved.

3.5.19. PMBASE1—Prefetchable Memory Base Address Register (Device 1)

Address Offset: 24–25h
Default Value: FFF0h
Access: Read/Write
Size: 16 bits

This register controls the host to AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE1 ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Prefetchable Memory Address Base 1(PMEM_BASE1).** Corresponds to A[31:20] of the memory address.
3:0	Reserved.

3.5.20. PMLIMIT1—Prefetchable Memory Limit Address Register (Device 1)

Address Offset: 26–27h
Default Value: 0000h
Access: Read/Write, Read Only
Size: 16 bits

This register controls the host to AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE1 ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Description
15:4	**Prefetchable Memory Address Limit 1(PMEM_LIMIT1).** Corresponds to A[31:20] of the memory address. Default=0
3:0	Reserved.

3.5.21. BCTRL1—PCI-to-PCI Bridge Control Register (Device 1)

Address Offset: 3Eh
Default: 00h
Access: Read Only, Read/Write
Size 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., AGP) as well as some bits that affect the overall behavior of the "virtual" PCI-to-PCI bridge embedded within MCH (e.g., VGA compatible address ranges mapping).

Bit	Descriptions
7	**Fast Back to Back Enable—RO.** Hardwired to 0. Since there is only one target allowed on AGP, this bit is meaningless. The MCH will not generate FB2B cycles in 1X mode, but will generate FB2B cycles in 2X and 4X fast write modes.
6	**Secondary Bus Reset—RO.** Hardwired to 0. MCH does not support generation of reset via this bit on the AGP. Note: The only way to perform a hard reset of the AGP is via the system reset either initiated by software or hardware via ICH2.
5	**Master Abort Mode—RO.** Hardwired to 0. This means that when acting as a master on AGP, the MCH discards data on writes and returns all 1s during reads when a Master Abort occurs.
4	Reserved.
3	**VGA Enable (VGAEN1)—R/W.** Controls the routing of host-initiated transactions targeting VGA compatible I/O and memory address ranges. 1 = MCH forwards the following host accesses to the AGP: • Memory accesses in the range 0A0000h to 0BFFFFh • I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded) When this bit is set, forwarding of these accesses issued by the host is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers. Forwarding of these accesses is also independent of the settings of bit 2 (ISA Enable) of this register if this bit is 1. 0 = VGA compatible memory and I/O range accesses are not forwarded to AGP; rather, they are mapped to primary PCI unless they are mapped to AGP via I/O and memory range registers defined above (IOBASE1, IOLIMIT1, MBASE1, MLIMIT1, PMBASE1, PMLIMIT1) Refer to the System Address Map chapter of this document for further information. **NOTES:** • Only one of Device 1–5's VGAEN bits is allowed to be set. This must be enforced via software. • If this bit is set, ISA Enable (bit 2) must also be set.
2	**ISA Enable—R/W.** This bit modifies the response by the MCH to an I/O access issued by the host that targets ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 1 = MCH does not forward to AGP any I/O transactions addressing the last 768 bytes in each 1 KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to AGP, these cycles are forwarded to PCI0 where they can be subtractively or positively claimed by the ISA bridge. 0 = All addresses defined by the IOBASE and IOLIMIT for host I/O transactions will be mapped to AGP. (Default)

Bit	Descriptions
1	Reserved.
0	**Parity Error Response Enable—R/W.** Controls MCH's response to data phase parity errors on AGP. Note that G_PERR# is not implemented by the MCH. 1 = Address and data parity errors detected on AGP are reported via the hub interface SERR# messaging mechanism, if further enabled by SERRE1. 0 = Address and data parity errors on AGP are not reported via the MCH hub interface SERR# messaging mechanism. Other types of error conditions can still be signaled via SERR# messaging independent of this bit's state.

3.5.22. ERRCMD1—Error Command Register (Device 1)

Address Offset: 40h
Default Value: 00h
Access: Read/Write
Size: 8 bits

Bit	Description
7:1	Reserved.
0	**SERR on Receiving Target Abort (SERTA).** 1 = MCH generates an SERR message over the hub interface upon receiving a target abort on AGP. SERR messaging for Device 1 is globally enabled in the PCICMD1 register. 0 = MCH does not assert an SERR message upon receipt of a target abort on AGP.

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4. System Address Map

A system based on the 82850 MCH or 82850E MCH supports 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. The I/O and memory spaces are divided by system configuration software into regions. The memory ranges are useful either as system memory or as specialized memory, while the I/O regions are used solely to control the operation of devices in the system.

When the MCH receives a write request whose address targets an invalid space, the data is ignored. For reads, the MCH respond by returning all zeros on the requesting interface.

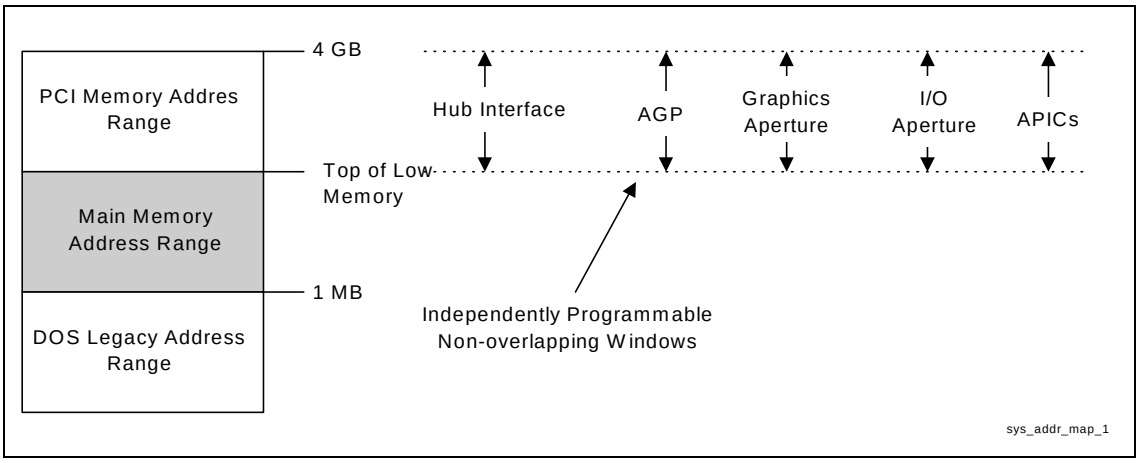
4.1. Memory Address Ranges

The system memory map is broken into two categories:

Extended Memory Range (1 MB to 4GB): The first is extended memory, existing between 1 MB and 4 GB. It contains a 32-bit memory space, which is used for mapping PCI, AGP, APIC, SMRAM, and BIOS memory spaces.

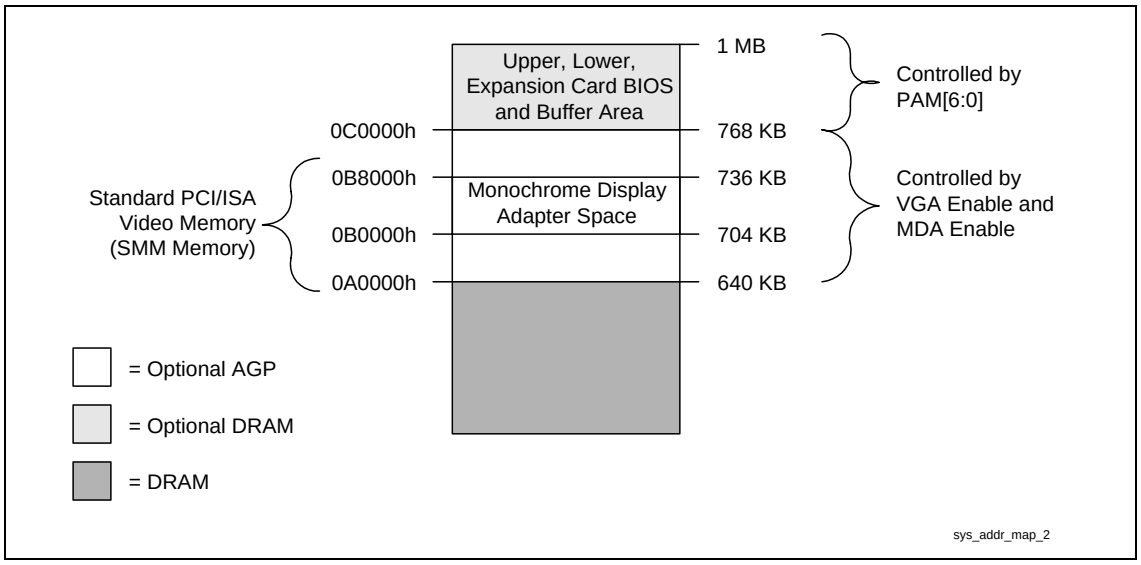
DOS Compatible Area (below 1 MB): The second range is a DOS legacy space, which is used for BIOS and legacy devices on the LPC interface.

Figure 3. System Address Map



These address ranges are always mapped to system memory, regardless of the system configuration. Memory may be carved out of the MAINMEM segment for use by System Management Mode (SMM) hardware and software. The Top of Low Memory (TOM) register defines the top of Main Memory. Note that the address of the highest 16 MB quantity of valid memory in the system is placed into the GBA15 register.

Figure 4. Detailed DOS Compatible Area Address Map



4.1.1. VGA and MDA Memory Space

VGAA	From	0_000A_0000h	To	0_000A_FFFFh
MDA		0_000B_0000h		0_000B_7FFFh
VGAB		0_000B_8000h		0_000B_FFFFh

Video cards use these legacy address ranges to map a frame buffer or a character-based video buffer. By default, accesses to these ranges are forwarded to the hub interface. However, if the VGA_EN bit is set in the BCTRL1-5 configuration registers, transactions within the VGA and MDA spaces are sent to AGP. **Note that the VGA_EN bit may be set in one and only one of the BCTRL registers. Software must not set more than one of the VGA_EN bits.** If the configuration bit MCHCFG.MDAP is set, accesses that fall within the MDA range are sent to the hub interface without regard for the VGAEN bits.

If the MCHCFG.MDAP bit is set, accesses that fall within the MDA range are sent to the hub interface without regard to the VGAEN bits. Legacy support requires the ability to have a second graphics controller (monochrome) in the system. In an 82850/82850E MCH system, accesses in the standard VGA range are forwarded to AGP. Since the monochrome adapter may be on the hub interface (or ISA), bus, the MCH must decode cycles in the MDA range and forward them to the hub interface. This capability is controlled by a configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3Bah, and 3BFh and forwards them to the hub interface.

An optimization allows the system to reclaim the memory displaced by these regions. If SMM memory space is enabled by SMRAM.G_SMRARE and either the SMRAM.D_OPEN bit is set or the system bus receives an SMM-encoded request for code (not data), the transaction is steered to system memory rather than the hub interface. Under these conditions, both of the VGAEN bits and the MDAP bit are ignored.

4.1.2. PAM Memory Spaces

PAMC0	From	0_000C_0000h	To	0_000C_3FFFh
PAMC4		0_000C_4000h		0_000C_7FFFh
PAMC8		0_000C_8000h		0_000C_BFFFh
PAMCC		0_000C_C000h		0_000C_FFFFh
PAMD0		0_000D_0000h		0_000D_3FFFh
PAMD4		0_000D_4000h		0_000D_7FFFh
PAMD8		0_000D_8000h		0_000D_BFFFh
PAMDC		0_000D_C000h		0_000D_FFFFh
PAME0		0_000E_0000h		0_000E_3FFFh
PAME4		0_000E_4000h		0_000E_7FFFh
PAME8		0_000E_8000h		0_000E_BFFFh
PAMEC		0_000E_C000h		0_000E_FFFFh
PAMF0		0_000F_0000h		0_000F_FFFFh

The 256-KB PAM region is divided into three parts:

- **ISA expansion region;** a 128 KB area between 0_000C_0000h – 0_000D_FFFFh
- **Extended BIOS region;** a 64 KB area between 0_000E_0000h – 0_000E_FFFFh
- **System BIOS region;** a 64 KB area between 0_000F_0000h – 0_000F_FFFFh.

The ISA expansion region is divided into eight 16-KB segments. Each segment can be assigned one of four read/write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the MCH and are subtractively decoded to ISA space.

The extended system BIOS region is divided into four 16 KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to the hub interface. Typically, this area is used for RAM or ROM.

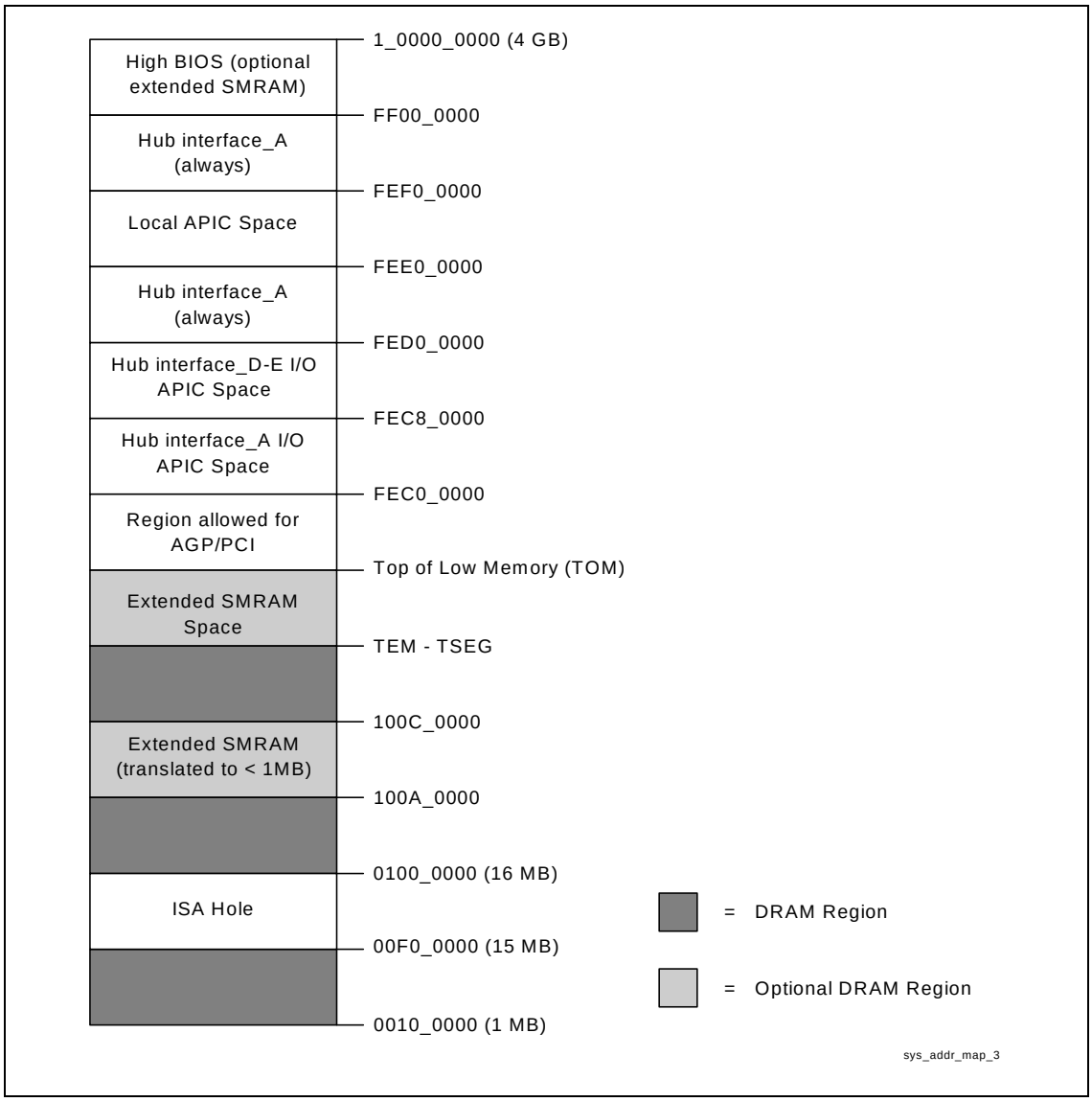
The system BIOS region is a single, 64-KB segment. This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to the hub interface. By manipulating the read/write attributes, the MCH can “shadow” BIOS into the main DRAM.

4.1.3. ISA Hole Memory Space

ISA15	From	0_00F0_0000h	To	0_00FF_FFFFh

BIOS can optionally open a “window” between 15 MB and 16 MB that relays transactions to the hub interface instead of completing them with a system memory access. This window is opened with the FDHC.HEN configuration field.

Figure 5. Detailed Extended Memory Range Address Map



4.1.4. TSEG SMM Memory Space

TSEGSMM From TOM – TSEG To TOM

The TSEG SMM space allows system management software to partition a region of main memory just below the top of low memory (TOM) that is accessible only by system management software. This region can be 128 KB, 256 KB, 512 KB, or 1 MB in size, depending on the ESMRAMC.TSEG_SZ field. SMM memory is globally enabled by SMRAM.G_SMRARE. Requests can access SMM system memory when either SMM space is open (SMRAM.D_OPEN) or the MCH receives an SMM code request on its system bus. To access the TSEG SMM space, the TSEG must be enabled by ESMRAMC.T_EN. When all of these conditions are met, a system bus access to the TSEG space (between TOM-TSEG and TOM) is sent to system memory. If the high SMRAM is not enabled or if the TSEG is not enabled, all memory requests from all interfaces are forwarded to system memory. If the TSEG SMM space is enabled, and an agent attempts a non-SMM access to TSEG space, the transaction is specially terminated.

Hub interface and AGP originated accesses are not allowed to SMM space.

4.1.5. I/O APIC Memory Space

IOAPIC0 (hub interface) From 0_FEC0_0000h To 0_FEC7_FFFFh

The I/O APIC spaces are used to communicate with I/O APIC interrupt controllers that may be populated on the hub interface. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the IOAPIC0 region are always sent to the hub interface.

4.1.6. System Bus Interrupt APIC Memory Space

SBINTR From 0_FEE0_0000 To 0_FEEF_FFFF

The system bus interrupt space is the address used to deliver interrupts to the system bus. Any device on AGP or the hub interface can issue a memory write to 0FEEx_xxxxh. The MCH forwards this memory write, along with the data, to the system bus as an interrupt message transaction. The MCH terminates the system bus transaction by providing the response and asserting TRDY#. This memory write cycle does not go to DRAM.

4.1.7. High SMM Memory Space

HIGHSMM From 0_FEDA_0000 To 0_FEDB_FFFF

The HIGHSMM space allows cacheable access to the compatible SMM space by re-mapping valid SMM accesses between 0_FEDA_0000 and 0_FEDB_FFFF to accesses between 0_000A_0000 and 0_000B_FFFF. The accesses are remapped when SMRAM space is enabled, an appropriate access is detected on the system bus, and when ESMRAMC.H_SMRAME allows access to high SMRAM space. SMM memory accesses from the hub interface or AGP are specially terminated: reads are provided with the value from address 0 while writes are ignored entirely.

4.1.8. AGP Aperture Space (Device 0 BAR)

AGPAPP	From	APBASE	To	APBASE + APSIZE

Processors and AGP devices communicate through a special buffer called the “graphics aperture”. This aperture acts as a window into main DRAM memory and is defined by the APBASE and APSIZE configuration registers of the MCH. Note that the AGP aperture must be above the top of memory and must not intersect with any other address space.

4.1.9. AGP Memory and Prefetchable Memory

M1	From	MBASE1	To	MLIMIT1
PM1		PMBASE1		PMLIMIT1

Plug-and-play software configures the AGP memory window to provide enough memory space for the devices behind this PCI-to-PCI bridge. Accesses whose addresses fall within this window are decoded and forwarded to AGP for completion. Note that these registers must be programmed with values that place the AGP memory space window between the value in the TOM register and 4 GB. In addition, neither region should overlap with any other fixed or relocatable area of memory.

4.1.10. Hub Interface Subtractive Decode

HLA_SUB	From	TOM	To	4 GB

All accesses that fall between the value programmed into the TOM register and 4 GB are subtractively decoded and forwarded to the hub interface if they do not decode to a space that corresponds to another device.

4.2. AGP Memory Address Ranges

The MCH can be programmed to direct memory accesses to the AGP bus interface when addresses are within either of two ranges specified via registers in MCH Device 1 configuration space. The first range is controlled via the Memory Base Register (MBASE1) and Memory Limit Register (MLIMIT1) registers. The second range is controlled via the Prefetchable Memory Base (PMBASE1) and Prefetchable Memory Limit (PMLIMIT1) registers

The MCH positively decodes memory accesses to AGP memory address space as defined by the following equations:

- Memory_Base_Address ≤ Address ≤ Memory_Limit_Address
- Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

The plug-and-play configuration software programs the effective size of the range and it depends on the size of memory claimed by the AGP device.

Note that the MCH Device 1 memory range registers described above are used to allocate memory address space for any devices sitting on AGP bus that require such a window.

4.2.1. AGP DRAM Graphics Aperture

Memory-mapped, graphics data structures can reside in a *Graphics Aperture* to main DRAM memory. This aperture is an address range defined by the APBASE and APSIZE configuration registers of the MCH Device 0. The APBASE register follows the standard base address register template as defined by the PCI 2.1 specification. The size of the range claimed by the APBASE is programmed via “back-end” register APSIZE (programmed by the chipset specific BIOS before plug-and-play session is performed). APSIZE allows the BIOS software to pre-configure the aperture size to be 4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB or 256 MB. By programming APSIZE to a specific size, the corresponding lower bits of APBASE are forced to “0” (behave as hardwired). Default value of APSIZE forces an aperture size of 256 MB. The aperture address range is naturally aligned.

Accesses within the aperture range are forwarded to the main DRAM subsystem. The MCH translates the originally issued addresses via a translation table maintained in main memory. The aperture range should be programmed as non-cacheable in the processor caches.

Plug-and-play software configuration model does not allow overlap of different address ranges. Therefore, the AGP Graphics Aperture and AGP Memory Address Range are independent address ranges that may abut, but cannot overlap one another.

4.3. System Management Mode (SMM) Memory Range

The MCH supports the use of main memory as System Management RAM (SMRAM) enabling the use of System Management Mode. The MCH supports two SMRAM options:

- Compatible SMRAM (C_SMRAM)
- Extended SMRAM (E_SMRAM).

System Management RAM (SMRAM) space provides a memory area that is available for the SMI handler’s and code and data storage. This memory resource is normally hidden from the operating system so the processor has immediate access to this memory space on entry to SMM. The MCH provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional larger write-back cacheable T_SEG area from 128 KB to 1 MB in size above 1 MB that is reserved from the highest area in system DRAM memory. The above 1 MB solutions require changes to compatible SMRAM handlers’ code to properly execute above 1 MB.

Masters from the hub interface and AGP are not allowed to access the SMM space.

4.3.1. SMM Space Definition

Its addressed SMM space and its DRAM SMM space define SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped; therefore, the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space.

Lock Cycles across Top-of-Memory (TOM) are illegal and should not be attempted/executed by software.

Table 12 describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in the describing SMM Space Transaction Handling.

Table 12. SMM Space Address Ranges

SMM Space Enabled	Transaction Address Space (Adr)	DRAM Space (DRAM)
Compatible (C)	A0000h to BFFFFh	A0000h to BFFFFh
High (H)	0FEDA0000h to 0FEDBFFFFh	A0000h to BFFFFh
TSEG (T)	(TOM-TSEG_SZ) to TOM	(TOM-TSEG_SZ) to TOM

NOTES:
1. High SMM: This is different than in previous chipsets. In previous chipsets the High segment was the 384 KB region from A0000h to FFFFFh. This has been removed in the MCH.
2. TSEG SMM: This is different than in previous chipsets. In previous chipsets the TSEG address space was offset by 256 MB to allow for simpler decoding and the TSEG was remapped to just under the TOM. In the MCH TSEG is not offset by 256 MB and it is not remapped.

4.3.2. SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to lock up:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, the AGP aperture range, or to any “PCI” devices (including the hub interface and AGP devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
- SMM space must not be accessed by the AGP Aperture GTLB.

4.4. I/O Address Space

The MCH does not support the existence of any other I/O devices beside itself on the system bus. The MCH generates either hub interface or AGP bus cycles for all processor I/O accesses. The MCH contains two internal registers in the processor I/O space, Configuration Address Register (CONF_ADDR) and the Configuration Data Register (CONF_DATA). These locations are used to implement the configuration space access mechanism as described in the Configuration Register section.

The processor allows 64K+3 bytes to be addressed within the I/O space. The MCH propagates the processor I/O address without any translation on to the destination bus and, therefore, provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when the A16# address signal on the system bus is asserted. A16# is asserted when an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. A16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the hub interface unless they fall within the AGP I/O address range as defined by the mechanisms explained below. The MCH will not post I/O write cycles to IDE.

The MCH never responds to I/O or configuration cycles initiated on AGP or the hub interface. Hub interface transactions requiring completion are terminated with “master abort” completion packets on the hub interface. Hub interface write transactions not requiring completion are dropped. AGP/PCI I/O reads are never acknowledged by the MCH.

4.5. MCH Decode Rules and Cross-Bridge Address Mapping

The address map described above applies globally to accesses arriving on any of the three interfaces (i.e., Host bus, the hub interface or AGP).

4.5.1. Hub Interface Decode Rules

The MCH accepts accesses from the hub interface with the following address ranges:

- All memory read and write accesses to main memory (except SMM space).
- All memory write accesses from the hub interface to AGP memory range defined by MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1.
- All memory read/write accesses to the Graphics Aperture defined by APBASE and APSIZE.
- Memory writes to VGA range on AGP if enabled.

All memory reads from the hub interface that are targeted > 4 GB memory range will be terminated with Master Abort completion, and all memory writes (>4 GB) from the hub interface will be ignored.

4.5.2. AGP Interface Decode Rules

Cycles Initiated Using AGP FRAME# Protocol

The MCH does not support any AGP FRAME# access targeting the hub interface. The MCH claims AGP-initiated memory read and write transactions decoded to the main DRAM range or the Graphics Aperture range. All other memory read and write requests are master-aborted by the AGP initiator as a consequence of MCH not responding to a transaction.

Under certain conditions, the MCH restricts access to the DOS Compatibility ranges governed by the PAM registers by distinguishing access type and destination bus. The MCH does NOT accept AGP FRAME# write transactions to the compatibility ranges if the PAM designates DRAM as writeable. If accesses to a range are not write enabled by the PAM, the MCH does not respond and the cycle results in a master-abort. The MCH accepts AGP FRAME# read transactions to the compatibility ranges if the PAM designates DRAM as readable. If accesses to a range are not read enabled by the PAM, the MCH does not respond and the cycle will result in a master-abort.

If an agent on AGP issues an I/O, PCI Configuration or PCI Special Cycle transaction, the MCH does not respond and the cycle results in a master-abort.

Cycles Initiated Using AGP PIPE# or SB Protocol

All cycles must reference main memory; these references are to the main DRAM address range (including PAM) or Graphics Aperture range (also physically mapped within DRAM but using different address range). AGP accesses to SMM space are not allowed. AGP-initiated cycles that target DRAM are not snooped on the host bus, even if they fall outside of the AGP aperture range.

If a cycle is outside of main memory range, it will terminate as follows:

- **Reads:** Remap to memory address 0h, return data from address 0h, and sets the IAAF error bit in ERRSTS register in Device 0
- **Writes:** Terminated internally without affecting any buffers or main memory.

AGP Accesses to MCH that Cross Device Boundaries

For AGP FRAME# accesses, when an AGP master gets disconnected, it resumes at the new address; this allows the cycle to be routed to or claimed by the new target. Thus, the target on potential device boundaries should disconnect accesses. The MCH disconnects AGP FRAME# transactions on 4 KB boundaries.

AGP PIPE# and SBA accesses are limited to 256 bytes and must hit DRAM. Read accesses crossing a device boundary returns invalid data when the access crosses out of DRAM. Write accesses crossing out of DRAM are discarded. The IAAF Error bit is set.

5. Memory Interface Description

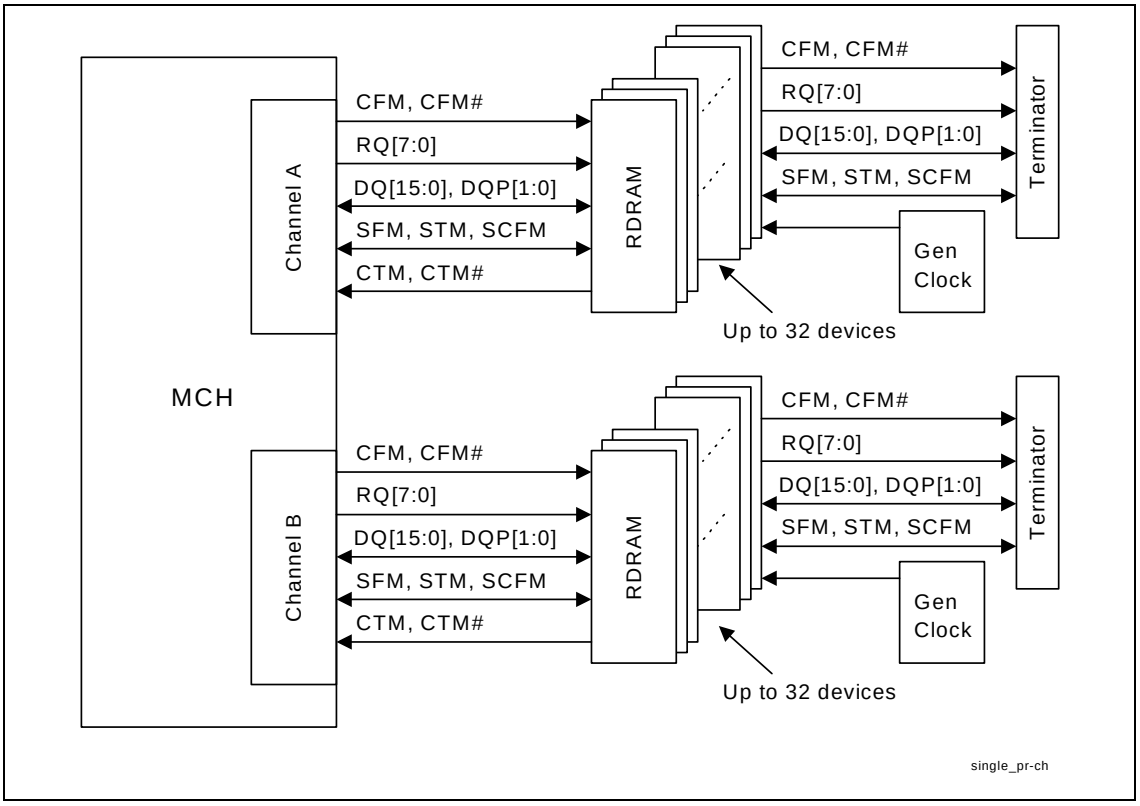
The MCH directly supports dual-channels (interfaces) of Rambus Direct memory operating in lock-step using RSL technology. The MCH supports the following operation mode:

- **Single-Channel Pair Mode –** The MCH is configured to directly support RDRAM devices on its dual Rambus interfaces. There is no MRH-R used on the memory subsystem. A maximum of 64 RDRAM devices are supported on the paired channels without external logic.

The interface between the MCH and Direct RDRAM devices is referred to as a “channel”. The channel interface consists of 33 signals including clocks. Out of these 33 signals, 30 are RSL signals and 3 are CMOS signals.

Figure 6 shows the interconnections between MCH and its dual Direct RDRAM channels configured in single-channel pair mode.

Figure 6. Single-Channel Pair Mode



The maximum system memory supported by MCH depends on the Direct RDRAM device technology. The following table shows the maximum memory supported in various configurations.

RDRAM*	Directly Supported
128 Mb	1 GB Maximum
256/288 Mb	2 GB Maximum

The row, column and bank address bits required for the Direct RDRAM device depends on the number of banks and page size of the device. Table 13 shows the different combinations supported by the MCH.

Table 13. Direct RDRAM* Device Configurations

CF#	Device Tech	Device Capacity in MB	# of Banks (D= dependent)	Page Size	# of Bank Address Bits	# of Row Address Bits	# of Column Address Bits
1	128Mbit	16	16 (D)	1 KB	5	9	6
2		16	2x16 (D)	1 KB	5	9	6
3	256/288 Mbit	32	2x16 (D)	1 KB	5	10	6
4		32	2x16 (D)	2 KB	5	9	7

A brief overview of the registers that configure the Direct RDRAM interface is provided below.

- **Group Boundary Address Register (GBA):** GBA registers define the upper and lower addresses for a group of Direct RDRAM device pairs in a channel-pair. Each group requires a separate GBA register. Each group consists of 4 device-pairs in single channel. The MCH contains 16 GBA registers of which 0-7 are usable.
- **Group Architecture Register (GAR):** GAR registers specify the architecture features of each group of device pairs in a channel pair. The architecture features specified are bank type and device core technology. Each GAR represents a group consisting of 4 device-pairs in single channel. There is a 1:1 correspondence between GBA and GAR registers.
- **RDRAM Timing Register (RDTR):** The DTR defines the timing parameters for all devices in all channels. The BIOS programs this register with “least common denominator” values after reading the configuration registers of each device in the channels.
- **RDRAM Pool Sizing Register (RPMR):** This register provides bits to program the number of RDRAM device-pair in one of three RDRAM power management states.
- **RDRAM Initialization Control Register (RICM):** This register provides bits to program the MCH to do initialization activities on Direct RDRAM devices.

5.1. RDRAM* Organization and Configuration

The MCH supports 16/18-bit Direct RDRAM configurations. The MCH supports a maximum of 64 RDRAM devices (32 devices per channel) on its dual Direct RDRAM channels. The Direct RDRAM channel can be populated with a mix of 128Mbit and 256/288Mbit Direct RDRAM devices.

5.1.1. Rules for Populating RDRAM* Devices

MCH Rambus channels can be implemented such that it is fully or partially loaded with RDRAM devices in single-device pair mode.

The MCH supports a maximum of two RIMMs per channel.

- **Single Device-pair:** The MCH is configured to directly support RDRAM devices on its dual Rambus channel. Each RDRAM device of the MCH Direct Rambus Interface A is paired with one RDRAM device of the Direct Rambus Interface B.

From the MCH point of view, all device-pairs in the channels are grouped into logical groups. System initialization software partitions the RDRAMs into groups of four device-pairs. As a result, there can be a maximum of 8 groups per channel-pair. All device-pairs populated in a group must be of the same architecture. In other words all device-pairs in a group must be the same core technology, and have the same number of banks. Following are the rules for populating the groups:

- A group can be partially populated.
- There is no requirement that group members have to be populated in contiguous physical slots.
- There can be a maximum of 8 groups. A member that does not belong to any of the groups in the channel will not be recognized.

Table 14 provides the device IDs for members in all groups.

Table 14. RDRAM* Device Grouping

Device-Pair IDs for Group Members	Group Name
0, 1, 2, 3	Group #0
4, 5, 6, 7	Group #1
8, 9, 10, 11	Group #2
12, 13, 14, 15	Group #3
16, 17, 18, 19	Group #4
20, 21, 22, 23	Group #5
24, 25, 26, 27	Group #6
28, 29, 30, 31	Group #7

All RSL signals must be terminated at the far end from the MCH. The default device ID for an RDRAM device after power up is 1Fh.

5.1.2. RDRAM* CMOS Signals

There are 3 CMOS signal pins per channel on MCH to support Direct RDRAM device configuration, SIO reset, register accesses, and powerdown exits. These signals are SCK, CMD and SIO. These signals are used to perform the following operations:

- SIO pin initialization
- SIO operations (includes register accesses and device reset)
- Device selection for powerdown exits

Figure 7. RDRAM* Devices Sideband CMOS Signal Configuration on Rambus* Channel A

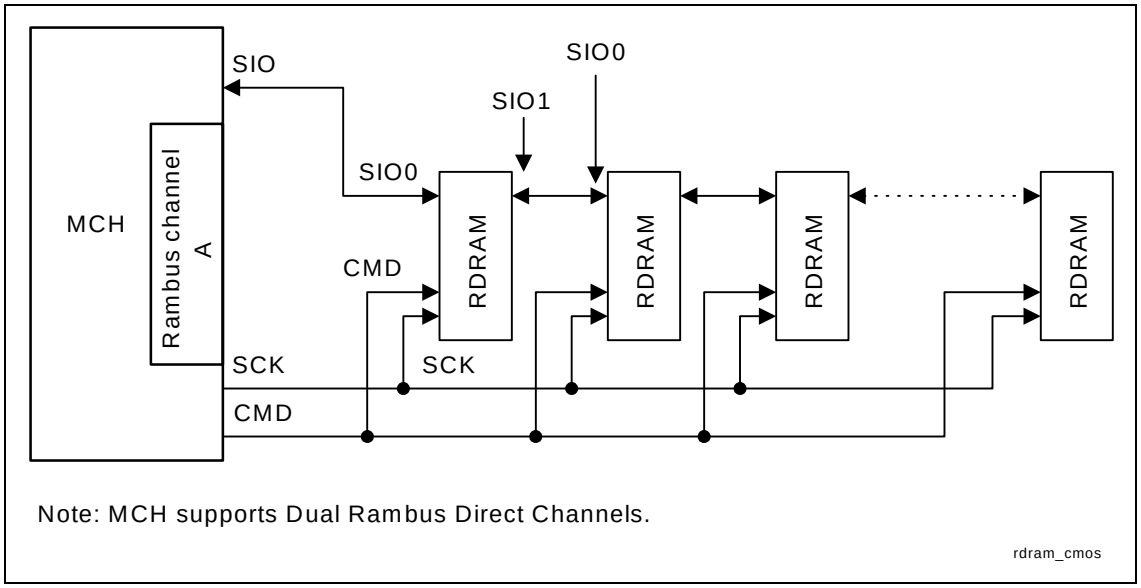


Table 15. Sideband CMOS Signal Description

Signal	Description
SCK	**Serial Clock:** This signal serves as the clock for SIO and CMD signals. SCK is a clock source used for reading from and writing to control register. • For SIO operations and pin initialization, SCK ≤ 1 MHz • For power mode operations, SCK ≤ 100 MHz
CMD	**Command:** CMD is a control signal used for power mode transitions, SIO pin configuration during initialization, and framing of SIO operations. CMD is active high. CMD is sampled at both edges of SCK. CMD is a level sensitive signal.
SIO	**Serial In Out:** This bi-directional signal is daisy chained through all Direct RDRAM (SIO0 to SIO1) devices in a channel. This pin carries data used for SIO operations, which include register accesses, device reset, and device ID initialization. It is also used for power mode control. SIO is an active low signal and is sampled on the falling edge of SCK.

Table 16. CMD Signal Value Decode

SIO = 0, CMD Sample Value on 4 SCK Edges				Command	SIO = 1, CMD Sample Value on 4 SCK Edges				Command
Cycle 0		Cycle 1			Cycle 0		Cycle 1		
0	1	X	x	Reserved	0	1	X	X	Power-down Exit
1	0	X	x	Reserved	1	0	X	X	Reserved
0	0	X	x	No-op	0	0	X	X	No-op
1	1	1	1	SIO Request Frame	1	1	1	1	SIO Request Frame
1	1	0	0	SIO Reset	1	1	0	0	SIO Reset
1	1	1	0	Reserved	1	1	1	0	Reserved
1	1	0	1	Reserved	1	1	0	1	Reserved

SIO Pin Initialization

SIO0 and SIO1 pins on Direct RDRAM devices are bi-directional, and their direction needs to be initialized. The “SIO Reset” initializes SIO0 and SIO1 pins on all Direct RDRAMs as daisy chain configuration and is performed with SCK and CMD. Once the SIO daisy chain is fully configured, SIO operations can occur. Note “SIO Reset” does NOT reset the entire device. For a complete description of operation and associated timing diagram, refer to Direct RDRAM data sheet from Rambus.

SIO Operations

SIO operations are also known as Direct RDRAM initialization operations. These operations include Direct RDRAM register accesses and device reset, and is performed using the CMOS pins (SCK, CMD, SIO0, and SIO1). For a complete description of operation and associated timing diagram, refer to Direct RDRAM data sheet from Rambus.

Powerdown Exits

The powerdown exits are performed using CMD, SIO and SCK signals. For complete description and timing diagrams associated with powerdown exits, refer to Direct RDRAM data sheet from Rambus.

5.1.3. Direct RDRAM* Core Refresh

All rows in a Direct RDRAM device must be refreshed within 32 ms. The refresh rate depends on the device size and page size of a device. The MCH supports two core refresh mechanisms: Active refresh and self refresh.

- **Active Refresh:** Refresh and precharge after refresh commands are issued from the primary control packet. These commands provide refresh support in Standby/Active modes.
- **Self Refresh:** Internal timebase and row/bank address counters in the core allow for a self refresh in powerdown modes without controller support.

Direct RDRAM Current Calibration

All Direct RDRAM devices must be current calibrated once every 100 ms. There are RSL commands to perform this function. The MCH schedules periodic current calibration activity such that every device in the channel is current calibrated at least once every 100 ms.

5.2. Direct RDRAM* Command Encoding

The operations on a Direct RDRAM channel are performed using control packets. There are two types of command packets: row (ROWA/ROWR) packet and column (COLC/COLM/COLX) packet. Each command packet requires a 4 Direct RDRAM clock duration and packet data is transferred on both (leading and falling) edges of the clock. Row packet contains 24 bits and column packet contains 40 bits.

5.2.1. Row Packet (ROWA/ROWR)

The row packet is defined using three RSL signals RQ[7:5]/ROW[2:0]. It is generally the first control packet issued to a device. Major characteristics of the row packet are:

- the only way to activate (sense) a row within a bank
- independent of Direct RDRAM's active/standby state
- a non-broadcast row package causes an addressed Direct RDRAM to move to active state

The packet definition of row packet is given below.

Table 17. ROWA Packet for Activating (Sensing) a Row (i.e., AV = 1)

Row	Cycle 0		Cycle 1		Cycle 2		Cycle 3	
ROW2	DR4T	DR[2]	BR[0]	BR[3]	R[10]	R[8]	R[5]	R[2]
ROW1	DR4F	D[R1]	BR[1]	BR[4]	R[9]	R[7]	R[4]	R[1]
ROW0	DR[3]	DR[0]	BR[2]	REV	AV = 1	R[6]	R[3]	R[0]

Table 18. ROWR Packet for Other Operations (i.e., AV = 0)

Row	Cycle 0		Cycle 1		Cycle 2		Cycle 3	
ROW2	DR4T	DR[2]	BR[0]	BR[3]	ROP[10]	ROP[8]	ROP[5]	ROP[2]
ROW1	DR4F	DR[1]	BR[1]	BR[4]	ROP[9]	ROP[7]	ROP[4]	ROP[1]
ROW0	DR[3]	DR[0]	BR[2]	REV	AV = 0	ROP[6]	ROP[3]	ROP[0]

DR4T	DR4F	Device ID
0	0	No row packet
0	1	DR[3:0], DR[4] = 0
1	0	DR[3:0], DR[4] = 1
1	1	Broadcast

DR[4]–DR[0]	Device address
BR[5]–BR[0]	Bank Address
R[10]–R[0]	Row address
AV	Select between ROWA and ROWR, Active Row
ROP[10]–ROP[0]	Opcode for Primary Control Packet
REV	Reserved

AV	Opcode bits									Operation Description
	10	9	8	7	6	5	4	3	2:0	
1	x	x	X	x	x	x	x	x	Xxx	Activate Row
0	1	1	0	0	0	0	0	0	000	Precharge
0	1	1	0	0	0	0	0	1	000	Precharge & Relax
0	0	0	0	1	1	0	0	0	000	Refresh
0	1	0	1	0	1	0	0	0	000	Precharge Postrefresh
0	0	0	0	0	0	1	0	0	000	Reserved
0	0	0	0	0	0	1	1	0	000	Reserved
0	0	0	0	0	0	0	1	0	000	Power Down
0	0	0	0	0	0	0	0	1	000	Relax
0	0	0	0	0	0	0	0	0	010	Temp Calibration Enable
0	0	0	0	0	0	0	0	0	001	Temp Calibration
0	0	0	0	0	0	0	0	0	000	No-op

NOTES:
1. x = Controller drives 0 or 1
2. 0 = Controller drives 0
3. 1 = Controller drives 1

5.2.2. Column Packet (COLC/COLX)

The column packet is defined using five of the RSL signals RQ[4:0]/COL[4:0]. Major characteristics of the column packet are:

- the only way to dispatch column operation for read or write
- requires the target Direct RDRAM to be in active state

When a Direct RDRAM is in active state it can receive both row and column packets. When a Direct RDRAM is in the Standby state it can only receive a row packet. Thus, before sending a column packet, make sure the addressed Direct RDRAM is in the active state. The packet definition of column packet is provided in Table 19.

Table 19. COLC Packet

Column	Cycle 0		Cycle 1		Cycle 2		Cycle 3	
COL4	DC[4]	S = 1					C[6]	C[4]
COL3	DC[3]						C[5]	C[3]
COL2	DC[2]	COP[1]				REV	BC[2]	C[2]
COL1	DC[1]	COP[0]				BC[4]	BC[1]	C[1]
COL0	DC[0]	COP[2]			COP[3]	BC[3]	BC[0]	C[0]

NOTES:
1. DC[4:0] Device ID for Column Operation
2. S Start bit, for framing
3. M Mask bit. Asserted indicates mask format for packet
4. COP[3:0] Column Operation Code
5. C[6:0] Address for Column operation
6. BC[4:0] Bank Address for Column operation
7. REV Reserved

Table 20. COLC Packet Field Encodings

S	COP[3]	COP[2]	COP[1]	COP[0]	Command Operation
0	x	X	x	X	No operation
1	x	0	0	0	NOCOP. Retire write buffer of this device
1	x	0	0	1	Write
1	x	0	1	1	Read

NOTES: All other combination are reserved.

Table 21. COLX Packet (M = 0)

Column	Cycle 0		Cycle 1		Cycle 2		Cycle 3	
COL4			DX[4]	XOP[4]	REV	BX[1]		
COL3		M = 0	DX[3]	XOP[3]	BX[4]	BX[0]		
COL2			DX[2]	XOP[2]	BX[3]			
COL1			DX[1]	XOP[1]	BX[2]			
COL0			DX[0]	XOP[0]				

NOTES:
1. DX[4:0] Device ID for Extra operation
2. BX[4:0] Bank Address for Extra operation
3. MA[7:0] Byte Mask (low order)
4. MB[7:0] Byte Mask (high order)
5. XOP[4:0] Opcode for Extra Operation
6. REV Reserved

Table 22. COLM Packet and COLX Packet Field Encodings

M	XOP Bits					Operation Description
	4	3	2	1	0	
1	X	x	x	x	X	Non existent Xop
0	0	0	0	0	0	NoXop
0	1	0	0	0	0	Reserved
0	0	1	0	0	0	Calibrate Current
0	0	1	1	0	0	Calibrate Current & Sample
0	0	0	0	0	1	Reserved

NOTES:
1. x = Controller drives 0 or 1
2. 0 = Controller drives 0
3. 1 = Controller drives 1

5.2.2.1. Data Packet

Table 23. Data Packet

	Cycle 0		Cycle 1		Cycle 2		Cycle 3	
DQA[8:0]	DA0[8:0]	DA1[8:0]	DA2[8:0]	DA3[8:0]	DA4[8:0]	DA5[8:0]	DA6[8:0]	DA7[8:0]
DQB[8:0]	DB0[8:0]	DB1[8:0]	DB2[8:0]	DB3[8:0]	DB4[8:0]	DB5[8:0]	DB6[8:0]	DB7[8:0]

5.3. Direct RDRAM* Register Programming

Software can read and write Direct RDRAM device registers by programming the “RDRAM Initialization Control Management Register” (RICM) in the MCH. The register data returned by the device is available in the “Device Register Data Register “(DRD).

5.4. Direct RDRAM* Operating States

The Direct RDRAM devices support different operating and idle states to minimize the power consumption and thermal overload. Table 24 provides an overview of the different operating/power states supported by Direct RDRAMs.

Table 24. DRAM Operating States

Direct RDRAM* State	Functionality	Refresh Scheme	RDRAM Clock State
Inactive States			
Powerdown	No operation allowed except refresh. Direct RDRAM awaits CMOS signals to exit powerdown state	Self Refresh	stopped
Active States			
Standby	Device Ready to receive row packet . with fast clock	Active Refresh	full speed
Active	Device ready to receive any control packet	Active Refresh	full speed
Active-Read	Device ready to receive any control packet. Transmitting data on channel	Active Refresh	full speed
Active-Write	Device ready to receive any control packet. Receiving data from channel	Active Refresh	full speed

- **Active-Read/Write state:** A Direct RDRAM device is in the active-Read/Write state when it is transferring data. This state lasts as long as data transfer is occurring. Once the data transfer is done, the Direct RDRAM transitions into Active or Standby state based on the column command last executed.
- **Active State:** A Direct RDRAM enters into active state immediately after the data transfer from/to that device is done and the last COLC command that caused the data transfer does not have its RC bit set to 1. When a device is in Active state, it can accept both row and column packets.
- **Standby State:** A Direct RDRAM enters into Standby state either from Active-Read/Write or Active state. Transition from Active-Read/Write to Standby happens if the last column executed has its RC bit set to 1. Transition from Active to Standby happens if COLC or row specifies an operation with Relax. When a device is in Standby mode, it can accept only row packets. Once a

device receives any row packet, it transitions into active state and only then can it accept a column packet.

- **Nap State:** A Direct RDRAM enters into Nap state when it receives a row packet which specified an operation with Nap. No operation except refresh is allowed during Nap state. This mode is not supported by the 82850/82850E MCH.
- **Powerdown State:** A Direct RDRAM enters into powerdown state when it receives a row packet which specified an operation with powerdown. No operation except Self-refresh is allowed during powerdown state.

5.5. RDRAM* Operating Pools

The RDRAM devices are grouped into three operating pools called Pool "A", Pool "B", and Pool "C".

5.5.1. Pool "A", Pool "B", and Pool "C" Operation

In the "pool" mode, three queues are used inside the MCH: the "A" pool contains references to device pairs that are currently in the active mode while the "B" pool contains references to device pairs that are in the standby mode. All devices that are not found in either pool "A" or "B" are said to be in Pool "C" and should be configured for standby. The "A" pool may hold between 1 and 8 device pairs, while the "B" pool may be configured to contain between 1 and 16 device pairs.

5.6. RDRAM* Power Management

The 850 chipset systems support ACPI based power management. The MCH puts all RDRAM devices into powerdown (PD) state during S3 power management states. To enter the powerdown state all RDRAM devices in the channel must be in active or standby state. The MCH then sends a broadcast Powerdown command to that channel.

During powerdown state, RDRAM devices are put into Self Refresh mode so that external (active) refreshes are not required. During the power-down state, the clocks to RDRAM are shut off.

Exiting the powerdown state is done through CMOS signals. Table 25 shows the actions taken by MCH during different processor and System power states.

Table 25. RDRAM* Power Management states

Processor State	System State	State of RDRAM* in Pool "A"	State of RDRAM in Pool "B"	State of RDRAM in Pool "C"	Refresh Scheme	RDRAM Clock State
C0, C1, C2 (processor in working state)	S0	Active-Read/Write, Active,	Standby	Standby	Active	Running
(processor in inactive state)	S1, S3(STR)	No devices in Pool "A"	No devices in Pool "B"	Power-down	Self	Stopped

5.7. Data Integrity

The MCH supports an Error Correcting Code (or Error Checking and Correcting) on the main memory interface. The MCH can optionally be configured to generate the ECC code for writes to memory and check the code for reads from memory. The MCH generates an 8-bit code word for each 64-bit QWord of memory. Since the code word covers a full QWord, writes of less than a QWord require a read-merge-write operation. Consider a DWord write to memory. In this case, when in ECC mode, the MCH will read the QWord where the addressed DWord will be written, merge in the new DWord, generate a code covering the new QWord and finally write the entire QWord and code back to memory. Any correctable (single) errors detected during the initial QWord read are corrected before merging the new DWord.

Single bit and multiple bit errors set separate flags in the ERRSTS register. Single bit errors and multiple bit errors can be independently enabled to generate hub interface SERR, SMI, or SCI special cycles to the I/O Controller Hub. The address and syndrome of the first single bit error are latched in the EAP and DERRCTL registers. Subsequent single bit errors will not overwrite the EAP and DERRCTL registers unless the single bit error status bit is cleared. A multiple bit error overwrites the EAP and DERRCTL registers. Subsequent multiple bit errors do not overwrite the EAP and DERRCTL registers unless the multiple bit error status bit is cleared.

5.8. RDRAM* Array Thermal Management

The RDRAM thermal and power management of the MCH has been optimized for desktop system designs. It is assumed that proper system design will always provide and ensure adequate cooling in an 850 chipset-based system.

In an 850-based system, RDRAM operates in one of two modes: active or standby. The number of devices that are allowed in each state at any given time is specified by the system designer. At any point, between 1 and 8 device-pairs may be in the “A” pool and are configured to operate in the active mode. In addition, between 1 and 16 device-pairs may be in the “B” pool and are configured to operate in the standby mode. The rest of the device-pairs are in the “C” pool and are configured to operate in standby mode. Regardless of how many devices are configured into the “A” and “B” pools or the “C” pool , the system designer is responsible for providing adequate cooling for the number of RDRAM devices in the system.

After BIOS loads the system’s “target” values into the DPS register and initializes the pools, it should load a “safer” set of values into the DPS register *without* setting the POOLINIT field. The POOLINIT bit instructs the MCH to transition to the new pool sizes. The following lists the conditions that cause the MCH to resize and initialize the pools:

- The detection of an over-temperature condition on any RDRAM device. The RDRAM devices report over-temperature conditions back to the MCH via a special bit asserted during their current calibration operations. When the MCH detects an over-temperature condition in any of the memory devices, the RDRAM pools are reinitialized with “safer” values. Finally, the MCH may be configured to send an SERR, SCI, or SMI hub interface message to the ICH2. The software may take action to cool the system or to log the condition.

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6. Electrical Characteristics

This chapter contains the power, thermal, and DC specifications for the MCH.

AGTL+ (Assisted Gunning Transceiver Logic) signals are open-drain and require termination to a supply that provides the high signal level. Termination resistors are provided on the MCH and are terminated to VTT, thus eliminating the need to terminate the bus on the system motherboard. For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused AGTL+ inputs should be left as no connects, as AGTL+ termination is provided on the silicon. Unused active high inputs should be connected through a resistor to ground (Vss). Unused outputs can be left unconnected.

The Direct RDRAM* interface introduces a new type of interface called RSL (Rambus Signaling Level) signaling. RSL signals are open-drain drivers, and must be terminated to 1.8 V via a 28-Ω termination resistor.

6.1. Absolute Maximum Ratings

Table 26 lists the MCH's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the AC and DC tables.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "operating Conditions" is not recommended and extended exposure beyond "operating Conditions" may affect reliability.

Table 26. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
Tdie	Die Temperature under Bias	0	110	°C	1
Tstorage	Storage Temperature	0	105	°C	
Vcc	1.8V Supply Voltage with respect to Vss	-0.3	2.5	V	
VTT	AGTL+ buffer DC input voltage with respect to Vss	1.4	1.7	V	
VDDQ	AGP bus DC input voltage with respect to Vss	1.4	1.8	V	

NOTES:
1. Based on a No Heat sink condition.

6.2. Thermal Characteristics

The MCH is designed for operation at die temperatures between 0 °C and 110 °C. The thermal resistance of the package is given in Table 27.

Table 27. MCH Package Thermal Resistance

Parameter	Unit	
	0 m/s	1 m/s
Psi_{jt} (°C/Watt)[1]	0.0	TBD
$Theta_{ja}$ (°C/Watt)[1]	20.0	16.0

NOTES:
1. Typical value measured in accordance with EIA/JESD 51-2 testing standard.

6.3. Power Characteristics

Table 28. DC Characteristics Functional Operating Range (VCC1_8 = 1.8V ±5%; Tdie = 110 °C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
P_{Tehama}	Thermal Power Dissipation for the 82850/82850E MCH		6.9	8.9	W	1
I_{VTT}	82850/82850E MCH VTT supply Current			2.2	A	
I_{DDQ}	Power supply current for AGP interface			370	mA	
I_{CC}	Power supply current for the 82850/82850E MCH			3.5	A	

NOTES:
1. This specification is the Thermal Design Power and it is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus. Studies by Intel indicate that no application will cause thermally significant power dissipation exceeding this specification, although it is possible to implement higher power synthetic workloads that write but never read. Under realistic read/write conditions, this higher power workload can only be transient, and is accounted in the Icc (Max) specification. For more information, refer to the *Intel® 850 Chipset: Thermal Considerations, Application Note (AP-720).*

6.4. I/O Interface Signal Groupings

The signal description includes the type of buffer used for the particular signal:

AGTL+ Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The MCH integrates AGTL+ termination resistors.

AGP AGP interface signals. These signals are compatible with AGP 2.0 1.5V Signaling Environment DC and AC Specifications. The buffers are not 3.3V tolerant.

CMOS 1.8 V CMOS buffers.

RSL RDRAM Signaling Level interface signal. Refer to the RDRAM* Direct Specification for complete details.

RCMOS RCMOS buffers are 1.8 V CMOS buffers used for the CMOS signals on the RDRAM* interface.

Table 29. Signal Groups

Signal Group	Signal Type	Signals	Notes
(a)	AGTL+ I/O	ADS#, BNR#, BRO#,DBSY#, DBI[3:0]#, DRDY#, HA[31:3]#, HADSTB[1:0] #, HD[63:0]#,HDSTBP[3:0]#, HDSTBN[3:0]#, HIT#, HITM#, HREQ[4:0]#	
(b)	AGTL+ Output	BPRI#, CPURST#, DEFER#, HTRDY#, RS[2:0]#	
(c)	AGTL+ Input	HLOCK#, BERR#	
(d)	Hub Interface's CMOS I/O	HL_A[11:0], HLA_STB, HLA_STB#	
(e)	CMOS Output	CHx_HCLK[A,B], CHx_RCLK[A,B]	
(f)	CMOS Input	TESTIN#, OVERT#, BUSPARK	
(g)	Miscellaneous CMOS Input	RSTIN#(3.3V)	
(h)	CMOS Clock Input	BCLK[1:0], 66IN	1
(i)	RSL I/O	DQA_A[8:0], DQB_A[8:0], DQA_B[8:0], DQB_B[8:0]	
(j)	RSL Output	RQ_A[7:5], RQ_A[4:0], CFM_A, CFM_A#, EXP_A[1:0], RQ_B[7:5], RQ_B[4:0], CFM_B, CFM_B#, EXP_B[1:0]	2
(k)	RSL Input	CTM_A, CTM_A#, CTM_B, CTM_B#	2
(l)	Rambus* CMOS I/O	SIO_A, SIO_B	
(m)	Rambus CMOS Output	CMD_A, SCK_A, CMD_B, SCK_B	
(n)	AGP Input	PIPE#, SBA[7:0], RBF#, WBF#, SB_STB, SB_STB#, G_REQ#, G_SERR#	
(o)	AGP Output	ST[2:0], G_GNT#	

Signal Group	Signal Type	Signals	Notes
(p)	AGP I/O	AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, G_FRAME#, G_IRDY#, G_TRDY#, G_STOP#, G_DEVSEL#, G_AD[31:0], G_C/BE[3:0]#, G_PAR	
(q)	RSL Reference	CHA_REF[1:0], CHB_REF[1:0]	
(r)	AGTL+ Reference	HAVREF[1:0], HDVREF[3:0], CCVREF	
(s)	Hub interface's & AGP Reference	GREF_0, GREF_1, HLREF_A	
(t)	Host Compensation Reference Voltage	HSWNG[1:0]	
(u)	AGP Compensation Reference Voltage	G_SWNG	
(v)	AGP I/O Voltage	VDDQ	
(w)	AGTL+ Termination Voltage	VTT	
(x)	1.8V	VCC1_8	

NOTES:

1. 66IN is a 3.3V signal coming from the system clock generator. A voltage translation will be done internally before the clocks are utilized in the 1.8V MCH. The system interconnect clock skew due to the voltage translation needs to be considered in the AC timing analysis.
2. CTM_A, CTM_A#, CTM_B, CTM_B#, CFM_A, CFM_A#, CFM_B, CFM_B# Rambus channel differential clocks are also operating at a different DC Value. For further details, refer to the DRCG datasheet at www.rambus.com

6.5. DC Characteristics

Table 30. DC Characteristics at VCC1_8 = 1.8 V ± 5%

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage							
VCC1_8	(x)	CMOS I/O Supply Voltage	1.71	1.8	1.89	V	
VDDQ	(v)	AGP I/O Supply Voltage	1.425	1.5	1.575	V	
VTT	(w)	Host AGTL+ Termination Voltage	1.44	1.6	1.7	V	
Reference Voltage							
CCVREF	I	Host Common Clock Reference Voltage	0.64 x VTT	2/3 x VTT	0.70 x VTT	V	
CHx_REF	(q)	Direct RDRAM* Channel RSL Reference Voltage	1.32	1.40	1.48	V	
GREF/ HLREF	(s)	Hub Interface Reference Voltage when Configured for Enhanced Buffer Mode	0.64 x VCC1_8	2/3 x VCC1_8	0.70 x VCC1_8	V	
		Hub Interface Reference Voltage when Configured for Standard Buffer Mode	0.48 x VCC1_8	½ x VCC1_8	0.52 x VCC1_8	V	
		AGP Reference Voltage	0.48 x VDDQ	½ x VDDQ	0.52 x VDDQ	V	
HxVREF	I	Host Address and Data Reference Voltage	0.64 x VTT	2/3 x VTT	0.70 x VTT	V	
HSWING	(t)	Host Compensation Reference Voltage	0.32 x VTT	1/3 x VTT	0.35 x VTT	V	
	(u)	Hub Interface Compensation Reference Voltage	0.32 x VCC1_8	1/3 x VCC1_8	0.35 x VCC1_8	V	
		AGP Compensation Reference Voltage	0.48 x VDDQ	½ x VDDQ	0.52 x VDDQ	V	
Host Interface							
V_{IL_H}	(a), (c)	Host AGTL+ Input Low Voltage			(2/3 x VTT) – 0.1	V	
V_{IH_H}	(a), (c)	Host AGTL+ Input High Voltage	(2/3 x VTT) + 0.1			V	
V_{OL_H}	(a), (b)	Host AGTL+ Output Low Voltage			(1/3 x VTT) + 0.1	V	VTT =1.7V
V_{OH_H}	(a), (b)	Host AGTL+ Output High Voltage	VTT–0.1			V	
I_{OL_H}	(a), (b)	Host AGTL+ Output Low Leakage	19	26.65	34	mA	V_{OL} max
I_{L_H}	(a), (c)	Host AGTL+ Input Leakage Current			10	µA	V_{OL} <Vpad<VTT
C_{PAD}	(a), (c)	Host AGTL+ Input Capacitance			3	pF	

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
RDRAM* Interface							
V_{IL_R}	(i)	RDRAM* RSL Input Low Voltage	CHx_REF – 0.5		CHx_REF – 0.175	V	
V_{IH_R}	(i)	RDRAM* RSL Input High Voltage	CHx_REF + 0.175		CHx_REF + 0.5	V	
$V_{IL\_R\_1066}$	(i)	RDRAM* RSL Input Low Voltage for 1066 RDRAM	CHx_REF – 0.5		CHx_REF – 0.080	V	
$V_{IH\_R\_1066}$	(i)	RDRAM* RSL Input High Voltage for 1066 RDRAM	CHx_REF + 0.080		CHx_REF + 0.5	V	
V_{IL_RC}	(l)	RDRAM* CMOS Input Low Voltage	-0.3		(VCC1_8 / 2) – 0.25	V	
V_{IH_RC}	(l)	RDRAM* CMOS Input High	(VCC1_8 / 2) + 0.25		VCC1_8 + 0.3	V	
V_{OL_RC}	(l), (m)	RDRAM* CMOS Output Low Voltage			(VCC1_8 / 2) – 0.65	V	Into Spec terminator of 91 Ω to VCC1_8 and 39 Ω to Vss
V_{OH_RC}	(l), (m)	RDRAM* CMOS Output High Voltage	(VCC1.0 / 2) + 0.45			V	Into Spec terminator of 91 Ω to VCC1_8 and 39 Ω to Vss
I_{OL_R}	(i), (j)	RDRAM* RSL Output Low Current	30		90	mA	
I_{OH_R}	(i), (j)	RDRAM* RSL Output High Current			±10	mA	
I_{OL_RC}	(l), (m)	RDRAM* CMOS Output Low Current			14.9	MA	V_{OL}= (VCC1_8 / 2) – 0.6 and VCC1_8(min)
I_{OH_RC}	(l), (m)	RDRAM* CMOS Output High Current	35.5			mA	V_{OH} = (VCC 1.8/ 2) + 0.4 and VCC 1.8(max)
I_{L_RC}	(l)	RDRAM* CMOS Input Leakage Current			±10	µA	0<Vin<VCC1_8
C_{IN_R}	(i)	RDRAM* RSL Input Capacitance	4		6	pF	F_C=1 MHz
C_{IN_RC}	(l)	RDRAM* CMOS Input (SCK, CMD) Capacitance	7		9	pF	F_C = 1 MHz
	(l)	RDRAM* CMOS Input (SIO) Capacitance	4		6	pF	F_C = 1 MHz

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
AGP Interface							
V_{IL_A}	(n), (p)	AGP Input Low Voltage	-0.5		0.4 x VDDQ	V	
V_{IH_A}	(n), (p)	AGP Input High Voltage	0.6 x VDDQ		VDDQ + 0.5	V	
V_{OL_A}	(o), (p)	AGP Output Low Voltage			0.15 x VDDQ	V	
V_{OH_A}	(o), (p)	AGP Output High Voltage	0.85 x VDDQ			V	
I_{OL_A}	(o), (p)	AGP Output Low Current			1	mA	V_{OL}=0.15VDDQ
I_{OH_A}	(o), (p)	AGP Output High Current	-0.2			mA	V_{OH}=0.85VDDQ
I_{L_A}	(n), (p)	AGP Input Leakage Current			±10	µA	0<Vin<VDDQ
C_{IN_A}	(n), (p)	AGP Input Capacitance			8	pF	F_C = 1 MHz
Hub Interface with Normal Buffer Mode							
V_{IL_HL}	(d)	Hub Interface Input Low Voltage			HLREF – 0.15	V	
V_{IH_HL}	(d)	Hub Interface Input High Voltage	HLREF + 0.15			V	
V_{OL_HL}	(d)	Hub Interface Output Low Voltage			0.1 x VCC1_8	V	I_{OL}= 1 mA
V_{OH_HL}	(d)	Hub Interface Output High Voltage	0.9 x VCC1_8			V	I_{OH} = 1 mA
I_{OL_HL}	(d)	Hub Interface Output Low Current			1	mA	V_{OL}=0.1 x VCC1_8
I_{OH_HL}	(d)	Hub Interface Output High Current	-1			mA	V_{OH}=0.9 x VCC1_8
I_{L_HL}	(d)	Hub Interface Input Leakage Current			±10	µA	0<Vin<VCC1_8
C_{IN_HL}	(d)	Hub Interface Capacitance			8	pF	F_C = 1 MHz
V_{OH_HL}	(d)	Hub Interface Output High Voltage	VCC1_8 –0.1			V	I_{OH} = 1 mA
I_{OL_HL}	(d)	Hub Interface Output Low Current	21.3		27.3	mA	VCC1_8/3
I_{OH_HL}	(d)	Hub Interface Output High Current			1	mA	
I_{L_HL}	(d)	Hub Interface Input Leakage Current			±10	µA	0<Vin<VCC1_8
C_{IN_HL}	(d)	Hub Interface Capacitance			8	pF	F_C = 1 MHz

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
1.8V CMOS Signals							
V_{IL_C}	(f)	CMOS Input Low Voltage	-0.3		(VCC1_8)/2 – 0.25	V	
V_{IH_C}	(f)	CMOS Input High Voltage	(VCC1_8)/2 + 0.25		VCC1_8 + 0.3	V	
V_{OL_C}	(e)	CMOS Output Low Voltage			0.3	V	
V_{OH_C}	(e)	CMOS Output High Voltage	VCC1_8 – 0.3			V	
I_{OL_C}	(e)	CMOS Output Low Current			1	mA	V_{OL}=0.3V
I_{OH_C}	(e)	CMOS Output High Current	–0.25			mA	V_{OH}=VCC1_8 – 0.3V
I_{L_C}	(f)	CMOS Input Leakage Current			±10	µA	0<Vin<VCC1_8
C_{IN_C}	(f)	CMOS Input Capacitance			9	pF	F_C = 1 MHz
Miscellaneous Interface							
V_{IL}	(g)	CMOS Input Low Voltage	–0.3		0.7	V	
V_{IH}	(g)	CMOS Input High Voltage	1.7		2.625	V	
I_L	(g)	CMOS Input Leakage Current			±10	µA	
C_{IN}	(g)	CMOS Input Capacitance			7	pF	
C_{IN_CLK}	(h)	CMOS Clock Input Capacitance			TBD	pF	F_C = 1 MHz

7. Pinout and Package Information

7.1. Ballout Information

This section provides the MCH ballout assignment. Figure 8 and Figure 9 show the footprint ballout assignment from a top view of the package. Table 31 lists the ballout assignment in alphabetical order by signal name.

Figure 8. MCH Ballout (Top View — Left Side)

	24	23	22	21	20	19	18	17	16	15	14	13
AF	VSS	G_AD6	G_AD8	G_AD13	G_PAR	GSTOP#	G_AD19	G_C/BE3#	G_AD25	G_AD27	SBA7	SBA2
AE	G_AD7	VDDQ	G_C/BE0#	G_AD12	VSS	VDDQ	G_AD18	VDDQ	G_AD24	G_AD26	VSS	SBA3
AD	G_AD2	G_AD4	VSS	G_AD11	VSS	VDDQ	G_AD17	G_AD23	VSS	VDDQ	G_AD31	SB_STB
AC	VDDQ	AD_STB0	AD_STB0#	VDDQ	G_C/BE1#	G_DEVSEL#	VSS	G_AD22	VSS	VDDQ	G_AD30	SB_STB#
AB	G_AD0	VSS	VDDQ	G_AD14	VSS	G_FRAME#	G_AD16	VDDQ	AD_STB1	AD_STB1#	VSS	SBA4
AA	G_AD5	VSS	G_AD3	G_AD9	G_AD15	VDDQ	G_C/BE2#	G_AD21	VSS	VDDQ	G_AD29	SBA5
Y	G_AD1	VDDQ	G_AD10	VDDQ	G_TRDY#	VSS	G_IRDY#	G_AD20	VSS	VDDQ	G_AD28	SBA6
W		DQA_A6	VSS	DQA_A8	VSS	DQA_A7	NC	GREF_0	VSS	GSWNG	GREF_1	GRCOMP
V		VSS	DQA_A4	VSS	DQA_A5	VSS	NC	VSS	66IN	VCC1_8	VSS	VDDQ
U	VSS	DQA_A2	VSS	DQA_A0	VSS	DQA_A3	VSS	VSS	VSS	VCC1_8	VCC1_8	VSS
T	VSS	VSS	VCC1_8	VSS	DQA_A1	VSS	VSS	VSS	VSS	VCC1_8	VCC1_8	VSS
R	CTM_A	CTM_A#	VSS	CHA_VREF1	VSS	VCC1_8	VSS	VCC1_8	VCC1_8	VSS	VSS	VCC1_8
P	CFM_A#	CFM_A	VSS	CHA_VREF0	VSS	VCC1_8	VSS	VCC1_8	VCC1_8	VSS	VSS	VCC1_8
N	VSS	VSS	VCC1_8	VSS	RQ_A7	VSS	VSS	VSS	VSS	VCC1_8	VCC1_8	VSS
M	VSS	RQ_A6	VSS	RESERVED	VSS	RQ_A5	VSS	VSS	VSS	VCC1_8	VCC1_8	VSS
L	RQ_A4	VSS	RESERVED	VSS	RQ_A3	VSS	VSS	VCC1_8	VCC1_8	VSS	VSS	VCC1_8
K	VSS	RQ_A2	VSS	RQ_A1	VSS	DQB_A0	VSS	VCC1_8	VCC1_8	VSS	VSS	VCC1_8
J	RQ_A0	VSS	VCC1_8	VSS	VCC1_8	VSS	VSS	VSS	VSS	VCC1_8	VCC1_8	VSS
H		DQB_A1	VSS	DQB_A2	VSS	DQB_A4	VSS	VSS	VSS	VCC1_8	VCC1_8	VSS
G		VSS	DQB_A6	VSS	DQB_A8	VSS	VSS	VSS	VSS	VSS	VSS	VSS
F	VSS	DQB_A5	VSS	DQB_A3	VSS	DQB_A7	VSS	DQA_B3	VSS	VCC1_8	VCC1_8	VSS
E	SCK_A	SIO_A	CMD_A	CHA_HCLKOUT	CHA_RCLKOUT	VSS	DQA_B5	VSS	DQA_B1	VSS	VSS	RQ_B7
D	HLRCOMP_A	HLREF_A	HL_A9	HL_A10	VSS	DQA_B7	VSS	DQA_B0	VSS	CHB_VR	CHB_VR	VSS
C	VSS	HL_A0	VSS	HLA_STB	HL_A8	VSS	DQA_B6	VSS	VCC1_8	VSS	VSS	VCC1_8
B	HL_A1	VCC1_8	HLA_STB#	HL_A6	VCC1_8	DQA_B8	VSS	DQA_B2	VSS	CTM_B#	CFM_B	VSS
A	HL_A2	HL_A3	HL_A4	HL_A5	HL_A7	VSS	DQA_B4	VSS	VSS	CTM_B	CFM_B#	VSS
	24	23	22	21	20	19	18	17	16	15	14	13

Figure 9. MCH Ballout (Top View — Right Side)

12	11	10	9	8	7	6	5	4	3	2	1	
ST0	RSTIN#	BNR#	VTT	DBSY#	HRCOMP0	VTT	HA21#	HA27#	VTT	HA22#	HA15#	AF
ST1	TESTIN#	DRDY#	RS2#	VSS	HSWNG0	ADS#	VSS	HA23#	HA18#	VSS	HA5#	AE
ST2	G_GNT#	VTT	HLOCK#	HA31#	CCVREF	HA19#	HA11#	VTT	HA30#	HA9#	VTT	AD
RBF#	G_REQ#	HITM#	VSS	CPURST#	HA29#	VSS	HA20#	HA24#	VSS	HREQ3#	HD60#	AC
PIPE#	BR0#	BPRI#	RS1#	VTT	HA28#	HA10#	VTT	HA8#	HA6#	VTT	HD63#	AB
WBF#	HIT#	VSS	HTRDY#	HA26#	VSS	HA17#	HA3#	VSS	HA7#	HD59#	VSS	AA
SBA0	RS0#	DEFER#	VTT	HADSTB1#	HA25#	VTT	HA4#	HREQ0#	VTT	HD58#	HD57#	Y
SBA1	VSS	BCLK1	BCLK0	VCC1_8	HA14#	HA12#	VSS	HD56#	HD61#	VSS		W
VSS	RESERVED	HAVREF1	VSS	HA13#	VTT	HREQ4#	HREQ2#	VTT	HD55#	VTT		V
VSS	VCC1_8	VCC1_8	HREQ1#	DBI3#	HA16#	VSS	HD49#	HD53#	VSS	HD54#	HD62#	U
VSS	VCC1_8	VCC1_8	VSS	HDVREF3	HADSTB0#	HD51#	VTT	HDSTBP3#	HD48#	VTT	HD52#	T
VCC1_8	VSS	VSS	VTT	DBI2#	VSS	HDSTBN3#	HD50#	VSS	HD47#	HD46#	VSS	R
VCC1_8	VSS	VSS	VSS	HDVREF2	HSWNG1	VTT	HD45#	HD40#	VTT	HD42#	HD44#	P
VSS	VCC1_8	VCC1_8	VTT	HAVREF0	HDSTBP2#	HDSTBN2#	VSS	HD35#	HD41#	VSS	HD43#	N
VSS	VCC1_8	VCC1_8	VSS	HDVREF1	VTT	HRCOMP1	HD28#	VTT	HD38#	HD37#	VTT	M
VCC1_8	VSS	VSS	VTT	DBI0#	DBI1#	VSS	HDSTBP1#	HD34#	VSS	HD33#	HD39#	L
VCC1_8	VSS	VSS	VSS	VTT	HDVREF0	HD19#	VTT	HDSTBN1#	HD29#	VTT	HD32#	K
VSS	VCC1_8	VCC1_8	VTT	HD13#	VSS	HDSTBN0#	HD21#	VSS	HD30#	HD26#	HD36#	J
VSS	VCC1_8	VCC1_8	VSS	HD7#	HDSTBP0#	VTT	HD16#	HD18#	VTT	HD25#		H
VSS	VSS	VSS	VTT	HD1#	HD3#	HD4#	VSS	HD12#	HD22#	VSS		G
RQ_B5	VSS	DQB_B0	VSS	DQB_B4	VSS	DQB_B7	HD9#	VTT	HD20#	HD27#	VTT	F
VSS	RQ_B3	VSS	VCC1_8	VSS	DQB_B8	VSS	CHB_RCLKOUT	HD11#	VSS	HD23#	HD31#	E
RESERVED	VSS	RQ_B1	VSS	DQB_B2	VSS	DQB_B3	CHB_HCLKOUT	HD15#	HD17#	VTT	HD24#	D
VSS	RESERVED	VSS	VCC1_8	VSS	DQB_B6	VSS	CMD_B	VSS	HD10#	HD14#	VSS	C
RQ_B6	VSS	RQ_B2	VSS	DQB_B1	VSS	DQB_B5	SIO_B	HD8#	VTT	HD5#	HD2#	B
VSS	RQ_B4	VSS	RQ_B0	VSS	VSS	VSS	SCK_B	HD0#	HD6#	VSS		A
12	11	10	9	8	7	6	5	4	3	2	1	

Table 31. MCH Ballout List (Alphabetical by Signal Name)

Name	Ball #
66IN	Vv
AD_STB0	AC23
AD_STB0#	AC22
AD_STB1	AB16
AD_STB1#	AB15
ADS#	AE6
BCLK0	W9
BCLK1	W10
BNR#	AF10
BPRI#	AB10
BR0#	AB11
CCVREF	AD7
CFM_A	P23
CFM_A#	P24
CFM_B	B14
CFM_B#	A14
CHA_HCLKOUT	E21
CHA_RCLKOUT	E20
CHA_VREF0	P21
CHA_VREF1	R21
CHB_HCLKOUT	D5
CHB_RCLKOUT	E5
CHB_VR	D15
CHB_VR	D14
CMD_A	E22
CMD_B	C5
CPURST#	AC8
CTM_A	R24
CTM_A#	R23
CTM_B	A15
CTM_B#	B15
DBI0#	L8
DBI1#	L7
DBI2#	R8
DBI3#	U8
DBSY#	AF8
DEFER#	Y10
DQA_A0	U21
DQA_A1	T20
DQA_A2	U23
DQA_A3	U19
DQA_A4	V22
DQA_A5	V20
DQA_A6	W23
DQA_A7	Wv19
DQA_A8	W21
DQA_B0	D17
DQA_B1	E16
DQA_B2	B17
DQA_B3	F17
DQA_B4	A18
DQA_B5	E18
DQA_B6	C18
DQA_B7	D19
DQA_B8	B19
DQB_A0	K19
DQB_A1	H23
DQB_A2	H21
DQB_A3	F21
DQB_A4	H19
DQB_A5	F23
DQB_A6	G22
DQB_A7	F19
DQB_A8	G20
DQB_B0	F10
DQB_B1	B8
DQB_B2	D8
DQB_B3	D6
DQB_B4	F8
DQB_B5	B6
DQB_B6	C7
DQB_B7	F6
DQB_B8	E7
DRDY#	AE10
G_AD0	AB24
G_AD1	Y24
G_AD2	AD24
G_AD3	AA22
G_AD4	AD23
G_AD5	AA24
G_AD6	AF23
G_AD7	AE24
G_AD8	AF22
G_AD9	AA21
G_AD10	Y22
G_AD11	AD21
G_AD12	AE21
G_AD13	AF21
G_AD14	AB21
G_AD15	AA20
G_AD16	AB18
G_AD17	AD18
G_AD18	AE18
G_AD19	AF18
G_AD20	Y17
G_AD21	AA17
G_AD22	AC17
G_AD23	AD17
G_AD24	AE16
G_AD25	AF16
G_AD26	AE15
G_AD27	AF15
G_AD28	Y14
G_AD29	AA14
G_AD30	AC14

Name	Ball #
G_AD31	AD14
G_C/BE0#	AE22
G_C/BE1#	AC20
G_C/BE2#	AA18
G_C/BE3#	AF17
G_DEVSEL#	AC19
G_FRAME#	AB19
G_GNT#	AD11
G_IRDY#	Y18
G_PAR	AF20
G_REQ#	AC11
G_TRDY#	Y20
GRCOMP	W13
GREF_0	W17
GREF_1	W14
GSTOP#	AF19
GSWNG	W15
HA3#	AA5
HA4#	Y5
HA5#	AE1
HA6#	AB3
HA7#	AA3
HA8#	AB4
HA9#	AD2
HA10#	AB6
HA11#	AD5
HA12#	W6
HA13#	V8
HA14#	W7
HA15#	AF1
HA16#	U7
HA17#	AA6
HA18#	AE3
HA19#	AD6
HA20#	AC5
HA21#	AF5

Name	Ball #
HA22#	AF2
HA23#	AE4
HA24#	AC4
HA25#	Y7
HA26#	AA8
HA27#	AF4
HA28#	AB7
HA29#	AC7
HA30#	AD3
HA31#	AD8
HADSTB0#	T7
HADSTB1#	Y8
HAVREF0	N8
HAVREF1	V10
HD0#	A4
HD1#	G8
HD2#	B1
HD3#	G7
HD4#	G6
HD5#	B2
HD6#	A3
HD7#	H8
HD8#	B4
HD9#	F5
HD10#	C3
HD11#	E4
HD12#	G4
HD13#	J8
HD14#	C2
HD15#	D4
HD16#	H5
HD17#	D3
HD18#	H4
HD19#	K6
HD20#	F3
HD21#	J5

Name	Ball #
HD22#	G3
HD23#	E2
HD24#	D1
HD25#	H2
HD26#	J2
HD27#	F2
HD28#	M5
HD29#	K3
HD30#	J3
HD31#	E1
HD32#	K1
HD33#	L2
HD34#	L4
HD35#	N4
HD36#	J1
HD37#	M2
HD38#	M3
HD39#	L1
HD40#	P4
HD41#	N3
HD42#	P2
HD43#	N1
HD44#	P1
HD45#	P5
HD46#	R2
HD47#	R3
HD48#	T3
HD49#	U5
HD50#	R5
HD51#	T6
HD52#	T1
HD53#	U4
HD54#	U2
HD55#	V3
HD56#	W4
HD57#	Y1

Name	Ball #
HD58#	Y2
HD59#	AA2
HD60#	AC1
HD61#	W3
HD62#	U1
HD63#	AB1
HDSTBN0#	J6
HDSTBN1#	K4
HDSTBN2#	N6
HDSTBN3#	R6
HDSTBP0#	H7
HDSTBP1#	L5
HDSTBP2#	N7
HDSTBP3#	T4
HDVREF0	K7
HDVREF1	M8
HDVREF2	P8
HDVREF3	T8
HIT#	AA11
HITM#	AC10
HL_A0	C23
HL_A1	B24
HL_A2	A24
HL_A3	A23
HL_A4	A22
HL_A5	A21
HL_A6	B21
HL_A7	A20
HL_A8	C20
HL_A9	D22
HL_A10	D21
HLA_STB	C21
HLA_STB#	B22
HLOCK#	AD9
HLRCOMP_A	D24
HLREF_A	D23

Name	Ball #
HRCOMP0	AF7
HRCOMP1	M6
HREQ0#	Y4
HREQ1#	U9
HREQ2#	V5
HREQ3#	AC2
HREQ4#	V6
HSWNG0	AE7
HSWNG1	P7
HTRDY#	AA9
NC	W18
NC	V18
PIPE#	AB12
RBF#	AC12
RESERVED	L22
RESERVED	M21
RESERVED	D12
RESERVED	V11
RESERVED	C11
RQ_A0	J24
RQ_A1	K21
RQ_A2	K23
RQ_A3	L20
RQ_A4	L24
RQ_A5	M19
RQ_A6	M23
RQ_A7	N20
RQ_B0	A9
RQ_B1	D10
RQ_B2	B10
RQ_B3	E11
RQ_B4	A11
RQ_B5	F12
RQ_B6	B12
RQ_B7	E13
RS0#	Y11

Name	Ball #
RS1#	AB9
RS2#	AE9
RSTIN#	AF11
SB_STB	AD13
SB_STB#	AC13
SBA0	Y12
SBA1	W12
SBA2	AF13
SBA3	AE13
SBA4	AB13
SBA5	AA13
SBA6	Y13
SBA7	AF14
SCK_A	E24
SCK_B	A5
SIO_A	E23
SIO_B	B5
ST0	AF12
ST1	AE12
ST2	AD12
TESTIN#	AE11
VCC1_8	B23
VCC1_8	T22
VCC1_8	N22
VCC1_8	J22
VCC1_8	J20
VCC1_8	B20
VCC1_8	R19
VCC1_8	P19
VCC1_8	R17
VCC1_8	P17
VCC1_8	L17
VCC1_8	K17
VCC1_8	R16
VCC1_8	P16
VCC1_8	L16

Name	Ball #
VCC1_8	K16
VCC1_8	C16
VCC1_8	V15
VCC1_8	U15
VCC1_8	T15
VCC1_8	N15
VCC1_8	M15
VCC1_8	J15
VCC1_8	H15
VCC1_8	F15
VCC1_8	U14
VCC1_8	T14
VCC1_8	N14
VCC1_8	M14
VCC1_8	J14
VCC1_8	H14
VCC1_8	F14
VCC1_8	R13
VCC1_8	P13
VCC1_8	L13
VCC1_8	K13
VCC1_8	C13
VCC1_8	R12
VCC1_8	P12
VCC1_8	L12
VCC1_8	K12
VCC1_8	U11
VCC1_8	T11
VCC1_8	N11
VCC1_8	M11
VCC1_8	J11
VCC1_8	H11
VCC1_8	U10
VCC1_8	T10
VCC1_8	N10
VCC1_8	M10

Name	Ball #
VCC1_8	J10
VCC1_8	H10
VCC1_8	E9
VCC1_8	C9
VCC1_8	W8
VDDQ	AC24
VDDQ	AE23
VDDQ	Y23
VDDQ	AB22
VDDQ	AC21
VDDQ	Y21
VDDQ	AE19
VDDQ	AD19
VDDQ	AA19
VDDQ	AE17
VDDQ	AB17
VDDQ	AD15
VDDQ	AC15
VDDQ	AA15
VDDQ	Y15
VDDQ	V13
VSS	AF24
VSS	U24
VSS	T24
VSS	N24
VSS	M24
VSS	K24
VSS	F24
VSS	C24
VSS	AB23
VSS	AA23
VSS	V23
VSS	T23
VSS	N23
VSS	L23
VSS	J23

Name	Ball #
VSS	G23
VSS	AD22
VSS	W22
VSS	U22
VSS	R22
VSS	P22
VSS	M22
VSS	K22
VSS	H22
VSS	F22
VSS	C22
VSS	V21
VSS	T21
VSS	N21
VSS	L21
VSS	J21
VSS	G21
VSS	AE20
VSS	AD20
VSS	AB20
VSS	W20
VSS	U20
VSS	R20
VSS	P20
VSS	M20
VSS	K20
VSS	H20
VSS	F20
VSS	D20
VSS	Y19
VSS	V19
VSS	T19
VSS	N19
VSS	L19
VSS	J19
VSS	G19

Name	Ball #
VSS	E19
VSS	C19
VSS	A19
VSS	AC18
VSS	U18
VSS	T18
VSS	R18
VSS	P18
VSS	N18
VSS	M18
VSS	L18
VSS	K18
VSS	J18
VSS	H18
VSS	G18
VSS	F18
VSS	D18
VSS	B18
VSS	V17
VSS	U17
VSS	T17
VSS	N17
VSS	M17
VSS	J17
VSS	H17
VSS	G17
VSS	E17
VSS	C17
VSS	A17
VSS	AD16
VSS	AC16
VSS	AA16
VSS	Y16
VSS	W16
VSS	U16
VSS	T16

Name	Ball #
VSS	N16
VSS	M16
VSS	J16
VSS	H16
VSS	G16
VSS	F16
VSS	D16
VSS	B16
VSS	A16
VSS	R15
VSS	P15
VSS	L15
VSS	K15
VSS	G15
VSS	E15
VSS	C15
VSS	AE14
VSS	AB14
VSS	V14
VSS	R14
VSS	P14
VSS	L14
VSS	K14
VSS	G14
VSS	E14
VSS	C14
VSS	U13
VSS	T13
VSS	N13
VSS	M13
VSS	J13
VSS	H13
VSS	G13
VSS	F13
VSS	D13
VSS	B13

Name	Ball #
VSS	A13
VSS	V12
VSS	U12
VSS	T12
VSS	N12
VSS	M12
VSS	J12
VSS	H12
VSS	G12
VSS	E12
VSS	C12
VSS	A12
VSS	W11
VSS	R11
VSS	P11
VSS	L11
VSS	K11
VSS	G11
VSS	F11
VSS	D11
VSS	B11
VSS	AA10
VSS	R10
VSS	P10
VSS	L10
VSS	K10
VSS	G10
VSS	E10
VSS	C10
VSS	A10
VSS	AC9
VSS	V9
VSS	T9
VSS	P9
VSS	M9
VSS	K9

Name	Ball #
VSS	H9
VSS	F9
VSS	D9
VSS	B9
VSS	AE8
VSS	E8
VSS	C8
VSS	A8
VSS	AA7
VSS	R7
VSS	J7
VSS	F7
VSS	D7
VSS	B7
VSS	A7
VSS	AC6
VSS	U6
VSS	L6
VSS	E6
VSS	C6
VSS	A6
VSS	AE5
VSS	W5
VSS	N5
VSS	G5
VSS	AA4
VSS	R4

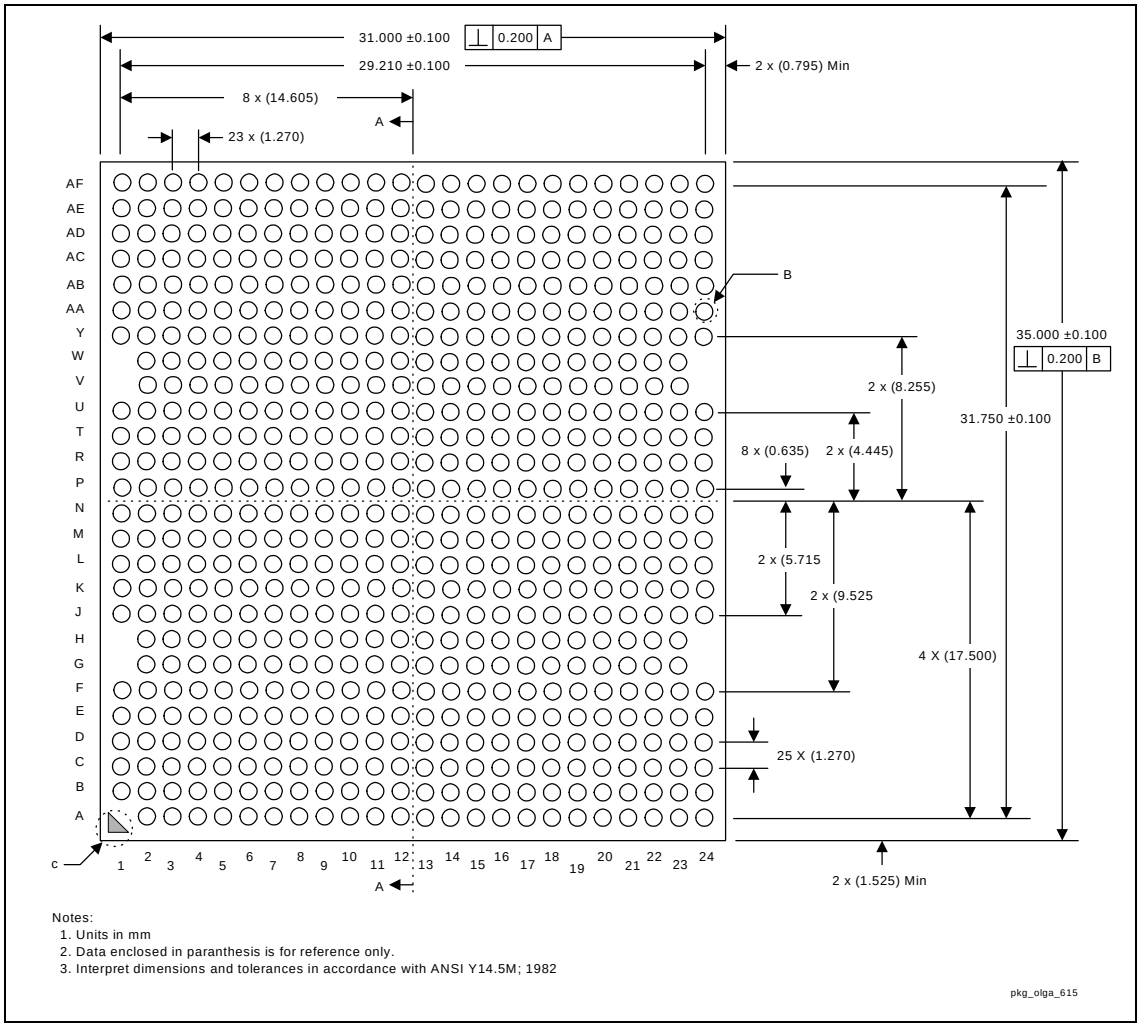
Name	Ball #
VSS	J4
VSS	C4
VSS	AC3
VSS	U3
VSS	L3
VSS	E3
VSS	AE2
VSS	W2
VSS	N2
VSS	G2
VSS	A2
VSS	AA1
VSS	R1
VSS	C1
VTT	AD10
VTT	AF9
VTT	Y9
VTT	R9
VTT	N9
VTT	L9
VTT	J9
VTT	G9
VTT	AB8
VTT	K8
VTT	V7
VTT	M7
VTT	AF6

Name	Ball #
VTT	Y6
VTT	P6
VTT	H6
VTT	AB5
VTT	T5
VTT	K5
VTT	AD4
VTT	V4
VTT	M4
VTT	F4
VTT	AF3
VTT	Y3
VTT	P3
VTT	H3
VTT	B3
VTT	AB2
VTT	V2
VTT	T2
VTT	K2
VTT	D2
VTT	AD1
VTT	M1
VTT	F1
WBF#	AA12

7.2. Package Information

This section shows the package information for the MCH. The package is a 31x35 mm 615 OLGA.

Figure 8. MCH Package Information



7.3. MCH RSL Package Dimensions

In this section, detailed information about the internal component package trace length to enable trace length compensation. Trace length compensation is very important to maximum design flexibility. These lengths must be considered when matching trace lengths as described in the platform design guide. Note that these lengths are normalized to 0 with the longest trace on the package. They do not represent the actual lengths from pad to ball.

The data given in the following sections can be renormalized to start routing from a different ball. If a different signal (other than longest trace) is used for nominalization, use the following equation:

$$\text{New } \Delta L_{pkg}' = \Delta L_{pkg} - \Delta L_{Ref}$$

ΔL_{Ref} is the reference signal used for nominalization For example: If signal MEMORY1 trace length is used for nominalization, then:

Table 32. Example Nominalization Table

	ΔL_{Pkg} (mils)	New ΔL_{Pkg} (mils)
MEMORY1	102.756	0.000
MEMORY2	118.897	16.141
MEMORY3	130.315	27.559
MEMORY4	152.364	49.608
.	.	.
.	.	.
.	.	.
MEMORYN	175.984	73.228

7.3.1. MCH RSL Compensation and Normalized Trace Length Data

To calculate the ΔL_{PCB} for RSL signals from the MCH to RIMMs, use the following formula.

$\Delta L_{PCB} = (\Delta L_{pkg} * V_{pkg}) / V_{PCB}$

- ΔL_{PCB} is the nominal Δ PCB trace length to be added on the PCB
- ΔL_{Pkg} is the nominal Δ package trace length of the MCH
- V_{pkg} is the package trace velocity of the MCH, and its the nominal value is 167.64 ps/in (6.6 ps/mm)
- V_{PCB} is the PCB trace velocity

Table 33. MCH ΔL_{Pkg} Data for Direct * Channels A and B

Channel A ΔL_{Pkg} Normalized to DQB_A5		
Signal	Ball No.	ΔL_{Pkg} (mils)
CFM_A	P23	158.780
CFM_A#	P24	91.969
CTM_A	R24	91.063
CTM_A#	R23	152.047
DQA_A0	U21	204.055
DQA_A1	T20	277.480
DQA_A2	U23	96.457
DQA_A3	U19	309.764
DQA_A4	V22	131.496
DQA_A5	V20	255.315
DQA_A6	W23	87.913
DQA_A7	W19	122.756
DQA_A8	W21	138.268
DQB_A0	K19	261.732
DQB_A1	H23	41.024
DQB_A2	H21	122.717
DQB_A3	F21	38.307
DQB_A4	H19	218.780
DQB_A5	F23	0.000
DQB_A6	G22	68.583
DQB_A7	F19	99.331
DQB_A8	G20	127.283
RQ_A0	J24	19.094
RQ_A1	K21	175.276
RQ_A2	K23	83.976
RQ_A3	L20	255.079
RQ_A4	L24	64.094
RQ_A5	M19	293.937
RQ_A6	M23	135.787
RQ_A7	N20	289.646

Channel B ΔL_{Pkg} Normalized to DQB_B5		
Signal	Ball No.	ΔL_{Pkg} (mils)
CFM_B	B14	115.354
CFM_B#	A14	62.362
CTM_B	A15	68.819
CTM_B#	B15	108.701
DQA_B0	D17	157.520
DQA_B1	E16	235.787
DQA_B2	B17	53.386
DQA_B3	F17	264.724
DQA_B4	A18	12.244
DQA_B5	E18	198.189
DQA_B6	C18	117.638
DQA_B7	D19	89.724
DQA_B8	B19	34.291
DQB_B0	F10	278.228
DQB_B1	B8	45.591
DQB_B2	D8	141.063
DQB_B3	D6	40.630
DQB_B4	F8	238.898
DQB_B5	B6	0.000
DQB_B6	C7	76.260
DQB_B7	F6	120.906
DQB_B8	E7	147.047
RQ_B0	A9	27.520
RQ_B1	D10	172.913
RQ_B2	B10	81.693
RQ_B3	E11	238.346
RQ_B4	A11	54.055
RQ_B5	F12	303.819
RQ_B6	B12	112.638
RQ_B7	E13	263.937

7.3.2. MCH System Bus Signal Normalized Trace Length Data

To calculate the ΔL_{PCB} for the system bus, first normalize the processor and MCH to the same signal within a group. Then follow the trace length equations documented in the *Intel® Pentium® 4 in the 423 pin package / Intel® 82850 Platform Design Guide or the Intel® Pentium® 4 in the 478 pin package / Intel® 850 Chipset Family Platform Design Guide*. Below is the MCH system bus interface normalized data per group.

Table 34. MCH System Bus Signal Normalized Trace Length Data per Group

HADSTB0# Group Normalized to HA15#		
Signal	**Ball No.**	**ΔL_{Pkg} (mils)**
HADSTB0#	T7	242.598
HA3#	AA5	321.732
HA4#	Y5	325.236
HA5#	AE1	4.409
HA6#	AB3	210.669
HA7#	AA3	271.142
HA8#	AB4	254.764
HA9#	AD2	69.370
HA10#	AB6	332.953
HA11#	AD5	124.882
HA12#	W6	519.331
HA13#	V8	473.661
HA14#	W7	467.244
HA15#	AF1	0.000
HA16#	U7	615.433
HREQ0#	Y4	291.063
HREQ1#	U9	37.244
HREQ2#	V5	404.921
HREQ3#	AC2	136.457
HREQ4#	V6	484.606

HADSTB1# Group Normalized to HA22#		
Signal	**Ball No.**	**ΔL_{Pkg} (mils)**
HADSTB1#	Y8	581.417
HA17#	AA6	476.299
HA18#	AE3	88.976
HA19#	AD6	305.512
HA20#	AC5	342.244
HA21#	AF5	146.772
HA22#	AF2	0.000
HA23#	AE4	234.882
HA24#	AC4	310.315
HA25#	Y7	550.472
HA26#	AA8	531.772
HA27#	AF4	182.756
HA28#	AB7	439.921
HA29#	AC7	390.827
HA30#	AD3	69.291
HA31#	AD8	336.890

HDSTBx3# Group Normalized to DBI3#		
Signal	**Ball No.**	**ΔL_{Pkg} (mils)**
HDSTBP3#	T4	451.299
HDSTBN3#	R6	588.543
HD48#	T3	336.929
HD49#	U5	439.016
HD50#	R5	518.583
HD51#	T6	226.654
HD52#	T1	286.535
HD53#	U4	340.079
HD54#	U2	288.189
HD55#	V3	307.638
HD56#	W4	320.236
HD57#	Y1	151.260
HD58#	Y2	166.181
HD59#	AA2	228.622
HD60#	AC1	86.654
HD61#	W3	319.488
HD62#	U1	224.094
HD63#	AB1	124.134
DBI3#	U8	0.000

Table 17. MCH System Bus Signal Normalized Trace Length Data per Group (continued)

HDSTBx2# Group Normalized to DBI2#		
Signal	Ball No.	ΔL_{Pkg} (mils)
HDSTBP2#	N7	469.213
HDSTBN2#	N6	432.244
HD32#	K1	108.701
HD33#	L2	182.165
HD34#	L4	174.409
HD35#	N4	303.031
HD36#	J1	36.142
HD37#	M2	138.701
HD38#	M3	217.992
HD39#	L1	111.772
HD40#	P4	330.709
HD41#	N3	185.118
HD42#	P2	173.307
HD43#	N1	95.827
HD44#	P1	169.291
HD45#	P5	369.291
HD46#	R2	132.165
HD47#	R3	165.827
DBI2#	R8	0.000

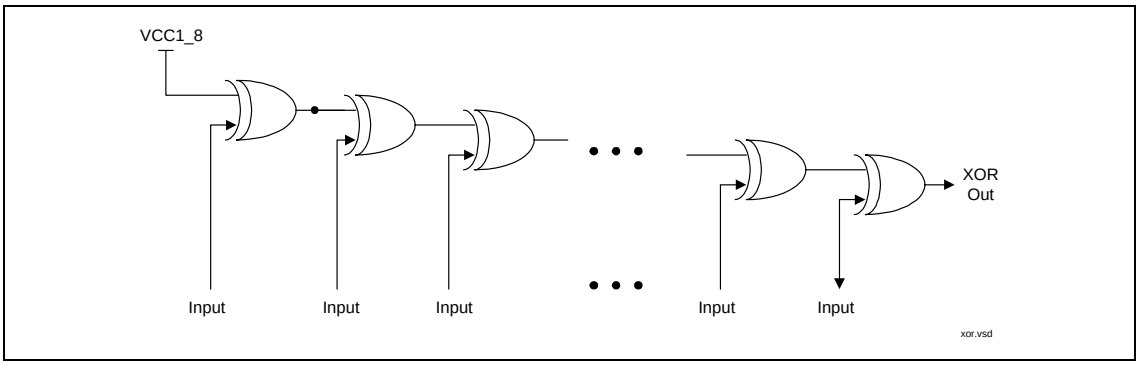
HDSTBx1# Group Normalized to HD24#		
Signal	Ball No.	ΔL_{Pkg} (mils)
HDSTBP1#	L5	558.543
HDSTBN1#	K4	496.850
HD16#	H5	494.803
HD17#	D3	207.441
HD18#	H4	408.583
HD19#	K6	578.031
HD20#	F3	269.685
HD21#	J5	501.890
HD22#	G3	330.669
HD23#	E2	190.866
HD24#	D1	0.000
HD25#	H2	268.465
HD26#	J2	330.591
HD27#	F2	227.480
HD28#	M5	567.047
HD29#	K3	429.606
HD30#	J3	400.591
HD31#	E1	68.937
DBI1#	L7	87.362

HDSTBx0# Group Normalized to HD2#		
Signal	Ball No.	ΔL_{Pkg} (mils)
HDSTBP0#	H7	521.299
HDSTBN0#	J6	555.906
HD0#	A4	122.283
HD1#	G8	539.488
HD2#	B1	0.000
HD3#	G7	494.291
HD4#	G6	457.598
HD5#	B2	73.780
HD6#	A3	42.756
HD7#	H8	595.000
HD8#	B4	159.449
HD9#	F5	345.354
HD10#	C3	126.496
HD11#	E4	215.433
HD12#	G4	338.425
HD13#	J8	643.425
HD14#	C2	47.244
HD15#	D4	215.039
DBI0#	L8	489.961

8. Testability

In the MCH, the testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-Tree is a chain of XOR gates, each with one input pin connected to it.

Figure 10. XOR-Tree Chain



The algorithm used for in-circuit test is as follows:

- Drive all Input pins to their initial logic level as indicated in the tables below. Observe the output.
- Toggle pins one at a time starting from the first pin continuing to the last pin from its initial logic level to its opposite level. Observe that the output changes with each pin toggle.
- Certain pin pairs must be toggled together. These pin pairs are: AD_STB0 and AD_STB0#, AD_STB1 and AD_STB1#, and SB_STB and SB_STB#. For example AD_STB0 has an initial state of 1 and AD_STB0# has an initial state of 0 when reaching AD_STB0, both AD_STB0 and AD_STB0# should be toggled together (AD_STB0: 1 -> 0 and AD_STB0#: 0 -> 1). When these pins are toggled together, the output will not change.
- It is important to use the initial input states found in the below tables.

The following pins must be connected to their proper circuit in order for the XOR chain to work:

- All reference voltage inputs
- All inputs must be driven to CMOS voltage levels (0-1.8V) regardless of signal type.

RSTIN#, TESTIN#, CFM_A, CFM_A#, CHA_REF[0:1], CFM_B, CFM_B#, CHB_REF[0:1] are not part of any XOR chain. This is in addition to SBA[0:7].

8.1. XOR Test Mode Initialization

The MCH uses a single pin (TESTIN#) to activate the XOR test mode.

- 32,771 clocks (66IN) after the de-assertion of PCI reset (IRSTIN#), drive TESTIN# from 1 to 0.
- Start to serially load the bits: 8010 0000 1000 0000 0000 3F0C 003C 0001h into the TESTIN# pin.
- Once in the XOR test mode, any high to low transition on TESTIN# will cause the serial test mode entry state machine to be activated. Care should be taken to keep TESTIN# stable after activating the XOR test mode.

8.2. XOR Chains

Table 35. XOR Chain 1

Chain 1	Ball	Element #	Note	Initial Logic Level
HA13#	V8	1	Input	1
HA14#	W7	2	Input	1
HA10#	AB6	3	Input	1
HA11#	AD5	4	Input	1
HA12#	W6	5	Input	1
HA16#	U7	6	Input	1
HA8#	AB4	7	Input	1
HA3#	AA5	8	Input	1
HA15#	AF1	9	Input	1
HREQ3#	AC2	10	Input	1
HADSTB0#	T7	11	Input	1
HA4#	Y5	12	Input	1
HA9#	AD2	13	Input	1
HA6#	AB3	14	Input	1
HREQ4#	V6	15	Input	1
HREQ0#	Y4	16	Input	1
HA7#	AA3	17	Input	1
HA5#	AE1	18	Input	1
HREQ1	U9	19	Input	1
HREQ2#	V5	20	Input	1
HD56#	W4	21	Input	1
HD59#	AA2	22	Input	1
HD60#	AC1	23	Input	1
HD61#	W3	24	Input	1

Chain 1	Ball	Element #	Note	Initial Logic Level
HD51#	T6	25	Input	1
HD49#	U5	26	Input	1
HD63#	AB1	27	Input	1
HD57#	Y1	28	Input	1
HD55#	V3	29	Input	1
HD58#	Y2	30	Input	1
HDSTBN3#	R6	31	Input	1
HDSTBP3#	T4	32	Input	1
HD53#	U4	33	Input	1
DBI3#	U8	34	Input	1
HD50#	R5	35	Input	1
HD54#	U2	36	Input	1
HD62#	U1	37	Input	1
HD48#	T3	38	Input	1
HD52#	T1	39	Input	1
HD46#	R2	40	Input	1
HD47#	R3	41	Input	1
HD44#	P1	42	Input	1
HD45#	P5	43	Input	1
HD43#	N1	44	Input	1
HD42#	P2	45	Input	1
HD40#	P4	46	Input	1
DBI2#	R8	47	Input	1
HD37#	M2	48	Input	1
HD41#	N3	49	Input	1
HD39#	L1	50	Input	1
HD35#	N4	51	Input	1
HD38#	M3	52	Input	1
HDSTBN2#	N6	53	Input	1
HDSTBP2#	N7	54	Input	1
SBA0	Y12	55	Output	N/A

Table 36. XOR Chain 2

Chain 2	Ball	Element #	Note	Initial Logic Level
HD32#	K1	1	Input	1
HD33#	L2	2	Input	1
HD34#	L4	3	Input	1
HD36#	J1	4	Input	1
HD31#	E1	5	Input	1
HD24#	D1	6	Input	1
HRCOMP1	M6	7	Input	1
HD28#	M5	8	Input	1
HD29#	K3	9	Input	1
HD25#	H2	10	Input	1
HD26#	J2	11	Input	1
DBI1#	L7	12	Input	1
HD30#	J3	13	Input	1
HD27#	F2	14	Input	1
HDSTBN1#	K4	15	Input	1
HDSTBP1#	L5	16	Input	1
HD22#	G3	17	Input	1
HD20#	F3	18	Input	1
HD21#	J5	19	Input	1
HD23#	E2	20	Input	1
HD18#	H4	21	Input	1
HD19#	K6	22	Input	1
HD16#	H5	23	Input	1
HD17#	D3	24	Input	1
HD2#	B1	25	Input	1
HD11#	E4	26	Input	1
HD14#	C2	27	Input	1
HD12#	G4	28	Input	1
HD5#	B2	29	Input	1
HD15#	D4	30	Input	1
HD10#	C3	31	Input	1
HDSTBN0#	J6	32	Input	1
HDSTBP0#	H7	33	Input	1
HD9#	F5	34	Input	1
HD6#	A3	35	Input	1

Chain 2	Ball	Element #	Note	Initial Logic Level
HD8#	B4	36	Input	1
HD4#	G6	37	Input	1
HD0#	A4	38	Input	1
HD3#	G7	39	Input	1
HD1#	G8	40	Input	1
HD13#	J8	41	Input	1
HD7#	H8	42	Input	1
DBI0#	L8	43	Input	1
CMD_B	C5	44	Input	1
SIO_B	B5	45	Input	1
SCK_B	A5	46	Input	1
CHB_HCLKOUT	D5	47	Input	1
CHB_RCLKOUT	E5	48	Input	1
HL_A7	A20	49	Input	1
HL_A8	C20	50	Input	1
HL_A5	A21	51	Input	1
HL_A6	B21	52	Input	1
HL_A4	A22	53	Input	1
HL_A3	A23	54	Input	1
SBA1	W12	55	Output	N/A

Table 37. XOR Chain 3

Chain 3	Ball	Element #	Note	Initial Logic Level
HL_A2	A24	1	Input	1
HLA_STB#	B22	2	Input	1
HLA_STB	C21	3	Input	0
HLRCOMP_A	D24	4	Input	1
HL_A9	D22	5	Input	1
HL_A0	C23	6	Input	1
HL_A1	B24	7	Input	1
HL_A10	D21	8	Input	1
CMD_A	E22	9	Input	1
SIO_A	E23	10	Input	1
SCK_A	E24	11	Input	1
CHA_RCLKOUT	E20	12	Input	1
CHA_HCLKOUT	E21	13	Input	1
G_AD1	Y24	14	Input	1
G_AD5	AA24	15	Input	1
G_AD0	AB24	16	Input	1
G_AD3	AA22	17	Input	1
G_AD10	Y22	18	Input	1
G_AD9	AA21	19	Input	1
G_AD14	AB21	20	Input	1
G_AD2	AD24	21	Input	1
G_AD15	AA20	22	Input	1
AD_STB0	AC23	23	Input	1
AD_STB0#	AC22	24	Input	0
G_AD4	AD23	25	Input	1
G_C/BE0#	AE22	26	Input	1
G_AD11	AD21	27	Input	1
G_AD7	AE24	28	Input	1
G_AD6	AF23	29	Input	1
G_AD8	AF22	30	Input	1
G_AD12	AE21	31	Input	1
G_C/BE1#	AC20	32	Input	1
G_AD13	AF21	33	Input	1
G_DEVSEL#	AC19	34	Input	1
G_FRAME#	AB19	35	Input	1

Chain 3	Ball	Element #	Note	Initial Logic Level
G_IRDY#	Y18	36	Input	1
G_TRDY#	Y20	37	Input	1
G_STOP#	AF19	38	Input	1
G_PAR	AF20	39	Input	1
G_C/BE2#	AA18	40	Input	1
G_AD20	Y17	41	Input	1
G_AD16	AB18	42	Input	1
G_AD21	AA17	43	Input	1
G_AD17	AD18	44	Input	1
G_AD18	AE18	45	Input	1
G_AD19	AF18	46	Input	1
G_AD23	AD17	47	Input	1
G_AD22	AC17	48	Input	1
AD_STB1	AB16	49	Input	1
AD_STB1#	AB15	50	Input	0
GRCOMP	W13	51	Input	1
G_C/BE3#	AF17	52	Input	1
G_AD24	AE16	53	Input	1
G_AD25	AF16	54	Input	1
SBA3	AE13	55	Output	N/A

Table 38. XOR Chain 4

Chain 4	Ball	Element #	Note	Initial Logic Level
G_AD27	AF15	1	Input	1
G_AD26	AE15	2	Input	1
G_AD30	AC14	3	Input	1
G_AD29	AA14	4	Input	1
G_AD28	Y14	5	Input	1
G_AD31	AD14	6	Input	1
SB_STB	AD13	7	Input	1
SB_STB#	AC13	8	Input	0
ST0	AF12	9	Input	1
ST1	AE12	10	Input	1
ST2	AD12	11	Input	1
RBF#	AC12	12	Input	1
G_GNT#	AD11	13	Input	1
PIPE#	AB12	14	Input	1
WBF#	AA12	15	Input	1
G_REQ#	AC11	16	Input	1
RESERVED	V11	17	Input	1
BRO#	AB11	18	Input	1
HTRDY#	AA9	19	Input	1
DRDY#	AE10	20	Input	1
HIT#	AA11	21	Input	1
HITM#	AC10	22	Input	1
BNR#	AF10	23	Input	1
HLOCK#	AD9	24	Input	1
BPRI#	AB10	25	Input	1
RS0#	Y11	26	Input	1
CPURST#	AC8	27	Input	1
DBSY#	AF8	28	Input	1
RS2#	AE9	29	Input	1
HRCOMP0	AF7	30	Input	1
RS1#	AB9	31	Input	1
DEFER#	Y10	32	Input	1
ADS#	AE6	33	Input	1
HA21#	AF5	34	Input	1
HA31#	AD8	35	Input	1

Chain 4	Ball	Element #	Note	Initial Logic Level
HA29#	AC7	36	Input	1
HA19#	AD6	37	Input	1
HA27#	AF4	38	Input	1
HA26#	AA8	39	Input	1
HA23#	AE4	40	Input	1
HADSTB1#	Y8	41	Input	1
HA20#	AC5	42	Input	1
HA18#	AE3	43	Input	1
HA22#	AF2	44	Input	1
HA30#	AD3	45	Input	1
HA24#	AC4	46	Input	1
HA25#	Y7	47	Input	1
HA28#	AB7	48	Input	1
HA17#	AA6	49	Input	1
SBA4	AB13	50	Output	N/A

Table 39. XOR Chain 5

Chain 5	Ball	Element #	Note	Initial Logic Level
DQA_A5	V20	1	Input	1
DQA_A3	U19	2	Input	1
DQA_A7	W19	3	Input	1
DQA_A6	W23	4	Input	1
DQA_A8	W21	5	Input	1
DQA_A0	U21	6	Input	1
DQA_A4	V22	7	Input	1
DQA_A1	T20	8	Input	1
DQA_A2	U23	9	Input	1
CTM_A	R24	10	Input	1
CTM_A#	R23	11	Input	1
RQ_A7	N20	12	Input	1
RESERVED	M21	13	Input	1
RQ_A6	M23	14	Input	1
RQ_A5	M19	15	Input	1
RQ_A4	L24	16	Input	1
RESERVED	L22	17	Input	1
RQ_A3	L20	18	Input	1
RQ_A0	J24	19	Input	1
RQ_A2	K23	20	Input	1
RQ_A1	K21	21	Input	1
DQA_B5	E18	22	Input	1
DQA_B1	E16	23	Input	1
DQA_B0	D17	24	Input	1
DQA_B6	C18	25	Input	1
DQA_B2	B17	26	Input	1
DQA_B3	F17	27	Input	1
DQA_B4	A18	28	Input	1
DQA_B8	B19	29	Input	1
DQA_B7	D19	30	Input	1
SBA6	Y13	31	Output	N/A

Table 40. XOR Chain 6

Chain 6	Ball	Element #	Note	Initial Logic Level
DQB_A5	F23	1	Input	1
DQB_A3	F21	2	Input	1
DQB_A7	F19	3	Input	1
DQB_A6	G22	4	Input	1
DQB_A8	G20	5	Input	1
DQB_A0	K19	6	Input	1
DQB_A4	H19	7	Input	1
DQB_A1	H23	8	Input	1
DQB_A2	H21	9	Input	1
CTM_B	A15	10	Input	1
CTM_B#	B15	11	Input	1
RQ_B7	E13	12	Input	1
RESERVED	D12	13	Input	1
RQ_B6	B12	14	Input	1
RQ_B5	F12	15	Input	1
RQ_B4	A11	16	Input	1
RESERVED	C11	17	Input	1
RQ_B3	E11	18	Input	1
RQ_B0	A9	19	Input	1
RQ_B2	B10	20	Input	1
RQ_B1	D10	21	Input	1
DQB_B5	B6	22	Input	1
DQB_B1	B8	23	Input	1
DQB_B0	F10	24	Input	1
DQB_B6	C7	25	Input	1
DQB_B2	D8	26	Input	1
DQB_B3	D6	27	Input	1
DQB_B4	F8	28	Input	1
DQB_B8	E7	29	Input	1
DQB_B7	F6	30	Input	1
SBA7	AF14	31	Output	N/A