Intel® 815G Chipset Platform

For Use with Universal Socket 370

Design Guide

September 4, 2002

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Revision History

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298253-001	Initial Release.	September 6, 2001
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1 Introduction

1.1 Design Guide and Chipset Basic Information

This design guide organizes Intel's design recommendations for the Intel® 82815G chipset platform for use with the Universal Socket 370. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document also addresses system design issues such as thermal requirements for 82815G chipset systems.

This document contains design recommendations, debug recommendations, and a system checklist. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues.

Consult the debug recommendations when debugging your design. However, these debug recommendations should be understood before completing board design, to ensure that the debug port, in addition to other debug features, are implemented correctly.

There is no AGP port capability in the 82815G GMCH. The 82815G GMCH uses internal graphics only.

There are six chipsets in the Intel® 815 chipset family:

- Intel® 82815 chipset: This chipset contains the Intel 82815 and the Intel 82801AA ICH.
- Intel® 82815E chipset: This chipset contains the Intel 82815E and the Intel 82801BA ICH2.
- Intel® 82815P chipset: This chipset contains the Intel 82815P and the Intel 82801AA ICH. There is no internal graphics capability. This GMCH uses an AGP port only.
- Intel® 82815EP chipset: This chipset contains the Intel 82815EP and the Intel 82801BA ICH2. There is no internal graphics capability. This GMCH uses an AGP port only.
- Intel® 82815G chipset: This chipset contains the Intel 82815G GMCH and Intel 82801AA ICH. There is no AGP port capability. This GMCH uses internal graphics only.
- Intel® 82815EG chipset. This chipset contains the Intel 82815EG GMCH and Intel 82801BA ICH2. There is no AGP port capability. This GMCH uses internal graphics only.

The only component difference between the 82815 GMCH and the 82815E GMCH is the I/O Controller Hub. The only component difference between the 82815P GMCH and the 82815EP GMCH is the I/O Controller Hub. The only component difference between the 82815G GMCH and the 82815EG GMCH is the I/O Controller Hub.

The 815G chipset platform supports the following processors:

- Intel® Pentium® III processor based on 0.18 micron technology (CPUID = 068xh).
- Intel® Celeron™ processor based on 0.18 micron technology (CPUID = 068xh). This applies to Celeron 533A MHz and ≥566 MHz processors
- Future 0.13 micron socket 370 processors

Note: The system bus speed supported by the design is based on the capabilities of the processor, chipset, and clock driver.

Note: The 815G chipset for use with the universal socket 370 is **not** compatible with the Intel® Pentium® II processor (CPUID = 066xh) 370-pin socket.

1.2 Terminology

This section describes some of the terms used in this document. Additional power delivery term definitions are provided at the beginning of *Chapter 12, Power Delivery*.

Term	Description
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGP	Accelerated Graphics Port
AGTL/AGTL+	Refers to processor bus signals that are implemented using either Assisted Gunning Transceiver Logic (AGTL+) or its lower voltage variant (AGTL), depending on which processor is being used.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk–coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Crosstalk–coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
GMCH	Graphics and Memory Controller Hub. A component of the Intel® 815 chipset platform for use with the Universal Socket 370
ICH	Intel® 82801AA I/O Controller Hub component.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network Length	The distance between agent 0 pins and the agent pins at the far end of the bus.

Term	Description
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on a substrate such as the motherboard. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) Effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or “push-out”), or a decrease in propagation delay (or “pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
System Bus	The system bus is the processor bus.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.
Universal Socket 370	Refers to the 815 chipset using the “universal” PGA370 socket. In general, these designs support 66/100/133 MHz system bus operation, VRM 8.5 DC-DC converter guidelines, and Intel® Celeron™ processors (CPUID=068xh), Intel® Pentium® III processor (CPUID=068xh), and future Pentium® III and Celeron™ processors using 0.13 micron technology in single-microprocessor based designs.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

1.3 Reference Documents

Document	**Document Number / Location**
Intel® 815 Chipset Family: 82815G/82815EG Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet	290714
Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet	290658
Intel® 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub Datasheet	290655
Pentium® II Processor Developer's Manual	243341
Pentium® III Processor Specification Update (latest revision from website)	(http://developer.intel.com/design/PentiumIII/specupdt/)
AP 907 Pentium® III Processor Power Distribution Guidelines	245085
AP-585 Pentium® II Processor AGTL+ Guidelines	243330
AP-587 Pentium® II Processor Power Distribution Guidelines	243332
Accelerated Graphics Port Specification, Revision 2.0	http://www.intel.com/technology/agp/agp_index.htm)
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/specifications/conventional_pci
Universal Serial Bus Specification, Revision 1.0	http://www.usb.org/developers/usb20/
AC '97 Component Specification, Revision 2.2(1)	http://developer.intel.com/pc-supp/platform/ac97/index.htm

NOTES:

1. Throughout this document, this specification will be referred to as *AC '97 v2.2*

1.4 System Overview

The 815G chipset for use with the Universal Socket 370 contains a Graphics Memory Controller Hub (GMCH) component and I/O Controller Hub (ICH) component for desktop platforms.

The GMCH provides the processor interface for uni-processor systems, (optimized for future 0.13 micron Celeron and Pentium III socket 370 processors and the Pentium III processor (CPUID = 068xh)), DRAM interface, hub interface, and internal graphics. It does not provide support for an external AGP port. This product provides flexibility and scalability in memory subsystem performance. PC100 SDRAM system memory may be scaled to PC133 system memory.

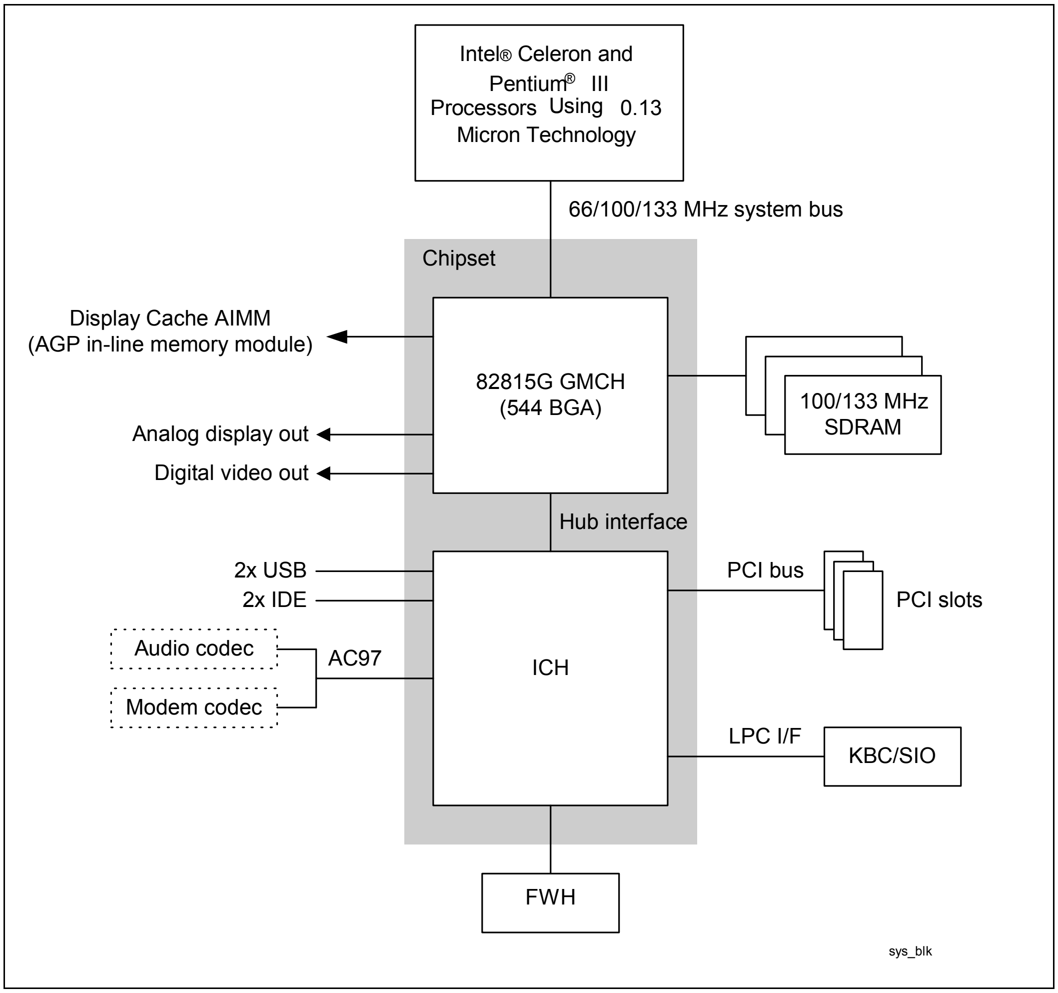
The Accelerated Hub Architecture interface (i.e., the chipset component interconnect) is designed into the chipset to provide an efficient, high-bandwidth communication channel between the GMCH and the I/O controller hub. The chipset architecture also enables a security and manageability infrastructure through the Firmware Hub component.

An ACPI-compliant 82815G chipset platform for use with the universal socket 370 can support the *Full-on (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4),* and *Soft-off (S5)* power management states. The chipset also supports *Wake-on-LAN** for remote administration and troubleshooting. The chipset architecture removes the requirement of the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC '97 allows the OEM to use *software-configurable* AC '97 audio and modem coder/decoders (codecs), instead of the traditional ISA devices.

1.4.1 System Features

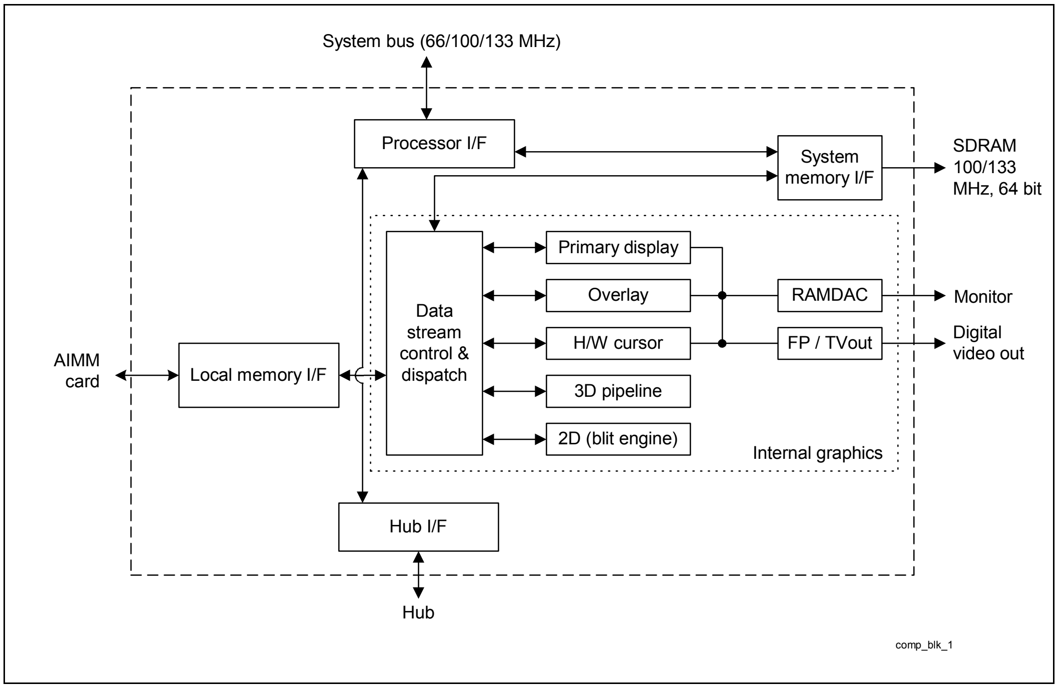
The 815G chipset for use with the Universal Socket 370 platform contains two components: the 82815G Graphics and Memory Controller Hub (GMCH) and the 82801AA I/O Controller Hub (ICH). The GMCH integrates a 66/100/133 MHz, P6 family system bus controller, integrated 2D/3D graphics accelerator, 100/133 MHz SDRAM controller, and a high-speed accelerated hub architecture interface for communication with the ICH. The ICH integrates an Ultra ATA/66 controller, USB host controller, LPC interface controller, FWH interface controller, PCI interface controller, AC '97 digital controller, and a hub interface for communication with the GMCH.

Figure 1. System Block Diagram



1.4.2 Component Features

Figure 2. GMCH Block Diagram



1.4.2.1 Graphics Memory Controller Hub (GMCH)

- Processor/System Bus Support
  - Optimized for Celeron and Pentium III processors which use 0.13 micron technology at 133MHz system bus frequency
  - Support for Celeron and Pentium III processors (CPUID = 068xh); at 66 MHz system bus frequency
  - Supports 32-bit AGTL or AGTL+ bus addressing
  - Supports uniprocessor systems
  - Utilizes AGTL and AGTL+ bus driver technology (gated AGTL/AGTL+ receivers for reduced power)
- Integrated DRAM controller
  - 32 MB to 512 MB using 16-Mb/64-Mb/128-Mb technology
  - Supports up to three double-sided DIMMS (six rows)
  - 100 MHz, 133 MHz SDRAM interface
  - 64-bit data interface
  - Standard Synchronous DRAM (SDRAM) support (x-1-1-1 access)
  - Supports only 3.3 V DIMM DRAM configurations
  - No registered DIMM support
  - Support for symmetrical and asymmetrical DRAM addressing
  - Support for x8, x16 DRAM device width
  - Refresh mechanism: CAS-before-RAS only
  - Support for DIMM serial PD (presence detect) scheme via SMbus interface
  - STR power management support via self-refresh mode using CKE

- Integrated Graphics Controller
  - Full 2D/3D/DirectX acceleration
  - Texture-mapped 3D with point sampled, bilinear, trilinear, and anisotropic filtering
  - Hardware setup with support for strips and fans
  - Hardware motion compensation assist for software MPEG/DVD decode
  - Digital Video Out interface adds support for digital displays and TV-Out
  - PC99A/PC2001 compliant
  - Integrated 230 MHz DAC
- Integrated Local Graphics Memory Controller (Display Cache)
  - 0 MB to 4 MB (via Graphics Performance Accelerator) using zero, one, or two parts
  - 32-bit data interface
  - 133 MHz memory clock
  - Supports ONLY 3.3 V SDRAMs
- Packaging/Power
  - 544 BGA with local memory port
  - 1.85 V (± 3% within margins of 1.795 V to 1.9 V) core and mixed 3.3 V, 1.5 V, and AGTL/AGTL+ I/O

1.4.2.2 Intel® 815 to Intel® 815G Signal Name Changes

Intel 82815 pins associated with AGP signals have name changes. The following table shows the old 82815 signal name, the ball number, and the new 82815G signal name. New designs for new 815G boards should use pull-ups or pull-downs as indicated by the 815G signal name. 815 boards using 815G devices may leave the associated 815 pins in the original 815 configuration.

Table 1. Intel® 82815 to Intel® 82815G Pin Name Changes

Intel® 815 Signal Name	Ball#	Intel® 815G Signal Name
WBF#	AB24	PU
AD_STB0	M22	PD
AD_STB0#	L23	PU
AD_STB1	U22	PD
AD_STB1#	V23	PU
SB_STB	Y23	PD
SB_STB#	AA24	PU
GRCOMP	J26	PD40
AGPREF	J24	0.5VDDQ
G_GNT#	AD25	NC
G_AD[24]	V25	PD

NOTES:

NC = No Connect. These pins should float

PU = Pull-up to 3.3 V through a weak pull-up resistor. (8.2 kΩ to 10 kΩ resistor.)

PD = Pull-down. These pins should be pulled down to ground through a weak pull-down resistor. (8.2 kΩ to 10 kΩ resistor.)

PD40 = Pull-down to VSS using a 40 Ω resistor.

0.5VDDQ = Set to 50% of the VDDQ voltage supply level.

1.4.2.3 Intel® 82801AA I/O Controller Hub (ICH)

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system, as follows:

- Upstream accelerated hub architecture interface for access to the GMCH
- PCI 2.2 interface (6 PCI Request/Grant pairs)
- Bus master IDE controller; supports Ultra ATA/66
- USB controller
- I/O APIC
- SMBus controller
- FWH interface
- LPC interface
- *AC '97 Component Specification, Revision 2.2* interface
- Integrated system management controller
- Alert on LAN*
- IRQ controller

- Packaging/Power
  - 241 BGA
  - 3.3 V core and 1.8 V and 3.3 V standby

1.4.2.4 Firmware Hub (FWH)

The hardware features of the firmware hub include:

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 GPIs

- Packaging/Power
  - 40-L TSOP and 32-L PLCC
  - 3.3 V core and 3.3 V / 12 V for fast programming

1.4.3 Platform Initiatives

1.4.3.1 Universal Socket 370 Design

The 815G chipset platform for use with the Universal Socket 370 allows systems designers to build one system that is compatible with the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors. When implemented, the 815G chipset platform for use with the Universal Socket 370 can detect which processor is present in the socket and function accordingly.

1.4.3.2 Intel® PC 133

The PC133 initiative provides the memory bandwidth necessary to obtain high performance from the processor and AGP graphics controllers. The platform's SDRAM interface supports 100 MHz and 133 MHz operations. The latter delivers 1.066 GB/s of theoretical memory bandwidth compared with the 800-MB/s theoretical memory bandwidth of 100 MHz SDRAM systems.

1.4.3.3 Accelerated Hub Architecture Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge becomes significant. With the addition of AC '97 and Ultra ATA/66, coupled with the existing USB, I/O requirements could affect PCI bus performance. The chipset platform's *accelerated hub architecture* ensures that the I/O subsystem, both PCI and integrated I/O features (IDE, AC '97, USB), receives adequate bandwidth. By placing the I/O bridge on the accelerated hub architecture interface instead of PCI, I/O functions integrated into the ICH and the PCI peripherals are ensured the bandwidth necessary for peak performance.

1.4.3.4 Internet Streaming SIMD Extensions

The Pentium III processor (CPUID = 068xh) provides 70 new SIMD (single-instruction, multiple-data) instructions. The new extensions are floating-point SIMD extensions. Intel® MMX™ technology provides integer SIMD instructions. The Internet Streaming SIMD extensions complement the MMX technology SIMD instructions and provide a performance boost to floating-point-intensive 3D applications.

1.4.3.5 Manageability

The 815G chipset platform integrates several functions designed to manage the system and lower the system's total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lock-ups, without the aid of an external microcontroller.

TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

Processor Present Indicator

The ICH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH will reboot the system.

Function Disable

The ICH provides the ability to disable the following functions: AC '97 Modem, AC '97 Audio, IDE, USB, and SMBus. Once disabled, these functions no longer decode I/O, memory or PCI configuration space. Also, no interrupts or power management events are generated by the disabled functions.

Intruder Detect

The ICH provides an input signal (INTRUDER#) that can be attached to a switch that is activated when the system case is opened. The ICH can be programmed to generate an SMI# or TCO event as the result of an active INTRUDER# signal.

Alert on LAN*

The ICH supports Alert on LAN. In response to a TCO event (intruder detect, thermal event, processor boot failure), the ICH sends a hard-coded message over the SMBus. A LAN controller supporting the Alert on LAN protocol can decode this SMBus message and send a message over the network to alert the network manager.

1.4.3.6 AC ’97

The *AC ’97v2.2* defines a digital interface that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC) or both an AC and an MC. The *AC ’97v2.2* defines the interface between the system logic and the audio or modem codec, known as the “AC-link.”

The chipset platform’s AC ’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC-link. Using the chipset’s integrated AC-link reduces cost and eases migration from ISA.

The ICH is an *AC ’97v2.2* -compliant controller that supports up to two codecs, with independent PCI functions for audio and modem. The ICH communicates with the codec(s) via a digital serial link called the AC-link. All digital audio/modem streams and command/status information are communicated over the AC-link. Microphone input and left and right audio channels are supported for a high-quality, two-speaker audio solution. Wake-on-ring-from-suspend also is supported with an appropriate modem codec.

By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC ’97. The chipset platform’s integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec or a modem with a modem codec. For systems requiring both audio and a modem, there are two solutions: the audio codec and the modem codec can be integrated into an AMC, or separate audio and modem codecs can be connected to the ICH.

Modem implementation for different countries must be taken into consideration, as telephone systems may vary. By implementing a split design, the audio codec can be on board and the modem codec can be placed on a riser. Intel is developing an AC-link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

1.4.3.7 Low-Pin-Count (LPC) Interface

In the 815G chipset platform, the Super I/O (SIO) component has migrated to the Low-Pin-Count (LPC) interface. Migration to the LPC interface allows for lower-cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended, because the AC ’97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of the devices offered and the features supported.

In addition, depending on system requirements, specific system I/O requirements may be integrated into the LPC Super I/O. For example, a USB hub may be integrated to connect to the ICH USB output and extend it to multiple USB connectors. Other SIO integration targets include a device bay controller or an ISA-IRQ-to-serial-IRQ converter to support a PCI-to-ISA bridge. Contact your Super I/O vendor to ensure the availability of the desired LPC Super I/O features.

2 General Design Considerations

This document provides motherboard layout and routing guidelines for systems based on the 815G chipset platform for use with the Universal Socket 370. The document does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations be completed for each design. Even when the guidelines are followed, it is recommended that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from these guidelines should be simulated.

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the "nominal" trace impedance for a 5-mil-wide trace. That is, it is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace, based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce the settling time.

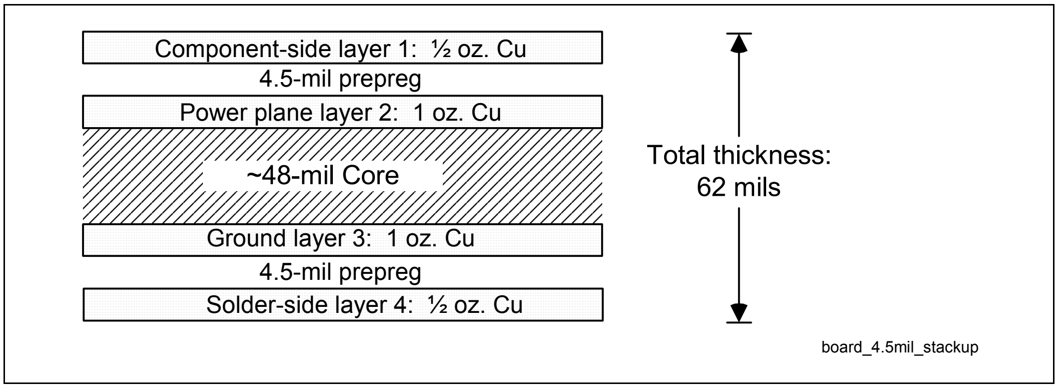
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, the routing guidelines in this document are created using a PCB *stack-up* similar to that described in the following section.

2.1 Nominal Board Stackup

The 815G chipset platform requires a board stack-up yielding a target impedance of 60 Ω ± 15%, with a 5-mil nominal trace width. Figure 3 shows an example stack-up that achieves this. It is a 4-layer printed circuit board (PCB) construction using 53%-resin, FR4 material.

Figure 3. Board Construction Example for 60 Ω Nominal Stackup



2.2 Future Designs Require Pull-Ups and Pull-Downs on any Unused Input and I/O Pins

Any new 815G platform Universal Socket 370 design should insure no input or I/O pin is left floating. For example, the TVCLKIN/INT# pin on many current 815 designs is left floating. This pin should be pulled up to 1.8 V by a weak pull-up resistor (8.2 kΩ to 10 kΩ) on any future 815G Universal Socket 370 design.

2.3 Support for P-MOS Kicker "ON": SMAA[9] Is Strapped High by an Internal 50 kΩ Pull-Up Resistor

The PSB P-MOS Kicker circuit should be enabled on all new, future 82815G Universal Socket 370 designs. Use of the P-MOS Kicker circuit improves PSB timings by improving AGTL and AGTL+ signal flight time. The 82815G SMAA[9] is strapped high through an internal 50 kΩ pull-up resistor to enable the PSB P-MOS Kicker.

Existing 815 designs which have implemented the pull-down resistor circuit on the SMAA[9] signal as shown in the 815 Customer Reference Board schematics and populated the resistor site to over-ride the internal pull-up resistor, may depopulate the site to enable the P-MOS Kicker circuit. This activity should be based on timing analysis of the specific platform.

P-MOS Kicker circuit "ON" is the recommended setting for 82815G Universal Socket 370 designs using future 0.13 micron technology processors.

3 Component Quadrant Layouts

Figure 4 illustrates the relative signal quadrant locations on the GMCH ballout. It does not represent the actual ballout. Refer to the *Intel® 815 Chipset Family: 82815G/82815EG Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet* for the actual ballout.

Figure 4. GMCH 544-Ball µBGA* CSP Quadrant Layout (Top View)

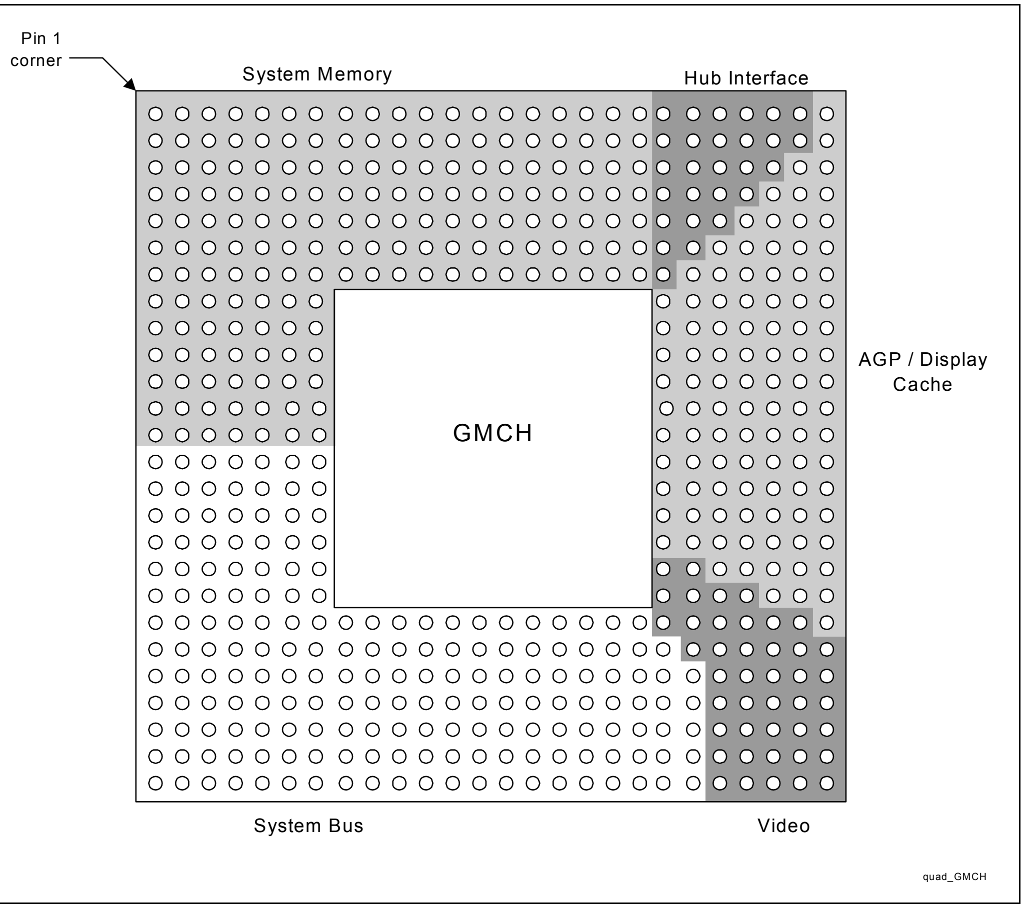


Figure 5 illustrates the relative signal quadrant locations on the ICH ballout. It does not represent the actual ballout. Refer to the *Intel® 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub Datasheet* for the actual ballout.

Figure 5. Intel® ICH 241-Ball µBGA* CSP Quadrant Layout (Top View)

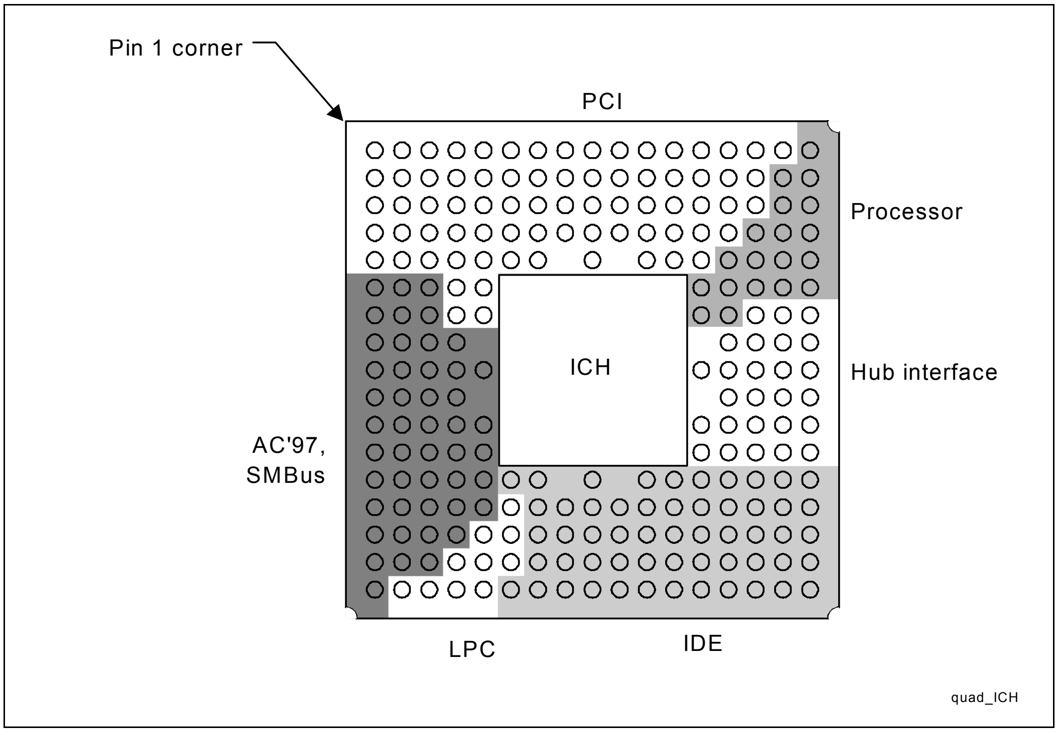
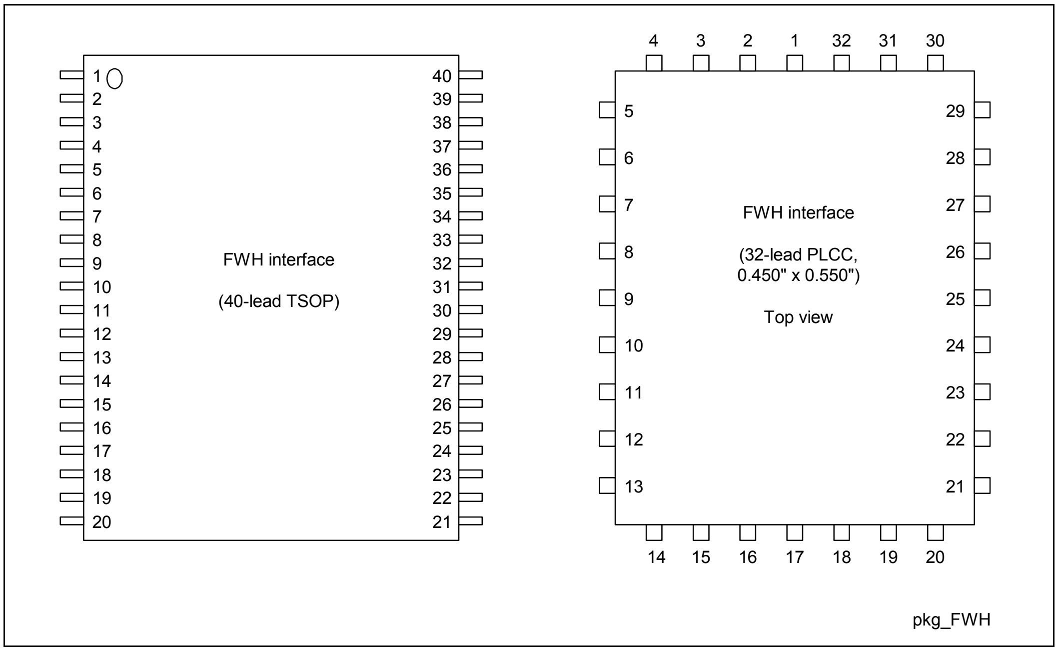


Figure 6. Firmware Hub (FWH) Packages



4 Universal Socket 370 Design

4.1 Universal Socket 370 Definitions

The universal socket 370 platform supports Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors. The Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) have different requirements for functioning properly in a platform than the future 0.13 micron socket 370 processors. It is necessary to understand these differences and how they affect the design of the platform. Refer to Table 2 through Table 5 for a high-level description of the differences that require additional circuitry on the motherboard. Specific details on implementing this circuitry are discussed further in this chapter. For a detailed description of the differences between the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processor pins, refer to Section 5.4.

Table 2. Processor Considerations for Universal Socket 370 Design

Signal Name or Pin Number	Function In Intel® Pentium® III Processor (CPUID=068xh) and Intel® Celeron™ Processor (CPUID=068xh)	Function In Future 0.13 Micron Socket 370 Processors	Implementation for Universal Socket 370 Design
AF36	VSS	DETECT	Addition of circuitry that generates a processor identification signal used to configure board-level operation.
AG1	VSS	VTT	Addition of FET switch to ground or VTT, controlled by processor identification signal. **Note:** FET must have no more than 100 milliohms resistance between source and drain.
AJ3	VSS	RESET2#	Addition of stuffing option for pull-down to ground, which lets designer prevent future 0.13 micron socket 370 processors from being used with incompatible stepping of Intel® 82815G GMCH.
AK22	GTL_REF	VCMOS_REF	Addition of resistor-divider network to provide 1.0 V, which will satisfy voltage tolerance requirements of the Intel® Pentium® III processor (CPUID=068xh) and Intel® Celeron™ processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors.
PICCLK	Requires 2.5 V	Requires 2.0 V	Addition of FET switch to provide proper voltage, controlled by processor identification signal.

Signal Name or Pin Number	Function In Intel® Pentium® III Processor (CPUID=068xh) and Intel® Celeron™ Processor (CPUID=068xh)	Function In Future 0.13 Micron Socket 370 Processors	Implementation for Universal Socket 370 Design
PWRGOOD	Requires 2.5 V	Requires 1.8 V	Addition of resistor-divider network to provide 2.1V, which will satisfy voltage tolerance requirements of the Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors.
VTT	Requires 1.5 V	Requires 1.25 V	Modification to VTT generation circuit to switch between 1.5 V or 1.25 V, controlled by processor identification signal.
VTTPWRGD	Not used	Input signal to future 0.13 micron socket 370 processors to indicate that VID signals are stable	Addition of VTTPWRGD generation circuit.

Table 3. GMCH Considerations for Universal Socket 370 Design

Pin Name/Number	Issue	Implementation For Universal Socket 370 Design
SMAA12	New strap required for determining Pentium® III Processor (CPUID=068xh) and Intel® Celeron™ Processor (CPUID=068xh) or Future 0.13 micron socket 370 processors	Addition of FET switch controlled by processor identification signal.

Table 4. Intel® ICH Considerations for Universal Socket 370 Design

Signal	Issue	Implementation For Universal Socket 370 Design
PWROK	GMCH and Intel® CK-815 must not sample BSEL[1:0] until VTTPWRGD asserted. ICH must not initialize before CK-815 clocks stabilize	Addition of circuitry to have VTTPWRGD gate PWROK from power supply to ICH. The ICH will hold the GMCH in reset until VTTPWRGD asserted plus 20 ms time delay to allow CK-815 clocks to stabilize.

Table 5. Clock Synthesizer Considerations for Universal Socket 370 Design

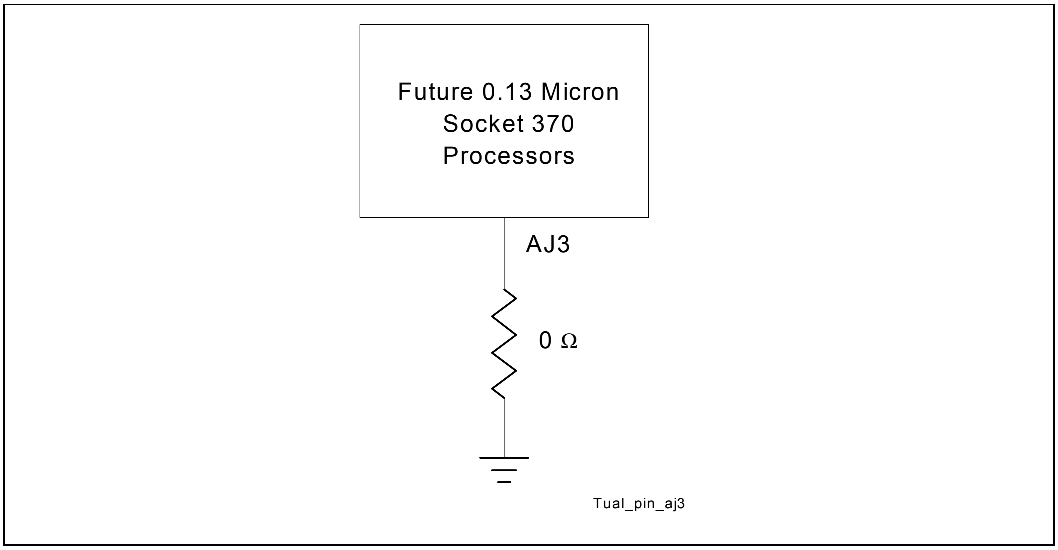
Signal	Issue	Implementation For Universal Socket 370 Design
VDD	Intel® CK-815 does not support VTTPWRGD	Addition of FET switch which supplies power to VDD only when VTTPWRGD is asserted. **Note:** FET must have no more than 100 milliohms resistance between source and drain.

4.2 Processor Design Requirements

4.2.1 Use of Universal Socket 370 Design with Incompatible GMCH

The universal socket 370 design is intended for use with the 815G chipset platform for use with the universal socket 370. A universal socket 370 design populated with an earlier stepping of the GMCH is not compatible with future 0.13 micron socket 370 processors and, if used, will cause eventual failure of these processors. To prevent a future 0.13 micron socket 370 processor from being used with an incompatible stepping of the GMCH, the recommendation is to lay out the site for a 0 Ω pull-down to ground on processor pin AJ3. This pin is a RESET# signal on future 0.13 micron socket 370 processors and, by populating the resistor, these future processors will be prevented from functioning when placed in a board with an incompatible stepping of the GMCH. All Pentium III (CPUID=068xh) and Celeron (CPUID=068xh) processors will continue to boot normally. Not populating the resistor will allow future 0.13 micron socket 370 processors to boot. Refer to Figure 7 for an example implementation.

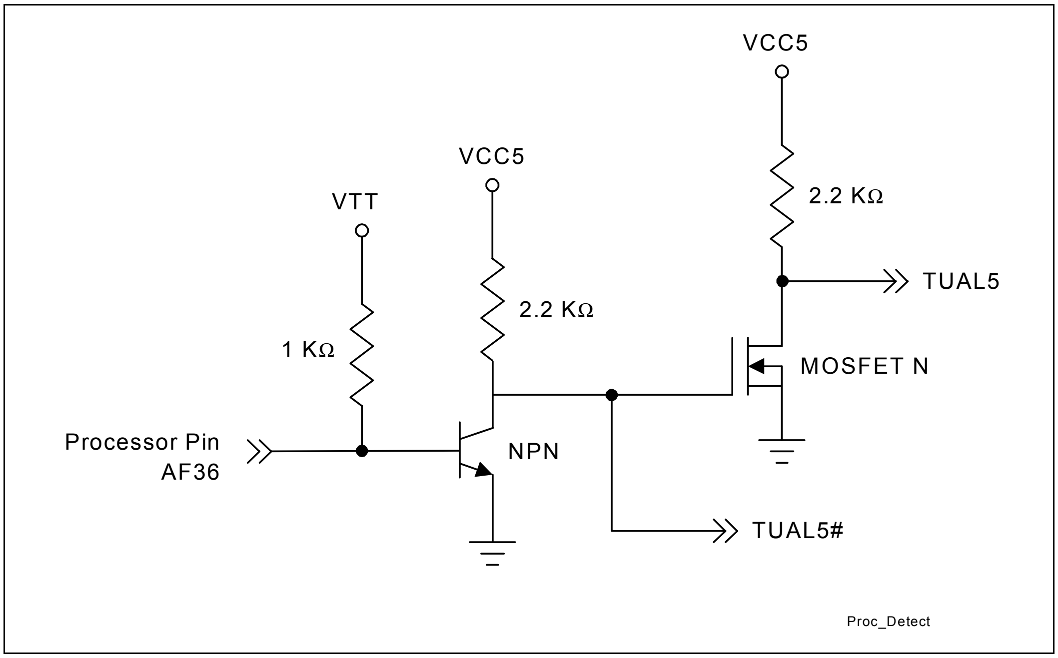
Figure 7. Future 0.13 Micron Socket 370 Processor Safeguard for Universal Socket 370 Designs Using A-2 GMCH



4.2.2 Identifying the Processor at the Socket

For the platform to configure for the requirements of the processor in the socket, it must first identify whether the processor is a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), or a future 0.13 micron socket 370 processors. Pin AF36 is a ground pin on a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh); pin AF36 is a detect pin on future 0.13 micron Socket 370 processors. Referring to Figure 8, the platform uses a detect circuit connected to this processor pin. If a future 0.13 micron Socket 370 processor is present in the socket, the TUAL5 reference schematic signal will be pulled to the 5 V rail and the TUAL5# reference schematic signal will be pulled to ground. Otherwise, for a Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh), the TUAL5 reference schematic signal will be pulled to ground and the TUAL5# will be pulled to the 5 V rail.

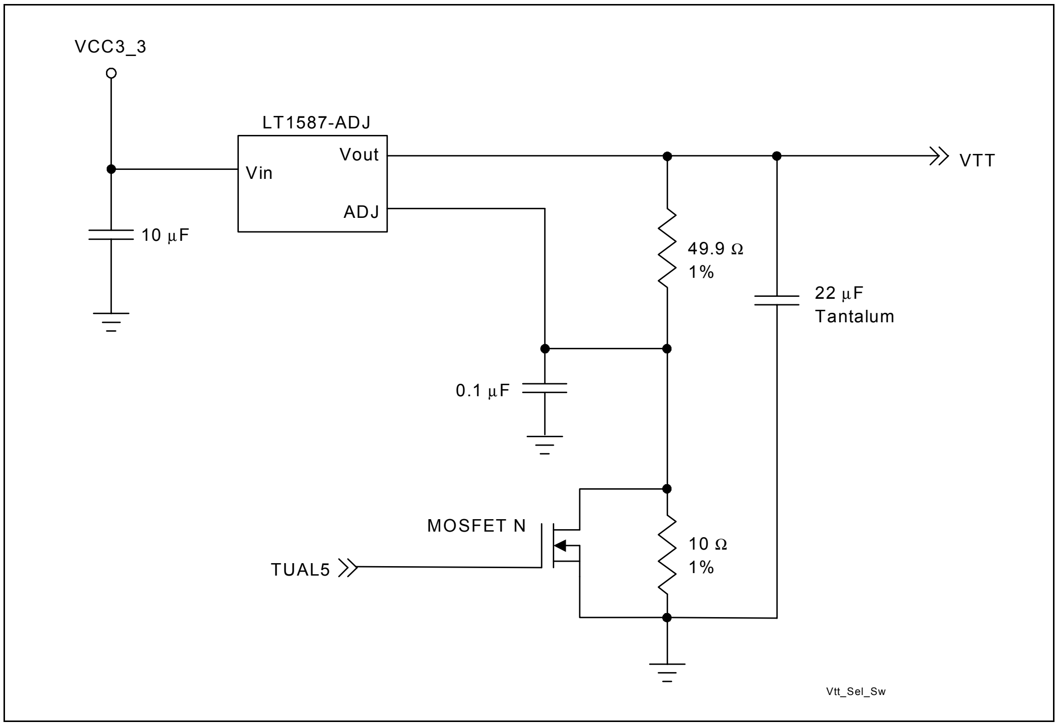
Figure 8. Processor Detect Mechanism at Socket/TUAL5 Generation Circuit



4.2.3 Setting the Appropriate Processor VTT Level

Because the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors require different VTT levels, the platform must be able to provide the appropriate voltage level after determining which processor is in the socket. Referring to Figure 9, the TUAL5 reference schematic signal serves to control the FET, and by doing so determines whether the voltage regulator supplies 1.25 V or 1.5 V to VTT for AGTL or AGTL+, respectively.

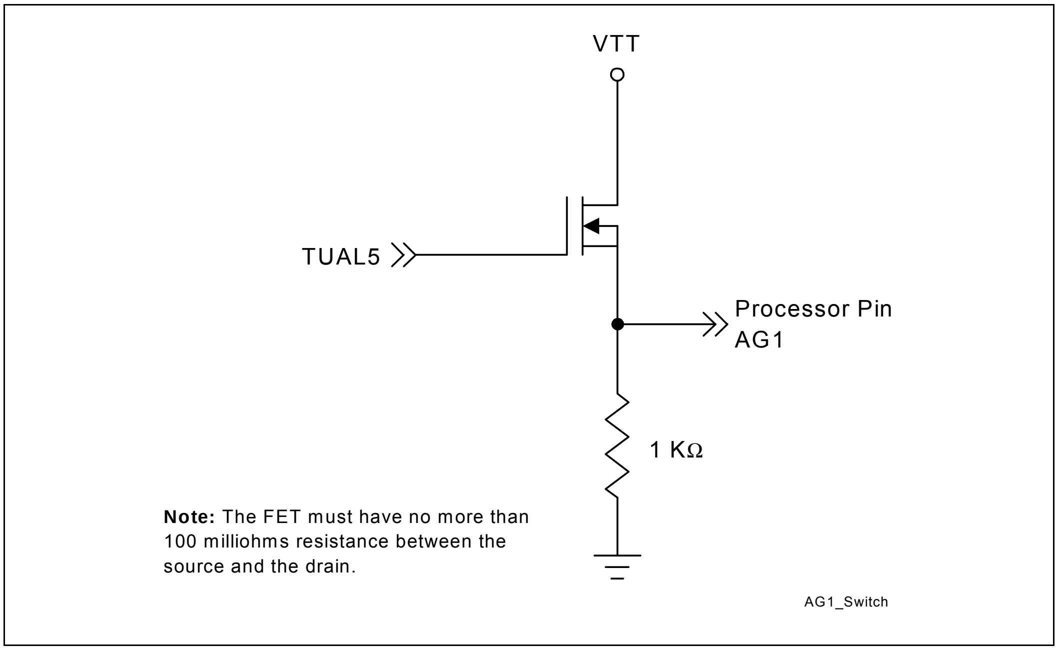
Figure 9. VTT Selection Switch



4.2.4 VTT Processor Pin AG1

Processor pin AG1 requires additional attention since it is a ground pin on a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) and a VTT pin on a future 0.13 micron socket 370 processor. A separate switch controlled by the TUAL5 reference schematic signal determines whether pin AG1 is pulled to ground or VTT. Refer to Figure 10 for an example implementation.

Figure 10. Switching Pin AG1



Note: The FET must have no more than 100 milliohms resistance between the source and the drain.

4.2.5 Identifying the Processor at the GMCH

The GMCH determines whether the socket contains a future 0.13 micron socket 370 processor or Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) based on the input to pin SMAA12 on the GMCH. In a system using future 0.13 micron socket 370 processors, SMAA12 will be pulled down during reset to indicate to the GMCH that a future 0.13 micron socket 370 processor is in the socket. Refer to Figure 11. for an example implementation.

Figure 11. Processor Identification Strap on GMCH

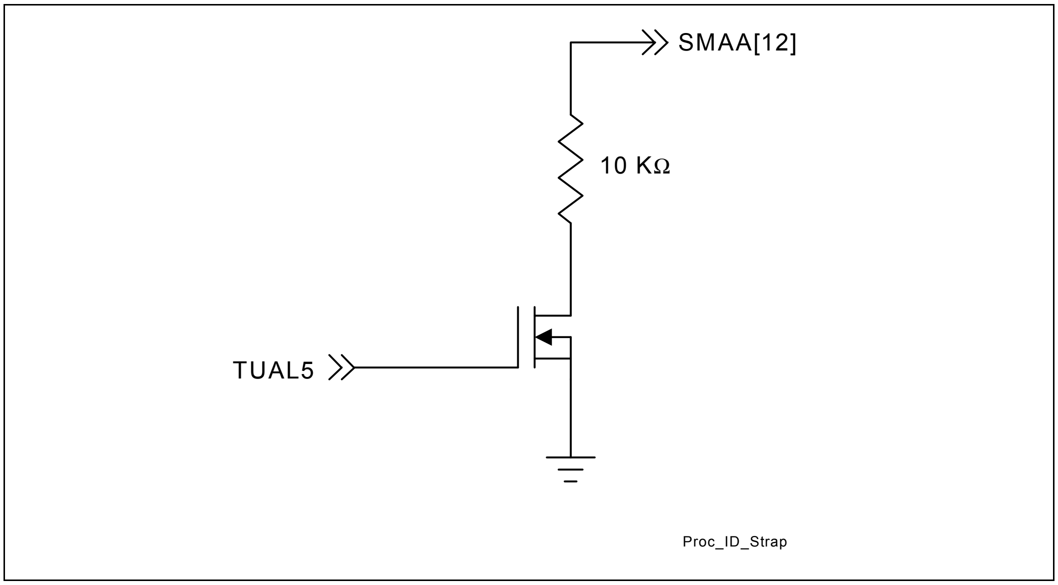


Table 6 provides the logic decoding to determine which processor is installed in a PGA370 design.

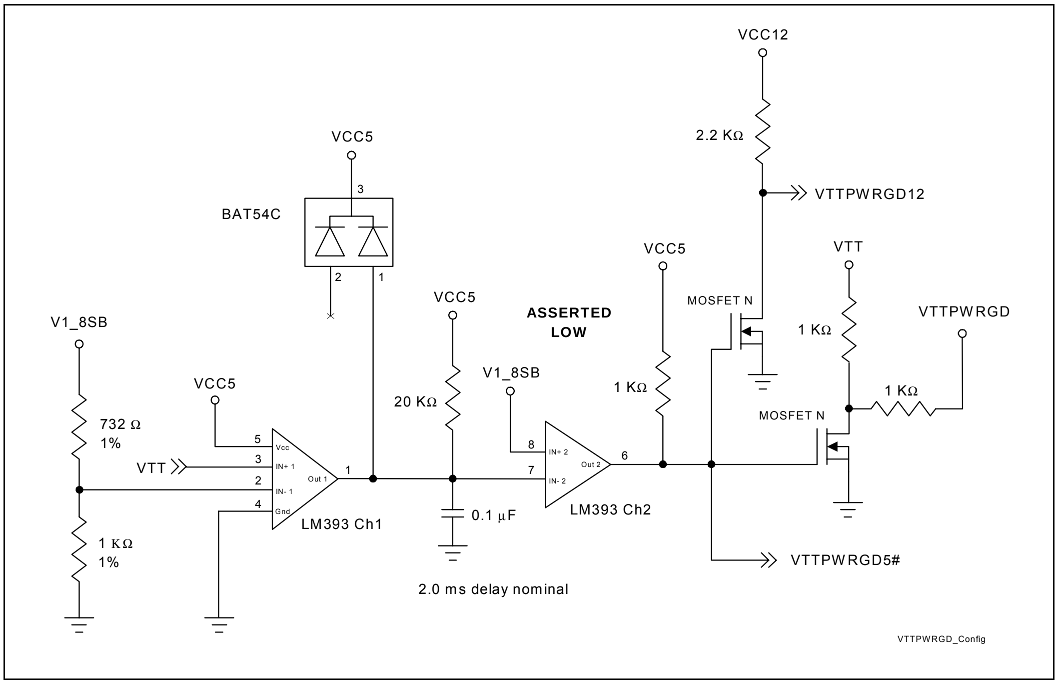
Table 6. Determining the Installed Processor via Hardware Mechanisms

Processor Pin AF36	CPUPRES#	Notes
Hi-Z	0	Future 0.13 micron socket 370 processor installed.
Low	0	Intel® Pentium® III processor (CPUID=068xh) or Intel® Celeron™ processor (CPUID=068xh) installed.
X	1	No processor installed.

4.2.6 Configuring Non-VTT Processor Pins

When asserted, the VTTPWGRD signal must be level-shifted to 12 V to properly drive the gating circuitry of the CK-815. Furthermore, while the VTTPWRGD signal is connected to the VTTPWRGD pin on a future 0.13 micron socket 370 processor, on a Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh) that same pin is a ground. To provide proper functionality, a 1.0 kΩ resistor must be placed in series between the circuitry that generates the signal VTTPWRGD and the processor pin VTTPWRGD. Refer to Figure 12 for an example implementation. Voltage regulators that generate the standard VTTPWRGD signal are available.

Figure 12. VTTPWRGD Configuration Circuit

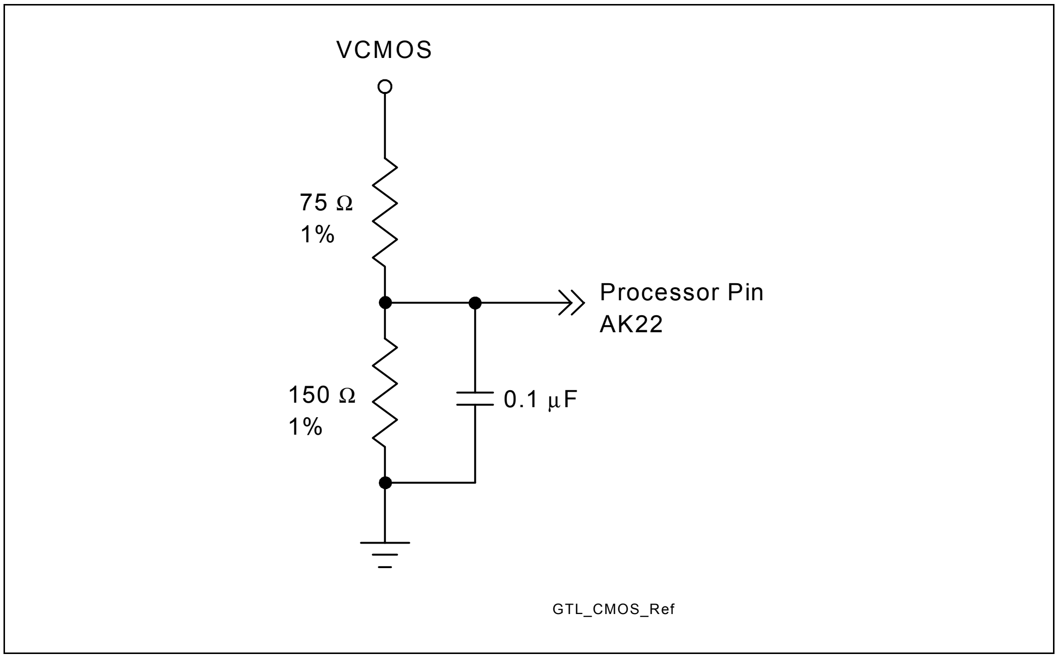


NOTE: The diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20 ms delay.

4.2.7 VCMOS Reference

In previous platforms supporting the Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh), VCMOS was generated by the processor itself. The future 0.13 micron socket 370 processors do not generate VCMOS, and the universal platform is required to generate this separately on the motherboard. Processor pin AK22, which is a GTL_REF pin on a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh), has been changed to a VCMOS_REF pin on future 0.13 micron socket 370 processors. Referring to Figure 13, a network of resistors and a capacitor must be added so that this pin operates appropriately for whichever processor is in the socket.

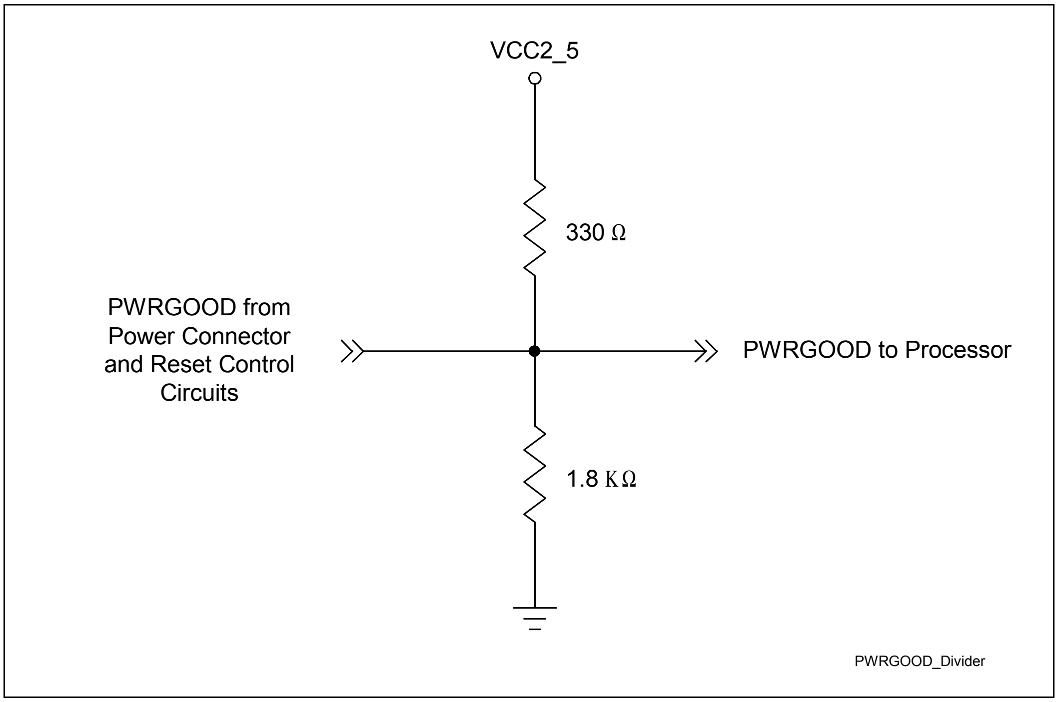
Figure 13. GTL_REF/VCMOS_REF Voltage Divider Network



4.2.8 Processor Signal PWRGOOD

The processor signal PWRGOOD is specified at different voltage levels depending on whether it is a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), or whether it is a future 0.13 micron socket 370 processor. As there is an overlap between the ranges of accepted voltage levels for these two processor groups, a resistor divider network that provides 2.1V will satisfy the requirements of all supported processors. See Figure 14 for an example implementation.

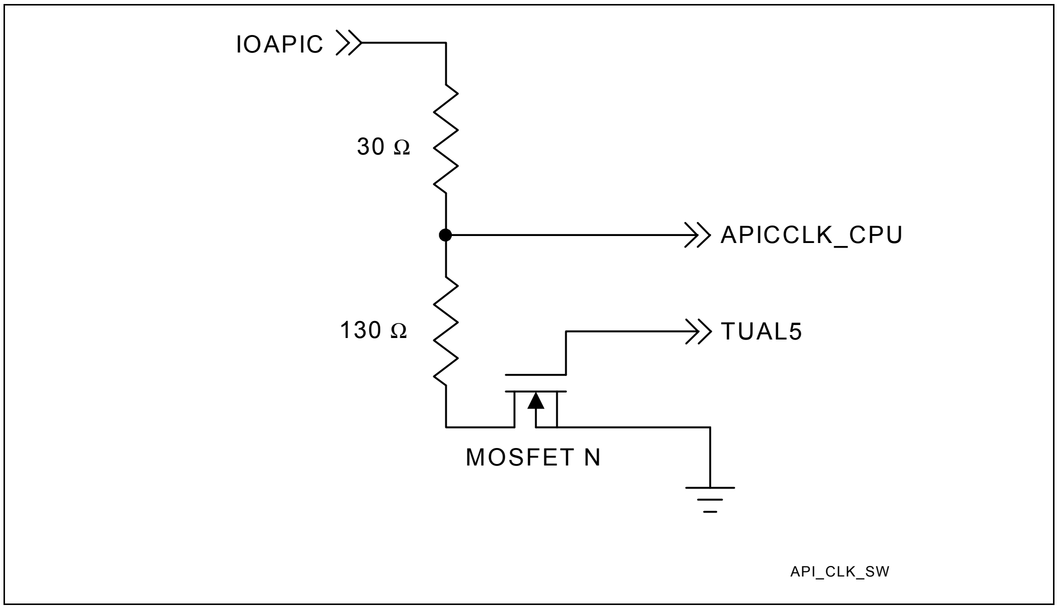
Figure 14. Resistor Divider Network for Processor PWRGOOD



4.2.9 APIC Clock Voltage Switching Requirements

The processor’s APIC clock is also specified at different voltage levels depending on whether it is for the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) or whether it is for a future 0.13 micron socket 370 processor. There is no overlap in the range of accepted voltage levels for the two processor groups, so a voltage switch is required to ensure proper operation. Figure 15 shows an example implementation.

Figure 15. Voltage Switch For APIC Clock from Clock Synthesizer to Processor



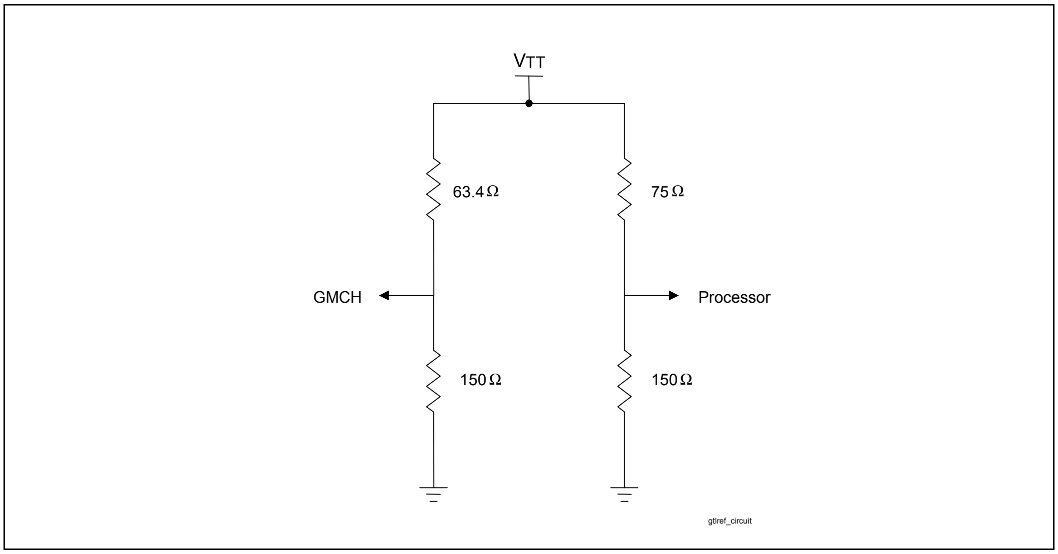
NOTE: The 30 Ω resistor represents the series resistor typically used in connecting the APIC clock to the processor.

4.2.10 GTLREF Topology and Layout

In a platform supporting the future 0.13 micron socket 370 processors, the voltage requirements for GTLREF are different for the processor and the chipset. The GTLREF on the processor is specified to be 2/3 * VTT, while the GTLREF on the chipset is 0.7 * VTT. This difference requires that separate resistor sites be added to the layout to split the GTLREF sources. In a universal motherboard design, a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) will be unaffected by the difference in GTLREF. The recommended GTLREF circuit topology is shown in Figure 16.

Note: If an A-2 stepping of the GMCH is used with the universal motherboard design, the GTLREF for the GMCH should be set at 2/3 * VTT. This requires changing the 63.4 Ω, 1% resistor on the GMCH side to 75 Ω, 1%.

Figure 16. GTLREF Circuit Topology



GTLREF Layout and Routing Guidelines

- Place all resistor sites for GTLREF generation close to the GMCH.
- Route GTLREF with as wide a trace as possible.
- Use one 0.1 µF decoupling capacitor for every two GTLREF pins at the processor (four capacitors total). Place as close as possible (within 500 mils) to the Socket 370 GTLREF pins.
- Use one 0.1 µF decoupling capacitor for each of the two GTLREF pins at the GMCH (two capacitors total). Place as close as possible to the GMCH GTLREF balls.

Given the higher GTLREF level for the GMCH, a debug test hook should be added for validation purposes. The debug test hook should be placed on the processor signal ADS# and consists of laying down the site for a 56 Ω pull-up to VTT. The resistor site should be located within 150 mils of the GMCH, and placed as close to the ADS# signal trace as possible.

4.3 Power Sequencing on Wake Events

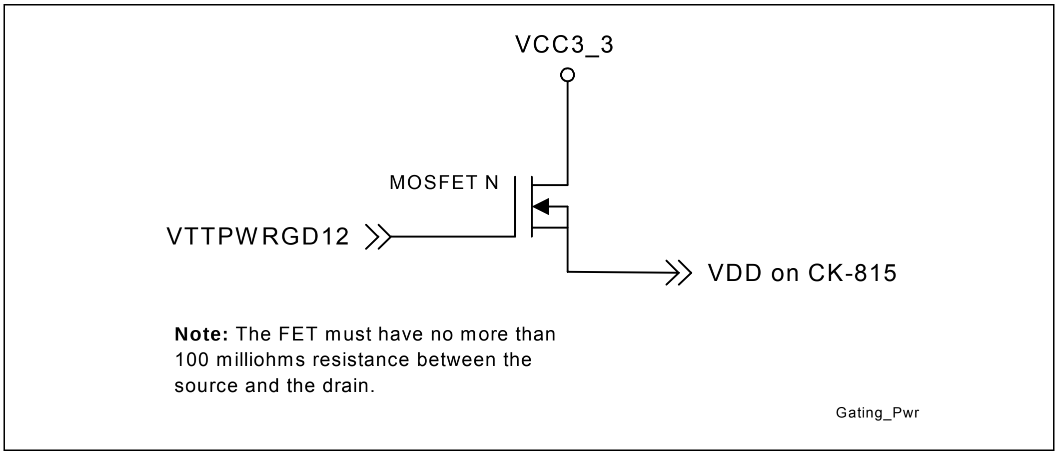
In addition to the mechanism for identifying the processor in the socket, special handling of wake events is required for the 815G chipset platform that support functionality of the future 0.13 micron socket 370 processors. When a wake event is triggered, the GMCH and the CK-815 must not sample BSEL[1:0] until the signal VTTPWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the CK-815-compliant clock driver until VTTPWRGD12 is asserted.
2. Clocks to the ICH stabilize before the power supply asserts PWROK to the ICH. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus, it is necessary to gate PWROK to the ICH from the power supply while the CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.
3. ICH takes the GMCH out of reset.
4. GMCH samples BSEL[1:0]. CK-815 will have sampled BSEL[1:0] much earlier.

4.3.1 Gating of Intel® CK-815 to VTTPWRGD

System designers must ensure that the VTTPWRGD signal is asserted before the CK-815-compliant clock driver receives power. This is handled by having the 3.3 V rail of the clock driver gated by the VTTPWRGD12 reference schematic signal. Unlike previous 815G chipset designs, the 3.3 V standby rail is not used to power the clock as the VTTPWRGD12 reference schematic signal will cut power to the clock when going into any sleep state. Refer to Figure 17 for an example implementation.

Figure 17. Gating Power to Intel® CK-815

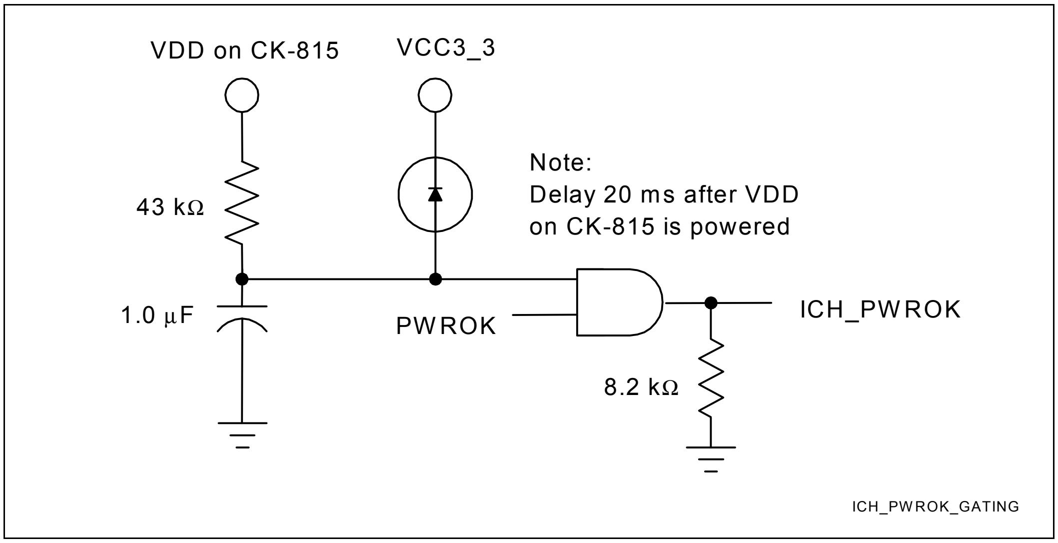


Note: The FET must have no more than 100 milliohms resistance between the source and the drain.

4.3.2 Gating of PWROK to Intel® ICH

With power being gated to the CK-815 by the signal VTTPWRGD12, it is important that the clocks to the ICH are stable before the power supply asserts PWROK to the ICH. As the clocking power gating circuitry relies on the 12 V supply, there is no guarantee that these conditions will be met. This is why an estimated minimum time delay of 20 ms must be added after power is connected to the CK-815 to give the clock driver sufficient time to stabilize. This time delay will gate the power supply's assertion of PWROK to the ICH. After the time delay, the power supply can safely assert PWROK to the ICH, with the ICH subsequently taking the GMCH out of reset. Refer to Figure 18 for an example implementation.

Figure 18. PWROK Gating Circuit for Intel® ICH



NOTE: The diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20 ms delay.

5 System Bus Design Guidelines

The Pentium III processor delivers higher performance by integrating the Level-2 cache into the processor and running it at the processor's core speed. The Pentium III processor runs at higher core and system bus speeds than previous-generation Intel® IA-32 processors while maintaining hardware and software compatibility with earlier Pentium III processors. The new Flip Chip-Pin Grid Array 2 (FC-PGA2) package technology enables compatibility with previous Flip Chip-Pin Grid Array (FC-PGA) packages using the PGA370 socket.

This section presents the considerations for designs capable of using the 815G chipset platform with the full range of Pentium III processors using the PGA370 socket.

5.1 System Bus Routing Guidelines

The following layout guide supports designs using Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors with the 815G chipset platform for use with the universal socket 370. The solution covers system bus speeds of 66/100/133 MHz for the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors. All processors must also be configured to 56 Ω on-die termination.

5.1.1 Initial Timing Analysis

Table 7 lists the AGTL/AGTL+ component timings of the processors and GMCH defined at the pins.

Note: **These timings are for reference only.** Obtain each processor's specifications from the respective processor datasheet and the chipset values from the appropriate 815 chipset ETS.

Table 7. Intel® Pentium® III Processor AGTL/AGTL+ Parameters for Example Calculations

IC Parameters	Intel® Pentium® III Processor at 133 MHz System Bus	GMCH	Notes
Clock to Output maximum (T_{CO_MAX})	• 3.25 ns (for 66/100/133 MHz system bus speeds)	4.1 ns	1, 2
Clock to Output minimum (T_{CO_MIN})	• 0.40 ns (for 66/100/133 MHz system bus)	1.05 ns	1, 2
Setup time (T_{SU_MIN})	• 1.20 ns (for BREQ Lines) • 0.95 ns (for all other AGTL/AGTL+ Lines @ 133 MHz) • 1.20 ns (for all other AGTL/AGTL+ Lines @ 66/100 MHz)	2.65 ns	1, 2,3
Hold time (T_{HOLD})	• 1.0 ns (for 66/100/133 MHz system bus speeds)	0.10 ns	1

NOTES:

1. All times in nanoseconds.
2. **Numbers in table are for reference only**. These timing parameters are subject to change. Check the appropriate component datasheet for the valid timing parameter values.
3. T_{SU_MIN} = 2.65 ns assumes that the GMCH sees a minimum edge rate equal to 0.3 V/ns.

Table 8 contains an example AGTL+ initial maximum flight time, and Table 9 contains an example minimum flight time calculation for a 133 MHz, uniprocessor system using the Pentium III processor and the 815G chipset platform's system bus. Note that assumed values were used for the clock skew and clock jitter.

Note: The clock skew and clock jitter values depend on the clock components and the distribution method chosen for a particular design and must be budgeted into the initial timing equations, as appropriate for each design.

Table 8and Table 9 were derived assuming the following:

- CLK_{SKEW} = 0.20 ns (Note: This assumes that the clock driver pin-to-pin skew is reduced to 50 ps by tying the two host clock outputs together (i.e., "ganging") at the clock driver output pins, and that the PCB clock routing skew is 150 ps. The system timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together as well as the use of a clock driver that meets the CK-815 Clock Synthesizer/Driver Specification.)
- CLK_{JITTER} = 0.250 ns

See the respective processor's datasheet, the appropriate 815G chipset platform documentation, and the *Intel® CK-815 Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Exact details regarding the host clock routing topology are provided with the platform design guideline.

Table 8. Example T_{FLT_MAX} Calculations for 133 MHz Bus [1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}
Processor	GMCH	7.50	3.25	2.65	0.20	0.25	0.40	1.1
GMCH	Processor	7.50	4.1	1.20	0.20	0.25	0.40	1.35

NOTES:

1. All times in nanoseconds
2. BCLK period = 7.50 ns at 133.33 MHz

Table 9. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor	GMCH	0.10	0.20	0.40	0.10
GMCH	Processor	1.00	0.20	1.05	0.15

NOTES: All times in nanoseconds

The flight times in Table 8 include margin to account for the following phenomena that Intel observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect the flight time and signal quality and sometimes are not accounted for during simulation. Accordingly, the maximum flight times depend on the baseboard design, and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in
- Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay
- Crosstalk on the PCB and inside the package which can cause variation in the signals

Additional effects exist that **may not necessarily** be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. These effects are included as M_{ADJ} in the example calculations in Table 8. Examples include:

- The effective board propagation constant (S_{EFF}), which is a function of:
  - — Dielectric constant (ε_r) of the PCB material
  - — Type of trace connecting the components (stripline or microstrip)
  - — Length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time, **but not necessarily equal to** the flight time.

5.2 General Topology and Layout Guidelines

Figure 19. Topology for 370-Pin Socket Designs with Single-Ended Termination (SET)

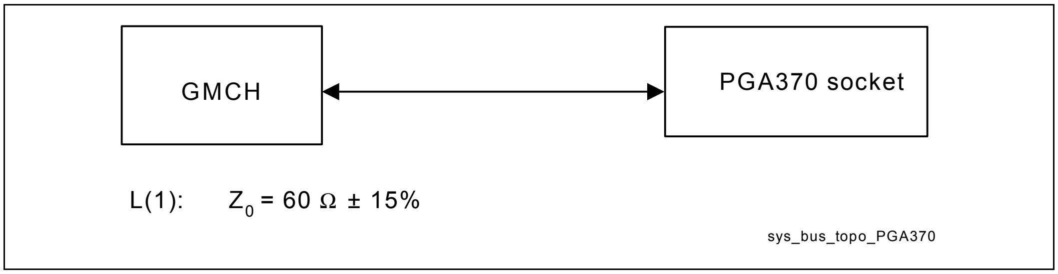


Table 10. Trace Guidelines for Figure 19 [1, 2, 3]

Description	Min. Length (inches)	Max. Length (inches)
GMCH to PGA370 socket trace	1.90	4.50

NOTES:

1. All AGTL/AGTL+ bus signals should be referenced to the ground plane for the entire route.
2. Use an intragroup AGTL/AGTL+ spacing : line width : dielectric thickness ratio of at least 2:1:1 for microstrip geometry. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10-mil spacing, 5-mil traces, and a 5-mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
3. The recommended trace width is 5 mils, but not greater than 6 mils.

Table 11 contains the trace width space ratios assumed for this topology. Three types of crosstalk are considered in this guideline: Intragroup AGTL/AGTL+, Intergroup AGTL/AGTL+, and AGTL/AGTL+ to non-AGTL/AGTL+. Intragroup AGTL/AGTL+ crosstalk involves interference between AGTL/AGTL+ signals within the same group. Intergroup AGTL/AGTL+ crosstalk involves interference from AGTL/AGTL+ signals in a particular group to AGTL/AGTL+ signals in a different group. An example of AGTL/AGTL+ to non-AGTL/AGTL+ crosstalk is when CMOS and AGTL/AGTL+ signals interfere with each other. The AGTL/AGTL+ signals consist of the following groups: data signals, control signals, clock signals, and address signals.

Table 11. Trace Width:Space Guidelines

Crosstalk Type	Trace Width:Space Ratios[1, 2]
Intragroup AGTL/AGTL+ signals (same group AGTL/AGTL+)	5:10 or 6:12
Intergroup AGTL/AGTL+ signals (different group AGTL/AGTL+)	5:15 or 6:18
AGTL/AGTL+ to System Memory Signals	5:30 or 6:36
AGTL/AGTL+ to non-AGTL/AGTL+	5:25 or 6:24

NOTES:

1. Edge-to-edge spacing.
2. Units are in mils.

5.2.1 Motherboard Layout Rules for AGTL/AGTL+ Signals

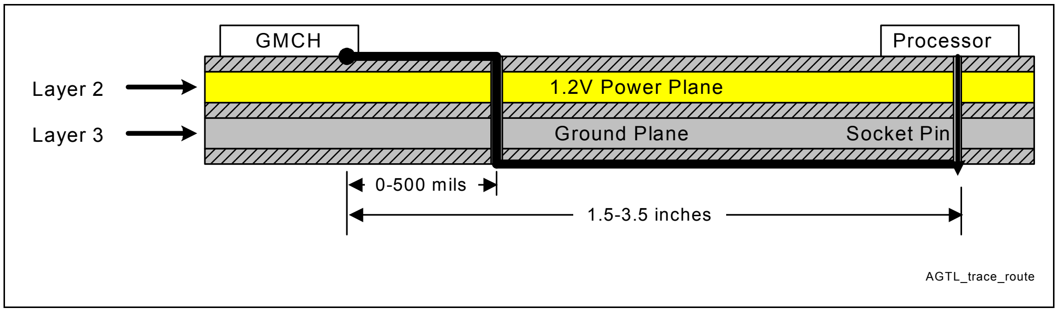
5.2.1.1 Ground Reference

It is strongly recommended that AGTL/AGTL+ signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide an effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane. If a signal has to go through routing layers, the recommendations are in the following list.

Note: Following these layout rules is critical for AGTL/AGTL+ signal integrity, particularly for 0.18-micron and smaller process technology.

- For signals going from a ground reference to a power reference, add capacitors between ground and power near the vias to provide an AC return path. One capacitor should be used for every three signal lines that change reference layers. Capacitor requirements are as follows: C=100 nF, ESR=80 mΩ, ESL=0.6 nH. Refer to Figure 20 for an example of switching reference layers.
- For signals going from one ground reference to another, separate ground reference, add vias between the two ground planes to provide a better return path.

Figure 20. AGTL/AGTL+ Trace Routing



5.2.1.2 Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance.

5.2.1.3 Processor Connector Breakout

It is strongly recommended that AGTL/AGTL+ signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the connector on the same layer. If routing is tight, break out from the connector on the opposite routing layer over a ground reference and cross over to main signal layer near the processor connector.

5.2.1.4 Minimizing Crosstalk

The following general rules minimize the impact of crosstalk in a high-speed AGTL/AGTL+ bus design:

- Maximize the space between traces. Where possible, maintain a minimum of 10 mils (assuming a 5-mil trace) between trace edges. It may be necessary to use tighter spacing when routing between component pins. When traces must be close and parallel to each other, minimize the distance that they are close together and maximize the distance between the sections when the spacing restrictions are relaxed.
- Avoid parallelism between signals on adjacent layers, if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL/AGTL+ is a low-signal-swing technology, it is important to isolate AGTL/AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings (e.g., 5 V PCI).
- AGTL/AGTL+ signals must be well isolated from system memory signals. AGTL/AGTL+ signal trace edges must be at least 30 mils from system memory trace edges within 100 mils of the ball of the GMCH.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL/AGTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes crosstalk.
- Route AGTL/AGTL+ address, data, and control signals in separate groups to minimize crosstalk between groups. Keep at least 15 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross-sectional area of the traces. This can be done by means of narrower traces and/or by using thinner copper, but the trade-off for this smaller cross-sectional area is higher trace resistivity, which can reduce the falling-edge noise margin because of the I*R loss along the trace.

5.2.2 Motherboard Layout Rules for Non-AGTL/AGTL+ (CMOS) Signals

Table 12. Routing Guidelines for Non-AGTL/Non-AGTL+ Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 9”
FERR#	5 mils	10 mils	1” to 9”
FLUSH#	5 mils	10 mils	1” to 9”
IERR#	5 mils	10 mils	1” to 9”
IGNNE#	5 mils	10 mils	1” to 9”
INIT#	5 mils	10 mils	1” to 9”

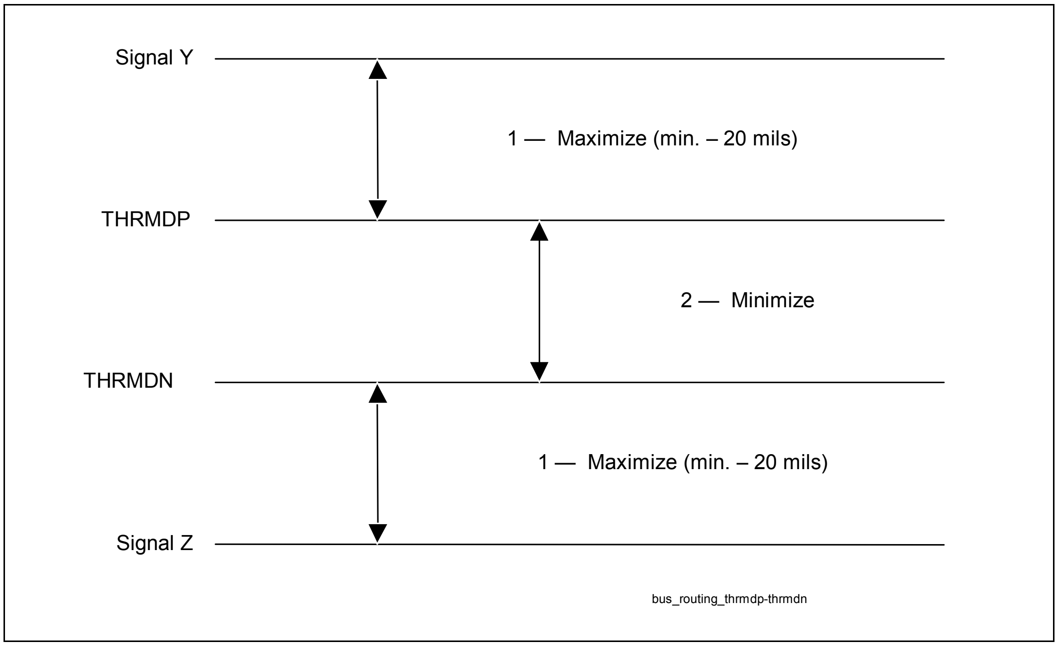
Signal	Trace Width	Spacing to Other Traces	Trace Length
LINT[0] (INTR)	5 mils	10 mils	1” to 9”
LINT[1] (NMI)	5 mils	10 mils	1” to 9”
PICD[1:0]	5 mils	10 mils	1” to 9”
PREQ#	5 mils	10 mils	1” to 9”
PWRGOOD	5 mils	10 mils	1” to 9”
SLP#	5 mils	10 mils	1” to 9”
SMI#	5 mils	10 mils	1” to 9”
STPCLK	5 mils	10 mils	1” to 9”
THERMTRIP#	5 mils	10 mils	1” to 9”

NOTE: Route these signals on any layer or combination of layers.

5.2.3 THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor’s thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance.

Figure 21. Routing for THRMDP and THRMDN



NOTES:

1. Route these traces parallel and equalize lengths within ±0.5 inch.
2. Route THRMDP and THRMDN on the same layer.

5.2.4 Additional Routing and Placement Considerations

- Distribute VTT with a wide trace. A 0.050 inch minimum trace is recommended to minimize DC losses. Route the VTT trace to all components on the host bus. Be sure to include decoupling capacitors.
- The VTT voltage should be 1.5 V ± 3% for static conditions, and 1.5 V ± 9% for worst-case transient conditions when the Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh) is present in the socket. If a future 0.13 micron socket 370 processor is being used, the VTT voltage should then be 1.25 V ± 3% for static conditions, and 1.25 V ± 9% for worst-case transient conditions.
- Place resistor divider pairs for VREF generation at the GMCH component. VREF also is delivered to the processor.

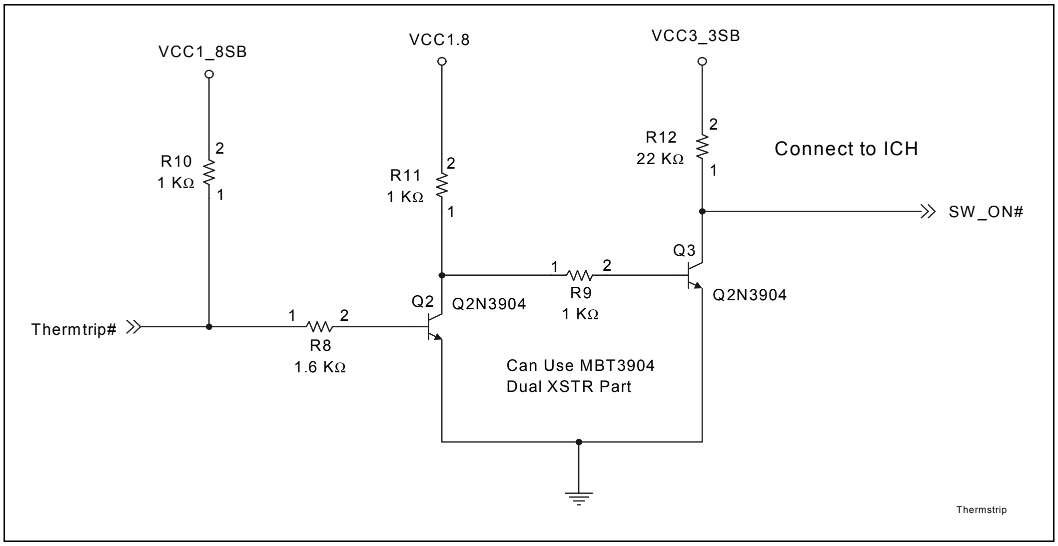
5.3 Electrical Differences for Universal PGA370 Designs

There are several electrical changes between previous PGA370 designs and the *universal PGA370* design, as follows:

- Changes to the PGA370 socket pin definitions.
- Addition of VTTPWRGD signal to ensure stable VID selection for future 0.13 micron socket 370 processors.
- Addition of THERMTRIP circuit to allow processor to detect catastrophic overheat.
- Addition of VID[25 mV] signal to support future 0.13 micron socket 370 processors.
- Processor VTT level is switchable to 1.25 V or 1.5 V, depending on which processor is present in the socket.
- In designs using future 0.13 micron socket 370 processors, the processor does not generate V_{CMOS}_REF.

5.3.1 THERMTRIP Circuit

Figure 22. Example Implementation of THERMTRIP Circuit



5.3.1.1 THERMTRIP Timing

When the THERMTRIP signal is asserted, both the VCC and VTT supplies to the processor must be turned off to prevent thermal runaway of the processor. The time required from THERMTRIP asserted to VCC rail at ½ nominal is 5 sec and THERMTRIP asserted to VTT rail at ½ nominal is 5 sec. System designers must ensure that the decoupling scheme used on these rails does not violate the THERMTRIP timing specifications.

5.3.1.2 THERMTRIP Support for 0.13 Micron Technology Processors, A-1 Stepping

A platform supporting the 0.13 micron technology processor must implement a workaround required for the A-1 stepping of that processor, identified by CPUID = 6B1h. The internal control register bit responsible for operation of the THERMTRIP circuit functionality may power up in an un-initialized state. As a result, THERMTRIP# may be incorrectly asserted during de-assertion of RESET# at nominal operating temperatures. When THERMTRIP# is asserted as a result of this, the processor may shut down internally and stop execution. In addition, when the THERMTRIP# pin is asserted the processor may incorrectly continue to execute, leading to intermittent system power-on boot failures. The occurrence and repeatability of failures is system dependent, however all systems and processors are susceptible to failure.

To prevent the risk of power-on boot failures, a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:

•Rising edge occurs after Vcc_core is valid and stable

•Rising edge occurs before or at the de-assertion of RESET#

•Rising edge occurs after all Vref input signals are at valid voltage levels

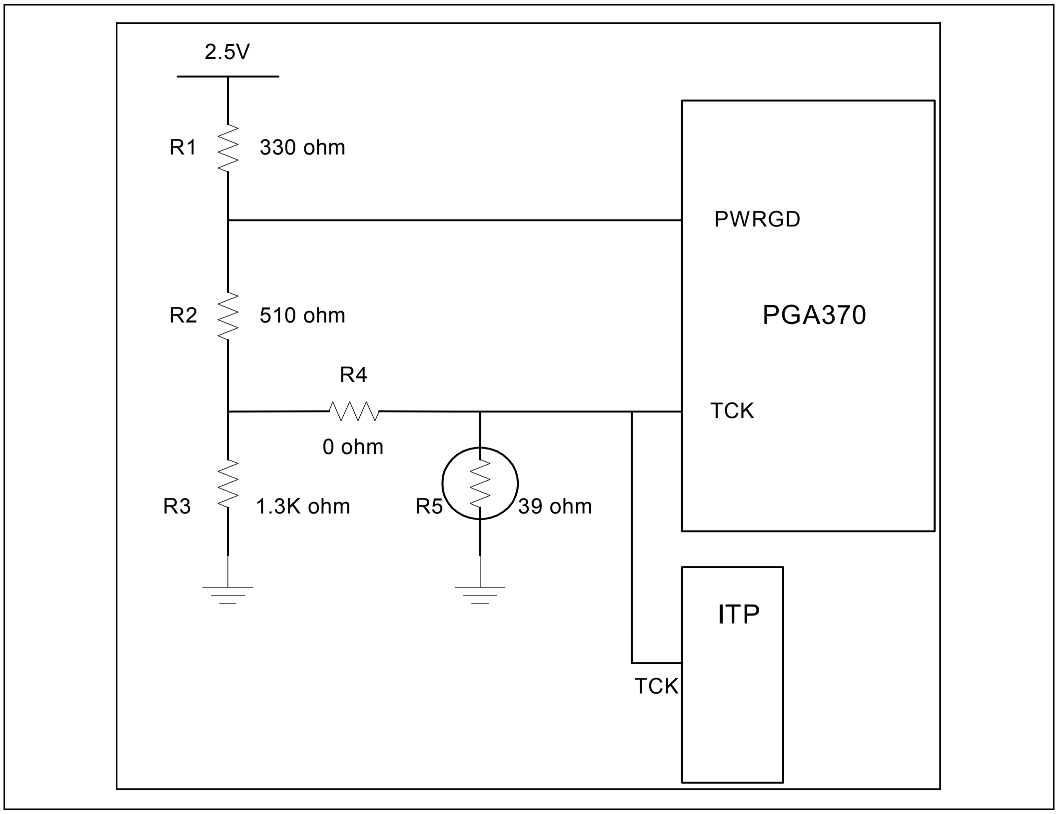
•TCK input meets the Vih min (1.3 V) and max (1.65 V) spec requirements

Specific workaround implementations may be platform specific. The following examples have been tested as acceptable workaround implementations.

Note: the example workaround circuits shown below require circuit modification for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Review the accompanying notes with each workaround for ITP modification details. If the system fails to boot when using ITP, issuing the ITP 'Reset Target' command on failing systems will reset the system and provide a sufficient rising edge on the TCK pin to ensure proper system boot.

In addition, the example workaround circuits shown below do not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround solutions must be found if such test capability is required.

Figure 23 THERMTRIP Support for A-1 Stepping 0.13 Micron Technology Processors



NOTES:

For Production Boards: Depopulate Resistor R5

To Use ITP: Install Resistor R5 and Depopulate Resistor R4

5.4 PGA370 Socket Definition Details

The following table compares the pin names and functions of the Intel processors supported in the 815G chipset platform for use with the universal socket 370.

Table 13. Processor Pin Definition Comparison

Pin #	Pin Name Intel® Celeron™ Processor (CPUID=068xh)	Pin Name Intel® Pentium® III Processor (CPUID=068xh)	Pin Name Future 0.13 Micron Socket 370 Processors	Function
AA33	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AA35	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AB36	VCC_{CMOS}	VCC_{CMOS}	VTT	• CMOS voltage level for Intel® Pentium® III processor (CPUID=068xh) and Intel® Celeron™ processor (CPUID=068xh). • AGTL termination voltage for future 0.13 micron socket 370 processors.
AD36	VCC1.5	VCC1.5	VTT	• VCC1.5 for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • VTT for future 0.13 micron socket 370 processors.
AF36	VSS	VSS	DETECT	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • Detect for future 0.13 micron socket 370 processors.
AG1[1]	VSS	VSS	VTT	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • VTT for future 0.13 micron socket 370 processors
AH4	Reserved	RESET#	RESET#	• Processor reset for the Pentium III processor (068xh) and Future 0.13 micron socket 370 processors
AH20	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage

Pin #	Pin Name Intel® Celeron™ Processor (CPUID=068xh)	Pin Name Intel® Pentium® III Processor (CPUID=068xh)	Pin Name Future 0.13 Micron Socket 370 Processors	Function
AJ3[1]	VSS	VSS	RESET2#	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • RESET2# for future 0.13 micron socket 370 processors
AK4	VSS	VSS	VTTPWRGD	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • VID control signal on future 0.13 micron socket 370 processors.
AK16	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AK22	GTL_REF	GTL_REF	VCMOS_REF	• GTL reference voltage for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • CMOS reference voltage for future 0.13 micron socket 370 processors
AK36	VSS	VSS	VID[25mV]	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • 25mV step VID select bit for future 0.13 micron socket 370 processors
AL13	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AL21	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN3	GND	GND	DYN_OE	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • Dynamic output enable for future 0.13 micron socket 370 processors
AN11	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN15	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN21	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
E23	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage

Pin #	Pin Name Intel® Celeron™ Processor (CPUID=068xh)	Pin Name Intel® Pentium® III Processor (CPUID=068xh)	Pin Name Future 0.13 Micron Socket 370 Processors	Function
G35	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage
G37	Reserved	Reserved	V_{TT}	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • AGTL termination voltage for future 0.13 micron socket 370 processors
N37[2]	NC	NC	NCHCTRL	• No connect for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • NCHCTRL for future 0.13 micron socket 370 processors
S33	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage
S37	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage
U35	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage
U37	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage
W3	Reserved	A34#	A34#	• Additional AGTL/AGTL+ address
X4[1]	RESET#	RESET2#	VSS	• Processor reset for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • Ground for future 0.13 micron socket 370 processors
X6	Reserved	A32#	A32#	• Additional AGTL/AGTL+ address
X34[2]	VCC_{CORE}	VCC_{CORE}	V_{TT}	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • AGTL termination voltage for future 0.13 micron socket 370 processors
Y1	Reserved	Reserved	RESERVED	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • Reserved for future 0.13 micron socket 370 processors
Y33	Reserved	CLKREF	CLKREF	• 1.25 V PLL reference

Pin #	Pin Name Intel® Celeron™ Processor (CPUID=068xh)	Pin Name Intel® Pentium® III Processor (CPUID=068xh)	Pin Name Future 0.13 Micron Socket 370 Processors	Function
Z36[2]	VCC2.5	VCC2.5	RESERVED	• VCC2.5 for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • Reserved for future 0.13 micron socket 370 processors

NOTES:

1. Refer to Chapter 4.
2. Refer to Section 13.2

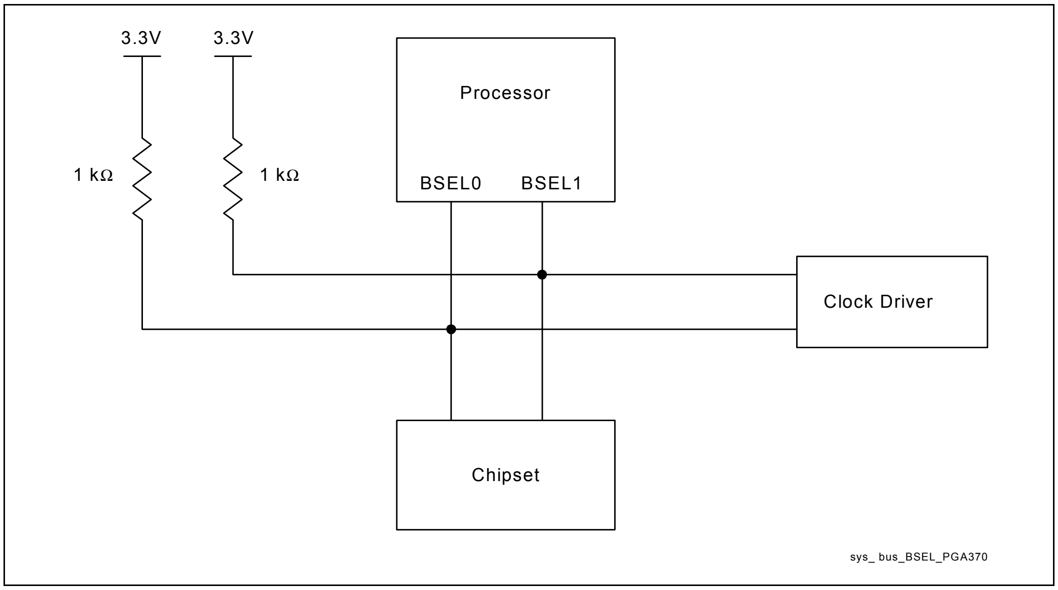
5.5 BSEL[1:0] Implementation Differences

A future 0.13 micron socket 370 processor will select the 133 MHz system bus frequency setting from the clock synthesizer. A Pentium III processor (CPUID=068xh) utilizes the BSEL1 pin to select either the 100 MHz or 133 MHz system bus frequency setting from the clock synthesizer. An Celeron processor (CPUID=068xh) will use both BSEL pins to select 66 MHz system bus frequency from the clock synthesizer. Processors in an FC-PGA or an FC-PGA2 are 3.3 V tolerant for these signals, as are the clock and chipset.

The CK-815 has been designed to support selections of 66 MHz, 100 MHz, and 133 MHz. The REF input pin has been redefined to be a frequency selection strap (BSEL1) during power-on and then becomes a 14 MHz reference clock output. The following figure details the new BSEL[1:0] circuit design for *universal PGA370* designs. Note that BSEL[1:0] now are pulled up using 1 kΩ resistors. Also refer to Figure 25 for more details.

Note: In a design supporting future 0.13 micron socket 370 processors, the BSEL[1:0] lines are not valid until VTTPWRGD is asserted. Refer to Section 4.2.10 for details.

Figure 24. BSEL[1:0] Circuit Implementation for PGA370 Designs



5.6 CLKREF Circuit Implementation

The CLKREF input (used by the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors) requires a 1.25 V source. It can be generated from a voltage divider on the VCC2.5 or VCC3.3 sources using 1% tolerant resistors. A 4.7 µF decoupling capacitor should be included on this input. See Figure 25 and Table 14 for example CLKREF circuits. **Do not use VTT as the source for this reference!**

Figure 25. Examples for CLKREF Divider Circuit

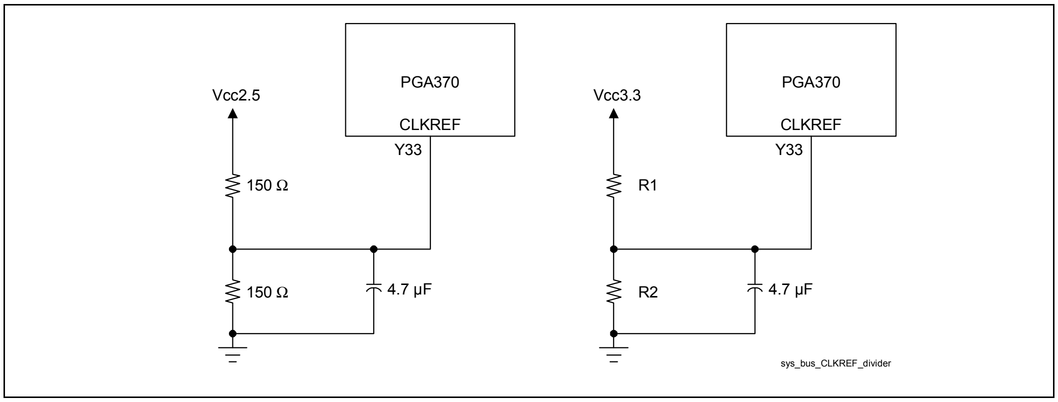


Table 14. Resistor Values for CLKREF Divider (3.3 V Source)

R1 (Ω), 1%	R2 (Ω), 1%	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

5.7 Undershoot/Overshoot Requirements

Undershoot and overshoot specifications become more critical as the process technology for microprocessors shrinks due to thinner gate oxide. Violating these undershoot and overshoot limits will degrade the life expectancy of the processor.

The Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors have more restrictive overshoot and undershoot requirements for system bus signals than previous processors. These requirements stipulate that a signal at the output of the driver buffer and at the input of the receiver buffer must not exceed the maximum absolute overshoot voltage limit or the minimum absolute undershoot voltage limit. Exceeding either of these limits will damage the processor. There is also a time-dependent, non-linear overshoot and undershoot requirement that depends on the amplitude and duration of the overshoot/undershoot. See the appropriate processor datasheet for more details on the processor overshoot/undershoot specifications.

5.8 Processor Reset Requirements

Universal PGA370 designs must route the AGTL/AGTL+ reset signal from the chipset to two pins on the processor as well as to the debug port connector. This reset signal is connected to the following pins at the PGA370 socket:

- **AH4 (RESET#).** The reset signal is connected to this pin for the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors
- **X4 (Reset2# or GND, depending on processor).** The X4 pin is RESET2# for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). X4 is GND for future 0.13 micron socket 370 processors. An additional 1kΩ resistor is connected in series with pin X4 to the reset circuitry since pin X4 is a ground pin in future 0.13 micron socket 370 processors.

Note: The AGTL/AGTL+ reset signal must always terminate to VTT on the motherboard.

Designs that do not support the debug port will not utilize the 240 Ω series resistor or the connection of RESET# to the debug port connector. RESET2# is not required for platforms that do not support the Celeron processor (CPUID=068xh). Pin X4 should then be connected to ground.

The routing rules for the AGTL/AGTL+ reset signal are shown in Figure 26.

Figure 26. RESET#/RESET2# Routing Guidelines

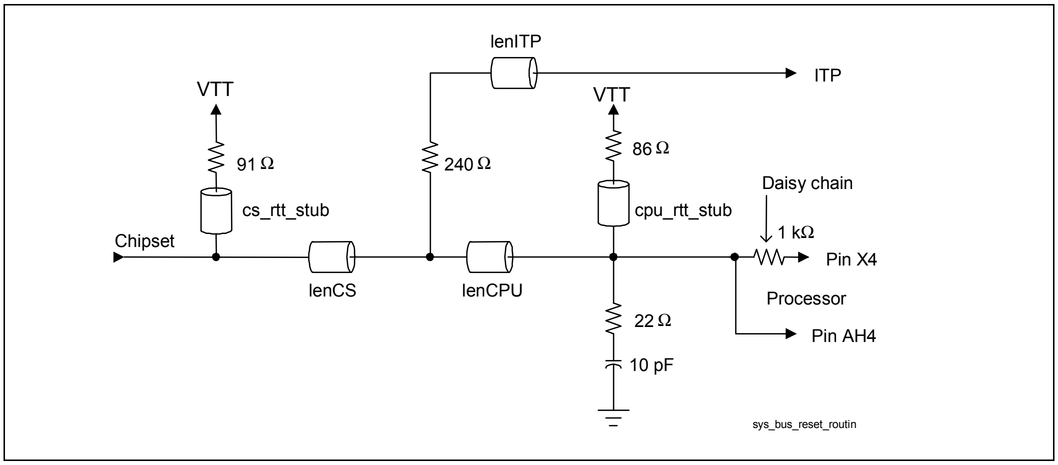


Table 15. RESET#/RESET2# Routing Guidelines (see Figure 26)

Parameter	Minimum (in)	Maximum (in)
LenCS	0.5	1.5
LenITP	1	3
LenCPU	0.5	1.5
cs_rtt_stub	0.5	1.5
cpu_rtt_stub	0.5	1.5

5.9 Processor PLL Filter Recommendations

Intel PGA370 processors have internal phase lock loop (PLL) clock generators that are analog and require quiet power supplies to minimize jitter.

5.9.1 Topology

The general desired topology for these PLLs is shown in Figure 28. Not shown are the parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

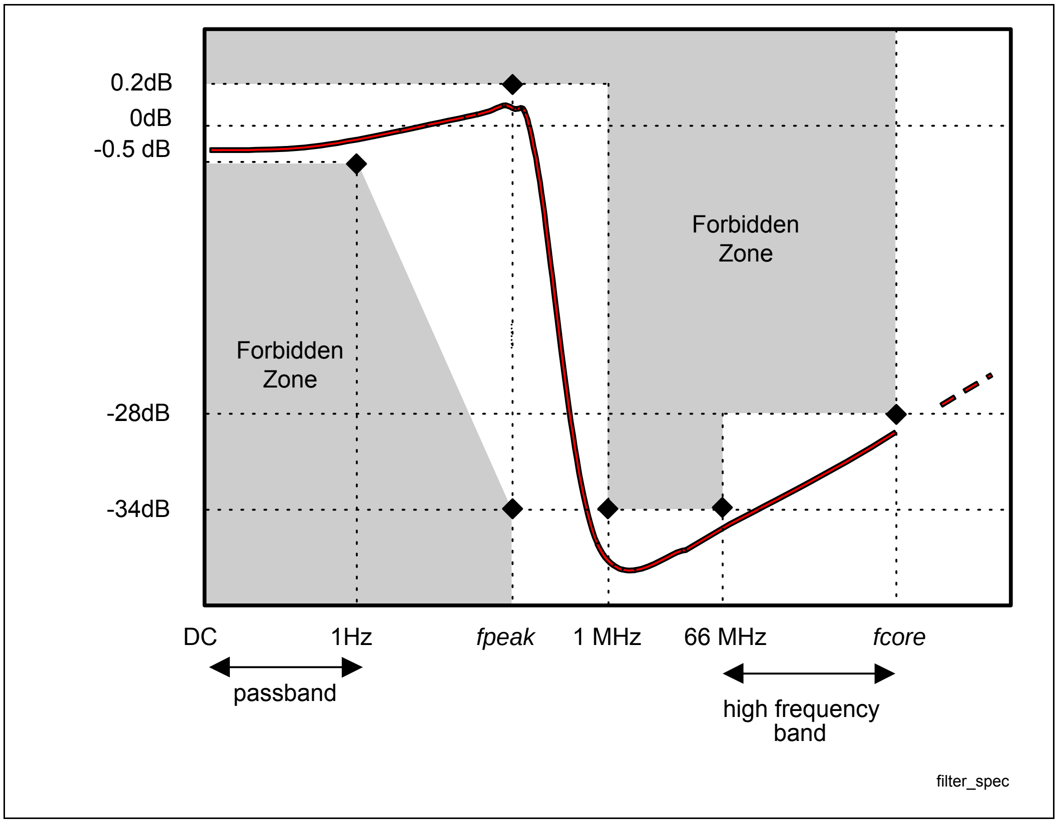
5.9.2 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 27.

Figure 27. Filter Specification



NOTES:

1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak* should be less than 0.05 MHz.

Other requirements:

- Use shielded-type inductor to minimize magnetic pickup.
- Filter should support DC current > 30 mA.
- DC voltage drop from VCC to PLL1 should be < 60 mV, which in practice implies series R < 2 Ω. This also means pass-band (from DC to 1 Hz) attenuation < 0.5 dB for VCC = 1.1V, and < 0.35 dB for VCC = 1.5 V.

5.9.3 Recommendation for Intel Platforms

The following tables contain examples of components that meet Intel's recommendations, when configured in the topology of Figure 28.

Table 16. Component Recommendations – Inductor

Part Number	Value	Tol.	SRF	Rated Current	DCR (Typical)
TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max.)
Murata LQG21N4R7K00T1	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (± 50%)
Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3 Ω max.

Table 17. Component Recommendations – Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%	2.5 nH	0.2 Ω

Table 18. Component Recommendation – Resistor

Value	Tolerance	Power	Note
1 Ω	10%	1/16 W	Resistor may be implemented with trace resistance, in which case a discrete R is not needed. See Figure 29.

To satisfy damping requirements, total series resistance in the filter (from VCC_{CORE} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component or routing or both. For example, if the chosen inductor has a minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1 (1 Ω ± 1%), the maximum DCR of the L (trace plus inductor) should be less than 2.0 - 1.1 = 0.9 Ω; this precludes the use of some inductors and sets a maximum trace length.

Other routing requirements:

- The capacitor (C) should be close to the PLL1 and PLL2 pins, < 0.1 Ω per route. These routes do not count towards the minimum damping R requirement.
- The PLL2 route should be parallel and next to the PLL1 route (i.e., minimize loop area).
- The inductor (L) should be close to C. Any routing resistance should be inserted between VCC_{CORE} and L.
- Any discrete resistor (R) should be inserted between VCC_{CORE} and L.

Figure 28. Example PLL Filter Using a Discrete Resistor

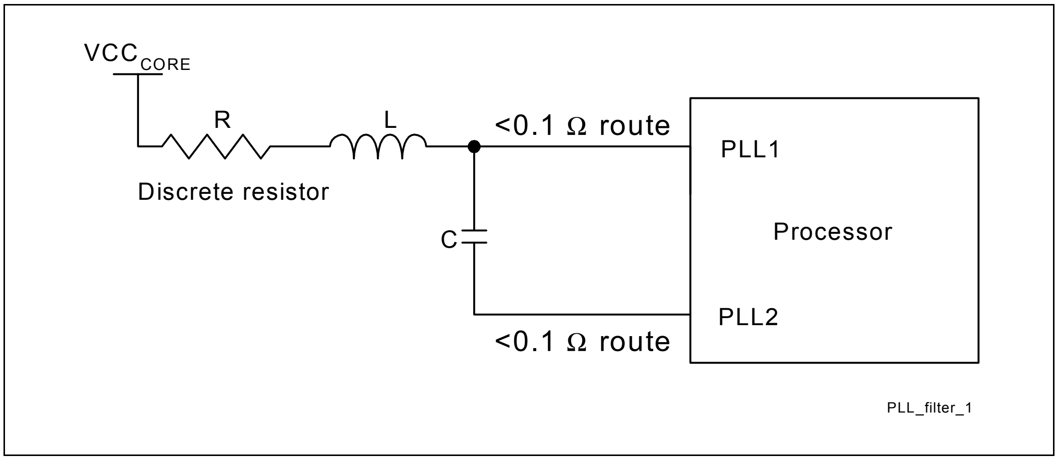
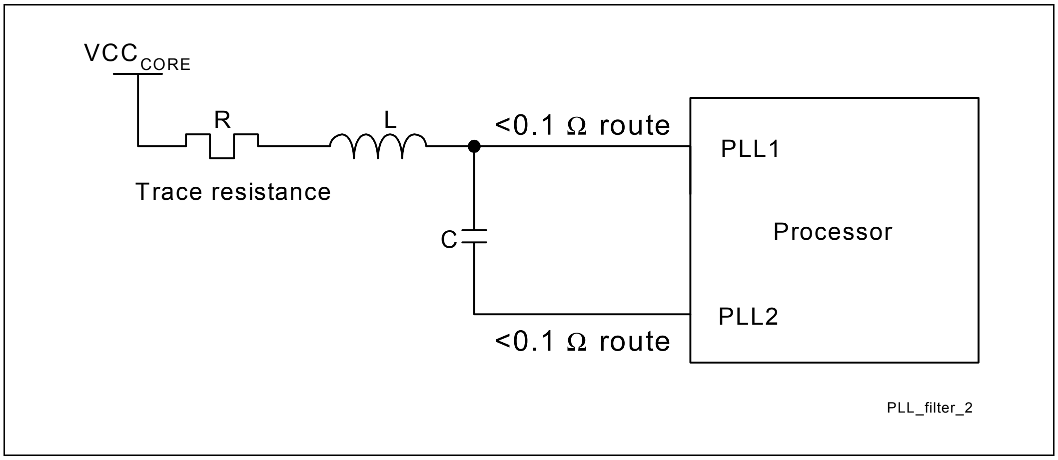


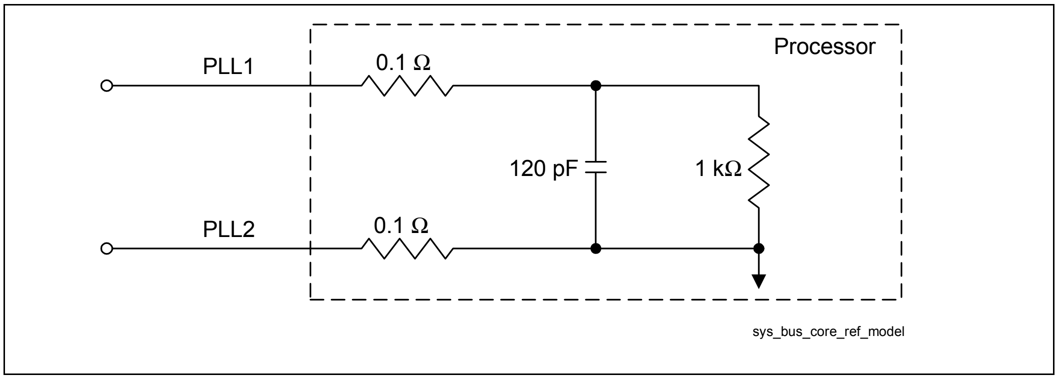
Figure 29. Example PLL Filter Using a Buried Resistor



5.9.4 Custom Solutions

As long as designers satisfy filter performance and requirements as specified and outlined in Section 5.9.2, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model (see Figure 30).

Figure 30. Core Reference Model



NOTES:

1. 0.1 Ω resistors represent package routing.
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1 kΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum VCC_{CORE} level.
7. For other modules (interposer, DMM, etc.), adjust routing resistor if desired, but use minimum numbers.

5.10 Voltage Regulation Guidelines

A *universal PGA370* design will need the voltage regulation module (VRM) or on-board voltage regulator (VR) to be compliant with Intel *VRM 8.5 DC-DC Converter Design Guidelines*.

5.11 Decoupling Guidelines for Universal PGA370 Designs

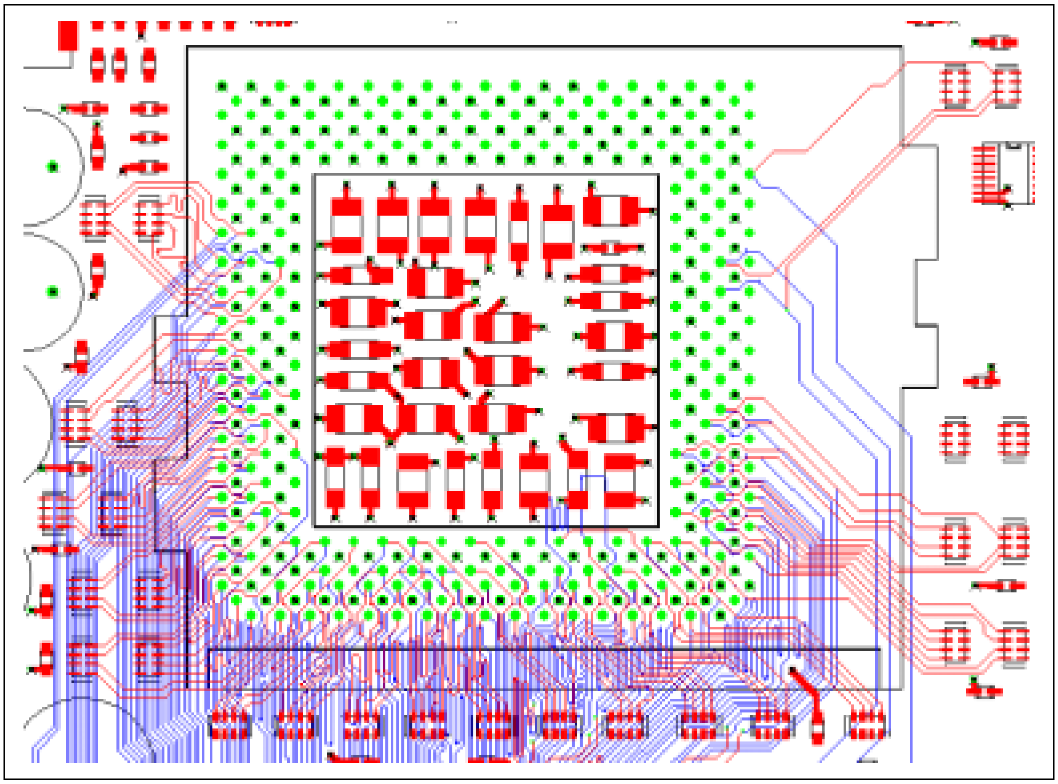
These preliminary decoupling guidelines for *universal PGA370* designs are estimated to meet the specifications of *VRM 8.5 DC-DC Converter Design Guidelines*.

5.11.1 VCC_{CORE} Decoupling Design

- Sixteen or more 4.7 µF capacitors in 1206 packages.

All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between the VCC_{CORE}/VSS power pins, as shown in Figure 31.

Figure 31. Capacitor Placement on the Motherboard



5.11.2 VTT Decoupling Design

For Itt = 2.3 A (maximum)

- Twenty 0.1 µF capacitors in 0603 packages placed as closed as possible to the processor VTT pins. The capacitors are shown on the exterior of the previous figure.

5.11.3 VREF Decoupling Design

- Four 0.1 µF capacitors in 0603 package placed near VREF pins (within 500 mils).

5.12 Thermal Considerations

5.12.1 Heatsink Volumetric Keep-Out Regions

Current heatsink recommendations are only valid for supported Celeron and Pentium III processor frequencies up to 1GHz.

Figure 32 shows the system component keep-out volume above the socket connector required for the reference design thermal solution for high frequency processors. This keep-out envelope provides adequate room for the heatsink, fan and attach hardware under static conditions as well as room for installation of these components on the socket. The heatsink must be compatible with the Integrated Heat Spreader (IHS) used by higher frequency Pentium III processors.

Figure 33 shows component keep-outs on the motherboard required to prevent interference with the reference design thermal solution. Note portions of the heatsink and attach hardware hang over the motherboard.

Adhering to these keep-out areas will ensure compatibility with Intel boxed processor products and Intel enabled third-party vendor thermal solutions for high frequency processors. While the keep-out requirements should provide adequate space for the reference design thermal solution, systems integrators should check with their vendors to ensure their specific thermal solutions fit within their specific system designs. Ensure that the thermal solutions under analysis comprehend the specific thermal design requirements for higher frequency Pentium III processors.

While thermal solutions for lower frequency processors may not require the full keep-out area, larger thermal solutions will be required for higher frequency processors, and failure to adhere to the guidelines will result in mechanical interference.

Figure 32. Heatsink Volumetric Keep-Out Regions

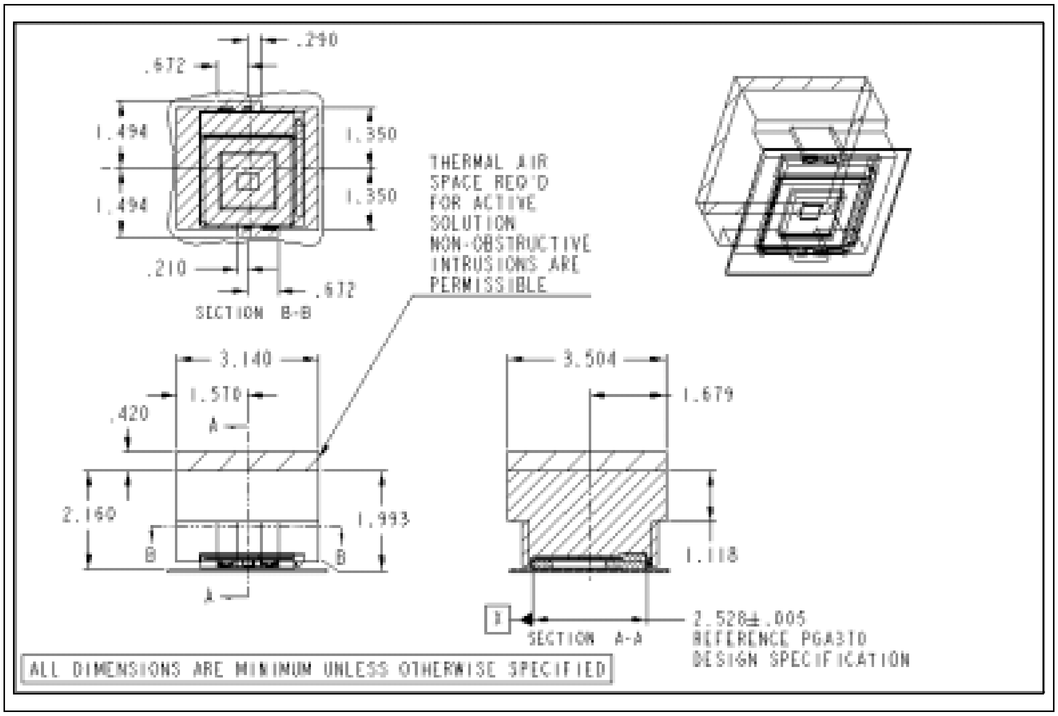
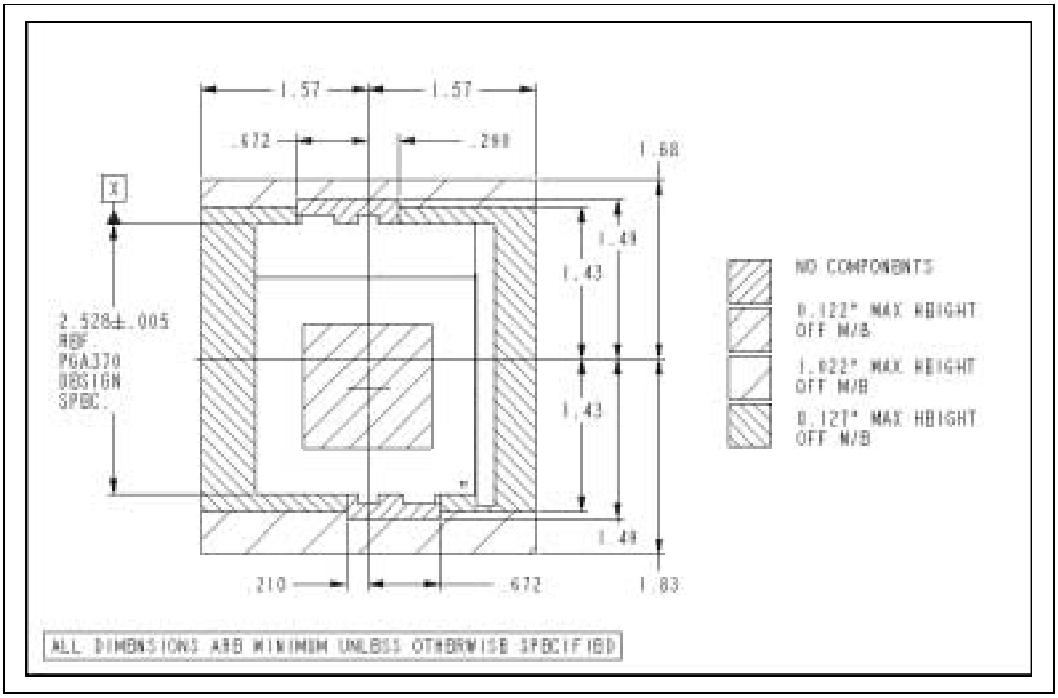


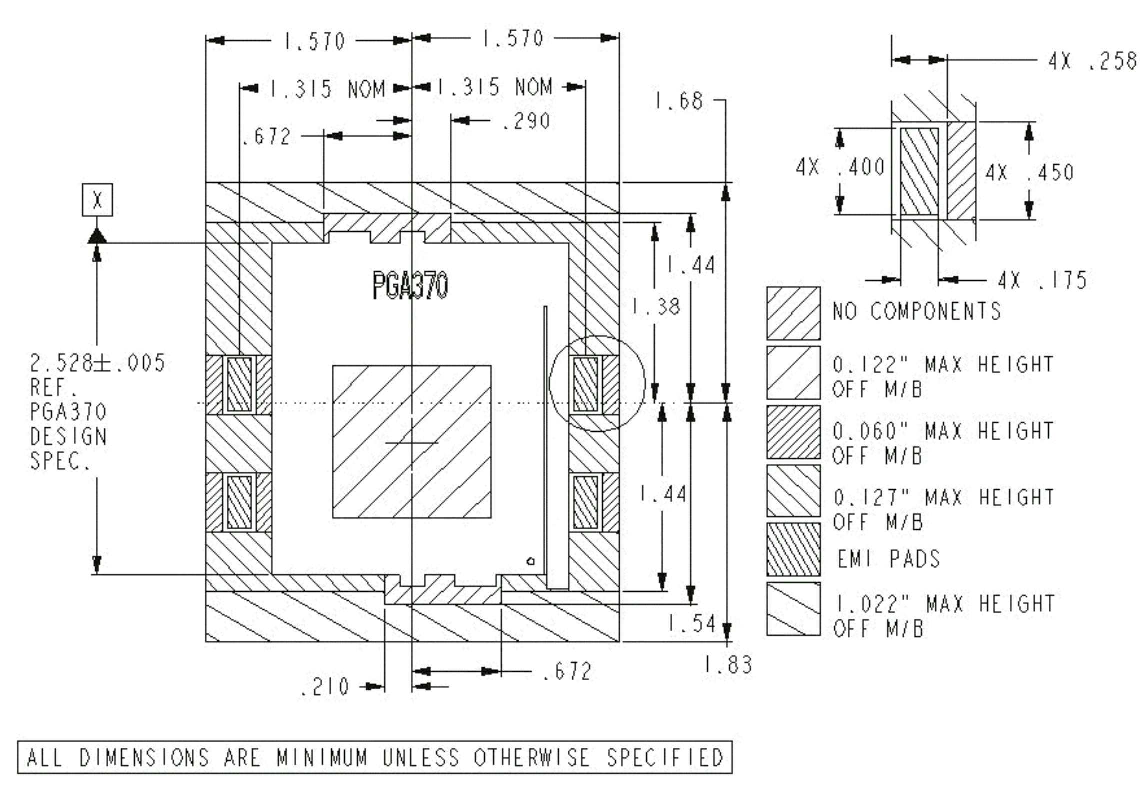
Figure 33. Motherboard Component Keep-Out Regions



5.12.2 Fan Heatsink Keep-Out Adherence for Future Boxed Intel® Celeron™ Processors

Mother board designs intended to support future boxed Celeron processors manufactured on the 0.13 micron process technology must meet fan heatsink keep-out requirements as specified in the *Intel® Celeron™ Processor EMTS*. (Also see figure below.) Future Celeron processors will use the larger fan heatsink, which demands adherence to maximum keep-out dimensions. Several previous 815 and 815E chipset based motherboards did not adhere to Intel specified keep-out requirements. When revising previous 815E motherboard designs to support the boxed Celeron processor manufactured on the 0.13-micron process technology, ensure motherboard components do not interfere with fan-heatsink maximum keep-out area.

Figure 34. Keep-Out Requirements for the 370-pin (Top View)

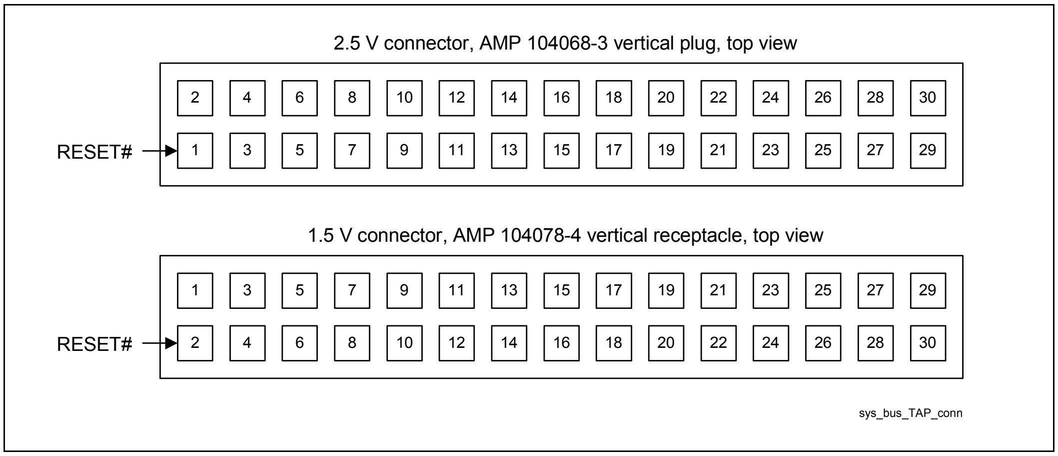


ALL DIMENSIONS ARE MINIMUM UNLESS OTHERWISE SPECIFIED

5.13 Debug Port Changes

Due to the lower voltage technology employed with newer processors, changes are required to support the debug port. Previously, test access port (TAP) signals used 2.5 V logic, as is the case with the Celeron processor in the PPGA package. Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors utilize 1.5 V logic levels on the TAP. As a result, the type of debug port connecter used in *universal PGA370* designs is dependent on the processor that is currently in the socket. The 1.5 V connector is a mirror image of the older 2.5 V connector. Either connector will fit into the same printed circuit board layout. Only the pin numbers change (see Figure 35). Also required, along with the new connector, is an In-Target Probe* (ITP) that is capable of communicating with the TAP at the appropriate logic levels.

Figure 35. TAP Connector Comparison



Caution: Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) require an in-target probe (ITP) compatible with 1.5 V signal levels on the TAP. Previous ITPs were designed to work with higher voltages and may damage the processor if connected to any of these specified processors.

See the processor datasheet for more information regarding the debug port.

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6 System Memory Design Guidelines

6.1 System Memory Routing Guidelines

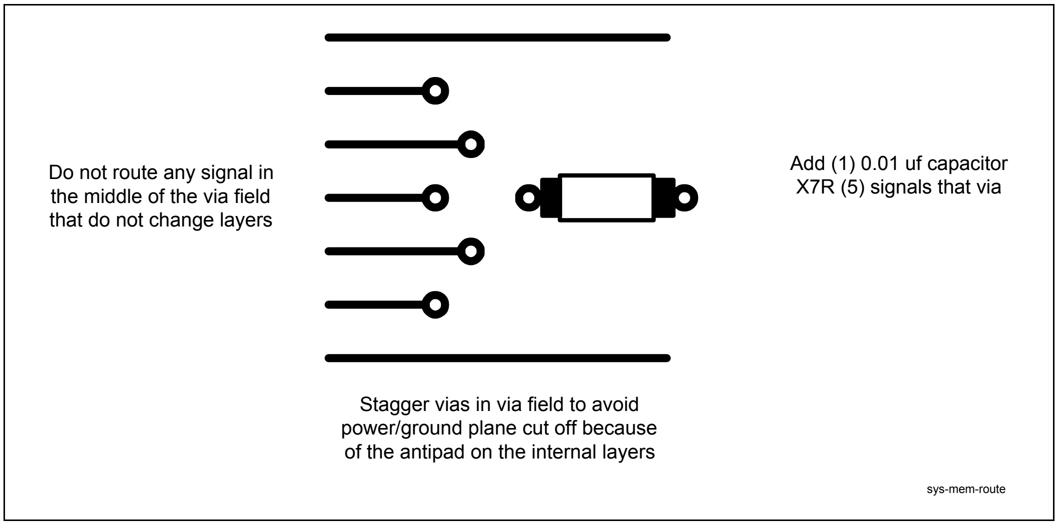
Ground plane reference all system memory signals. To provide a good current return path and limit noise on the system memory signals, the signals should be ground referenced from the GMCH to the DIMM connectors and from DIMM connector-to-DIMM connector. If ground referencing is not possible, system memory signals should be, at a minimum, referenced to a single plane. If single plane referencing is not possible, stitching capacitors should be added no more than 200 mils from the signal via field. System memory signals may via to the backside of the PCB under the GMCH without a stitching capacitor as long as the trace on the topside of the PCB is less than 200 mils.

Note: Intel recommends that a parallel plate capacitor between VCC3.3SUS and GND be added to account for the current return path discontinuity (See decoupling section). Use one 0.01 µF X7R capacitor per every five system memory signals that switch plane references. No more than two vias are allowed on any system memory signal.

If a group of system memory signals must to change layers, a via field should be created and a decoupling capacitor should be added at the end of the via field. Do not route signals in the middle of a via field; this causes noise to be generated on the current return path of these signals and can lead to issues on these signals (see Figure 36). The traces shown are on layer 1 only. The figure shows signals that are changing layer and two signals that are not changing layer.

Note: The two signals around the via field create a keep-out zone where no signals that do not change layer should be routed.

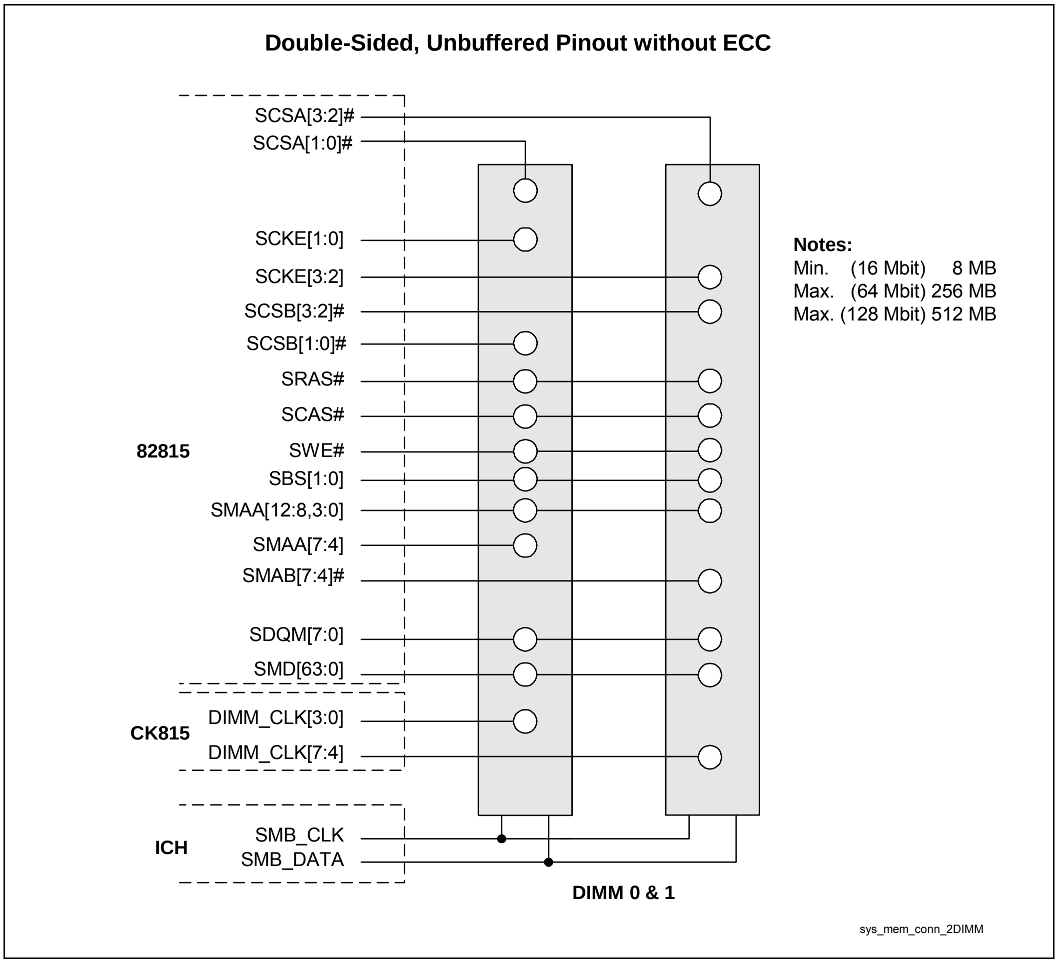
Figure 36. System Memory Routing Guidelines



6.2 System Memory 2-DIMM Design Guidelines

6.2.1 System Memory 2-DIMM Connectivity

Figure 37. System Memory Connectivity (2 DIMM)



6.2.2 System Memory 2-DIMM Layout Guidelines

Figure 38. System Memory 2-DIMM Routing Topologies

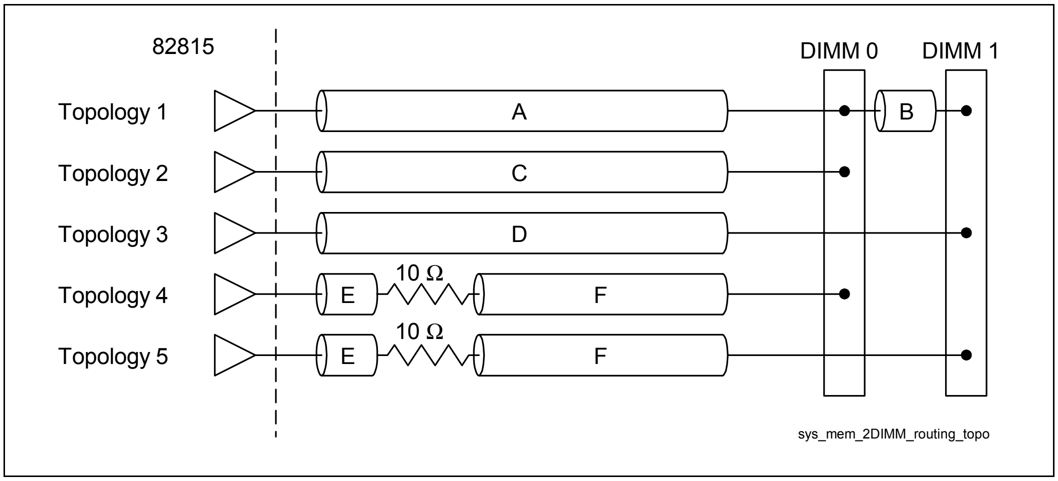
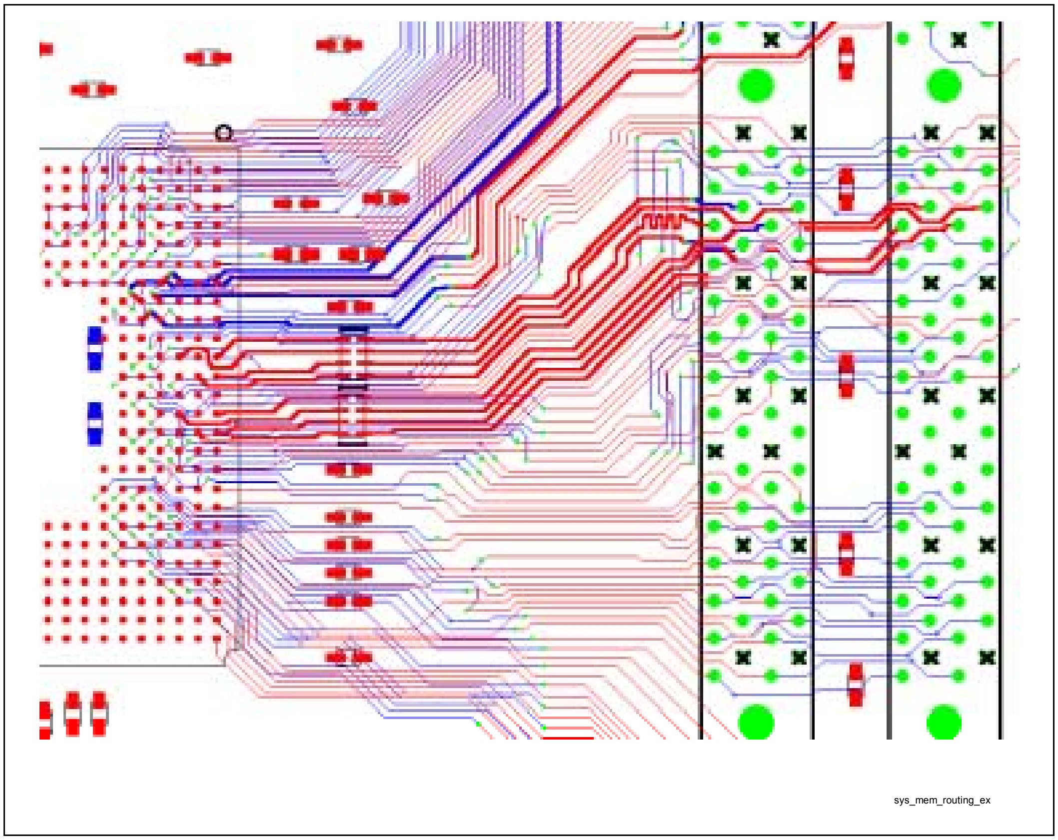


Table 19. System Memory 2-DIMM Solution Space

Signal	Top.	Trace (mils)		Trace Lengths (inches)											
				A		B		C		D		E		F	
		Width	Spacing	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SCS[3:2]#	3	5	10							1	4.5				
SCS[1:0]#	2	5	10					1	4.5						
SMAA[7:4]	4	10	10									0.4	0.5	2	4
SMAB[7:4]#	5	10	10									0.4	0.5	2	4
SCKE[3:2]	3	10	10							3	4				
SCKE[1:0]	2	10	10					3	4						
SMD[63:0]	1	5	10	1.75	4	0.4	0.5								
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5								
SCAS#, SRAS#, SWE#	1	5	10	1	4.0	0.4	0.5								
SBS[1:0], SMAA[12:8,3:0]	1	5	10	1	4.0	0.4	0.5								

In addition to meeting the spacing requirements outlined in Table 19, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

Figure 39. System Memory Routing Example

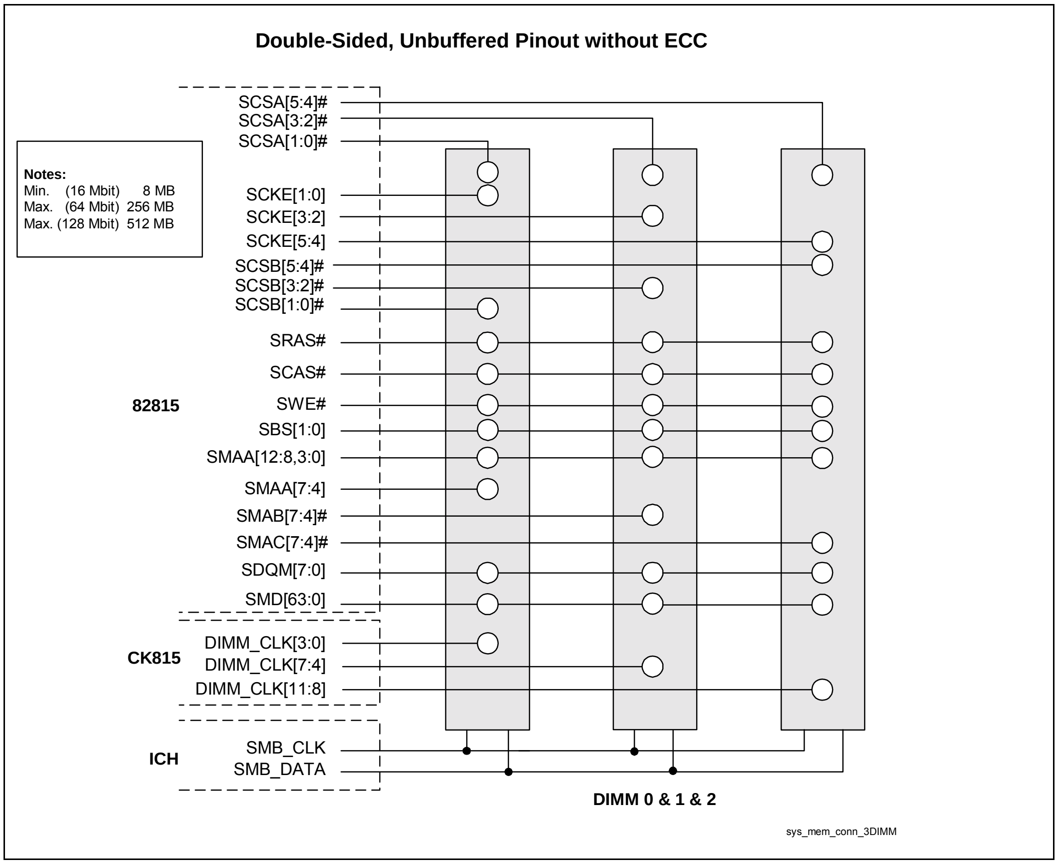


NOTE: Routing in this figure is for example purposes only. It does not necessarily represent complete and correct routing for this interface.

6.3 System Memory 3-DIMM Design Guidelines

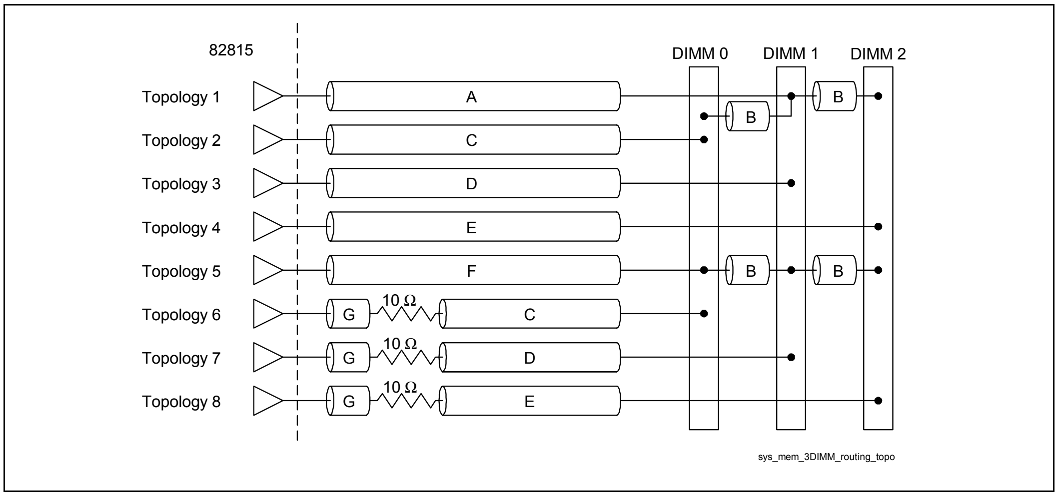
6.3.1 System Memory 3-DIMM Connectivity

Figure 40. System Memory Connectivity (3 DIMM)



6.3.2 System Memory 3-DIMM Layout Guidelines

Figure 41. System Memory 3-DIMM Routing Topologies



In addition to meeting the spacing requirements outlined in Table 20, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

Table 20. System Memory 3-DIMM Solution Space

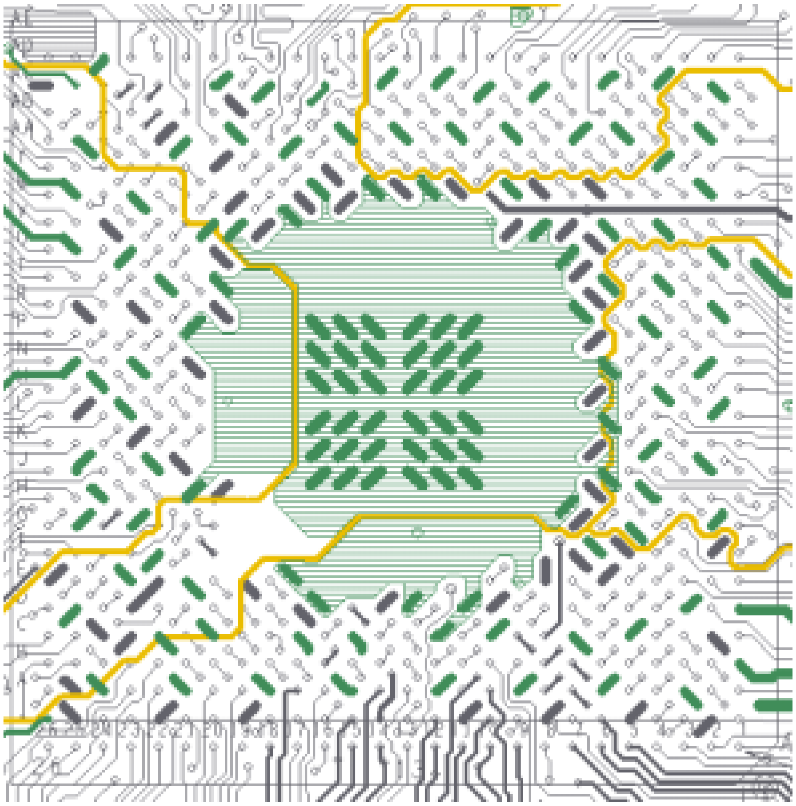
Signal		**Trace (mils)**		**Trace Lengths (inches)**													
				A		**B**		**C**		**D**		**E**		**F**		**G**	
	Top.	**Width**	**Spacing**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
SCS[5:4]#	4	5	10									1	4.5				
SCS[3:2]#	3	5	10							1	4.5						
SCS[1:0]#	2	5	10					1	4.5								
SMAA[7:4]	6	10	10					2	4							0.4	0.5
SMAB[7:4]#	7	10	10							2	4					0.4	0.5
SMAC[7:4}	8	10	10									2	4			0.4	0.5
SCKE[5:4]	4	10	10									3	4				
SCKE[3:2]	3	10	10							3	4						
SCKE[1:0]	2	10	10					3	4								
SMD[63:0]	1	5	10	1.75	4	0.4	0.5										
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5										
SCAS#, SRAS#, SWE#	5	5	10			0.4	0.5							1	4		
SBS[1:0], SMAA[12:8,3:0]	5	5	10			0.4	0.5							1	4		

6.4 System Memory Decoupling Guidelines

A minimum of eight 0.1 µF low-ESL ceramic capacitors (e.g., 0603 body type, X7R dielectric) are required and must be as close as possible to the GMCH. They should be placed within at most 70 mils to the edge of the GMCH package edge for VSUS_3.3 decoupling, and they should be evenly distributed around the system memory interface signal field including the side of the GMCH where the system memory interface meets the host interface. There are power and GND balls throughout the system memory ball field of the GMCH that need good local decoupling. Make sure to use at least 14 mil drilled vias and wide traces from the pads of the capacitor to the power or ground plane to create a low-inductance path. If possible, multiple vias per capacitor pad are recommended to further reduce inductance. To add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (500 mils maximum).

To further decouple the GMCH and provide a solid current return path for the system memory interface signals it is recommended that a parallel plate capacitor be added under the GMCH. Add a topside or bottom side copper flood under center of the GMCH to create a parallel plate capacitor between VCC3.3 and GND, see following figure. The dashed lines indicate power plane splits on layer 2 or layer 3 depending on stack-up. The filled region in the middle of the GMCH indicates a ground plate (on layer 1 if the power plane is on layer 2 or on layer 4 if the power layer is on layer 3).

Figure 42. Intel® 815G Chipset Platform Decoupling Example

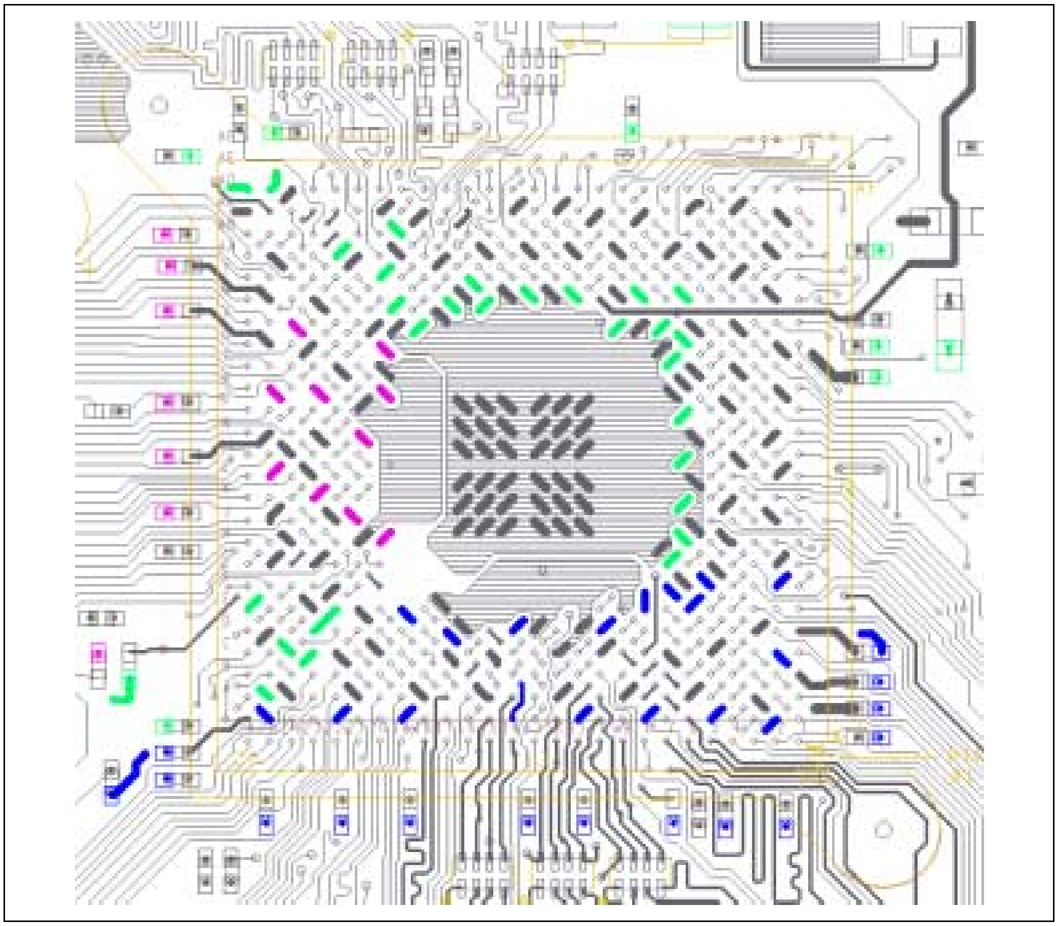


Yellow lines in Figure 42 show layer-two plane splits. (Printed versions of this document will show the layer two plane splits in the left-side, bottom, right-side, and upper-right-side quadrants enclosed in gray lines.) Note that the layer 1 shapes do **not** cross the plane splits. The bottom shape is a VSS fill over VddSDRAM. The left-side shape is a VSS fill over VddAGP. The larger upper-right-side shape is a VSS fill over VddCORE.

Additional decoupling capacitors shown in Figure 43 should be added between the DIMM connectors to provide a current return path for the reference plane discontinuity created by the DIMM connectors themselves. One 0.01 µF X7R capacitor should be added per every ten SDRAM signals. Capacitors should be placed between the DIMM connectors and evenly spread out across the SDRAM interface.

For debug purposes, four or more 0603 capacitor sites should be placed on the backside of the board, evenly distributed under the 815G chipset platform’s system memory interface signal field.

Figure 43. Intel® 815G Chipset Platform Decoupling Example



6.5 Compensation

A system memory compensation resistor (SRCOMP) is used by the GMCH to adjust the buffer characteristics to specific board and operating environment characteristics. Refer to the *Intel® 815 Chipset Family: 82815G Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370* Datasheet for details on compensation. Tie the SRCOMP pin of the GMCH to 40 Ω 1% or 2% pull-up resistor to 3.3 Vsus (3.3 V standby) via a 10-mil-wide, 0.5 inch trace (targeted for a nominal impedance of 40 Ω).

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7 Display Cache Design Guidelines

7.1 Display Cache Interface

The display cache interface of the 815G chipset is similar to the 810E chipset. Note that the display cache is optional. There do not have to be any GPA (Graphics Performance Accelerator) card SDRAM devices connected to the interface. The only dedicated display cache signals are OCLK and RCLK, which need not connect directly to the SDRAM devices.

7.2 GPA Card Considerations

To support the fullest flexibility, the display cache exists on an add-in card (AIMM or GPA) that complies with the AGP connector form factor. If the motherboard designer follows the flexible routing guidelines for the AGP interface, the customer can choose to populate the AGP slot in a system based on the 815G chipset platform with either a GPA card to enable the highest-possible internal graphics performance, or with nothing to get the lowest-cost internal graphics solution. AGP card functionality has been disabled in the 82815G GMCH device. Some of the GPA/ 815G chipset platform for use with the universal socket 370 interfacing implications are listed below. For a complete description of the GPA card design, refer to the *Graphics Performance Accelerator Card Specification* available from Intel.

- A strap is required to determine which frequency to select for display cache operation. This is the L_FSEL pin of the GMCH. The GPA card will pull this signal up or down, as appropriate to communicate to the appropriate operating frequency to the 815G chipset platform. The platform will sample this pin on the deasserting edge of reset.
- Since current SDRAM technology is always 3.3 V, the GPA card should set the TYPEDET# signal correctly to indicate that it requires a 3.3 V power supply. Furthermore, the GPA card should have only the 3.3 V key and not the 1.5 V key, thereby preventing it from being inserted into a 1.5 V-only connector.
- The pad buffers on the chip will be the normal AGP buffers and will work for both interfaces.
- In internal graphics mode, the AGPREF signal, which is required for the AGP mode, should remain functional as a reference voltage for sampling 3.3 V LMD inputs. The voltage level on AGPREF should remain exactly the same as in the AGP mode, as opposed to VCC/2 used for previous products.

7.3 GPA Mechanical Considerations

The GPA card will be designed with a notch on the PCB to go around the AGP universal retention mechanism. To guarantee that the GPA card will meet all shock and vibration requirements of the system, the AGP universal retention mechanism will be required on all AGP sockets that are to support a GPA card.

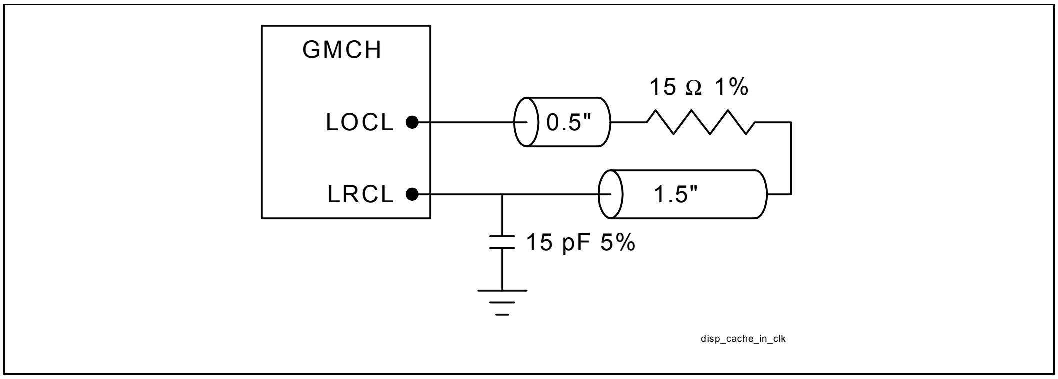
7.4 Display Cache Clocking

The display cache is clocked source-synchronously from a clock generated by the GMCH. The display cache clocking scheme uses three clock signals.

- **LTCLK** clocks the SDRAM devices, is muxed with an AGP signal, and should be routed according to the flexible AGP guidelines.
- **LOCLK and LRCLK** clock the input buffers of the universal platform. LOCLK is an output of the GMCH and is a buffered copy of LTCLK. LOCLK should be connected to LRCLK at the GMCH, with a length of PCB trace to create the appropriate clock skew relationship between the clock input (LRCLK) and the SDRAM capacitor clock input(s).

The guidelines are illustrated in Figure 44.

Figure 44. Display Cache Input Clocking



The capacitor should be placed as close as possible to the GMCH LRCLK pin. To minimize skew variation, Intel recommends a 1% series termination resistor and a 5% NP0 (also known as C0G) capacitor, to stabilize the value across temperatures. In addition to the 15 Ω, 1% resistor and the 15 pF, 5% NP0 capacitor. The following combination also can be used: 10 Ω, 1% and 22 pF, 5% NP0.

7.5 VDDQ Generation

NOTE: AGP functionality has been removed from the 82815G GMCH. However, VDDQ voltage must be maintained in 82815G designs even though the AGP capability is removed.

For the designer developing an 82815G motherboard, there is no distinction between VCC and VDDQ, as both are tied to the 3.3 V power plane on the motherboard.

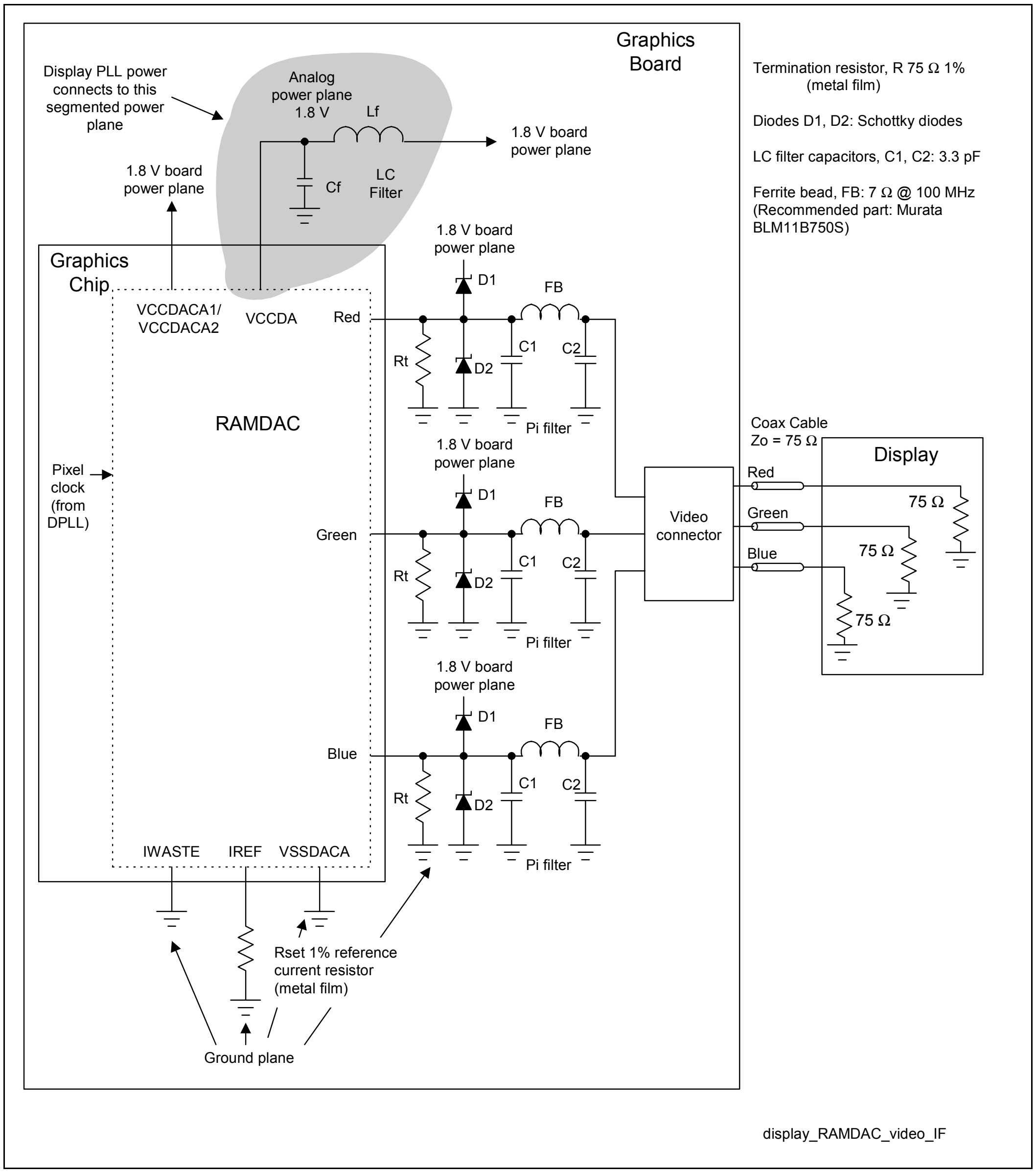
8 Integrated Graphics Display Output

8.1 Analog RGB/CRT

8.1.1 RAMDAC/Display Interface

Figure 45 shows the interface of the RAMDAC analog current outputs with the display. Each DAC output is doubly terminated with a 75 Ω resistance. One 75 Ω resistance is from the DAC output to the board ground and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC output is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also an LC pi-filter that is used to reduce high-frequency glitches and noise and to reduce EMI. To maximize performance, the filter impedance, cable impedance, and load impedance should be the same. The LC pi-filter consists of two 3.3 pF capacitors and a ferrite bead with a 75 Ω impedance at 100 MHz. The LC pi-filter is designed to filter glitches produced by the RAMDAC while maintaining adequate edge rates to support high-end display resolutions.

Figure 45. Schematic of RAMDAC Video Interface



NOTE: Diodes D_1, D_2 are clamping diodes with low leakage and low capacitive loading. An example is: California Micro Devices PAC DN006 (6 channel ESD protection array).

In addition to the termination resistance and LC pi-filter, there are protection diodes connected to the RAMDAC outputs to help prevent latch-up. The protection diodes must be connected to the same power supply rails as the RAMDAC. An LC filter is recommended to connect the segmented analog 1.85 V power plane of the RAMDAC to the 1.85 V board power plane. The LC filter should be designed for a cut-off frequency of 100 kHz.

8.1.2 Reference Resistor (Rset) Calculation

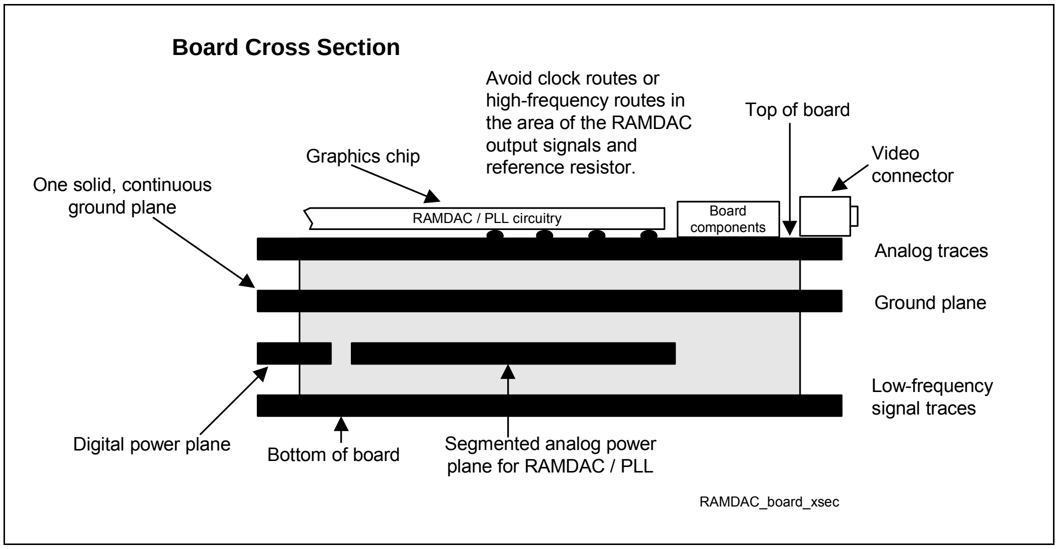
The full-swing video output is designed to be 0.7V according to the VESA video standard. With an equivalent DC resistance of 37.5 Ω (two 75 Ω in parallel; one 75 Ω termination on the board and one 75 Ω termination within the display), the full-scale output current of a RAMDAC channel is 0.7/37.5 Ω = 18.67 mA. Since the RAMDAC is an 8-bit current-steering DAC, this full-scale current is equivalent to 255 I, where I is a unit current. Therefore, the unit current or LSB current of the DAC signals equals 73.2 µA. The reference circuitry generates a voltage across this R_{set} resistor equal to the bandgap voltage divided by three (407.6 mV). The RAMDAC reference current generation circuitry is designed to generate a 32-I reference current using the reference voltage and the R_{set} value. To generate a 32-I reference current for the RAMDAC, the reference current setting resistor, R_{set}, is calculated using the following equation:

$$R_{set} = VREF / 32*I = 0.4076\ V / 32*73.2\ \mu A = 174\ \Omega$$

8.1.3 RAMDAC Board Design Guidelines

Figure 46 shows a general cross-section of a typical four-layer board. The recommended RAMDAC routing for a four-layer board is such that the red, green, and blue video outputs are routed on the top (bottom) layer over (under) a solid ground plane to maximize the noise rejection characteristics of the video outputs. It is essential to prevent toggling signals from being routed next to the video output signals to the VGA connector. A 20-mil spacing between any video route and any other routes is recommended.

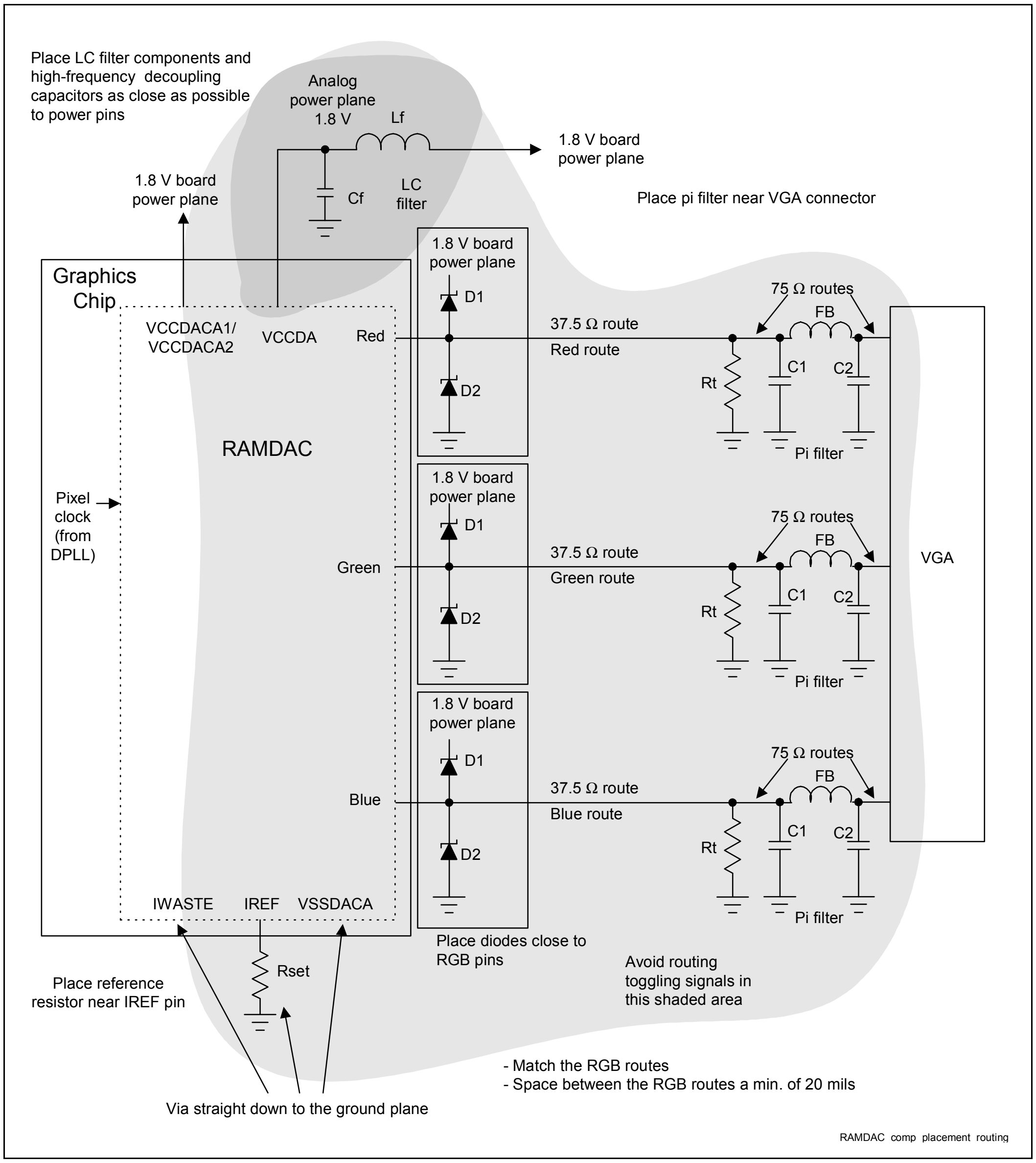
Figure 46. Cross-Sectional View of a Four-Layer Board



Matching the video routes (i.e., red, green, blue) from the RAMDAC to the VGA connector also is essential. The routing for these signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends, and jogs).

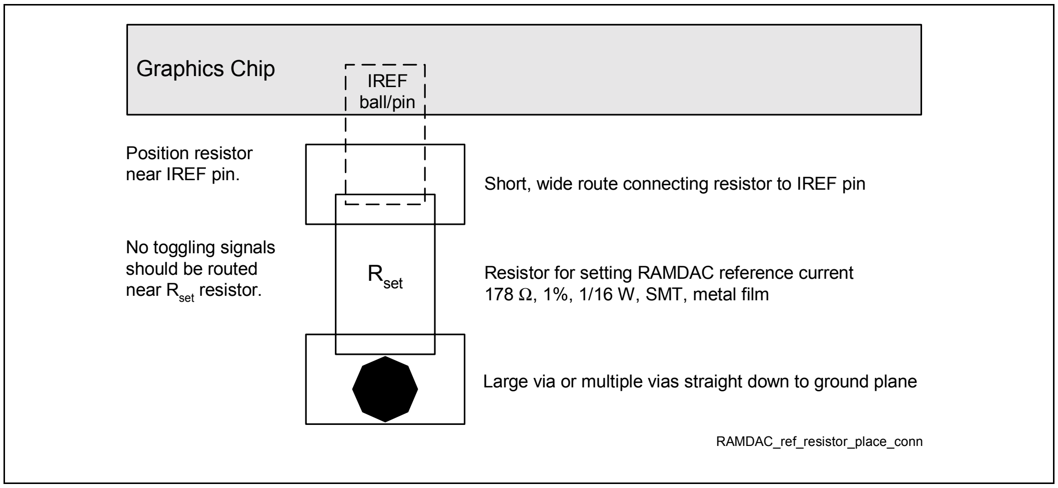
Figure 47 shows the recommended RAMDAC component placement and routing. The termination resistance can be placed anywhere along the video route from the RAMDAC output to the VGA connector, as long as the trace impedances are designed as indicated in the following figure. It is advisable to place the pi-filters in close proximity with the VGA connector, to maximize the EMI filtering effectiveness. The LC filter components for the RAMDAC/PLL power plane, the decoupling capacitors, the latch-up protection diodes, and the reference resistor should be placed in close proximity with the respective pins. Figure 48 shows the recommended reference resistor placement and the ground connections.

Figure 47. Recommended RAMDAC Component Placement & Routing



NOTE: Diodes D_1, D_2 are clamping diodes with low leakage and low capacitive loading. An example is: California Micro Devices PAC DN006 (6 channel ESD protection array).

Figure 48. Recommended RAMDAC Reference Resistor Placement and Connections



8.1.4 RAMDAC Layout Recommendations

- The primary concern with regard to the RGB signal length is that the RGB routes are matched and routed with the correct impedance. The impedance should be 37.5 Ω, single-ended trace to the 75 Ω, termination resistor. Routing from the 75 Ω resistor to the video pi-filter and to the VGA connector should be 75 Ω impedance.
- The trace width for the RGB signal should be selected for a 37.5 Ω impedance (single-ended route) to the 75 Ω termination resistor. The 75 Ω termination resistor should be placed near the VGA connector.
- The spacing for each DAC channel routing (i.e., between red and green, green and blue outputs) should be a minimum of 20 mils.
- The space between the RGB signal route and other routes should be a minimum of 20 mils for each DAC route.
- All RGB signals should be referenced to ground.
- The trace width for the HSYNC and VSYNC signal routes should be selected for an approximately 40 Ω impedance.
- The spacing between the HSYNC /VSYNC signal routes should be at least 10 mils, preferably 20 mils.
- The space between HSYNC/VSYNC signal routes and other routes should be at least 10 mils, preferably 20 mils.
- Route the HSYNC and VSYNC over the ground plane, if possible. The HSYNC and VSYNC signals should not route over or near any clock signals or any other high switching routing.

8.1.5 HSYNC/VSYNC Output Guidelines

The HSYNC and VSYNC output of the GMCH may exhibit up to 1.26V P-P noise when driven high under high traffic system memory conditions. To minimize this, the following is required:

- Add external buffers to HSYNC and VSYNC.
    - — Examples include: Series 10 Ω resistor with a 74LVC08

8.2 Digital Video Out

The Digital Video Out (DVO) port is a scaleable, low-interface port that ranges from 1.1V to 1.8 V. This DVO port interfaces with a discrete TV encoder to enable platform support for TV-Out, with a discrete TMDS transmitter to enable platform support for DVI-compliant digital displays, or with an integrated TV encoder and TMDS transmitter.

The GMCH DVO port controls the video front-end devices via an I^2C interface, by means of the LTVDA and LTVCK pins. I^2C is a two-wire communications bus/protocol. The protocol and bus are used to collect EDID (extended display identification) from a digital display panel and to detect and configure registers in the TV encoder or TMDS transmitter chips.

8.2.1 DVO Interface Routing Guidelines

Route data signals (LTVDATA[11:0]) with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the GMCH, the DVO data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH component. The maximum trace length for the DVO data signals is 7 inches. These signals should each be matched within ±0.1 inch of the LTVCLKOUT[1] and LTVCLKOUT[0] signals.

Route the LTVCLKOUT[1:0] signals 5 mils wide and 20 mils apart. This signal pair should be a minimum of 20 mils from any adjacent signals. The maximum length for LTVCLKOUT[1:0] is 7 inches and the two signals should be the same length.

8.2.2 DVO I^2C Interface Considerations

LTVDA and LTVCK should be connected to the TMDS transmitter, TV encoder or integrated TMDS transmitter/TV encoder device, as required by the specifications for those devices. LTVDA and LTVCK should also be connected to the DVI connector as specified by the DVI specification. Pull-ups of 4.7 kΩ (or pull-ups with the appropriate value derived from simulation) are required on each of LTVDA and LTVCK.

8.2.3 Leaving the DVO Port Unconnected

If the motherboard does not implement any of the possible video devices with the universal platform’s DVO port, the following are recommended on the motherboard:

- Pull-up LTVDA and LTVCK with 4.7 kΩ resistors at the GMCH. This will prevent the universal platform’s DVO controller from confusing noise on these lines for false I^2C cycles.
- Route LTVDATA[11:0] and LTVCLKOUT[1:0] out of the BGA to test points for use by automated test equipment (if required). These signals are part of one of the GMCH XOR chains.

9 Hub Interface

The GMCH ball assignment and the ICH ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals be routed directly from the GMCH to ICH with all signals referenced to VSS (see Figure 49). Layer transition should be kept to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

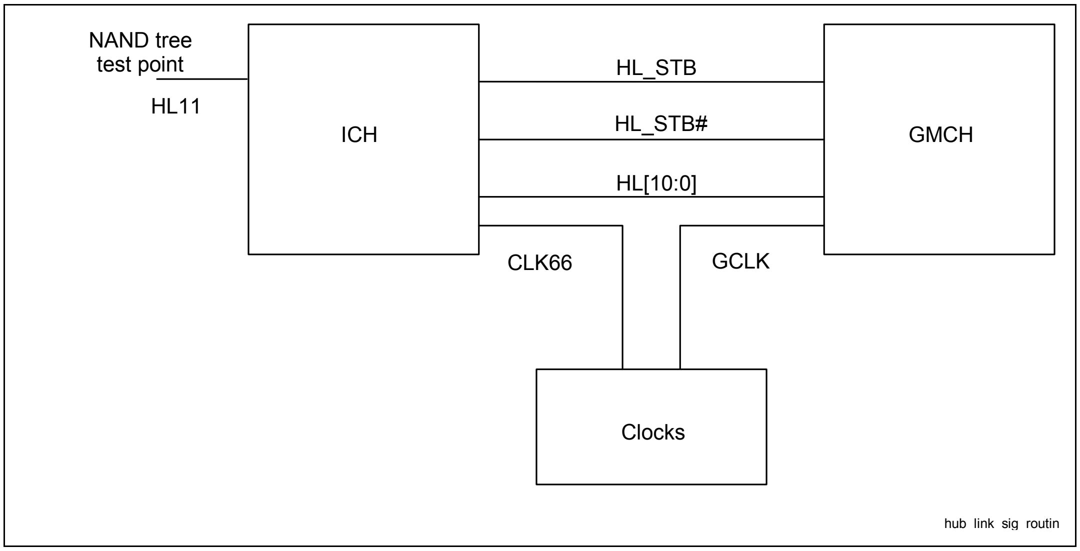
The hub interface signals are divided into two groups: data signals (HL) and strobe signals (HL_STB). For the 8-bit hub interface, HL[0:7] are associated with HL_STB and HL_STB#.

- Data Signals:
  - HL[10:0]
- Strobe Signals:
  - HL_STB
  - HL_STB#

Note: HL_STB/HL_STB# is a differential strobe pair.

No pull-ups or pull-downs are required on the hub interface. HL11 on the ICH should be brought out to a test point for NAND Tree testing. Each signal should be routed such that it meets the guidelines documented for its signal group.

Figure 49. Hub Interface Signal Routing Example



9.1.1 Data Signals

Hub interface data signals should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the GMCH and the ICH, the hub interface data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH/ICH components.

The maximum trace length for the hub Interface data signals is 7 inches. These signals should each be matched within ±0.1 inch of the HL_STB and HL_STB# signals.

9.1.2 Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signal. The maximum length for the strobe signals is 7 inches, and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes, within ±0.1 inch.

9.1.3 HREF Generation/Distribution

HREF is the hub interface reference voltage. It is 0.5 * 1.85 V = 0.92 V ± 2%. It can be generated using a single HREF divider or locally generated dividers (see Figure 50 and Figure 51). The resistors should be equal in value and rated at 1% tolerance (to maintain 2% tolerance on 0.9V). The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from a minimum of 100 Ω to a maximum of 1 kΩ (300 Ω shown in example).

The single HREF divider should not be located more than 4 inches away from either the GMCH or ICH. If the single HREF divider is located more than 4 inches away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor must be close to the component HREF pin.

Figure 50. Single-Hub-Interface Reference Divider Circuit

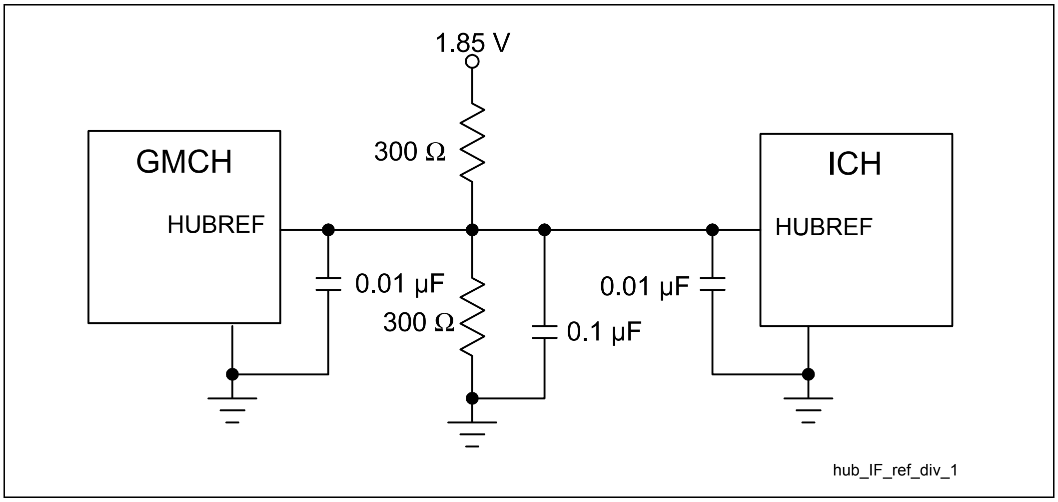
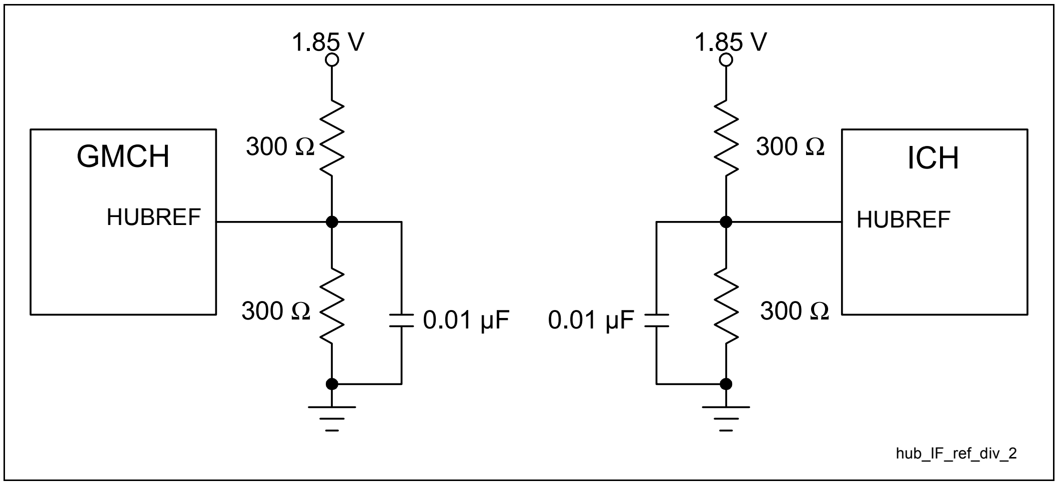


Figure 51. Locally Generated Hub Interface Reference Dividers



9.1.4 Compensation

Independent hub interface compensation resistors are used by the GMCH and ICH to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 815 Chipset Family: 82815G/82815EG Graphics and Memory Controller Hub (GMCH) for use with Universal Socket 370 Datasheet* and the *Intel® 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub Datasheet* for details on compensation. The resistive compensation (RCOMP) guidelines are as follows:

- **RCOMP:** Tie the HLCOMP pin of each component to a 40 Ω 1% or 2% pull-up resistor (to 1.85 V) via a 10-mil-wide, 0.5 inch trace (targeted at a nominal trace impedance of 40 Ω). The GMCH and ICH each requires their own RCOMP resistor.

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10 I/O Subsystem

This chapter provides guidelines for connecting and routing the IDE, AC '97, USB, I/O APIC, SMBus, PCI, LPC/FWH, and RTC subsystems.

10.1 IDE Interface

This section contains guidelines for connecting and routing the ICH IDE interface. The ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement and signal termination for both IDE channels. The ICH has integrated the series resistors that typically have been required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. Intel does not anticipate requiring additional series termination, but OEMs should verify the motherboard signal integrity via simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by providing future stuffing options.

The IDE interface can be routed with 5-mil traces on 5-mil spaces, and it should be less than 8 inches long (from ICH to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 1 inch shorter than the longest IDE signal (on the channel).

10.1.1 Cabling and Motherboard Requirements

- **Length of Cable:** Each IDE cable must be equal to or less than 18 .
- **Cable Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the connector next closest to the end of the cable (6 inches away from the end of the cable).
- **Grounding:** Provide a direct low-impedance chassis path between the motherboard ground and hard disk drives.
- **Ultra ATA/66:** Ultra ATA/66 requires the use of an 80-conductor cable.
- **ICH Placement:** The ICH must be placed at most 8 inches from the ATA connector(s).
- **Termination Resistors:** There is no need for series termination resistors on the data and control signals, since series termination is integrated into these signal lines on the ICH.
- **Capacitance:** The capacitance of each pin of the IDE connector on the host should be less than 25 pF when the cables are disconnected from the host.
- **IDE Absent:** If no IDE is implemented with the ICH, the input signals (xDREQ and xIORDY) can be grounded and the output signals can be left as no connects.

Figure 52. IDE Minimum/Maximum Routing and Cable Lengths

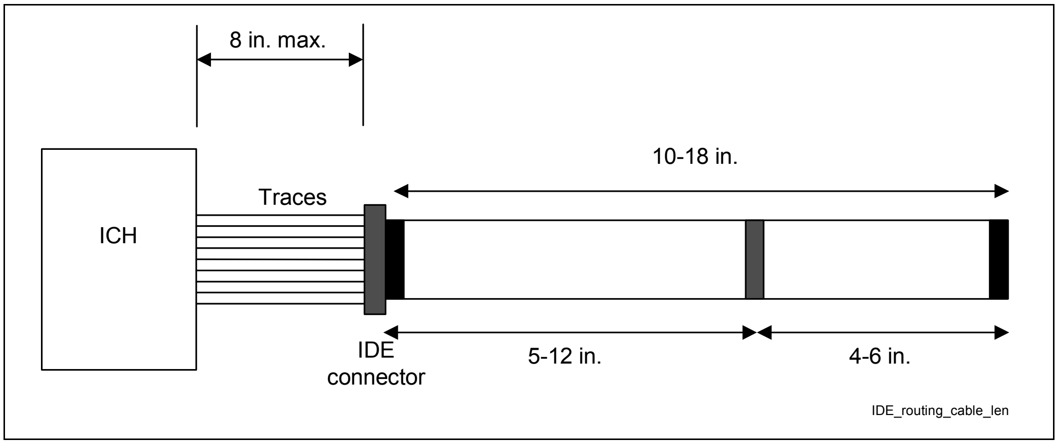
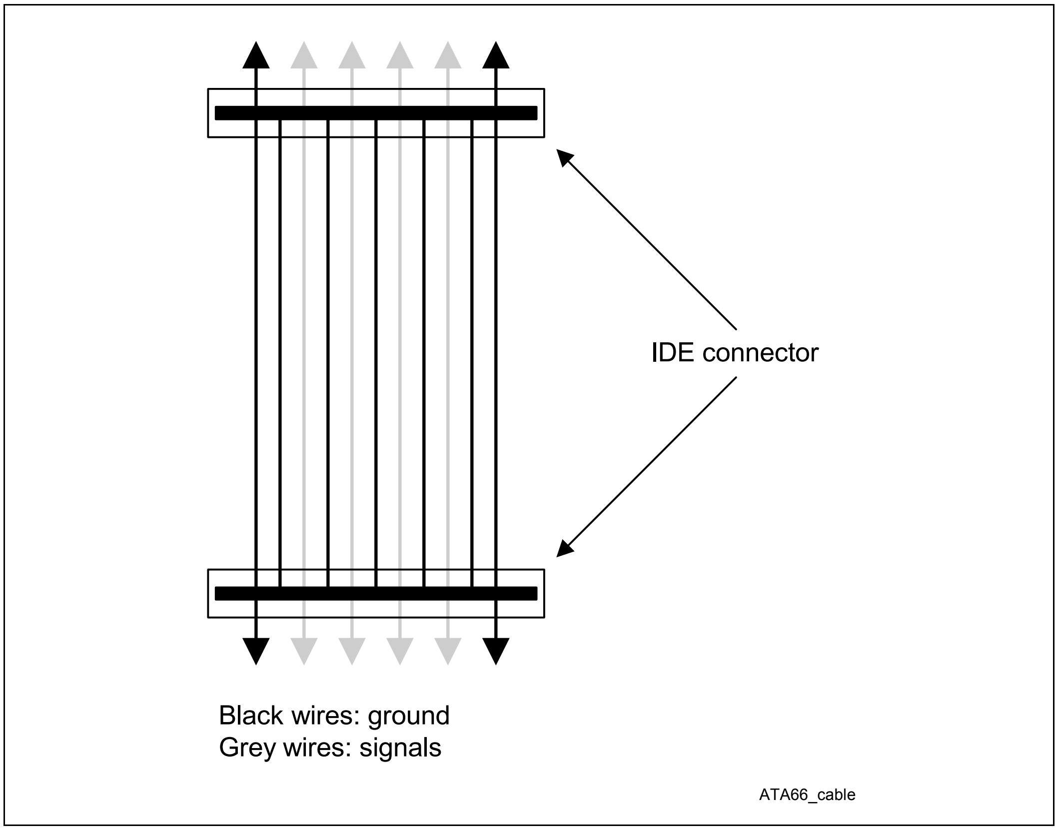


Figure 53. Ultra ATA/66 Cable



10.2 Cable Detection for Ultra ATA/66

An 80-conductor IDE cable is required for Ultra ATA/66. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal,. . . . All ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*, which is obtainable from the Small Form Factor Committee.

To determine whether the ATA/66 mode can be enabled, the chipset using the ICH requires the system BIOS to attempt to determine the type of cable used in the system. The BIOS does this in one of two ways:

- Host-side detection
- Device-side detection

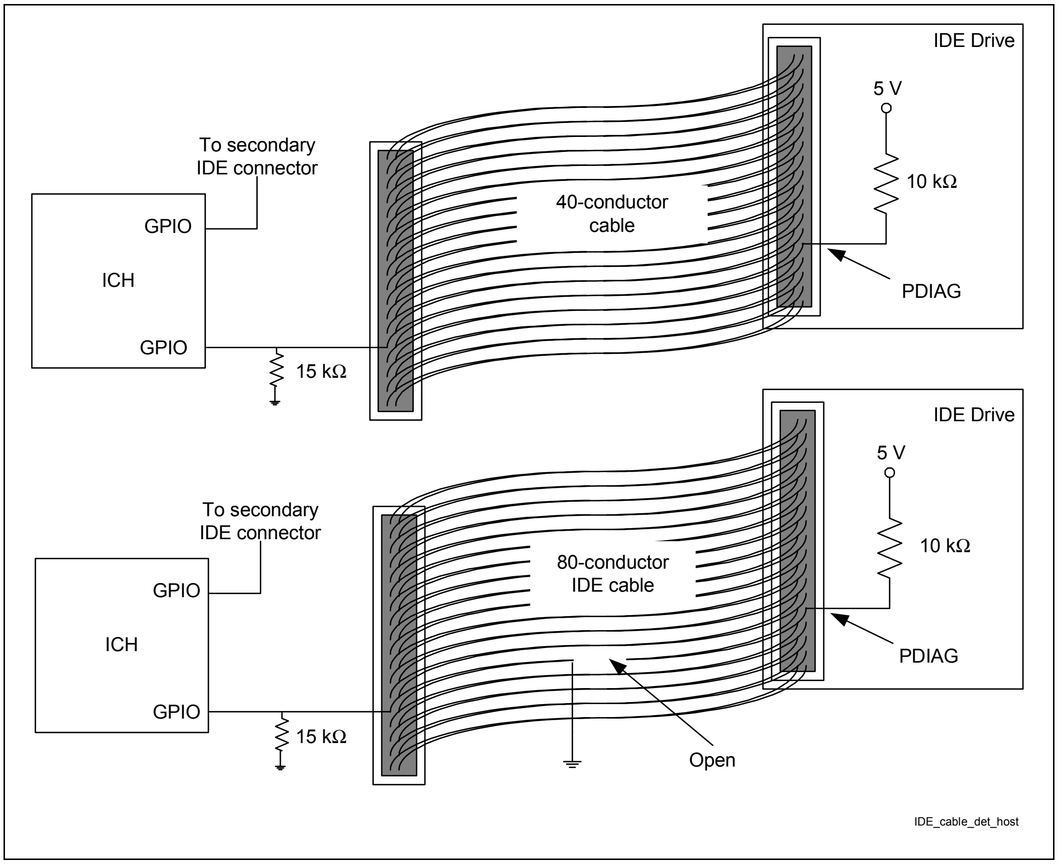
To determine whether the ATA/66 mode can be enabled, the ICH requires that the system software attempt to determine the type of cable used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

10.2.1 Host Side Cable Detection

BIOS Detects Cable Type Using GPIOs

Host-side detection requires the use of two GPI pins (one per IDE controller). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 54. All Ultra ATA/66 devices have a 10 kΩ pull-up resistor to 5 V. Most GPIO pins on the ICH and all GPIs on the FWH are not 5 V tolerant. This requires a resistor divider so that 5 V will not be driven to the ICH or FWH pins. The proper value of the series resistor is 15 kΩ (as shown in the following figure). This creates a 10 kΩ/15 kΩ resistor divider and will produce approximately 3 V for a logic high. This mechanism allows the host to sample PDIAG#/CBLID#, after diagnostics. If PDIAG#/CBLIB# is high, then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG#/CBLID# is low, then there is an 80-conductor cable in the system.

Figure 54. Host-Side IDE Cable Detection

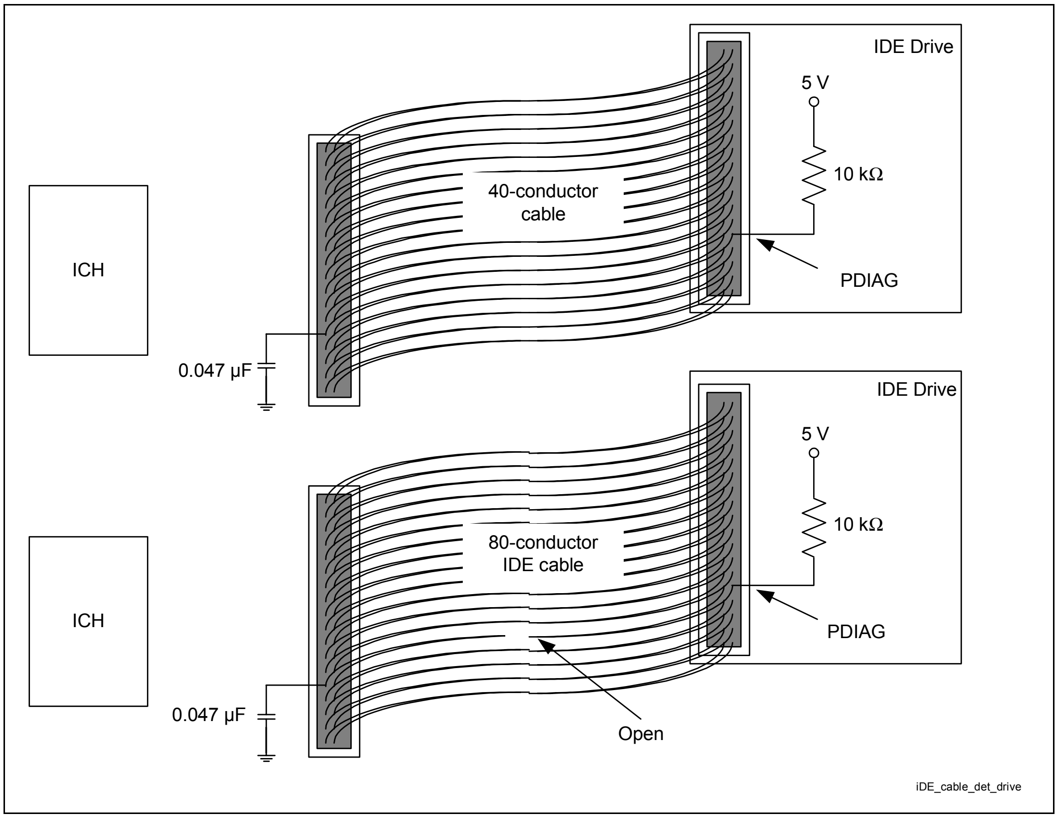


10.2.2 Device Side Cable Detection

BIOS Queries IDE Device for Cable Type

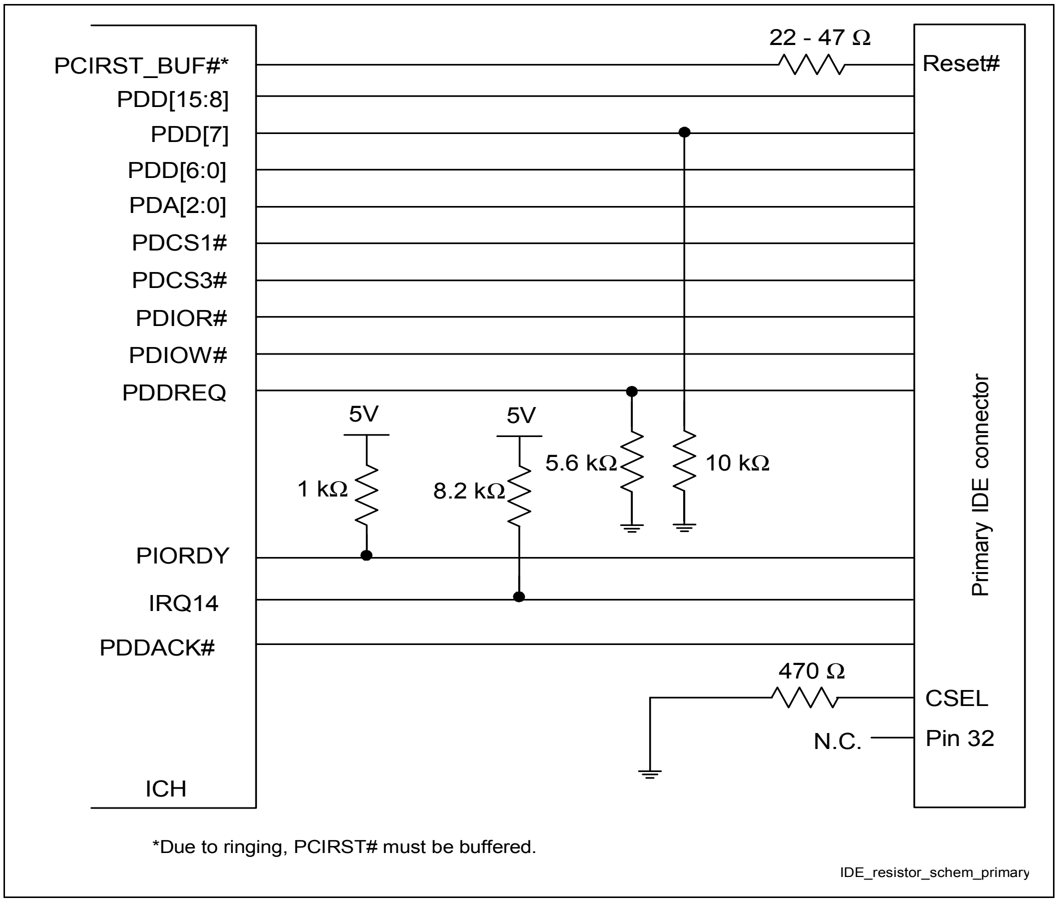
Device-side detection requires only a 0.047 µF capacitor on the motherboard, as shown in Figure 55. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 device will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The device will sample the PDIAG# signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through; therefore, the capacitor has no effect. In a 40-conductor cable, PDIAG#/CBLID# is connected through to the device; therefore, the signal will rise more slowly. The device can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot, as described in the ATA/66 specification.

Figure 55. Drive-Side IDE Cable Detection



10.2.3 Primary IDE Connector Requirements

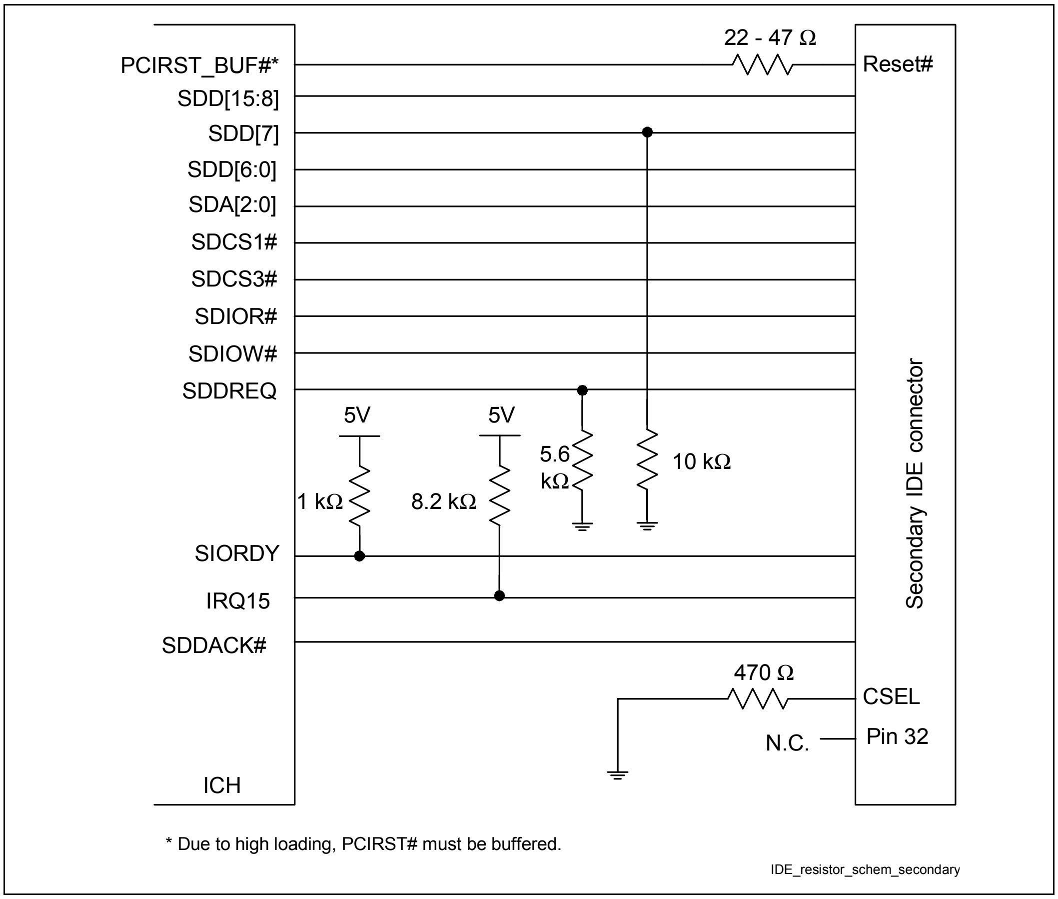
Figure 56. Resistor Schematic for Primary IDE Connectors



- Due to the elimination of the ISA bus from the ICH, PCI_RST# should be connected to pin 1 of the IDE connectors as the IDE reset signal. Because of high loading, the PCI_RST# signal should be buffered.
- 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- IRQ14 and IRQ15 each require an 8.2 kΩ pull-up resistor to VCC.
- A 1 kΩ pull-up to 5 V is required on PIORDY and SIORDY.
- A 470 Ω pull-down is required on pin 28 of each connector.
- A 5.6 kΩ pull-down is required on PDREQ and SDREQ.
- The primary IDE connector uses IRQ14, and the secondary IDE connector uses IRQ15.
- There is no internal pull-up or pull-down on PDD7 or SDD7 of the ICH. Devices must not have a pull-up resistor on DD7. It is recommended that a host have a 10 kΩ pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up (as required by the ATA-4 specification).

10.2.4 Secondary IDE Connector Requirements

Figure 57. Resistor Schematic for Secondary IDE Connectors



- Due to the elimination of the ISA bus from the ICH, PCI_RST# should be connected to pin 1 of the IDE connectors as the IDE reset signal. Because of high loading, the PCI_RST# signal should be buffered.
- 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- IRQ14 and IRQ15 each require an 8.2 kΩ pull-up resistor to VCC.
- A 1 kΩ pull-up to 5 V is required on PIORDY and SIORDY.
- A 470 Ω pull-down is required on pin 28 of each connector.
- A 5.6 kΩ pull-down is required on PDREQ and SDREQ.
- The primary IDE connector uses IRQ14, and the secondary IDE connector uses IRQ15.
- There is no internal pull-up or pull-down on PDD7 or SDD7 of the ICH. Devices must not have a pull-up resistor on DD7. It is recommended that a host have a 10 kΩ pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up (as required by the ATA-4 specification).

10.2.5 Layout for Both Host-Side and Device-Side Cable Detection

The 815G chipset platform (using the ICH) can use two methods to detect the cable type. Each mode requires a different motherboard layout.

It is possible to lay out for both host-side and device-side cable detection and decide the method to be used during assembly. Figure 58 shows the layout that allows for both host-side and drive-side detection.

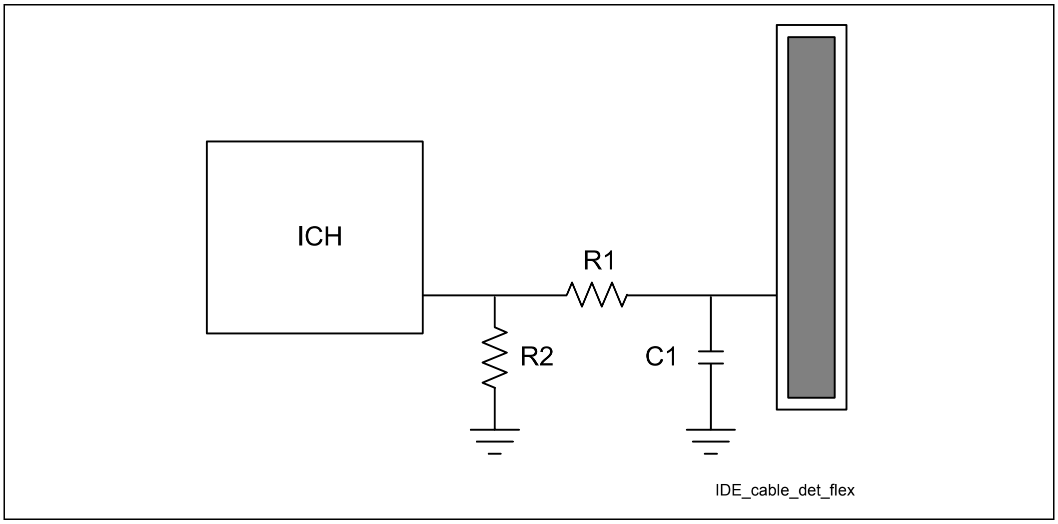
For Host-Side Detection:

- R1 is a 0 Ω resistor.
- R2 is a 15 kΩ resistor.
- C1 is not stuffed.

For Device-Side Detection:

- R1 is not stuffed.
- R2 is not stuffed.
- C1 is a 0.047 µF capacitor.

Figure 58. Flexible IDE Cable Detection



10.3 AC ’97

The ICH implements an *AC ’97 v2.2*-compliant digital controller. Any codec attached to the ICH AC-link must be *AC ’97 v2.2*compliant as well. Contact your codec IHV for information on *AC ’97 v2.2*compliant products. The *AC ’97 v2.2*specification is available on the Intel website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The ICH supports the codec combinations listed in Table 21.

Table 21. AC ’97 Configuration Combinations

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in Table 21, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC may not be present.

10.3.1 AC ’97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH) and by any other codec present. The clock is used as the time base for latching and driving data.

The ICH supports wake-on-ring from S1–S4 via the AC-link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

If no codec is attached to the link, internal pull-downs will prevent the inputs from floating. Therefore, external resistors are not required.

10.3.2 AC ’97 Signal Quality Requirements

In a lightly loaded system (e.g., single codec down), AC ’97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet *AC ’97 v2.2*, with the specified load of 50 pF.

10.3.3 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH platform using AC ’97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH platform.

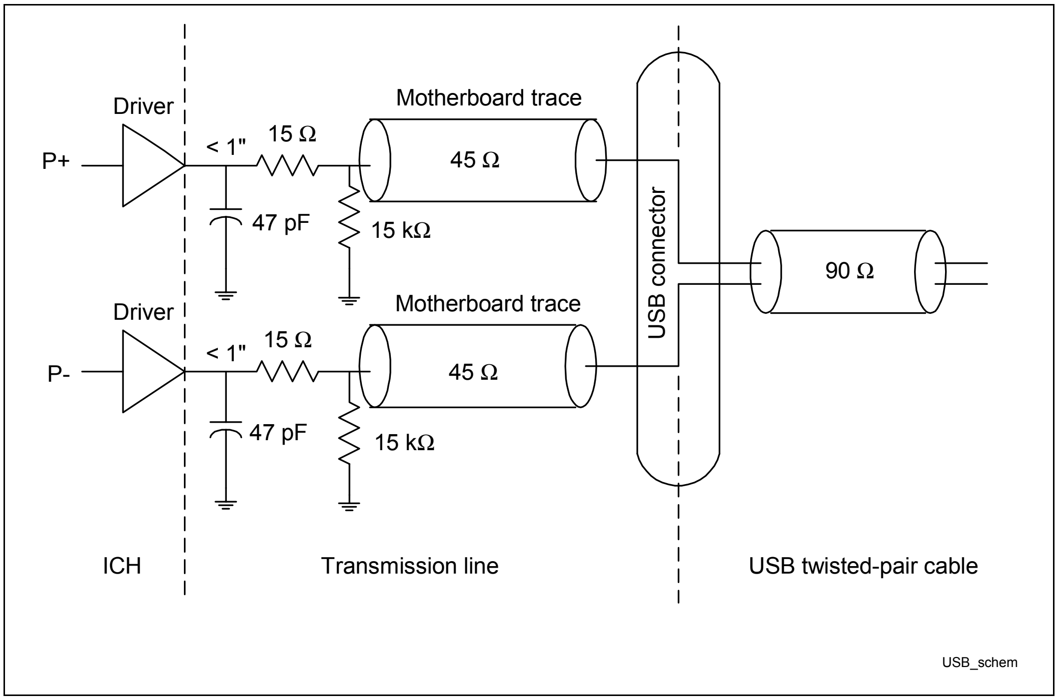
- Codec Implementation
  - Any valid combination of codecs may be implemented on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on a CNR module. However, nothing precludes a modem codec on the motherboard.
  - Only one primary codec may be present on the link. A maximum of two codecs can be supported in an ICH platform.
  - Components (e.g., FET switches, buffers or logic states) should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
  - The ICH supports wake-on-ring from S1–S4 states via the AC-link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required. The ICH does not wake from the S5 state via the AC-link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active. Rather, they should be pulled to ground through a weak (approximately 10 kΩ) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH’s internal pull-down resistors are enabled, so there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that might not be connected to a codec*. For example, if a dedicated audio codec is on the motherboard and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. However, if the SDATAIN signal has no codec connected or is connected to an on-board codec that can be hardware-disabled, then the signal should have an external pull-down resistor to ground.
- The ICH provides internal weak pull-downs. Therefore, the motherboard does not need to provide discrete pull-down resistors.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.4 Using Native USB Interface

The following are general guidelines for the native USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH (<1 inch). These series resistors provide source termination of the reflected signal.
- 47 pF capacitors must be placed as close as possible to the ICH as well as on the ICH side of the series resistors on the USB data lines (P0±, P1±). These capacitors are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ±5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±). They provide the signal termination required by the USB specification. The stub should be as short as possible.
- The trace impedance for the P0± and P1± signals should be 45 Ω (to ground) for each USB signal P+ or P-. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 3. The impedance is 90 Ω between the differential signal pairs P+ and P-, to match the 90 Ω USB twisted-pair cable impedance. Note that the twisted-pair characteristic impedance of 90 Ω is the series impedance of both wires, which results in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as ‘critical signals’ (i.e., hand-routing preferred). The P+/P- signal pair should be routed together and not parallel to other signal traces, to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. The P+/P- signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

Figure 59. Recommended USB Schematic



The recommended USB trace characteristics are as follows:

- Impedance ‘Z0’ = 45.4 Ω
- Line delay = 160.2 ps
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Res at 20 °C = 53.9 mΩ

10.5 I/O APIC (I/O Advanced Programmable Interrupt Controller)

Systems not using the I/O APIC should comply with the following recommendations:

- On the ICH
  - Connect PICCLK directly to ground.
  - Connect PICD0, PICD1 to ground through a 10 kΩ resistor.
- On the processor
  - PICCLK requires special implementation for universal motherboard designs. See Section 4.2.9
  - Connect PICD0 to 2.5 V through 10 kΩ resistors.
  - Connect PICD1 to 2.5 V through 10 kΩ resistors.

10.6 SMBus

The **Alert on LAN** signals can be used as:

- **Alert on LAN signals:** 4.7 kΩ pull-up resistors to 3.3VSB are required.
- **GPIOs:** Pull-up resistors to 3.3VSB and the signals must be allowed to change states on power-up. (For example, on power-up the ICH drives *heartbeat* messages until the BIOS programs these signals as GPIOs.) The values of the pull-up resistors depend on the loading on the GPIO signal.
- **Not Used:** 4.7 kΩ pull-up resistors to 3.3VSB are required.

If the SMBus is used only for the three SPD EEPROMs (one on each RIMM), both signals should be pulled up with a 4.7 kΩ resistor to 3.3 V.

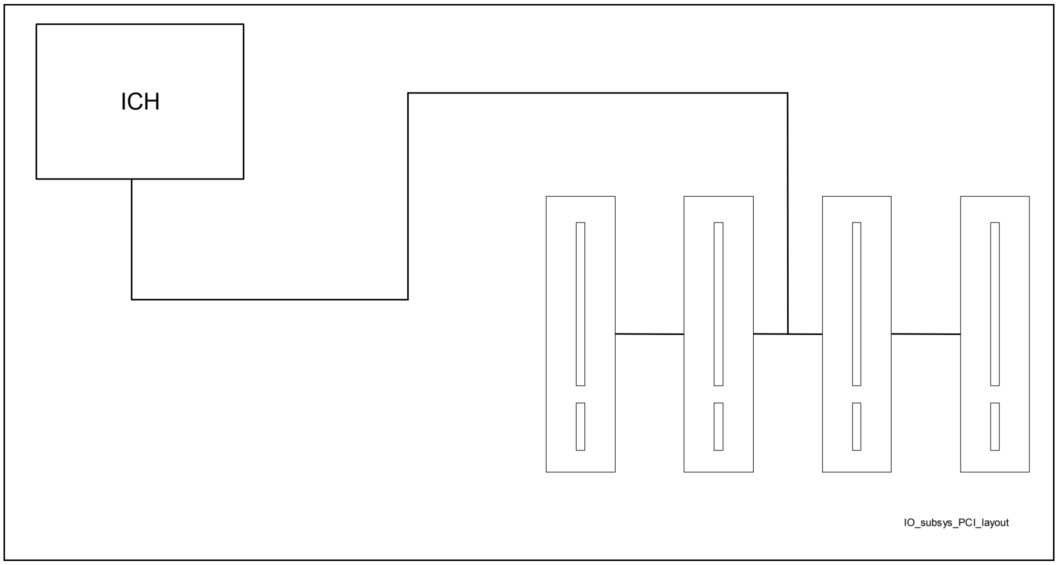
10.7 PCI

The ICH provides a PCI bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH supports 6 PCI Bus masters by providing 6 REQ#/GNT# pairs. In addition, the ICH supports 2 PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Based on simulations performed by Intel, a maximum of 4 PCI slots should be connected to the ICH. This limit is due to timing and loading considerations established during simulations. If a system designer wants 5 PCI slots connected to the ICH, then the designer's company should perform its own simulations to verify a proper design.

Figure 60. PCI Bus Layout Example for Four PCI Connectors



10.8 LPC/FWH

10.8.1 In-Circuit FWH Programming

All cycles destined for the FWH will appear on the PCI. The ICH hub interface to the PCI bridge puts all processor boot cycles out on the PCI (before sending them out on the FWH interface). If the ICH is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on PCI. This enables booting from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH in subtractive decode mode. If a PCI boot card is inserted and the ICH is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it also is necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind the 82380AB. After booting from the PCI card, one potentially could program the FWH in circuit and program the ICH CMOS.

10.8.2 FWH V_{PP} Design Guidelines

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports a V_{PP} of 3.3 V or 12 V. If V_{PP} is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V V_{PP} for 80 hours. The 12 V V_{PP} would be useful in a programmer environment, if it typically is an event that occurs very infrequently (much fewer than 80 hours). The V_{PP} pin **must** be tied to 3.3 V on the motherboard.

10.9 RTC

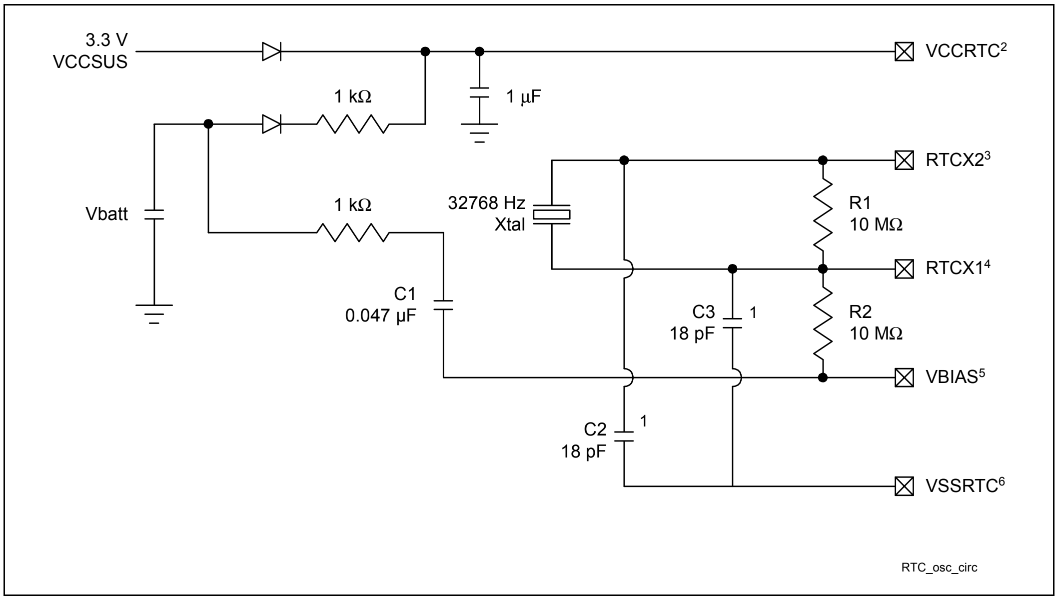
The ICH contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. This internal RTC module provides two key functions: keeping the date and time and storing system data in its RAM when the system is powered down. This section explains the recommended hookup for the RTC circuit for the ICH.

Note: This circuit is not the same as the circuit used for the PIIX4.

10.9.1 RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins.

Figure 61. External Circuitry of RTC Oscillator



NOTES:

1. The exact capacitor value should be based on the crystal vendor's recommendations.
2. VCCRTC: Power for RTC well
3. RTCX2: Crystal input 2 – Connected to the 32.768 kHz crystal
4. RTCX1: Crystal input 1 – Connected to the 32.768 kHz crystal
5. VBIAS: RTC bias voltage – This pin is used to provide a reference voltage. This DC voltage sets a current, which is mirrored through the oscillator and buffer circuitry.
6. VSS: Ground

10.9.2 External Capacitors

To maintain RTC accuracy the external capacitor C1 must be 0.047 µF. The external capacitor values for C2 and C3 should be chosen to provide the manufacturer-specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate will be the RTC.

The following equation can be used to choose the external capacitance values (C2 and C3):

$$\text{Cload} = (\text{C2} * \text{C3}) / (\text{C2} + \text{C3}) + \text{Cparasitic}$$

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain 32.768 kHz.

10.9.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible. Approximately 0.25 inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route any switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean. Use a filter, such as an RC low-pass or a ferrite inductor.

10.9.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system.

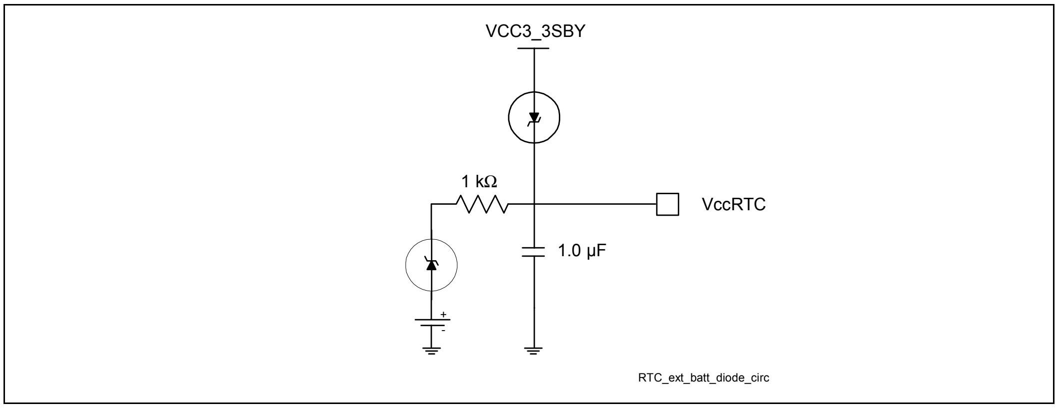
Example batteries are the Duracell* 2032, 2025 or 2016 (or equivalent), which give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

$$170{,}000\ \mu\text{Ah} / 3\ \mu\text{A} = 56{,}666\ \text{h} = 6.4\ \text{years}$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is within the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse-biased when the system power is not available. Figure 62 is an example of a diode circuitry that can be used.

Figure 62. Diode Circuit to Connect RTC External Battery

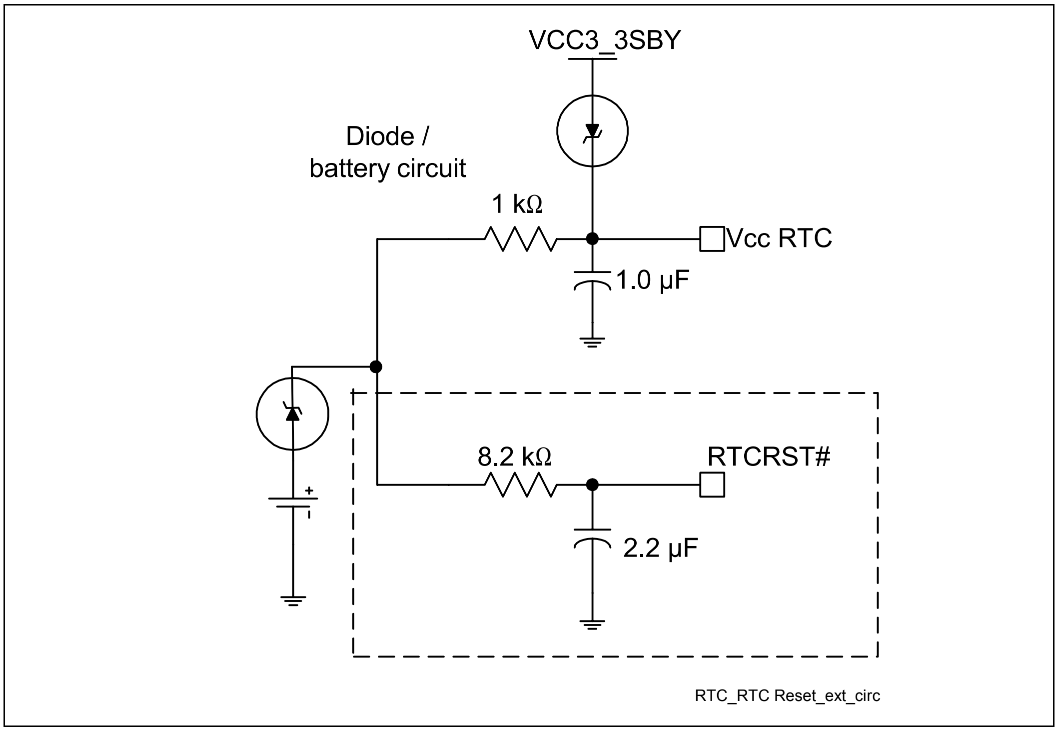


A standby power supply should be used to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

10.9.5 RTC External RTC Reset Circuit

The ICH RTC requires some additional external circuitry. The RTCRST# (RTC Well Test) signal is used to reset the RTC well. The external capacitor (2.2 µF) and the external resistor (8.2 kΩ) between RTCRST# and the RTC battery (Vbat) were selected to create a RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be within the range 10–20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and it remains set until cleared by software. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

Figure 63. RTC Reset External Circuit for the Intel® ICH RTC



This RTC Reset circuit is combined with the diode circuit (Figure 63), which allows the RTC well to be powered by the battery when the system power is not available. Figure 63 shows an example of this circuitry, which is used in conjunction with the external diode circuit.

10.9.6 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 63 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This prevents these nodes from floating in G3, and correspondingly prevents ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

10.9.7 RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should be routed with trace lengths shorter than 1 inch. The shorter, the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimally, there would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

10.9.8 Guidelines to Minimize ESD Events

Guidelines to minimize ESD events that may cause loss of CMOS contents:

- Provide a 1 µF 805 X5R dielectric, monolithic, ceramic capacitor on the VCCRTC pin. This capacitor connection should not be stubbed off the trace run and should be as close as possible to the ICH. If a stub is required, its maximum length should be a few mm. The ground connection should be made through a via to the plane, with no trace between the capacitor pad and the via.
- Place the battery, the 1 kΩ series current limit resistor, and the common-cathode isolation diode very close to the ICH. If this is not possible, place the common-cathode diode and the 1 kΩ resistor as close as possible to the 1 µF capacitor. Do not place these components between the capacitor and the ICH. The battery can be placed remotely from the ICH.
- On boards that have chassis intrusion utilizing inverters powered by the VCCRTC pin, place the inverters as close as possible to the common-cathode diode. If this is not possible, keep the trace run near the center of the board.
- Keep the ICH VCCRTC trace away from the board edge. If this trace must run from opposite ends of the board, keep the trace run towards the board center, away from the board edge where contact could be made by those handling the board.

10.9.9 VBIAS and DC Voltage and Noise Measurements

- Steady-state VBIAS will be a DC voltage of about 0.38 V ± 0.06V.
- VBIAS will be “kicked” when the battery is inserted, to about 0.7–1.0 V, but it will return to its DC value within a few msec.
- Noise on VBIAS must be kept to a minimum (200 mV or less).
- VBIAS is very sensitive and cannot be probed directly. It can be probed through a 0.01 µF capacitor.
- Excessive noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely.
- To minimize the VBIAS noise, it is necessary to implement the routing guidelines described previously as well as the required external RTC circuitry.

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11 Clocking

For an 815EG chipset platform, there are two clock specifications. One is for a 2-DIMM solution, and the other is for a 3-DIMM solution. In both specifications only single-ended clocking is supported. The 815EG chipset platforms using a future 0.13 micron socket 370 processors cannot implement differential clocking.

11.1 2-DIMM Clocking

Table 22 shows the characteristics of the clock generator for a 2-DIMM solution.

Table 22. Intel® CK-815 (2-DIMM) Clocks

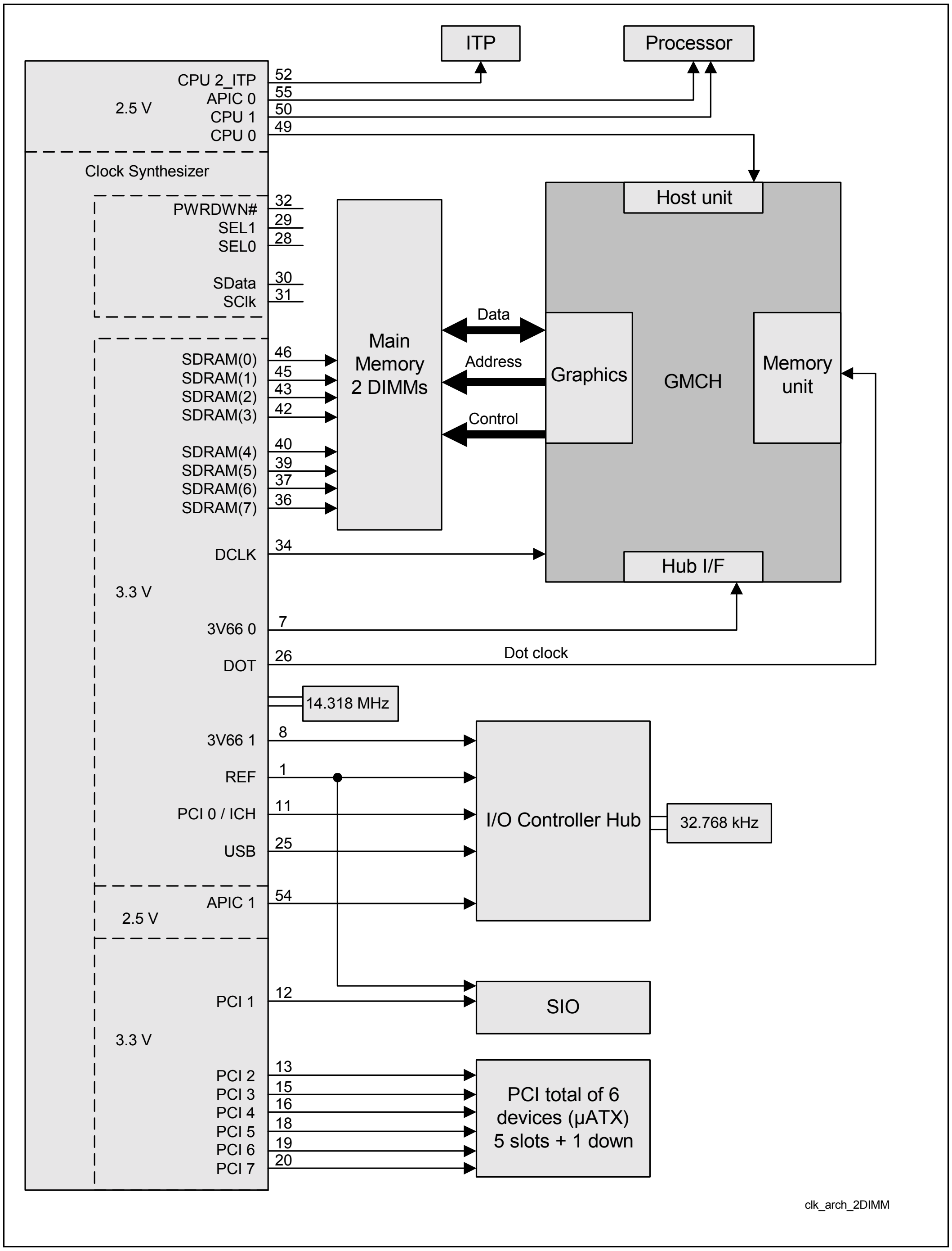
Number	Clock	Frequency
3	processor clocks	66/100/133 MHz
9	SDRAM clocks	100 MHz
7	PCI clocks	33 MHz
2	APIC clocks	16.67/33 MHz
2	48 MHz clocks	48 MHz
3	3 V, 66 MHz clocks	66 MHz
1	REF clock	14.31818 MHz

The following bullets list the features of the CK-815 clock generator in a 2-DIMM solution:

- Nine copies of 100 MHz SDRAM clocks (3.3 V) [SDRAM0…7, DClk]
- Seven copies of PCI clock (33 MHz) (3.3 V)
- Two copies of APIC clock at 33 MHz, synchronous to processor clock (2.5 V)
- One copy of 48 MHz USB clock (3.3 V) (non-SSC) (type 3 buffer)
- One copy of 48 MHz DOT clock (3.3 V) (non-SSC) (see DOT details)
- Three copies of 3 V, 66 MHz clock (3.3 V)
- One copy of REF clock at 14.31818 MHz (3.3 V)
- Ref. 14.31818 MHz xtal oscillator input
- Power-down pin
- Spread-spectrum support
- I^{2}C support for turning off unused clocks
- 56-pin SSOP package

Figure 64 shows the 815G chipset platform clock architecture for a 2-DIMM solution.

Figure 64. Platform Clock Architecture (2 DIMMs)



11.2 3-DIMM Clocking

Table 23 shows the characteristics of the clock generator for a 3-DIMM solution.

Table 23. Intel® CK-815 (3-DIMM) Clocks

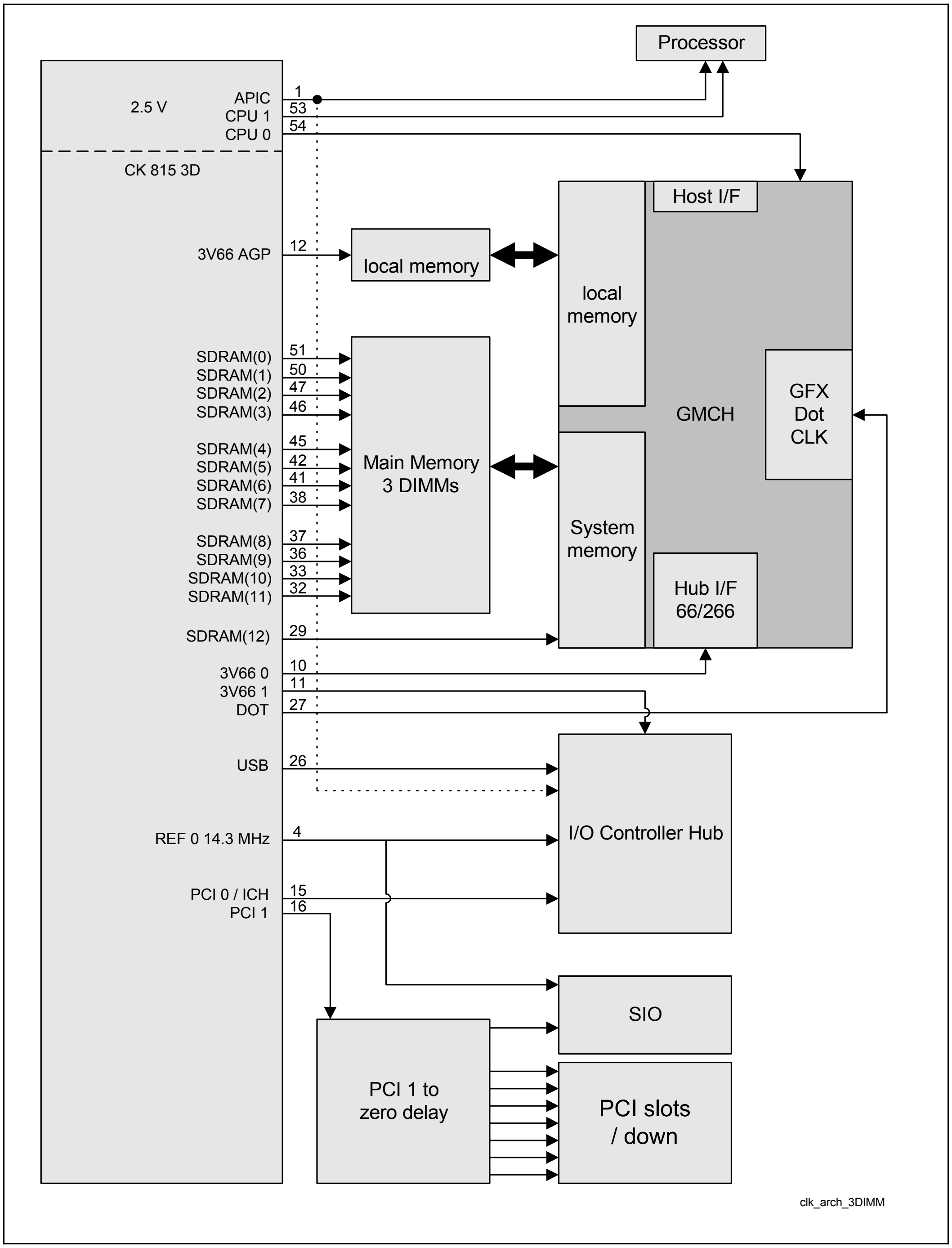
Number	Clock	Frequency
2	processor clocks	66/100/133 MHz
13	SDRAM clocks	100 MHz
2	PCI clocks	33 MHz
1	APIC clocks	33 MHz
2	48 MHz clocks	48 MHz
3	3 V, 66 MHz clocks	66 MHz
1	REF clock	14.31818 MHz

The following bullets list the features of the CK-815 clock generator:

- Thirteen copies of SDRAM clocks
- Two copies of PCI clock
- One copy of APIC clock
- One copy of 48 MHz USB clock (3.3 V) (non-SSC) (type 3 buffer)
- One copy of 48 MHz DOT clock (3.3 V) (non-SSC) (see DOT details)
- Three copies of 3 V, 66 MHz clock (3.3 V)
- One copy of ref. clock @ 14.31818 MHz (3.3 V)
- Ref. 14.31818 MHz xtal oscillator input
- Spread-spectrum support
- I^2C support for turning off unused clocks
- 56-pin SSOP package

Figure 65 shows the 815GE chipset platform clock architecture for a 3-DIMM solution.

Figure 65. Universal Platform Clock Architecture (3 DIMMs)



11.3 Clock Routing Guidelines

This section presents the generic clock routing guidelines for both 2-DIMM and 3-DIMM boards. For 3-DIMM boards, additional analysis must be performed by the motherboard designer to ensure that the clocks generated by the external PCI clock buffer meet the PCI specifications for clock skew at the receiver, when compared with the PCI clock at the ICH.

Figure 66. Clock Routing Topologies

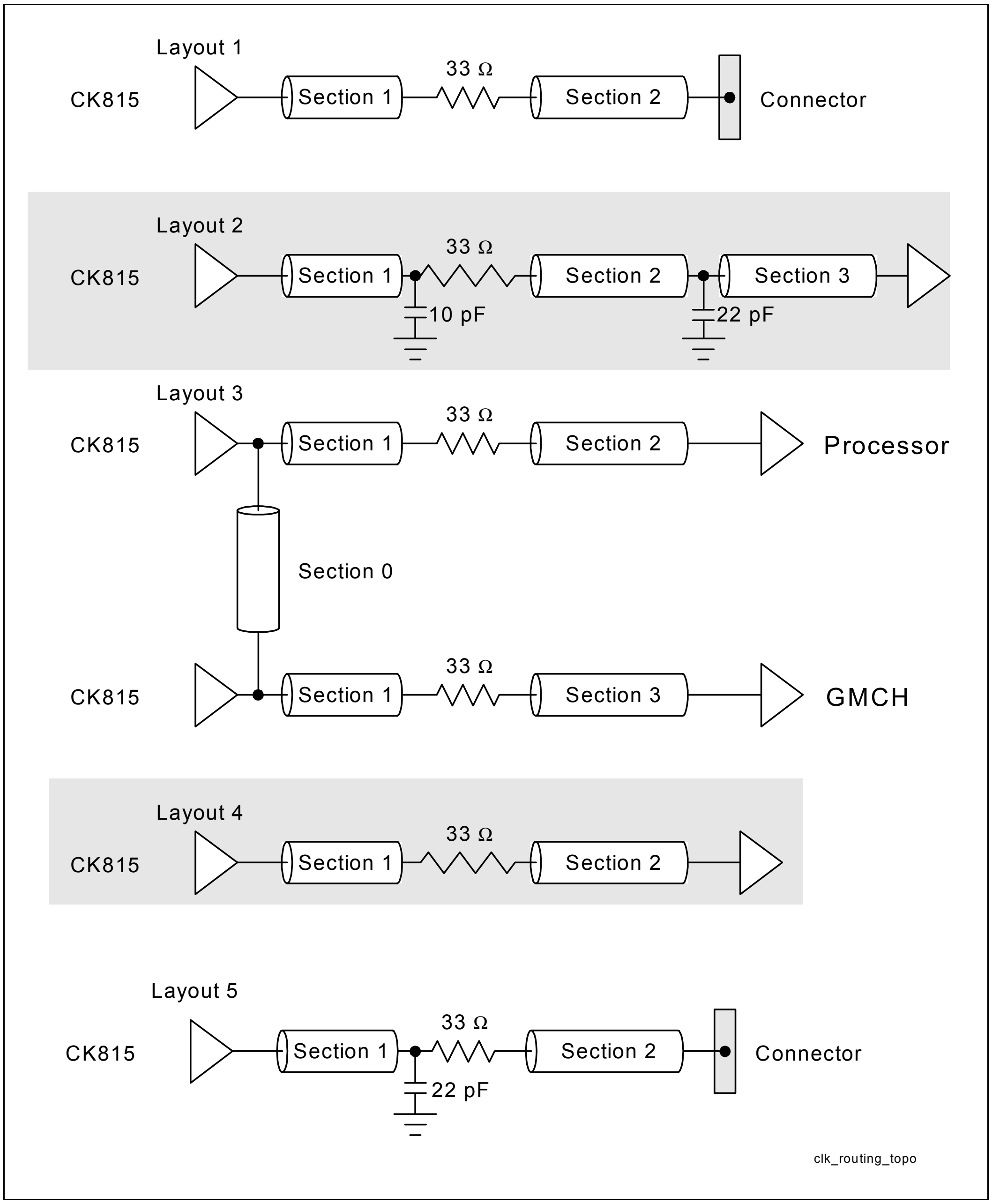


Table 24. Simulated Clock Routing Solution Space

Destination	Topology from Previous Figure	Section 0 Length	Section 1 Length	Section 2 Length	Section 3 Length
SDRAM MCLK	Layout 5	N/A	< 0.5”	A[1]	N/A
GMCH SCLK[3]	Layout 2	N/A	< 0.5”=L1	A + 3.5” – L1	0.5”
Processor BCLK	Layout 3	< 0.1”	< 0.5”	A + 5.2”	A + 8”
GMCH HCLK			<0.5”		
GMCH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH PCICLK	Layout 4	N/A	<0.5”	A + 8”	N/A
AGP CLK	Layout 4	N/A	<0.5”	A + 3” to A + 4”	N/A
PCI down[2]	Layout 4	N/A	<0.5”	A + 8.5” to A + 14”	N/A
PCI slot[2]	Layout 1	N/A	<0.5”	A + 5” to A + 11”	

NOTES:

1. Length “A” has been simulated up to 6 inches. The length must be matched between SDRAM MCLK lines by ±100 mils.
2. All PCI clocks must be within 6 inches of the ICH PCICLK route length. Routing on PCI add-in cards must be included in this length. In the presented solution space, the ICH PCICLK was considered to be the shortest in the 6 inches trace routing range, and other clocks were adjusted from there. The system designer may choose to alter the relationship of PCI device and slot clocks, as long as all PCI clock lengths are within 6 inches. Note that the ICH PCICLK length is fixed to meet the skew requirements of the ICH PCICLK to ICH HUBCLK.
3. 22 pF Load capacitor should be placed 0.5 inch from GMCH Pin.

General Clock Layout Guidelines

- All clocks should be routed 5 mils wide with 15-mil spacing to any other signals.
- It is recommended to place capacitor sites within 0.5 inch of the receiver of all clocks. They are useful in system debug and AC tuning.
- Series resistor for clock guidelines: 22 Ω for GMCH SCLK and SDRAM clocks. All other clocks use 33 Ω.
- Each DIMM clock should be matched within ±10 mils.

11.4 Clock Decoupling

Several general layout guidelines should be followed when laying out the power planes for the CK-815 clock generator.

- Isolate the power plane to each clock group.
- Place local decoupling as close as possible to power pins and connect with short, wide traces and copper.
- Connect pins to the appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14-mil finished hole with a 24-mil to 26-mil path. An example power via is an 18-mil finished hole with a 33-mil to 38-mil path. For large decoupling or power planes with large current transients, a larger power via is recommended

11.5 Clock Driver Frequency Strapping

A CK-815-compliant clock driver device uses two of its pins to determine whether processor clock outputs should run at 133 MHz, 100 MHz, or 66 MHz. The pin names are SEL0 and REF0. In addition, a third strapping pin is defined (SEL1) that must be pulled high for normal clock driver operation. Refer to the appropriate CK-815 clock driver specification for detailed strap timings and the logic encoding of straps.

SEL0 and REF0 are driven by either the processor, which depends on the processor populated in the 370-pin socket, or pull-up resistors on the motherboard. While SEL0 is a pure input to a CK-815-compliant clock driver, REF0 is also the 14 MHz output that drives the ICH and other devices on the platform. In addition to sampling BSEL[1:0] at reset, CK-815-compliant clock drivers are configured by the BIOS via a two-wire interface to drive SDRAM clock outputs at either 100 MHz (default) or 133 MHz (if all system requirements are met).

11.6 Clock Skew Assumptions

The clock skew assumptions in the following table are used in the system clock simulations.

Table 25. Simulated Clock Skew Assumptions

Skew Relationships	Target	Tolerance (±)	Notes
HCLK @ GMCH to HCLK @ processor	0 ns	200 ps	• Assumes ganged clock outputs will allow maximum of 50 ps skew
HCLK @ GMCH to SCLK @ GMCH	0 ns	600 ps	• 500 ps pin-to-pin skew • 100 ps board/package skew
SCLK @ GMCH to SCLK @ SDRAM	0 ns	630 ps	• 250 ps pin-to-pin skew • 380 ps board + DIMM variation
HLCLK @ GMCH to SCLK @ GMCH	0 ns	900 ps	• 500 ps pin-to-pin skew • 400 ps board/package skew
HLCLK @ GMCH to HCLK @ GMCH	0 ns	700 ps	• 500 ps pin-to-pin skew • 200 ps board/package skew
HLCLK @ GMCH to HLCLK @ ICH	0 ns	375 ps	• 175 ps pin-to-pin skew • 200 ps board/package skew
HLCLK @ ICH to PCICLK @ ICH	0 ns	900 ps	• 500 ps pin-to-pin skew • 400 ps board/package skew
PCICLK @ ICH to PCICLK @ other PCI devices	0 ns	2.0 ns window	• 500 ps pin-to-pin skew • 1.5 ns board/add-in skew
HLCLK @ GMCH to AGPCLK @ connector			• Total electrical length of AGP connector + add-in card is 750 ps (according to AGP2.0 specification and AGP design guide 1.0). • Motherboard clock routing must account for this additional electrical length. Therefore, AGPCLK routed to the connector must be shorter than HLCLK to the GMCH, to account for this additional 750 ps.

11.7 Intel® CK-815 Power Gating On Wake Events

For systems providing functionality with future 0.13 micron socket 370 processors, special handling of wake events is required. When a wake event is triggered, the GMCH and the CK-815 must not sample BSEL[1:0] until the signal VTTPWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the CK-815-compliant clock driver until VTTPWRGD12 is asserted.
2. Clocks to the ICH stabilize before the power supply asserts PWROK to the ICH. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus, it is necessary to gate PWROK to the ICH from the power supply while the CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.
3. ICH takes the GMCH out of reset.
4. GMCH samples BSEL[1:0]. CK-815 will have sampled BSEL[1:0] much earlier.

Refer to Chapter 4 for full implementation details.

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12 Power Delivery

12.1 Power Delivery Guidelines

Table 26 provides definitions for power delivery terms used in this chapter.

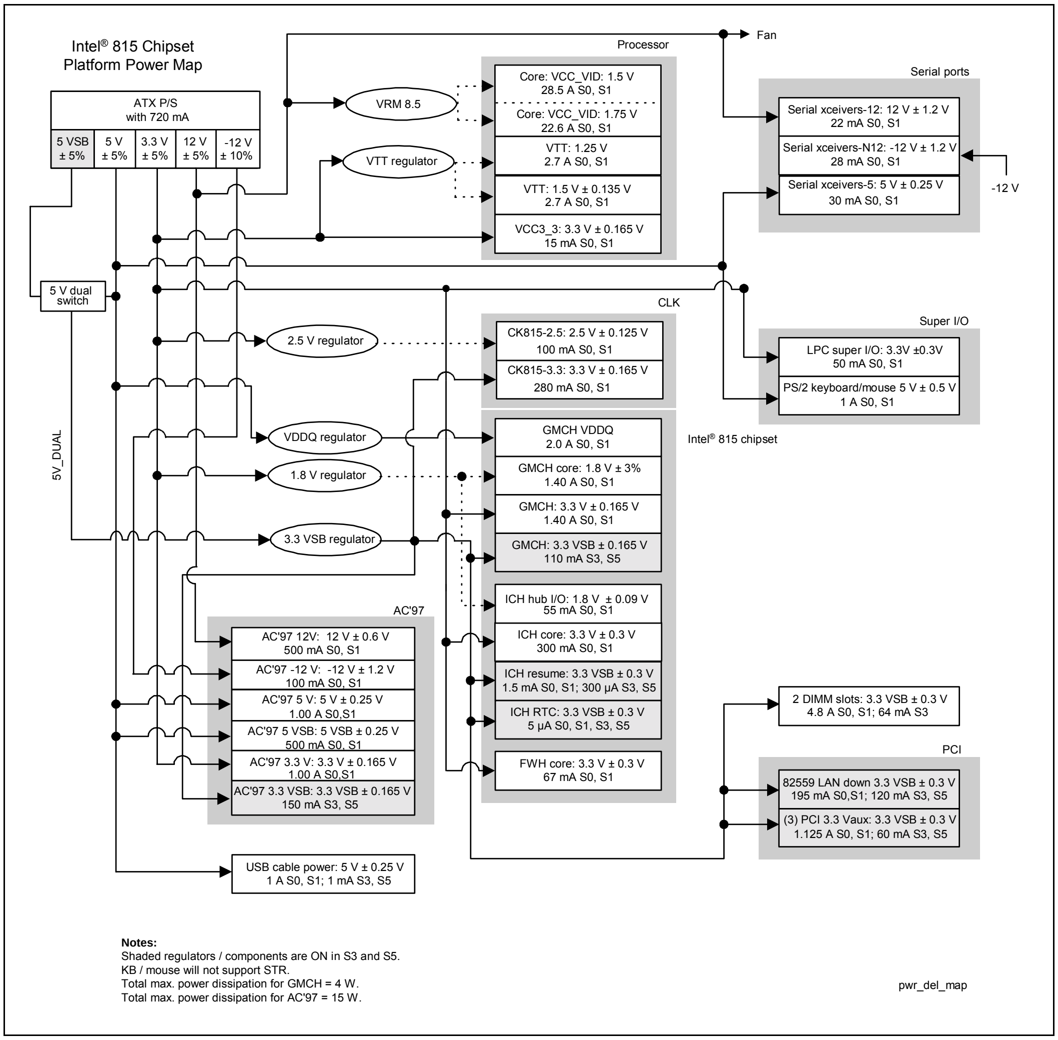
Table 26. Power Delivery Terminology

Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered. This state is used in the Customer Reference Board (CRB) to satisfy the S3 ACPI power management state.
Full-power operation	During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (CPU stop-grant state) state.
Suspend operation	During *suspend* operation, power is removed from some components on the motherboard. The CRB supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Power rails	An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, 5VSB. In addition to these power rails, several other power rails are created with voltage regulators on the CRB.
Core power rail	A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed *directly* from the ATX power supply are: ±5V, ±12V and +3.3V.
Standby power rail	A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is: 5VSB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator (on the CRB, 3.3VSB is derived from 5V_DUAL).
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

Figure 67 shows a power delivery architecture example for a system based on the 815G chipset platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the *suspend-to-RAM* (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH resume well, PCI wake devices (via 3.3 Vaux), AC ’97, and optionally USB (USB can be powered only if sufficient standby power is available.). To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *full-power*. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions in this Design Guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 67. Power Delivery Map



Notes:
Shaded regulators / components are ON in S3 and S5.
KB / mouse will not support STR.
Total max. power dissipation for GMCH = 4 W.
Total max. power dissipation for AC'97 = 15 W.

In addition to the power planes provided by the ATX power supply, an *instantly available* 815G chipset platform (using *Suspend-to-RAM)* requires six power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the CRB will have a *5V Dual Switch*.

12.1.1 5V Dual Switch

This switch will power the *5V Dual plane* from the 5V core ATX supply during *full-power* operation. During *Suspend-to-RAM*, the *5V Dual plane* will be powered from the 5 V Standby power supply.

Note: The voltage on the 5V Dual plane **is not 5 V!** There is a resistive drop through the *5V Dual Switch* that must be considered. Therefore, NO COMPONENTS should be connected directly to the 5V Dual plane. On the CRB, the only devices connected to the 5V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in an 815G chipset platform that does not support Suspend-to-RAM (STR).

12.1.2 VTT

This power plane is used to power the AGTL/AGTL+ termination resistors. Refer to the latest revisions of:

- Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) Datasheets

Note: This regulator is required in ALL designs.

12.1.3 1.85 V

The 1.85 V plane powers the GMCH core and the ICH hub interface I/O buffers. This power plane has a total power requirement of approximately 1.7A. The 1.85 V plane should be decoupled with a 0.1 µF and a 0.01 µF chip capacitor at each corner of the GMCH and with a single 1 µF and 0.1 µF capacitor at the ICH.

Note: This regulator is required in ALL designs.

12.1.4 VDDQ

The VDDQ plane is used to power the GMCH internal graphics component interface.

NOTE: AGP functionality has been removed from the 82815G GMCH. However, VDDQ voltage must be maintained in 82815G designs even though the AGP capability is removed.

For the designer developing an 82815G motherboard, there is no distinction between VCC and VDDQ, as both are tied to the 3.3 V power plane on the motherboard.

For the consideration of component long-term reliability, the following power sequence is strongly recommended while the GMCH's internal graphics interface is running at 3.3 V. The power sequence recommendations are:

- During the power-up sequence, the 1.85 V must ramp up to 1.0 V **before** 3.3 V ramps up to 2.2 V.
- During the power-down sequence, the 1.85 V **cannot** ramp below 1.0 V **before** 3.3 V ramps below 2.2 V.

The same power sequence recommendation also applies to the entrance and exit of S3 state, since the GMCH power is compete off during the S3 state.

Refer to Section 12.5.1 for more information on the power ramp sequence requirement between 3.3 V and 1.85 V. System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply. For further details on the voltage sequencing requirements, refer to the *Intel® 815 Chipset Family: 82815G/82815EG Graphics and Memory Controller Hub (GMCH) For Use With Universal Socket 370* Datasheet.

Note: This regulator is required in ALL designs (unless the design does not support 1.5 V AGP, and therefore does not support 4X AGP).

12.1.5 3.3VSB

The 3.3VSB plane powers the I/O buffers in the resume well of the ICH and the PCI 3.3Vaux suspend power pins. The 3.3Vaux requirement state that during suspend, the system must deliver 375 mA to each *wake-enabled* card and 20 mA to each *non wake-enabled* card. During *full-power* operation, the system must be able to supply 375 mA to **each** card. Therefore, the total current requirement is:

- *Full-power Operation:* 375 mA * number of PCI slots
- *Suspend Operation:* 375+20 mA * (number of PCI slots – 1)

In addition to the PCI 3.3Vaux, the ICH suspend well power requirements must be considered as shown in Figure 67.

Note: This regulator is required in **all** designs.

12.1.6 1.85VSB

The 1.85VSB plane powers the logic to the resume well of the ICH. This should not be used for VCMOS.

12.2 Thermal Design Power

Thermal Design Power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP for the GMCH component is 5.1 W.

12.2.1 Pull-Up and Pull-Down Resistor Values

The pull-up and pull-down values are system dependent. The appropriate value for a system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, the input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high-voltage/low-voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be performed to determine the minimum/maximum values usable on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, and other considerations.

A simplistic DC calculation for a pull-up value is:

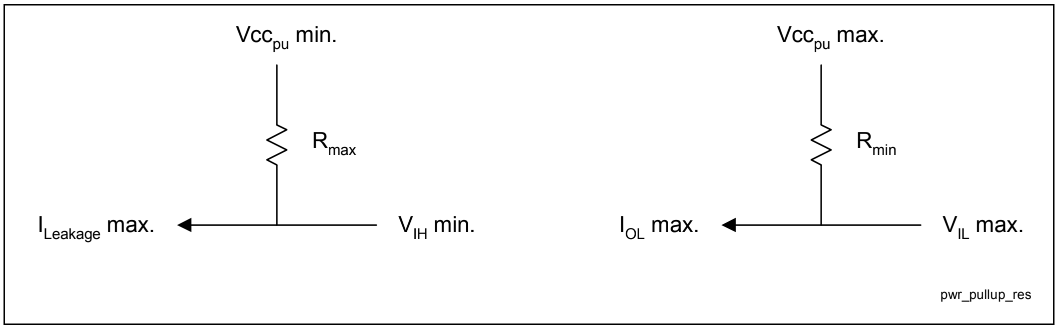
$$R_{MAX} = (VCC_{PU}\ MIN - V_{IH}\ MIN) / I_{LEAKAGE}\ MAX$$

$$R_{MIN} = (VCC_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$$

Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} also is determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including the input capacitance of the devices to be driven, the output capacitance of the driver, and the line capacitance. This calculation yields the largest pull-up resistor allowable to meet the rise time t.

$$R_{MAX} = -t / (C * \ln(1-(V_{IH}\ MIN / VCC_{PU}\ MIN)))$$

Figure 68. Pull-Up Resistor Example



12.3 ATX Power Supply PWRGOOD Requirements

The PWROK signal must be glitch free for proper power management operation. The ICH sets the PWROK_FLR bit (ICH GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at offset A2h). If this bit is set upon resume from S3 power-down, the system will reboot and control of the system will not be given to the program running when entering the S3 state. System designers should insure that PWROK signal designs are glitch free.

12.4 Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH integrates 16 ms debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH to detect power failure.
- It is recommended that the ATXPWROK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity. It should not be connected directly to logic on the board.
- PWROK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, while making sure that the input to the ICH is at the 3 V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1-ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- It is recommended that 3.3 V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3 V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V, using a 330 Ω resistor.
- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.
- SLP_S3# from the ICH must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

12.4.1 Power Button Implementation

The following items should be considered when implementing a power management model for a desktop system. The power states are as follows:

S1 – Stop Grant – (processor context not lost)

S3 - STR (Suspend to RAM)

S4 - STD (Suspend to Disk)

S5 - Soft-off

1. Wake: Pressing the power button wakes the computer from S1–S5.
2. Sleep: Pressing the power button signals software/firmware in the following manner:
    a. If SCI is enabled, the power button will generate an SCI to the operating system (OS).
        1. The OS will implement the power button policy to allow orderly shutdowns.
        2. Do not override this with additional hardware.
    b. If SCI is not enabled:
        1. Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
        2. Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
        3. Always install an SMI handler for the power button that operates until ACPI is enabled.
3. Emergency Override: Pressing the power button for 4 seconds goes directly to S5.
    a. This is only to be used in EMERGENCIES when system is not responding.
    b. This will cause the user data to be lost in most cases.
4. Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off. This violates ACPI.
5. To be compliant with the latest PC9x specification, machines must appear to the user to be off when in the S1–S4 sleeping states. This includes:
    a. All lights, except a power state light, must be off.
    b. The system must be inaudible: silent or stopped fan, drives off.

Note: Contact Microsoft for the latest information concerning PC9x or PC200x and Microsoft Logo programs.

12.5 1.85 V/3.3 V Power Sequencing

This section shows the timings among various signals during different power state transitions.

Figure 69. G3-S0 Transition

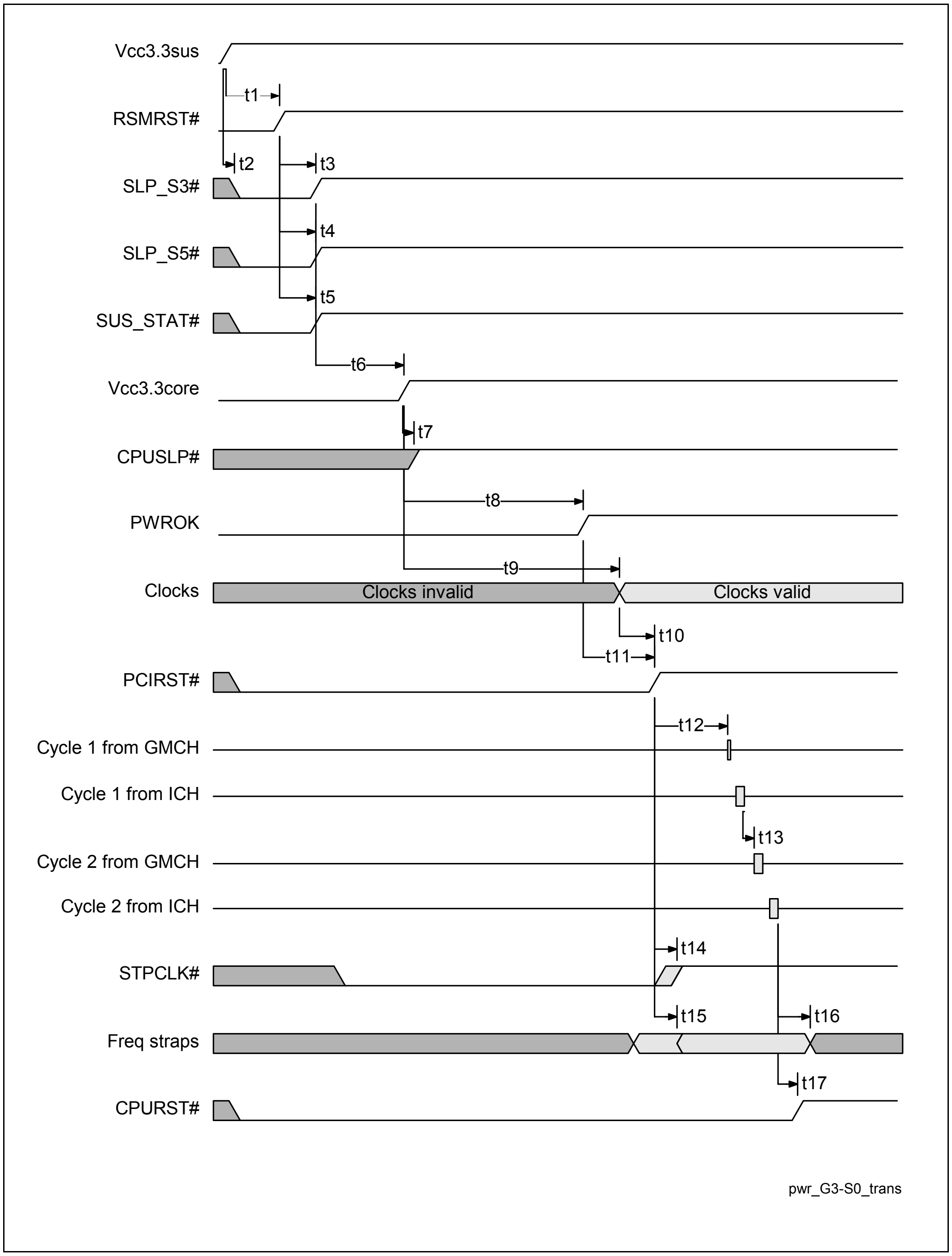


Figure 70. S0-S3-S0 Transition

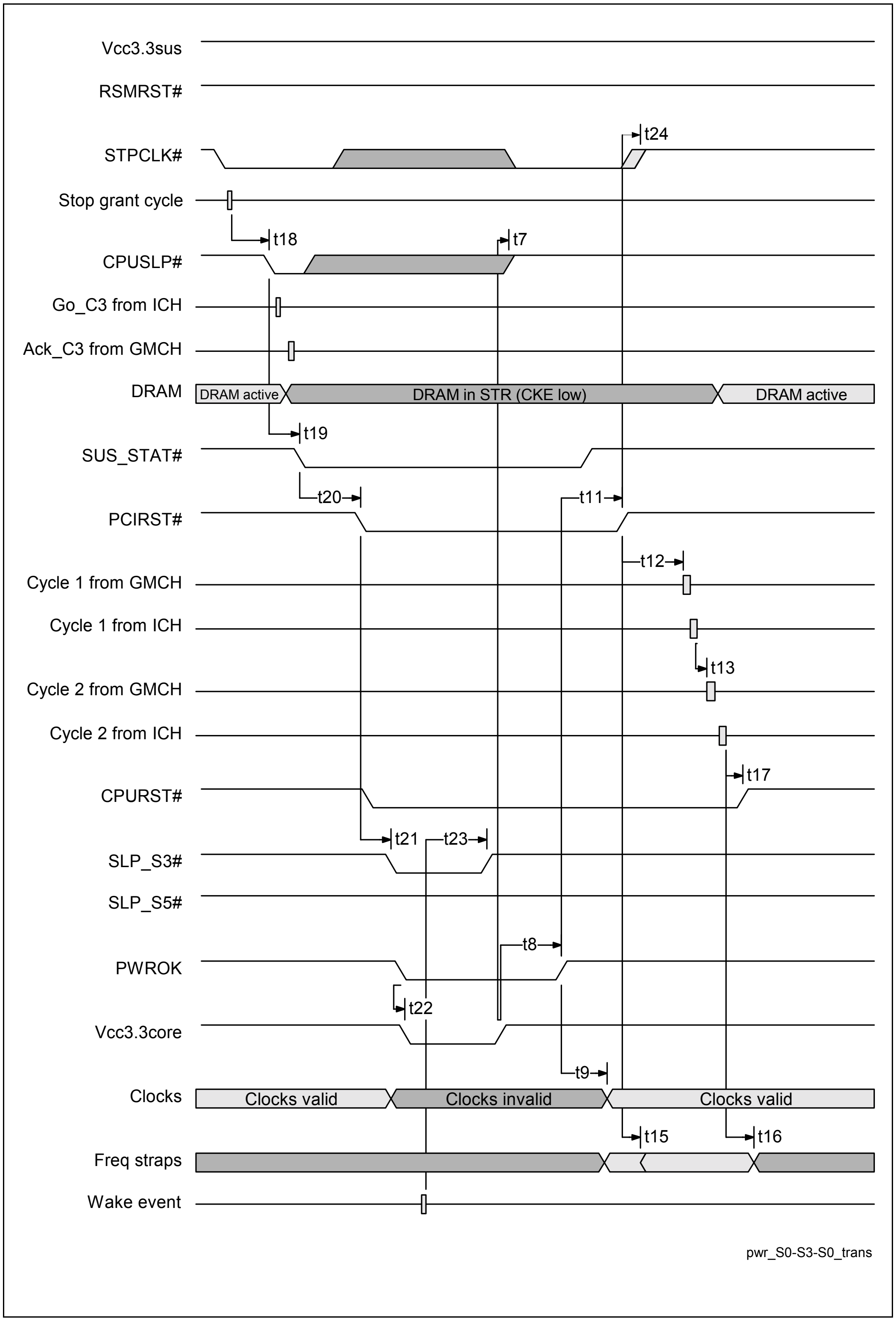


Figure 71. S0-S5-S0 Transition

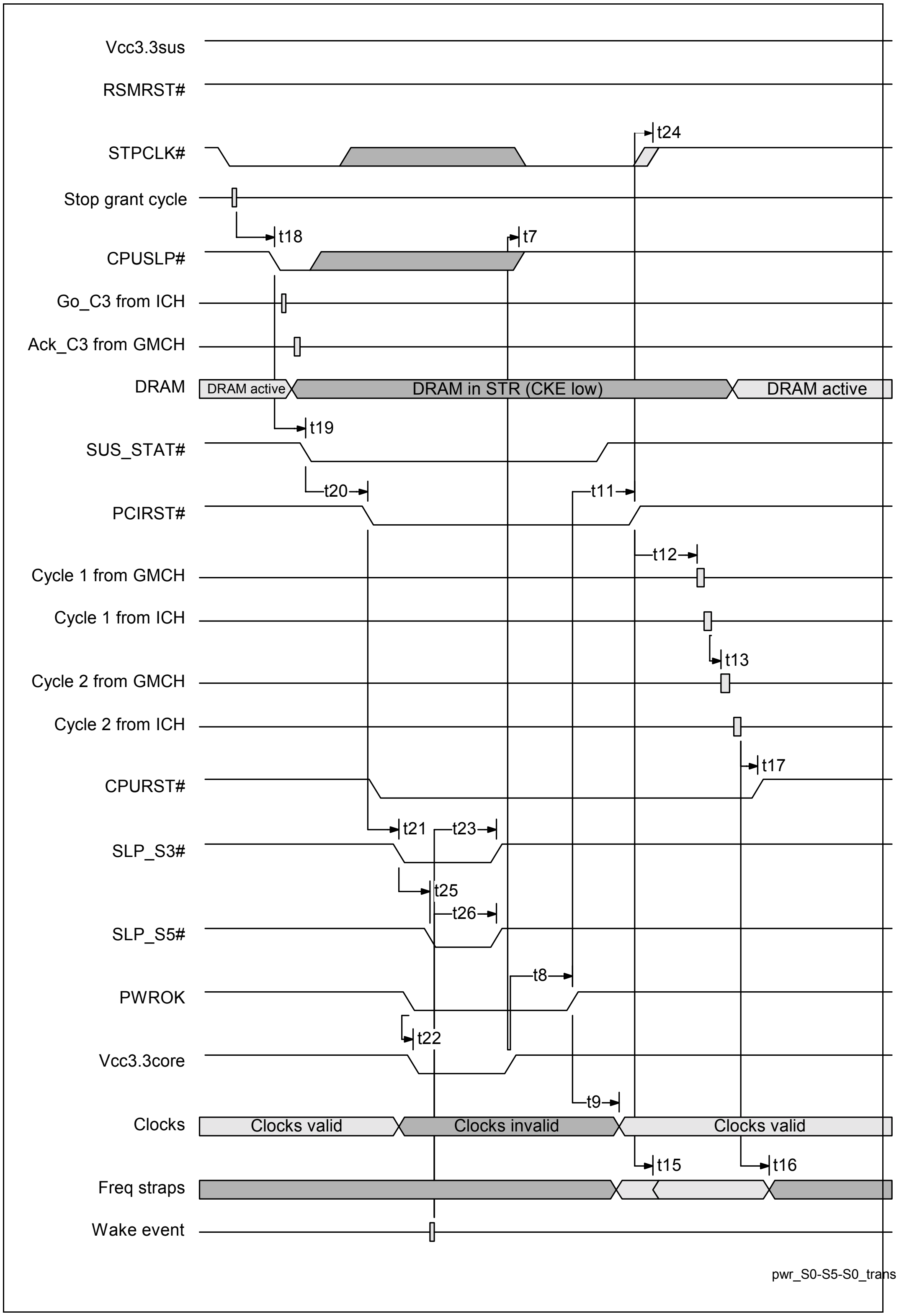


Table 27. Power Sequencing Timing Definitions

Symbol	Parameter	Min.	Max.	Units
t1	VccSUS Good to RSMRST# inactive	1	25	ms
t2	VccSUS Good to SLP_S3#, SLP_S5#, and PCIRST# active		50	Ns
t3	RSMRST# inactive to SLP_S3# inactive	1	4	RTC clocks
t4	RSMRST# inactive to SLP_S5# inactive	1	4	RTC clocks
t5	RSMRST# inactive to SUS_STAT# inactive	1	4	RTC clocks
t6	SLP_S3#, SLP_S5#, SUS_STAT# inactive to Vcc3.3core good	*	*	
t7	Vcc3.3core good to CPUSLP# inactive		50	ns
t8	Vcc3.3core good to PWROK active	*	*	
t9	Vcc3.3core good to clocks valid	*	*	
t10	Clocks valid to PCIRST# inactive	500		µs
t11	PWROK active to PCIRST# inactive	0.9	1.1	ms
t12	PCIRST# inactive to Cycle 1 from GMCH		1	ms
t13	Cycle 1 from ICH to Cycle 2 from GMCH		60	ns
t14	PCIRST# inactive to STPCLK deassertion	1	4	PCI clocks
t15	PCIRST# to frequency straps valid	-4	4	PCI clocks
t16	Cycle 2 from ICH to frequency straps invalid		180	ns
t17	Cycle 2 from ICH to CPURST# inactive		110	ns
t18	Stop Grant Cycle to CPUSLP# active		8	PCI clocks
t19	CPUSLP# active to SUS_STAT# active		1	RTC clock
t20	SUS_STAT# active to PCIRST# active	2	3	RTC clocks
t21	PCIRST# active to SLP_S3# active	1	2	RTC clocks
t22	PWROK inactive to Vcc3.3core not good	20		ns
t23	Wake event to SLP_S3# inactive	2	3	RTC clocks
t24	PCIRST# inactive to STPCLK# inactive	1	4	PCI clocks
t25	SLP_S3# active to SLP_S5# active	1	2	RTC clocks
t26	SLP_S5# inactive to SLP_S3# inactive	2	3	RTC clocks

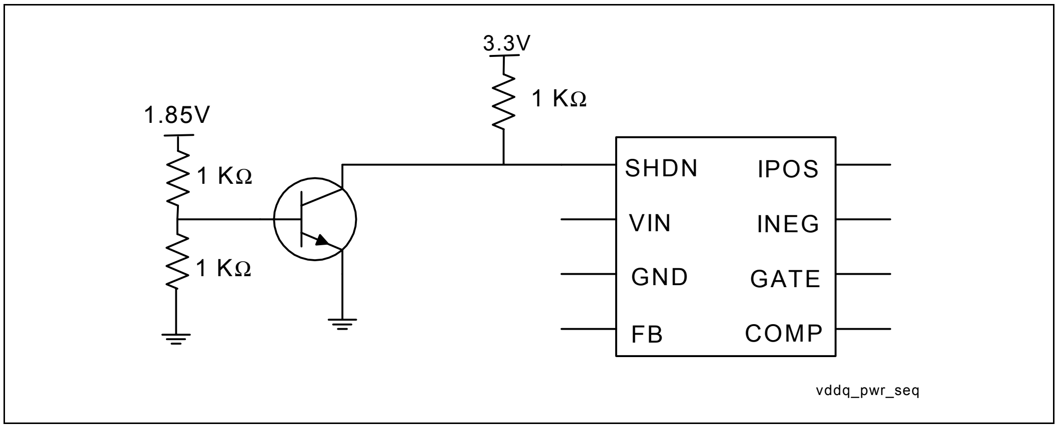
12.5.1 VDDQ/VCC1_85 Power Sequencing

For the consideration of long term component reliability, the following power sequence is strongly recommended while the AGP interface of the GMCH is running at 3.3 V. If the AGP interface is running at 1.5 V, the following power sequence recommendation is no longer applicable. The power sequence recommendation is:

- During the power-up sequence, the 1.85 V **must** ramp up to 1.0 V **before** 3.3 V ramps above 2.2V
- During the power-down sequence, the 1.85 V **cannot** ramp below 1.0 V **before** 3.3 V ramps below 2.2V
- The same power sequence recommendation also applies to the entrance and exit of S3 state

System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply. An example VDDQ power sequencing circuit is shown in Figure 72.

Figure 72. VDDQ Power Sequencing Circuit



12.5.2 1.85 V/3.3V Power Sequencing

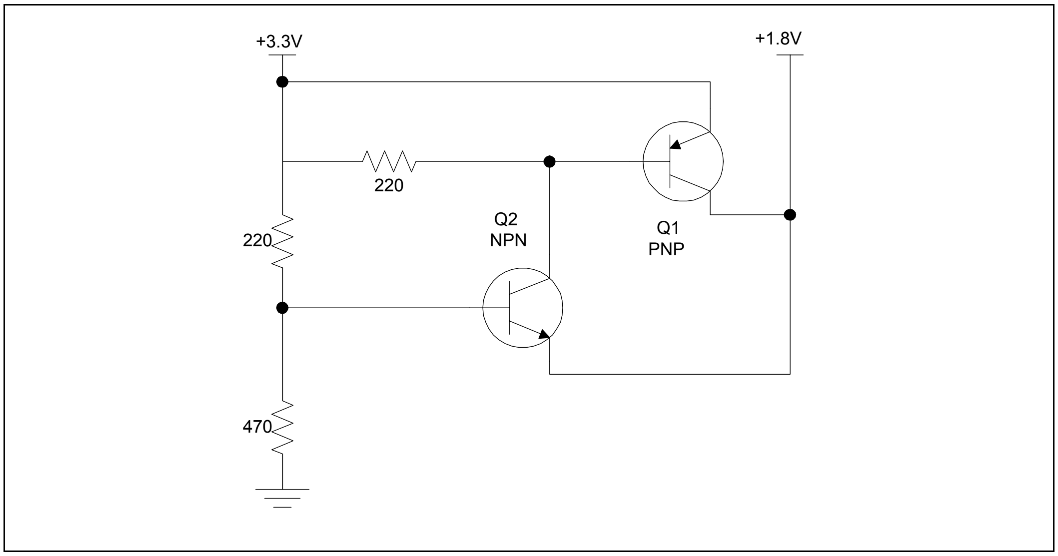
The ICH has two pairs of associated 1.85 V and 3.3 V supplies. These are {Vcc1_8, Vcc3_3} and {VccSus1_8, VccSus3_3}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.85 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.85 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violation of the 2V Rule, is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.85 V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.85 V logic is powered up. Some signals that are defined as “Input-only” actually have output buffers that are normally disabled, and the ICH may unexpectedly drive these signals if the 3.3 V supply is active while the 1.85 V supply is not.

Figure 73 shows an example power-on sequencing circuit that ensures the 2V Rule is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.85 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.85 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.85 V plane, current will not flow from the 3.3 V supply into 1.85 V plane when the 1.85 V plane reaches 1.85 V.

Figure 73. Example 1.85 V/3.3 V Power Sequencing Circuit



When analyzing systems that may be “marginally compliant” to the 2V Rule, pay close attention to the behavior of the ICH’s RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells

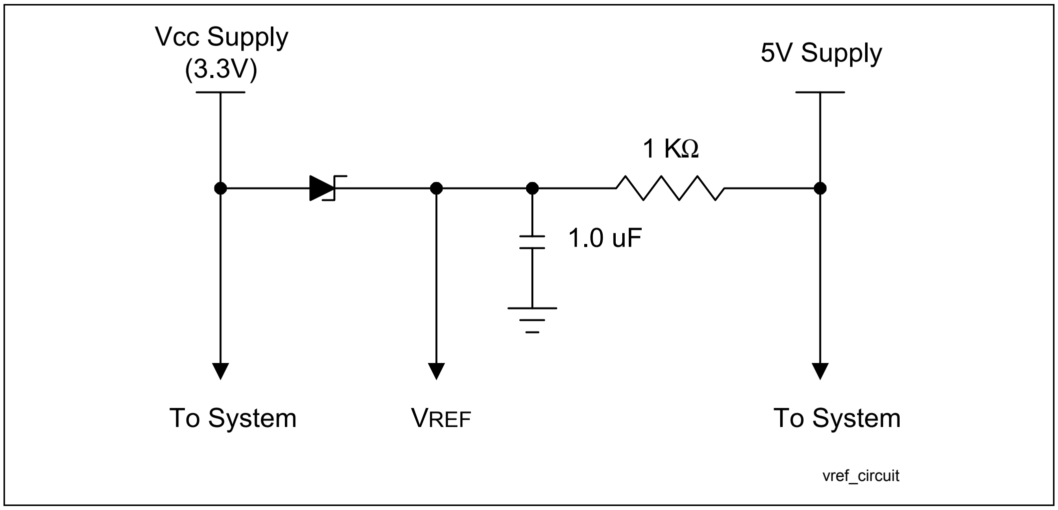
If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

12.5.3 3.3V/V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH. V5REF must be powered up before or simultaneously to VCC3_3. It must also power down after or simultaneous to VCC3_3. The rule must be followed to ensure the safety of the ICH. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 74 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VCCSus3_3 rail is derived from the VCCSus5 and therefore, the VCCSus3_3 rail will always come up after the VCCSus5 rail. As a result, V5REF_Sus will always be powered up before VCCSus3_3. In platforms that do not derive the VCCSus3_3 rail from the VCCSus5 rail, this rule must be comprehended in the platform design. As an additional consideration, during suspend the only signals that are 5 V tolerant are USBOC. If these signals are not needed during suspend, V5REF_Sus can be hooked to the VCCSus3_3 rail.

Figure 74. 3.3V/V5REF Sequencing Circuitry



13 System Design Checklist

13.1 Design Review Checklist

Introduction

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an 815G chipset platform for use with the universal socket 370. This is not a complete list and does not guarantee that a design will function properly. For items other than those in the following text, refer to the latest revision of the design guide for more-detailed instructions regarding motherboard design.

Design Checklist Summary

The following set of tables provides design considerations for the various portions of a design. Each table describes one of those portions and is titled accordingly. Contact your Intel Field Representative in the event of questions or issues regarding the interpretation of the information in these tables.

13.2 Processor Checklist

13.2.1 GTL/AGTL Checklist

Checklist Items	Recommendations
A[35:3]#	• Connect A[31:3]# to GMCH. Leave A[35:32]# as No Connect (not supported by chipset).
BNR#, BPRI#, DBSY#, DEFER#, DRDY#, D[63:0]#, HIT#, HITM#, LOCK#, REQ[4:0]#, RS[2:0]#, TRDY#	• Connect to GMCH.
ADS#	• Resistor site for 56 Ω pull-up to VTT placed within 150 mils of GMCH for debug purpose. Connect to GMCH.
BREQ[0]# (BR0#)	• 33 Ω pull-down resistor to ground
RESET# (AH4)	• Terminate to VTT through 86 Ω resistor, decoupled through 22 Ω resistor in series with 10 pF capacitor to ground. Connect to GMCH. For ITP, also connect to ITP pin 2 (RESET#) with 240 Ω series resistor.
RESET2# (X4)	• 1 kΩ series resistor to RESET#.

13.2.2 CMOS Checklist

Checklist Items	Recommendations
IERR#	• 150 Ω pull-up resistor to VCC_{CMOS} if tied to custom logic, or leave as No Connect (not used by chipset)
PREQ#	• 200–300 Ω pull-up resistor to VCC_{CMOS} / Connect to ITP or else leave as No Connect.
THERMTRIP#	• See Section 5.3.1.
A20M#, IGNNE#, INIT#, INTR, NMI, SLP#, SMI#, STPCLK#	• 150 Ω pull-up to VCMOS / Connect to ICH
FERR#	• Requires 150 Ω pull-up to VCC_{CMOS}/Connect to ICH.
FLUSH#	• Requires 150 Ω pull-up to $VCC_{CMOS.}$ (Not used by chipset.)
PWRGOOD	• 330 Ω pull-up to VCC2_5 /1.8 kΩ pull-down resistor to ground /Connect to POWERGOOD logic.

13.2.3 TAP Checklist for 370-Pin Socket Processors

Checklist Items	Recommendations
TCK	• 39 Ω pull-down resistor to ground / Connect to ITP.
TMS	• 39Ω pull-up resistor to VCMOS / Connect to ITP
TDI	• 200–330 Ω pull-up resistor to VCMOS / Connect to ITP.
TDO	• 150 Ω pull-up resistor to VCMOS / Connect to ITP.
TRST#	• 500-680 Ω pull-down resistor to ground / Connect to ITP.
PRDY#	• Pull-up resistor that matches GTL characteristic impedance to VTT / 240 Ω series resistor to ITP.

NOTE: Resistors need to be placed within 1 inch of the TAP connector.

13.2.4 Miscellaneous Checklist for 370-Pin Socket Processors

Checklist Items	Recommendations
BCLK	• Connect to clock generator. / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the GMCH and processor.
BSEL0	• **Case 1 (66/100/133 MHz support):** 1 kΩ pull-up resistor to 3.3 V. Connect to Intel® CK-815 SEL0 input. Connect to GMCH LMD29 pin via 10 kΩ **series resistor.** • **Case 2 (100/133 MHz support):** 1 kΩ pull-up resistor to 3.3 V. Connect to PWRGOOD logic such that a logic Low on BSEL0 negates PWRGOOD.
BSEL1	• 1 kΩ pull-up resistor to 3.3 V. Connect to CK-815 REF pin via 10 kΩ series resistor. Connect to GMCH LMD13 pin via 10 kΩ series resistor.

Checklist Items	Recommendations
CLKREF	• Connect to divider on VCC2.5 or VCC3.3 to create 1.25 V reference with a 4.7 µF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. Do not use VTT as source voltage for this reference!
CPUPRES#	• Tie to ground. Leave as No Connect or connect to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1 kΩ to 10 kΩ pull-up resistor to VCC_{CMOS}.
DYN_OE	• 1 kΩ pull-up resistor to VTT.
PICCLK	• See Section 10.5.
PICD[1:0]	• 150 Ω pull-up resistor to VCC_{CMOS}/Connect to ICH.
PLL1, PLL2	• Low-pass filter on VCC_{CORE} provided on motherboard. Typically a 4.7 µH inductor in series with VCC_{CORE} is connected to PLL1, and then through a series 33 µF capacitor to PLL2.
RTTCTRL[5] (S35)	• 56 Ω ± 1% pull-down resistor to ground.
SLEWCTRL (E27)	• 110 Ω ± 1% pull-down resistor to ground.
STPCLK# (AG35)	• Connect to ICH.
THERMDN, THERMDP	• No Connect if not used. Otherwise, connect to thermal sensor using vendor guidelines.
VCC2.5	• No connect for Intel® Pentium® III processors
GTL_REF/VCMOS_REF (AK22)	• Connect to a 1.0 V voltage divider derived from VCC_{CMOS}. See Section 4.2.7.
VCC_{CORE}	• 16 ea. (minimum) 4.7 µF in 1206 package all placed within the PGA370 socket cavity. • 8 ea. (minimum) 1 µF in 0612 package placed in the PGA370 socket cavity.
VID[25mV, 3:0]	• Connect to on-board VR or VRM. 25mV should connect to VID25mV. For on-board VR, 10 kΩ pull-up resistor to power solution-compatible voltage is required (usually pulled up to input voltage of the VR). Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.
VTTPWRGD	• Pull-up to VTT through 1 kΩ resistor and connect to VTTPWRGD circuitry. See Section 4.2.6.
VREF [6:0]	• Connect to VREF voltage divider made up of 75 Ω and 150 Ω 1% resistors connected to VTT. Processor VREF must be able to be separate from chipset VREF. • Decoupling Guidelines: —4 ea. (minimum) 0.1 µF in 0603 package placed within 500 mils of VREF pins
VTT	• Connect AH20, AK16, AL13, AL21, AN11, AN15, G35, G37, AD36, AB36, X34, AA33, AA35, AN21, E23, S33, S37, U35, and U37 to VRM 8.5-compliant regulator. Provide high- and low-frequency decoupling. • Decoupling Guidelines: —20 ea (minimum) 0.1 µF in 0603 package placed as near the VTT processor pins as possible. —4 ea (minimum) 0.47 µF in 0612 package

Checklist Items	Recommendations
NO CONNECTS	- The following pins must be left as no-connects: A29, A31, A33, AC37, AJ3, AK24, AK30, AL1, AL11, AM2, AN13, AN23, B36, C29, C31, C33, C35, E21, E29, E31, E35, E37, F10, G33, L33, N33, N35, Q33, Q35, Q37, R2, V4, W35, X2, Y1, Z36.
NCHCTRL (N37)	- 14 Ω pull-up resistor to VTT.

13.3 System Memory Interface Checklist

Checklist Items	Recommendations
SM_CSA#[0:3, SM_CSB#[3:0, SMAA[11:8,3:0], SM_MD[0:63], SM_CKE[0:3], S_DQM[0:7]	- Connect from GMCH to DIMM0, DIMM1
SM_MAA[7:4], SM_MAB[7:4]#	- Connect from GMCH to DIMM0, DIMM1 through 10 Ω resistors
SMAA[12]	- Connect GMCH through 10 kΩ resistor to transistor junction as per Chapter 4 for systems supporting the *universal PGA370* design.
SM_CAS#	- Connected to R_REFCLK through 10 kΩ resistor.
SM_RAS#	- Jumpered to GND through 10 kΩ resistor
SM_WE#	- Connected to R_BSEL0# through 10 kΩ resistor.
CKE[5..0] (For 3 DIMM implementation)	- When implementing a 3 DIMM configuration, all six CKE signals on the GMCH are used. (0,1 for DIMM0; 2, 3 for DIMM1; 4,5 for DIMM2)
REGE	- Connect to GND (since the Intel® 815G chipset platform does not support registered DIMMS).
WP(Pin 81 on the DIMMS)	- Add a 4.7 kΩ pull-up resistor to 3.3 V. This recommendation write-protects the DIMM's EEPROM.
SRCOMP	- Needs a 40 Ω resistor pulled up to 3.3 V standby.

13.4 Hub Interface Checklist

Checklist Items	Recommendations
HUBREF	- Connect to HUBREF generation circuitry.
HL_COMP	- Pull-up to VCC1.85 through 40 Ω (both GMCH and ICH side).

13.5 Digital Video Output Port Checklist

Checklist Items	Recommendations
DVI Input Reference Circuit	• See the third party vendor of the device of choice in your design. The Third-Party Vendor information is a part of this Design Guide and its associated Design Guide Updates.

13.6 Intel® ICH Checklist

13.6.1 PCI Checklist

Checklist Items	Recommendations
AD[31:0]	• AD16,17 pass through 100 Ω resistor.
ACK 64# REQ 64#	• (5 V PCI environment) 2.7 kΩ (approximate) pull-up resistors to VCC5. • (3 V PCI environment) 8.2 kΩ (approximate) pull-up resistors to VCC3_3. • Each REQ 64# and ACK 64# requires it's own pull-up.
PTCK	• Pull-down through 5.6 kΩ to GND • Connect to PCI Connectors only.
PTDI, PTRST#, PTMS	• Pull-up through 5.6 kΩ resistor to VCC5 • Connect to PCI Connectors only.
PRSNT#21, PRSNT#22, PRSNT#31, PRSNT#32	• Decoupled with 0.1 µF capacitor to GND
PIRQ#C, PIRQ#D, U2_ACK64#, U2_REQ64#, U3_ACK64#, U3_REQ64#, PREQ#1, PLOCK#1, STOP#, TRDY#, SERR#, PREQ#3, PIRQ#A, PERR#, PREQ#0, PREQ#2 DEVSEL#, FRAME#, IRDY#	• Pull-up through 2.7 kΩ resistor to VCC5
PCIRST#	• Pull signal down through 0.1 µF capacitor when input for USB. Input to buffer for PCIRST_BUF#.
PCPCI_REQ#A, REQ#B/GPIO1, GNT#B/GPIO17, PGNT#0, PGNT#1, PGNT#2, PGNT#3	• Pull-up through 8.2 kΩ resistor to VCC3_3
PCLK_3	• Signal coming from Intel® CK-815 device pass through a 33 Ω resistor to PCI connector.
PCIRST_BUF#	• Signal comes from buffered PCIRST# • Pull-up through 8.2 kΩ resistor to VCC3_3 • Passes through 33 Ω resistor

Checklist Items	Recommendations
SDONEP2, SDONEP3, SBOP2, SBOP3	- Pull-up through 5.6 kΩ resistor to VCC5
R_RSTP#, R_RSTS#	- Signal is from PCIRST_BUF# and passes through a 33 Ω resistor
IDSEL lines to PCI connectors	- 100 Ω series resistor.
3V_AUX	- Optional to 3VSB, but required if PCI devices supporting wake up events.

13.6.2 USB Checklist

Checklist Items	Recommendations
USBP0P, USBP0N, USB_D1_N, USB_D1_P	- Decouple through a 47 pF capacitor to GND - Signal goes through 15 Ω resistor - Pull-down through a 15 kΩ resistor to GND
OC#0	- Connected to AGP/AC ’97 Circuitry (See Intel CRB Schematic pg. 20)
USB_D2_N, USB_D2_P, USB_D3_N, USB_D3_P, USB_D4_N, USB_D4_P, USBP1P, USBP1N, USBP0P, USBP0N	- Pull-down through a 15 kΩ resistor to GND
D-/D+ data lines	- Use 15 Ω series resistors.
VCC USB	- Power off 5 V standby if wake on USB is to be implemented IF there is adequate standby power. It should be powered off of 5 V core instead of 5 V standby if adequate standby power is not available.
Voltage Drop Considerations	- The resistive component of the fuses, ferrite beads and traces must be considered when choosing components and Power/GND trace width. This must be done such that the resistance between the VCC5 power supply and the host USB port is minimized. Minimizing this resistance will minimize voltage drop seen along that path during operating conditions.
Fuse	- A minimum of 1A fuse should be used. A larger fuse may be necessary to minimize the voltage drop.
Voltage Droop Considerations	- Sufficient bypass capacitance should be located near the host USB receptacles to minimize the voltage droop that occurs on the hot attach of new device. See most recent version of the USB specification for more information.

13.6.3 AC ’97 Checklist

Checklist Items	Recommendations
AC_SDOUT	- Pulled up to VCC3_3 through a 10 kΩ resistor and a jumper to AC ’97 Connector and AC ’97 codec from ICH.
AC_SDIN0 AC_SDIN1	- Pull-down through a 10 kΩ resistor to GND. The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active – they should be pulled to ground through a weak (approximately 10 kΩ) pull-down resistor (see Section 5.9.3 for more information).

Checklist Items	Recommendations
AC97_OC#	• Connects to OC# circuitry. (see CRB schematics page 20).
AC_XTAL_OUT, AC_XTAL_IN	• Signal comes from Oscillator Y4 • Decouple through a 22 pF capacitor to GND
PRI_DWN#	• Connected through jumper to PRI_DWN_U or GND. (see CRB schematic page 27) If the motherboard implements an active primary codec on the motherboard and provides and AMR connector, it must tie PRI_DN# to GND.
PRI_DWN_U	• Pull-up through a 4.7 kΩ resistor to VCC3SBY
LINE_IN_R	• From FB9 decouple through a 100 pF NPO capacitor to AGND. Run signal through 1 µF TANT capacitor

13.6.4 IDE Checklist

Checklist Items	Recommendations
PDCS3#, SDCS3#, PDA[2:0], SDA[2:0], PDD[15:0], SDD[15:0], PDDACK#, SDDACK#, PRIOR#, SDIOR#, PDIOW#, SDIOW#	• Connect from ICH to IDE Connectors. No external series termination resistors required on those signals with integrated series resistors.
PDD7, SDD7	• Pull-down through a 10 kΩ resistor to GND.
PDREQ, SDREQ	• Pull-down through a 5.6 kΩ resistor to GND.
PIORDY, SIORDY	• Pull-up through a 1 kΩ resistor to VCC5
PDCS1#, SDCS1#	• Connect from ICH to IDE Connectors
PRI_PD1, PRI_SD1	• Pull-down through a 470 Ω resistor to GND.
IDE_ACTIVE	• From IDEACTP# and IDEACTS# connect to HD LED circuitry (see CRB Schematic page 35)
CBLID#/PDIAG#	• Refer to Section 10.2 for the correct circuit. • NOTE: All ATA66 drives will have the capability to detect cables.
IDE Reset	• This signal requires a 22 Ω–47 Ω series termination resistor and should be connected to buffered PCIRST#.
IRQ14, IRQ15	• Need 8.2 kΩ resistor to 10 kΩ pull-up resistor to 5 V.
CSEL	• Pull-down to GND through 4.7 kΩ resistor (approximate).
IDEACTP#, IDEACTS#	• For HD LED implementation use a 10 kΩ (approximate) pull-up resistor to 5 V.

13.6.5 Miscellaneous Intel® ICH Checklist

Checklist Items	Recommendations
RTC circuitry	• Refer to Section 10.9 for exact circuitry.
PME#, PWRBTN#, LAD[3..0]#/FWH[3..0]#	• No external pull-up resistor on those signals with integrated pull-ups.
SPKR	• Optional strapping: Internal pull-up resistor is enabled at reset for strapping after - reset the internal pull-up resistor is disabled. Otherwise connect to motherboard speaker logic. (When strapped, use strong pull-up, e.g., 2 kΩ)
AC_SDOUT, AC_BITCLK	• Optional strapping: Internal pull-up resistor is enabled at reset for strapping after - reset the internal pull-up resistor is disabled. Otherwise connect to AC ’97 logic.
AC_SDIN[1:0]	• Internal pull-down resistor is enabled only when the AC link hut-off bit in the ICH is set. • Use 10 kΩ (approximate) pull-down resistors on both signals if using AMR. • For onboard AC ’97 devices, use a 10 kΩ (approximate) pull-down resistor on the signal that is not used. • Otherwise, connect to AC ’97 logic.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	• No external series termination resistors on those signals with integrated series resistors.
PCIRST#	• The PCIRST# signal should be buffered to the IDE connectors.
No floating inputs (including bi-directional signals):	• Unused core well inputs should be tied to a valid logic level (either pulled up to 3.3 V or pulled down to ground). Unused resume well inputs must be either pulled up to 3.3VSB or pulled down to ground. Ensure all unconnected signals are OUTPUTS ONLY!
PDD[15:0], SDD[15:0]	• PDD7 and SDD7 need a 10 kΩ (approximate) pull-down resistor. No other pull-ups/pull-downs are required. Refer to ATA ATAPI-4 specification.
PIORDY, SDIORDY	• Use approximately 1 kΩ pull-up resistor to 5 V.
PDDREQ, SDDREQ	• Use approximately 5.6 kΩ pull-down resistor to ground.
IRQ14, IRQ15	• Need 8.2 kΩ (approximate) pull-up resistor to 5 V.
HL11	• No pull-up resistor required. A test point or no stuff resistor is needed to be able to drive the ICH into a NAND tree mode for testing purposes.
VCCRTC	• No clear CMOS jumper on VCCRTC. Use a jumper on RTCRST# or a GPI, or use a safe-mode strapping for clear CMOS.
SMBus: SMBCLK SMBDATA	• The value of the SMBus pull-ups should reflect the number of loads on the bus. For most implementations with 4–5 loads, 4.7 kΩ resistors are recommended. OEMs should conduct simulation to determine exact resistor value.

Checklist Items	**Recommendations**
APICD[0:1], APICCLK	• If the APIC is used: 150 Ω (approximate) pull-ups on APICD[0:1] and connect APICCLK to the clock generator. • If the APIC is not used: The APICCLK can either be tied to GND or connected to the clock generator, but not left floating.
GPI[8:13]	• Ensure all wake events are routed through these inputs. These are the only GPIs that can be used as ACPI-compliant wake events because they are the only GPI signals in the resume well that have associated status bits in the GPE1_STS register.
HL_COMP	• RCOMP Method: Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull-up resistor to 1.85 V via a 10-mil wide, very short(-0.5 inch) trace (targeted for a nominal trace impedance of 40 Ω)
5V_REF	• Refer to Section 12.5.3 for implementation of the voltage sequencing circuit.
SERIRQ	• Pull-up through 8.2 kΩ resistor (approximate) to 3.3 V
SLP_S3#, SLP_S5#	• No pull-ups required. These signals are always driven by the ICH.
CLK66	• Use 18 pF tuning capacitor as close as possible to ICH.
GPIO27/ALERTCLK GPIO28/ALERTDATA	• Add a 10 kΩ pull-up resistor to 3VSB (3 V standby) on both of these signals.
PCI_GNT#	• No external pull-ups are required on PCI_GNT# signals. However, if external pull-ups are implemented, they must be pulled up to 3.3 V.

13.7 LPC Checklist

Checklist Items	Recommendations
RCIN#	• Pull-up through 8.2 kΩ resistor to VCC3_3
LPC_PME#	• Pull-up through 8.2 kΩ resistor to VCC3_3. Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH.
LPC_SMI#	• Pull-up through 8.2 kΩ resistor to VCC3_3. This signal can be connected to any ICH GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion.
TACH1, TACH2	• Pull-up through 4.7 kΩ resistor to VCC3_3 • Jumper for decoupling option (decouple with 0.1 µF capacitor).
J1BUTTON1, JPBUTTON2, J2BUTTON1, J2BUTTON2	• Pull-up through 1 kΩ resistor to VCC5. Decouple through 47 pF capacitor to GND
LDRQ#1	• Pull-up through 4.7 kΩ resistor to VCC3SBY
A20GATE	• Pull-up through 8.2 kΩ resistor to VCC3_3
MCLK, MDAT	• Pull-up through 4.7 kΩ resistor to PS2V5.
L_MCLK, L_MDAT	• Decoupled using 470 pF to ground
RI#1_C, CTS0_C, RXD#1_C, RXD0_C, RI0_C, DCD#1_C, DSR#1_C, DSR0_C, DTR#1_C, DTR0_C, DCD0_C, RTS#1_C, RTS0_C, CTS#1_C, TXD#1_C, TXD0_C	• Decoupled using 100 pF to GND
L_SMBD	• Pass through 150 Ω resistor to Intel® 82559
SERIRQ	• Pull-up through 8.2 kΩ to VCC3_3
SLCT#, PE, BUSY, ACK#, ERROR#	• Pull-up through 2.2 kΩ resistor to VCC5_DB25_DR • Decouple through 180 pF to GND
LDRQ#0	• Connect to ICH from SIO. This signal is actively driven by the Super I/O and does not require a pull-up resistor.
STROBE#, ALF#, SLCTIN#, PAR_INIT#	• Signal passes through a 33 Ω resistor and is pulled up through 2.2 kΩ resistor to VCC5_DB25_CR. Decoupled using a180 pF capacitor to GND.
PWM1, PWM2	• Pull-up to 4.7 kΩ to VCC3_3 and connected to jumper for decouple with 0.1 µF capacitor to GND.
INDEX#, TRK#0, RDATA#, DSKCHG#, WRTPRT#	• Pull-up through 1 kΩ resistor to VCC5
PDR0, PDR1, PDR2, PDR3, PDR4, PDR5, PDR6, PDR7	• Passes through 33 Ω resistor • Pull-up through 2.2 kΩ to VCC5_DB5_CRDecouple through 180 pF capacitor to GND
SYSOPT	• Pull-down with 4.7 kΩ resistor to GND or IO address of 02Eh

13.8 System Checklist

Checklist Items	Recommendations
KEYLOCK#	• Pull-up through 10 kΩ resistor to VCC3_3
PBTN_IN	• Connects to PBSwitch and PBin.
PWRLED	• Pull-up through a 220 Ω resistor to VCC5
R_IRTX	• Signal IRTX after it is pulled down through4.7 kΩ resistor to GND and passes through 82 Ω resistor
IRRX	• Pull-up to 100 kΩ resistor to VCC3_3 • When signal is input for SI/O Decouple through 470 pF capacitor to GND
IRTX	• Pull-down through 4.7 kΩ to GND • Signal passes through 82 Ω resistor • When signal is input to SI/O Decouple through 470 pF capacitor to GND
FP_PD	• Decouple through a 470 pF capacitor to GND • Pull-up 470 Ω to VCC5
PWM1, PWM2	• Pull-up through a 4.7 kΩ resistor to VCC3_3
INTRUDER#	• Pull signal to VCCRTC (VBAT), if not needed.

13.9 FWH Checklist

Checklist Items	Recommendations
No floating inputs	• Unused FGPI pins need to be tied to a valid logic level.
WPROT, TBLK_LCK	• Pull-up through a 4.7 kΩ to VCC3_3
R_VPP	• Pulled up to VCC3_3, decoupled with two 0.1 µF capacitors to GND.
FGPI0_PD, FGPI1_PD, FGPI2_PD, FPGI3_PD, FPGI4_PD, IC_PD	• Pull-down through a 8.2 kΩ resistor to GND
FWH_ID1, FWH_ID2, FWH_ID3	• Pull-down to GND
INIT#	• FWH INIT# must be connected to processor INIT#.
RST#	• FWH RST# must be connected to PCIRST#.
ID[3:0]	• For a system with only one FWH device, tie ID[3:0] to ground.

13.10 Clock Synthesizer Checklist

Checklist Items	Recommendations
REFCLK	• Connects to R-RefCLK, USB_CLK, SIO_CLK14, and ICHCLK14.
GMCH_3V66/3V66_1	• Passes through 33 Ω resistor
ICH_3V66/3V66_0, DOTCLK	• Passes through 33 Ω resistor • When signal is input for ICH it is pulled down through a 18 pF capacitor to GND
DCLK/DCLK_WR	• Passes through 33 Ω resistor • When signal is input for GMCH it is pulled down through a 22 pF capacitor to GND
CPUHCLK/CPU_0_1	• Passes through 33 Ω resistor • When signal is input for 370PGA, Decouple through a 18 pF capacitor to GND
R_REFCLK	• REFCLK passed through 10 kΩ resistor • When signal is input for 370PGA, pull-up through 1 kΩ resistor to VCC3_3 and pass through 10 kΩ resistor
USB_CLK, ICH_CLK14	• REFCLK passed through 10 Ω resistor
XTAL_IN, XTAL_OUT	• Passes through 14.318 MHz Osc • Pulled down through 18 pF capacitor to GND
SEL1_PU	• Pulled up via MEMV3 circuitry through 8.2 kΩ resistor.
FREQSEL	• Connected to clock frequency selection circuitry through 10 kΩ resistor. (see CRB schematic, page 4)
L_VCC2_5	• Connects to VDD2_5[0..1] through ferrite bead to VCC2_5.
GMCHHCLK/CPU_1, ITPCLK/CPU_2, PCI_0/PCLK_OICH, PCI_1/PCLK_1, PCI_2/PCLK_2, PCI_3/PCLK_3, PCI_4/PCLK_4, PCI_5/PCLK_5, PCI_6/PCLK_6, APICCLK_CPU/APIC_0, APICCLK)ICH/APIC_1, USBCLK/USB_0, GMCH_3V66/3V66_1, AGPCLK_CONN	• Passes through 33 Ω resistor
MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7,	• Pass through 10 Ω resistor
SCLK	• Pass through 22 Ω resistor.
VCC3.3	• Connected to VTTPWRGD gating circuit as per Section 4.3.1 for systems supporting the *universal PGA370* design.

13.11 LAN Checklist

Checklist Items	Recommendations
TDP, TDN, RDP, RDN	- Pull-down through 50 Ω resistor to GND
LANAPWR	- Passes through 3 kΩ resistor
LANCLKRUN	- Pull-down through 62 kΩ resistor
LAN_ISOLATE#	- Connect to SUS_STAT# and PWROK
LAN_TEST	- Pull-down through a 4.7 kΩ resistor to GND
LAN_XTAL1, LAN_XTAL2	- Signal from 25 MHz oscillator - Decouple through a 22 pF capacitor to GND
FLD5_PD, FLD6_PD, RBIAS10, RBIAS100	- Pull-down through a 619 Ω resistor to GND
ACTLED/LI_CR	- Passes through 330 Ω resistor
LILED	- Connect to jumper, pull-up through 330 Ω resistor to VCC3SBY
ACT_CR	- Pull-up through 330 Ω resistor to VCC3SBY
RD_PD	- Pull-down RDP through 50 Ω resistor and to RDN through 50 Ω resistor to GND
TD_PD	- Pull-down TDP through 50 Ω resistor and to TDN through 50 Ω resistor to GND
SPEEDLED	- Connect LED anode to VCC3SBY through 330 Ω resistor and cathode to Intel® 82559. Jumper to VCC3SBY through 330 Ω resistor
CHASSIS_GND	- Use plane for this signal.
JP7_PU, JP18_PU, JP23_PU	- Pull-up through 330 Ω resistor to VCC3SBY
R_LANIDS	- Pass through 100 Ω resistor to AD20 from 82559 pin IDSEL.

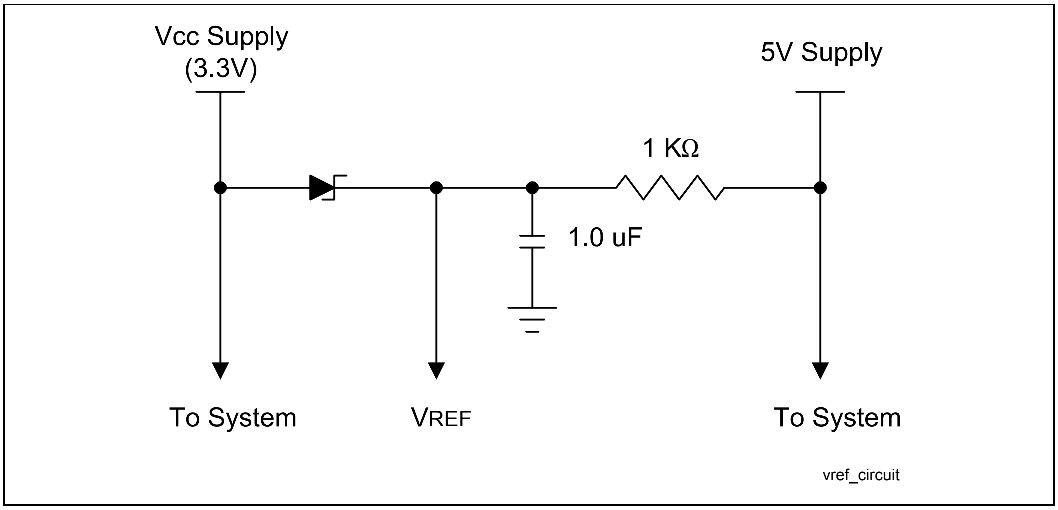
13.12 Power Delivery Checklist

Checklist Items	Recommendations
All voltage regulator components meet maximum current requirements	- Consider all loads on a regulator, including other regulators.
All regulator components meet thermal requirements	- Ensure the voltage regulator components and dissipate the required amount of heat.
VCC1_8	- VCC1_8 power sources must supply 1.85 V
If devices are powered directly from a dual rail (i.e., not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET.	- “Dual” voltage rails may not be at the expected voltage.
Dropout Voltage	- The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage.
Voltage tolerance requirements are met	- See individual component specifications for each voltage tolerance.

13.12.1 Power

Checklist Items	Recommendations
V_CPU_IO[1:0]	• The power pins should be connected to the proper power plane for the processor 's CMOS compatibility signals. Use one 0.1 µF decoupling capacitor.
VCCRTC	• No clear CMOS jumper on VCCRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS
VCC3.3	• Requires six 0.1 µF decoupling capacitors
VCCSus3.3	• Requires one 0.1 µF decoupling capacitor.
VCC1.85	• Requires two 0.1 µF decoupling capacitors.
VCCSus1.85	• Requires one 0.1 µF decoupling capacitor.
5V_REF SUS	• Requires one 0.1 µF decoupling capacitor. • V5REF_SUS only affects 5 V-tolerance for USB OC[3:0] ins and can be connected to VCCSUS3_3 if 5 V tolerance on these signal is not required.
5V_REF	• 5VREF is the reference voltage for 5 V tolerant inputs in the ICH. Tie to pins VREF[2:1]. 5VREF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. Refer to the figure below for an example circuit schematic that may be used to ensure the proper 5VREF sequencing.
VCMOS	• VCMOS power source must supply 1.5 V and be generated by circuitry on the motherboard.

Figure 75. V5REF Circuitry



14 Third-Party Vendor Information

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the 815G chipset platform for use with the universal socket 370. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

Super I/O (Vendors Contact Phone)

SMSC	Dave Jenoff (909) 244-4937
National Semiconductor	Robert Reneau (408) 721-2981
ITE	Don Gardenhire (512)388-7880
Winbond	James Chen (02) 27190505 - Taipei office

Clock Generation (Vendors Contact Phone)

Cypress Semiconductor	John Wunner 206-821-9202 x325
ICS	Raju Shah 408-925-9493
IMI	Elie Ayache 408-263-6300, x235
PERICOM	Ken Buntaran 408-435-1000

Memory Vendors

http://developer.intel.com/design/motherbd/se/se_mem.htm

Voltage Regulator Vendors (Vendors Contact Phone)

- TBD

GPA (a.k.a. AIMM) Card (Vendors Contact Phone)

Kingston	JK_TSAI@kingston.com Richard_Kanadjian@kingston.com
Smart Modular	James.Lee@smartm.com Arthur.SAINIO@smartm.com
Micron Semiconductor	TBD

TMDS Transmitters

Silicon Images	John Nelson (408) 873-3111
Texas Instrument	Greg Davis [gdavis@ti.com] (214) 480-3662
Chrontel	Chi Tai Hong [cthong@chrontel.com] (408) 544-2150

TV Encoders

Chrontel	Chi Tai Hong [cthong@chrontel.com] (408)544-2150
Conexant	Eileen Carlson [eileen.carlson@conexant.com] (858) 713-3203
Focus	Bill Schillhammer [billhammer@focusinfo.com] (978) 661-0146
Philips	Marcus Rosin [marcus.rosin@philips.com]
Texas Instrument	Greg Davis[gdavis@ti.com] (214) 480-3662

Combo TMDS Transmitters/TV Encoders

Chrontel	Chi Tai Hong [cthong@chrontel.com] (408) 544-2150
Texas Instrument	Creg Davis[gdavis@ti.com] (214) 480-3662

LVDS Transmitter

National Semiconductor	387R Jason Lu [Jason.Lu@nsc.com] (408) 721-7540

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