Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845GE/845PE Chipset

Platform Design Guide Update

August 2004

Notice: The Intel® 845 chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 252396-004

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Revision History

Revision	Draft/Changes	Date
-001	Initial Release	June 2003
-002	Added Documentation Change #7, Replace Power Delivery Map in Section 13.1, Figure 13-1	September 2003
-003	Added Documentation Change #8, Revise Section 17.1.3, Schematic Checklist, Processor Connector/Intel ICH4 Items, PWRGOOD	March 2004
-004	Added Documentation Change 9-11	August 2004

Preface

This public Design Guide Update document is an update to the specifications and information contained in the *Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845GE/845PE Chipset Platform Design Guide*, Oct 2002. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2002. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types.

Affected Documents

Document Title	Document Number
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845GE/845PE Chipset Platform Design Guide, October 2002	251925-001

Related Documents

Document Title	Document Number
Intel® 845GE/845PE Chipset Datasheet, Intel® 82845GE Graphics and Memory Controller Hub (GMCH) and Intel® 82845PE Memory Control Hub (MCH), October 2002	251924-001

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 82845GE GMCH or 82845PE MCH.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Consideration changes in this Design Guide Update revision.

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
1	Doc	The Intel® 845GE Chipset GMCH Ball AB3 is a RSVD Ball and Is a No-Connect (NC) Ball

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Corrected CLK 408 Pin Names
2	Doc	Replaced Section 8.1.4, Hub Interface HI_REF/HI SWING HI_SWING, Generation/Distribution
3	Doc	Modified Section 17.11.1, Intel® ICH4 Power and Ground Items Checklist
4	Doc	Changed Section 17.10.5, Intel® ICH4 System Bus / SMLink Interface Items Checklist
5	Doc	Changed the title of Section 9.10 to “Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM”
6	Doc	Replaced Section 9.10.1, Intel® 82562EZ/ET/EX/EM Disable Guidelines
7	Doc	Replace Power Delivery Map in Section 13.1, Figure 13-1
8	Doc	Revise Section 17.1.3, Schematic Checklist, Processor Connector/Intel® ICH4 Items, PWRGOOD
9	Doc	Revise Section 9.8.1, RTC Crystal, to Figure 9-30 add Note 11
10	Doc	Revise Section 9.8.5, RTC External RTCRST# Circuit, Figure 9-32
11	Doc	Revise Section 9.11.3, Power-Well Isolation Control Requirement

General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

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Schematic, Layout, and Routing Updates

1. The Intel® 845GE Chipset GMCH Balls AB3 Is a RSVD Ball and Is a No-Connect (NC) Ball

Reference sheet 11 of the *Intel® 845GE DDR Schematics, Rev 2.0*, which is *Appendix A, Customer Reference Board Schematics*, of the *Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845GE/845PE Chipset Platform Design Guide*, document number 251925-001.

IC U6D1, block 5 of 5 of the 845GE device, on the right side of sheet 11, shows ball AB3 in the lower left corner of block 5 of 5 as a RSVD pin with an input from sheet 77 and/or sheet 76 of the schematics. This is incorrect. There are no sheets 76 or 77 in the schematics.

AB3 is a RSVD ball and should be left as a no-connect (NC) ball.

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Documentation Changes

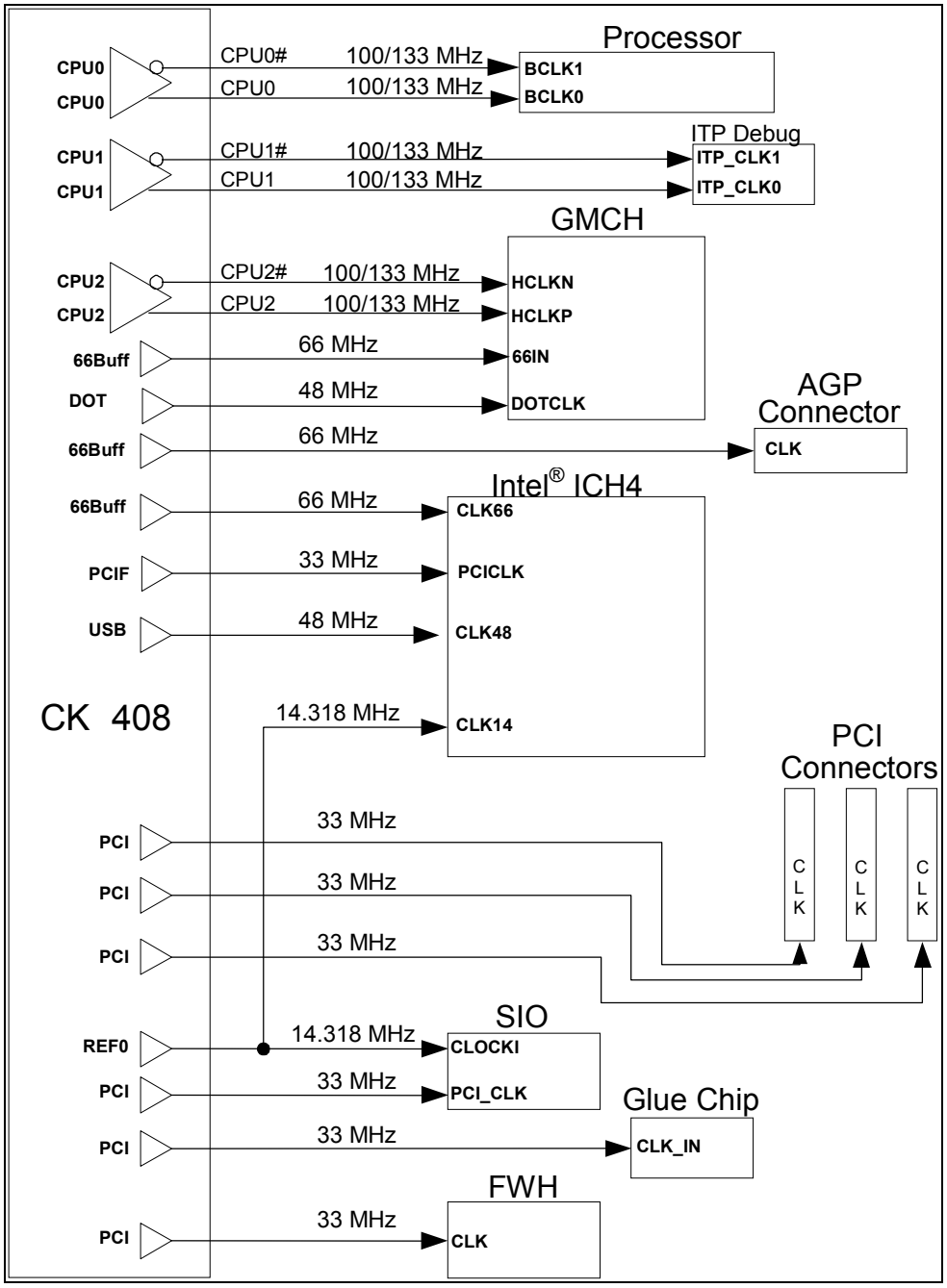
1. CLK408 Pin Names

(1) Reference Section 12, *Platform Clock Routing Guidelines*. Replace Table 12-2, *Platform System Clock Cross-Reference*, with the following new table:

Table 12-2. Platform System Clock Cross Reference

Clock Group	CK-408 Pin	Component	Component Pin Name
HOST_CLK	CPU0	CPU	BCLK0
	CPU0#	CPU	BCLK1
	CPU1	ITP Debug Port	BCK
	CPU1#	ITP Debug Port	BCK#
	CPU2	(G)MCH	HCLKP
	CPU2#	(G)MCH	HCLKN
DOT_CLK	DOT_48 MHz	GMCH (845GE chipset only)	DREFCLK
CLK66	3V66	(G)MCH	GCLKIN
		Intel® ICH4	CLK66
AGPCLK	3V66	AGP Connector or AGP Device	AGPCLK
CLK33	PCIF	Intel® ICH4	PCICLK
	PCI	SIO	PCI_CLK
	3V66	Glue Chip	CLK_IN
	PCI	FWH/Flash BIOS	CLK
CLK14	REF0	ICH4	CLK14
		SIO	CLOCKI
PCICLK	PCI	PCI Connector #1	CLK
		PCI Connector #2	CLK
		PCI Connector #3	CLK
USBCLK	USB_48MHz	ICH4	CLK48

(2) Replace Figure 12-1, *Platform Clocking Block Diagram*, with the following new diagram:



(3) Reference Section 17.9, *Clock Interface CK_408 Items*. Replace the CPU2 and CPU2# Checklist Items with the following:

CPU2	• Connect to **HCLKP** in GMCH • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	Host Clock Group Refer to Section 12.2.1.
CPU2#	• Connect to **HCLKN** in GMCH • Connect to a series 27.4 Ω ± 1% resistor and terminate to GND through a 49.9 Ω ±1% resistor	Host Clock Group Refer to Section 12.2.1.

2. Replace Section 8.1.4, Hub Interface HI_REF/HI SWING HI_SWING, Generation/Distribution

Replace Section 8.1.4, *Hub Interface HI_REF/HI_SWING Generation/Distribution* with the following new section. The new material includes a new Table 8-1 and new Figures 8-2 and 8-3.

8.1.4 Hub Interface HI_REF/HI_SWING Generation/Distribution

HI_REF is the Hub Interface reference voltage. The ICH4 uses HI_VSWING to control voltage swing and impedance strength of the hub interface buffers. The GMCH HI_REF and HI_SWING voltage requirement and associated resistor/capacitor recommendations for the voltage divider circuit are listed in Table 8-1. Only one of the two HI_VSWING values (700 mV or 800 mV) should be used. It is suggested that 800 mV be used on new designs. Any new design using either 700 mV or 800 mV should be validated.

Table 8-1. Hub Interface HI_REF/HI_VSWING Generation Circuit Specifications

HIREF (V)	Recommended Values for the HIREF / HI_VSWING Divider Circuit (Ω)	
350 mV +/- 2% at 1.5 V nominal	**Using HI_VSWING Spec of 800 mV ± 2% at 1.5 V Nominal (Recommended)**	**Using HI_VSWING Spec of 700 mV ± 2% at 1.5 V Nominal (Requires System Validation)**
	Option 1 (Figure 8-2 and Figure 8-3) R1 = 226 Ω ± 1%, R2 = 147 Ω ± 1%, R3 = 113 Ω ± 1% Option 2 (Figure 8-2 and Figure 8-3) R1 = 80.6 Ω ± 1%, R2 = 51.1 Ω ± 1%, R3 = 40.2 Ω ± 1% Option 3 (Figure 8-2 and Figure 8-3) R1 = 255 Ω ± 1%, R2 = 162 Ω ± 1%, R3 = 127 Ω ± 1% Capacitance Values For All Options C1 and C3 = 0.1uF (near divider) C2, C4, C5, C6 = 0.01uF (near component)	Option 1 (Figure 8-2 and Figure 8-3) R1 = 226 Ω ± 1%, R2 = 100 Ω ± 1%, R3 = 100 Ω ± 1% Other options are available using Figure 8-2 and Figure 8-3 by changing resistor values to achieve the correct voltage. Capacitance Values For All Options C1 and C3 = 0.1uF (near divider) C2, C4, C5, C6 = 0.01uF (near component)

The resistor values, R1, R2, and R3, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. Two 0.1 µF capacitors (C2, C5) should be placed close the divider. In addition, the 0.01 µF bypass capacitors (C1, C3, C4, C6) should be placed within 0.25 inch of the component HI_REF/VREF pin (for C3 and C4) and HI_SWING pin (for C1 and C6). The max distance from the voltage divider resistor network to the device is 4 inches (less is better). Normal care must be taken to minimize crosstalk to other signals (< 10–15 mV). Two examples of the HI_REF/HI_VSWING voltage divider circuits are Figure 8-2 and Figure 8-3. If the single HI_REF/HI_SWING divider circuit is located more than 4 inches away from the divider network, the locally generated reference divider (Figure 8-3) should be used.

Figure 8-2. Hub Interface Single HI_REF/HI_SWING Generation Circuit

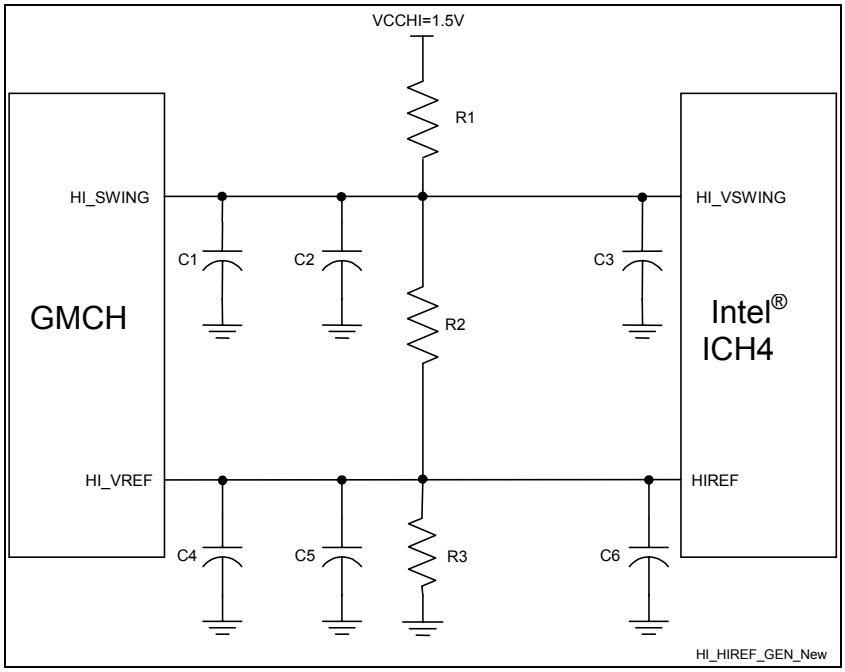
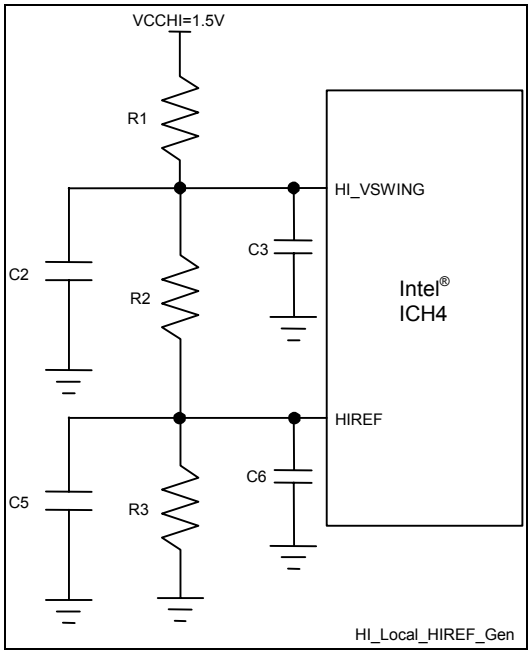


Figure 8-3. Hub Interface Local HI_REF/HI_SWING Generation Circuit (Intel® ICH4 side)



3. Section 17.11.1, Intel® ICH4 Power and Ground Items Checklist

Reference Section 17.11.1, *Intel® ICH4 Power and Ground Items Checklist*.

(1) In the "Reason/Impact/Documentation" section of the V5_REF Checklist Item, add the following: "V5_REF must be connected properly for USB2 to work."

(2) In the "Reason/Impact/Documentation" section of the V5_REF_Sus Checklist Item, add the following: "V5_REF_Sus must be connected properly for USB2 to work."

4. Section 17.10.5, Intel® ICH4 System Bus / SMLink Interface Items Checklist

Change the "Recommendation" of the INTRUDER# Checklist Item to: "This signal requires a very weak pull-up to the RTC power well. Pull signal to VCCRTC (VBAT) through a 330 kΩ resistor."

5. Section 9.10 Title is Changed to "Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM"

Change the title of Section 9.10 to show the correct title shown above.

6. Section 9.10.1, Intel® 82562EZ/ET/EX/EM Disable Guidelines

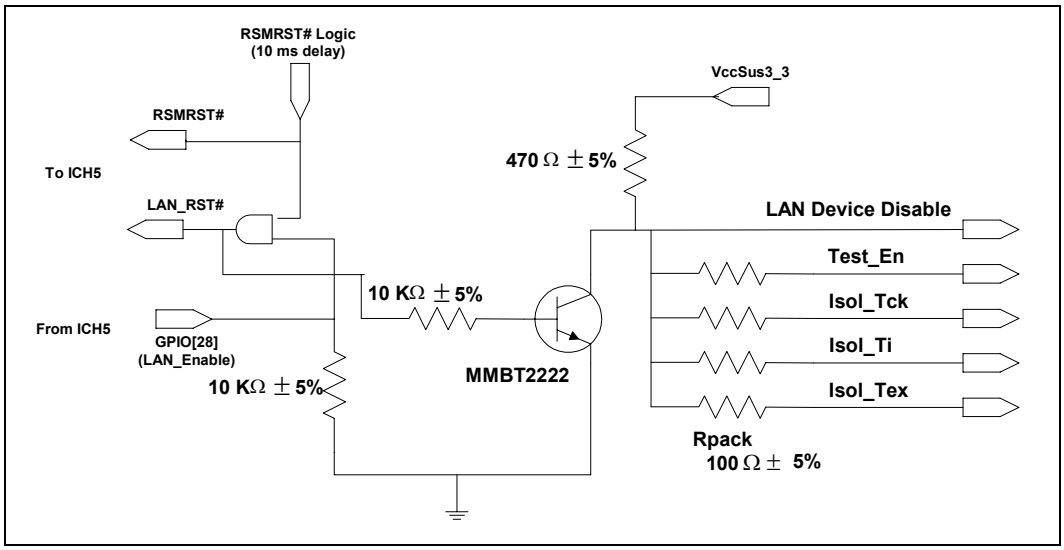
Section 9.10.1, *Intel® 82562EZ/ET/EX/EM Disable Guidelines*, is replaced with the following:

9.10.1 Intel® 82562EZ/ET/EX/EM Disable / Power Down Guidelines

To power down the Intel® 82562EZ/ET/EX/EM, the device must be isolated (disabled) prior to or during reset (LAN_RST#) asserting. Using a GPIO, such as GPIO[28] to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss, since GPIO[28] is high during and after reset. The example circuit shown below will correct this behavior. The BIOS controlling the GPIO can disable the LAN PHY.

Note: LAN_RST# needs to be held low for 10 ms after power is stable. It is assumed that the RSMRST# logic will provide this delay. Because GPIO[28] will default to high on power up, an AND gate has been implemented to ensure the required delay for LAN_RST# is met.

Figure 9-40. Example Intel® 82562EZ/ET/EX/EM Disable/Power Down Circuitry



There are 4 pins which are used to put the Intel® 82562EZ/ET/EX/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

The four control signals shown in the below table should be configured as follows:

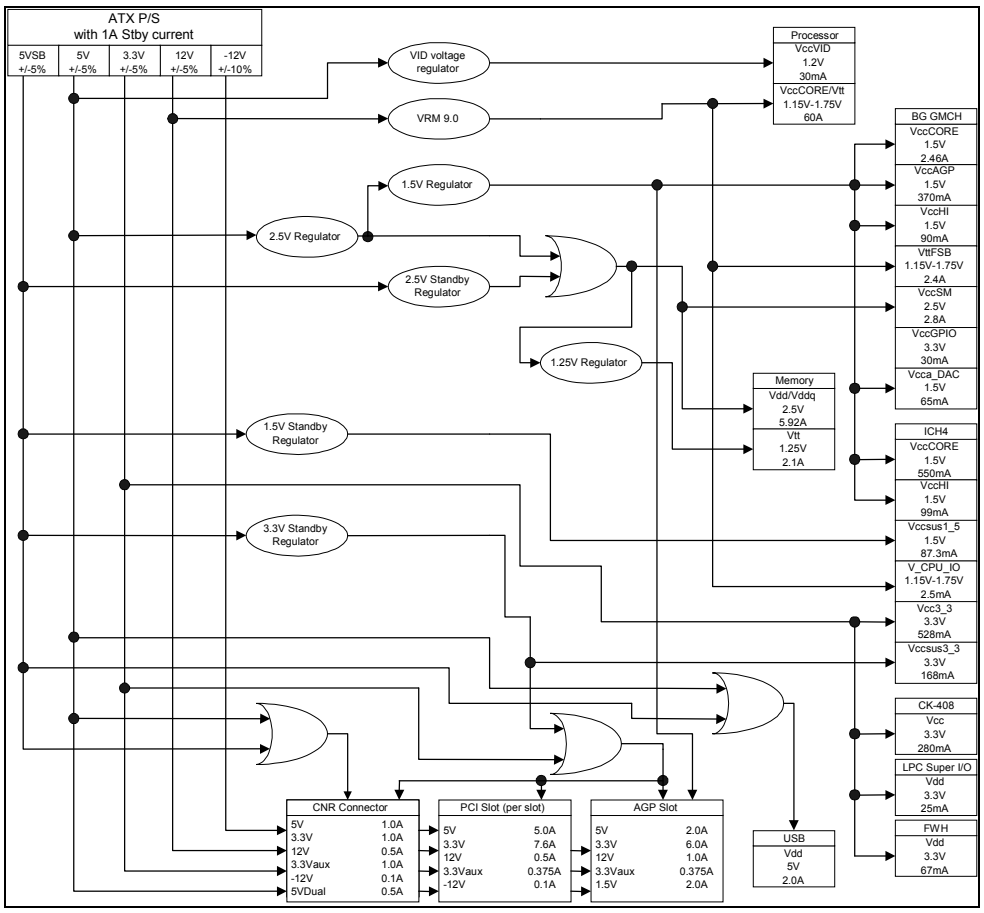
- Test_En should be pulled-down thru a 100 Ω resistor.
- The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node "Intel® 82562EZ/ET/EX/EM _Disable" of the disable circuit.

Table 9-20. Intel® 82562EZ/ET/EX/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

7. Replace the Power Delivery Map in Section 13.1, Figure 13-1, with the following:

Figure 13-1. Intel® 845GE/845PE Chipset DDR Platform Power Delivery Map



8. Revise Section 17.1.3, Schematic Checklist, Processor Connector/Intel® ICH4 Items, PWRGOOD

Revise Section 17.1.3, Schematic Checklist, Processor Connector/Intel® ICH4 Items, PWRGOOD, Connection, with the following:

Checklist Items	Connection
PWRGOOD	Connects to CPUPWRGD in ICH4 through a 60 ohm – 80 ohm series resistor (No extra pull-up resistors required). Note that a weak pullup to VCCP (V_CPU_IO) is required and that such value should not exceed ICH4s Ioh2/Iol2 specs.

9. Revise Section 9.8.1, RTC Crystal, Figure 9-30

In Section 9.8.1, RTC Crystal, add Note 11 to Figure 9-30:

Note 11: The diodes should be Schottkey diodes.

10. Revise Section 9.8.5, RTC External RTCRST# Circuit, Figure 9-32

In Section 9.8.5, revise Figure 9-32 as follows:

The resistor and capacitor on RTCRST# should be changed to the following values:

R: 180k ohm to 20K ohm

C: 0.1uF to 1.0uF

11. Revise Section 9.11.3, Power-Well Isolation Control Requirement

In Section 9.11.3, Power-Well Isolation Control Requirement, replace the first sentence with the following:

The RSMRST# signal of the ICH4 must transition from 20% signal level to 80% signal level and vice-versa in 50uS or less.