FC-PGA Intel® Pentium® III Processor and Intel® 840 Chipset

Design Guide

August 2000

Order Number: 273332-002

Contents

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Revision History

Date	Revision	Description
Aug 2000	002	Removed MRH-S references. Integrated the uniprocessor design guide supplement (273334) into this document.
Feb 2000	001	First public release.

Design Guide Introduction 1

This design guide organizes Intel's design recommendations for implementing single- or dual-processor systems using the Intel® Pentium® III processor (100/133 MHz system bus) in the Flip-Chip Pin Grid Array (FC-PGA) package together with the Intel® 840 chipset. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document also addresses possible system design issues such as thermal requirements for Intel 840 chipset systems.

This document presents design recommendations, board schematics, debug recommendations, and a system checklist that should be used in system design. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

The Intel schematics can be used as a reference for board designers. While the schematics may cover specific dual processor designs, the core schematics will remain the same for most FC-PGA Pentium III processor/Intel 840 chipset platforms.

The reference schematic features includes the following features:

- Dual processor, FC-PGA Socket 370
- Intel 840 chipset MCH, ICH, FWH, and P64H
- Two channels of RDRAM, 2 RIMMs per channel
- AGP universal connector
- 4x33 MHz/32-bit PCI (ICH) and 2x66 MHz/64-bit PCI (P64H)
- UltraDMA/66
- AC '97 audio
- 82559
- Super IO
- CK133W
- DRCG for Rambus*

1.1 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either uppercase or lowercase.
Numbers	Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)
Units of Measure	The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names	Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.2 Technical Support

1.2.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

1.2.1.1 Online Documents

Product documentation is provided online in a variety of Web-friendly formats at:

http://developer.intel.com/design/litcentr/index.htm

1.2.1.2 Intel Product Forums

Intel provides technical expertise through electronic messaging. With publicly accessible forums, you have all of the benefits of e-mail technical support, with the added benefit of the option of viewing previous messages written by other participants, and providing suggestions and tips that can help others.

Each of Intel's technical support forums is based on a single product or product family. Questions and replies are limited to the topic of the particular forum. Intel also provides several non-technical support related forums.

Complete information on Intel forums is available at:

http://support.intel.com/newsgroups/index.htm

1.2.2 Telephone Technical Support

In the U.S. and Canada, technical support representatives are available to answer your questions between 5 a.m. and 5 p.m. PST. You can also fax your questions to us. (Please include your voice telephone number and indicate whether you prefer a response by phone or by fax.) Outside the U.S. and Canada, please contact your local distributor.

800-628-8686	U.S. and Canada
916-356-7599	U.S. and Canada
916-356-6100 (fax)	U.S. and Canada

1.3 Product Literature

You can order product literature from the following Intel literature centers.

800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.4 Related Information

Table 1-1. Related Documents

Document Title	Order Number
Pentium® III Processor for the PGA370 at 500 MHz to 1GHz datasheet	245264
Intel® Pentium® III Processor Specification Update	244453
Intel® Pentium® III Processor Thermal Design Guide	273325
Intel® 840 Chipset: 82840 Memory Controller Hub (MCH) datasheet	298020
Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub datasheet	290655
Intel® 82806AA PCI64 Hub (P64H) datasheet	298025
P6 Family of Processors Hardware Developer's Manual	244001
Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	243191
Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide	243192
Intel Processor Serial Number application note	245125

Table 1-2. Related Specifications

Specification	URL
AC '97 Component Specification, Revision 2.1	http://developer.intel.com/pc-supp/platform/ac97/
Accelerated Graphics Port Interface Specification, Revision 2.0	http://developer.intel.com/technology/agp/agp_index.htm
Low Pin Count Interface Specification, Revision 1.0	http://developer.intel.com/design/chipsets/industry/lpc.htm
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com
PCI Local Bus Specification, Revision 2.2 ECNs	http://www.pcisig.com
PCI-PCI Bridge Specification, Revision 1.0	http://www.pcisig.com
PCI Bus Power Management Interface Specification, Revision 1.0	http://www.pcisig.com
Universal Serial Bus Specification, Revision 1.1	http://www.usb.org/developers/docs.html

System Overview 2

The Intel® 840 chipset is designed for Intel's Pentium® II, Pentium III, and Pentium III Xeon™ processor-based architectures. This chipset allows flexibility for dual and single FC-PGA Pentium III processor configurations with a 100 MHz or 133 MHz system bus. The Intel 840 chipset consists of three main components: the Memory Controller Hub (MCH), I/O Controller Hub (ICH) and Firmware Hub (FWH). Architectural expansion is provided with a memory expansion card and a PCI 64-bit Hub (P64H). The Intel 840 chipset components are interconnected via an interface called the hub interface. The hub interface is designed into the Intel 840 chipset to provide efficient communication between the chipset components.

Additional hardware platform features supported by the Intel 840 chipset include AGP 4X, RDRAM, Ultra DMA/66, Low Pin Count interface (LPC), and the Universal Serial Bus (USB). The Intel 840 chipset architecture eliminates the requirement for an ISA expansion bus, which was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many conflicts experienced when installing legacy ISA hardware and drivers.

The Intel 840 chipset architecture enables a new security and manageability infrastructure through the Firmware Hub component. A custom set of features provides a consistent pre-boot environment and enables a protected infrastructure for storing and updating platform code and data. The Intel 840 chipset is also ACPI-compliant and supports Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-off power management states. Through the use of an appropriate LAN device, the Intel 840 chipset also supports Wake-on-LAN for remote administration and troubleshooting.

2.1 Intel® 840 Chipset Components

The Intel 840 chipset consists of the Memory Controller Hub (MCH), the I/O Controller Hub (ICH) and the Firmware Hub (FWH). Additional functionality can be provided using memory expansion (memory repeater hub MRH-R) and the P64H.

2.1.1 Memory Controller Hub (MCH)

The MCH component contains the CPU interface, DRAM controller, P64H interface, AGP interface and ICH interface. It communicates with the Intel 840 chipset I/O controller (ICH) and the P64H over the hub interface. It supports dual channels of Direct RDRAM and AGP 4X data transfers. The MCH also contains advanced power management logic.

The Intel 840 chipset MCH contains the following functionality:

- Provides Dual Channel Pre-Fetched Architecture
- Supports single or dual FC-PGA Pentium III processor configurations at 100/133 MHz
- AGTL + host bus supporting 32-bit or 36-bit host addressing
- Dual direct RDRAM channels support for 300 MHz or 400 MHz operation
- Support 4-Gbyte RDRAM device support
- AGP interface with 4X SBA/Data Transfer and 2X/4X Fast Write capability
- 8-bit/66 MHz hub interface A to ICH
- 16-bit/66 MHz hub interface B to P64H
- Fully optimized data paths and buffering
- Distributed arbitration for highly concurrent operation

2.1.2 I/O Controller Hub (ICH)

The I/O Controller Hub provides the I/O subsystem access to the rest of the system. Additionally, it integrates many I/O functions. The ICH integrates the following features:

- Upstream hub link for access to the MCH
- Two-channel Ultra ATA/66 Bus Master IDE controller
- USB controller
- I/O APIC
- SMBus controller
- FWH interface
- Low Pin Count interface
- AC ’97 2.1 interface
- PCI 2.2 interface
- Integrated System Management controller
- Alert-on-LAN

The ICH also contains the arbitration and buffering needed to efficiently utilize these interfaces.

2.1.3 Firmware Hub (FWH)

The FWH component is a key element in enabling a new security and manageability infrastructure for the PC platform. The device operates under the FWH interface and protocol. The hardware features of this device include a unique Random Number Generator (RNG), register-based locking, and hardware-based locking.

2.1.4 Memory Repeater Hub for RDRAM (MRH-R)

The MRH-R component provides the capability to support multiple RDRAM channels from an "expansion channel." The expansion channel is the interconnect between the Intel 840 chipset MCH and the MRH-R. Each MRH-R can support up to two "stick" channels. The MRH-R acts as a pass-through logic with fixed delay for read and write accesses from expansion channels to RDRAM channels. MRH-R features also include:

- Maximum of 1-Gbyte memory per channel
- Nap Entry/Exit, Power Down Exit, Refresh and Precharge on a channel upon request from memory controller
- Core logic gating to minimize power consumption
- Clock generation for Direct Rambus* Clock Generator (DRCG)
- Integrated SMBus controller to read/write data from/to SPD EEPROM on the RIMMs

2.1.5 PCI 64-bit Hub (P64H)

The PCI-64 Hub (P64H) is a peripheral chip that performs PCI bridging functions between the hub interface and the PCI Bus and is used as an integral part of the Intel 840 chipset. The P64H has a 16-bit primary hub interface to the Memory Controller Hub (MCH) and a secondary 64-bit PCI Bus interface. The 64-bit interfaces inter-operate transparently with either 64-bit or 32-bit devices. The P64H fully complies with the *PCI Local Bus Specification,* Revision 2.2.

The P64H integrated functions include:

- Integrated PCI low skew clock driver
- I/O APIC

2.2 Bandwidth Summary

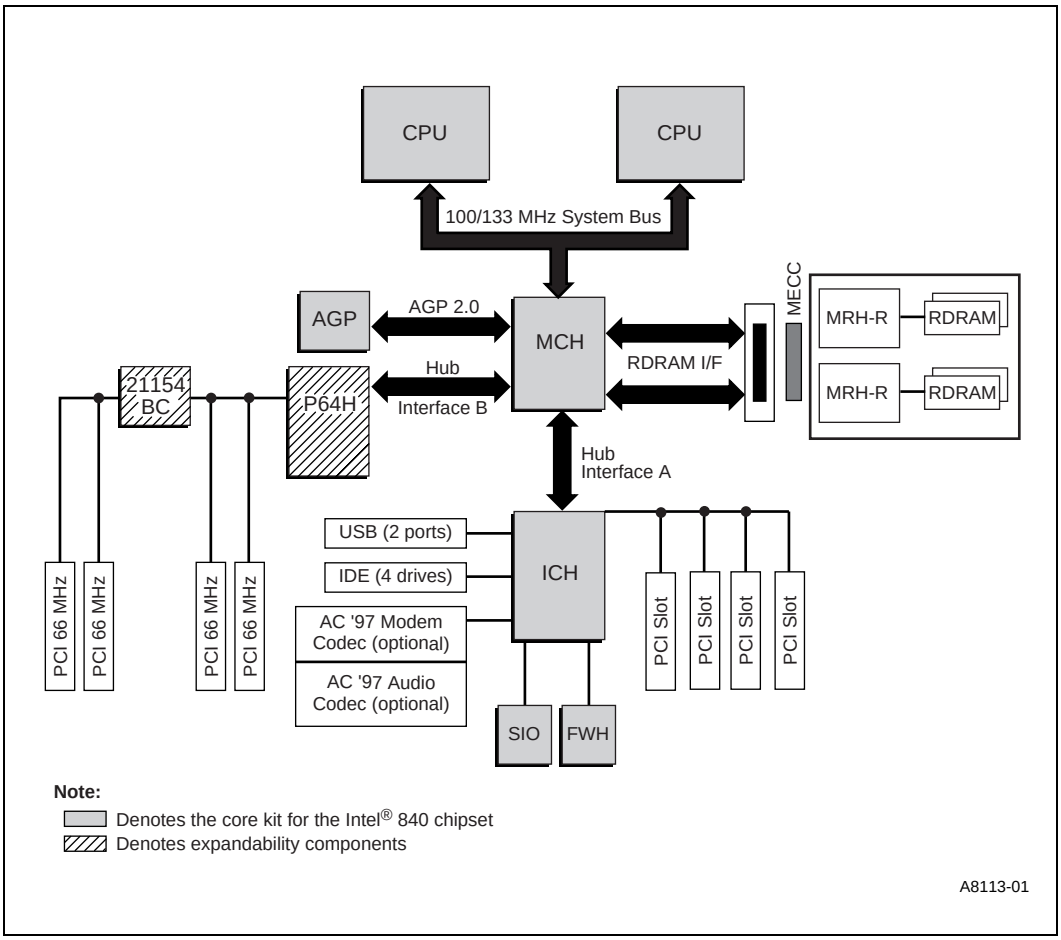
Table 2-1. Intel® 840 Chipset Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Msamples/s)	Data Width (Bytes)	Bandwidth (Mbyte/s)
CPU bus	133	1	133	8	1066
AGP 2.0	66	4	266	4	1066
Hub interface A	66	4	266	1	266
Hub interface B	66	4	266	2	533
PCI 2.2 (32-bit)	33	1	33	4	133
PCI 2.2 (64-bit)	66	1	66	8	528

2.3 System Configuration

2.3.1 Platform Configuration

Figure 2-1. Intel® 840 Chipset Configuration



Platform Initiatives 3

3.1 Memory Expansion Card and Connector

The memory expansion card (MEC) concept is intended to provide flexibility and scalability of memory to Intel® 840 chipset-based platforms. Specific design information on the memory expansion card and connector will be described in future releases of this document.

3.2 Direct RDRAM

The Direct RDRAM initiative will provide the necessary memory bandwidth for achieving optimal processor performance and enabling implementation of a high performance AGP controller. The MCH RDRAM interface supports 300-MHz and 400-MHz operations; 300-MHz operation provides 1.6 Gbyte/s of theoretical memory bandwidth and twice the memory bandwidth of 100 MHz SDRAM systems. Coupled with the greater bandwidth, the RDRAM protocol provides substantially more efficient data transfer. The RDRAM memory interface can achieve greater than 95% utilization of the 1.6 Gbyte/s theoretical maximum bandwidth.

In addition to the RDRAM's performance features, this new memory architecture provides enhanced power management capabilities. The powerdown mode of operation will enable Intel 840 chipset-based system to cost-effectively support suspend-to-RAM.

Industry leading DRAM vendors have agreed to develop RDRAMs, and module vendors will be developing RDRAM Inline Memory Modules (RIMMs). RIMMs provide approximately the same form factor as SDRAM DIMMs.

3.3 Accelerated Graphics Port (AGP)

3.3.1 AGP 2.0

The Accelerated Graphics Port (AGP) is a high performance, component-level interconnect targeted at 3-D graphical display applications. AGP is based on a set of performance extensions or enhancements to the PCI bus. The AGP interface is optimized for a point-to-point topology using either 1.5 V or 3.3 V signaling. The baseline performance level utilizes a 66 MHz clock to provide a peak bandwidth of 266 Mbyte/s. There are two options for higher performance levels: 2x mode and 4x mode. The 2x mode provides a peak bandwidth of 533 Mbyte/s and the 4x mode provides a peak bandwidth of 1066 Mbyte/s.

Refer to the *Accelerated Graphics Port Interface Specification,* Revision 2.0 and *AGP Design Guide (1x, 2x and 4x Modes & 1.5 V and 3.3 V Signaling),* Revision 1.0 for further details.

3.3.2 AGP Pro

AGP Pro specifies an extension to the AGP graphics bus connection for the high-performance workstation market segment. The AGP Pro specifications include electrical, mechanical and thermal requirements for the AGP Pro connector, card and chassis. It will also include examples of possible thermal solutions.

AGP Pro is expected to deliver up to four times the electrical power of the standard AGP interface through an extension to the AGP connector and provision of sufficient space for dissipating this increased power. AGP Pro also allows for multiple slot implementations where an AGP Pro Card is coupled with one or more PCI cards. The specification allows for flexible utilization of the thermal space provided for cards that dissipate significantly less than the maximum power-envelope. AGP Pro will retain mechanical and functional compatibility with AGP implying that an AGP card can plug into an AGP Pro connector, though the reverse will not be allowed.

Refer to the *AGP Pro Specification 1.0* for complete details at: http://www.agp.org.

3.4 Hub Interface

As I/O speed increases, the demand placed on the PCI bus becomes significant. With the addition of AC ’97, ATA/66 and existing USB, I/O requirement could impact the PCI bus performance. Intel 840 chipset’s hub interface architecture ensures that the I/O subsystem will receive adequate bandwidth. By placing the I/O bridge on the hub interface, it allows the I/O functions to obtain the necessary bandwidth for peak performance. In addition, the hub interface’s lower pin count allows a smaller package for the memory controller.

3.5 Security: The Intel® Random Number Generator

The Intel 840 chipset features the first of Intel’s platform security features, the Intel Random Number Generator (RNG). The Intel RNG is a component of the 82802 Firmware Hub (FWH) that supplies applications and security middleware products with true non-deterministic random numbers, through the Intel Security Driver.

Better random numbers provide for better security. Most cryptographic functions, especially those that provide authentication or encryption services, require random numbers for purposes such as key generation. One means of attacking those cryptographic functions is to predict the random numbers being used to generate those keys. Current methods that use system and user input to seed a pseudo-random number generator have shown to be susceptible to those attacks. The Intel RNG uses thermal noise across a resistor to generate true non-deterministic, unpredictable random numbers.

Applications often access cryptographic functions through security middleware products such as Microsoft’s CAPI*, RSA’s BSAFE*, and the OpenGroup’s CDSA*. Intel is working to ensure that middleware products and applications are enabled to take advantage of this capability. Implementing the BIOS requirements, and testing and loading the Intel Security Driver, ensures that the Intel RNG is enabled on your platform design.

The system BIOS must contain a System Device Node (devnode) for the FWH device in order for plug-and-play operating systems to use the Intel Random Number Generator through the Intel Security Driver. The devnode is required in order for the OS to find the FWH at enumeration time, and the specific devnode number associates the FWH with the Intel Security Driver. The *ICH BIOS Specification* (FM-1604) contains complete details on BIOS requirements to enable the Intel RNG.

- BIOS must report a single device node for the FWH:
  - — Intel Specific EISA ID (devnode number must be INT0800)
  - — Device Type: System peripherals/other
  - — Device Attribute: Non-configurable and cannot be disabled
  - — ANSI ID String: “Intel FWH”
  - — Memory Range Descriptor: Describing feature space
- For plug-and-play operating systems, BIOS ranges are allocated through E820h and ACPI structures, as in current BIOS.
- For non plug-and-play operating systems, FWH ranges should be reserved through the Int 15h E820h function.

A complete Intel 840 chipset system must have the Intel Security Driver loaded in order for applications to take advantage of the Intel Random Number Generator. The Intel Security Driver implements an interface that middleware and some applications call to access the Intel RNG. The Intel Security Driver can be obtained from the Intel Chipset Software Driver Web site at:

http://amber.intel.com/scripts-arms/index.asp.

The Intel Security Driver tests the Intel RNG hardware each time the driver is initialized. The Driver obtains a set of random numbers from the Intel RNG hardware and verifies that they meet the federal FIPS 140-1 randomness standard. A self-test application that explicitly verifies that the Intel RNG output is meeting the FIPS 140-1 standard is bundled with the Intel Security Driver at the above Web site. Running the self-test in continuous mode gets numbers from the Intel RNG and runs the FIPS 140-1 randomness test on those numbers.

To install the driver and self-test, run the InstallShield* executable, or unzip the OEM floppy version to two 3.5” disks and run SETUP.EXE from the disk. The default setup options add an Intel Security Driver folder, which contains the Self Test application, to the Windows Programs menu.

The Self Test application is not targeted at the end user; it should be used by the OEM to verify operation of the Intel RNG and the Intel Security Driver.

3.6 Clocks

A new clock synthesizer/generator specification, CK133W, has been defined for the Intel 840 chipset platform.

The CK133W shares the same pinout as CK133. Its features include:

- 14.31818 MHz Xtal Oscillator Input
- Four copies of 100/133 MHz CPU clocks (cycle jitter=150 ps @ 2.5 V)
- Two CPU/2 outputs
- Four copies of fixed 66 MHz @3.3 V clocks
- Eight copies of PCI clocks
- Three copies of I/O APIC clocks @16.667 MHz
- One copy of 48 MHz clock
- Two copies of 14.31818 MHz reference clocks
- Power Management Control Input pins
- Spread Spectrum Clocking support

Reference the *CK98W/S Clock Synthesizer/Driver Specification* for complete details.

3.7 WTX Form Factor

WTX is a new board-set and system form factor developed for the mid-range workstation market. This specification defines the board-set volume, the interface between the board-set and chassis, the I/O openings, and the thermal requirements. It also provides design suggestions for motherboard and chassis development.

Several major Intel architecture workstation vendors worldwide worked jointly to define the WTX form factor, incorporating the flexibility to accommodate the best designs for current and future mid-range workstations. The specification and other information on WTX are available at:

http://www.wtx.org

3.8 Manageability

The Intel 840 platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

3.8.1 TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset for recovery from a hardware lock.

3.8.2 CPU Present Indicator

The ICH looks for the CPU to fetch the first instruction after reset. If the CPU does not fetch the first instruction, the ICH reboots the system at the safe-mode frequency multiplier.

3.8.3 ECC Error Reporting

Upon detecting an ECC error, the MCH has the ability to send one of several messages to the ICH. The MCH can tell the ICH to generate either an SMI#, NMI#, SERR#, or TCO interrupt.

3.8.4 Function Disable

The ICH provides the ability to disable the following functions: AC '97 Modem, AC '97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. No interrupts or power management events are generated from the disabled functions.

3.8.5 Intruder Detect

The ICH provides an input signal, INTRUDER#, that can be attached to a switch that is activated when the system case is opened. The ICH can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

3.8.6 SMBus

The ICH integrates an SMBus controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RIMMs and thermal sensors.

3.8.7 Alert-On-LAN

The ICH supports Alert-On-LAN. In response to a TCO event (intruder detect, thermal event, CPU not booting) the ICH will send a hard coded message over the SMBus. A LAN controller can decode this SMBus message and send a message over the network to alert the network manager.

Refer to the *Wired for Management (WfM) Design Guide* for complete details at this URL:

http://www.intel.com/ial/wfm/design/

3.9 AC ’97

The *Audio Codec ’97 (AC ’97) Specification* defines a digital link that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC), or both an AC and an MC. Figure 3-1 and Figure 3-2 illustrate these digital links. The AC ’97 Specification defines the interface between the system logic and the audio/modem codec known as the AC ’97 Digital Link. The ability to add cost-effective audio and modem solutions as the platform migrates away from ISA is important. In addition, the AC ’97 audio and modem components are software configurable. AC ’97 replaces ISA audio and modem functionality, improves overall platform integration, eases migration from ISA architecture, and reduces cost.

By using an audio codec, the AC ’97 digital link enables cost-effective, high-quality, integrated audio on the Intel 840 chipset platform. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. The integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec or a modem with a modem codec. For systems requiring both audio and a modem, there are two solutions: the audio codec and the modem codec can be integrated into an AMC or separate audio and modem codecs can be connected to the ICH.

Modem implementation for different countries must be considered due to varying telephone standards. Using a single integrated codec or AMC, both the audio and modem can be routed to a connector near the rear panel where the external ports can be located. The digital link in the ICH is AC ’97 Rev. 2.1-compliant, supporting two codecs with independent PCI functions for the audio and modem. Microphone input and left/right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

Figure 3-1. AC ’97 with Audio/Modem Codec

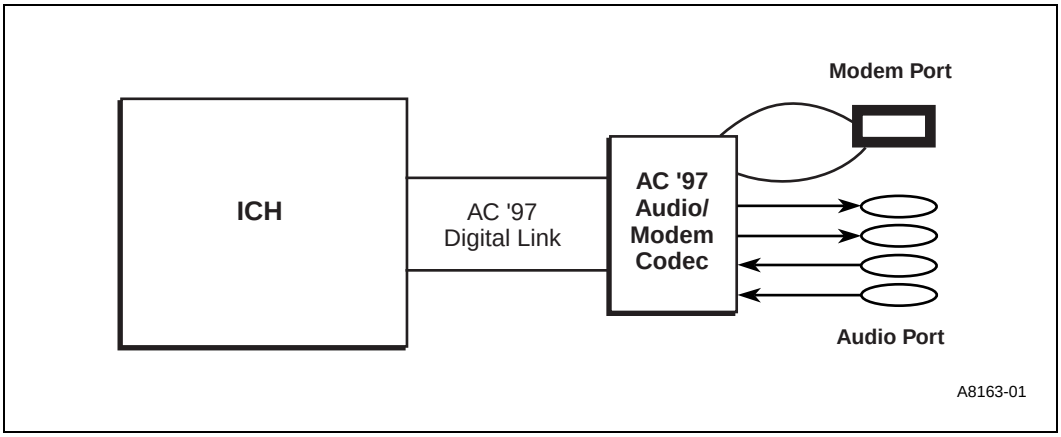
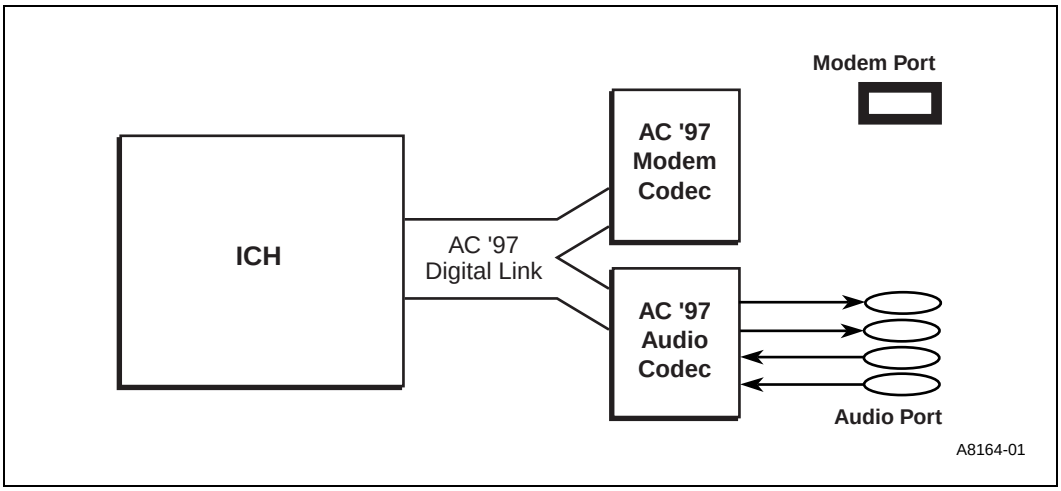


Figure 3-2. AC ’97 with Audio and Modem Codec



See the *AC ’97 Specification*, Revision 2.1, (http://developer.intel.com/pc-supp/platform/ac97/), for complete details.

3.10 Low Pin Count (LPC) Interface

In the Intel 840 chipset platform, the Super I/O component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It generally includes a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the standard Super I/O features, an integrated game port is recommended because the AC ’97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The 15-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface.

Refer to the *Low Pin Count Interface Specification*, Revision 1.0, (http://developer.intel.com/design/chipsets/industry/lpc.htm), for complete details. Consult your Super I/O vendor for a comprehensive list of devices offered and features supported.

3.11 Ultra DMA

Ultra DMA widens the path to the hard drive by transferring twice as much data per clock cycle. The maximum disk drive burst data transfer rate increases from 16.6 Mbyte/s to 66 Mbyte/s. Hard disk drive manufacturers can now bring higher performance products to market that can scale with the rest of the PC platform (faster hard drives to feed faster processors, memory, and graphics).

The Ultra DMA protocol lets host computers (PCs) send and retrieve data faster, removing bottlenecks associated with data transfers — especially during sequential operations. Users of new PCs will need less time to boot their systems and open applications, a direct result of the improved throughput provided by Ultra DMA. Current disk drive technology has been optimized to perform

within the limits of the legacy protocol (16.6 Mbyte/s). Raising the data transfer headroom results in moderate performance gains with today's drive technology. Greater performance improvements will emerge as drive manufacturers introduce products that generate a faster data stream.

The ICH supports both the Ultra DMA/33 and Ultra DMA/66 protocols. Ultra DMA/66 is similar to the Ultra DMA/33 scheme and is intended to be device driver compatible. The Ultra DMA/66 logic operates at 66 MHz and can move 16-bits of data every two clocks, for a maximum of 66 Mbyte/s.

3.12 Universal Serial Bus (USB)

Universal Serial Bus (USB) simplifies the process of attaching peripherals to the computer and accessing them. It also eases the system configuration process from an end-user's perspective. The USB specification outlines a single connector-type for all PC peripherals, automatic detection/ configuration of the USB devices, and transfer types allowed in the bus.

In the Intel 840 chipset-based platform, the ICH has an integrated USB Host Controller, and includes the root hub with two separate USB ports. The ICH Host Controller supports the standard Universal Host Controller Interface (UHCI), Revision 1.0.

Refer to the *USB Specification, Revision 1.1* at: http://www.usb.org for further details.

System Manufacturing 4

4.1 Component Quadrant Layout

The preliminary quadrant layouts shown are approximate. Only the exact ball assignment should be used to conduct routing analysis. Please reference the specific component's datasheet or other specification to document this information.

Figure 4-1. Top View - MCH 544 MBGA Quadrant Layout

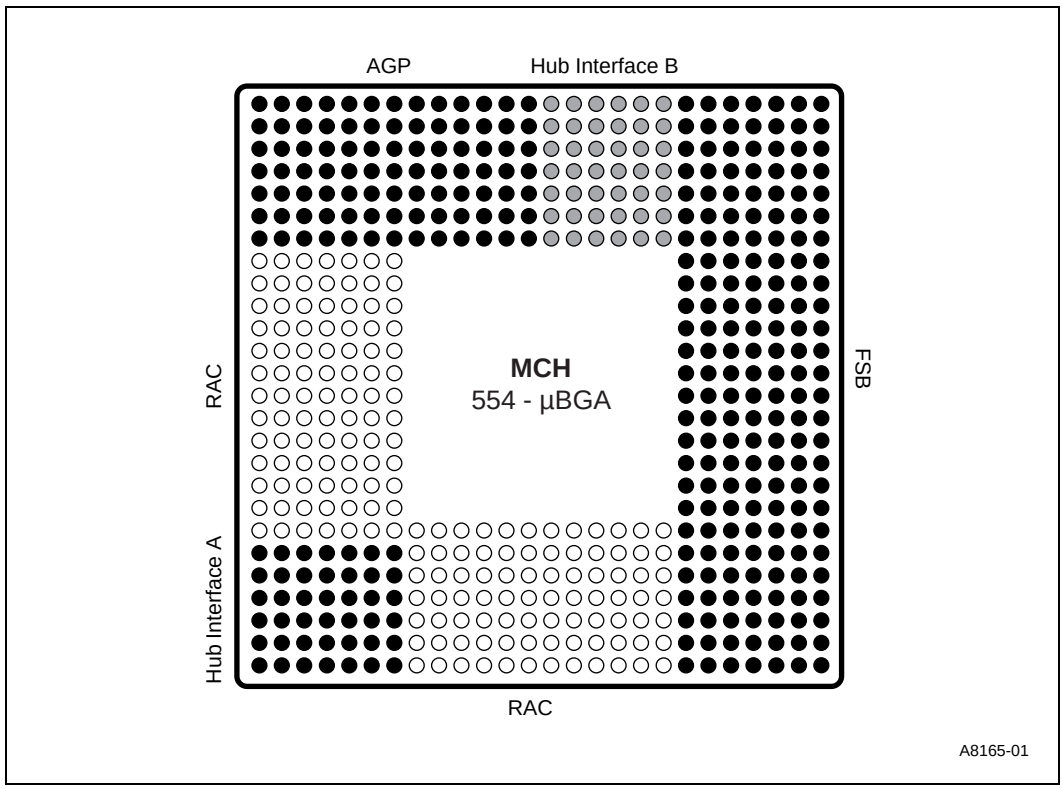


Figure 4-2. Top View - ICH 241 MBGA Quadrant Layout

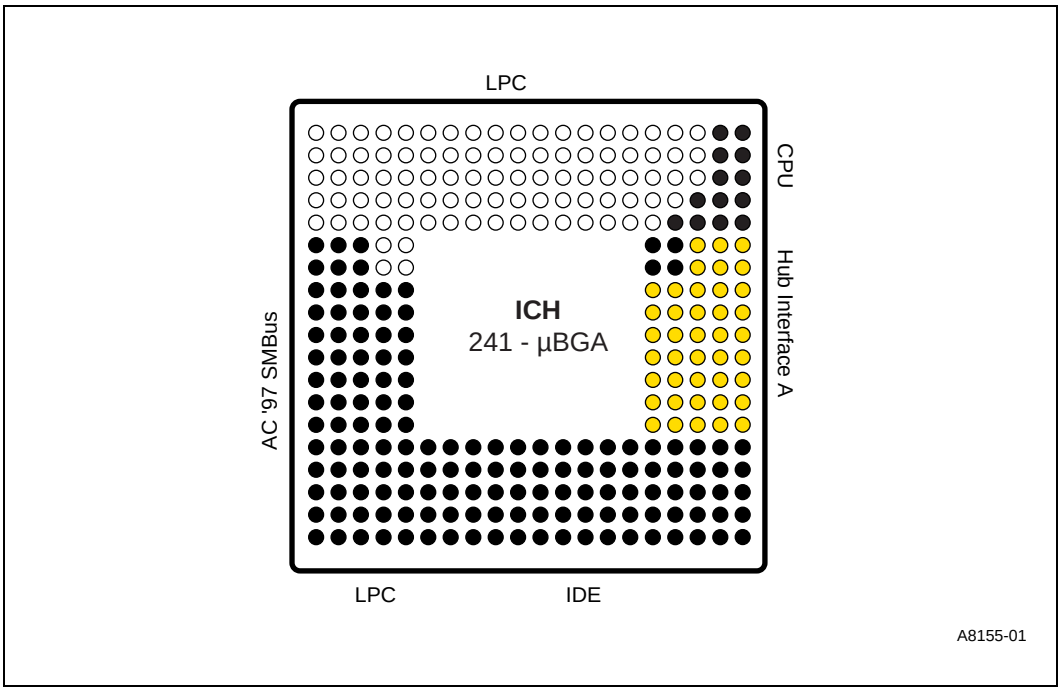


Figure 4-3. Top View - FWH Package

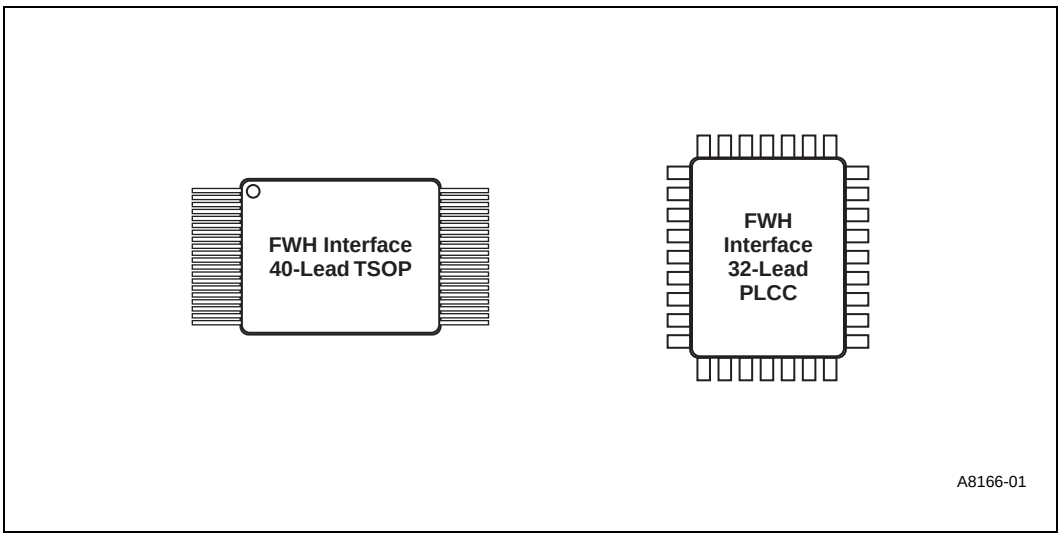


Figure 4-4. Top View - P64H 241 MBGA Quadrant Layout

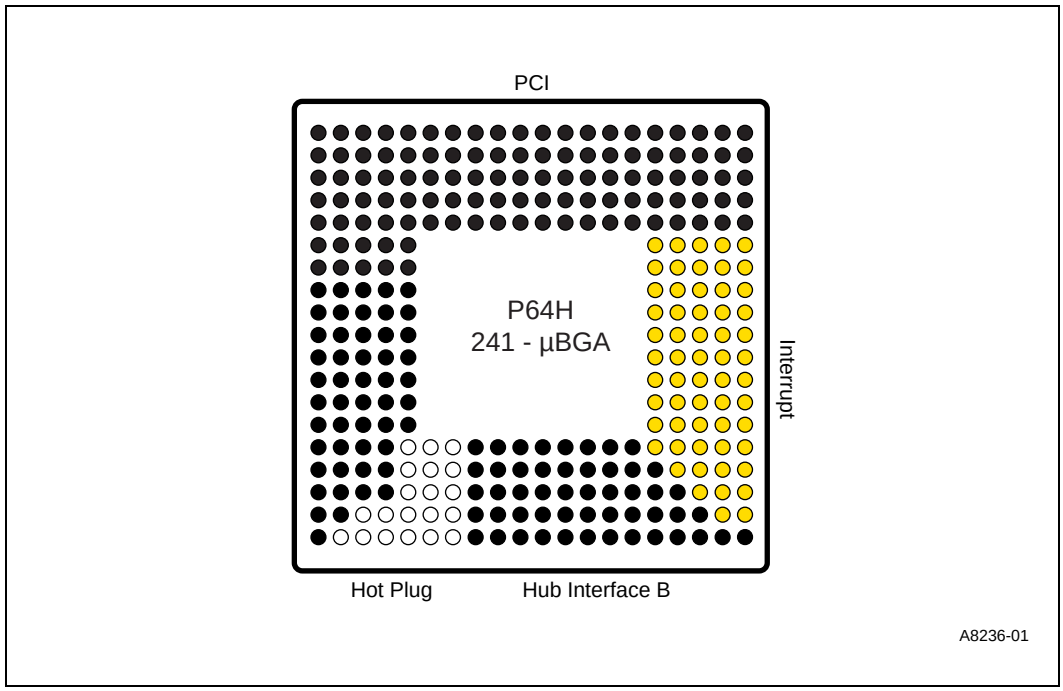
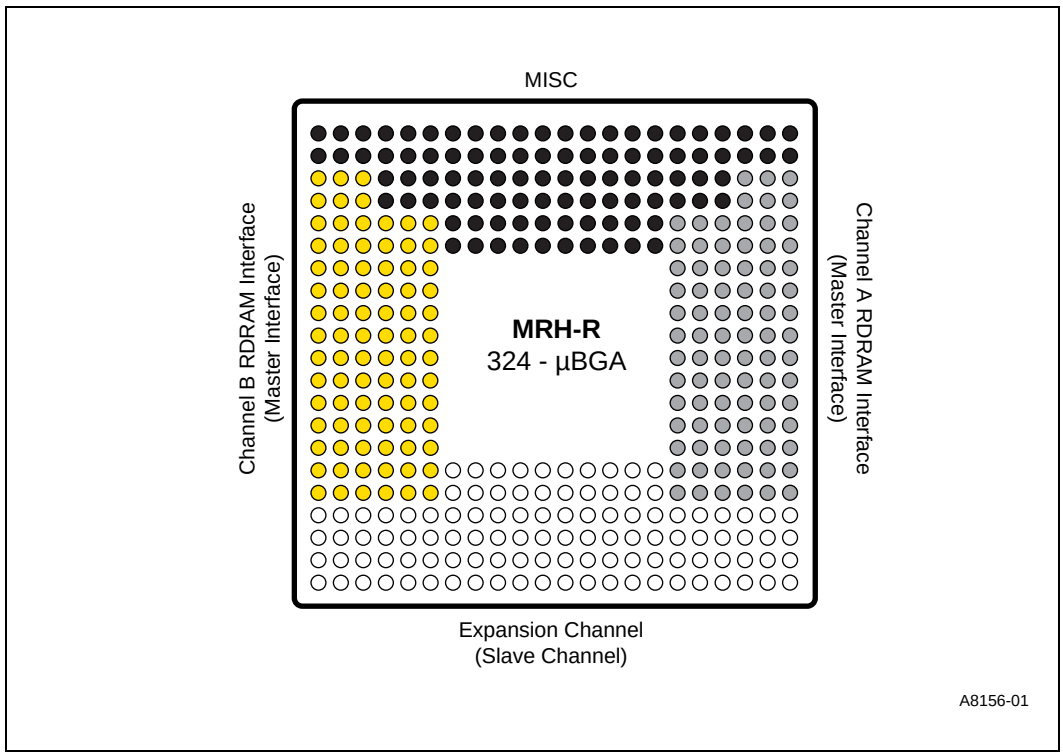


Figure 4-5. Top View- MRH-R 324 MBGA Quadrant Layout



Board Layout and Routing Guidelines 5

This section documents motherboard layout and routing guidelines for an Intel® 840 chipset-based system. For the component functionality information, refer to each component's respective specification.

Although layout and routing guidelines are provided, it is recommended that OEMs simulate all signals to ensure proper signal integrity and flight time. Complete signal integrity and timing simulation is important whether or not the design deviates from the following layout and routing guidelines.

5.1 General Recommendations

The nominal trace impedance used is 60 Ω ±10%. When calculating flight times, it is important to consider the minimum and maximum impedance trace based on the switching neighboring traces. Wider spaces between traces may be used since this can minimize trace-to-trace coupling, and reduce crosstalk.

All recommendations described in this document assume a 5 mil wide signal trace unless otherwise specified. If wider traces are used, the trace spacing must be adjusted accordingly (linearly). For example, it is recommended that AGP signals be routed with minimum of 5 mil traces on 20 mil spaces (ratio 1:4). An increase to 6 mil trace width, requires the trace spacing be adjusted to 24 mil, maintaining the 1:4 ratio.

These guidelines were generated based on eight- and 12-layer board stack-ups. Other stack-ups may be used, but thorough simulation is highly recommended.

5.2 Stack-up Requirement

5.2.1 Overview

The Intel 840 chipset requires a board stack-up with a 4.5 mil prepreg on the outer layer. This change in dimension (previously, typically 7 mil) is required because of the signaling environment used for Direct RDRAM*, AGP 2.0 and hub link. The RDRAM channel is designed for 28 Ω and mismatched impedance will cause signal reflections that will reduce voltage and timing margins. For example, with a 2X clock at 400 MHz operation, which equals a 1.25 ns sampling window, only 100 ps is allotted for total channel timing error. Channel error results not only from PCB impedance, but also PCB and Z0 process variation. Therefore, it is critical to attain the required 28 Ω impedance.

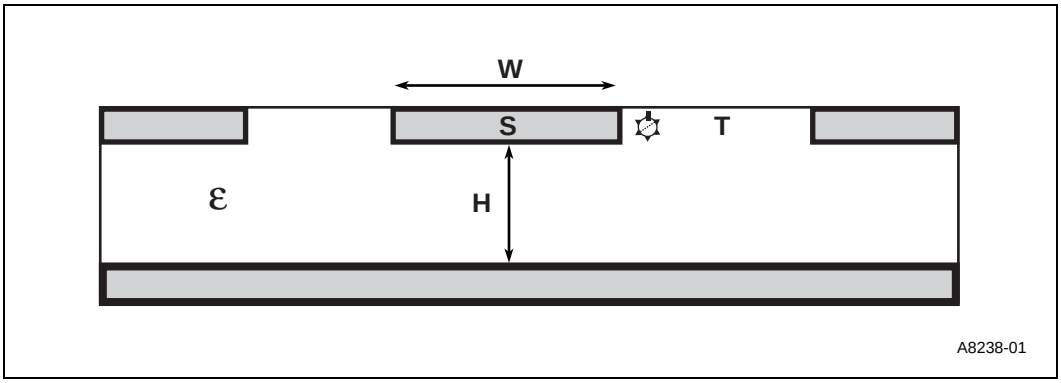
5.2.2 PCB Material

PCB tolerances determine Z0 variation. Those tolerances include trace width, prepreg thickness, plating thickness, and dielectric constant. See Figure 5-1. The prepreg type impacts the H tolerance and e_r tolerance, which includes single ply, two-ply, and resin content. To design to the correct Z0 variation, PCBs typically need to meet the following:

- Height tolerance ± 10% (~ 0.4 mil)
- Width tolerance ± 2.5% (~ 0.4 mil)
- e_r tolerance ± 5% (~0.2)

The stack-up impedance requirement must be 28 Ω ± 10%.

Figure 5-1. 28 Ω Trace Geometry



Steps to design and meet the tight tolerance requirements may include:

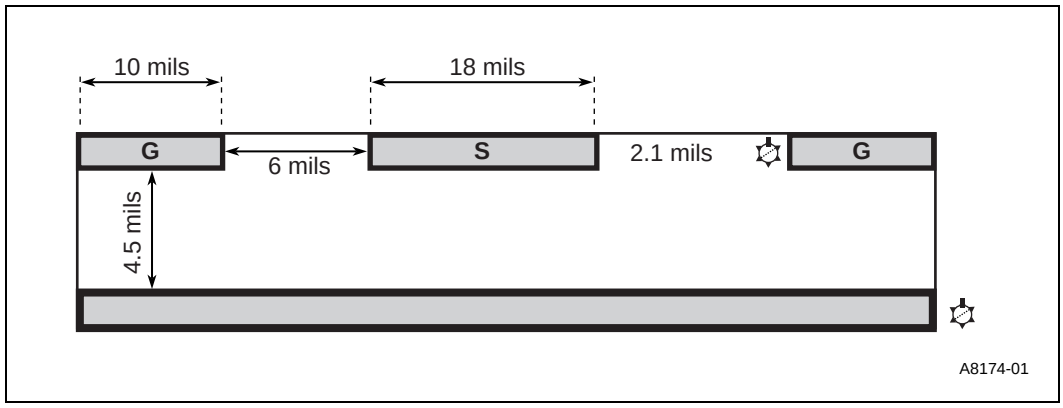
- Specify the material to be used.
- Calculate board geometry for the desired impedance - or use the example stack-up provided.
- Build test boards and coupons.
- Measure the board impedance using a TDR and follow the procedures in the *Impedance Test Methodology* document. This document is available on the Intel developer's web site: http://developer.intel.com/
- Measure board geometry with cross-section.
- Adjust design parameters and/or material as required.
- Build a new board, measure the key parameters and again be prepared to generate one or two board iterations.

5.2.3 Inner Layer Routing

Inner layer routing has many possible stack-up combinations. The initial TDR should fall within acceptable limits, 28 Ω ± 10%, with these parameters. It is important to consider the ground floods and stitching as well.

Figure 5-2 provides an example of the Stripline and Microstrip cross sections:

Figure 5-2. Microstrip Cross Section for 28 Ω Trace



5.2.4 Impedance Calculation Tools

3-D Field Solvers, such as those by HP, Ansoft, Sonnet, and Polar are the most accurate for impedance calculations. The Z calculators, based on equations (ZCALC*), are also reasonably accurate. The differences are shown:

Table 5-1. 3-D Field Solver vs. ZCALC*

	Example #1	Example #2	Example #3	Example #4	Example #5	Example #6
H	4.5	4.5	4.2	4.8	4.5	4.5
W	18	18	18	18	17	19
W1	18.1	18.1	18.1	18.1	17.1	19.1
T	1.4	2.8	1.4	1.4	1.4	1.4
ε_r	4.5	4.5	4.5	4.5	4.5	4.5
Results with Z0 (3D)	29.0	28.4	27.6	30.4	30.2	27.9
Results with Z0 (ZCALC)	29.1	28.7	27.7	30.4	3.02	28.0

5.2.5 Board Stack-Up

There are two board stack-ups shown, one for eight-layer platforms, shown in Figure 5-3, and the other for 12-layer platforms, shown in Figure 5-4. The additional prepreg thickness is recommended to accommodate the high-speed signal environment. For example: Direct RDRAM, MEC interface, AGP and hub interfaces.

There are two popular prepreg types:

- 7628 Cloth, 1 ply .007” when cured with 40% resin
- 2116 Cloth, 1 ply .0045” when cured with 53% resin

Although 7628 Cloth is more common, it is recommended that 2116 Cloth be used because it better accommodates the high speed signals impedance and layout requirements. Other board stack-ups can be achieved but it is important to maintain the traces on inner and outer layers as close to 60 Ω as possible. It is also important to maintain the 4.5 mil prepreg that is needed to keep the 18 mil RDRAM RSL traces at 28 Ω impedance.

Figure 5-3. 8-Layer Board Stack-up Example

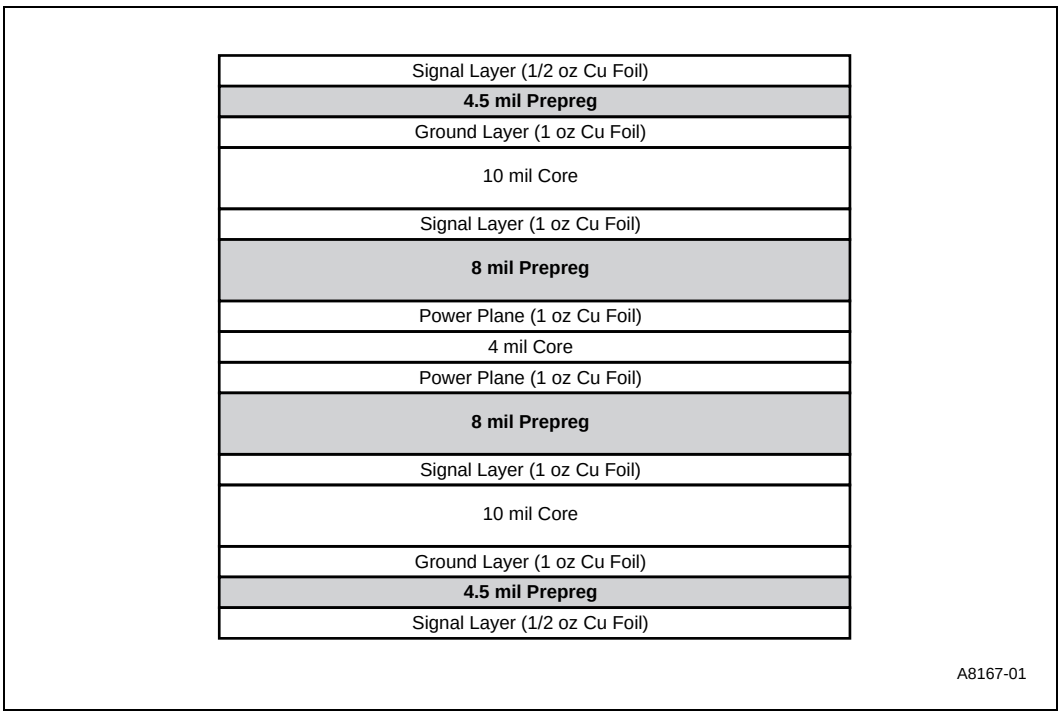
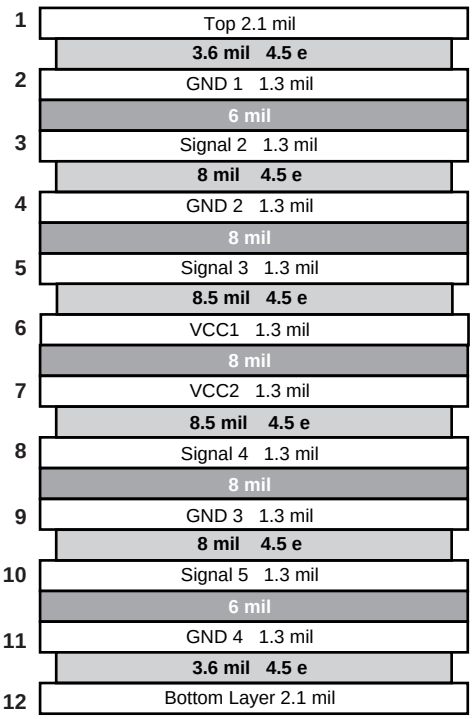


Figure 5-4. 12-Layer Board Stack-up Example



5.3 Power Distribution

Designs using the Pentium III processor require several different voltages. The following paragraphs describe some of the impact of two common methods used to distribute the required voltages. Refer to the *Flexible Motherboard Power Distribution Guidelines* for more information on power distribution.

The most conservative method of distributing these voltages is for each of them to have a dedicated plane. When any of these planes are used as an “AC ground” reference for traces to control trace impedance on the board, then the plane needs to be AC coupled to the system ground plane. This method may require more total layers in the PCB than other methods. 1 ounce/ft^2 thick copper is recommended for all power and reference planes.

A second method of power distribution is to use partial planes in the immediate area needing the power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing area that can be used to route traces. These partial planes may also change the impedance of adjacent trace layers. (For instance, the impedance calculations may have been done for microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.)

5.3.1 Reference Planes and PCB Stackup

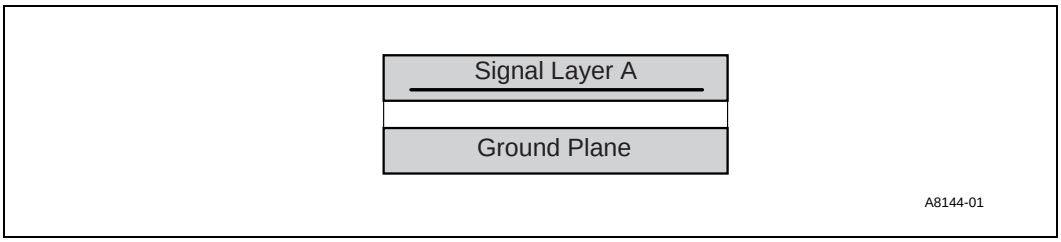
The type and number of layers for the PCB need to be chosen to balance many requirements. Many of these requirements include:

- The maximum trace resistance for AGTL+ signal paths should not exceed 2 Ω. Depending on the trace width chosen and PCB vendor's process tolerance, this may require 1 ounce/ft^2 thick copper instead of 1/2 ounce/ft^2 thickness. A higher trace resistivity increases the voltage drop along the trace, which reduces the falling edge noise margin.
- Providing enough routing channels to support the minimum and maximum timing requirements of the components
- Providing stable voltage distribution for each of the components
- Providing uniform impedance for the processor bus and other signals as needed
- Providing a ground plane under the principal component side of the baseboard, preferably under both sides when active components are mounted on both sides
- Minimizing coupling/cross-talk between the networks
- Minimizing RF emissions
- Maximizing PCB yield
- Minimizing PCB cost
- Minimizing cost to assemble PCB

The following baseboard layout requirements should help processor signal integrity requirements and reduce the amount of Simultaneous Switching Output (SSO) effects experienced.

It is *strongly recommended* that baseboard stackup be arranged such that AGTL+ signals are referenced to a ground (VSS) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path that can lead to large SSO effects that degrade timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will expose the platform to a risk that is very hard to predict in pre-layout simulation. Figure 5-5 shows the ideal case where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

Figure 5-5. One Signal Layer and One Reference Plane



When it is not possible to route the entire AGTL+ signal on a single VSS referenced layer, there are methods to reduce the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 5-6). Figure 5-7 shows another method of minimizing layer switch discontinuities, but may be less effective than Figure 5-7. In this case, the signal still references the same type of reference plane (ground). In such a case, it is important to connect the two ground planes together with vias in the vicinity of the signal transition via.

Figure 5-6. Layer Switch with One Reference Plane

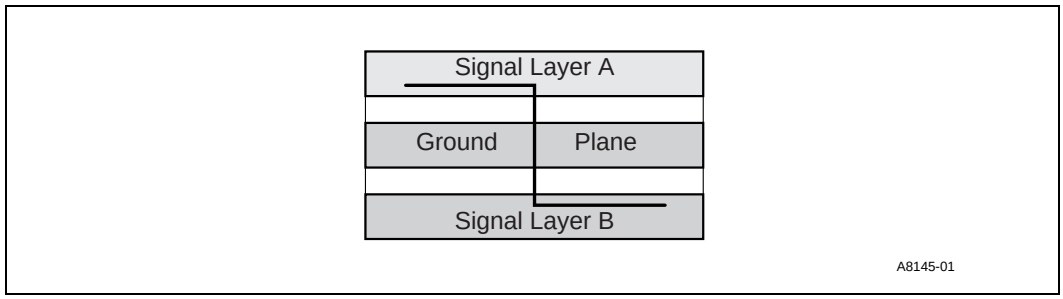
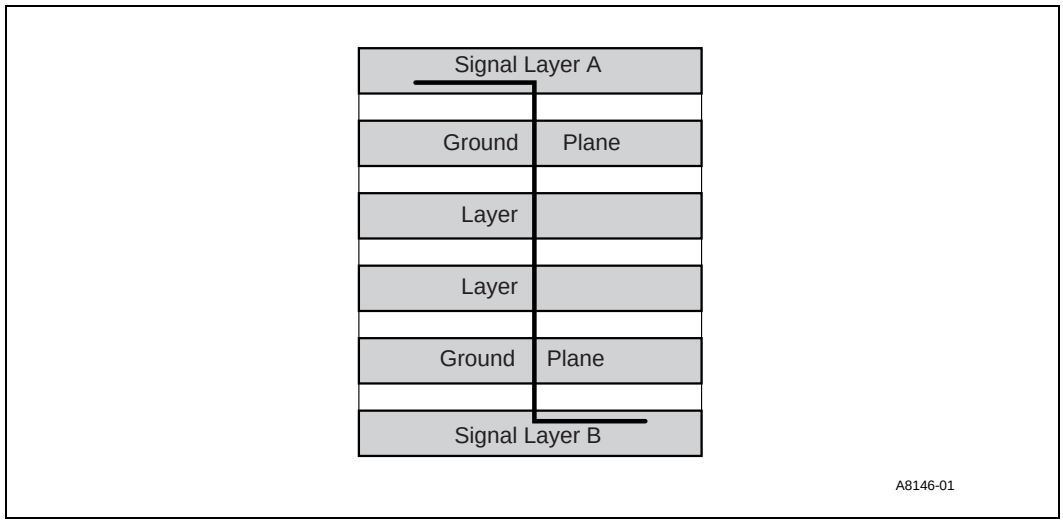


Figure 5-7. Layer Switch with Multiple Reference Planes (same type)



When routing and stackup constraints require that an AGTL+ signal reference V_{CC} or multiple planes, special care must be given to minimize the SSO impact to timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling wherever the transitions occur. Such decoupling should, again, be in the vicinity of the signal transition via and use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps it is recommended to space the V_{SS} and V_{CC} vias as close as possible and/or use dual vias since the via inductance may sometimes be higher than the actual capacitor inductance.

Figure 5-8. One Layer with Multiple Reference Planes

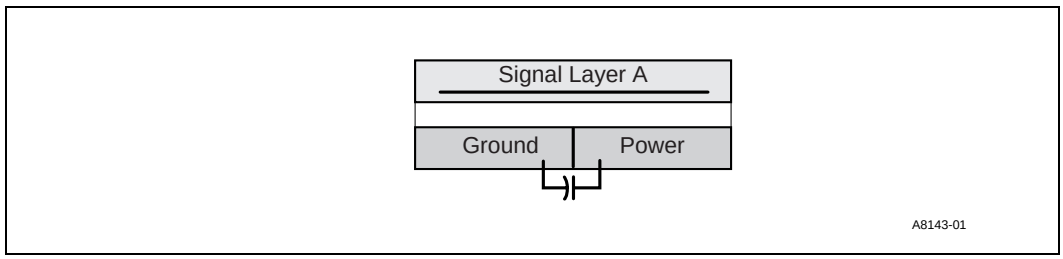
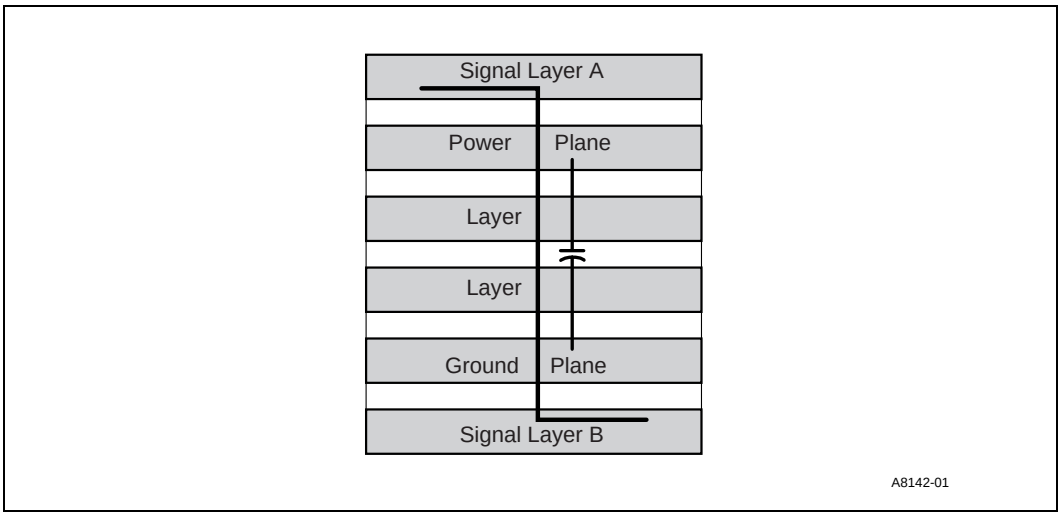


Figure 5-9. Layer Switch with Multiple Reference Planes



5.3.1.1 High Frequency Decoupling

This section contains several high frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will very likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities may also occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across V_{CC_CORE} and ground interface on the baseboard will minimize the discontinuity in the signal's reference plane at this junction. Please note that these additional high-frequency decoupling capacitors are in addition to the high-frequency decoupling already on the processor.

Transmission line geometry also influences the return path of the reference plane. The following are decoupling recommendations that take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling between all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 840 MCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

5.4 Decoupling Guidelines for PGA370 Designs

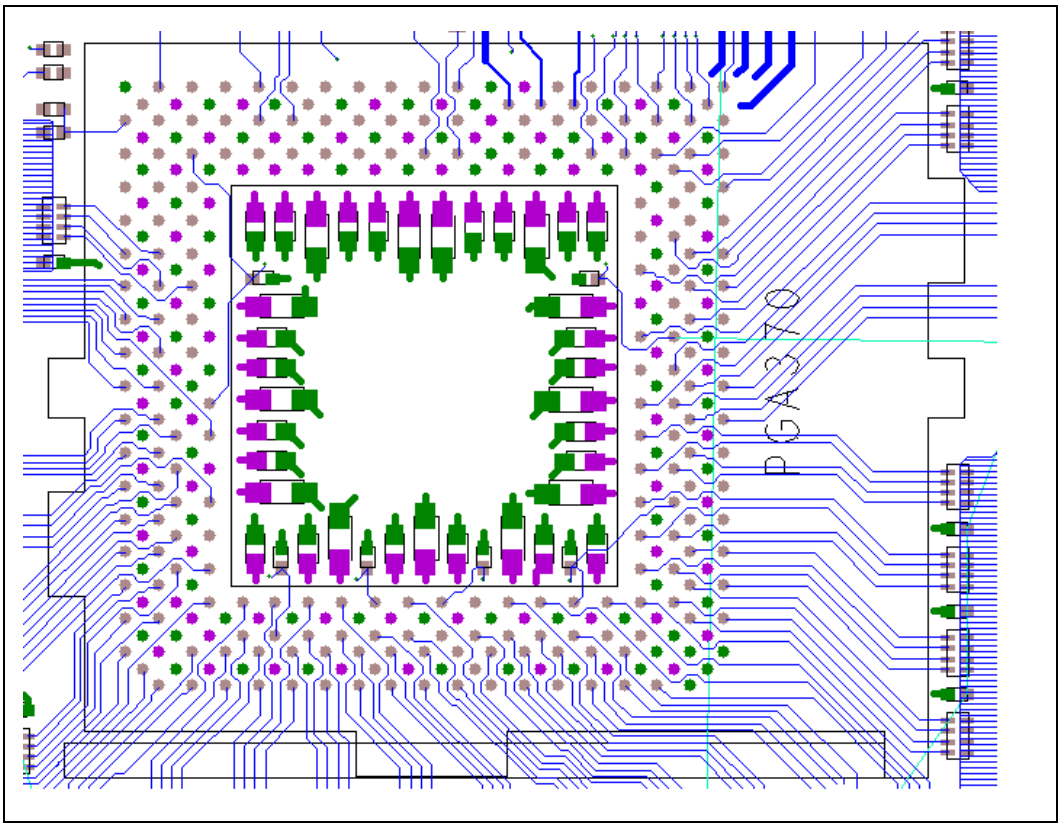
These are decoupling guidelines for PGA370 designs and are estimated to meet VRM8.4 1.5 V flexible motherboard requirements (V_{CC}=1.6 V, I_{CC} = 0.8 - ~18.4 A).

5.4.1 V_{CC_CORE} Decoupling Design

- 10 or more 4.7 µF capacitors in 1206 packages.

All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between V_{CC_CORE}/V_{SS} power pins, as shown in Figure 5-10 below.

Figure 5-10. Capacitor Placement on the Motherboard



5.4.2 V_{TT} Decoupling Design

Decoupling guidelines: 2 ea. minimum 4.7 µF capacitors in 1206 package and 3 ea. minimum 0.1 µF in 0603 package.

5.4.3 V_{REF} Decoupling Design

- Four - 0.1 µF capacitors in 0603 package placed near the V_{REF} pins (within 500 mils).

5.5 Thermal/EMI Differences

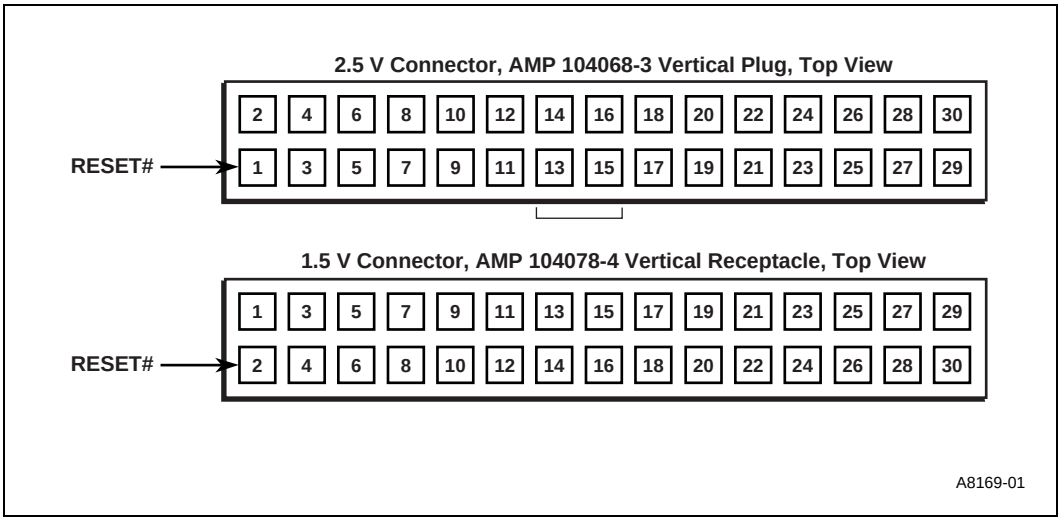
Heatsink requirements will be different for FC-PGA processors from previous processors using PPGA packaging. The current flexible motherboard specification for 256K FC-PGA Pentium III processor calls for 37.4 W.

- Increased power density for Pentium III processor (approximately 51.5 W/cm^2)
- Different thermal design verification for FC-PGA compared to PPGA packaged processors. Pentium III processors are specified using T_J versus T_{CASE} (used with Intel® Celeron™ processors).
- New heatsink for FC-PGA package which is not backwards compatible with PPGA processors.
- New heatsink clips for FC-PGA processor heatsinks.

5.5.1 Debug Port Changes

Due to the lower voltage technology employed with the FC-PGA Pentium III processor, changes are required to support the debug port. Previously, the test access port (TAP) signals used 2.5 V logic. This is the case with the Intel Celeron processor in the PPGA package. The Pentium III processor utilizes 1.5 V logic levels on the TAP. As a result, a new ITP connector is to be used on flexible PGA370 designs. The new 1.5 V connector is the mirror image of the older 2.5 V connector. Either connector will fit into the same printed circuit board layout. Just the pin numbers would change, as can be seen in the drawing below.

Figure 5-11. TAP Connector Comparison



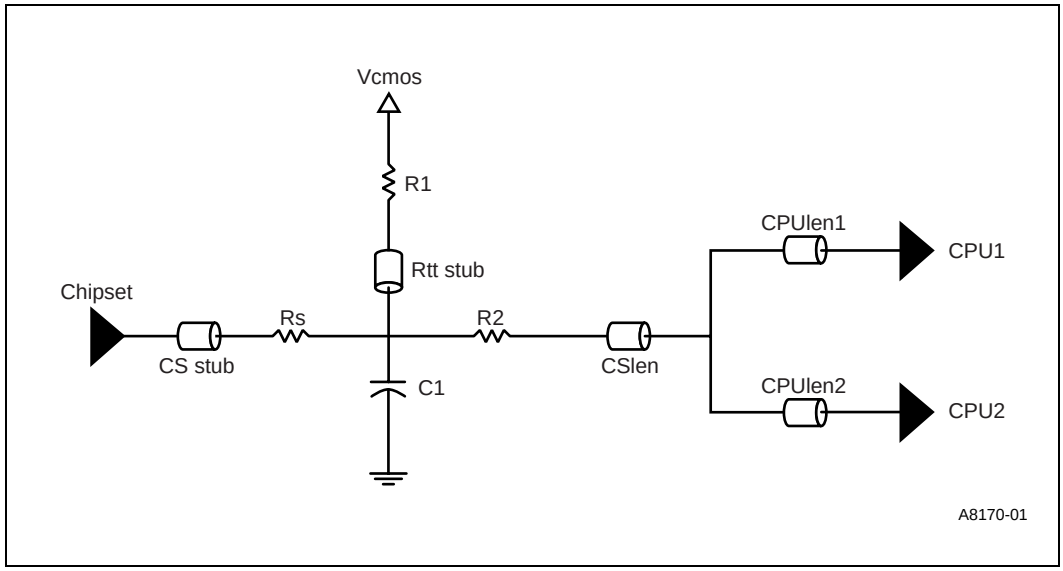
Caution: The FC-PGA Pentium III processor requires an in-target probe (ITP) with a 1.5 V tolerant buffer. Previous ITPs are designed to work with higher voltages and may damage the processor if they are connected to an FC-PGA Pentium III processor.

See the processor EMTS for more information regarding the debug port.

5.6 SMI# Layout Guidelines

For design assistance with reducing or eliminating the non-monotonic rising edge of the SMI# signal, refer to the simulated topologies for UP/DP FC-PGA, as shown in Figure 5-12. The Pentium III processor SMI# erratum is documented in the latest specification update and the erratum will be fixed in the B-step silicon. Please refer to the Pentium III processor specification update for additional information on the steppings affected by this anomaly.

Figure 5-12. Topology Simulated



Parameter	Minimum	Maximum
CS stub	0.25"	1.5"
Rtt stub	0"	1.5"
CSlen	0.25"	10"
CPUlen1	0.25"	10"
CPUlen2	0.25"	10"

All simulations assume:

- 60 Ω ±10% motherboard manufacturing impedance
- 5:15 trace width to spacing ratio
- R1 = 150 Ω ± 5%
- Rs = 56 Ω ± 5%
- R2 = 33 Ω ± 5%
- C1 = 100 pF ± 5%

Dual (FC-PGA) Intel® Pentium® III Processors 6

This chapter discusses using the FC-PGA Intel® Pentium® III processor in a dual processor system design. Chapter 7 discusses single processor design.

6.1 Two-Way FC-PGA Pentium® III Processors and Intel® 840 Chipset Layout

The Intel Pentium III processor is the most powerful and advanced member of Intel's family of P6 processors. The Intel 840 chipset has been designed to provide a high-performance memory, Advanced Graphics Port (AGP), and I/O subsystem to support Intel processors interfacing to the SC242 connector and FC-PGA Pentium III processors. The processors implement a synchronous, latched bus protocol that allows a full clock cycle for signal transmission and a full clock cycle for signal interpretation and generation. This protocol simplifies interconnect timing requirements and supports 133 MHz system bus designs using conventional interconnect technology. The processor system bus operates using Assisted Gunning Transceiver Logic, or AGTL+.

This chapter provides information needed to design a dual FC-PGA Pentium III processor (133 MHz system bus) system using the Intel 840 chipset. This layout guideline *does not* support designs using other chipsets. This section provides guidelines and methodologies that are to be used with good engineering practices. See the *Pentium® III Processor for the PGA370 Socket at 500 MHz to 1 GHz* datasheet and the Intel 840 chipset documents for component-specific electrical details. Intel strongly recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design.

For additional details, reference the following documents:

- *Pentium® III Processor for the PGA370 Socket at 500 MHz to 1 GHz* datasheet (order number 245264)
- *CK98 Clock Synthesizer/Driver Specification*
- *CK133 Clock Synthesizer/Driver Specification*
- *Pentium® II Processor Developer's Manual* (order number 243341)

6.2 Definition of Terms

Table 6-1. Definition of Terms (Sheet 1 of 2)

Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. This results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock-to-output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Cross-talk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • **Backward Cross-talk** - coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. • **Forward Cross-talk** - coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. • **Even Mode Cross-talk** - coupling from multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • **Odd Mode Cross-talk** - coupling from multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Flight Time	A term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as the time difference, between a signal at the input pin of a receiving agent crossing V_{REF} (adjusted to meet the receiver manufacturer’s conditions required for AC timing specification; i.e., ringback, etc.) and the output pin of the driving agent crossing V_{REF}, if the driver was driving the TEST load used to specify the driver’s AC timings.
GTL+	The bus technology used by the Pentium Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See the *Pentium® II Processor Developer’s Manual* for more details of GTL+.
M_{ADJ}	Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs when multiple data bits switch in the same cycle. The adjustment factor includes such mechanisms as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise.
Network	The trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	Distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors.
Overdrive Region	The voltage range, at a receiver, located above and below V_{REF} for signal integrity analysis. See the *Pentium® II Processor Developer’s Manual* for more details.

Table 6-1. Definition of Terms (Sheet 2 of 2)

Overshoot	Maximum voltage allowed for a signal at the processor core pad. See each processor's datasheet for overshoot specification.
Pin	A feature of a logic package used to connect the package to the 370-pin FC-PGA socket.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, etc. See each processor's datasheet for ringback specifications.
Settling Limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See each processor's datasheet for settling limit specifications.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO) Effects	Refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high- to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "pushout"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, terminating at agent pads.
Undershoot	Maximum voltage allowed for a signal to extend below V_{SS} at the processor core pad. See each processor's datasheet for undershoot specifications.
Victim	A network that receives a coupled cross-talk signal from another network is called the victim network.
V_{REF} Guardband	A guardband (ΔV_{REF}) defined above and below V_{REF} to provide a more realistic model accounting for noise such as cross-talk, V_{TT} noise, and V_{REF} noise.

6.2.1 AGTL+ Design Guideline

The following step-by-step guideline was developed for systems based on two processor loads and one Intel 840 MCH load.

The guideline recommended in this section is based on experience developed at Intel while developing many different P6 family (Pentium Pro, Pentium II and Pentium III) processor-based systems. Begin with an initial timing analysis and topology definition. Perform pre-layout analog simulations for a detailed picture of a working “solution space” for the design. These pre-layout simulations help define routing rules prior to placement and routing. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

1. Begin with an initial timing analysis and topology definition.
2. Perform pre-layout analog simulation for a detailed picture of a working “solution space” for the design. These pre-layout simulations help define routing rules prior to placement and routing.
3. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis.
4. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

Guideline Methodology:

- Initial timing analysis
- Determine general topology, layout, and routing
- Pre-layout simulation
  - — Sensitivity sweep
  - — Monte Carlo analysis
- Place and route board
  - — Estimate component-to-component spacing for AGTL+ signals
  - — Layout and route board
- Post-layout simulation
  - — Interconnect extraction
  - — Inter-symbol interference (ISI), cross-talk, and Monte Carlo analysis
- Validation
  - — Measurements
  - — Determining flight time

6.2.2 Initial Timing Analysis

Intel highly recommends performing simulations as part of the board design process. This includes pre-layout simulations to provide a passing and robust solution space. Run post-layout simulations based on the extracted board layout to verify that the layout meets timing and noise requirements. Simulations are required for all designs that deviate from the recommended layout guidelines.

Table 6-2 lists the AGTL+ component timings of the processors and Intel 840 MCH defined at the pins. These timings are for **reference only**; obtain processor and chipset component specifications from the datasheets.

Table 6-2. AGTL+ Component Timings

IC Parameters	Intel® Pentium® III Processor (FC-PGA) Core at 133 MHz Bus	Intel® 840 MCH	Notes
Clock to Output maximum (T_{CO_MAX})	3.25 ns	3.00 ns	1,2
Clock to Output minimum (T_{CO_MIN})	0.4 ns	0.25 ns	1,2
Setup time (T_{SU_MIN})	0.95 ns	1.85 ns	1,2
Hold time (T_{HOLD})	1.0 ns	0.60 ns	1,2

NOTES:
1. Numbers in table are for reference only. These timing parameters are subject to change. Please check the appropriate component documentation for valid timing parameter values.
2. T_{SU_MIN} = 1.85 ns assumes the Intel 840 MCH sees a minimum edge rate equal to 0.3 V/ns.

Table 6-3 and Table 6-4 show a recommended setup and hold margin timing budget for a 133 MHz system bus supporting two-way FC-PGA Pentium III processor operation with the Intel 840 chipset. The recommended topologies should support the maximum and minimum flight times suggested in these tables. The processor and chipset timing values used in these tables are for reference only and should be taken from the latest component datasheet.

The maximum and minimum flight times suggested for this topology make certain assumptions as described below. Any deviations from these assumptions must be analyzed to verify that the recommended topology and flight times are still valid. These flight times also assume that the component AGTL+ signal quality requirements are met or derated properly. See the appropriate component documentation for more details.

These timing tables make assumptions about the clock skew and jitter and are not meant to be clock-specific; e.g., clock driver skew is minimized by ganging the outputs together at a clock driver device that supports this operation. Clock skew and jitter values are dependent on the components and clock distribution method chosen for a particular design and *must* be budgeted into these timing equations as appropriate for each design. Note that the M_{ADJ} factor accounts for multi-bit switching effects that may worsen the flight time and/or signal quality and are not always seen in simulation. This factor is highly dependent on how high-speed design practices are implemented on the baseboard (e.g., decoupling, signal return paths) and should be budgeted accordingly in each design.

The following timing equations were used to calculate the minimum and maximum flight times:

Processor driving:

$$T_{FLT–MAX} \leq Period - T_{CO–MAX} - T_{SU–MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ} + CLK_{SHFT}$$

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ} + CLK_{SHFT}$$

Chipset driving:

$$T_{FLT–MAX} \leq Period - T_{CO\_MAX} - T_{SU–MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ} - CLK_{SHFT}$$

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ} - CLK_{SHFT}$$

Table 6-3 gives an example of AGTL+ initial maximum flight time and Table 6-4 gives an example of a minimum flight time calculation for a 133 MHz, two-way FC-PGA Pentium III processor and Intel 840 chipset system bus. Note that assumed values for clock skew and clock jitter are used.

Note: Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.

Table 6-3 and Table 6-4 assume:

- CLK_{SKEW} = 0.15 ns
- CLK_{JITTER} = 0.25 ns
- CLK_{SHIFT} = 0.26 ns

Note: These values are derived from the assumption that three host clocks are tied together (ganged), resulting in no pin-to-pin skew at the clock driver output pins. PCB clock routing skew is assumed to be 150 ps. System timing budget must assume 0.175 ns of clock driver skew if output are not tied together and clock driver that meets the CK98W/S or CK133 Clock Synthesizer/Driver Specification is being used. Some clock driver components may not support ganging the outputs together. Be sure to verify with your clock component vendor before ganging the outputs.

See the respective processor's datasheet, appropriate Intel 840 chipset documentation, and *CK133 Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Exact details of host clock routing topology are still under investigation and will be documented in the future release of this document. The new CK98W/S specification, with tighter clock jitter at 0.150 ns, is also available for designs that need tighter control on jitter.

Table 6-3. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	CLK Period[2]	T_{CO_MAX}	T_{SU_MIN}	CLK_{SKEW}	CLK_{JITTER}	CLK_{SHIFT}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor	Processor	7.5	3.25	0.95	0.15	0.25	0.0	0.40	2.5
Processor	840 MCH	7.5	3.25	1.85	0.15	0.25	0.26	0.40	1.86
840 MCH	Processor	7.5	3.00	0.95	0.15	0.25	0.26	0.40	2.49

NOTES:
1. All times are in nanoseconds.
2. BCLK period = 7.5 ns @ 133 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SSO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Cross-talk on the PCB and internal to the package can cause variation in the signals.

There are additional effects that may not necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include the effective board propagation constant (S_{EFF}), which is a function of:

- Dielectric constant (ε_r) of the PCB material.
- The trace type connecting the components (stripline or microstrip).
- The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a component of the flight time but not necessarily equal to the flight time.

Table 6-4. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	CLK_{SKEW}	T_{CO_MIN}	CLK_{SHIFT}	Recommended T_{FLT_MIN}
Processor	Processor	1.0	0.15	0.4	0.0	0.75
Processor	840 MCH	0.60	0.15	0.4	0.26	0.61
MCH	Processor	1.0	0.15	0.25	0.26	0.64

NOTE: All times in nanoseconds.

6.2.3 Dual Processor General Topology

Table 6-5 below provides segment descriptions and length recommendations for the simulated bus topology shown in Figure 6-1. Segment lengths are defined at the pins of the devices or components. The signal routing assumes a **four-signal layer** (six or eight-layer motherboard) ATX form factor platform. For dual processor FC-PGA/Intel 840 chipset designs, a termination device must be placed in the unused socket when only one processor is populated. To ensure signal integrity requirements, it is required that all system bus signal segments (CPU_{len}, CS_{len}) be referenced to the ground plane for the entire route. If multiple ground plane references are used, then the ground planes should be stitched together with vias between all the ground planes.

Figure 6-1. Intel® Pentium® III Processor – Dual Processor Configuration

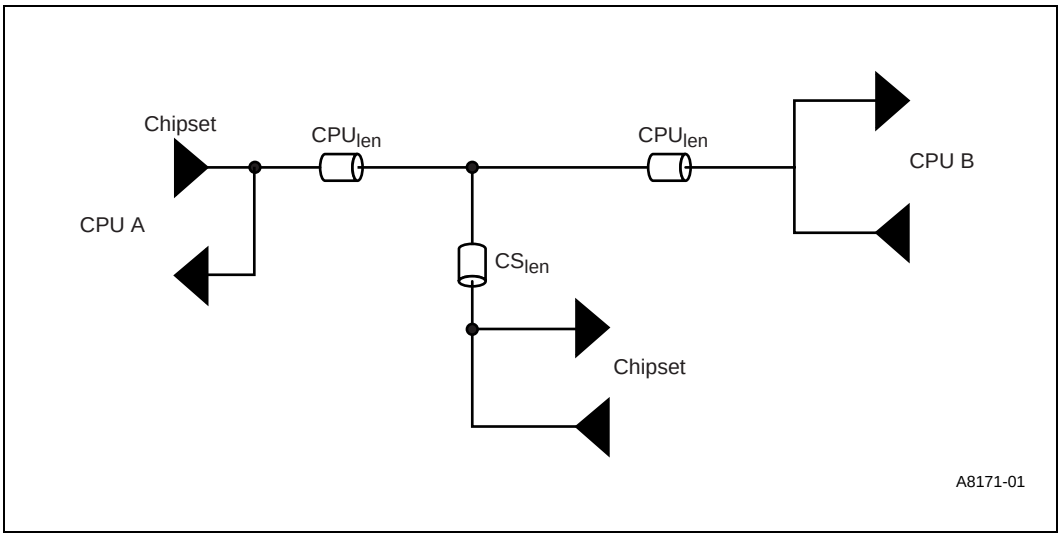


Table 6-5. Segment Descriptions and Lengths for Figure 6-1

Parameter	Min length (inches)	Max length (inches)
CPU_{len}	2.75	3.75
CS_{len}	2.25	2.75

All simulations assume the following:

- V_{TT} is maintained at 1.5 V ± 3%
- V_{REF} is maintained at 2/3 V_{TT} ± 50 mV
- Motherboard impedance, Zo, is 60 Ω ± 10%
- Signal propagation delay is between 1.93 ns/ft and 2.057 ns/ft on baseboard
- The dielectric constant, ε_r, is 4.5
- The tracewidth-to-spacing ration is 5:15
- The CPU stub length of the same net must be matched with 0.25”
- R_{TT} = 68 Ω ± 15% on the processor die

6.2.4 Cross-talk Routing Guidelines

To ensure adequate levels of cross-talk, follow these trace width spacing recommendations on the baseboard:

Intragroup AGTL+	5:15
Intergroup AGTL+	5:15
AGTL+ to non-AGTL+	5:20 or 6:24

Intragroup AGTL+ refers to AGTL+ signals in the same group. Intergroup AGTL+ refers to AGTL+ signals in different groups. For a signal listing of AGTL+ groups, see Section 3.4 in the *Pentium® Pro Family Developer's Manual*, Volume 1. An example of a non-AGTL+ signal is CMOS.

6.3 Processor Overshoot/Undershoot Limits

For the FC-PGA Pentium III processor, the maximum absolute overshoot voltage limit has been increased from 2.0 V to 2.18 V. However, this value is still based on very preliminary studies and is subject to change. Refer to the processor datasheet for more information on overshoot specifications. There is also a time dependent, non-linear overshoot and undershoot requirement that is dependent on the amplitude and duration of the overshoot/undershoot. Any deviations from the layout guidelines recommended in this chapter require additional overshoot/undershoot verification in order to ensure that these specifications are met.

6.4 Wired-OR Signals

There are six "wired-OR" AGTL+ signals that can be driven by more than one agent simultaneously. When a signal is asserted (driven electrically low) by two agents on the same clock edge, the two falling wave fronts will meet at some point on the bus. This can create a large undershoot and ringback. Pay special attention during the layout and validation of these signals to prevent signal quality violations. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

6.5 Signal Return Path Considerations

Adequate signal return path is very important for maintaining signal quality and timing margin for a high-speed bus such as AGTL+. Failure to address these effects may result in excessive signal flight time push-out, overshoot/undershoot, and ringback violations. The best way to maintain a high-speed signal return path is to reference a single ground plane (preferred) or single power plane that is continuous for the entire length of the signal route. Avoid routing layer switches and multiple reference planes as these create discontinuities in the signal return path. When routing layer switches is unavoidable, minimize possible adverse effects on return path by making sure the signal still references either the same plane or same type of reference plane. When a layer switch occurs where the signal references the same type of plane located on another layer, then vias should be inserted in the immediate vicinity of the layer switch to allow the return current to traverse from one plane to another. When a layer switch occurs where the signal references a different type of plane located on another layer, then place fast-response decoupling capacitors in the immediate

vicinity of the layer switch. Fast-response decoupling caps should also be placed in the immediate vicinity of any partial plane breaks when being used as a signal's reference plane. Ideally, the signal should not have any reference plane breaks cutting across the entire signal path.

For additional details on return path considerations, refer to "Power Distribution" on page 5-5.

6.6 Intel Pentium III Processor (FC-PGA) Pull-Up Values

Table 6-6 documents pull-up resistor values for Pentium III processor signals in a DP design and should be used as a guideline. The specific value should be calculated for each design. In a two-way system, dual pull-ups are required on each of the PICD[1:0] signals, and should be placed near the two extreme ends of the trace. Pull-up resistors for CPU CMOS outputs should near the CPU. For dual processor designs, terminate the PICD[1:0] signals at the end of the trace.

Table 6-6. Pull-Up Values

Signal	Resistor[1]	Signal	Resistor[1]
BSEL[1:0]	1 KΩ[2]	STPCLK#	150 Ω
FERR#	150 Ω	INIT#	150 Ω
TDO	150 Ω	PREQ#	200-330 Ω
A20M#	150 Ω	TCK	1.0 KΩ
IGNNE#	150 Ω	TMS	1.0 KΩ
LINT0/INTR	150 Ω	TDI	330 Ω
LINT1/NMI	150 Ω	PICD[1:0]	300-330 Ω
SMI	150 Ω	PWRGOOD[3]	150-330 Ω
SLP	150 Ω		

NOTE:
1. Unless noted, the signals listed should be pulled-up to 1.5 V.
2. BSEL[1:0] must be pulled up to 3.3 V.
3. PWRGOOD must be pulled-up to 2.5 V.

6.7 APIC / CMOS Bus

6.7.1 Two-way FC-PGA and Intel 840 Chipset APIC Bus Layout Guidelines

Figure 6-2 shows the layout guidelines for two-way Pentium III processor 256K FC-PGA systems based on the Intel 840 chipset. These guidelines are still preliminary, but simulations suggest that this daisy-chain, dual-ended termination topology and corresponding segment lengths will support timing and signal quality requirements for a 16.67 MHz bus frequency. Intel recommends APIC and CMOS bus simulation and good layout practices.

Figure 6-2. PICD[1:0] Two-way Topology

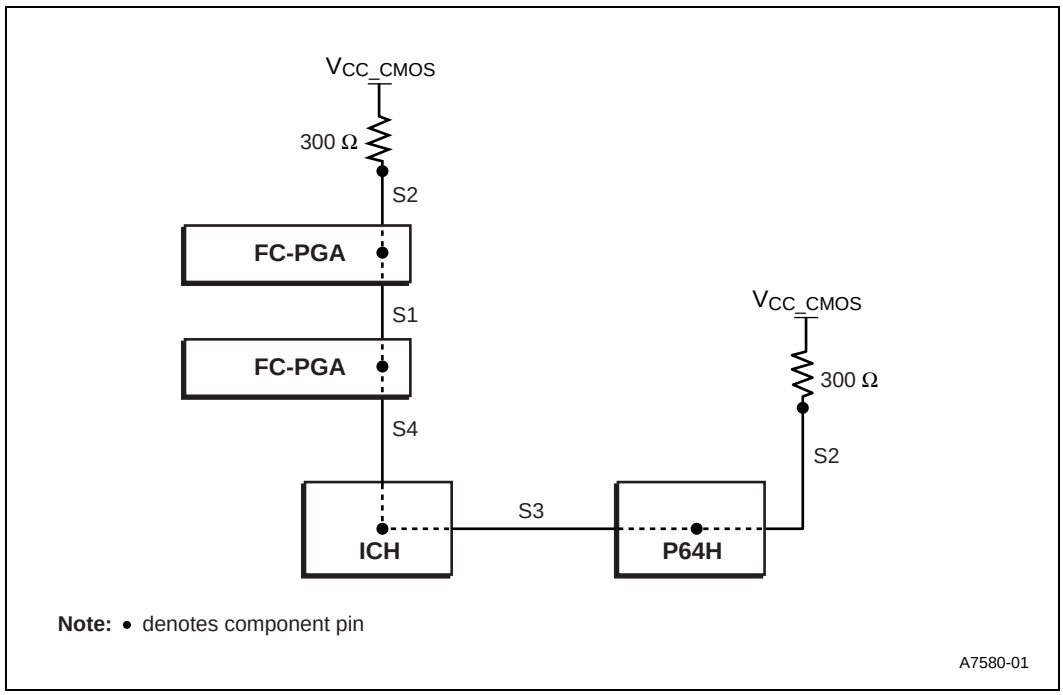


Table 6-7. PICD[1:0] Two-way Topology Segment Lengths

Length	Min (in inches)	Max (in inches)
S1	7	18
S2	0.25	1.0
S3	7	16
S4	9.5	19.5

6.8 Processor THERMTRIP# Pin Connection

PGA370 socket design implements the following connection for the THERMTRIP# pin between the two processors. Platform designs that do not use THERMTRIP# sensing can leave the processor THERMTRIP# pins unconnected. The corresponding THRM# pin on the ICH must be pulled-up to 3.3 V via a 1 KΩ resistor. The ICH THRM# pin must not be connected to any of the processor's THERMTRIP# pins directly.

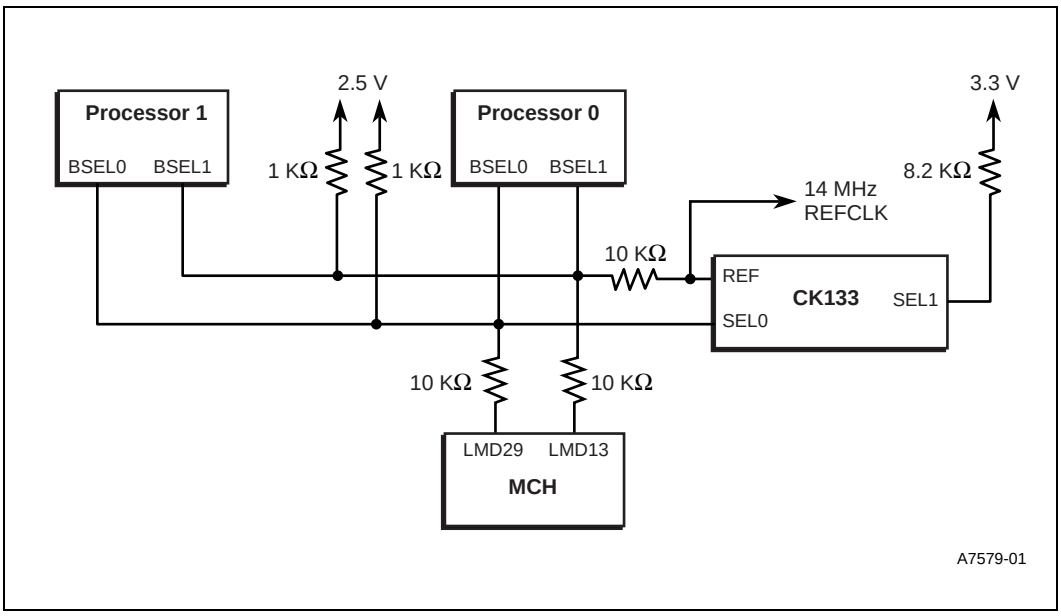
6.9 BSEL[1:0] Implementation

The Pentium III processor utilizes the BSEL1 pin to select either the 100 MHz or 133 MHz host bus frequency setting from the clock synthesizer. While the BSEL0 signal is still connected to the PGA370 socket, the Pentium III processor does not utilize it. Only the Intel® Celeron™ processor utilizes the BSEL0 signal. Pentium III processors are 3.3 V tolerant for these signals, as is the 840 chipset.

A new clock synthesizer has been designed to support selections of 100 MHz and 133 MHz. The REF input pin has been redefined to be a frequency selection strap (BSEL1) during power-on and then becomes a 14 MHz reference clock output. Figure 6-3 details the new BSEL[1:0] circuit design for flexible PGA370 designs.

Note: BSEL[1:0] are now pulled up using 1 KΩ resistors.

Figure 6-3. BSEL[1:0] Circuit Implementation for PGA370 Designs



6.10 CLKREF Circuit Implementation

The CLKREF input requires a 1.25 V source. It can be generated from a voltage divider on the $V_{CC2.5}$ or $V_{CC3.3}$ sources utilizing 1% tolerance resistors. A 4.7 µF decoupling capacitor should be included on this input. See Figure 6-4 and Figure 6-8 for example CLKREF circuits. *Do not use V_{TT} as the source for this reference!*

Figure 6-4. Examples for CLKREF Divider Circuit

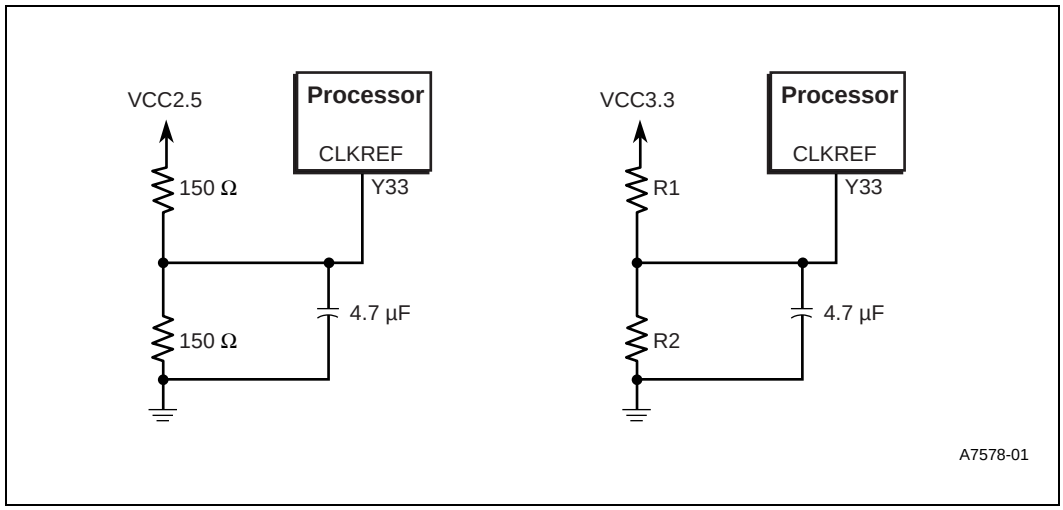


Table 6-8. Resistor Values for CLKREF Divider (3.3V Source)

R1 (Ω)	R2 (Ω)	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

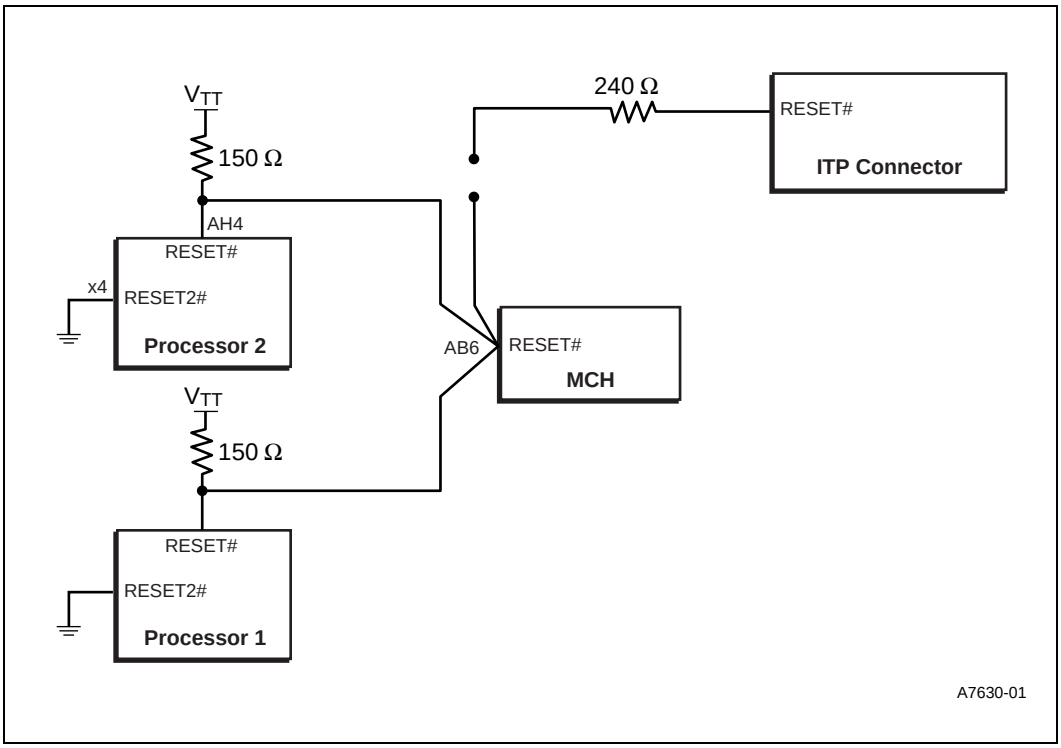
6.11 On-die R_{TT} Considerations

6.11.1 Connecting RESET# in Dual Processor PGA370 Designs

For dual processor PGA370-processor designs, route the AGTL+ signal from the chipset to the RESET# pin (AH4) on the processor as well as to the ITP connector. The RESET2# pin (X4) is provided for backwards compatibility only, and should be connected to ground. Finally, the AGTL+ reset signal must always be terminated to V_{TT} on the motherboard. See Figure 6-5.

6.11.2 AGTL+ Reset Layout Topology

Figure 6-5. AGTL+ Reset Schematic for PGA370 Designs



Single (FC-PGA) Intel® Pentium® III Processors 7

This chapter discusses using the FC-PGA Intel® Pentium® III processor in a single processor system design. Chapter 6 discusses dual processor design.

7.1 One-Way FC-PGA Pentium® III Processors and Intel® 840 Chipset Layout

The Intel Pentium III processor is the most powerful and advanced member of Intel's family of P6 processors. The Intel 840 chipset has been designed to provide a high-performance memory, Accelerated Graphics Port (AGP), and I/O subsystem to support Intel Pentium III processors. The Pentium III processor implements a synchronous, latched bus protocol that allows a full clock cycle for signal transmission and a full clock cycle for signal interpretation and generation. This protocol simplifies interconnect timing requirements and supports 133 MHz system bus designs using conventional interconnect technology. The processor system bus operates using Assisted Gunning Transceiver Logic (AGTL+).

The goal of this chapter is to provide the information needed to design uniprocessor systems with the Intel 840 chipset. This layout guideline *does not* support designs using other chipsets. This chapter provides guidelines and methodologies that are to be used with good engineering practices. See the *Pentium® III Processor for the PGA370 Socket at 500 MHz to 1 GHz* datasheet (order number 245264) and the Intel 840 Chipset component datasheets for specific electrical details. Intel strongly recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design.

7.2 Definition of Terms

Table 7-1. Definition of Terms (Sheet 1 of 2)

Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
CLK_{SHIFT}	Clock timing offset between chipset and CPU, used to maximize timing margins.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. This results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Cross-talk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • **Backward Cross-talk** - coupling which creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. • **Forward Cross-talk** - coupling which creates a signal in a victim network that travels in the same direction as the aggressor’s signal. • **Even Mode Cross-talk** - coupling from multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • **Odd Mode Cross-talk** - coupling from multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Flight Time	A term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, and any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as the time difference, between a signal at the input pin of a receiving agent crossing V_{REF} (adjusted to meet the receiver manufacturer’s conditions required for AC timing specification; *i.e.*, ringback, etc.) and the output pin of the driving agent crossing V_{REF}, if the driver was driving the TEST load used to specify the driver’s AC timings.
GTL+	The bus technology used by the Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL Gunning Transceiver Logic) technology. See the *Pentium® II Processor Developer’s Manual* for more details of GTL+.
M_{ADJ}	Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs when multiple data bits switch in the same cycle. The adjustment factor includes such mechanisms as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise.
Network	The trace of a printed circuit board (PCB) that completes an electrical connection between two or more components.
Network Length	Distance between extreme bus agents on the network, not including the distance connecting the end bus agents to the termination resistors.

Table 7-1. Definition of Terms (Sheet 2 of 2)

Overdrive Region	The voltage range, at a receiver, located above and below V_{REF} for signal integrity analysis. See the *Pentium® II Processor Developer's Manual* for more details.
Overshoot	Maximum voltage allowed for a signal at the processor core pad. See the processor's datasheet for overshoot specification.
Pin	A feature of a logic package used to connect the package to the 370-pin FC-PGA socket.
Ringback Voltage	The voltage that a signal rings back to during a rising or falling edge. Ringback may be due to reflections, driver oscillations, etc. See each processor's datasheet for ringback specifications.
Settling Limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective processor's datasheet for settling limit specifications.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO) Effects	Refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "pushout"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the trunk terminating at the pad of an agent.
Test Load	Intel uses a 50-Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, terminating at agent pads.
Undershoot	Maximum voltage allowed for a signal to extend below V_{SS} at the processor core pad. See each processor's datasheet for undershoot specifications.
Victim	A network that receives a coupled cross-talk signal from another network is called the victim network.
V_{REF} Guardband	A guardband (ΔV_{REF}) defined above and below V_{REF} to provide a more realistic model accounting for noise such as cross-talk, V_{TT} noise, and V_{REF} noise.

7.3 AGTL+ Design Methodology

The guideline recommended in this document is based on experience at Intel in developing many different P6 family (Pentium Pro, Pentium II and Pentium III) processor-based systems.

1. Begin with an initial timing analysis and topology definition.
2. Perform pre-layout analog simulation for a detailed picture of a working "solution space" for the design. These pre-layout simulations help define routing rules prior to placement and routing.
3. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis.
4. Validate the analog simulations when actual systems become available. The validation section (see Appendix A) describes a method for determining the flight time in the actual system.

Guideline Methodology:

- Initial timing analysis
- Determine general topology, layout, and routing
- Pre-Layout Simulation
  - — Sensitivity sweep
  - — Monte Carlo analysis
- Place and route board
  - — Estimate component-to-component spacing for AGTL+ Signals
  - — Layout and route board
- Post-layout simulation
  - — Interconnect extraction
  - — Inter-symbol interference (ISI), cross-talk, and Monte Carlo analysis
  - — Verify BCLK skew meets design specifications
- Validation
  - — Measurements
  - — Determining flight time

7.4 Initial Timing Analysis

Intel highly recommends performing simulations as part of the board design process. This includes pre-layout simulations to define a passing and robust solution space. Intel also recommends running post-layout simulations based on the extracted board layout to verify that the layout meets timing and noise requirements. Simulations are required for all designs that deviate from the recommended layout guidelines.

Table 7-2 lists the AGTL+ component timings of the Pentium III processor and Intel 840 MCH defined at the pins. These timings are for **reference only**; obtain each component's specifications from its datasheet.

Table 7-2. AGTL+ Component Timings

IC Parameters	Intel® Pentium® III Processor at 133 MHz Processor System Bus Frequency	Intel® 840 MCH	Notes
Clock to Output maximum (T_{CO_MAX})	3.25 ns	3.00 ns	1, 2
Clock to Output minimum (T_{CO_MIN})	0.4 ns	0.25 ns	1, 2
Setup time (T_{SU_MIN})	0.95 ns	1.85 ns	1, 2
Hold time (T_{HOLD})	1.0 ns	0.60 ns	1, 2

NOTES:
1. Numbers in the table are for reference only and are subject to change. Please check the appropriate component documentation for the current timing parameter values.
2. T_{SU_MIN} = 1.85 ns assumes the Intel 840 MCH sees a minimum edge rate equal to 0.3 V/ns.

Table 7-3 gives an example of AGTL+ initial maximum flight time and Table 7-4 gives an example of a minimum flight time calculation for a 133 MHz, FC-PGA Pentium III processor/Intel 840 chipset system bus. Table 7-3 and Table 7-4 show a recommended setup and hold margin timing budget for a 133 MHz system bus supporting FC-PGA Pentium III processor operation with the Intel 840 chipset. The recommended topologies should support the maximum and minimum flight times suggested in these tables. The processor and chipset timing values used in these tables are for reference only and should be taken from the latest component datasheet.

The maximum and minimum flight times suggested for this topology make certain assumptions as described below. Any deviations from these assumptions must be analyzed to verify that the recommended topology and flight times are still valid. These flight times also assume that the component AGTL+ signal quality requirements are met or derated properly.

- The timing tables make assumptions about the clock skew and jitter and are not meant to be clock-specific (e.g., clock driver skew is minimized by ganging the outputs together at a clock driver device that supports this operation). Clock skew and jitter values are dependent on the components and clock distribution method chosen for a particular design and *must* be budgeted into these timing equations as appropriate for each design.
- System timing budget must assume 0.175 ns of clock driver skew if the outputs are not tied together and a clock driver that meets the CK98W/S or CK133 Clock Synthesizer/Driver Specification is being used. Be sure to verify with your clock component vendor that ganging together the clock outputs is supported. See the respective processor's datasheet, appropriate Intel 840 chipset documentation, and CK133 clock synthesizer/driver documentation for details on clock skew and jitter specifications. Refer to the Chapter 17, "Clocking."
- The M_{ADJ} factor accounts for multi-bit switching effects that may worsen the flight time or signal quality and are not always seen in simulation. This factor is highly dependent on how high-speed design practices are implemented on the baseboard (e.g., decoupling, signal return paths) and should be budgeted accordingly in each design.

  There are additional effects that may not necessarily be covered by the multi-bit adjustment factor (M_{ADJ}) and should be budgeted as appropriate to the baseboard design. Examples include the effective board propagation constant (S_{EFF}), which is a function of:

  — Dielectric constant (ε_r) of the PCB material

  — The trace type connecting the components (stripline or microstrip)

  — The length of the trace and the load of the components on the trace. The board propagation constant multiplied by the trace length is a component of the flight time but not necessarily equal to the flight time.

Table 7-3. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	CLK Period[2]	T_{CO_MAX}	T_{SU_MIN}	CLK_{SKEW}	CLK_{JITTER}	CLK_{SHIFT}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor	840 MCH	7.5	3.25	1.85	0.15	0.25	0.26	0.40	1.86
840 MCH	Processor	7.5	3.00	0.95	0.15	0.25	0.26	0.40	2.49

NOTES:
1. All times are in nanoseconds.
2. BCLK period = 7.5 ns @ 133 MHz.
3. The flight times in this column include margin to account for the timing degradation multi-bit adjustment factor (M_{ADJ}). The following factors influence the M_{ADJ} factor:
   - SSO timing push-out or pull-in
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path
   - Cross-talk on the PCB and internal to the chipset and CPU packages

Table 7-4. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	CLK_{SKEW}	T_{CO_MIN}	CLK_{SHIFT}	Recommended T_{FLT_MIN}
Processor	840 MCH	0.60	0.15	0.4	0.26	0.61
840 MCH	Processor	1.0	0.15	0.25	0.26	0.64

NOTE: All times are in nanoseconds.

7.4.1 Flight Time Calculation

The following timing equations were used to calculate the minimum and maximum flight times:

Processor driving:

$$T_{FLT\_MAX} \leq \text{Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ} + CLK_{SHFT}$$

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ} + CLK_{SHFT}$$

Chipset driving:

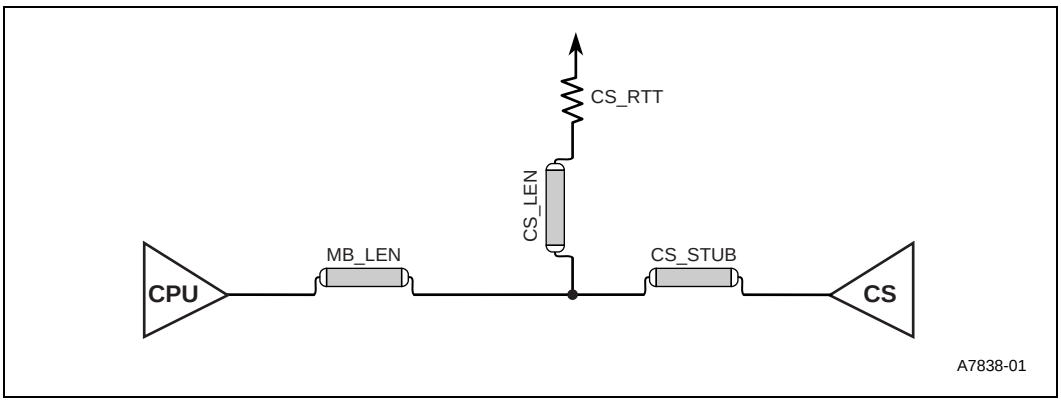
$$T_{FLT\_MAX} \leq \text{Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ} - CLK_{SHFT}$$

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ} - CLK_{SHFT}$$

7.5 General Topology

Segment descriptions and length recommendations are provided below for the simulated bus topology shown in Figure 7-1. Segment lengths are defined to the pins of the devices or components. The signal routing assumes a **four-signal layer** (six or eight-layer motherboard) ATX form factor platform. For uniprocessor FC-PGA/Intel 840 chipset designs, a termination resistor is required at the chipset. To satisfy signal integrity requirements, it is required that all system bus signal segments (MB_LEN, CS_STUB, CS_LEN) be referenced to the ground plane for the entire route. If multiple ground plane references are used, then the ground planes should be stitched together with vias between all the ground planes.

Figure 7-1. Uniprocessor Topology for 133 MHz Processor System Bus Frequency



The CPU to chipset distance minimum and maximum can be calculated using Table 7-5. The key requirement is to keep CS_RTT located close to the chipset and follow a “T” topology, as shown in Figure 7-1.

Table 7-5. Recommendations

Parameter	Min	Max	Comments
CS_RTT	59 Ω	65 Ω	Terminator Resistor Value Recommended: 62 Ω
CS_LEN	0”	0.5”	Terminator Resistor Stub
CS_STUB	0.2”	1.0	Resistor Stub via to CS ball
MB_LEN	5.25”	6.25”	CPU to “T” point
CPU_{RTT}			On-die R_{TT} set to 62 Ω nominal on the processor die

All simulations assume the following:

- V_{TT} is maintained at 1.5 V ± 3%
- V_{REF} is maintained at 2/3 V_{TT} ± 50 mV
- Motherboard impedance, Z0, is 60 Ω ± 15%
- Signal propagation delay is between 1.93 ns/ft and 2.057 ns/ft on baseboard
- The dielectric constant, εr, is 3.7–4.7
- The tracewidth-to-spacing ratio is 5:15 (i.e., 5 mil trace with 15 mil space)

7.6 Changes in Signal Connectivity for Uniprocessor Systems

Four signals are implemented differently for uniprocessor systems, as shown in Table 7-6. All other signals are as defined in Table 19-2 on page 19-12.

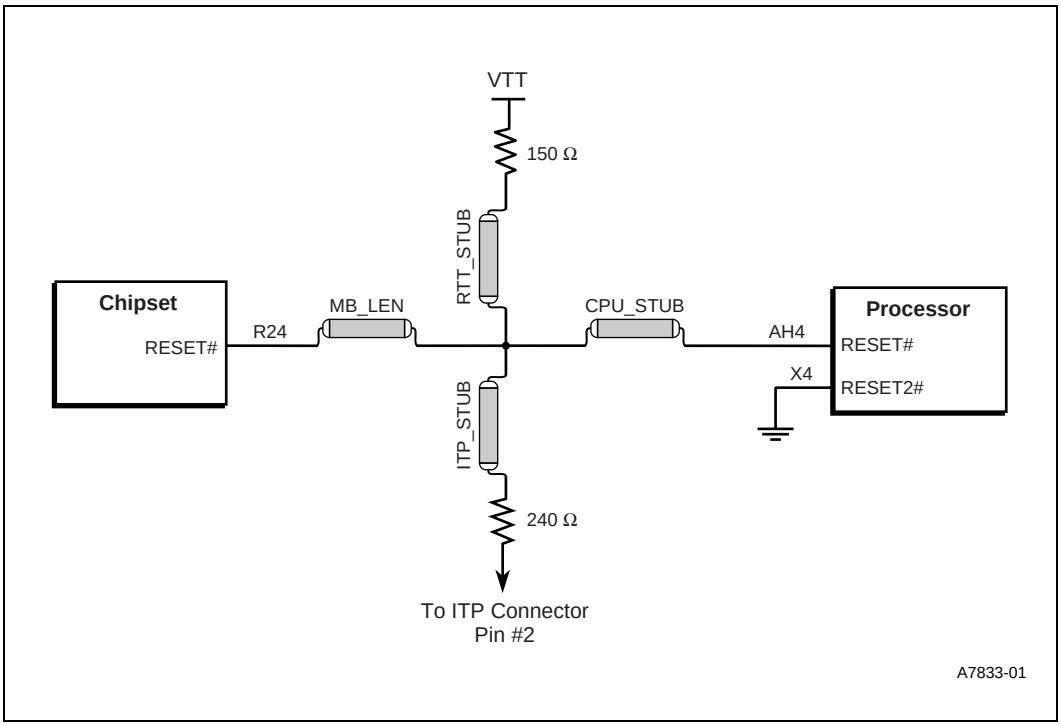
Table 7-6. Signal Differences for Uniprocessor Intel® 840 Chipset Systems

CPU Pin	I/O	Comments
BREQ0#	I/O	Connect to MCH
BREQ1#	I	No Connect
RESET#	I	150 Ω pull-up to V_{TT}. Connect to MCH. (Optional Debug) 240 Ω series resistor to ITP.
R_{TT_CTRL}	I	The R_{TT_CTRL} input signal provides AGTL+ termination control. For uniprocessor implementations, both on-die and on-board termination is required. Placing a 62 Ω, 1% resistor on the RTT_CTRL pin to ground will set the appropriate on-die R_{TT} value for the uniprocessor topology.

7.7 Connecting RESET# in Uniprocessor PGA370 Designs

Route the AGTL+ signal from the chipset to the RESET# pin (AH4) on the processor as well as to the ITP connector. The RESET2# pin (X4) is provided for backwards compatibility only, and should be connected to ground. Finally, the AGTL+ reset signal must always be terminated to V_{TT} (using a 15 Ω pull-up resistor.) on the motherboard. See Figure 7-2.

Figure 7-2. Uniprocessor Reset Topology

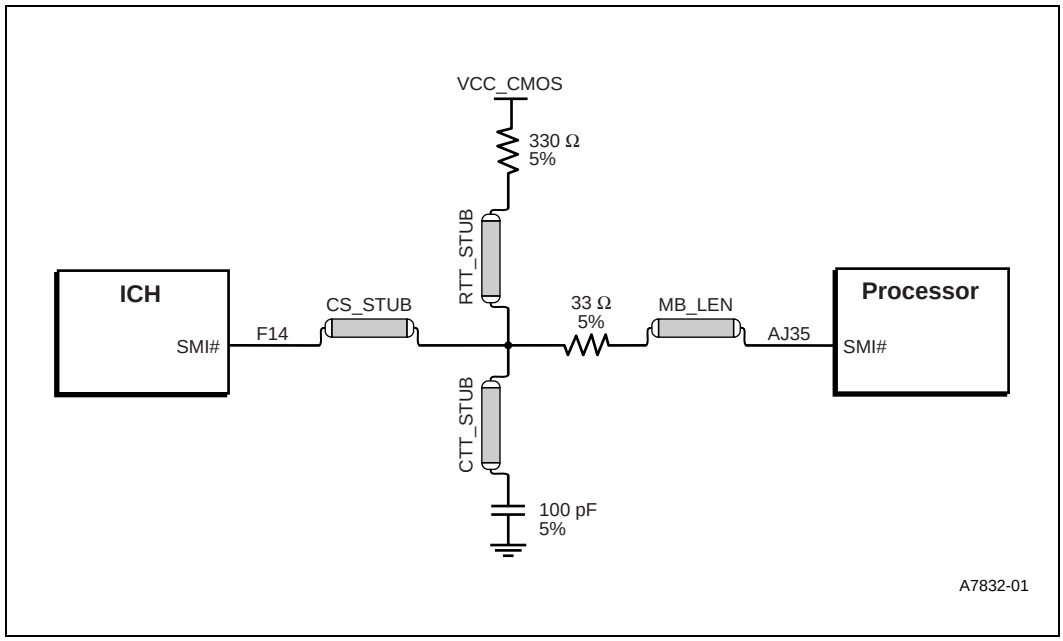


Parameter	Min (inches)	Max (inches)
MB_LEN (chipset to “T” point)	5.25	6.25
CPU_STUB	0.2	1.0
RTT_STUB	0.0	0.5
ITP_STUB	0.0	0.5

7.8 SMI# Layout Guidelines

For design assistance with reducing or eliminating the non-monotonic rising edge of the SMI# signal, refer to the simulated topologies shown in Figure 7-3. The Pentium III processor SMI# erratum is documented in the latest specification update. Please refer to the specification update for additional information on the steppings affected.

Figure 7-3. Uniprocessor SMI# Topology



Parameter	Min (inches)	Max (inches)	Comments
CS_STUB	0.2	1.5	ICH to “T” point
RTT_STUB	0	0.5	“T” point to termination resistor
CTT_STUB	0	0.5	“T” point to termination cap
MB_LEN (CPU to “T” point)	0.5	20.0	Series resistor to CPU

Memory Interface 8

The perfect matching of transmission line impedance and uniform trace length is essential for the Direct RDRAM interface to work properly. Maintaining 28 Ω (+/- 10%) loaded impedance for every RSL (Rambus* Signaling Level) signal requires some changes to the standard trace width and board prepreg thickness.

Typically, achieving 28 Ω nominal impedance with 7 mil prepreg requires 28 mil-wide traces. The 28 mils-wide traces are too wide to break out of the two rows of RSL signals on the 82840 MCH. In order to reduce the trace width, a 4.5 mil prepreg is required. This thinner prepreg allows 18 mil wide traces to meet the 28 Ω (+/- 10%) nominal impedance requirement. Refer to Figure 5-3 and Figure 5-4 for board stackup details. The signals on RDRAM Channels are broken into three groups: RSL, CMOS and Clock signals, as shown in Table 8-1.

Table 8-1. RDRAM Channel Signal Groups

RSL Signals	DQA[8:0] DQB[8:0] RQ[7:0]
CMOS Signals	CMD† SCK† SIO
Clock Signals	CTM CTM# CFM CFM#

† Denotes high speed CMOS signals.

Characterization and understanding of the trace impedance is critical for delivering reliable systems at the increased bus frequencies. Incorporating a test coupon design into the motherboard makes testing simpler and more accurate. The test coupon pattern must match the probe type being used. Providing the test coupon in the memory section will provide the greatest accuracy, as board impedance varies with location.

The location of the test coupon is listed in order of preference below:

First Choice (Ideal Location)	=	Memory section of the motherboard
Second Choice	=	Any section of the motherboard
Third Choice	=	Separate location in the panel

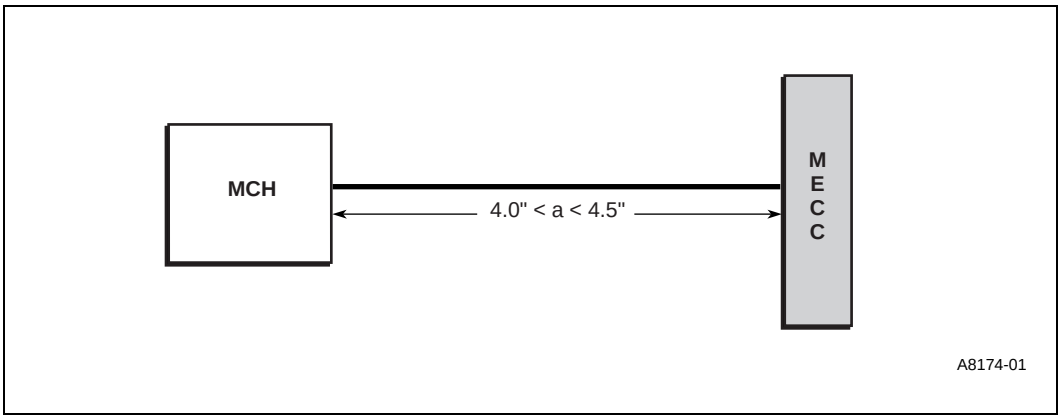
The *Intel Impedance Test Methodology Document* should be used to ensure that boards are within the 28 Ω +/- 10% requirement. The *Intel Controlled Impedance Design and Test Document* should be used for the test coupon design and implementation. These documents can be found at:

http://developer.intel.com/design/chipsets/memory/rdram.htm (select “Application Notes”)

8.1 Memory Design with MEC/MECC (Outer Layer Routing)

The Memory Expansion Card (MEC) concept is intended to provide flexibility and scalability of memory to an Intel® 840 chipset-based platform. The Intel 840 chipset supports both RIMMs down and MECC configurations. Additional details will be published in future revisions of this document. Figure 8-1 illustrates the MEC connection to the MCH.

Figure 8-1. MCH to MECC Layout (Outer Layer Routing)



All RSL signals between 82840 MCH and MECC should be maintained between 4.0” (min) and 4.5” (max). Although channels A and B are not required to match one another, the difference between channels should be minimized and must meet MCH levelization requirements.

In order to maintain 28 Ω trace impedance, the RSL signals must be nominally 18 mil wide. The exact width is determined by the board stack-up. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals. The 10 mil ground isolation traces must be connected to ground with a via every 0.5”. A 6 mil gap is required between the RSL signals and ground isolation traces. To ensure uniform traces, the trace width variation must be uniform on all RSL signals at every neck down. The RSL signals within each channel must be length matched to +/- 2 mils in the line section between the MCH and first device (MRH-R) on the MEC using trace length matching methods. Also, all RSL signals must have the same number of vias. It may be necessary to place additional vias (dummy vias) on RSL signals, even if vias are not needed, to meet the via loading requirement (equal number of vias).

8.2 RIMMs on the Motherboard

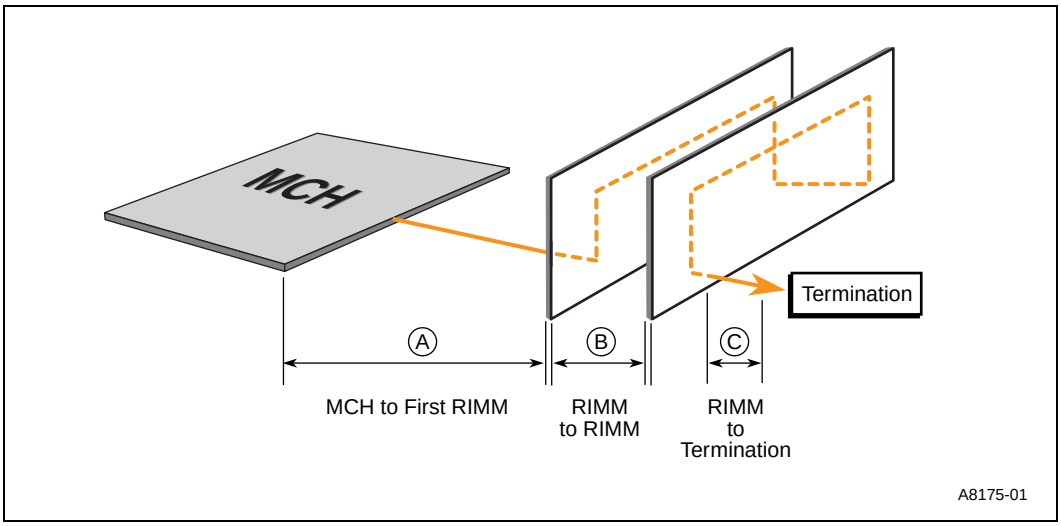
The following RDRAM layout guidelines are applicable for outer-layer routing for each channel. Additional layout guidelines will be available in future releases of this design guide.

8.2.1 RSL Signals

The RSL signals enter the first RIMM on the left side, propagate through the RIMM, and then exit on the right. The signal continues through the rest of the existing RIMMs until it is terminated at V_{TERM}. The unpopulated slot must have continuity modules in place to ensure that the signals propagate to the termination. Refer to the following Web site for more information regarding the Direct Rambus* technology:

http://www.rambus.com

Figure 8-2. RSL Routing Dimension for Two RIMMs



With the Intel 840 MCH, it is possible to achieve a longer trace length A (MCH to the first RIMM connector) in a two RIMMs-per-RDRAM channel implementation. Although channels A and B minimized are not required to match one another, the difference between channels should be minimized and must meet MCH levelization requirements, as shown in Table 8-2.

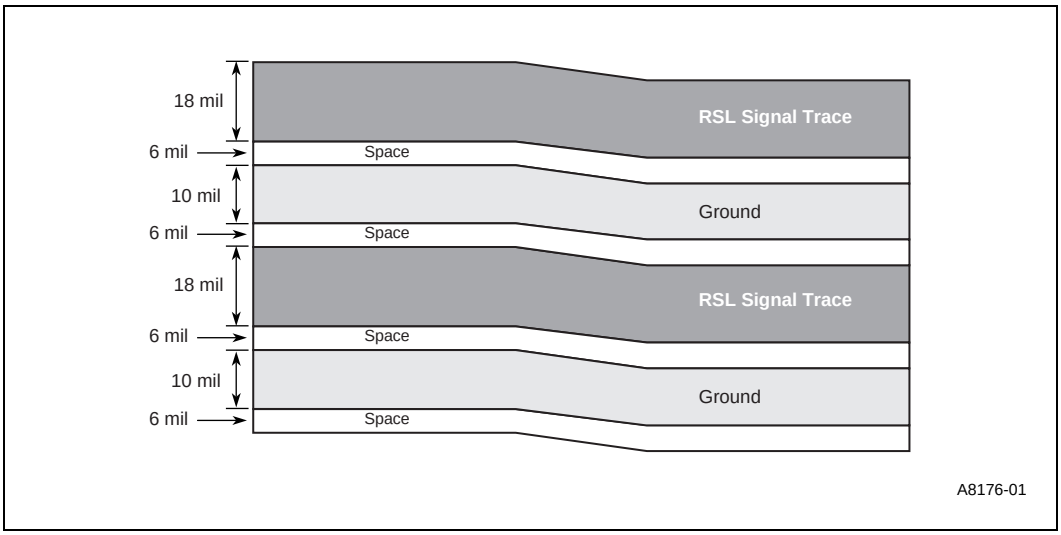
Table 8-2. RSL Routing Trace Lengths

Reference Section	Trace Description	Trace Length
A	MCH to first RIMM connector (Microstrip)	0” to 6”
A	MCH to first RIMM connector (Stripline)	0" to 3.75"
B	RIMM connector to RIMM connector	0.4” to 0.45”
C	RIMM to Termination	0” to 3”

In order to maintain a nominal 28 Ω trace impedance, the RSL signals must be 18 mils wide. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals through all sections “A,” “B” and “C”. The 10 mil ground isolation traces must be connected to ground with a via every 0.5”. A 6 mil gap is required between the RSL signals and the ground isolation trace. To ensure uniform trace lines, trace width variation must be uniform on all RSL signals at every neck-down for each line section. The RSL signals within each channel must be length matched to +/- 2 mils in line sections labelled “A” and +/- 2 mils in both line sections labeled “B” using the trace length matching methods described in the next section. Also, all RSL signals must have the same number of vias. It may be necessary to place additional

vias (dummy vias) on certain RSL signals, even if vias are not needed, to meet the via loading requirement (equal number of vias). There is no trace length matching requirement for traces in section “C”.

Figure 8-3. Example RSL Routing Diagram



8.2.2 RSL Signal Layer Alternation

All RSL signals must alternate layers as they are routed through the channel. For example, a signal routed on the primary side from the MCH to the first RIMM socket must be routed on the secondary side from the first RIMM to the second RIMM (signal B). When a signal is routed on the secondary layer from the MCH to the first RIMM socket, it must then be routed on the primary side from the first RIMM to the second (signal A). Signals can be routed on either layer from the last RIMM to the termination resistors. See Figure 8-4 and Table 8-3.

Figure 8-4. RSL Signal Layer Alternation

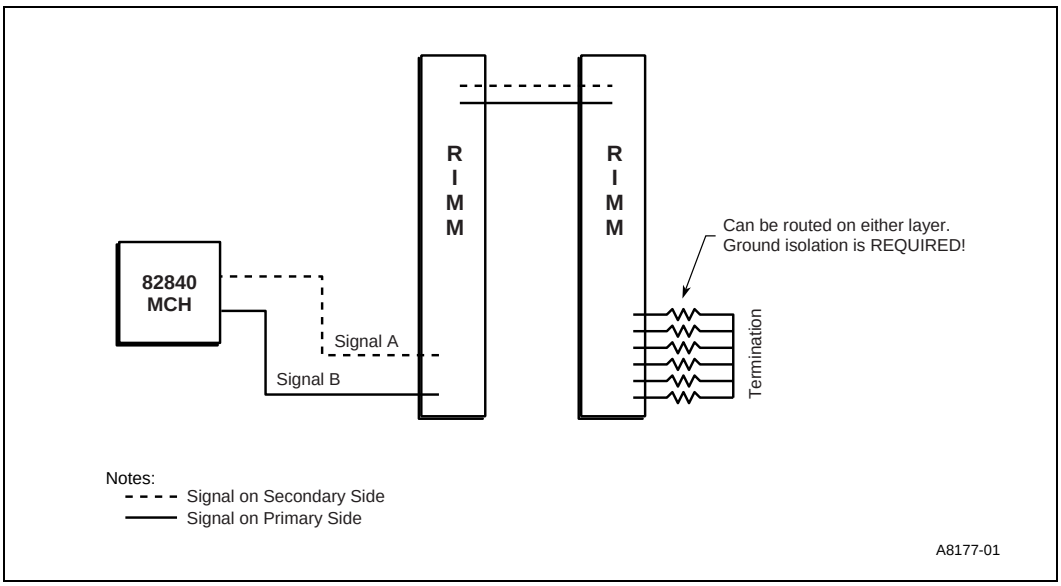


Table 8-3. RSL Signal Layer Alteration

MCH to First RIMM	First RIMM to Second RIMM
Primary Side	Secondary Side
Secondary Side	Primary Side

8.2.3 RSL Signal Termination

All RSL signals must be terminated to 1.8 V (V_{TERM}) using 27 Ω-2% or 28 Ω–2% resistors at the end of the channel opposite the MCH. Resistor packs are acceptable. V_{TERM} must be decoupled using very high-speed bypass capacitors (one 0.1 µF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, bulk capacitance is required. Assuming a linear regulator with approximate 20 µs response time, two 100 µF tantalum or other low ESR capacitors are recommended. All capacitors should use a minimum of two vias for each connection to the ground layer. The trace length between the last RIMM and the termination resistors should be less than 3". Length matching in this section of the channel is not required. The V_{TERM} power island should be *at least* 50 mils wide. This voltage is not required during Suspend-to-RAM (STR).

Figure 8-5. Direct RDRAM Termination

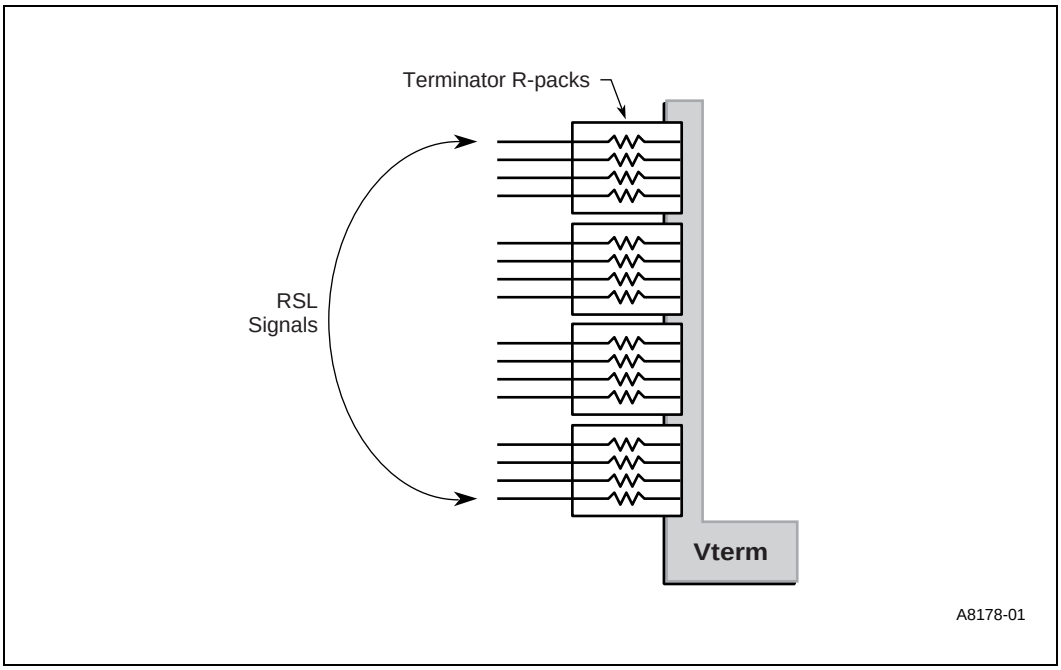
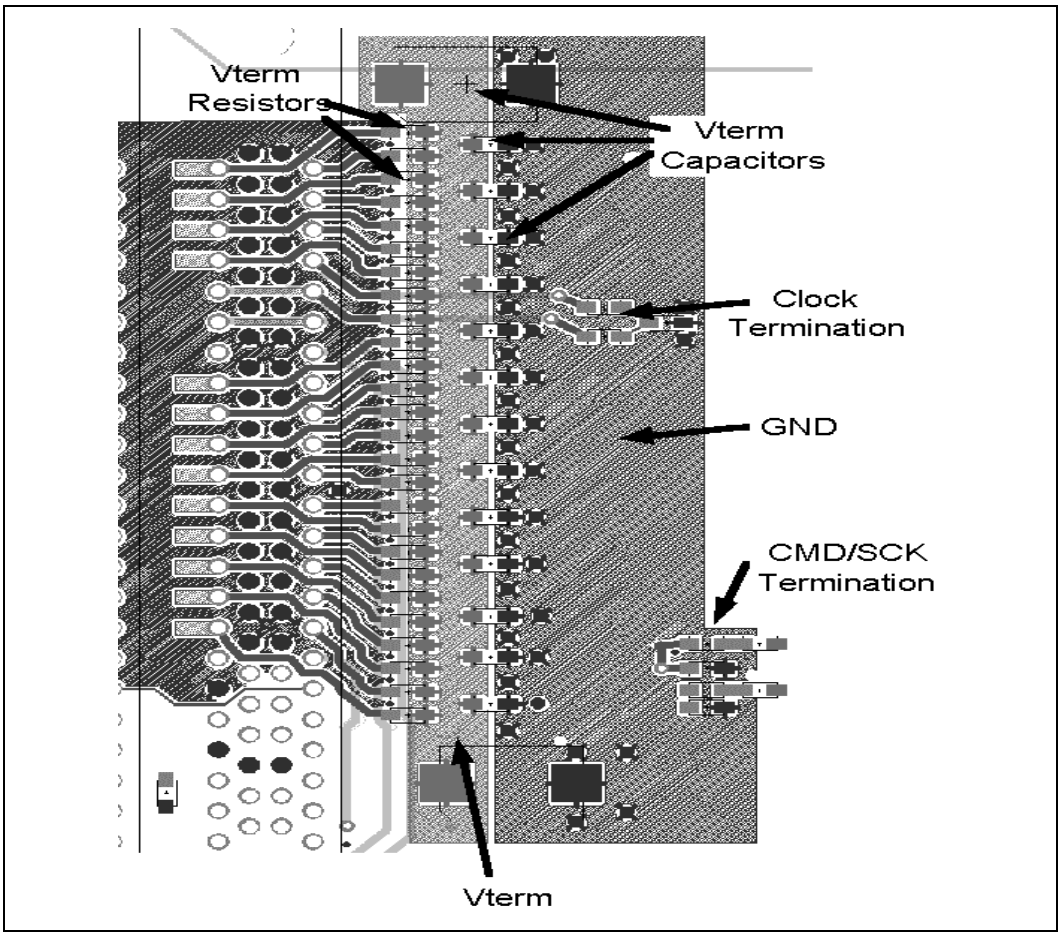


Figure 8-6. Rambus Termination Example



It is necessary to compensate for the electrical characteristic difference between a “dummy” via and “real” vias. Refer to “Via Compensation” on page 8-12 for more details.

8.2.4 RDRAM Connector Compensation

The RIMM connector inductance causes an impedance discontinuity on the Rambus* channel. This may reduce voltage and timing margin.

In order to compensate for the inductance of the connector, approximately 0.65 pF–0.85 pF compensating capacitive tab (C-TAB) is required on each RSL connector pin. This compensating capacitance must be added to the following connector pins at each connector:

LCTM	LCFM	LRQ[7:0]	RDQB[8:0]
LCTM#	LCFM#	RRQ[7:0]	LDQB[8:0]
RCTM	RCFM	RDQA[8:0]	
RCTM#	RCFMRE	LDQA[8:0]	

This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector. The target value is approximately 0.65 pF–0.85 pF. The copper tab area for the recommended stackup was determined through simulation. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Equation 8-1 is an approximation that can be used for calculating the copper tab area on an outer layer.

Equation 8-1. Length*Width = Area = C_{plate} * Thickness of prepreg / [(ε_0) (ε_r)] * (1.1)

C_{plate} = Capacitance of the plates
$\varepsilon_0 = 2.25 \times 10^{-16}$ F/mil
ε_r = Relative dielectric constant of prepreg material
Thickness of prepreg = Stackup dependent
Length, Width = Dimensions in mils of copper plate to be added
Factor of 1.1 accounts for fringe capacitance

Based on the stackup requirement outlined in the *Intel® 840 Chipset Platform Design Guide*, the copper tab area should be 2800 to 3600 sq mils. Different stackups require different copper tab area. Table 8-4 shows the suggested copper tab area:

Table 8-4. Copper Tab Area Calculation

Dielectric Thickness (D)	Separation Between Signal Traces & Copper Tab	Minimum Ground Flood	Air Gap between Signal & GND Flood	Compen-sating Capacitance in C_{plate} (pF)	CTAB Area (A) in sq mils	CTAB Shape
4.5	6	10	6	0.65	2800	140 L x 20 W 70 L x 40 W

Based on Equation 8-1, the area is 2800 sq mils, where ε_r is 4.2 and D is 4.5. These values are based on 2116 prepreg material.

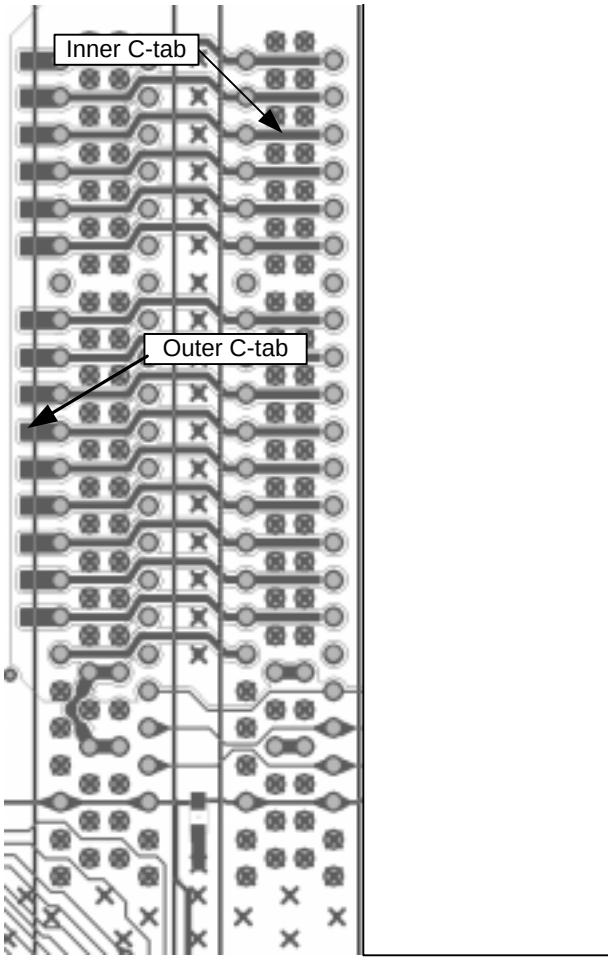
Note that more than one copper tab shape may be used as shown in Figure 8-7. The tab dimensions are based on the copper area over the ground plane. The actual length and width of the tabs may be different due to routing constraints (e.g., if the tab must extend to the center of hole or anti-pad); however each copper tab should have equivalent area. The copper tabs in Figure 8-7 and Figure 8-8 have the following dimensions:

Inner CTAB (C_A)= 140 (length) x 20 (width)

Outer CTAB (C_B)= 70 (length) x 40 (width)

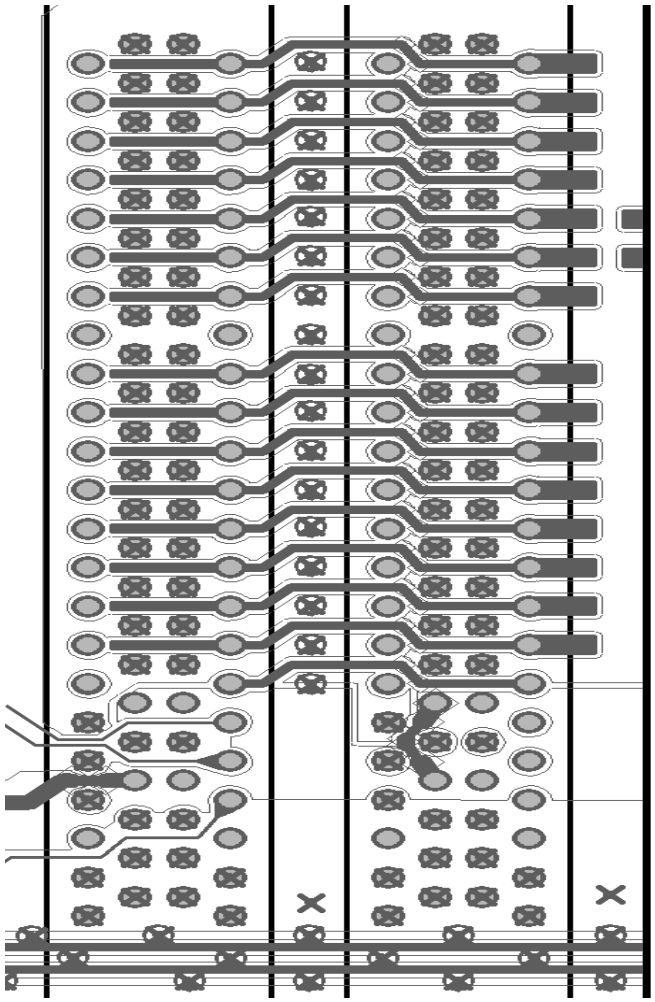
The following figures show a routing example of tab compensation capacitors. Note that ground floods around the RIMM pins must not be interrupted by the capacitor tabs, and they must be connected to avoid discontinuity in the ground plane as shown. Also, compensating capacitive tabs (C-TAB) are required at the connector pins for SCK and CMD signals.

Figure 8-7. C-Tab Example, Top Layer



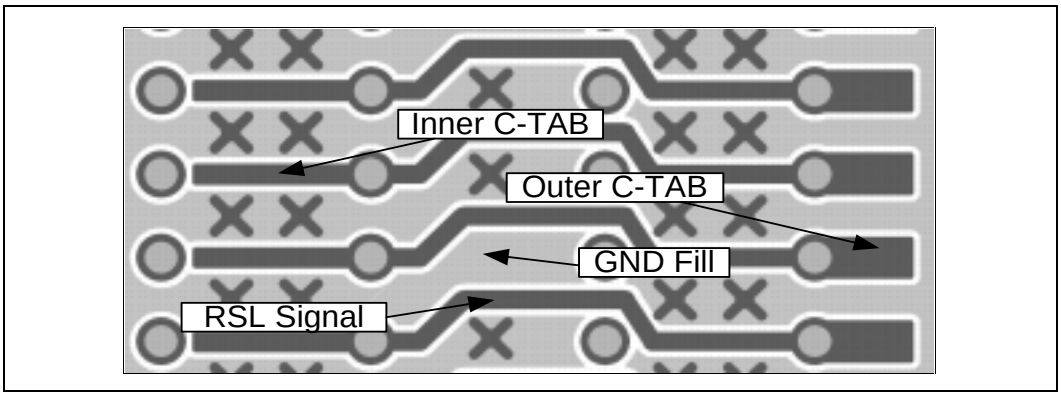
*Ground floods were removed for picture clarity.

Figure 8-8. C-Tab Example, Bottom Layer



*Ground floods were removed for picture clarity.

Figure 8-9. Close-up of C-TABs



8.2.5 Direct RDRAM Ground Plane Reference

The ground reference island under the RSL signals must be continuous from the last RIMM to the back of the termination capacitors and resistors. The return current flows through the V_{TERM} capacitors into the ground island and under the RSL traces. Any split in the ground island will cause a sub-optimal return path, resulting in an impedance variation. In a four-layer board, this requires the V_{TERM} island to be on an outer layer. The V_{TERM} island should *always* be placed on the top layer as shown in Figure 8-6.

8.2.6 Length Matching Method

Package dimension (ΔL_{PKG}): a representation of the length from the pad to the ball.

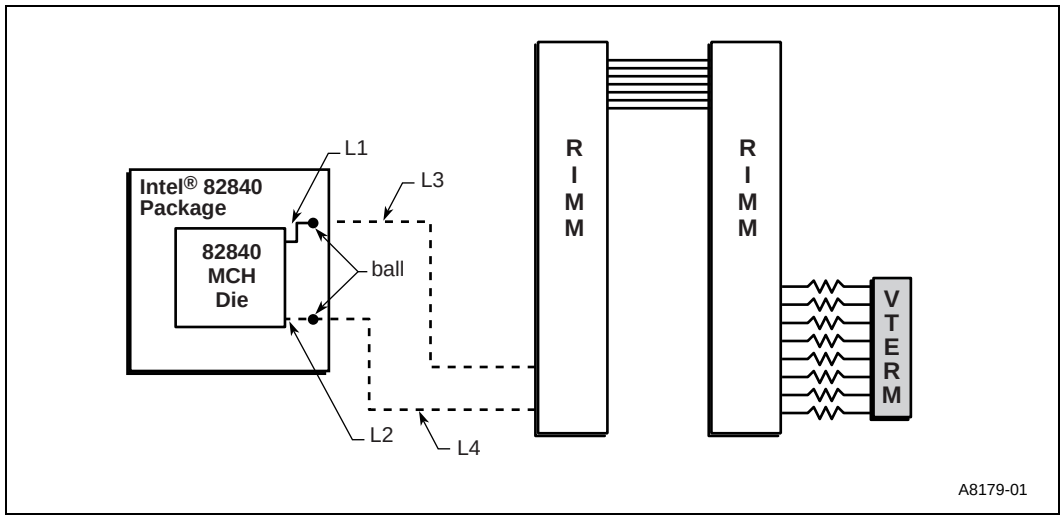
Board trace length (L_{MB}): the trace length on the board.

Nominal RSL length: the length to which all signals are matched. The Nominal RSL length is an arbitrary value to which all the RSL signals will be matched (within 10 mils).

L1, L2 = ΔL_{PKG} = Package dimension

L3, L4 = ΔL_{PCB} = Board trace length

Figure 8-10. RDRAM Trace Length Matching Example



To allow for greater routing flexibility, the RSL signals require pad-to-pin length matching between the 82840 MCH to the first RIMM connector or 82840 MCH to the MECC. When only the trace lengths between the balls of the 82840 MCH to the pins of RIMM connector are matched, the length mismatch between the pad (on the die) and the ball has not been compensated. All RSL signals, per channel, are required to have matching trace lengths from pad-to-pin within ±10 mils.

8.2.6.1 RSL Signals Length Match Requirement

L1 and L3 must be length matched to L2 and L4 within ±10 mils.

8.2.6.2 Compensated Trace Length Calculation

$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\text{TRACE VELOCITY}}) / PCB_{\text{TRACE VELOCITY}}$

The PCB trace length for each signal is a calculated value and may vary with designs. The actual package trace velocity is between 177 ps/in and 183 ps/in. The nominal trace velocity of 180 ps/in can be used when calculating the compensated PCB trace length. The $PCB_{\text{TRACE VELOCITY}}$ is board-dependent.

The RSL signal lengths (ΔL_{PKG}) can be normalized to either the shortest or longest RSL trace using the equation in the next section. Please refer to the *RS-Intel® 840 Chipset Ballout and Mechanical* document for specific package traces. Note that this ballout document provides RSL signal lengths NORMALIZED TO THE LONGEST trace length. Additional RSL length matching on the MEC with the MRH-R is available in the *Intel 840 Chipset: Workstation/Server MEC Design Guide*.

8.2.6.3 Normalized Trace Length Calculation

$\text{New } \Delta L_{PKG} = \Delta L_{PKG} - \Delta L_{\text{NORMALIZED RSL}}$

The RDRAM clocks (CTM, CTM#, CFM and CFM#) must be longer than the RDRAM signals due to their increased trace velocity (because they are differential and routed as a pair). To calculate the length for each clock, the following formula should be used:

Clock Length = Nominal RSL Signal Length (package + board)* 1.021

The lengthening of the clock signals, to compensate for their trace velocity change, applies *only* to routing between the MCH and the first RIMM. The clock signals should be matched in length to the RSL signals between RIMMs.

It is not necessary to account for CMOS signals package compensation. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be minimized; i.e., route the CMOS signals PCB trace length equal to nominal RSL PCB trace length.

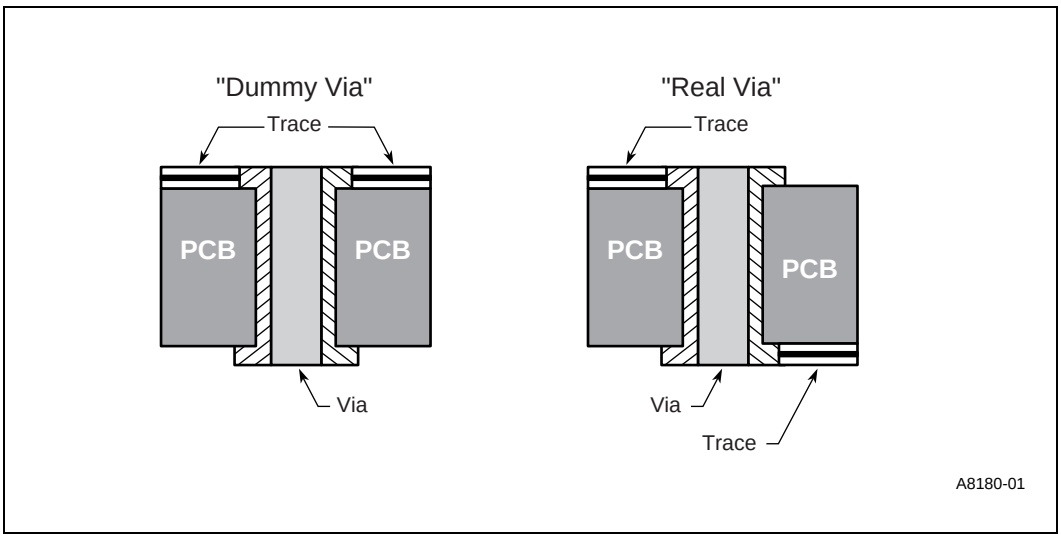
8.2.7 Via Compensation

All signals must have the same number of vias. As a result, each trace will have one via (near the BGA pad) because some of the RSL signals must be routed on the bottom of the motherboard. It is necessary to place dummy vias on all signals that are routed on the top layer. The electrical characteristics of dummy and real vias are not exactly the same, so additional compensation is needed on each signal that has dummy via. See Figure 8-11. Each signal with dummy via must have 25 mils of additional trace length. The additional 25 mils trace length must be added to the signal, routed on the top layer, after length matching.

Real via = Dummy via + 25 mils of trace length.

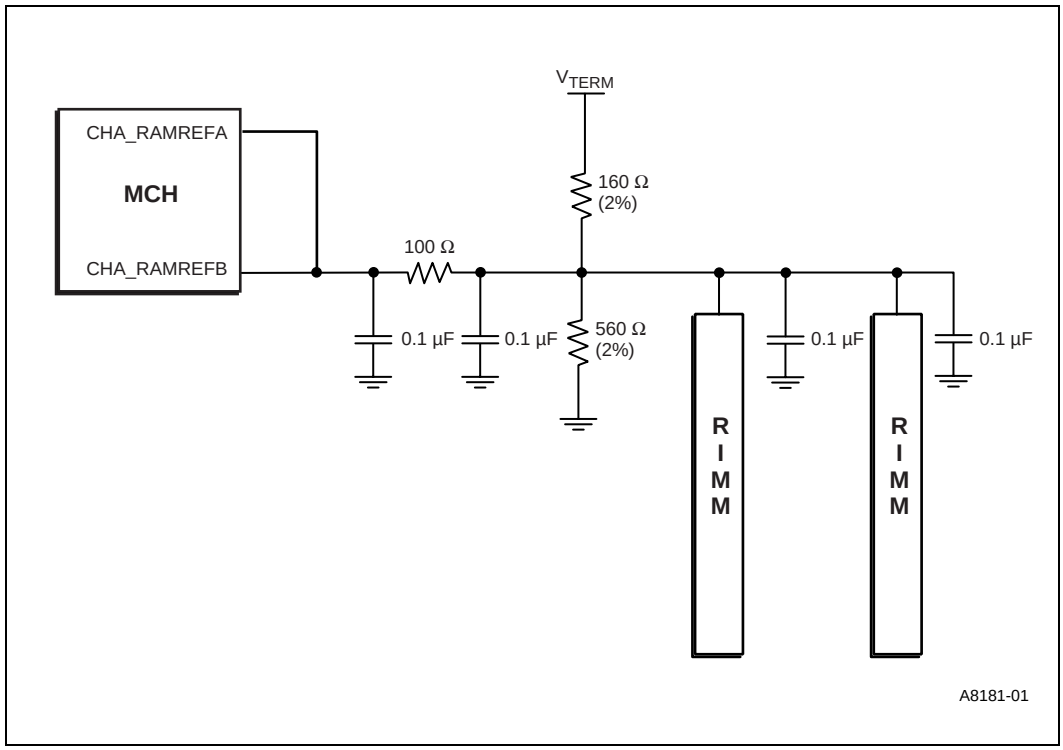
It is important to compensate for the electrical difference between real and dummy vias.

Figure 8-11. Dummy vs. Real Vias



8.2.8 Direct RDRAM Reference

Figure 8-12. RAMREF Generation Example Circuit



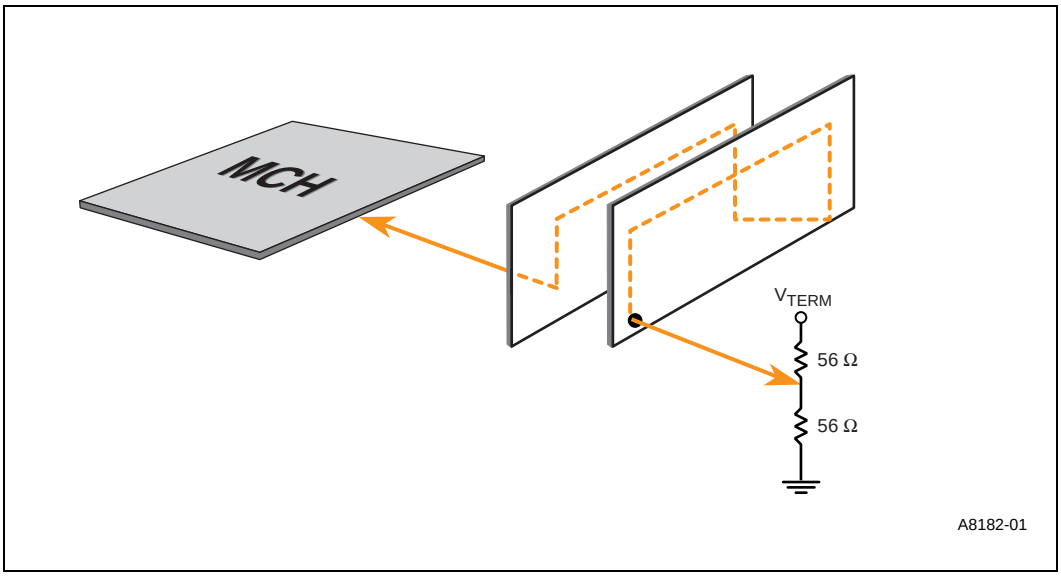
The RDRAM reference voltage (RAMREF) must be generated as shown in Figure 8-12. RAMREF should be generated from a typical resistor divider using 2% tolerant resistors. Additionally, RAMREF must be decoupled locally at EACH RIMM connector, at the resistor divider and at the 82840 MCH. Finally, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with 6 mils wide traces.

8.2.9 High Speed CMOS Routing

Due to the synchronous requirements between the RSL signals and the high-speed CMOS signals, these signals should be routed as part of the RSL channel. They must be impedance matched and properly terminated (using a different termination scheme than the RSL signals). The high-speed CMOS signals should be routed in their respective positions in the channel.

The high-speed CMOS signals must be length matched to the RSL signals within 1200 mils (1.2 inch) due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit.

Figure 8-13. High Speed CMOS Termination



A CMOS voltage must be supplied to each RIMM. This CMOS voltage is used by the RDRAMs CMOS interface. This voltage (V_{CMOS}) must be 1.8 V and the maximum load is 3 mA.

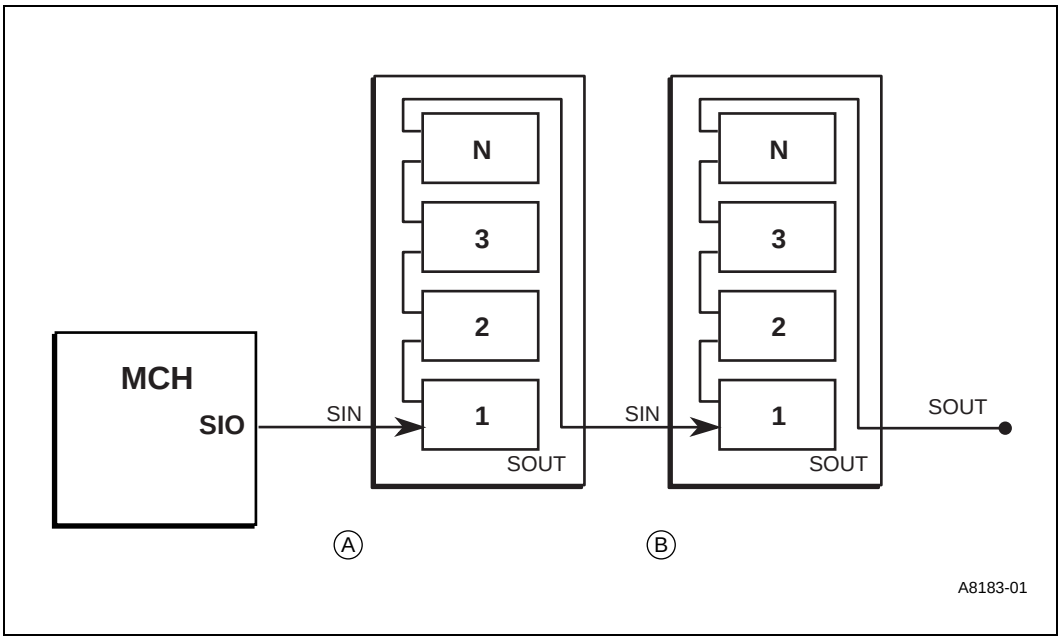
The additional voltage must be supplied during Suspend to RAM. Therefore, V_{TERM} and V_{CMOS} cannot be generated from the same source (i.e., they cannot be the same power plane). Due to the low power requirements of V_{CMOS}, it can be generated by a 36 Ω / 100 Ω resistor divider from 2.5 V. The high-speed CMOS signals require AC termination as shown in Figure 8-13, with two 56 Ω resistors.

8.2.10 SIO Routing

The SIO signal is a bidirectional signal that operates at 1 MHz. The SIO signal must be routed from RIMM connector to RIMM connectors as shown below. The SIO signal enters the first RIMM, propagates through all the devices (this signals is buffered by each device) on the RIMM, and then exits the RIMM. The signal continues through the next RIMM and is not terminated. The SIO is routed with a 5 mil wide, 60 Ω trace. The motherboard routing length for the SIO signals are the same as RSL signals.

The SIO signal requires a 2.2 KΩ–10 KΩ terminating resistor on the last RIMM's SOUT pin. Figure 8-14 illustrates an SIO routing example.

Figure 8-14. SIO Routing Example



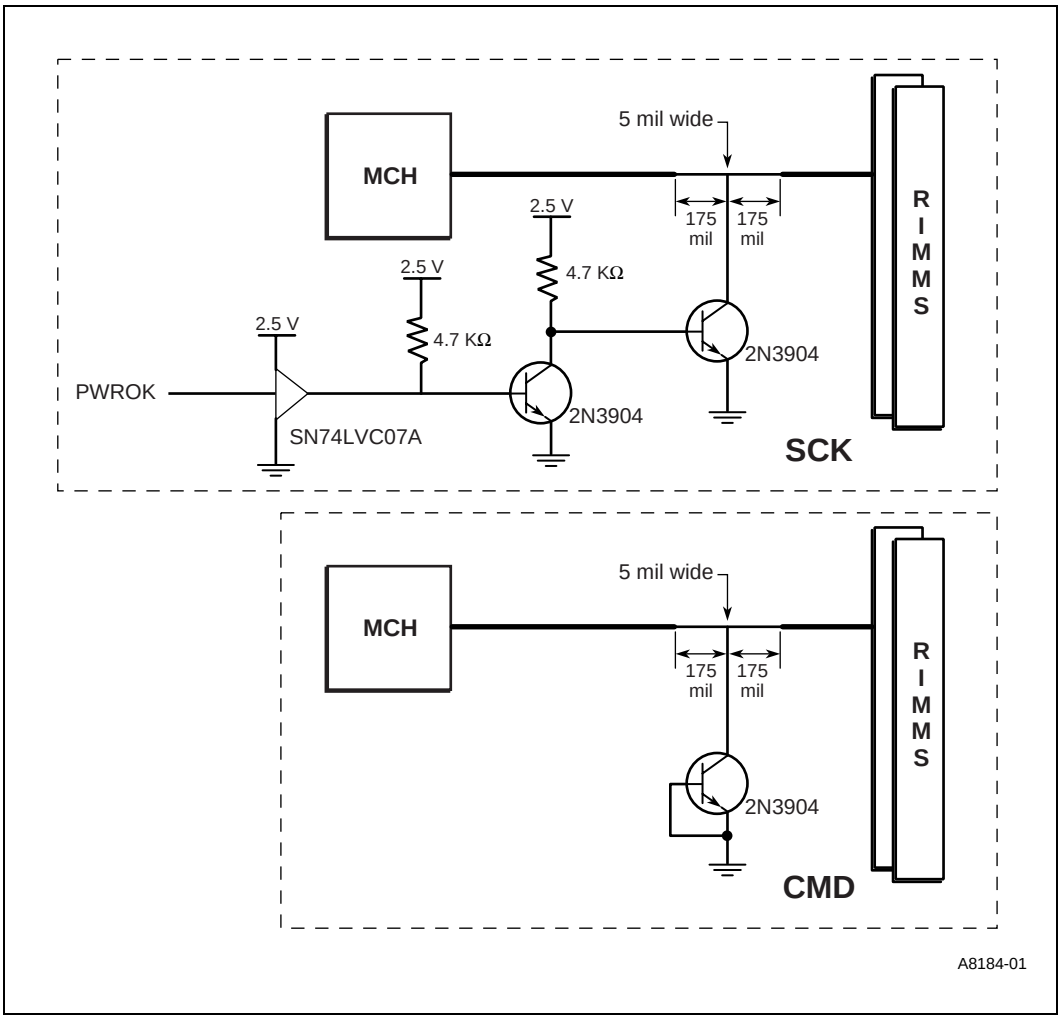
8.2.11 Suspend-to-RAM Shunt Transistor

When the Intel 840 chipset based system enters or exits Suspend-to-RAM, power will be ramping to the 82840 MCH (i.e., it will be powering-up or powering-down). When power is ramping, the state of the 82840 MCH outputs is not guaranteed. Therefore, the 82840 MCH could drive the CMOS signals and issue CMOS commands. One of the commands (the only one the RDRAM would respond to) is the power-down exit command. To avoid the 82840 MCH inadvertently taking the RDRAMs out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal must be shunted to ground when the 82840 MCH is entering and exiting Suspend-to-RAM. This shunting can be accomplished using the NPN transistor shown in the circuit shown in Figure 8-15. The transistor should have a C_{obo} of 4 pf or less (i.e., MMBT3904LT1).

In addition, to match the electrical characteristics on the SCK signal, the CMD signal needs a dummy transistor. This transistor's base should be tied to ground (i.e., always turned off).

To minimize impedance discontinuities, the traces for CMD and SCK must have a neck down from 18 mil traces to 5 mil traces for 175 mils on either side of the SCK/CMD attach point as shown in Figure 8-15.

Figure 8-15. RDRAM CMOS Shunt Transistor



This implementation is applicable for RIMMs down solution only, and is not needed on the repeater channels. Also, this implementation is not necessary if Suspend-to-RAM is not supported within the system.

AGP 2.0 9

For detailed AGP interface functionality (including protocols, rules, and signaling mechanisms) refer to the latest *AGP Interface Specification*, revision 2.0, which can be obtained from: http://www.agpforum.org. This design guide focuses only on specific Intel® 840 platform recommendations.

The *AGP Interface Specification*, revision 2.0 enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (four data samples per clock) and 1.5 V operation. In addition to these major enhancements, additional performance enhancements and clarifications, such as fast write capability, are included in revision 2.0. The Intel 840 chipset is the first Intel chipset that supports the enhanced features of revision 2.0.

The 4X operation of the AGP interface provides for quad-sampling of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. That is, the data is sampled four times during each 66 MHz AGP clock. This means that each data cycle is ¼ of 15 ns (66 MHz clock), or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time; not the clock cycle time. During 2X operation, the data is sampled twice during a 66 MHz clock cycle; therefore the data cycle time is 7.5 ns.

In order to allow for these high-speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing. During 4X operation, the AGP interface uses differential source synchronous strobing.

With data cycle times as small as 3.75 ns, and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5 V) requires even more noise immunity. For example, during 1.5 V operation, V_{ilmax} is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

The AGP signals are broken into three groups: 1X timing domain and 2X/4X timing domain signals. In addition, the 2X/4X timing domain signals are divided into three sets of signals (#1-#3). All signals must meet the minimum and maximum trace length, width and spacing requirements. The trace length matching requirements are only applicable between the 2X/4X timing domain signal sets. AGP signal groups are shown in Table 9-1.

Table 9-1. AGP 2.0 Signal Groups

1X Timing Domain	CLK
	RBF#
	WBF#
	ST[2:0]
	PIPE#
	REQ#
	GNT#
	PAR
	FRAME#
	IRDY#
	TRDY#
	STOP#
	DEVSEL#

2X/4X Timing Domain SET #1	AD[15:0]
	C/BE[1:0]#
	AD_STB0
	AD_STB0#[1]
SET #2	AD[31:16]
	C/BE[3:2]#
	AD_STB1
	AD_STB1#†
SET #3	SBA[7:0]
	SB_STB
	SB_STB#†

Misc. Signals	USB+
	USB-
	OVRCNT#
	PME#
	TYPDET#
	PERR#
	SERR#
	INTA#
	INTB#

† Signals AD_STB1 and SB_STB are AGP 4X signals only.

Strobe signals are not used in the 1X AGP mode.

In 2X AGP mode:

- AD[15:0] and C/BE[1:0]# are associated with AD_STB0
- AD[31:16] and C/BE[3:2]# are associated with AD_STB1
- SBA[7:0] is associated with SB_STB.

In 4X AGP mode:

- AD[15:0] and C/BE[1:0]# are associated with AD_STB0 and AD_STB0#
- AD[31:16] and C/BE[3:2]# are associated with AD_STB1 and AD_STB1#
- SBA[7:0] is associated with SB_STB and SB_STB#

9.1 General AGP Routing Guidelines

The routing guidelines provided in this section are recommended for optimal system design. However, these guidelines are not intended to replace thorough system validation on products based on the Intel 840 chipset.

9.1.1 Decoupling

A minimum of six 0.01 µF capacitors are required (at least four must be within 0.5” of the outer row of balls on the MCH) for V_{DDQ} decoupling. The designer should evenly distribute the placement of decoupling capacitors among the AGP interface signal field. It is recommended that the designer use a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric.

In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. One extra 0.01 µF capacitor is required per 10 vias. The capacitor should be placed as close to the center of the via field as possible.

The designer should ensure that the AGP connector is well decoupled as described in the *AGP Design Guide*, revision 1.0, section 1.5.3.3.

Note: In order to add the decoupling capacitors within 0.5" of the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short of a distance as possible (1" maximum).

9.1.2 Ground Reference

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector utilizing a minimum number of vias on each net:

AD_STB0	G_GNT#
AD_STB0#	G_GTRY#
AD_STB1	SB_STB
AD_STB1#	SB_STB#
G_IRDY#	ST[2:0]

In addition to the minimum signal set listed above, it is strongly recommended that half of all your AGP signals be reference to ground depending on board layout. An ideal design would have the complete AGP interface signal field referenced to ground.

The recommendations above are not specific to a particular PCB stackup, but are applicable to all Intel chipset designs.

9.2 1X Timing Domain Routing Guidelines

- The AGP 1X timing domain signals have a maximum trace length of 7.5". This maximum length applies to ALL 1X timing domain signals.
- AGP 1X timing domain signals can be routed with 5 mils minimum trace separation.
- There is no trace length mismatch requirement for 1X timing domain signals.

9.3 2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to *all* 2X/4X timing domain signals. These signals should be routed using 5 mils wide (~60 Ω) traces.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making trade-offs between signal coupling (trace spacing) and line lengths. The maximum trace length for AGP 2X/4X interface signals is 7.5".

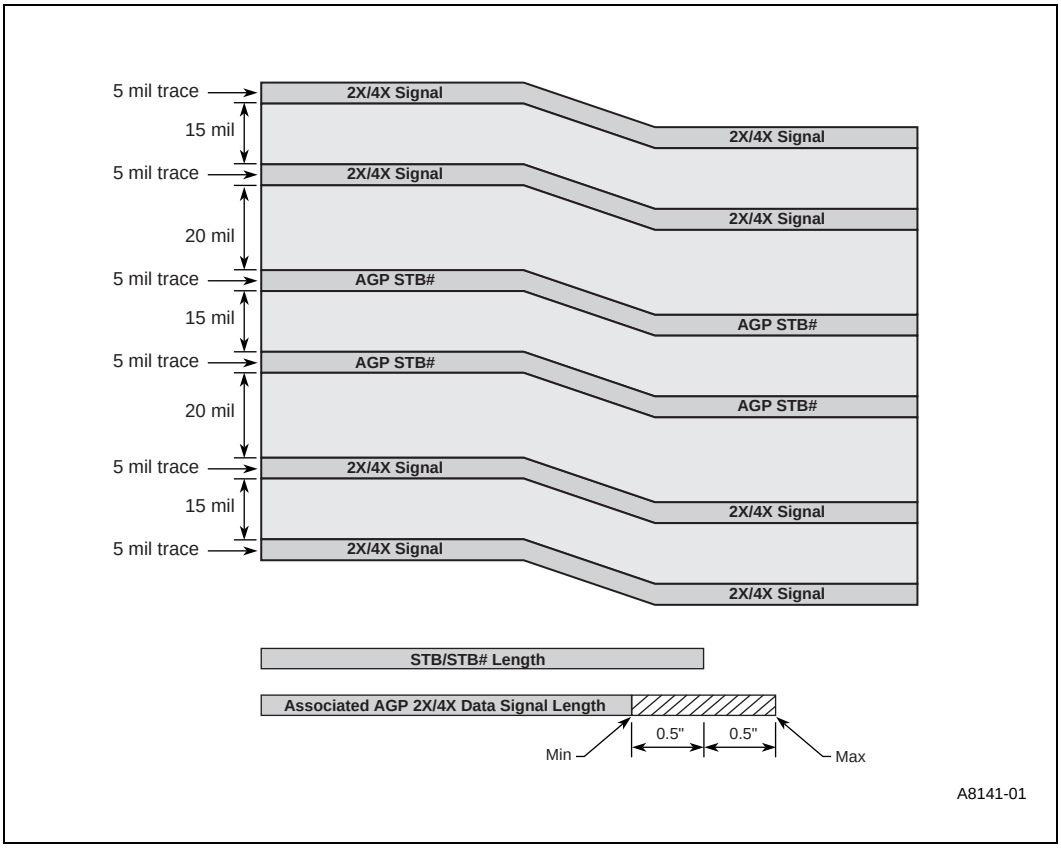
9.3.1 AGP Interfaces Signals < 6” Routing Guidelines

These guidelines are for designs that require less than 6” between the AGP connector and the MCH. If the AGP interface is less than 6 inches, at least 1:3 trace spacing is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched to their associated strobe within ±0.5 inches.

For example, when a set of strobe signals (e.g., AD_STB0 & AD_STB0#) are 5.3” long, then the associated data signals (i.e., AD[15:0] and C/BE#[2:0]) can be 4.8” to 5.8”. Another example, when strobe set SB_STB and SB_STB# is 4.2” long, the associated data signals (i.e., SBA[7:0]) can be 3.7” to 4.7”.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; special care must be taken when routing these signals. Because each strobe pair is a differential pair, the pair should be routed together (i.e., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1”. An example of AGP 2X/4X routing for interfaces greater than 6” is shown in Figure 9-1.

Figure 9-1. AGP 2X/4X Routing Example for Interfaces < 6”



9.3.2 AGP Interface Signals ≥ 6” and ≤ 7.25” Routing Guidelines

Longer lines have more crosstalk. Therefore in order to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths between 6” and 7.25”, 1:4 routing is required for all data lines and strobes. In this case, the line length mismatch must be less than ±0.125” within each signal group (between all data signals and the strobe signals).

For example, when a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5” long, then the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE#[2:0]), can be 6.475” to 6.625” long. When another strobe set (e.g., SB_STB and SB_STB#) is 6.2” long, then the data signals associated with those strobe signals (e.g., SBA[7:0]), can be 6.075” to 6.325” long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. Each strobe pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1” (that is, a strobe and its compliment must be the same length within 0.1”).

9.3.3 AGP Routing Summary

The 2X/4X Timing Domain Signals can be routed with 5 mil spacing when breaking out of the MCH 544 BGA. The routing must widen to the documented requirements within 0.3” of the MCH 544 BGA package.

When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

It is important to reduce line length mismatch to ensure added margin. In order to reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements *must not* be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

Table 9-2 summarizes AGP signal routing guidelines.

Table 9-2. AGP Routing Summary

Signals Group	Max Length	Trace Spacing	Length Mismatch	Associated Strobe(s)	Note(s)
1X Timing Domain	7.5”	5 mil†	-	-	-
2X/4X Timing Domain					
SET #1	7.25”	20 mil†	± 0.125”	AD_STB0 AD_STB0#	Strobe signal pair must be the same length
SET #2	7.25”	20 mil†	± 0.125”	AD_STB1 AD_STB1#	Strobe signal pair must be the same length
SET #3	7.25”	20 mil†	± 0.125”	SB_STB SB_STB#	Strobe signal pair must be the same length
2X/4X Timing Domain					
SET #1	6.0”	15 mil†	± 0.5”	AD_STB0 AD_STB0#	Strobe signal pair must be the same length
SET #2	6.0”	15 mil†	± 0.5”	AD_STB1 AD_STB1#	Strobe signal pair must be the same length
SET #3	6.0”	15 mil†	± 0.5”	SB_STB SB_STB#	Strobe signal pair must be the same length

† Each strobe pair must be separated from other signals by at least 20 mils.

9.3.4 AGP Clock Skew

The maximum total AGP clock skew, between the 82840 MCH and the AGP component, is 1 ns for all transfer modes. This 1 ns skew, includes the skew and jitter originated by the motherboard, add-in card and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage but at all points of the clock edge that fall in the switching range. The 1 ns skew is divided such that the motherboard is allotted 0.9 ns. The motherboard designer must determine how the 0.9 ns is allotted between the board and the synthesizer.

9.3.5 V_{DDQ} and TYPEDET#

AGP specifies two separate power planes: V_{CC} and V_{DDQ}. V_{CC} is the core power for the graphics controller. This voltage is *always* 3.3 V. V_{DDQ} is the interface voltage and is 3.3 V for AGP 1.0 implementations. For the designer developing an AGP 1.0 motherboard, there is no distinction between V_{CC} and V_{DDQ}. Both are tied to the 3.3 V power plane on the motherboard.

AGP 2.0 requires V_{CC} and V_{DDQ} to be tied to separate power planes. The *AGP Specification*, revision 2.0 implements a TYPEDET# (type detect) signal on the AGP connector that determines the operating voltage of the AGP 2.0 interface (V_{DDQ}). The motherboard must be able to provide either 1.5 V or 3.3 V to the add-in card depending on the state of the TYPEDET# signal. The 1.5 V low-voltage operation applies only to V_{DDQ}; V_{CC} is always 3.3 V, as shown in Table 9-3.

The TYPEDET# signal indicates whether the AGP 2.0 interface operates 1.5 V or 3.3 V. If TYPEDET# is floating (no connect) on an AGP add-in card, the interface is 3.3 V. If TYPEDET# is shorted to ground, the interface is 1.5 V.

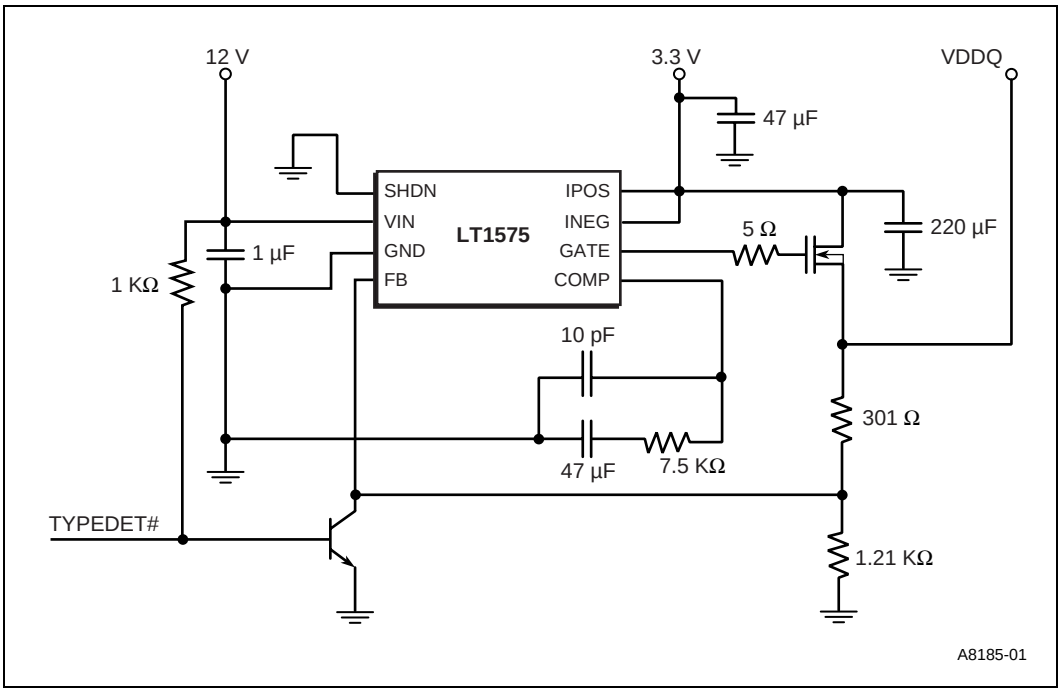
Table 9-3. TYPEDET# and V_{DDQ} Relationship

TYPEDET# (on the graphics add-in card)	V_{DDQ} (supplied by the motherboard)
GND	1.5 V
N/C	3.3 V

The motherboard must provide 3.3 V to the V_{CC} pins of the AGP connector. When the graphics controller requires a lower voltage, then the add-in card must regulate the 3.3 V V_{CC} voltage to the controller's requirement. The graphics controller may *only* power AGP I/O buffers with the V_{DDQ} power pins.

Because of this, a flexible voltage regulator must be used to supply the appropriate voltage to the V_{DDQ} pin on the AGP connector.

Figure 9-2. AGP VDDQ Generation Example



The example in Figure 9-2 demonstrates one way to design the V_{DDQ} voltage regulator. This regulator is a linear regulator with an external, low Rds_{on} FET. The source of the FET is connected to 3.3 V. This regulator will convert 3.3 V to 1.5 V or pass 3.3 V depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3 V (not 5 V) in order to control thermals (i.e., 5 V regulated down to 1.5 V with a linear regulator will dissipate approximately 7 W at 2 A). Because it must draw power from 3.3 V and, in some situations, must simply pass that 3.3 V to V_{DDQ} (when a 3.3 V add-in card is placed in the system), the regulator MUST use a low Rds_{on} FET.

AGP 1.0 ECR #44 modified $VDDQ3.3_{min}$ to 3.1 V. Using an ATX power supply, the 3.3 V_{MIN} is 3.168. Therefore, 68 mV of drop is allowed across the FET at 2 A. This corresponds to a FET with a Rds_{on} of 34 mΩ.

How does the regulator switch? The feedback resistor divider is set to 1.5 V. When a 1.5 V card is placed in the system, the transistor is off and the regulator regulates to 1.5 V. When a 3.3 V card is placed in the system, the transistor is on, and the feedback will be pulled to ground. When this happens, the regulator will drive the gate of the FET to nearly 12 V. This will turn the FET on and pass 3.3 V - 2A * Rds_{on} to V_{DDQ}.

9.3.6 V_{REF} Generation

3.3 V AGP cards generate V_{REF} locally. The cards have a resistor divider circuit which divides V_{DDQ} down to V_{REF}. To account for differences between V_{DDQ} and GND, 1.5 V cards use source-generated V_{REF}; that is, the V_{REF} signal is generated at the graphics controller and sent to the MCH, and another V_{REF} is generated at the MCH and sent to the graphics controller.

For 1.5 V add-in cards (only), both the graphics controller and the MCH are required to generate V_{REF} and distribute it through the connector. Two signals have been defined on the universal connector to allow V_{REF} passing:

- V_{REFGC} — V_{REF} from the graphics controller to the chipset
- V_{REFCG} — V_{REF} from the chipset to the graphics controller

The V_{REF} divider network should be placed near the AGP interface to achieve the common mode power supply effect. The minimum trace spacing around the V_{REF} signal must be 25 mils, in order to reduce crosstalk and maintain signal integrity. V_{REF} must be 0.4 VDDQ for 3.3 V operation and 0.5 VDDQ for 1.5 V operation. One example of a flexible VREF voltage divider circuit is shown in Figure 9-3 and Figure 9-4.

Figure 9-3. AGP 2.0 V_{REF} Generation and Distribution for 1.5 V Cards

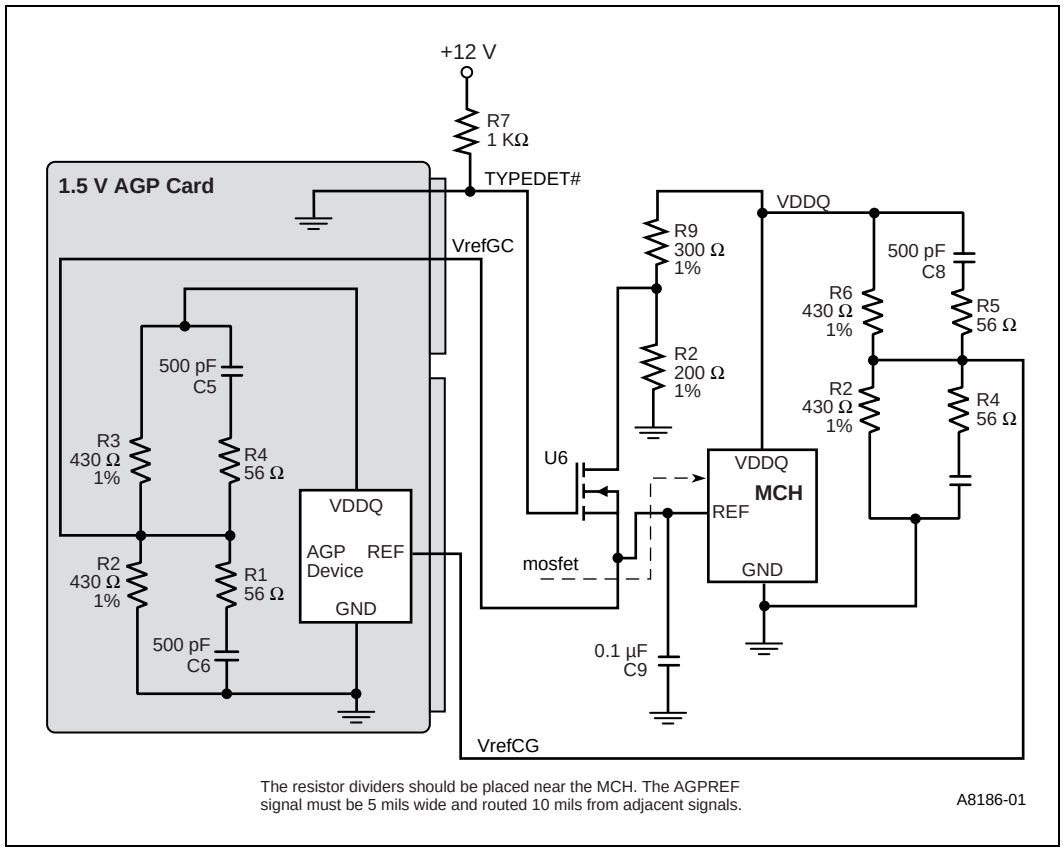
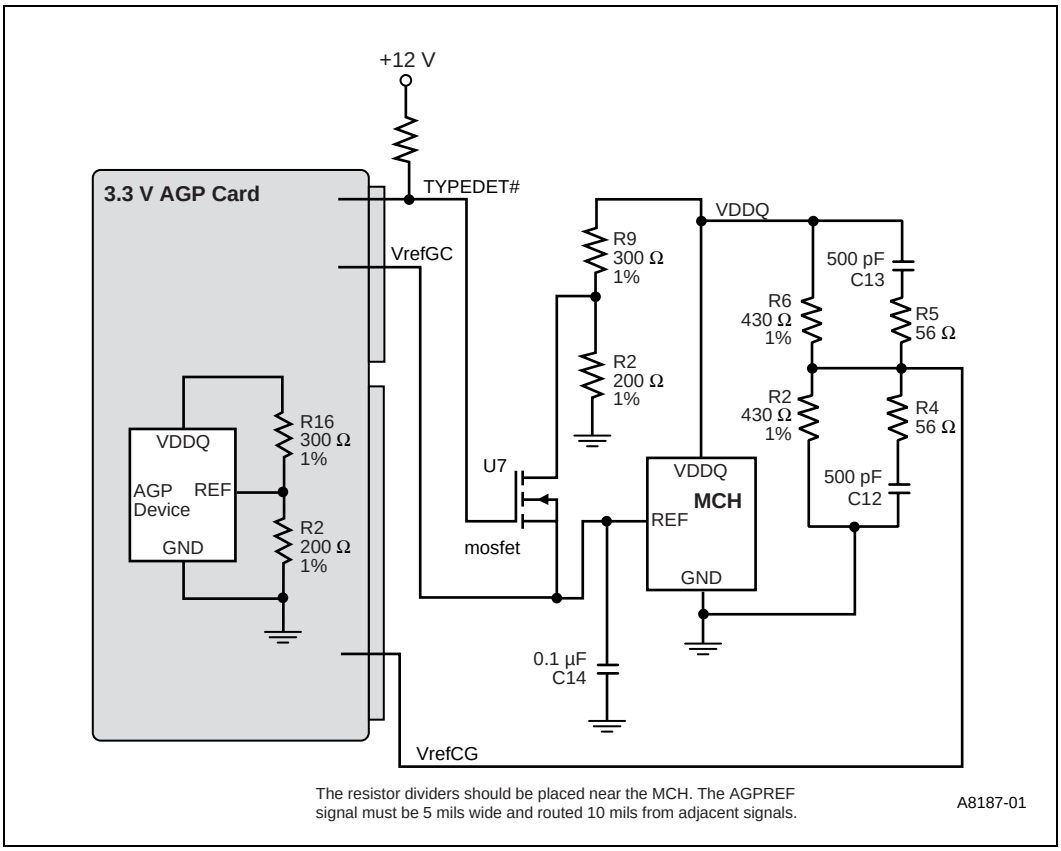


Figure 9-4. AGP 2.0 V_{REF} Generation and Distribution for 3.3 V Cards



9.3.7 Compensation

The MCH AGP interface supports resistive buffer compensation (AGPRCOMP). The AGPRCOMP signal must be tied to a 40 Ω - 2% or 39 Ω - 1% pull-down resistor to ground. This trace should be kept to 10 mils wide and less than 0.5” long.

9.3.8 AGP Pull-ups/Pull-down on AGP Signals

Some of the AGP signals may require either a pull-up resistor to V_{DDQ} (not $V_{CC3.3}$) or pull-down resistor to ground. This is to ensure that stable values are maintained when agents are not actively driving the bus. The recommended AGP pull-up/pull-down resistor value is 8.2 KΩ (4 KΩ $\leq R_{value} \leq$ 16 KΩ). The AGP interface does not require external termination.

The trace stub length to the pull-up/pull-down resistor should be kept to a minimum to avoid signal reflection. This trace length is different for 1X and 2X/4X modes. A summary is shown in Table 9-4.

Table 9-4. 1X AGP Pull-up/Pull-down Resistors

1X Timing Domain	
Signals	**PU/PD Requirement**
FRAME#	Pull-up resistor to V_{DDQ}
TRDY#	Pull-up resistor to V_{DDQ}
IRDY#	Pull-up resistor to V_{DDQ}
DEVSEL#	Pull-up resistor to V_{DDQ}
STOP#	Pull-up resistor to V_{DDQ}
SERR#	Pull-up resistor to V_{DDQ}
PERR#	Pull-up resistor to V_{DDQ}
RBF#	Pull-up resistor to V_{DDQ}
PIPE#	Pull-up resistor to V_{DDQ}
REQ#	Pull-up resistor to V_{DDQ}
WBF#	Pull-up resistor to V_{DDQ}
GNT#	Pull-up resistor to V_{DDQ}
ST[2:0]	Pull-up resistor to V_{DDQ}
INTA#	Pulled to 3.3 V
INTB#	Pulled to 3.3 V

The trace stub to the pull-up resistor on the 1X timing signals should be kept to less than 0.5”. This is to avoid signal reflections from the stub. The strobe signals require pull-up/pull-down on the motherboard to ensure stable values when there are no agents driving the bus, as shown in Table 9-5.

Table 9-5. 2X/4X AGP Pull-up and Pull-down Resistors

2X/4X Timing Domain	
Signals	**PU/PD Requirement**
AD_STB[1:0]	Pull-up resistor to V_{DDQ}
SB_STB	Pull-up resistor to V_{DDQ}
AD_STB[1:0]#	Pull-down resistor to GND
SB_STB#	Pull-down resistor to GND

The trace stub to the pull-up/pull-down resistor on the 2X/4X timing domain signals should be kept to less than 0.1” to avoid signals reflection from the stub. The recommended AGP pull-up/pull-down resistor value is 8.2 KΩ (4 KΩ $\leq R_{value} \leq$16 KΩ).

9.3.9 AGP Signal Voltage Tolerance List

The following AGP signals are 3.3 V tolerant during 1.5 V operation:

PME#
INTA#
INTB#
PERR#
SERR#
CLK
RST

The following AGP signals are 5 V tolerant (refer to the USB Specification for more details):

USB+
USB-
OVRCNT#

Note: The TYPDET# is a dedicated AGP signal. This is neither grounded nor no connect (N/C) on AGP cards. All other signals, in the V_{DDQ} group, are not 3.3 V tolerant during 1.5 V AGP operation.

9.3.10 AGP Connector

All AGP cards are either 3.3 V or 1.5 V cards. There are three types of AGP connectors: the 3.3 V AGP connector, 1.5 V AGP connector, and Universal connector. The Universal connector offers the most flexibility in a platform. Table 9-6 and Table 9-7summarize which cards and voltages work with which connectors.

Table 9-6. Connector/Add-in Card Interoperability

	1.5 V Connector	3.3 V Connector	Universal Connector
1.5 V Card	YES	NO	YES
3.3 V Card	NO	YES	YES

Table 9-7. Voltage/Data Rate Interoperability

	1X	2X	4X
1.5 V V_{DDQ}	YES	YES	YES
3.3 V V_{DDQ}	YES	YES	NO

9.3.11 Unused AGP interface

All recommended AGP pull-up and pull-down resistors are required, even when the MCH AGP interface is not used. AGP strobe signals (AD_STB0/AD_STB0#, AD_STB1/AD_STB1#, SB_STB/SB_STB#) can be left as no connects. In addition, the AGP Enable bit (AGP Command Register, offset A8-Abh) in the 840 MCH must be set to ‘0’.

Hub Interface 10

The MCH, ICH and P64H ballout assignment have been optimized to simplify the hub interface routing between these devices. Via transition should be minimized on the high-speed interface.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HL_STB). Figure 10-1 and Figure 10-2 provide 8-bit and 16-bit hub interface routing examples.

Figure 10-1. Hub Interface A (8-Bit) Routing Example

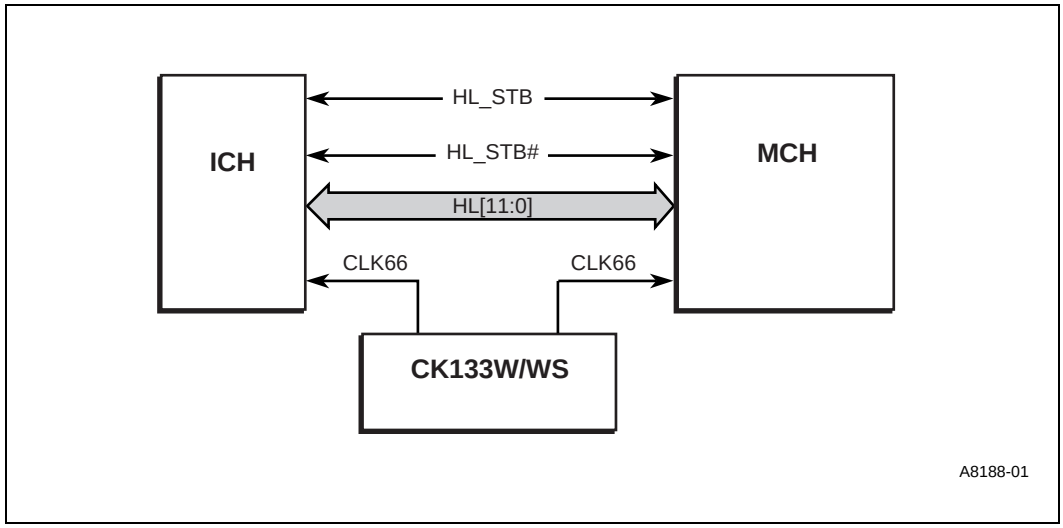
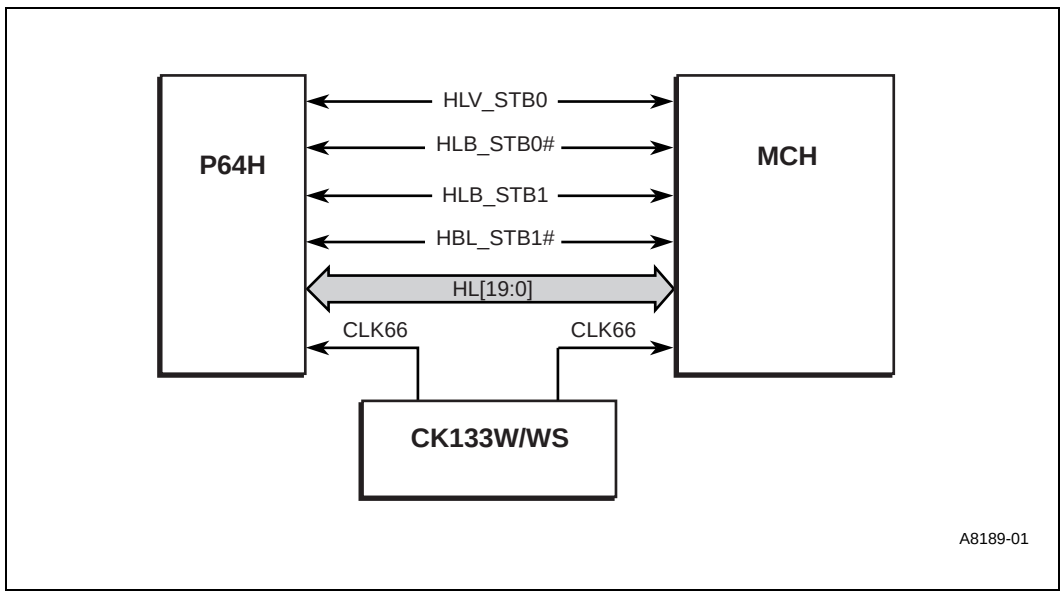


Figure 10-2. Hub Interface B (16-Bit) Routing Example



10.1 Hub Interface A (8-bit) to ICH

10.1.1 Hub Interface A Data Signals

Hub interface data signal traces should be routed 5 mils wide with 20 mils trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. In order to break out of the MCH and ICH package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mil of the package.

The maximum hub interface data signal trace length is 7". Each data signal must be matched within ± 0.1" of the HL_STB differential pair.

10.1.2 Hub Interface A Strobe Signals

The hub interface strobe signals should be routed 5 mils wide with 20 mils trace spacing (5 on 20). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signal is 7". The lengths for the strobe pair, HL_STB and HL_STB#, should be matched.

10.1.3 Hub Interface A (HLAREF) Generation/Distribution

HLAREF is the hub interface reference voltage for the Hub Interface A and should be 0.9 V ± 2% (0.5 * 1.8 V). This reference voltage can be generated with a single HREF divider circuit (example in Figure 10-3) or can be generated locally (example in Figure 10-4).

Figure 10-3. MCH/ICH Single Hub Interface Reference Divider Circuit

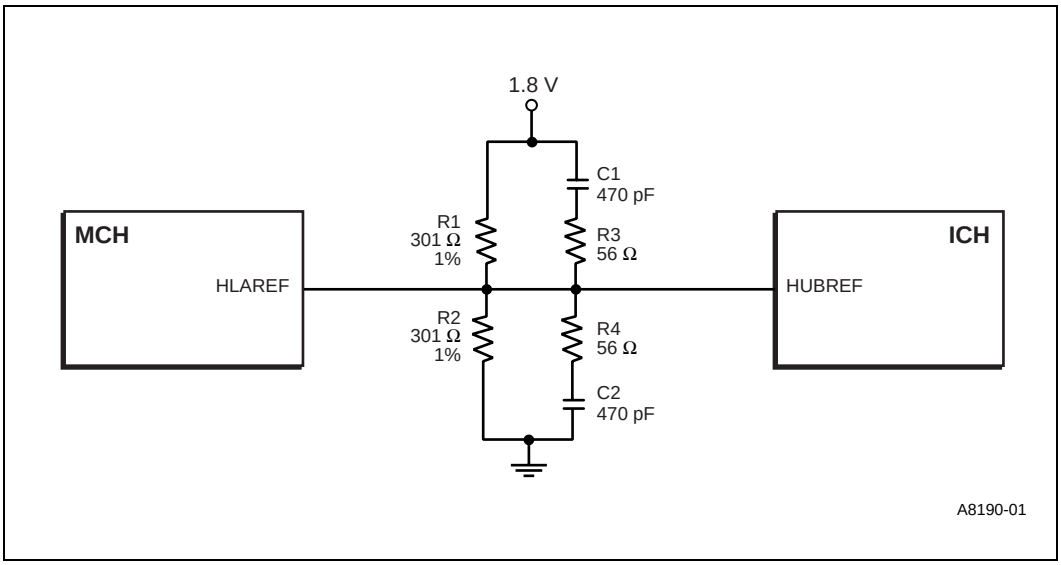
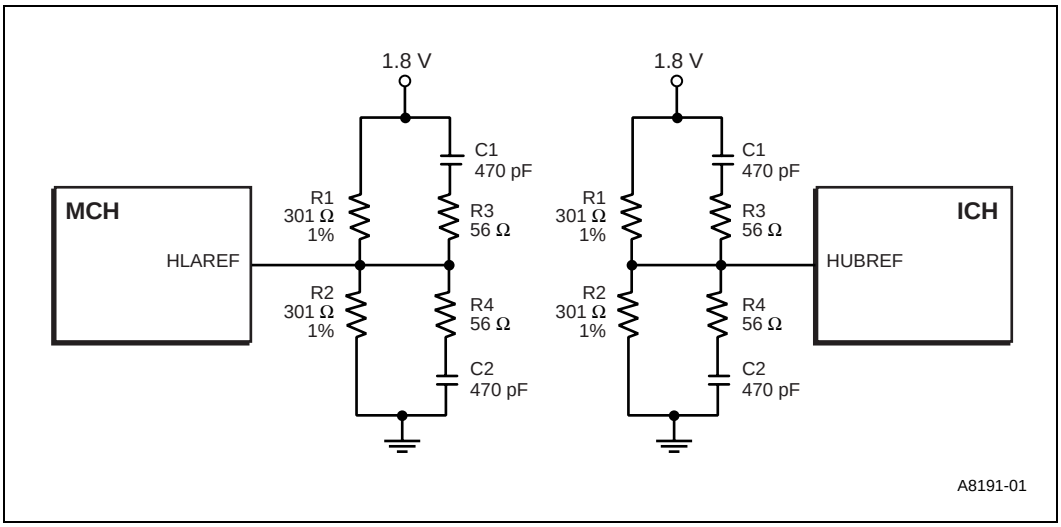


Figure 10-4. MCH/ICH Locally Generated Hub Interface Reference Divider Circuit



The resistor values, R1 and R2, must be equal and rated at 1% tolerance. These selected resistor values must also ensure that the reference voltage tolerance is maintained over the input leakage specification. The recommended resistor and capacitor values (R3, R4, C1, C2) for controlling signal overshoot and undershoot are $\leq$ 80 Ω and 470 pF respectively. Also (not shown), individual component reference voltage should be bypassed to ground via a 0.1 µF capacitor at the device.

10.1.4 Hub Interface A Compensation

There are two options for the MCH and ICH hub interface compensation. HLCOMP is used by the ICH to adjust the buffer characteristics to specific board characteristics. The compensation can be either Impedance Compensation (ZCOMP) or Resistive Compensation (RCOMP).

- RCOMP: Tie the HLCOMP pins to a 40 Ω-2% or 39 Ω-1% pull-up resistor to 1.8 V. This trace should be kept at less than 0.5” length and 10 mils wide trace.
- ZCOMP: The HLCOMP signals are routed via an 18” minimum length and 10 mil wide trace. This trace must be non-terminated and must not cross power plane splits. 15-20 mils separation between this signal and adjacent signal is recommended.

The MCH hub interface compensation for hub interface A can support either compensation methods. The same compensation method should be used at the MCH and ICH.

10.2 Hub Interface B (16-bit) to P64H

10.2.1 Data Signals

Hub interface data signal traces should be routed 5 mil wide with 20 mil trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. In order to break out of the MCH and P64H package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mil of the package.

The hub link interface B has minimum and maximum requirements. The minimum trace length for all hub interface B signals is 4.5”. The maximum hub interface signal trace length is 16”. Each data signal must be matched within ±0.1” of the HL_STB[1:0] differential pairs. There is no length match requirement between the data signals.

10.2.2 Strobe Signals

The hub interface strobe signals should be routed 5 mil wide with 20 mil trace spacing (5 on 20). This strobe pair should have a minimum of 20 mil spacing from any adjacent signals. The minimum trace length for the strobe signals is 4.5”. The maximum length for the strobe signals is 16”. The lengths for all of the strobe signals, HLB_STB0, HLB_STB0#, HLB_STB1 and HLB_STB1#, should be matched.

10.2.3 Hub Interface B HUBREF Generation/Distribution

HUBREF is the hub interface reference voltage and should be 2/3 V_{TERM}. This reference can be generated locally or with a single HREF divider circuit. A HREF divider circuit example is shown in Figure 10-5.

Figure 10-5. MCH/P64H Single Hub Interface Reference Divider Circuit

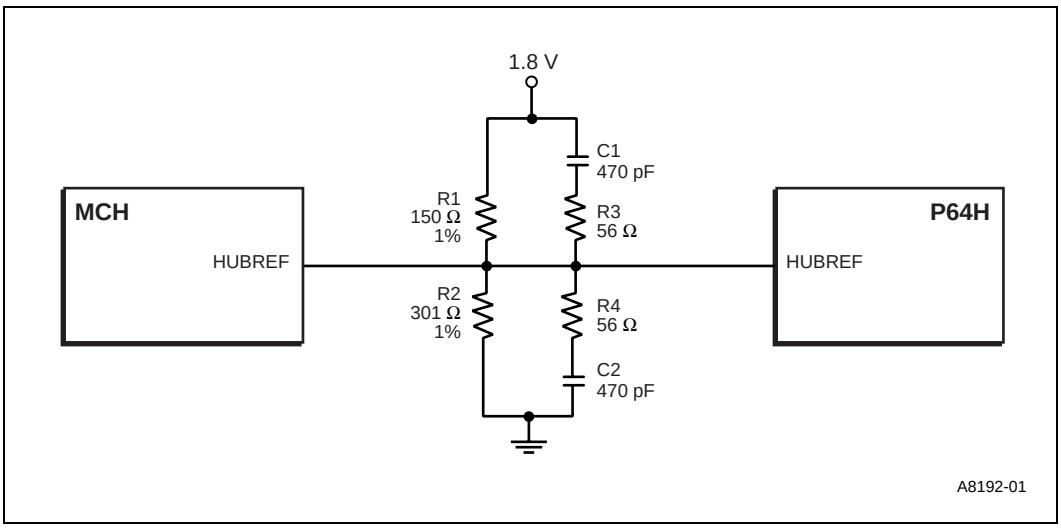
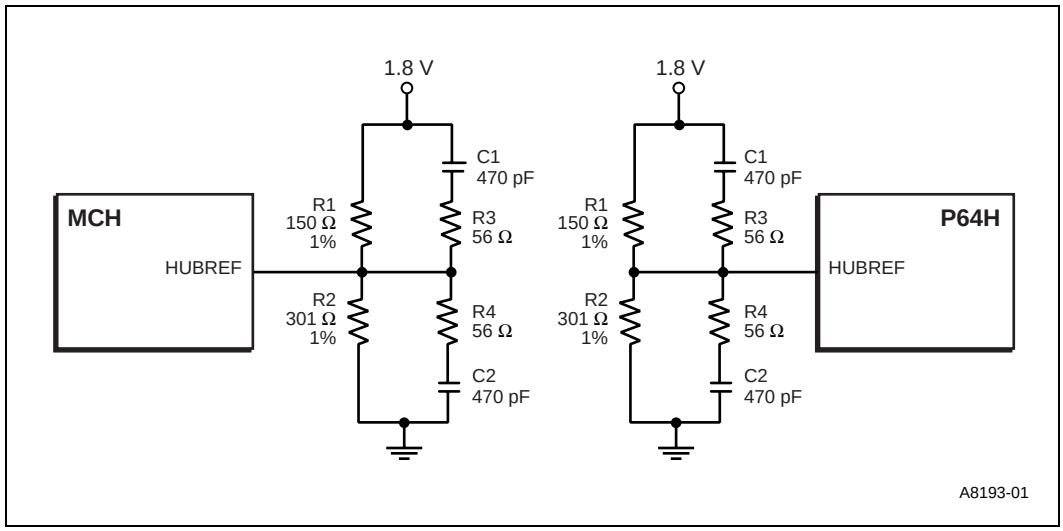


Figure 10-6. MCH/P64H Locally Generated Hub Interface Reference Divider Circuit



The resistor values, R1 and R2, must be rated at 1% tolerance. These selected resistor values must also ensure that the reference voltage tolerance is maintained over the input leakage specification. The recommended resistor and capacitor values (R3, R4, C1, C2), for controlling signal overshoot and undershoot, are $\leq$ 80 Ω and 470 pF respectively. Also, the reference voltage should be bypassed to ground via a 0.1 µF capacitor.

10.2.4 HLB_RCOMP Signal

HLB_RCOMP is used by the P64H to adjust the buffer characteristics to specific board characteristics. The HLB compensation requires Resistive Compensation (RCOMP).

- RCOMP: Tie the HLB_COMP pins to a 30 Ω-1% pull-down resistor to GND. This can done using a 10 mil wide trace and short (~0.5”) trace.

The MCH hub interface compensation for hub interface B must use the same compensation method (RCOMP).

10.2.5 Unused Hub Interface B

When the hub interface B is not used, all HLB signals except the MCH HUBREF and HLBRCOMP can be left as No Connect on the Intel® 840 chipset MCH. Note that 2/3 V_{TERM} must be applied to HUBREF even if hub interface B is not used. Also, a 30 Ω ±1% pulled-down resistor to GND is required on HLBRCOMP. When the 840 chipset MCH detects that the P64H is not present, it will internally maintain the HLB signals at a “High” state and disable the P2P bridge for the hub interface B (MCH device 2).

Ultra ATA/66 11

This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels.

The ICH has two independent IDE channels. The ICH integrates the 33 Ω series resistors that are typically required on the IDE data signals, running to the two ATA connectors. The IDE interface can be routed with 5 mil traces on 5 mil spaces, but must be less than 8” long (from ICH to IDE connector). Per each IDE channel, the difference between the shortest and longest signal must not be greater than 0.5”.

11.1 Cable Requirement

A new IDE cable is required for Ultra ATA/66. This cable is an 80-pin conductor cable; however, the 40-pin connectors do not change. The wires in the cable alternate: ground, signal, ground, signal, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6” between drive connectors on the cable. When a single drive is placed on the cable it should be placed at the end of the cable. When a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **ICH Placement:** The ICH must be placed equal to OR less than 8” from the ATA connector(s).
- **PC99 requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft PC99. CSEL signal needs to be pulled down at the host side by using a 470 Ω pull-down resistor for each ATA connector.

11.2 Ultra ATA/66 Cable Detection

The ICH supports many Ultra DMA modes including ATA/66. The ICH needs to determine the installed IDE device mode and the type of cable to configure its own hardware and software to support it.

To determine if ATA/66 mode can be enabled, the Intel® 840 chipset requires the system BIOS to determine the cable type used in the system. There are two methods for the BIOS:

1. Host Side Detection
2. Device Side Detection

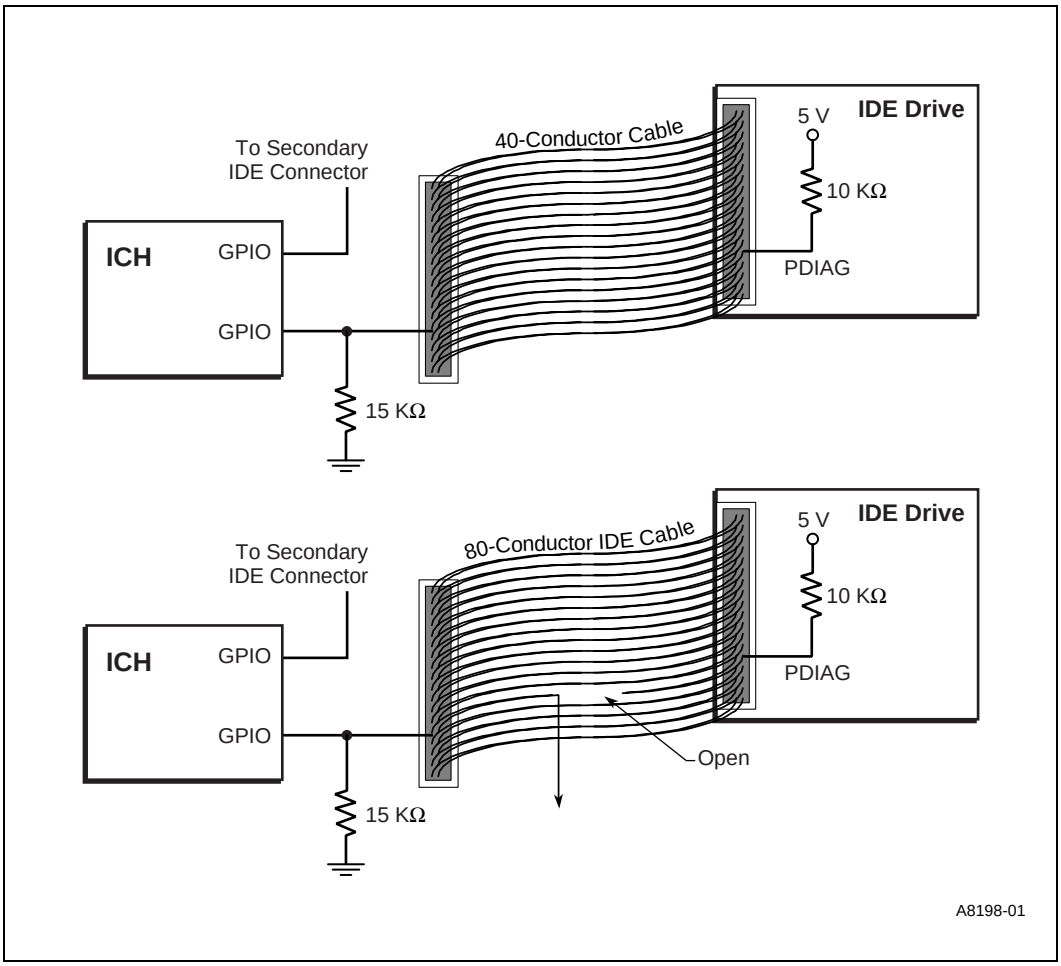
If the BIOS detects an 80-conductor cable, it may be used with any Ultra DMA mode up to the highest transfer mode supported by both the ICH and the IDE device. Otherwise, the BIOS will only enable modes that do not require an 80-conductor cable (i.e., Ultra ATA/33 Mode). After the BIOS determines the Ultra DMA mode, the BIOS will configure the ICH hardware and software to match the selected mode.

11.2.1 Host Side Detection-BIOS Detects Cable Type Using GPIOs

Host side detection requires the use of two GPI pins (one per IDE controller). The proper way to connect the PDIAG/CBLID signal of the IDE connector to the host is shown in Figure 11-1. Most of the ICH GPIO and all FWH GPIs are not 5 V-tolerant. Since all IDE devices have a 10 KΩ pull-up resistor to 5 V, a resistor divider circuit is needed to protect ICH and FWH from 5 V signaling. One suggestion, a 10/15 KΩ resistor divider circuit, will produce approximately 3 V for a logic high.

This mechanism allows the host, after diagnostics, to sample PDIAG/CBLID. If PDIAG/CBLIB is high then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG/CBLID is low, then there is an 80-conductor cable in the system.

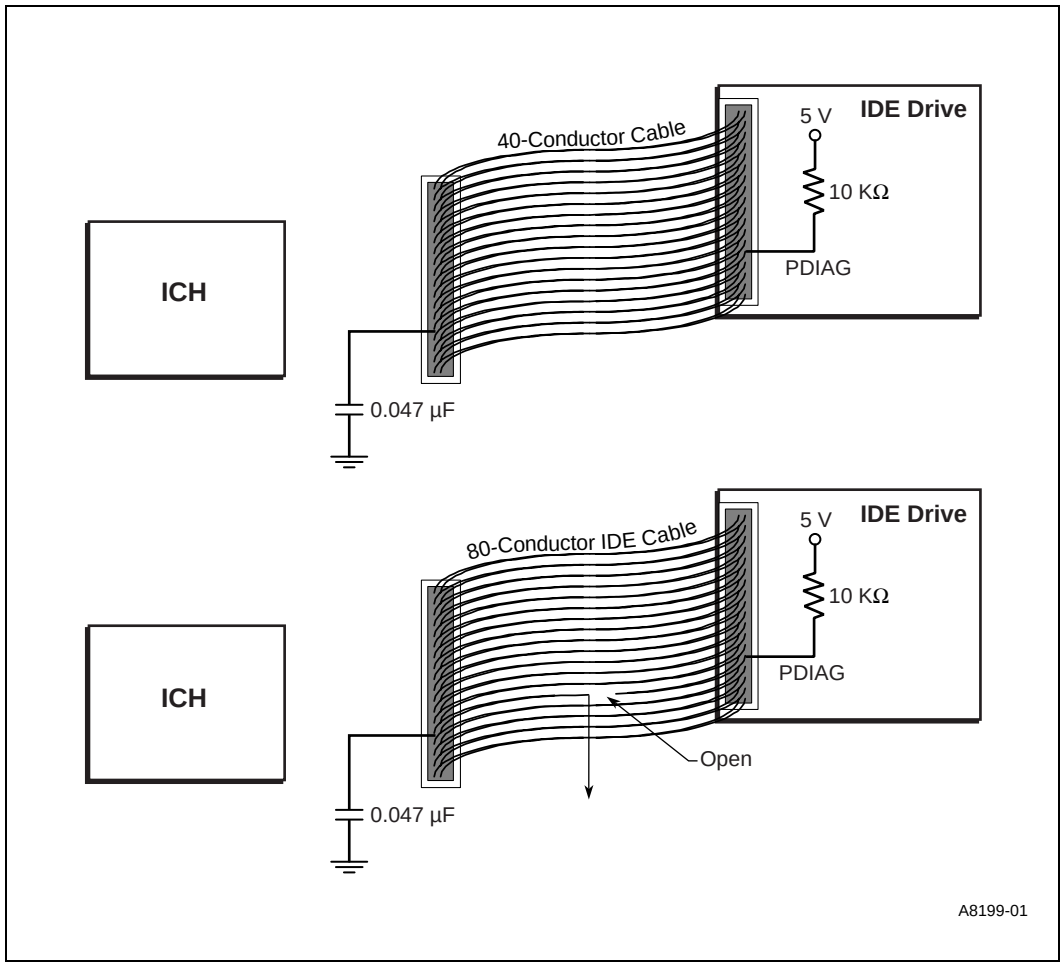
Figure 11-1. Host Side IDE Cable Detection #1



11.2.2 Device Side Detection-BIOS Queries IDE Drive for Cable Type

Device side detection requires only a 0.047 µF capacitor on the motherboard as shown in Figure 11-2. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 will drive PDIAG/CBLID low and then release it (pulled up through a 10 KΩ resistor). The drive will sample the PDIAG signal after releasing it. In an 80-conductor cable, PDIAG/CBLID is not connected, therefore the capacitor has no effect. In a 40-conductor cable, PDIAG/CBLID is connected to the drive, thus the signal will rise more slowly. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

Figure 11-2. Driver Side IDE Cable Detection #2



11.3 Layout for Host Side and Driver Side Cable Detection

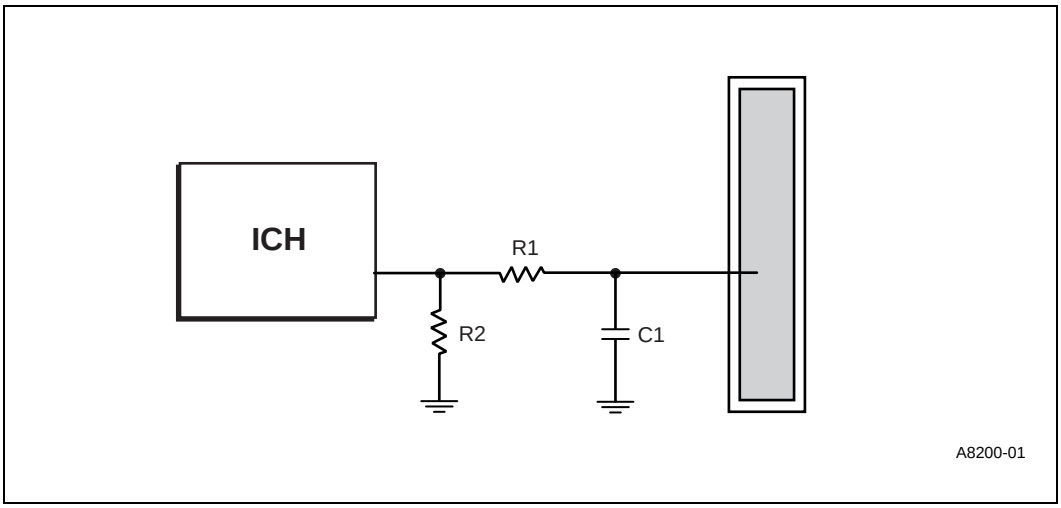
For Host-Side Detection:

- R1 is a 0 Ω resistor
- R2 is a 15 Ω resistor
- C1 is not stuffed

For Driver-Side Detection

- R1 is not stuffed
- R2 is not stuffed
- C1 is a 0.047 µF capacitor

Figure 11-3. Driver-side IDE Detection Layout

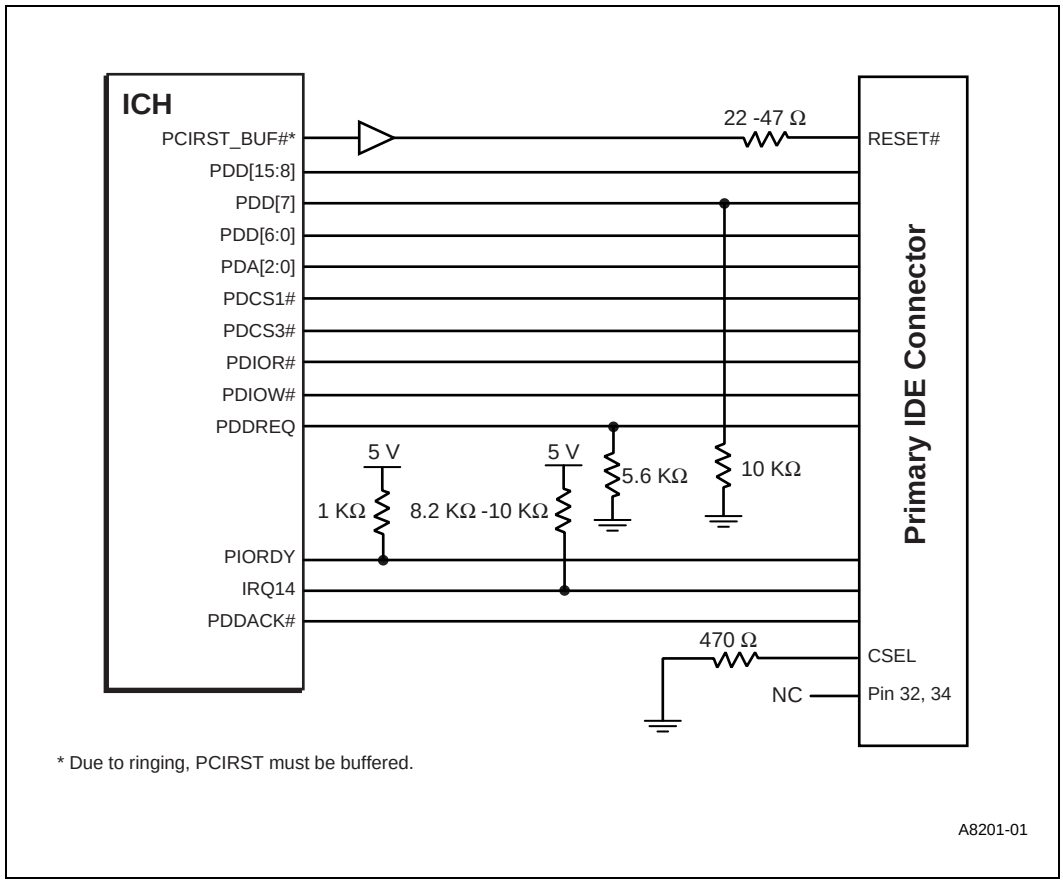


11.4 Guidelines

- 22 Ω - 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- A 8.2 KΩ-10 KΩ pull-up resistor is required on IRQ14 and IRQ15 to V_{CC5}.
- A 10 KΩ pull-down resistor is required on PDD7 and SDD7 (as required by the ATA-4 specification).
- A 5.6 KΩ pull-down resistor is required on PDDREQ# and SDDREQ# (as required by the ATA-4 specification).
- A 1 KΩ pull-up resistor is required on PIORDY and SIORDY (as required by the ATA-4 specification).

Figure 11-4 illustrates resistor placement for primary and secondary IDE connectors.

Figure 11-4. Resistor Placement for Primary and Secondary IDE Connector



If the IDE interface is not used, the respective xDREQ and xIORDY signals should be grounded and output signals left as No Connects. If both of the primary and secondary IDE interfaces are not used, the appropriate ICH bit should also be set to disable the IDE controller.

AC ’97 12

The ICH implements an AC ’97 2.1-compliant digital controller. Any codec used with the ICH AC-link must be AC ’97 2.1 compliant. Please contact your codec hardware vendor for information on AC ’97 2.1 compliant products. The AC ’97 2.1 specification is available on the Intel web site:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The ICH supports the following codec combinations:

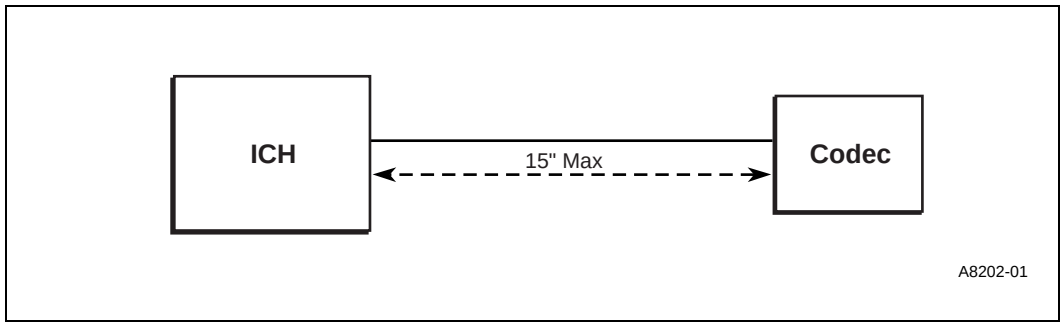
Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in the table, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

12.1 AC ’97 Codec-only

When implementing the codec-only solution, unused SDIN signal must be pulled-down to GND using a weak resistor (~10 KΩ).

Figure 12-1. Codec-only Topology Trace Length Requirements



12.2 Audio/Modem Riser Specification

Intel has developed a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM to add a plug-in card option. The AMR specification provides a mechanism for AC ’97 codecs to be on a riser card. This is important for modem codecs as it helps ease international certification of the modem. The Audio/Modem Riser Specification is available on the Intel web site:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

For increased part placement flexibility, there are two routing methods for the AC ’97 interface: the *tee* topology (see Figure 12-2) and the *daisy-chain* topology (see Figure 12-3). The AC ’97 interface can be routed using 5 mil traces with 5 mil space between the traces.

Figure 12-2. Tee Topology Trace Length Requirements

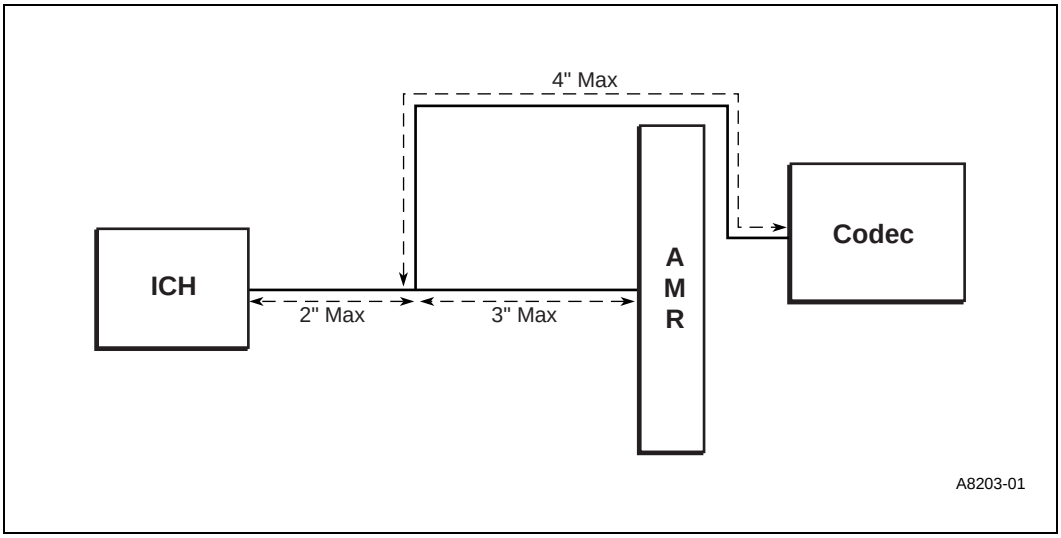
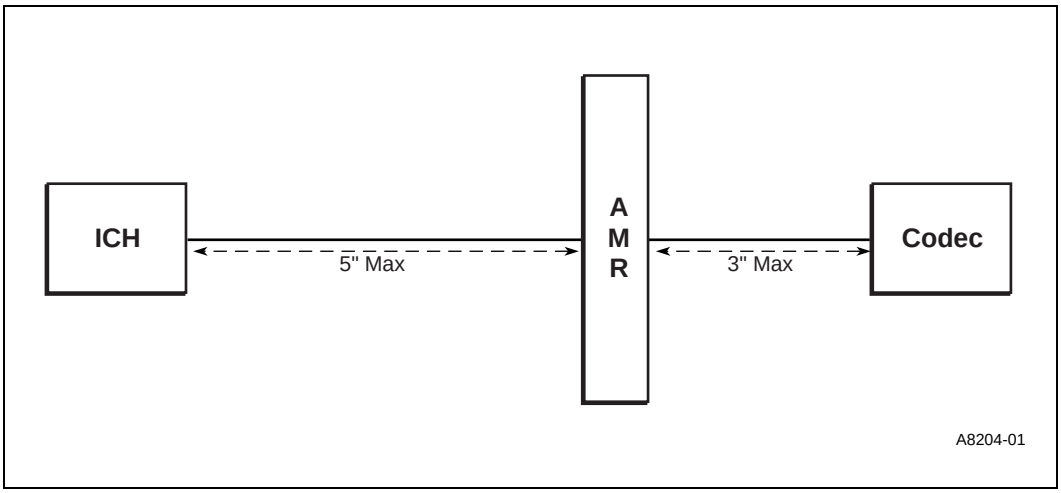


Figure 12-3. Daisy-Chain Topology Trace Length Requirements



Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH), and any other codec present. This clock is used as the time base for latching and driving data.

The ICH supports wake on ring from S1-S4 via the AC '97 link. The codec will assert SDATAIN to wake the system. For wake capability and/or caller ID, standby power must be provided to the modem codec.

There are integrated pull-down resistors on the ICH AC_SDIN0 and AC_SDIN1/GPIO9 signals. The pull-down resistor on these signals is only enabled when the ACLINK Shut Off bit, in the AC '97 Global Control Register (AC '97 I/ O Space) is set to '1'. This will prevent the link from floating when the AC-link is off or when there is no codec present. Otherwise, the internal pull-down resistor is disabled and an external pull-down resistor is required.

12.3 AC '97 Signal Quality Requirements

In a lightly loaded system (e.g., single codec down), AC '97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented in order to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC '97 2.1 specification with the specified load of 50 pF.

12.4 AC '97 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH platform using AC '97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. These recommendations do not represent the only implementation or a complete checklist, but provides recommendations based on the ICH platform.

- Codec Implementation
  - — The motherboard can implement any valid combination of codecs on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on the AMR module; however, nothing precludes a modem codec on the motherboard.
  - — Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH platform.
  - — If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground.
  - — The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
  - — Components such as FET switches, buffers, or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so may interfere with timing margins and signal integrity.

— If the motherboard requires that an AMR module override a primary codec down, a means of preventing contention on the AC-link must be provided for the on-board codec.

— The ICH supports Wake On Ring from S1-S4 states via the AC '97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pulldowns will prevent the inputs from floating, therefore external resistors are not required. The ICH does not wake from the S5 state via the AC '97 link.

— The SDATAIN[1:0] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10 KΩ) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH's internal pull-down resistors are enabled, and thus there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that has the potential of not being connected to a codec*. For example, if a dedicated audio codec is on the motherboard, and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. If however, the SDATAIN signal has no codec connected, or is connected to an AMR slot, or is connected to an on-board

— Codec that can be hardware disabled, then the signal should have an external pull-down resistor to ground.

- AMR Slot Special Connections
  — AUDIO_MUTE#: No Connect on the motherboard.
  — AUDIO_PWRDN: No Connect on the motherboard. Codecs on the AMR card should implement a powerdown pin, per the AC '97 2.1 specification, to control the amplifier.
  — MONO_PHONE: Connect top on-board audio codec if supported.
  — MONO_OUT/PC_BEEP: Connect to SPKR output from the ICH, or MONO_OUT from on-board codec.
  — PRIMARY_DN#: See discussion above.
  — +5VDUAL/+5VSB: Connect to V_{CC5} core on the motherboard, unless adequate power supply is available. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
  — S/P-DIF_IN: Connect to ground on the motherboard.
  — AC_SDATAIN[3:2]: No connect on the motherboard. The ICH supports a maximum of two codecs, which should be attached to SDATAIN[1:0].
  — AC97_MSTRCLK: Connect to ground on the motherboard.
- The ICH provides internal weak pulldowns. Therefore, the motherboard does not need to provide discrete pulldown resistors.

PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

Universal Serial Bus (USB) 13

General USB guidelines:

- Unused USB ports should be terminated with 15 KΩ pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH (<1"). These series resistors are there for source termination of the reflected signal.
- 47 pF caps must be placed as close to the ICH as possible and on the ICH side of the series resistors on the USB data lines (P0+/-, P1+/-). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 K +/-5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/-, P1+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0+/-, P1+/- signals should be 45 Ω (to ground) for each USB signal P+ or P-. The suggested board stack-up (eight-layer board stack-up and 60 Ω ± 10% board impedance), requires that the traces be 9 mils wide. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as ‘critical signals’ (i.e., hand routing preferred). The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces helps prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length to minimize the effect of common mode current on EMI.

Figure 13-1 illustrates the recommended USB schematic, and Table 13-1 provides recommended trace values.

Figure 13-1. USB Data Signals

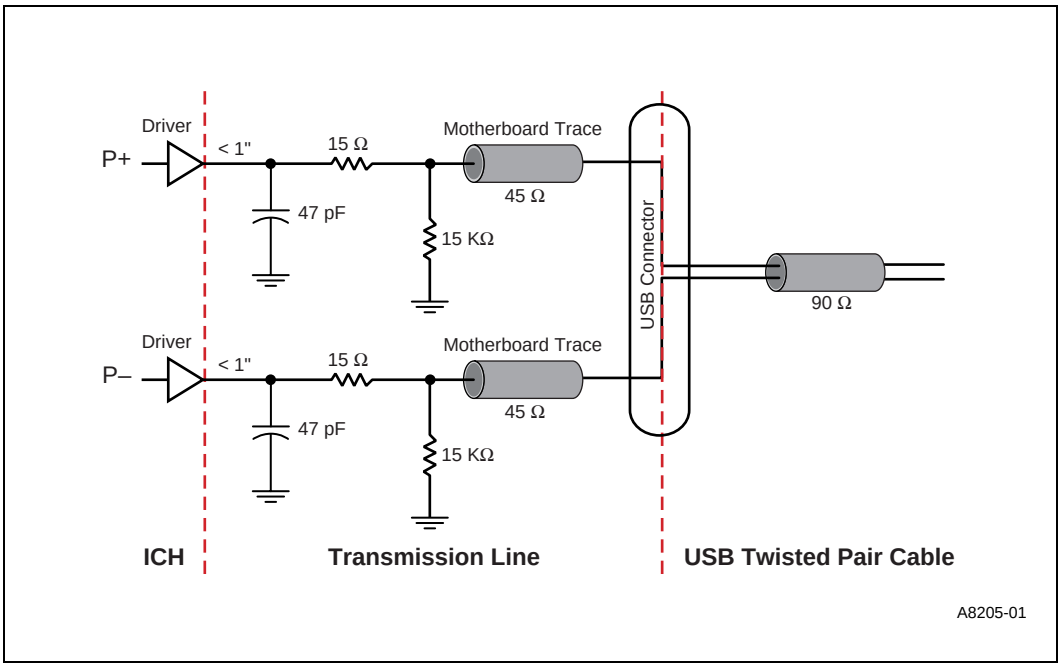


Table 13-1. Recommended USB Trace Characteristics

Impedance ‘Z0’	45.4 Ω
Line Delay	160.2 ps
Capacitance	3.5 pF
Inductance	7.3 nH
Res @ 20° C	53.9 mΩ

Low Pin Count Interface (LPC)/FWH 14

14.1 In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH is set for subtractive decode, these boot cycles can be accepted by a positive decode agent out on PCI. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot off a PCI card, it is necessary to keep the ICH in subtractive decode mode. If a PCI boot card is inserted and the ICH is programmed for positive decode; there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot off a ROM behind the 82380AB/AC. Once you have booted from the PCI card, you could potentially program the FWH in-circuit and program the ICH CMOS.

14.2 FWH V_{PP} Design Guidelines

The V_{pp} pin on the FWH is used for programming the flash cells. The FWH supports V_{pp} of 3.3 V or 12 V. If V_{pp} is 12 V, the flash cells will program about 50% faster that at 3.3 V. However, the FWH only supports 12 V V_{pp} for 80 hours. The 12 V V_{pp} would be useful in a programmer environment. The V_{pp} pin on the FWH needs to be tied to 3.3 V for normal operation.

RTC 15

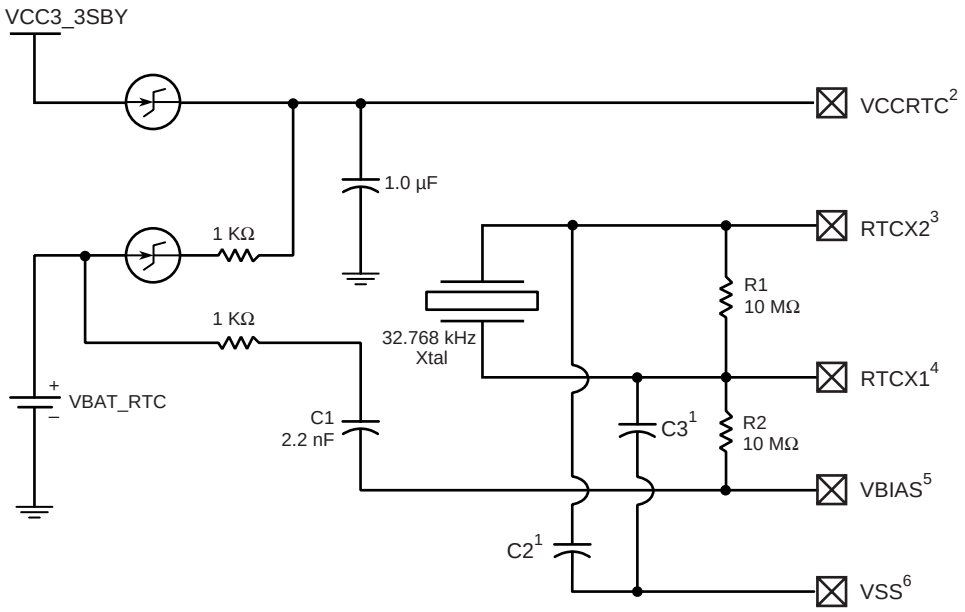
The ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. This internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down. The RTC also maintains the CMOS memory used by the BIOS, and a backup battery to keep the clock running and the CMOS fresh when the PC is switched off.

Please note that the ICH RTC implementation is different than the implementation for PIIX4E.

15.1 RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 pins. Figure 15-1 represents the external circuitry that comprises the oscillator of the ICH RTC.

Figure 15-1. External Circuitry for ICH RTC



1. The exact capacitor value needs to be based on what the crystal maker recommends.
2. VCCRTC: Power for RTC Well
3. RTCX2: Crystal Input 2 - Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1 - Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage - This pin is used to provide a reference voltage, and this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
6. V_{SS}: Ground

A8206-01

15.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 must be set to 2.2 nF and the external capacitor values (C2 and C3) should be chosen to support the manufacturer's specified load capacitance (C_{load}) for the crystal. The values should also account for C_{load} with parasitic capacitance of the trace, socket (if used), and package. By adding the external capacitor values with the capacitance of the trace, socket, and package, the capacitor value will be better matched to the actual load capacitance of the crystal used.

The following equation can be used to choose the external capacitance values (C2 and C3):

$C_{load} = (C2* C3)/(C2+C3) + C_{parasitic}$

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 KHz.

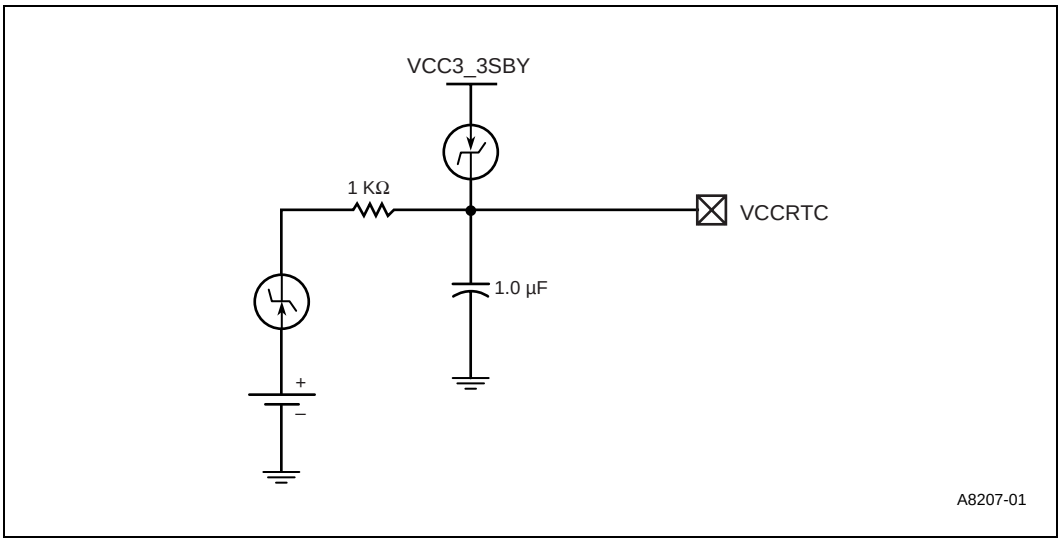
15.3 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system. Example batteries are: Duracell 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least: 170,000 µAh / 3 µA = 56,666 h = 6.4 years.

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 15-2 is an example of a diode circuitry that can be used.

Figure 15-2. A Diode Circuit to Connect RTC External Battery



A standby power supply should be used to provide continuous power to the RTC when available. This will significantly increase the RTC battery life and the RTC accuracy.

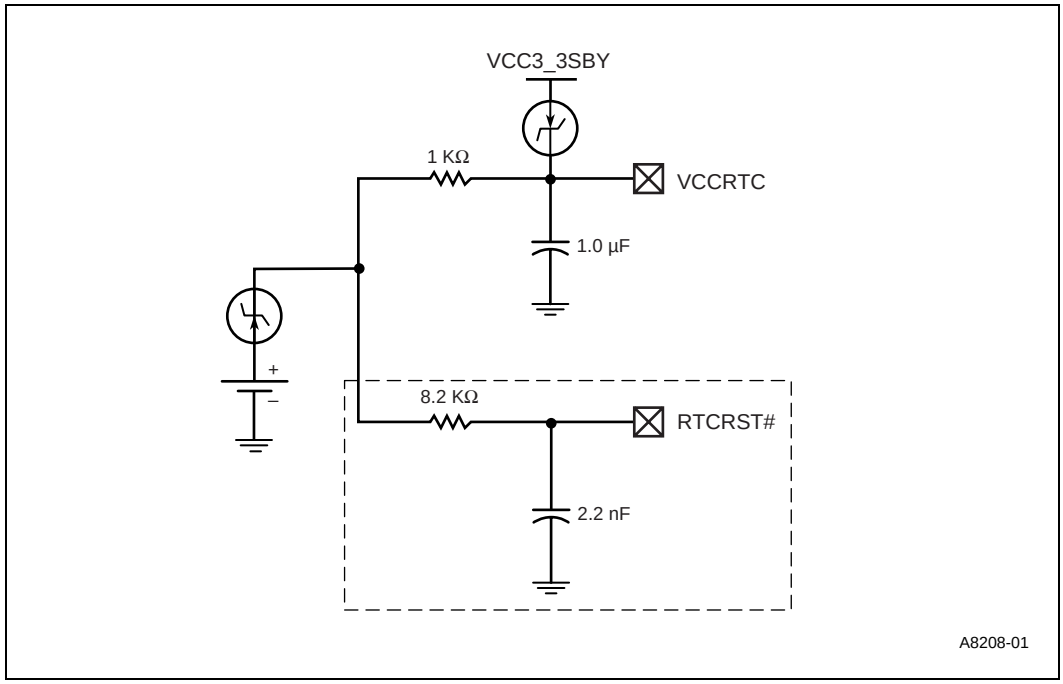
15.4 RTC External RTCRST Circuit

The ICH RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC Well. The external capacitor (2.2 µF), external resistor (8.2 KΩ) and the RTC battery (V_{bat}) were selected to create a RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10-20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set and remains '1' until software clears it. As a result of this, when the system boots, the BIOS will know if the RTC battery has been removed.

This RTCRST circuit is combined with the diode circuit which allows RTC-well to be powered by the battery when the system power is not available.

The RTCRST external circuit for the ICH RTC is shown in Figure 15-3.

Figure 15-3. RTCRST External Circuit for the ICH RTC



15.5 VBIAS Clarification

15.5.1 RTC Routing Guidelines

All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1”. It is recommended to minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them), and place a ground plane under all of the external RTC circuitry. Do not route any switching signals under the external components (unless on the other side of the ground plane).

15.5.2 VBIAS DC Voltage and Noise Measurements

Steady state VBIAS will be a DC voltage of about 0.38 V +/- .06 V. VBIAS will be “kicked” when the battery is inserted to about 0.7-1.0 V, but it will come back to its DC value within a few ms.

Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely. Therefore, it is important to minimize the noise, to 200 mV or less, on VBIAS. To minimize noise of VBIAS, implement the above routing guidelines and the external RTC circuitry described in the ICH datasheet.

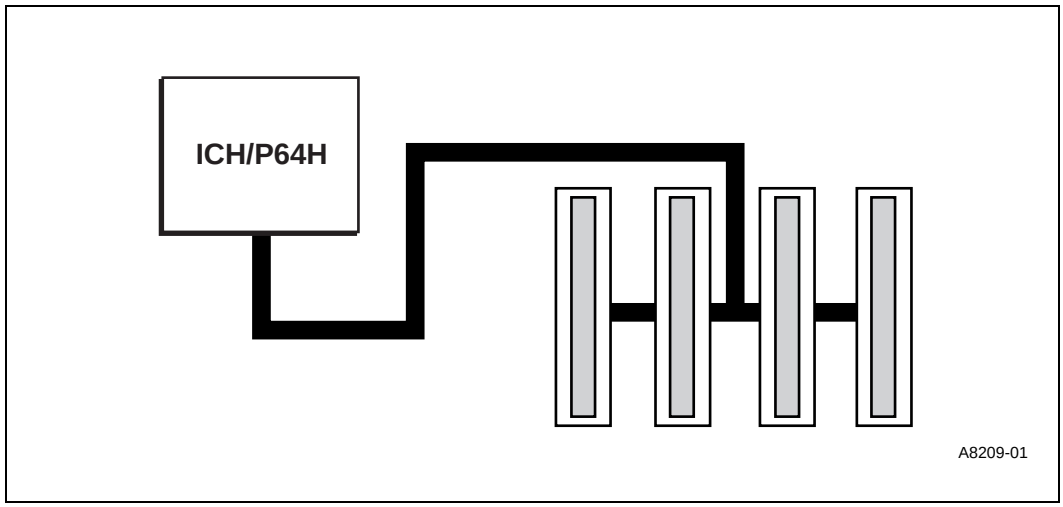
Please also note that VBIAS is very sensitive and cannot be directly probed. It can be probed through a .01 µF capacitor.

The Intel® 840 chipset offers support for both 33 MHz and 66 MHz PCI operations. The ICH supports 33 MHz and the P64H supports both 33/66 MHz PCI operations. The ICH and P64H each provide six pairs of REQ#/GNT# signals, supporting six PCI masters. In addition, the ICH supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

16.1 PCI 33 MHz Guidelines

The ICH and P64H both provide PCI Bus interface that is compliant with the *PCI Local Bus Specification*, Revision 2.2. This implementation, illustrated in Figure 16-1, is optimized for high-performance data streaming when either ICH or P64H is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification*, Revision 2.2.

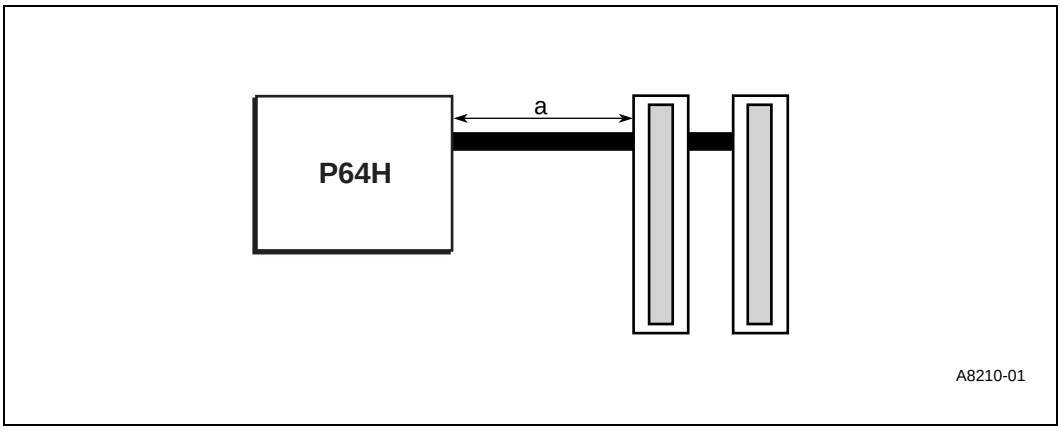
Figure 16-1. PCI 33 MHz Bus Layout Example



16.2 PCI 66 MHz Guidelines

The P64H provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the P64H is acting as either the target or the initiator on the PCI bus. See Figure 16-2. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification*, Revision 2.2.

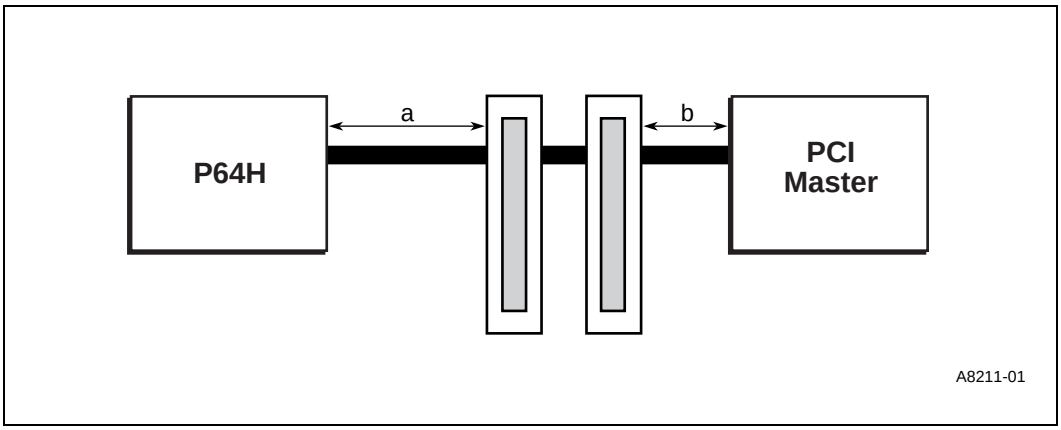
Figure 16-2. PCI 66 MHz — 2 Slots Only



All of the PCI 66 MHz signals can be routed using 5 mil traces with 7 mil spacing between the traces. The following guidelines apply to Figure 16-2:

- (a) P64H to first 66 MHz slot connector length: a ≤ 13”
- The typical spacing between PCI connectors is 0.8”

Figure 16-3. PCI 66 MHz — 2 Slots w/ 1 Device Down



All of the PCI 66 MHz signals can be routed using 5 mil traces with 7 mil spacing between the traces. The following guidelines apply to Figure 16-3:

- (a) P64H to first 66 MHz slot connector length: 0” ≤ a ≤ 6”
- (b) Second 66 MHz slot to PCI device down length: 1” ≤ b ≤ 5”
- The typical spacing between PCI connectors is 0.8”

Clocking 17

There are three clock generator components required in a Intel® 840 chipset platform. Two Direct Rambus* Clock Generators (DRCGs) generate the clock for the RDRAM interface and a CK133W/S clock generator is used for the other platform components. Clock synthesizers that meet the *CK98W/S Clock Synthesizer/Driver Specification* and DRCG specification are suitable for an Intel 840 chipset system.

17.1 CK133W

The CK133W pinout is identical to that of the CK133, but limits CPU clock jitter to 150 ps. The clocks generated by CK133W are described in Table 17-1.

Table 17-1. Intel® 840 Chipset System Clocks w/ CK133W

# of Clocks	Name	Routed to		Frequency	Voltage
4	CPUCLK[3:0]	Two processors MCH ITP	CLK HCLKIN BCLK	100/133 MHz	2.5 V
3	APIC[2:0]	2 processors P64H ICH	PICCLK APICCLK APICCLK	16.667 MHz	2.5 V
8	PCICLK[7:0]	PCI Devices ICH FWH LPC	CLK PCICLK CLK CLK	33 MHz	3.3 V
4	3V66[3:0]	MCH ICH P64H AGP	CLK66 CLK66 CLK66 CLK	66 MHz	3.3 V
2	REF[1:0]	ICH SIO	CLK14	14.318 MHz	3.3 V
1	48MHz	ICH	CLK48	48 MHz	3.3 V
2	CPU_DIV2[1:0]	DRCG	REFCLK	50/66 MHz	2.5 V

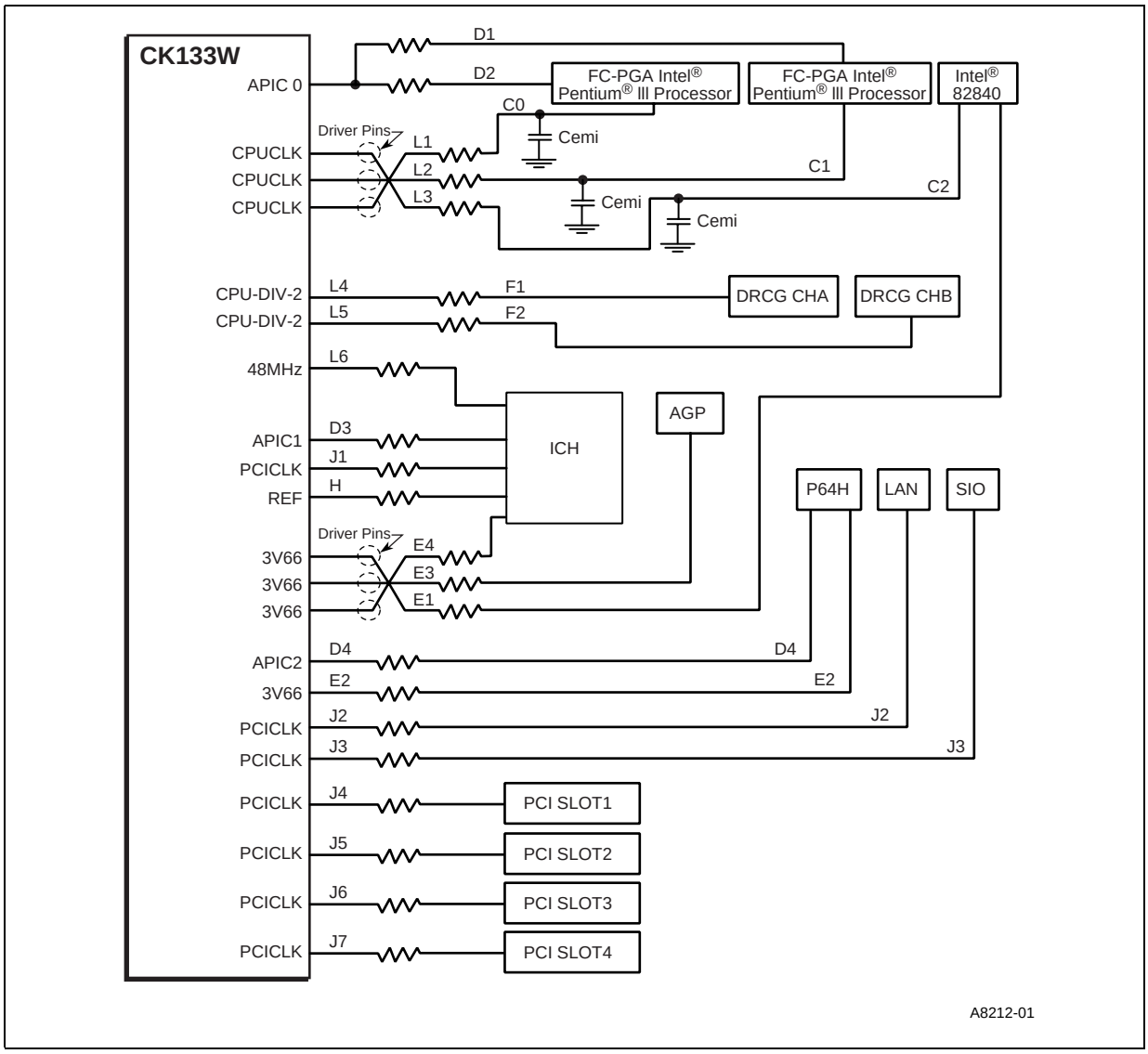
The CK133W is a mixed voltage component. Some of the output clocks are 3.3 V and some of the output clocks are 2.5 V. As a result, the CK133W device requires both 3.3 V and 2.5 V. These power supplies should be as “clean” as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines.

The MCH uses the same clock for hub interfaces and AGP. It is important that the hub interface/AGP clocks are routed to ensure that the skew requirements are met between the following:

- Intel 82820 Memory Controller Hub (MCH) interface/AGP clock and the AGP connector (or device).
- Intel 82820 Memory Controller Hub (MCH) interface/AGP clock, Intel 82810AA (I/O Controller Hub-ICH) interface clock, and the Accelerated Hub Architecture Interface Controller-P64H interface clock.

17.1.1 FC-PGA Intel® Pentium® III Processor

Figure 17-1. CK133W Clock Diagram



NOTES:
1. The processor EMTS defines the AC timing specifications for the skew rate of BCLKs. The recommended source series resistor termination is 33 Ω and the shunt capacitor is 10 pF. The shunt capacitor implementation is optional for EMI control.
2. As shown in Section 17.3, other implementations can be investigated, such as series termination at the clock driver and AC termination at each receiver pin of the high speed clocks, (e.g., the host clocks, the 3V66 clocks, and the 48 MHz clocks). This implementation tends to decrease the amount of jitter seen by the receiver.

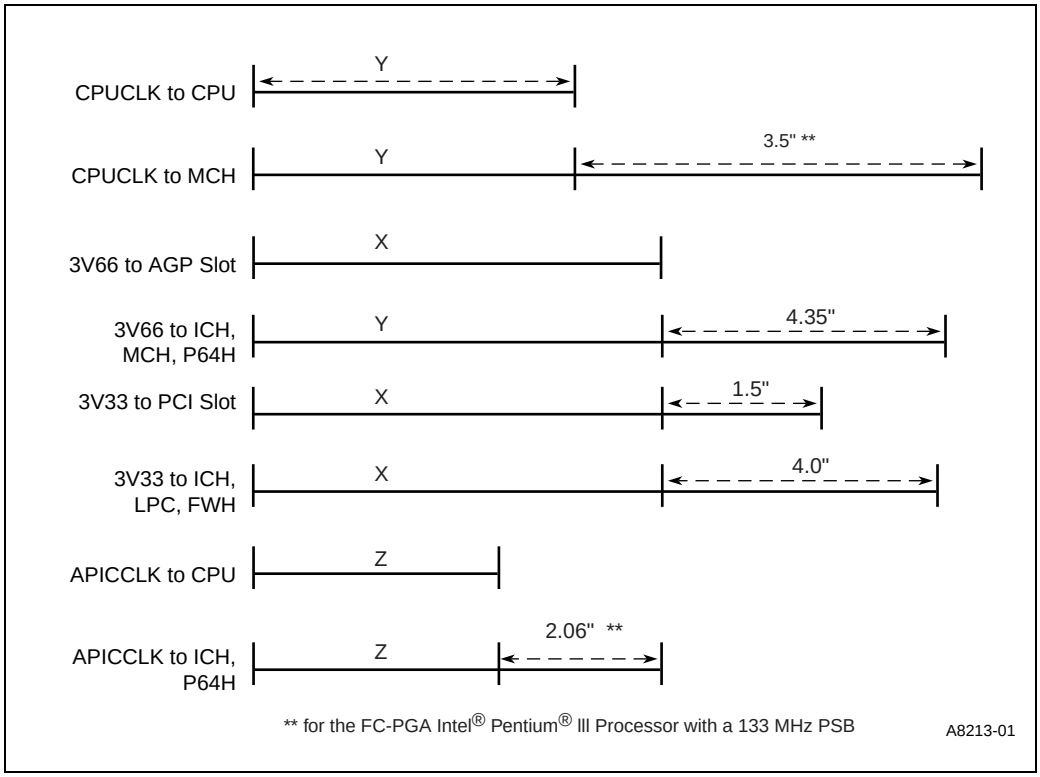
17.1.2 CK133W - FC-PGA Intel Pentium III Processor and Intel 840 Chipset Clock Skew

Table 17-2. Intel® 840 Chipset Clock Skew

Clock Symbol	Relationship	Skew			Notes
		Pin-Pin (ps)	Base Board (ps)	Total (ps)	
		Typical	Typical	Typical	
C0 - C1	FC-PGA CPUCLK **leads** FC-PGA CPUCLK	0	150	150	1, 2, 3
C0 - C1	FC-PGA CPUCLK **lags** FC-PGA CPUCLK	0	-150	-150	1, 2, 3
(C0, C1) - C2	FC-PGA CPUCLK **leads** MCH CPUCLK	0	150	150	3, 4
(C0, C1) - C2	FC-PGA CPUCLK **lags** MCH CPUCLK	0	-150	-150	3, 4
D1 - D2	CPU PICCLK **leads** CPU PICCLK	250	125	375	
D1 - D2	CPU PICCLK **lags** CPU PICCLK	-250	-125	-375	
(D1, D2) – (D3, D4)	CPU PICCLK **leads** ICH APICCLK and P64H APICCLK	250	125	375	
(D1, D2) – (D3, D4)	CPU PICCLK **lags** ICH APICCLK and P64H APICCLK	-250	-125	-375	
E1 – E3	MCH CLK66 **leads** AGP device AGPCLK	250	125	375	5, 6, 6
E1 – E3	MCH CLK66 **lags** AGP device AGPCLK	-250	-125	-375	5, 6, 6
E1 - (E3, E4)	MCH CLK66 **leads** ICH CLK66 and P64H CLK66	250	125	375	6
E1 - (E3, E4)	MCH CLK66 **lags** ICH CLK66 and P64H CLK66	-250	-125	-375	6
E4 – J1	ICH CLK66 **to** ICH PCICLK	1500-3500	±500	1000-4000	6, 7
J1, J2, J3, J4, J5, J6	PCICLK **leads** PCICLK	500	1500	2000	7
J1, J2, J3, J4, J5, J6	PCICLK **lags** PCICLK	-500	-1500	-2000	7

NOTES:
1. Two-way processor configuration only.
2. Clock driver output pins tied together to reduce pin-to-pin skew.
3. An additional ±40 ps have been added to the skew to support Spread Spectrum Clocking.
4. See “BCLK Skew Between CPU and Chipset” on page 17-4 for details.
5. Additional board skew of 332.5 ps (332.5 ps = 2.06” @ 161 ps/in) must be added to the ICH APICCLK to compensate for the propagation delay to the Pentium III FC-PGA processor. The ±250 ps board skew shown does not reflect this addition.
6. An additional ±60 ps have been added to the skew to support Spread Spectrum Clocking.
7. Additional board skew (700 ps = 4.35” @ 175 ps/inch) must be added to MCH CLK66, ICH CLK66, and P64H CLK66 if an AGP connector/card is used. This is stated in the AGP Specification. The ±125 ps board skew shown does not reflect this addition.
8. ICH CLK66 must lead ICH PCICLK.
9. Additional board skew must be added to ICH PCICLK if a PCI connector/card is used. This is stated in the PCI Specification. The ±1500 ps board skew shown does not reflect this addition.

Figure 17-2. CK133W Intel® Pentium® III Processor/Intel® 840 Chipset Guidelines



NOTES:
1. There is no relationship between lengths X, Y, and Z.
2. All lengths shown are based on calculations using a board velocity (microstrip) of 1.93 ns/ft.

17.1.3 BCLK Skew Between CPU and Chipset

In order to best center the timing margins, it is recommended that the BCLK timing at the chipset lag behind the CPU by 260 ps. In practice, this skew has been generated by making the BCLK trace length to the chipset 3.5 inches longer than BCLK trace(s) to the CPU. While this length delta would typically indicate a longer skew time, post-layout extractions and simulation of the BCLK traces have verified this recommendation.

It is highly recommended that the designer perform extractions and simulations of the BCLK signal to assure that timing requirements are met.

17.1.4 Processor Platform CPU Clocks Ganging Solution

Processor platform CPU clocks ganging solution is an optional implementation. This implementation requires shorting the CPUCLK signals together to improve the output-to-output skew. It is important that the signal quality of the receiver clock meet the specified edge rate, jitter, skew and monotonicity under all loading conditions. Note all clock tables and length recommendation contained in this document assume clock outputs are ganged and meet the

specification. All lengths from clock driver to the series and parallel termination resistors must comply with Equation 17-1 on page 17-6. Also the lengths between the driver and the all receivers must comply with Table 17-3 below, which is a sample calculation based on Equation 17-1.

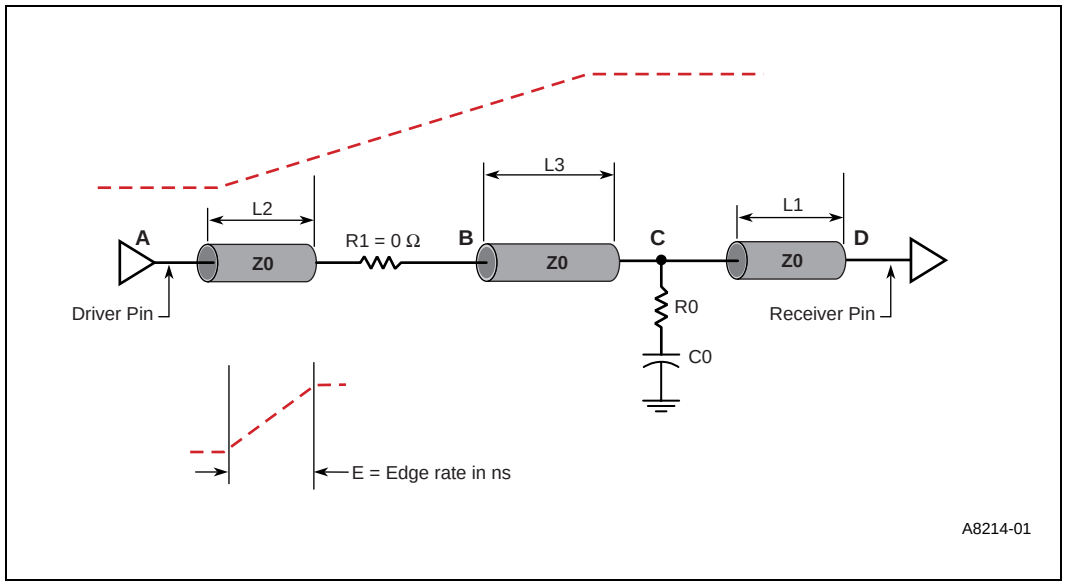
17.2 Series Termination Resistor for CK133W Clock Outputs

All outputs require series termination resistors. The recommended resistor values are defined by simulation. The stub length to the CK133W of these resistors can be compromised to make room for decoupling caps. The rule is to keep all resistor stubs close to the CK133W pins in accordance with the length specify by Equation 17-1. If routing rules allow, Rpacks can be used assuming power dissipation is not exceeded for the Rpack.

17.3 Topology Under Investigation – Source Series Termination with Receiver AC Termination

In addition to the 0-Ω series termination on all CPUCLKs, all CPU-clock signals, the MCH-host, the CPU_DIV2 (to DRCG), and the 48 MHz clock to ICH must have a parallel termination and a capacitor decoupling at the destination, as shown in Figure 17-3. The combination of the parallel termination and the decoupling capacitor must be placed close to the receiver using Equation 17-1.

Figure 17-3. Transmission Line Termination



Equation 17-1.

$$L1 = L2 = \frac{1}{6} \cdot \frac{E}{0.085 \cdot \sqrt{\varepsilon_r}}$$

L1 = L2 = Distance between driver and receiver pin to the termination resistors (in inches)
E = Edge rate of the clock signal; board impedance and process dependent (in ps)
1/6 of the signal rise time and fall time for the driver and the receiver
Constant 0.085 is the signal speed in ns per inch
ε_r is the dielectric of the board, which is board material dependent
R1 = 0 Ω
R0 = 75 Ω
C0 = 0.1 µF

Because of the presence of passive components between length A to B and length C to D, the termination resistor R1 and R0 must be placed at L2 and L1, respectively. This model yields an accuracy of about ±2% provided the line delay is about 1/6 of the signal rise-time/fall-time for both receiver and driver. Table 17-3 provides an example calculation for FR-4, where dielectric (ε_r) is 4.5, using the CPU /PSB bus edge rate (E) of 350 ps.

Table 17-3. Sample Trace Length Calculation

L1	L2	From	To	Min Trace Length Driver to Receiver (inches) Including L1+l2+L3	Max Trace Length Driver to Receiver (inches) Including L1+l2+L3
0.33”	0.33”	CK133W Series Resistor (R1)	CPU Parallel Resistor (R0)	3” +0.33+3.33 =3.66”	6” +.33” +.33” = 6.66
0.33”	0.33”	CK133W Series Resistor (R1)	MCH Parallel Resistor (R0)	3” +0.33+3.33 =3.66”	6” +.33” +.33” = 6.66

NOTE: These guidelines assume 60 Ω board impedance and 33 Ω series resistor for all clock outputs, but 0 Ω series termination for all CPUCLKs.

17.4 Unused CK133W Clock Outputs

All unused clock outputs shall be tied to ground through a series resistor that approximates the impedance of the output buffer as shown in Table 17-4. The intent of these resistors is to terminate the unused outputs to eliminate EMI radiation.

Table 17-4. Unused Clock Output Connection Guidelines

Buffer Name	V_{CC} Range (V)	Impedance (Ω)	If Unused Output Termination to V_{SS} (Ω)
CPU, CPU_DIV2, IOAPIC	2.375 - 2.625	13.5 - 45	30
48 MHz, REF	3.135 - 3.465	20 - 60	40
PCI, 3V33, 3V66	3.135 - 3.465	12 - 55	33

17.5 DRCG

The DRCG reference clock operates at one-half the CPU clock frequency. It is an input into the DRCG and is used to generate the Direct RDRAM “Clock to Master” differential pair (CTM, CTM#). The DRCG generates one pair of differential Direct RDRAM Clocks (CTM, CTM#) from the DRCG reference clock generated by the CK133W. In addition, the DRCG uses phase information provided by the Intel 82840 Memory Controller Hub (MCH) to phase align the Direct RDRAM clock with the CPU clocks.

This phase alignment information is sent to the DRCG SYNCLKN and PCLKM pins from the Intel 82840 Memory Controller Hub (MCH) RCLK and HCLK.

17.6 Component Placement and Layout Requirements

Figure 17-4 shows the conceptual overview of layout requirements among components. The following sections provide detailed explanations of layout requirements for each interconnection:

- Crystal to CK133W
- CK133W to DRCG
- Intel 82840 Memory Controller Hub (MCH) to DRCG
- DRCG to RDRAM channel

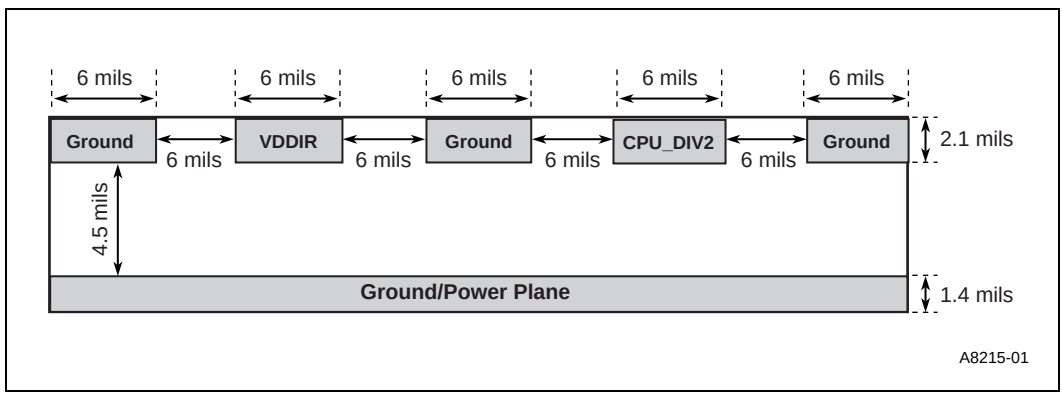
17.6.1 14.318 MHz Crystal to CK133W

The distance between the crystal and the CK133 should be minimized. The maximum trace length is 500 mils.

17.6.2 CK133W to DRCG

VDDIR and CPU_DIV2 must be routed as shown in Figure 17-4. Note that the VDDIR pin can be connected directly to 2.5 V near the DRCG if the 2.5 V plane extends near the DRCG. However, if a 2.5 V trace must be run as a trace, it should originate at the CK133W and routed as shown in Figure 17-4.

Figure 17-4. VDDIR and CPU_DIV2 Routing

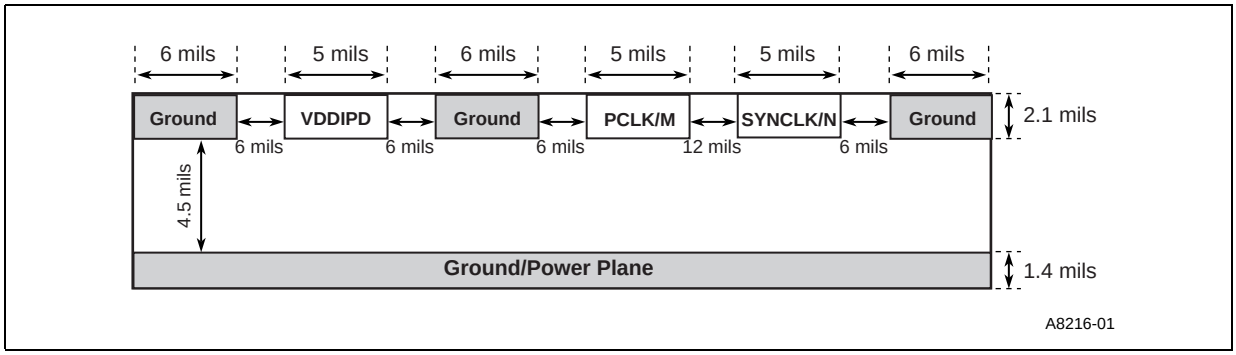


17.6.3 Intel® 82840-MCH to DRCG

The PCLKM, SYNCLKN and VDDIPD should be routed as shown in Figure 17-5. Note that VDDIPD can be connected directly to 1.8 V near the DRCG if the 1.8 V plane extends near the DRCG. However, if a 1.8 V trace must be run, it should originate at the Intel 82840 memory controller hub (MCH) and be routed as shown. If the VDDIPD pin is connected to the 1.8 V plane using a via (i.e., a trace is not run from the CK133W/WS), PCLK/M, and SYNCLK/N (HCLKOUT and RCLKOUT) it must still be routed differentially and ground isolated.

The maximum length for PCLK/M and SYNCLK/N is 6". Additionally, PCLK/M and SYNCLK/N must be length matched within 50 mils. These signals should be routed on the same layer. If the signals must switch layers, then *both* signals should change layers together.

Figure 17-5. MCH to DRCG Routing Diagram



17.6.4 DRCG to RDRAM Channels

The RDRAM clock signals (CTM/CTM# and CFM/CFM#) are high-speed, impedance matched transmission lines. The RDRAM clocks begin at the end of the RDRAM channel and propagate to the controller as CTM/CTM#, where they loop back as CFM/CFM# to the RDRAM devices and terminate at the end of the channel. See Figure 17-6.

The CTM/CTM# signals must be ground referenced (with continuous ground island/plane) from the DRCG to the second RIMM. Table 17-5 provides RDRAM clock routing guidelines.

Figure 17-6. RDRAM Clock Routing Dimension

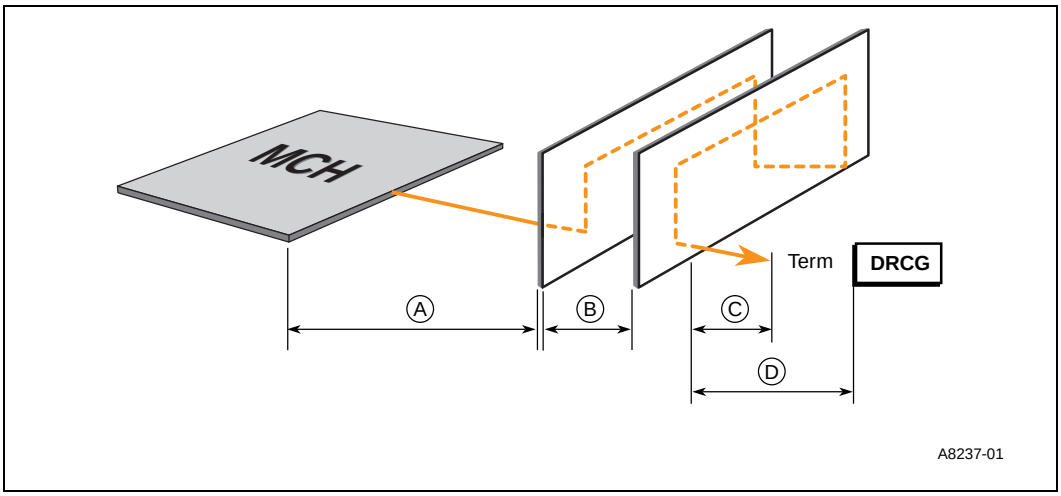


Table 17-5. RDRAM* Clock Routing Guidelines

RDRAM* Clock Routing Length Guidelines				
Clock	**From**	**To**	**Length (inches)**	**Figure 17-6 Trace**
CTM/CTM#	DRCG	Second RIMM Connector	0.0 - 6.0	D
	RIMM	RIMM	0.4 – 0.45	B
	First RIMM Connector	Chipset	0.0 – 6.0	A
CFM/CFM#	Chipset	First RIMM Connector	0.0 – 6.0	A
	RIMM	RIMM	0.4 – 0.45	B
	Second RIMM Connector	Termination	0.0 – 3.0	C

In line section A, C and D, the clock signals should be routed differentially. The clock signals in section B should be routed non-differentially.

For trace section A and D, the clock signals (CTM/CTM# and CFM/CFM#) must be 14 mils wide and routed as shown in Figure 17-6. For all section B and C, the clock signals must be routed with 18 mil-wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via per every 1”. A 6 mil gap is required between the clock signals and the ground isolation traces. In section A, 0.021” of CLK per 1” of RSL trace length must be added to compensate for the clock’s faster trace velocity on the outer layer. CTM/CTM# and CFM/CFM# must be matched within ±2 mils in line section A and B using the trace length matching method. In section C, CFM/CFM# must be length matched within ±2 mils. In section D, the CTM/CTM# must be length matched within ±2 mils.

17.6.5 Trace Lengths

For section A, CTM/CTM# and CFM/CFM# must be length matched within ±2 mils (although exact length matching is ideal). Package trace compensation, via compensation and RSL signal layer alteration must also be considered. Additionally, 0.021” of CLK per 1” of RSL trace length must be added to compensate for the clock’s faster trace velocity on the outer layer.

For trace section B, the clock signals must be routed with 16 mil-wide traces. There must be a 10 mil ground isolation trace routed around the clock differential pair signals. The clock signals must be matched within ±2 mil to the RSL trace length. Exact matching is preferred.

For trace section C, the clock signals must be routed with 16 mil wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. A 6 mil gap is required between the clock signals and the ground isolation traces. CFM/CFM# must be matched within ±2 mils. Exact matching is preferred.

For trace section D, the clock signals must be routed with 16 mil wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. A 6 mil gap is required between the clock signals and the ground isolation traces. CTM/CTM# must be matched within ±2 mils. Exact matching is preferred.

Figure 17-7. Board Stack-up: RSL Signals

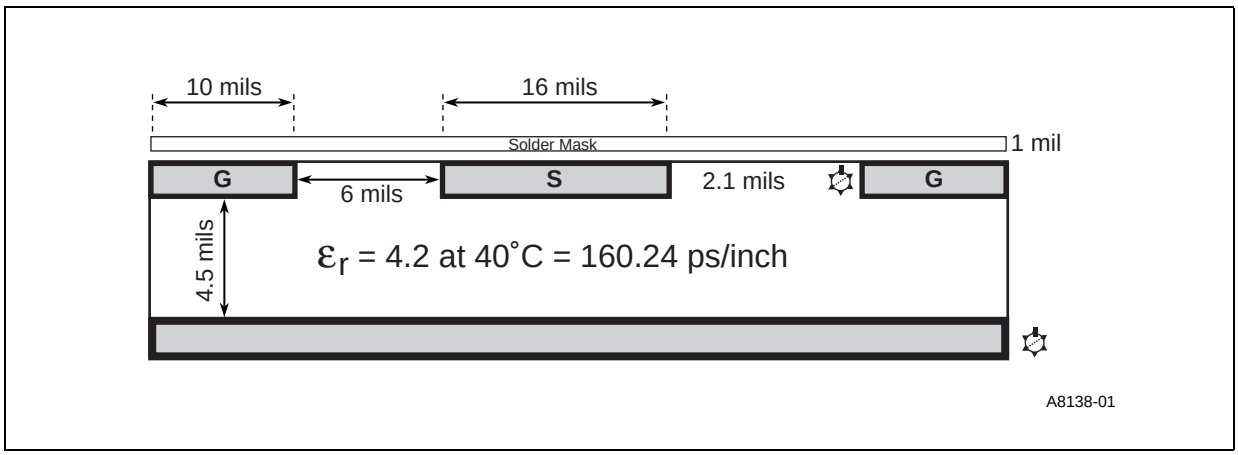
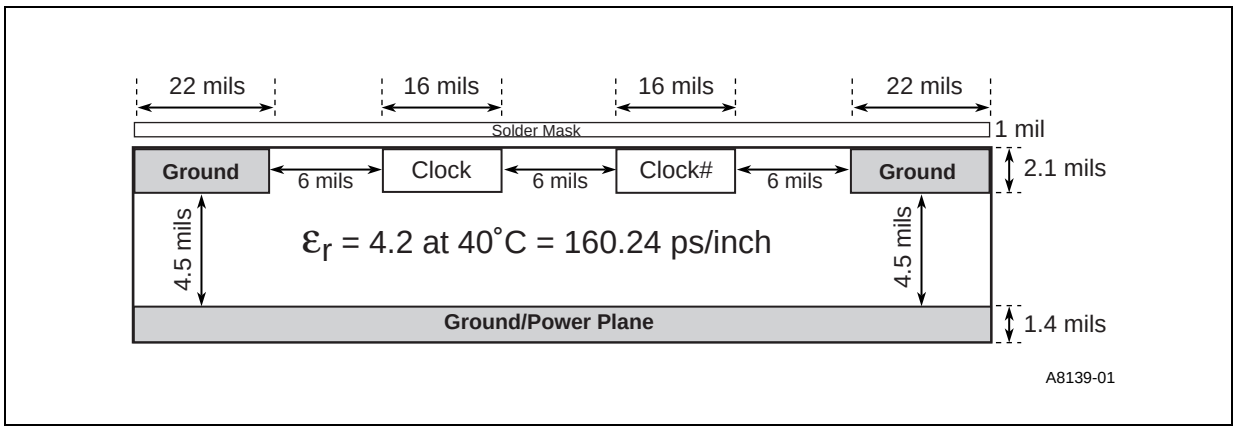
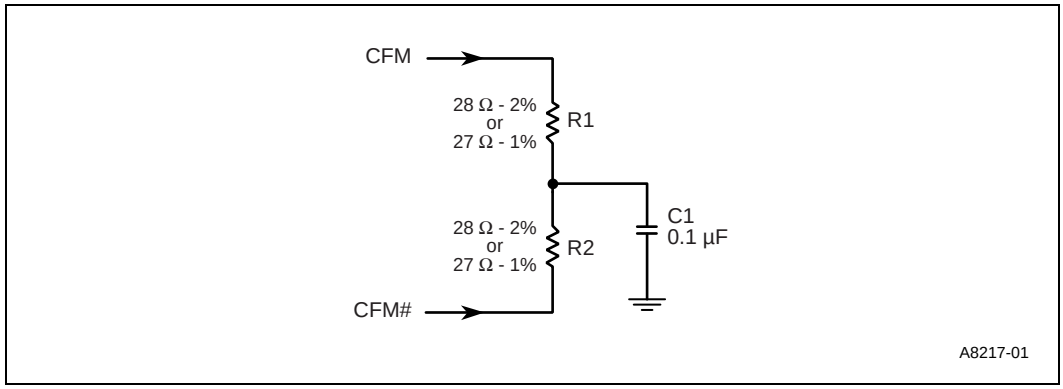


Figure 17-8. Board Stack-up: Differential CLK Signals



The CFM/CFM# differential pair signals require termination using either 1% or 2% 28 Ω resistors and a 0.1 µF capacitor as shown in Figure 17-9:

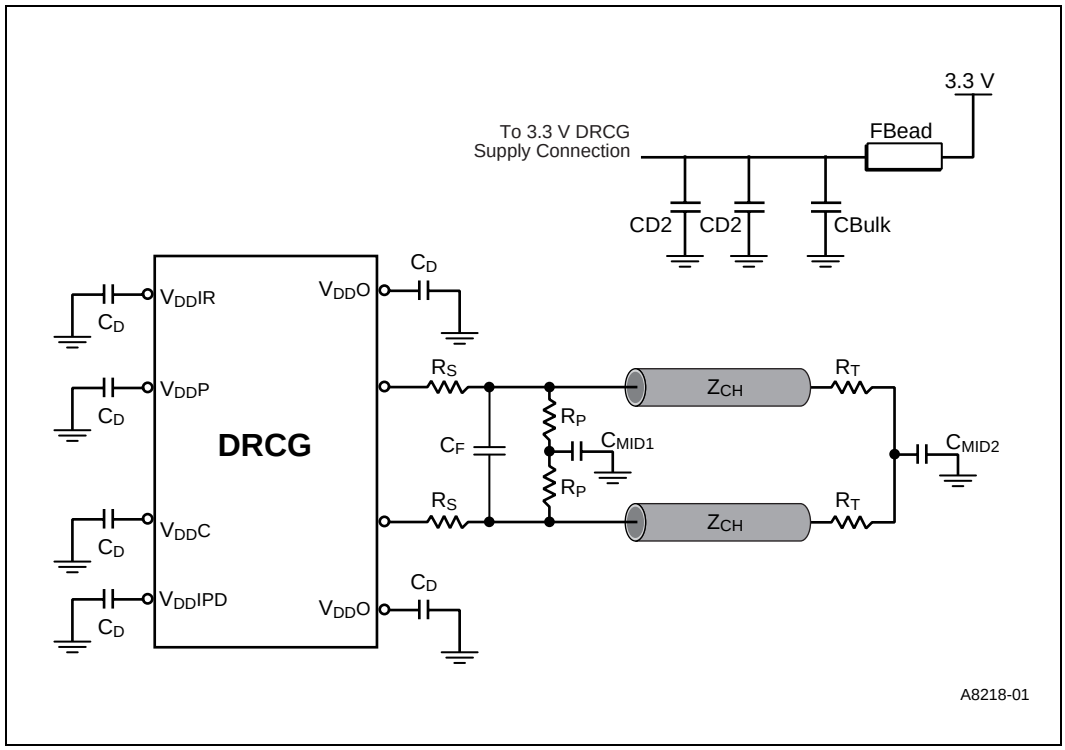
Figure 17-9. CFM/CFM# Termination



17.6.6 DRCG Impedance Matching Circuit

The external DRCG impedance matching circuit is shown in Figure 17-10.

Figure 17-10. DRCG Impedance Matching Network



Component	Nominal Value	Notes
C_D	0.1 µF	Decoupling caps to GND
R_S	39 Ω	Series termination resistor
R_P	91 Ω	Parallel termination resistor
C_{MID1}, C_{MID2}	0.1 µF	Virtual GND caps
R_T	27 Ω	End of channel termination
C_F	4-15 pF	Do Not Stuff, leave pads for future use
FBead	50 Ω @ 100 MHz	Ferrite bead
CD2	0.1 µF	Additional 3.3 V decoupling caps
CBulk	10 µF	Bulk cap on device side of ferrite bead

Details:

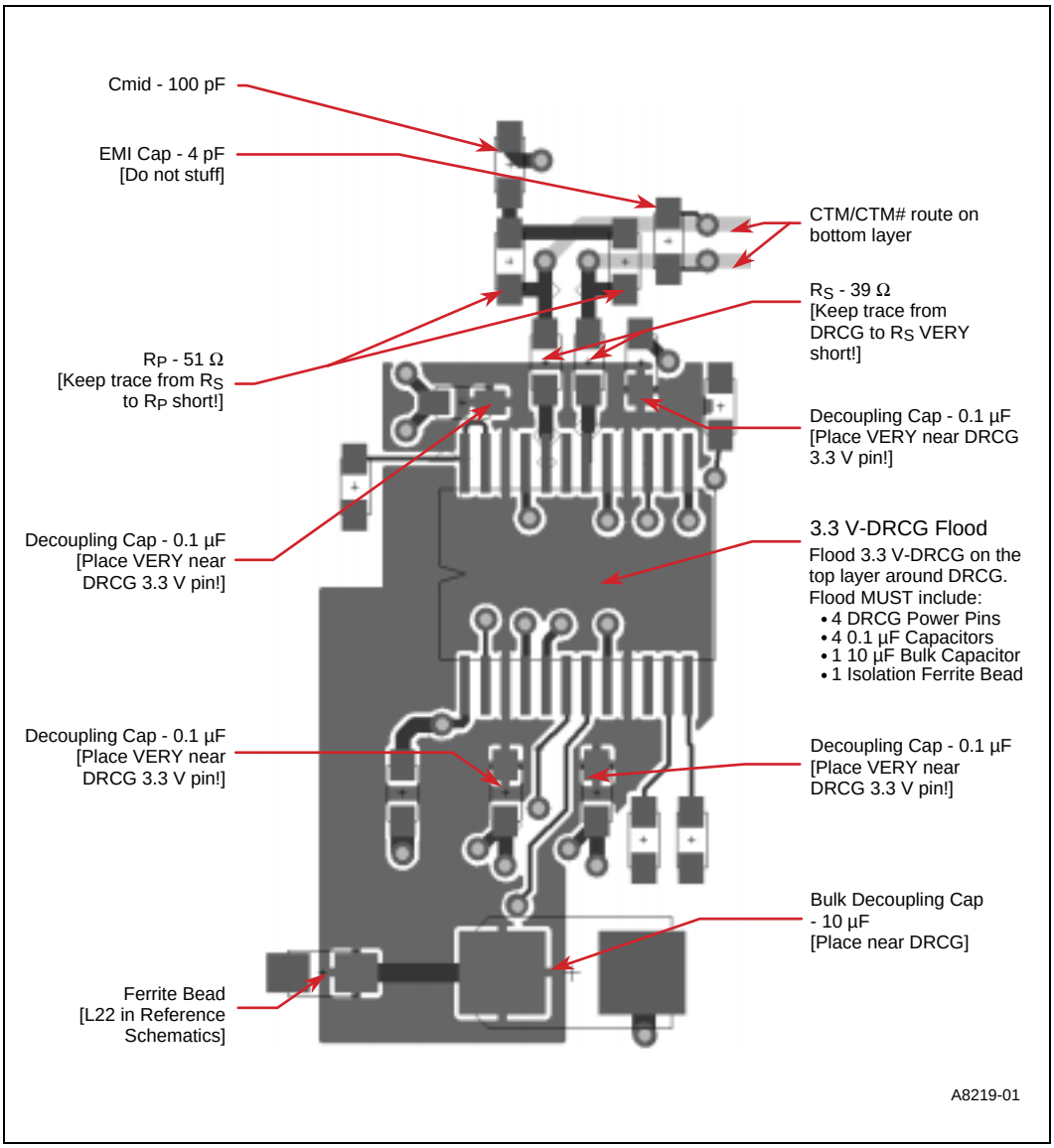
1. Note the removal of the original EMI capacitors between the junctions of R_S, R_P and ground. These capacitors had minimal impact on EMI and increased DRCG output jitter by approximately 2X.
2. The intent of component C_F is to decouple CLK and CLKB outputs to each other, but early data shows this actually increases device jitter. C_F should not be stuffed at this time.
3. The ferrite bead and 10 µF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system. The additional 3.3 V capacitors (CD2) have a minor positive impact, but the ideal values have not been extensively optimized. There is a possibility that one or both CD2 caps can be removed in future board revisions.
4. µF capacitors are better than 0.01 µF or 0.001 µF caps for DRCG decoupling. Most decoupling experiments that replaced 0.1 µF caps with higher frequency caps ended up with the same or worse jitter. Replacing existing 0.1 µF caps with higher frequency caps is not advised.
5. C_{mid} at 0.1 µF has improved jitter versus C_{mid} at 100 pF. However, this will increase the latency coming out of a stop clock or three-state mode.
6. R_S, R_P, R_T were modified to improve channel signal integrity through increasing CTM/CTMN swing.

The circuit shown is required to match the impedance of the DRCG to the 28 Ω channel impedance. More detailed information can be found in the *Direct RDRAM* Clock Generator Specification.*

The previously recommended 15 pF capacitors on CTM/CTM# should be removed. The 4 pF capacitor shown in Figure 17-11 should not be assembled (“no-stuff”).

17.6.7 DRCG Layout Example

Figure 17-11. DRCG Layout Example



17.6.8 Decoupling Recommendation for CK133W and DRCG

Some CK133W vendors may integrate the XTAL_IN and XTAL_OUT frequency adjust capacitors. However, pads should be placed on the board for these external capacitors for testing/debug. To further reduce jitter and voltage supply noise, the addition of a ferrite filter with two caps (10 µF and 0.1 µF) on both the 2.5 V and 3.3 V planes close to the CK133W clock devices is recommended.

17.7 DRCG Frequency Selection and DRCG+

17.7.1 DRCG Frequency Selection Table

To provide further flexibility, Intel has enabled a variation of the DRCG labeled *DRCG+*. The device has the same pin out and form-factor as the existing DRCG device document at:

http://www.rambus.com

The DRCG+ Mult[1:0] select table has changed to modify two of the multiplier ratios, as shown in Table 17-6. An additional 9/2 multiplier allows 133/300 MHz. Please note that the 133/356 ratio is not support by the Intel 840 chipset. Support for the 300 and 400 MHz memory bus remains unchanged.

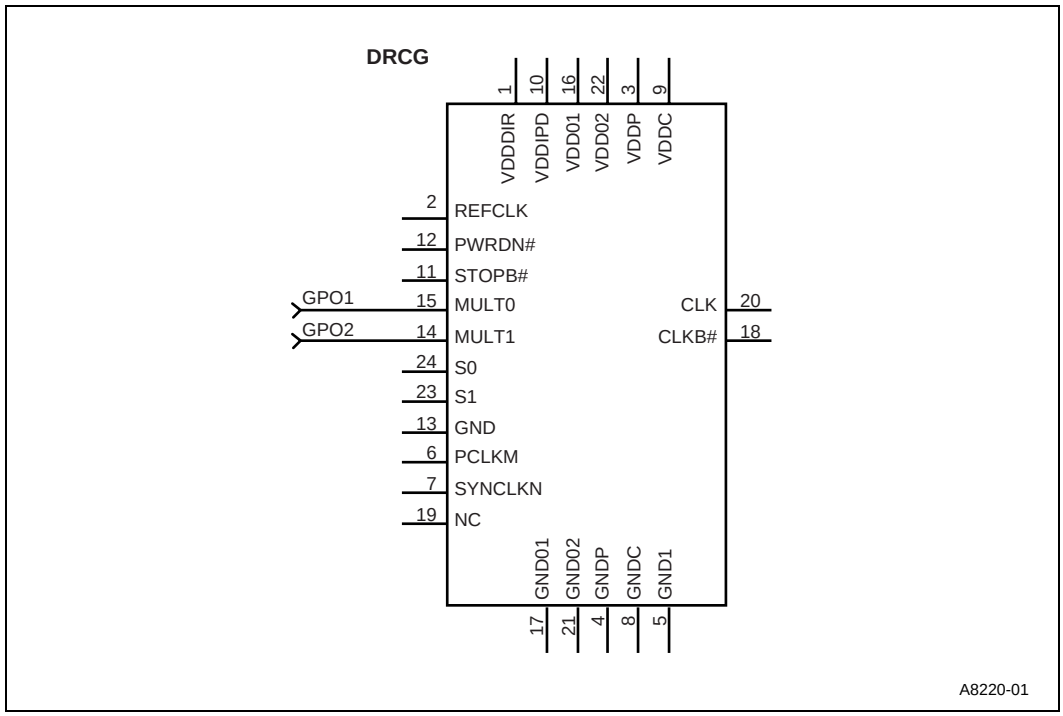
Table 17-6. DRGC+ vs DRGC Multiplier Ratios

Mult[1:0]	DRCG	DRCG+
0:0	4:1	9:2
0:1	6:1	6:1
1:0	8:3	16:3
1:1	8:1	8:1

17.7.2 DRCG+ Frequency Selection Schematic

DRCG+ frequency can be selected by connecting two GPIOs to the MULT[1:0] pins, as shown in Figure 17-12. This will allow selection of all frequencies that are supported by the Intel 840 chipset.

Figure 17-12. DRCG+ Frequency Selection



17.8 AGP Clock Routing Guidelines

The AGP clock must be routed with 20 mil spacing to all other signals.

17.8.1 P64H PCI 33 MHz Clock Routing Guidelines

At 33 MHz, the P64H can support 4x33 MHz PCI slots. The P64H can provide six copies of the PCLKOUT to PCI devices on its primary PCI bus. PCLKFBOUT is used as the feedback clock and must be routed into PCLKFBIN of the P64H. The PCLKOUT routing guidelines are shown in Figure 17-13 and Figure 17-14:

Figure 17-13. P64H PCI 33 MHz Clock Routing

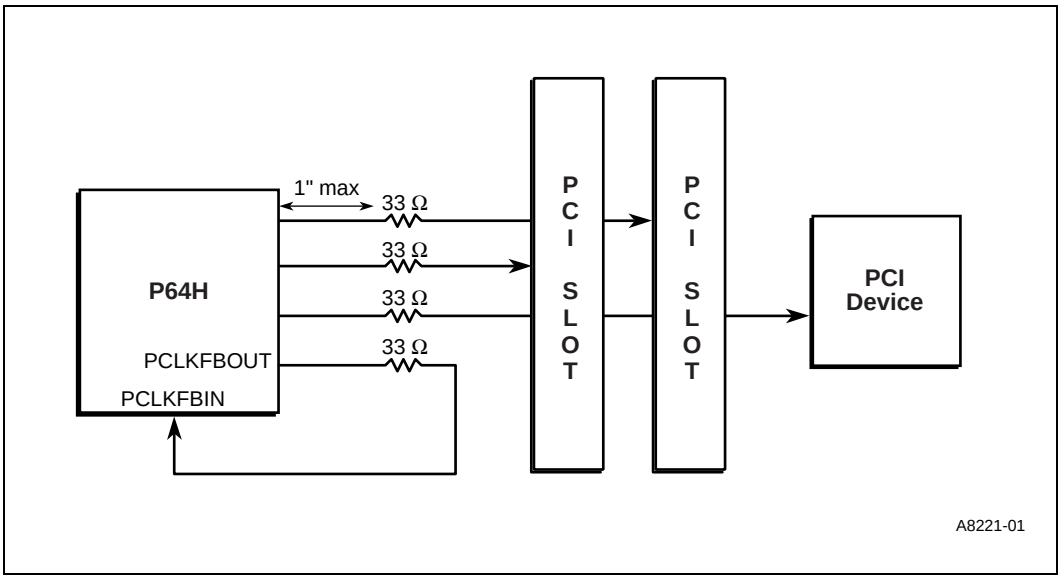


Figure 17-14. P64H PCI 33 MHz Clock Trace

Per the PCI Specification, the PCI CLK signal length from the expansion board edge connector to the PCI device should be 2.5” ± 0.1 inches for 32-bit and 64-bit expansion boards.

17.9 P64H PCI 66 MHz Clock Routing Guidelines

At 66 MHz, the P64H can support 2x66 MHz PCI slots and 1x66 MHz device down. The P64H can provide three copies of the PCLKOUT to PCI devices on its primary PCI bus. PCLKFBOUT is used as the feedback clock and must be routed into PCLKFBIN of the P64H. The PCLKOUT layout guidelines are shown in Figure 17-15 and Figure 17-16:

Figure 17-15. P64H PCI 66 MHz Clock Routing

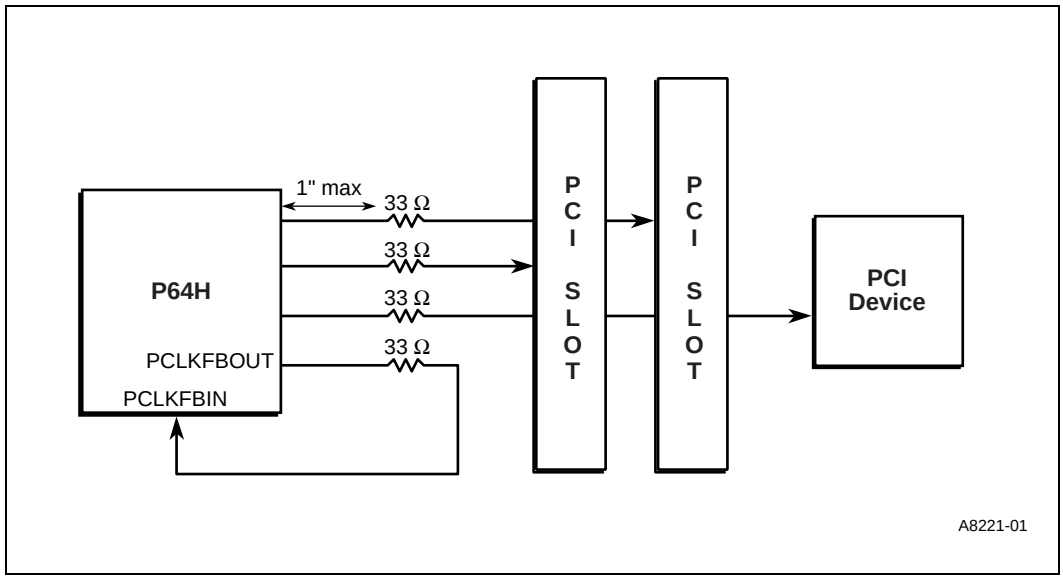
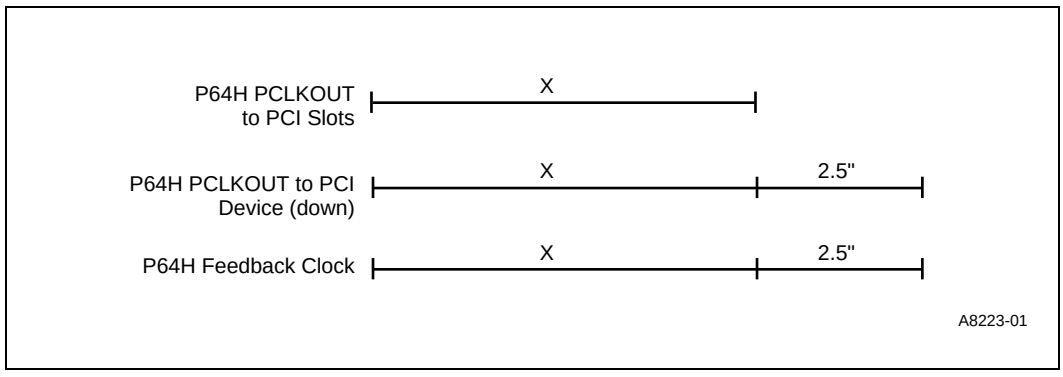


Figure 17-16. P64H PCI 66 MHz Clock Trace



System Design Considerations 18

18.1 Power Delivery

18.1.1 Definitions

Suspend-To-RAM (STR): In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.

Full-power operation: During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (CPU stop grant state) state.

Suspend operation: During suspend operation, power is removed from some components on the motherboard.

Power rails: WTX power supply has six power rails: +5 V, -5 V, +12 V_{DIG} (digital power to CPU VRM 8.4), +12 V, -12 V, +3.3 V, -3.3 V, 3VSB, 5VSB. In addition to these power rails, other power rails can be created with voltage regulators.

Core power rail: A power rail that is only on during full-power operation.

Derived power rail: A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 1.8 V can be derived (on the motherboard) from either the 3.3 V or 5 V using a voltage regulator.

Standby power rail: A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rails that are distributed directly from the WTX power supply are: 3VSB and 5VSB (3 V Standby and 5 V Standby). Other standby rails are created with voltage regulators on the motherboard.

Dual power rail: A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation.

18.1.2 Intel® 840 Chipset Board Power Delivery

Figure 18-1. FC-PGA Intel® Pentium® III Processor and Intel® 840 Chipset RIMMs Power Delivery Architecture

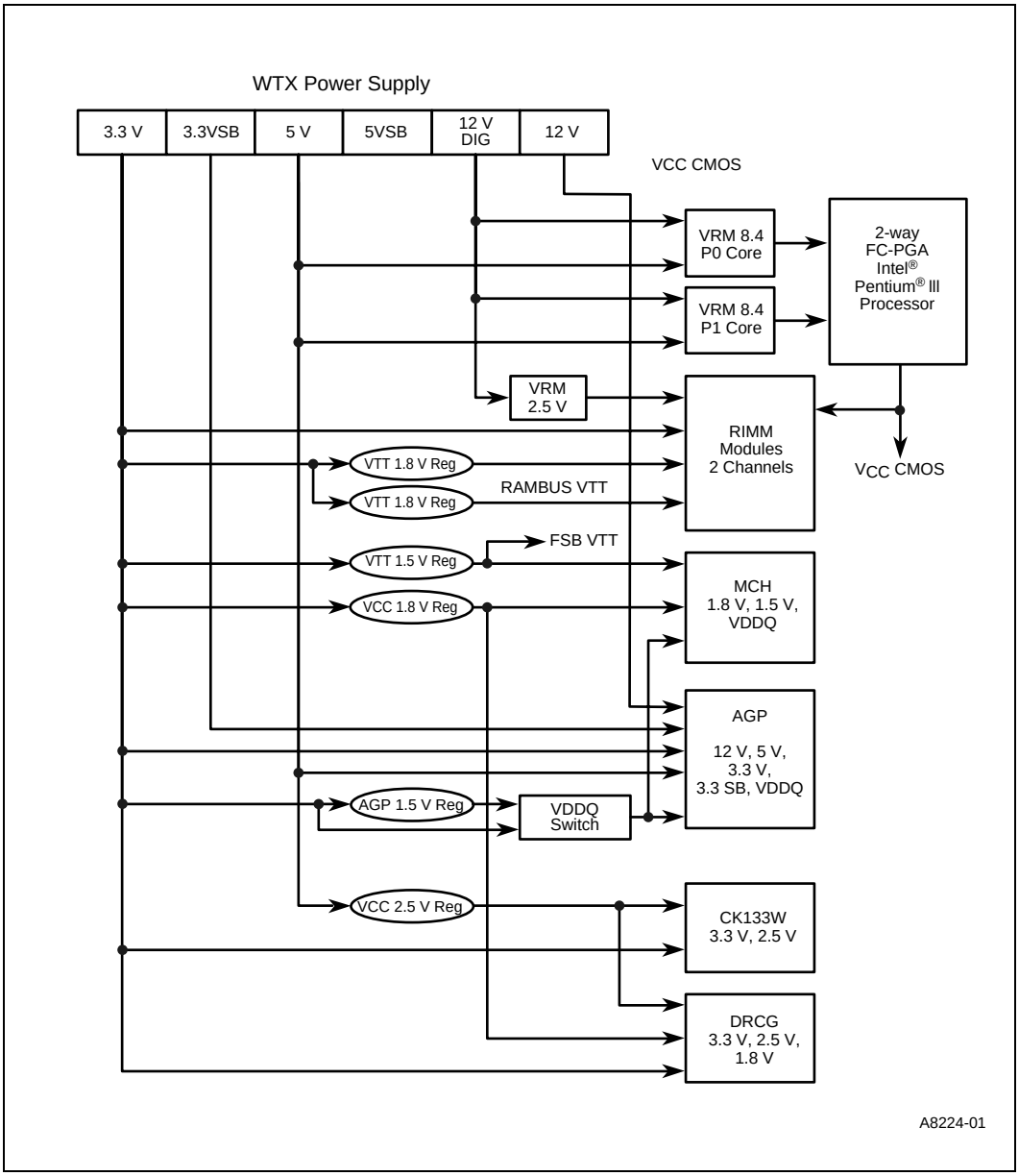


Figure 18-2. FC-PGA Intel® Pentium® III Processors and Intel® 840 Chipset MEC Power Delivery

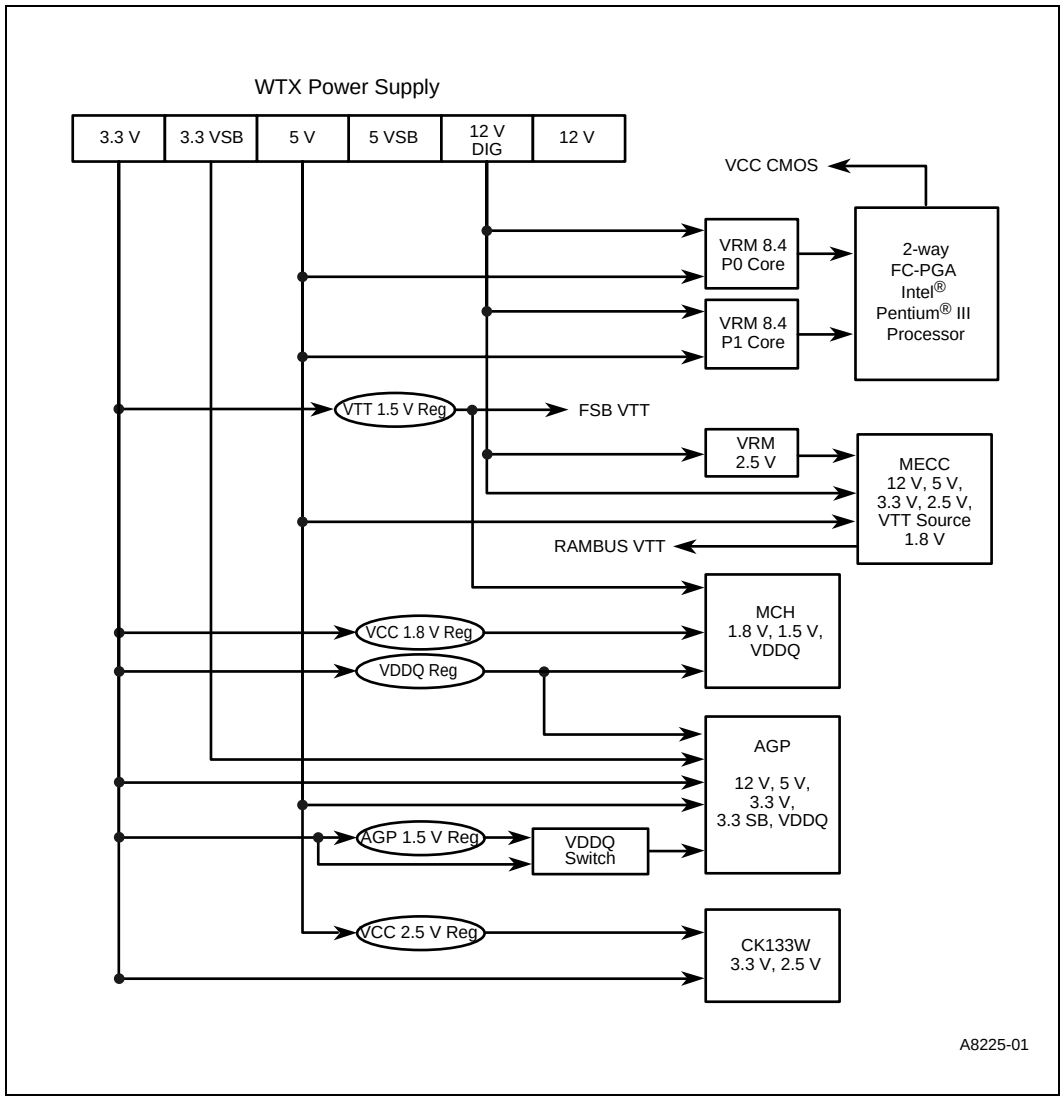
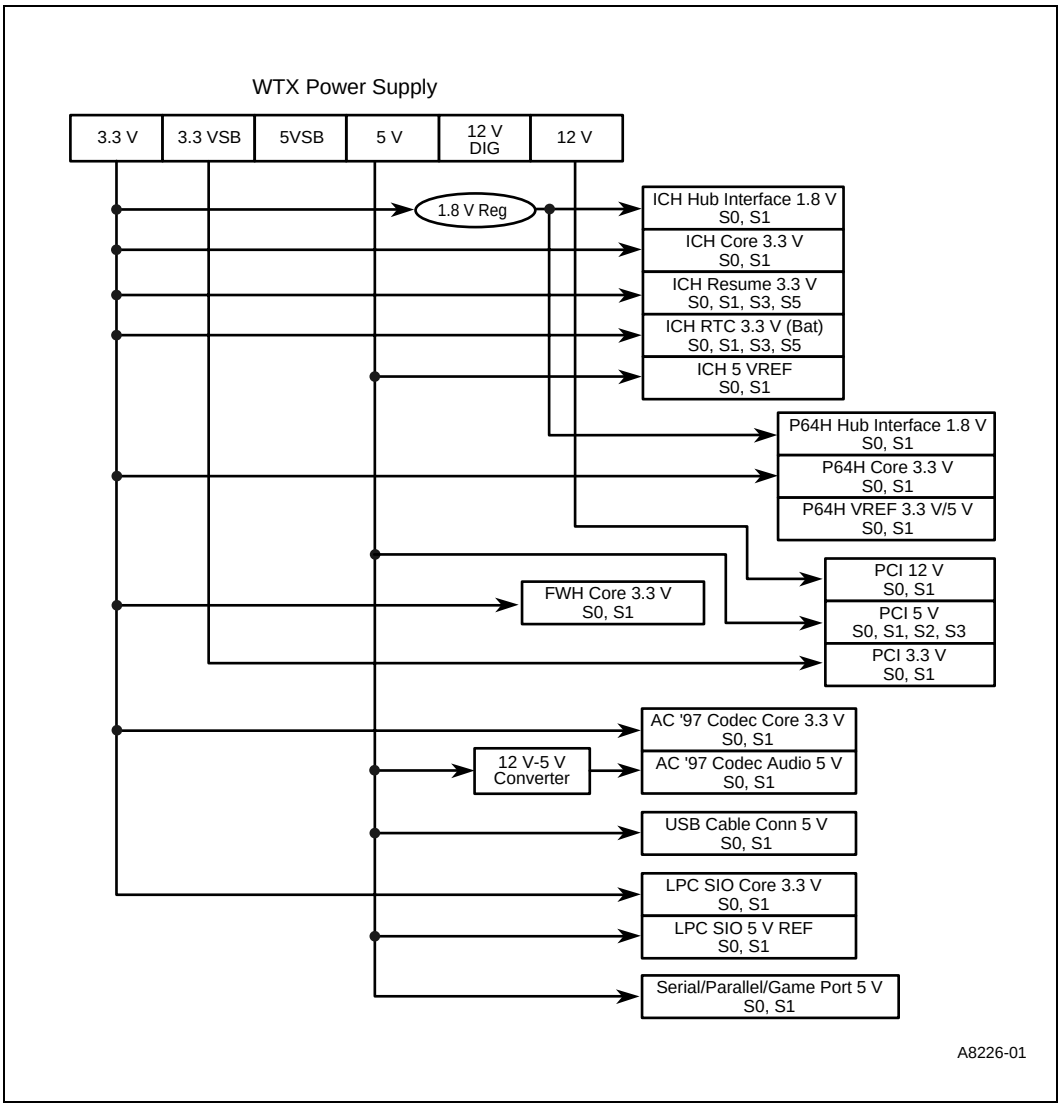


Figure 18-3. Intel® 840 Chipset System I/O Power Delivery



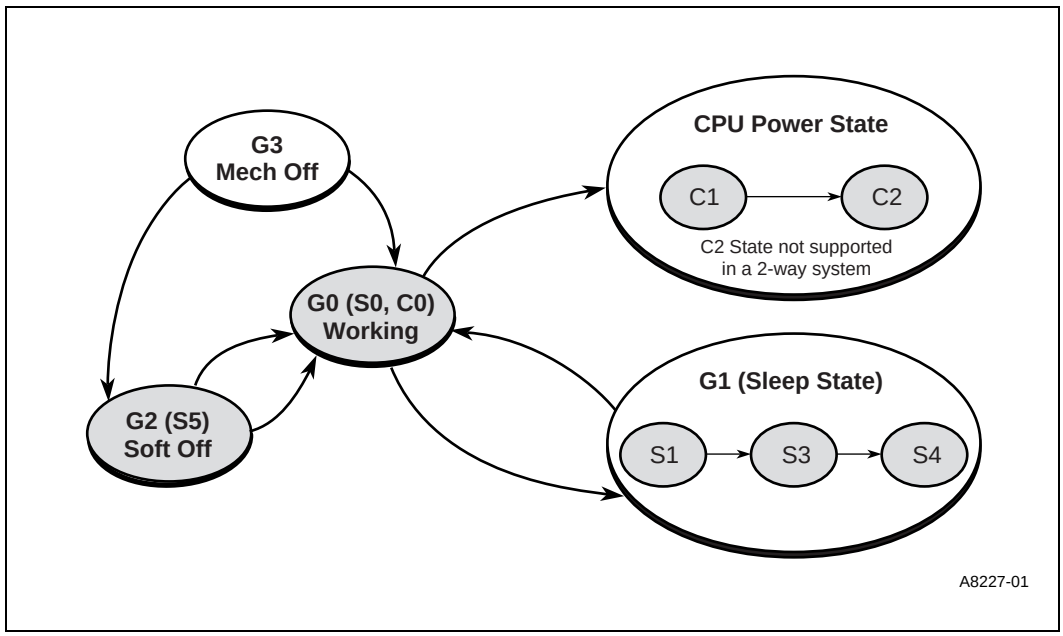
18.2 Power Management

The Intel® 840 chipset-based platform implements the ACPI mechanisms software and hardware that enables the system to minimize system power consumption, manage system thermal limits, and maximize the battery life. This implementation involves trade-offs among system speed, noise.

18.3 ACPI Hardware Model

The Intel 840 chipset-based platform supports both legacy and ACPI operations, which involves sequencing the platform between the various global system states (G0-G3). Figure 18-4 depicts global states and the transitions. For complete detail of the mechanisms involved in transition from any of the global states, refer to *ACPI Interface Specification*, Revision 1.0b, Section 4.5.

Figure 18-4. Global System Power States and Transition



18.4 Thermal Design Power

The thermal design power numbers are an estimation of the maximum expected power generated by a component in a realistic application. It is based on extrapolations in both hardware and software technology over the product life. It does not represent the expected power generated by a power virus. The ICC max sustained worst-case rated amperes (WCRAs) are estimations of the maximum expected current generated within a die section in a realistic application. For example, an application that is doing only extensive memory reads/writes.

The numbers shown in Table 18-1 should be used for power supply design and not thermal design. Refer to the *Intel® 840 Chipset Thermal Application Note* for thermal design details.

Table 18-1. Thermal Design Power

MCH Max Thermal Design Power = 4.2 W			
Parameter	**Operating Voltage**	**I_{CC} Max Sustained Current (mA)**	**Instantaneous Peak Current (A)**
Core	1.8 V	1000	2.0
RAC Core	1.8 V	340	
RSL	1.8 V	730[1]	1.2[5]
Hub Interface	1.8 V	360	
AGP	3.3 V	230	0.370
V_{DDQ} -AGP	1.5 V	200	
P64H Max Thermal Design Power = 2.2 W			
Parameter	**Operating Voltage**	**I_{CC} Max Sustained Current (mA)**	**Instantaneous Peak Current (A)**
Core	3.3 V	560	1.1
PCI I/O	3.3 V	280	
HL I/O	1.8 V	360	0.075
MRH-R Max Thermal Power = 2.2 W			
Parameter	**Operating Voltage**	**I_{CC} Max Sustained Current (mA)**	**Instantaneous Peak Current (A)**
RAC Core	1.8 V	1020	1.3[6]
RSL RAC A	1.8 V	730[3]	
RAC B	1.8 V	730[4]	
RAC C	1.8 V	730[4]	
ICH Max Thermal Power = 1.4 W			
Parameter	**Operating Voltage**	**I_{CC} Max Sustained Current (mA)**	**Instantaneous Peak Current (A)**
Core	3.3 V	300	
PCI I/O	3.3 V	1500	
HL I/O	1.8 V	55	

NOTES:
1. Could be shared between the MCH and RDRAM.
2. Could be shared between MCH and MRH-R.
3. Could be shared between MRH-R and RDRAM.
4. This is consumed by either RIMMs or MCH, and not by both.
5. The 1.8 V RDRAM termination (MCH) is consumed by either RIMMs or MCH, and not by both.

18.5 64/72-Mbit RDRAM Excessive Power Consumption

During initialization of RDRAM devices, all RDRAM devices on the channel responds incorrectly to device directed commands. These commands are the SET_FAST_CLOCK, SET_RESET, and CLEAR_RESET commands. This causes excessive current consumption on the 2.5 V supply. The amount of excessive current depends on the number of devices and frequency used. The worst case current draw is 7.5 A, in a system with 32 devices and a frequency of 400 MHz. This issue will be present in initial production of 64/72-Mbit RDRAM devices; however, 128-Mbit device operation will be corrected. There are two potential options/solutions:

1. Reduce the clock frequency during initialization
2. Increase the current capability of the 2.5 V voltage regulator

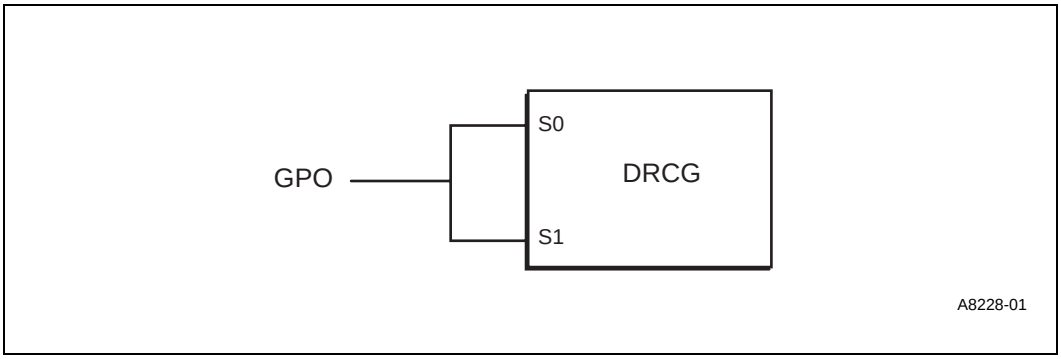
For specific RDRAM impact, please contact the RDRAM vendors.

18.5.1 Option 1: Reduce the Clock Frequency During Initialization

Tie a single core well GPO with a default high state to both the S0 and S1 pins of the DRCG (i.e., tie S0 and S1 together and then connect to a GPO as shown in Figure 18-5.) When the core power supply to the system is turned on, the DRCG will enter a test mode and the output frequency will match the input REFCLK frequency. For details on this DRCG mode, please refer to the latest DRCG specification. By slowing down the DRCG output clock, the power consumption from the 2.5 V power supply will be reduced. After the SetR/ClrR commands have been issued, the BIOS will drive the GPO low to bring the DRCG back to normal operation.

Note that if a default low GPO is used, on power up, all the devices may come up in the standby state at full speed, thus requiring more power.

Figure 18-5. Using a GPO to Reduce DRCG Frequency



This solution requires BIOS modifications. Refer to the *Intel® 840 MCH BIOS Specification* for detailed instructions.

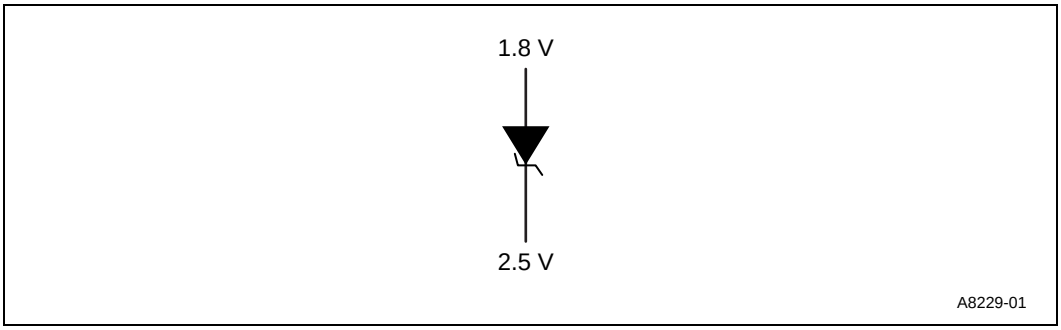
18.5.2 Option 2: Increase the Current Capability of the 2.5 V Voltage Regulator

The second implementation option requires that the 2.5 V power supply be modified to maintain the maximum amount of current required by a fully populated RDRAM channel (~7.5 A).

18.6 V_{TERM}/V_{DD} Power Sequencing Requirement

Power to the RDRAM termination resistors (V_{TERM}) must follow the power to the RDRAM core. A schottky diode can be placed between the 1.8 V and 2.5 V to ensure this power-up sequence, as shown in Figure 18-6.

Figure 18-6. 1.8 V and 2.5 V Power Sequence (Schottky Diode)



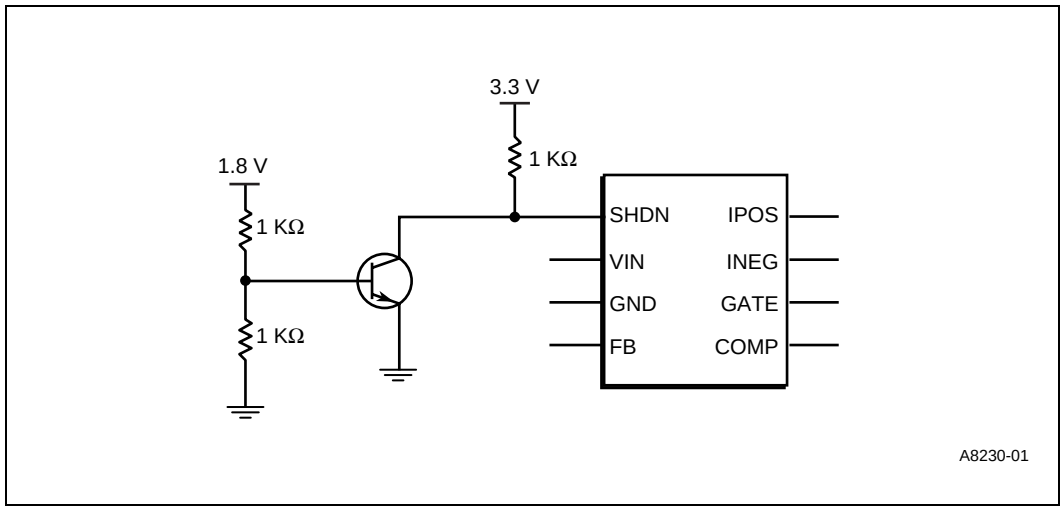
18.7 $V_{DDQ}/V_{CC1.8}$ Power Sequencing

For the consideration of component long term reliability, the following power sequence is strongly recommended while the AGP interface of MCH is running at 3.3 V. If the AGP interface is running at 1.5 V, the following power sequence recommendation is no longer applicable. The power sequence recommendation is:

1. During the power-up sequence, the 1.8 V must ramp up to 1.0 V BEFORE 3.3 V ramps below 2.2 V.
2. During the power-down sequence, the 1.8 V *cannot* ramp below 1.0 V BEFORE 3.3 V ramps below 2.2 V.
3. The same power sequence recommendation also applies to the entrance and exit of S3 state.

System designers must be aware of this requirement while designing the voltage regulators and selecting the power supply. Figure 18-7 provides a power sequencing example.

Figure 18-7. V_{DDQ} Power Sequencing Example



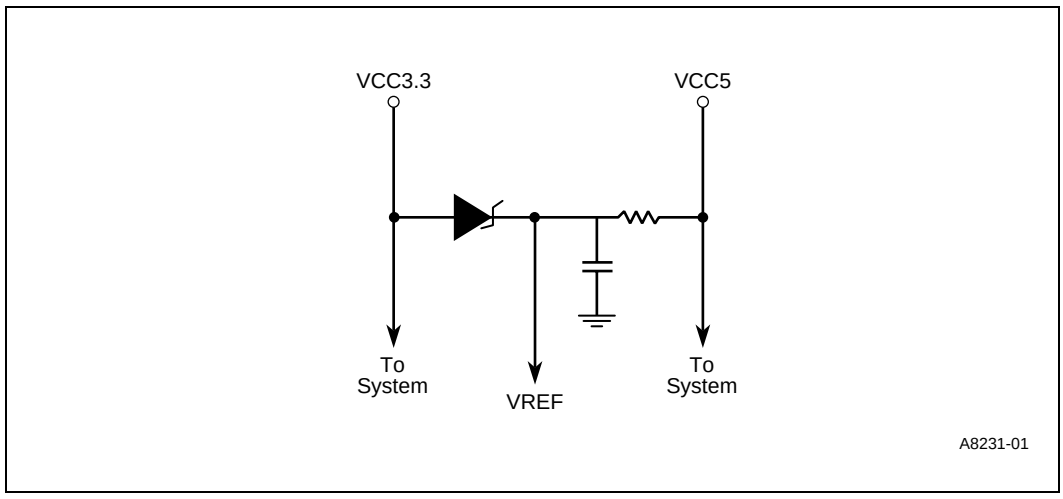
18.8 ICH/P64H $5V_{REF}$ and $V_{CC3.3}$ Sequencing Requirement

$5V_{REF}$ is the reference voltage for 5 V tolerance on inputs to the ICH. $5V_{REF}$ must power up before or simultaneous to 3.3 V_{CC}. It must also power down after or simultaneous to 3.3 V_{CC}.

VCC5REF and PVCC5REF signals are reference voltage for 5 V tolerance on P64H inputs. These signals share the same sequencing requirement as the ICH $5V_{REF}$ signal.

The circuit shown in Figure 18-8 demonstrates one possible method to ensure this power sequence requirement is met.

Figure 18-8. $5V_{REF}$ Sequencing Circuit



Design Considerations/Checklist 19

19.1 General Design Considerations

Pull-up and pull-down values are system-dependent. The appropriate value is determined by AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the high/low voltage specification, the input timing specification (RC rise time), and other factors. Analysis should be done to determine the minimum/maximum values that may be used on the individual signal. Engineering judgment should be used to determine the optimal values. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications.

DC calculation for pull-up value:

- $R_{max} = (V_{CCPU}$ MIN - V_{ih} MIN) / $I_{leakage}$ MAX
- $R_{min} = (V_{CCPU}$ MAX – V_{il} MAX) / I_{ol} MAX

Because $I_{leakage}$ MAX is normally very small, R_{max} may not be meaningful. R_{max} is also determined by the maximum allowable rise time.

19.2 Design Consideration

The following design consideration is intended to be use for Intel® 840 Chipset design reviews.

19.2.1 FC-PGA Intel® Pentium® III Processors

- Pay special attention to the high-speed layout of AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#. These wired-OR signals may be driven simultaneously by more than one agent and may be more susceptible to undershoot/ringback caused by falling edge transitions. Make sure that **only ground planes** are used as reference planes for the entire path of these signals.
- The CPU outputs, at the clock driver, should be shorted together if ganging is supported.
- Use the VRM_PWRGD signal with the CPUPWRGOOD/RESET generation logic to ensure correct timings.
- PRDY# should be connected to the processor and ITP PRDYX# pin through a 240 Ω series resistor. A 50 Ω pull-up to $V_{TT1.5}$ must also be added on the CPU side of the series resistor.
- Pull up or pull down should be implemented in SA[2:0] to set the address bits accordingly.

19.3 82840 Memory Controller Hub (MCH)

19.3.1 System Bus Interface

- System bus frequency and system bus ECC straps require external network for proper enabling. HLA10 is used to determine the system bus frequency. ST0 (AGP) is used to enable ECC.
- BREQ0 is provided by the MCH and must be connected to the processors.
- GTL+ termination is recommended for the CPURST# signal.
- GTLREF[B:A] can be generated with a 75 Ω and 150 Ω resistor divider circuit. The 75 Ω and 150 Ω resistors should be connected to $V_{TT1.5}$ and GND, respectively. There should be one divider circuit for each GTLREF signal. Additionally, GTLREF signals should also be decoupled to GND with a 0.1 µF capacitor.

19.3.2 RDRAM Interface

- RDRAM channel termination should be pulled to a 1.8 V source.
- Source generation circuit (RAMREF) is recommended when MECCs are implemented. This circuit should be placed near the MCH to generate RAMREF_FM to the MECC. An identical circuit should be placed on the MECC, to generate the RAMREF_TM signal to REF[1:0]. This is a typical resistor divider circuit and comprises of 160 Ω to V_{TERM} and 560 Ω to GND.

19.3.2.1 Ground Isolation

- Via to ground every ½ inch around edge of isolation island
- Via to ground every ½ inch between RIMMs
- Via to ground every ½ inch between RSL signals
- Via between every signal within 100 mils of the MCH edge and the RIMM/MEC connector edge
- No unconnected ground floods
- All ground isolation at least 6 mils wide
- Ground isolation fills between *serpentines*
- Ground isolation not *broken* by C-TABs
- Ground isolation connects to the ground pins in the middle of the RIMM connectors
- Ground isolation vias connect on all layers and should NOT have thermal relieves
- Ground pins in RIMM connector connect on all layers

19.3.2.2 V_{TERM} Layout Guidelines for Low Noise

Warning: Proper V_{TERM} decoupling is *critical*!

- Solid V_{TERM}-island is on top routing layer; DO NOT split this plane
- Ground island (for ground-side of V_{TERM} caps) is on top routing layer
- Termination Resistors connect DIRECTLY to the V_{TERM} island on the routing (without vias)
- Decoupling capacitors connect to top layer V_{TERM}-island and top routing layer ground island directly
- Use AT LEAST two vias per decoupling capacitor in the top layer ground island
- Use 2 x 100 µF tantalum capacitors to decouple V_{TERM} (aluminum/electrolytic capacitors are too slow)
- High-frequency decoupling capacitors MUST be spread-out across the termination-island so that all termination resistors are near high-frequency capacitors
- 100 µF TANTALUM capacitors should be at each end of the V_{TERM}-island
- 100 µF TANTALUM capacitors must be connected to V_{TERM}-island directly
- 100 µF TANTALUM capacitors must have AT LEAST 2 vias/cap to ground
- V_{TERM}-island should be 50–75 mils wide and should not be broken
- If any RSL signals are routed out of the second RIMM (towards termination) on a plane referenced to power (even for a short distance), ensure that the Ground Reference Plane (on the power plane) is continuous under the termination resistors/capacitors
- Ensure current path for power delivery to the MRH does not go through the V_{TERM}-island

19.3.2.3 CTM/CTM# Routing

- CTM/CTM# are routed differentially from DRCG to second RIMM
- CTM/CTM# are ground isolated from DRCG to second RIMM
- CTM/CTM# are ground referenced from DRCG to second RIMM
- Vias are placed in ground isolation and ground reference every ½”
- If CTM/CTM# serpentine together, they MUST maintain *exactly* 6 mils spacing

19.3.2.4 DRCG Power Supply

- 3.3 V DRCG power flood on the top layer.
- High frequency (0.1 µF) capacitors should be placed near the DRCG power pins, with one capacitor next to each power pin.
- 10 µF bulk *tantalum* capacitor near DRCG connected directly to the 3.3 V DRCG power flood on the top layer.
- Ferrite bead isolating DRCG power flood from 3.3 V main power also connecting directly to the 3.3 VDRCG power flood on the top layer.
- Use two vias on the ground-side of each.

19.3.2.5 DRCG Output Network Layout

- Series resistors (39 Ω) should be *very* near CTM/CTM# pins and parallel resistors (51 Ω) should be very near series resistors.
- CTM/CTM# should be 16 mils wide from the CTM/CTM# pins to the resistors.
- CTM/CTM# should be 16 on 6 routed differential as soon as possible after the resistor network.
- When not 16 on 6, the clocks should be 18 mils wide.
- Ensure CTM/CTM# are ground referenced and the ground reference is connected to the ground plane every ½" to 1". Also ensure CTM/CTM# are ground isolated and the ground isolation is connected to the ground plane every ½" to 1".
- Ensure 15 pF EMI capacitors to ground are removed (the pads are not necessary and removing the pads provides more space for better placement of other components).
- Ensure the 4 pF EMI capacitor (but do not assemble the capacitor).

19.3.2.6 RSL Transmission Line

- RSL traces are 18 mils wide.
- Do NOT neckdown RSL traces to the RIMM connector.
- If tight serpentine configuration is necessary, 10 mil ground isolation MUST be between serpentine segments (i.e., an RSL signal CAN NOT serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines).
- RSL traces do not cross power plane splits. RSL signals must also not be routed *on next to* a power plane splits.
- Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times.
- ALL RSL, CMD/SCK and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin.
- All RSL signals are routed adjacent to a ground reference plane. This includes all signals from the second RIMM to the termination. If signals are routed referenced to ground from the second RIMM to the termination, the ground reference plane MUST extend under these signals AND include the ground-side of the V_{TERM} decoupling capacitors.
- CTABs must not cross (or be on top of) power plane splits. They must be *entirely* referenced to ground.
- At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MRH-R (and the first RIMM) as possible. If possible connect the flood to the ground balls/pins on the MRH-R/connector.

19.3.2.7 V_{REF} Routing

- Do not route V_{REF} near high-speed signals and ensure 1 x 0.1 µF capacitor on V_{REF} at each connector
- Use 10 mil wide trace (6 mils minimum)

19.3.2.8 RSL Routing

- All signals must be length matched within +/- 10 mils of the Nominal RSL Length as described in the *Intel® Workstation/Server MEC Design Guide*. Ensure that signals with a dummy via are compensated correctly.
- ALL RSL signals must have 1 via near the MRH BGA pad. Signals routed on the bottom layer of the MB will have a “real via” while signals routed on the top layer will have a “dummy via.” Additionally, all signals with a dummy via must have an additional trace length of 25 mils.
- Signals must “alternate” layers as shown in “Power Distribution” on page 5-5.

19.3.2.9 RDRAM Clock Routing

- Clock signals must be routed as a differential pair. The traces must be 14 mils wide and 6 mils apart (with no ground isolation.
- Clock signals must be length compensated (using the 1.021 length factor described in Section 8.2.6, “Length Matching Method” on page 8-10). Ensure that each clock pair is length matched within +/- 2 mils.
- If clock signals serpentine, they must serpentine together (to maintain differential 14:6 routing).
- 22 mils ground isolation required on each side of the differential pair.

19.3.2.10 Hub Interface A

- HLAREF reference voltage is ½ of 1.8 V.
- HLACOMP can support either RCOMP or ZCOMP implementation.

19.3.2.11 AGP Interface

- AGP interrupts can be shared with PCI interrupts (PCI Specification, Revision 2.2). It is recommended that interrupts be staggered and each PIRQ should be programmed to a different IRQ.
- AGPREF can be generated with a voltage divider circuit to V_{DDQ}.
- TYPEDET# must be connected to a flexible voltage regulator for V_{DDQ}.
- All AGP pull-up resistors should be pulled to V_{DDQ}.
- V_{REFCG} should be tied to a resistor divider circuit, near the MCH.
- V_{REFGC} should be connected to a FET switch that will supply either locally or source generated V_{REF} to the MCH.

19.3.3 I/O Controller Hub (ICH)

19.3.3.1 AC'97 Interface

- ACSDIN[1:0] require external 8.2 KΩ pull-down if a codec is not present or if the codec is not powered in suspend.

19.3.3.2 APIC Interface

- If the APIC is not used, 150 Ω pull-ups are required on APICD[1:0] and APICCLK must be tied to GND. The APICCLK can also be connected to CK133W/S if unused, but it can not be left floating.

19.3.3.3 FWH Interface

- The FWH INIT pin should be connected directly to the CPUs. This pin must be tied to the FWH to allow the FWH to abort its programming sequence in the event that the CPU is reset during programming stage.
- ID[3:0] should be tied to GND is only one FWH is implemented.

19.3.3.4 Hub Interface A

- Initial stepping of the ICH requires a 110 Ω +/-1% pull-up to 3.3 V on HLAZCOMP. All production stepping requires 40 Ω 1% pull-up to 1.8 V on HLAZCOMP.
- There are two options for HLAZCOMP:
  - RCOMP: Connect 40 Ω 1% pull-up resistor to 1.8 V.
  - ZCOMP: Connect this signal to a 10-mil wide trace that is 18" long. This trace must be not be terminated and my not cross power planes.

19.3.3.5 IDE

- The ICH should be placed as close as possible to the ATA connector(s). The total signal length, from the IDE drivers to the end of the IDE cable, should be less than 26".
- The capacitance of each of the IDE connector (on the host) pins should be less than 25 pF when the cable is disconnected from the host.
- The following signals do not require series termination resistors: PDD[15:0], SDD[15:0], PDIOW#, SDIOW#, PDIOR#, SDIOR#, PDREQ#, SDREQ#, PDDACK#, SDDACK#, PIORDY, SIORDY, PDA[2:0], SDA[2:0], PDCS1#, SDCS1#, PDCS3#, SDCS3#, IRQ14, IRQ15.
- To allow the host to recognize the absence of a device during power-up, a 10 KΩ pull-down resistor should be placed on unused PDD7 or SDD7. If IDE is not implemented, xDREQ and xIORDY should be grounded and other IDE output signals can be left as no connects.
- PCI_RST# should be use as the IDE reset signal and should be connected to pin 1 of the IDE connector(s). The PCIRST# should be buffered to the IDE connector. The IDE reset signal requires series termination.
- Primary IDE connector uses IRQ14 and secondary IDE connector uses IRQ15. These IRQ signals requires additional 8.2 KΩ pull-up to 5 V.

- Pin 34 of the IDE connector should be connected to a GPI. This allows Ultra ATA/66 cable detection. This pin is sampled low if an 80-pin cable is installed, and is sampled high if a 40-pin cable is installed.

19.3.3.6 LPC SIO

- The SIO PME# should be connected to an ICH resume-well GPI. The SIO PME# should not be connected to the PCI PME# because this would violate the ACPI specification.
- The LPC_SMI# signal can be connected to any ICH GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion.
- Additional pull-up resistors are not require on LFRAME#, LAD[3:0] and LDREQ0#.

19.3.3.7 PCI Interface

- PCI control signals require pull-up resistors to ensure that they contain stable values when no agent is actively driving the bus. Pull-up required: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#, REQ64#and ACK64#. SBO# and SDONE must be separately pulled-up with a ~5 KΩ resistor if unused. Also, if boundary scan is not used, TMS and TDI must be independently pulled-up, and TRST# and TCK must be independently pulled-down via 5 KΩ resistors. TDO must be left open.
- 100 Ω series resistor is recommended on IDSEL signals.
- All unused core well inputs must be pulled-up to 3.3 V, and unused resume well inputs must be pulled-up to 3.3VSBY.
- The following signals do not require additional pull-up resistors: PME#, PWRBTN#, GNT#[A:B]
- PCI GNT# pull-ups should not be implemented. The GNT# lines are actively driven by the ICH.
- PCIRST# rise time should be evaluated in large I/O systems, buffering may be needed. This signal must be buffered to the IDE connectors.

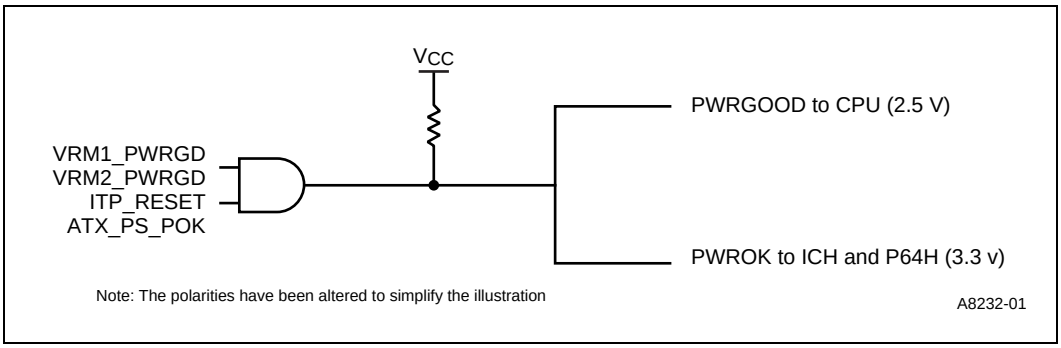
19.3.3.8 Power and Ground

- $5V_{REF}$ must be tied to 5 V in a 5 V tolerant or non-tolerant system. This signal must be power up before or simultaneous to V_{CC5}, and it must be power down after or simultaneous to V_{CC5}. In a STR system, $5V_{REF}$ can be tied to the V_{CC5} since there will be no 5 V signals active during the STR state.
- A Schottky diode in the $5V_{REF}$ circuit for a minimum voltage drop from $V_{CC3.3}$ to $5V_{REF}$ because there is an internal diode in parallel to the Schottky diode that does not have high current capability. The Schottky diode will begin to conduct first, carrying the high current.

Power Management

- A power button is required by the ACPI specification. PWRBTN# is connected to the front panel on/off power button. The ICH integrates 16 ms debouncing logic on this pin and AC power loss circuitry has been integrated into the ICH to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a schmitt trigger to square-off and maintain its signal integrity, and not be connected directly to logic on the board. PS_POK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, making sure that the input to the ICH is at a 3 V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed V_{CC}(RTC). It is recommended that 3.3 V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from V_{CC5}.
- The PWROK signal to the chipset is a 3 V signal. The core well power valid to PWROK asserted at the chipset is a minimum of 1ms. PWROK to the chipset must be deasserted a minimum of 0 ns after RSMRST#.
- PWRGOOD signal to CPU is driven with an open collector buffer pulled up to 2.5 V using a 330 Ω resistor.
- Figure 19-1 a simplified diagram of the PWRGOOD and PWROK logic, connected to the CPU and ICH respectively in a DP system. The circuitry checks for both slots occupied, both CPU VRMs powered up, and the PS_POK signal from the ATX power supply connector before asserting PWRGOOD and PWROK to the CPU, ICH and P64H.

Figure 19-1. PWRGOOD and PWROK Generation Logic



- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shut-down feature.
- SLP_S3# from the ICH must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- The SLP_S3# from the ICH must connected to the SLEEP of the WTX power supply connector to control the state of the core well during sleep states.
- The PS_ON of the WTX power supply connector is control by ICH SLP_S5# and P0/P1_PRES signals.

19.3.3.9 RTC

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1". It is recommended to minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them), and place a ground plane under all of the external RTC circuitry. Do not route any switching signals under the external components (unless on the other side of the ground plane).
- Provide a 1 µF 805 X5R dielectric, monolithic, ceramic capacitor on the VCCRTC pin. The cap +ve connection should not be stubbed off the trace run and must be as close as possible to the ICH. If a stub is required, it should be within a few mm of the maximum length. The ground connection must be made through a via to the plane with no trace between the capacitor pad and the via.
- Place the battery, 1 K series current limit resistor, and the common-cathode isolation diode very close to the ICH. If this is not possible, place the common-cathode diode and the 1 KΩ resistor as close to the 1 µF cap as possible. Do not place these components between the cap and the ICH. The battery can be placed remotely from the ICH.
- On boards that have chassis-intrusion utilizing inverters powered by the VCCRTC pin, place the inverters as close to the common-cathode diode as possible. If this is not possible, keep the trace run near the center of the board.

19.3.3.10 SMBus/Alert Bus

- If the Alert-on-LAN signals are used, 4.7 KΩ pull-up resistors to 3.3VSBY are required. Otherwise, if the Alert-on-LAN signals are used as GPIOs, pull-up resistors to 3.3VSBY are required. The signals must be allowed to change states on power-up. The pull-up resistor values depend on the loading on the GPIO signals.
- ALERTCLK and ALERTDATA requires 4.7 KΩ pull-up resistors to 3.3VSBY if unused.
- SMBus implementation needs to provide proper isolation if there are SMBus devices that are both powered by V_{CC} and VCCSBY. SMBus devices powered by 3.3VCCSBY requires pull-up resistors.
- The value if the SMBus pull-up resistors should reflect the number of loads on the bus. For implementation with 4-5 loads, 4.7 KΩ are recommended. OEMs should complete simulation to determine the exact value.

19.3.3.11 USB Interface

- The AGP OVRCNT# pin should be pulled-up with a 330 KΩ resistor to 3.3 V, on the motherboard, to prevent this line from floating when add-in card is not present.
- 15 Ω resistors should be used on D-/D+ data lines.
- V_{CC} USB (cable power) should be power off the 5 V source, rather than 5VSBY.
- The resistive component of the fuses, ferrite beads and traces must be considered when choosing components and power/GND trace width. This must be done such that the resistance between the $5V_{CC}$ power supply and the host USB port is minimized. Minimizing the resistance will also minimize voltage drop seen along the path.
- Sufficient bypass capacitance should be located near the host USB receptacles. This is to minimize the voltage droop that occurs upon hot attach of new devices.
- For complete USB design and layout guidelines, please refer to (Intel Confidential) *82371AB PIIX4 Application Note #1-USB Design Guide and Checklist*.

19.3.3.12 Firmware Hub (FWH)

- If an ATE is used to program the FWH, it is recommended that pull-up resistors be added to the FGPI pins. Otherwise, unused FGPI pins can be tied to V_{CC} or GND.
- FWH INIT# should be connected to CPU INIT#.
- FWH RST# must be connected to ICH PCIRST#.

19.3.4 PCI 64-bit Hub (P64H)

19.3.4.1 APIC Interface

- All I/O APIC IRQs are wired-OR to BT_INTR#. The BT_INTR# signal should be connected to ICH PCI interrupt to support boot devices on the P64H PCI segment. This signal is internally disabled once the I/O APIC is enabled.
- External pull-up resistors are required on APICCLK and APICD[1:0] if P64H APIC is not used.
- Additional pull-up resistors are recommended on all IRQ signals.

19.3.4.2 Hub Interface B

- HUBREF reference voltage is 2/3 1.8 V.
- HLBRCOMP requires a 30 Ω pull-down resistor to GND.

19.3.4.3 PCI Interface

- Per the PCI Specification, pull-up resistor must be added to AD[63:32], C/BE[7:4] and PAR64. This prevent floating input if a 32-bit PCI card is installed into a 64-bit PCI connector.
- PCI GNT# pull-up resistor should not be implemented. These signals are actively driven by the P64H.

19.3.4.4 PCI Clocks

- Unused clock outputs (PCLKOUT) can be left as N/C. These clock outputs must be disable via the P64H Configuration register.

19.3.4.5 Power and Ground

- PCI 66 MHz operates with 3.3 V signaling only.
- PVCC5REF and VCC5REF are P64H voltage reference pins. For a 3.3 V-only environment, these signals can be tied together to a 3.3 V source. For a 5 V tolerant environment, a Schottky diode should be used to ensure that the 5 V reference voltage powers up before or simultaneous to the 3.3 V source.
  - VCC5REF (ball P7) is used for the hot plug interface and RSTIN#.
  - VCC5REF (ball H17) is used for the IRQs, TEST# and BT_INTR#.
  - PVCC5REF (ball F4) is used for the PCI interface.

19.3.5 CK133W/S Clock Synthesizer

- All unused clock outputs should be tied to GDN through a series resistor. The resistor value should be the approximately the impedance of the output buffer. The intent of these termination resistors is to eliminate the EMI radiation.
- 33 Ω series resistors are recommended on all clock outputs.
- Ganging the CPUCLK signals improves the output-to-output skew. This implementation requires that all CPUCLK signals be tied (short) together.
- If power-down mode is not supported, it is recommended that PWRDWN# be pulled-up with to 3.3 V via a 10 KΩ resistor.
- SEL pins can be used to select special functionality using 10 KΩ pull-up resistors, as listed in Table 19-1:

Table 19-1. SEL Pins Special Functions

SEL133/100#	SEL1	SEL0	FUNCTION
0	0	0	Three-state
0	0	1	RESERVED
0	1	0	Active 100 MHz, 48 MHz PLL inactive
0	1	1	Active 100 MHz, 48 MHz PLL active
1	0	0	Test Mode
1	0	1	RESERVED
1	1	0	Active 133 MHz, 48 MHz PLL inactive
1	1	1	Active 133 MHz, 48 MHz PLL active

Check with your clock vendor and the reference schematics for decoupling considerations.

19.4 Design Checklist

The following checklist is intended to be used for Intel 840 Chipset design schematic reviews. This checklist should be used with the Pentium® III processor/Intel 840 chipset evaluation board (dual FC-PGA Pentium III processor at 100 MHz PSB) schematics and can be used for dual processor 133 MHz systems. This checklist represents only one possible system configuration and will be revised as new information becomes available. Please note that V_{CC}, V_{SS} and GND signals are not included into the below connectivity checklist.

19.4.1 FC-PGA Intel® Pentium® III Processors

Table 19-2. FC-PGA Intel® Pentium® III Processor and Intel 840 Chipset Connectivity[1]

CPU Pin	I/O	Comments
A[35:3]#[2]	I/O	Connect to MCH.
ADS#[2]	I/O	Connect to MCH.
AERR#	I/O	Leave as No Connect.
AP[1:0]#	I/O	Connect to MCH.
BERR#	I/O	Connect to MCH.
BINIT#	I/O	Leave as No Connect.
BNR#[2]	I/O	Connect to MCH.
BP[3:2]#	I/O	Leave as No Connect.
BPM[1:0]	I/O	Leave as No Connect.
BPRI#[2]	I	Connect to MCH.
BREQ0# / BR0#[3]	I/O	Tie BR0# of CPU1 to BR1# of CPU2. Connect to MCH.
BREQ1# / BR1#[3]	I	Tie BR1# of CPU1 to BR0# of CPU2
D[63:0]#[2]	I/O	Connect to MCH.
DBSY#[2]	I/O	Connect to MCH.
DEFER#[2]	I	Connect to MCH.
DEP[7:0]#	I/O	Connect to MCH.
DRDY#[2]	I/O	Connect to MCH.
HIT#[2]	I/O	Connect to MCH.
HITM#[2]	I/O	Connect to MCH.
LOCK#[2]	I/O	Connect to MCH.
REQ[4:0]#[2]	I/O	Connect to MCH.
RESET#[3]	I	150 Ω pullup to V_{TT} at each processor. Connect to MCH. (Optional Debug) 240 Ω series resistor to ITP.
RESET2#	I	Connect to GND.
RP#	I/O	Connect to MCH.
RS[2:0]#	I	Connect to MCH.
RSP#	I	Connect to MCH.
TRDY#[2]	I	Connect to MCH.

NOTES:
1. This table provides connectivity guideline for DP FCPGA Pentium III processor design. It does not provide connectivity for backward compatibility.
2. For FCPGA Pentium III processor, on die AGTL+ termination is provided by the processor (**except RESET#**).
3. These signal connections are different for uniprocessor designs. See Table 19-7 on page 19-16.

Table 19-3. CMOS Connectivity Checklist for 370-Pin Socket Processors

CPU Pin	I/O	Comments
A20M#	I	150 Ω pull-up resistor to V_{CC_CMOS}. Connect to ICH.
FERR#	O	150 Ω pull-up resistor to V_{CC_CMOS}. Connect to ICH.
FLUSH#	I	150 Ω pull-up resistor to V_{CC_CMOS}.
IERR#	O	150 Ω pullup resistor to V_{CC_CMOS}. Connect to MCH.
IGNNE#	I	150 Ω pull-up resistor to V_{CC_CMOS}. Connect to ICH.
INIT#	I	150 Ω pull-up resistor to V_{CC_CMOS}. Connect to ICH and FWH.
LINT0/INTR LINT1/NMI	I	150 Ω pull-up resistor to V_{CC_CMOS}. Connect to ICH.
PICD[1:0]	I/O	Two 300 Ω pull-up resistor to V_{CC_CMOS}, one near the processor, another near chipset, at furthest point. Connect to ICH and P64H.
PREQ#	I	200-330 Ω pull-up resistor to V_{CC_CMOS}. Connect to ITP.
PWRGOOD	I	150-330 Ω pull-up to $V_{CC2.5}$, output from the PWRGOOD logic.
SLP#	I	150 Ω pull-up to V_{CC_CMOS}. Connect to ICH.
SMI#	I	150 Ω pull-up to V_{CC_CMOS}. Connect to ICH.
STPCLK#	I	150 Ω pull-up to V_{CC_CMOS}. Connect to ICH.
THERMTRIP#	O	150 Ω pull-up resistor to V_{CC_CMOS}. Connect processor one THERMTRIP# pin to processor two THERMTRIP# pin.

Table 19-4. TAP Checklist for 370-Pin Socket Processors[1, 2]

CPU Pin	I/O	Comments
TCK	I	1 KΩ pull-up resistor to V_{CC_CMOS}. Connect to ITP through bessel filter.
TDI	I	330 Ω pull-up resistor to V_{CC_CMOS}. Connect to ITP.
TDO	O	150 Ω pull-up resistor to V_{CC_CMOS}. Connect to ITP.
TMS	I	1 K Ω pull-up resistor to V_{CC_CMOS}. Connect to ITP through bessel filter.
TRST#	I	~680 Ω pull-down resistor to ground. Connect to ITP.
PRDY#	I	150 Ω pull-up resistor to V_{TT}. 240 Ω series resistor to ITP.

NOTES:
1. The ITP connector is different than the one previously specified for other Intel IA-32 processors. It is the female counterpart to the previously specified connector and is specifically for use with processors utilizing 1.5 V CMOS TAP I/O signals. See the EMTS for more details.
2. The FC-PGA Pentium III processor requires an ITP with a 1.5 V tolerant buffer board. Previous ITPs are designed to work higher voltages and may damage the processor if they are connected to an FC-PGA Pentium III processor.

Table 19-5. Miscellaneous Checklist for 370-Pin Socket Processors (Sheet 1 of 2)

CPU Pin	I/O	Comments
BCLK[1]	I	Connect to clock generator and MCH. To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the MCH and processor. A 0 Ω ± 5% series resistor place near to the clock driver is recommended.
BSEL0	I/O	1 KΩ pull-up resistor to $V_{CC3.3}$.
BSEL1	I/O	1 KΩ pullup resistor to $V_{CC3.3}$, connect to CK133.
CLKREF	I	Connect to divider on $V_{CC2.5}$ or $V_{CC3.3}$ to create 1.25 V reference with a 4.7 µF decoupling capacitor. Use 330 Ω resistor divider created from 1% tolerance resistors. Do not use V_{TT} as source voltage for this reference!
CPUPRES#	O	Leave as No Connect or tie to GND. (Optional) Connected to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1 K – 10 KΩ pull-up resistor to $V_{CC3.3}$.
EDGCTRL	I	Not used by FCPGA Pentium III processor. Leave as No Connect.
PICCLK	I	Connect to clock generator and APIC agent. A 22Ω±5% series resistor place near to the clock driver is recommended.
PLL1, PLL2	I	Low pass filter on VCC_CORE provided on motherboard. Typically a 4.7 µH inductor in series with V_{CC_CORE} is connected to PLL1 then through a series 33 µF capacitor to PLL2.
RTTCTRL (S35)[2]	I	68 Ω ±1% pull-down resistor to ground.
SLEWCTRL (E27)	I	110 Ω ±1% pull-down resistor to ground.
THERMDN	O	No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
THERMDP	I	No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
$V_{CC1.5}$	I	Connected to same voltage source as V_{TT}.
$V_{CC2.5}$	I	Not used by FCPGA Pentium III processor. Leave as No Connect.
V_{CC_CMOS}	O	Used as pull-up voltage source for CMOS signals between processor and chipset and for TAP signals between processor and ITP. Must have some decoupling (HF/LF) present.
V_{CC_CORE}	I	10 ea (min) 4.7 µF in 1206 package all placed within the PGA370 socket cavity. 4 ea (min) 10 µF in 1210 package placed near the PGA370 socket cavity. 4 ea (min) 820 µF placed near the PGA370 socket cavity.
V_{CORE_DET} (E21)	O	Leave as No Connect or tie to GND. (Optional) Connect to PWRGOOD logic to prevent system from powering up if an Intel® Celeron™ processor is installed.
VID[3:0]	O	Connect to VR or VRM. For on-board VR, 10 KΩ pullup resistor to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pullups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.

NOTES:
1. These termination resistors act as damping resistors to eliminate high speed signal reflection. Proper timing of the resistor values must be ensured.
2. These signal connections are different for uniprocessor designs. See Table 19-7 on page 19-16.

Table 19-5. Miscellaneous Checklist for 370-Pin Socket Processors (Sheet 2 of 2)

CPU Pin	I/O	Comments
VREF[7:0]	I	Connect to V_{REF} voltage divider made up of 75 and 150 Ω 1% resistors connected to V_{TT}. Decoupling Guidelines: 4 ea. (min) 0.1 µF in 0603 package and 2 ea (min) 1 µF in 0805 package placed within 500 mils of V_{REF} pins.
V_{TT}	I	Connect AA33, AA35, AH20, AK16, AL13, AL21, AN11, AN15, AN21, E23, G35, S33, S37, U35 and U37 to 1.5 V regulator. Provide high and low frequency decoupling. Decoupling Guidelines: 2 ea (min) 4.7 µF in 1206 package and 3 ea (min) 0.1 µF in 0603 package. Connect pin G37 (RESERVED) to V_{TT}.
RESERVED	N/A	The following pins must be left as no-connects: AK30, AM2, F10, L33, N33, N35, N37, Q33, Q35, Q37, R2, W35, Y1

NOTES:
1. These termination resistors act as damping resistors to eliminate high speed signal reflection. Proper timing of the resistor values must be ensured.
2. These signal connections are different for uniprocessor designs. See Table 19-7 on page 19-16.

Table 19-6. Clock Generator Checklist

Checklist Line Items[1]	Comments
CPU	Series resistor 0 Ω ± 5%. Refer to Figure 17-1.
3V66	Series resistor 22 Ω ± 5%. cap: 18 pF ± 2%.
PCI	Series resistor 22 Ω ± 5%.
TCLK	Series resistor 22 Ω ± 5%.
OCLK/RCLK	Series resistor 33 Ω ± 5%.
48 MHz	Series resistor 33 Ω ± 5%.
APIC	Series resistor 22 Ω ± 5%.
REF	Series resistor 10 Ω ± 5%.

NOTE:
1. These termination resistors act as damping resistors to eliminate high speed signal reflection. Proper timing of the resistor values must be ensured.

Four signals are implemented differently for uniprocessor systems, as shown in Table 19-7. All other signals are as defined above.

Table 19-7. Signal Differences for Uniprocessor Intel® 840 Chipset Systems

CPU Pin	I/O	Comments
BREQ0#	I/O	Connect to MCH
BREQ1#	I	No Connect
RESET#	I	150 Ω pull-up to V_{TT}. Connect to MCH. (Optional Debug) 240 Ω series resistor to ITP.
R_{TT_CTRL}	I	The R_{TT_CTRL} input signal provides AGTL+ termination control. For uniprocessor implementations, both on-die and on-board termination is required. Placing a 62 Ω, 1% resistor on the RTT_CTRL pin to ground will set the appropriate on-die R_{TT} value for the uniprocessor topology.

19.4.2 82840 Memory Controller Hub (MCH)

Table 19-8. MCH Connectivity (Sheet 1 of 3)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
ADS#		Connect to CPUs.
ADSTB0	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
ADSTB0#	8.2 KΩ PD to GND	Connect to AGP device.
ADSTB1	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
ADSTB1#	8.2 KΩ PD to GND	Connect to AGP device.
AGPRCOMP	40.2 Ω PD to GND	
AGPREF		Connect to AGP voltage reference circuit.
AP0#		Connect to CPUs.
AP1#		Connect to CPUs.
BERR#		Connect to CPUs.
BNR#		Connect to CPUs.
BPRI#		Connect to CPUs.
BREQ0#		Connect to CPUs.
CHA_CFM		Connect to RIMMs or MECC.
CHA_CFM#		Connect to RIMMs or MECC.
CHA_CMD	Refer to the circuit shown on Figure 8-15	Connect to RIMMs or MECC.
CHA_CTM		Connect to RIMMs or MECC.
CHA_CTM#		Connect to RIMMs or MECC.
CHA_DQA[0:8]		Connect to RIMMs or MECC.
CHA_DQB[0:8]		Connect to RIMMs or MECC.
CHA_EXP0	28 Ω PU to $V_{CC1.8}$ or N/C with RIMMs down solution	Connect to RIMMs or MECC.
CHA_EXP1	28 Ω PU to $V_{CC1.8}$ or N/C with RIMMs down solution	Connect to RIMMs or MECC.
CHA_REF0		Connect to CHA_REF1 through noise filter.
CHA_REF1		Connect to CHA_REF0 through noise filter.

Table 19-8. MCH Connectivity (Sheet 2 of 3)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
CHA_RQ[0:7]		Connect to RIMMs or MECC.
CHA_SCK	Refer to the circuit shown on Figure 8-15	Connect to RIMMs or MECC.
CHA_SIO		Connect to RIMMs or MECC.
CHB_CFM		Connect to RIMMs or MECC.
CHB_CFM#		Connect to RIMMs or MECC.
CHB_CMD	Refer to the circuit shown on Figure 8-15	Connect to RIMMs or MECC.
CHB_CTM		Connect to RIMMs or MECC.
CHB_CTM#		Connect to RIMMs or MECC.
CHB_DQA[0:8]		Connect to RIMMs or MECC.
CHB_DQB[0:8]		Connect to RIMMs or MECC.
CHB_EXP0	28 Ω PU to $V_{CC1.8}$ or N/C with RIMMs down solution	Connect to MECC.
CHB_EXP1	28 Ω PU to $V_{CC1.8}$ or N/C with RIMMs down solution	Connect to MECC.
CHB_REF0		Connect to CHB_REF1 through noise filter.
CHB_REF1		Connect to CHB_REF0 through noise filter.
CHB_RQ[0:7]		Connect to RIMMs or MECC.
CHB_SCK	Refer to the circuit shown on Figure 8-15	Connect to RIMMs or MECC.
CHB_SIO		Connect to RIMMs or MECC.
CLK66		Connect to clock synthesizer.
CPURST#	Two 150 Ω PU to $V_{TT1.5}$	Connect to CPUs.
DBSY#		Connect to CPUs.
DEFER#		Connect to CPUs.
DEP[0:7]#		Connect to CPUs.
DRDY#		Connect to CPUs.
GAD[0:31]		Connect to AGP device.
GC/BE[0:3]#		Connect to AGP device.
GDEVSEL#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GFRAME#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GGNT#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GIRDY#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GPAR	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GREQ#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GSERR#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GSTOP#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
GTLREFA	75Ω/150Ω	Connect to resistor divider circuit.
GTLREFB	75Ω/150Ω	Connect to resistor divider circuit.
GTRDY#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
HA[3:35]#		Connect to CPUs.
HCLKIN		Connect to clock synthesizer.

Table 19-8. MCH Connectivity (Sheet 3 of 3)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
HCLKOUTA		Connect to DRCG.
HCLKOUTB		Connect to DRCG
HD[0:63]#		Connect to CPUs.
HIT#		Connect to CPUs.
HITM#		Connect to CPUs.
HLA[0:11]		Connect to ICH.
HLA_REF	Figure 10-3 and Figure 10-4	Connect to HLA HUBREF generation circuit.
HLA_STB		Connect to ICH.
HLA_STB#		Connect to ICH.
HLA_ZCOMP	40.2 Ω PU to $V_{CC1.8}$	
HLB[0:19]		Connect to P64H.
HLBREF	Figure 10-5 and Figure 10-6	Connect to HLB HUBREF generation circuit.
HLB_STB0		Connect to P64H.
HLB_STB0#		Connect to P64H.
HLB_STB1		Connect to P64H.
HLB_STB1#		Connect to P64H.
HLB_ZCOMP	30 Ω PD to GND	
HLOCK#		Connect to CPUs.
HREQ[0:4]#		Connect to CPUs.
HTRDY#		Connect to CPUs.
IERR#		Connect to CPUs.
OVERT#	10 KΩ PU to $V_{CC1.8}$	
PIPE#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
RBF#	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
RCLKOUTA		Connect to DRCG
RCLKOUTB		Connect to DRCG
RP#		Connect to CPUs.
RS[0:2]#		Connect to CPUs.
RSP#		Connect to CPUs.
RSTIN#		Connect to ICH.
SBA[0:7]		Connect to AGP device.
SBSTB	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
SBSTB#	8.2 KΩ PD to GND	Connect to AGP device.
ST[0:2]	8.2 KΩ PU to V_{DDQ}	Connect to AGP device.
TEST#	10 KΩ P/U to $V_{CC1.8}$	
WBF#	8.2 K PU to V_{DDQ}	Connect to AGP device.

19.4.3 I/O Controller Hub (ICH)

Table 19-9. ICH Connectivity (Sheet 1 of 4)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
A20GATE	8.2 KΩ PU to $V_{CC3.3}$	Connect to SIO.
A20M#	150 Ω PU to V_{CC_CMOS}	Connect to CPUs.
AC_BITCLK		Connect to audio codec
AC_RST#		Connect to audio codec
AC_SDIN0		Connect to audio codec
AC_SDIN1/GPIO9	8.2 KΩ PD to GND	
AC_SDOUT		Connect to audio codec
AC_SYNC		Connect to audio codec
AD[31:0]		Connect to all PCI connectors/devices.
APICCLK		Connect to clock synthesizer.
APICD0	300 Ω x 2 PU to $V_{CC1.5}$	Connect to CPUs, ICH and P64H.
APICD1	300 Ω PU to $V_{CC1.5}$	Connect to CPUs, ICH and P64H.
C/BE[0:3]#		Connect to all PCI connectors/devices.
CLK14		Connect to clock synthesizer.
CLK48		Connect to clock synthesizer
CLK66		Connect to clock synthesizer
DEVSEL#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI connectors/devices.
FERR#	1 KΩ PU to $V_{CC1.5}$	Connect to CPUs.
FRAME#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI connectors/devices.
GNT[0:4]#		Connect to PCI connectors/devices.
GPIO0/ REQA#	8.2 KΩ PU to $V_{CC3.3}$	
GPIO1/REQB#/ REQ5#	8.2 KΩ PU to $V_{CC3.3}$	Connect to PCI connector/device.
GPIO10/ INTRUDER#	8.2 KΩ PU to $V_{CC3.3SBY}$	
GPIO12	8.2 KΩ PU to $V_{CC3.3SBY}$	
GPIO13	8.2 KΩ PU to $V_{CC3.3SBY}$	
GPIO16/ GNTA#	N/C	
GPIO17/ GNTB#/ GNT5#		Connect to PCI device.
GPIO22	N/C	
GPIO23	4.7 KΩ PD to GND	Connect to front panel LEDs.
GPIO24/ SLP_S3#		Connect to power connector.
GPIO25/ SUSSTAT#		

Table 19-9. ICH Connectivity (Sheet 2 of 4)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
GPIO27/ ALERTCLK	4.7 KΩ PU to $V_{CC3.3SBY}$	Connect to 82559.
GPIO28/ ALERTDATA	4.7 KΩ PU to $V_{CC3.3SBY}$	Connect to 82559.
GPIO5	8.2 KΩ PU to $V_{CC3.3}$	Connect to LPC SIO device.
GPIO6	8.2 KΩ PU to $V_{CC3.3}$	Connect to LPC SIO device.
GPIO8/ LDRQ1#	8.2 KΩ PU to $V_{CC3.3SBY}$	
GPIO9/ AC_SDIN1	8.2 KΩ PD to GND	
HLA[0:11]		Connect to MCH.
HL_STB		Connect to MCH.
HL_STB#		Connect to MCH.
HLCOMP	40.2 Ω PU to $V_{CC1.8}$	
HUBREF		Connect to HUBREF generation circuit.
IGNNE#	150 Ω PU to V_{CC_CMOS}	Connect to CPUs.
INIT#	150 Ω PU to V_{CC_CMOS}	Connect to CPUs, FWH.
INTR	150 Ω PU to V_{CC_CMOS}	Connect to CPUs.
IRDY#	8.2 KΩ PU to $V_{CC3.3}$	Connect to PCI devices, 82559 and ICH.
IRQ14	8.2 KΩ PU to V_{CC5}	Connect to IDE connector.
IRQ15	8.2 KΩ PU to V_{CC5}	Connect to IDE connector.
LAD0/ FWH0		Connect to FWH and LPC SIO device.
LAD1/ FWH1		Connect to FWH and LPC SIO device.
LAD2/ FWH2		Connect to FWH and LPC SIO device.
LAD3/ FWH3		Connect to FWH and LPC SIO device.
LDRQ0#		Connect to LPC SIO device.
LFRAME#/ FWH4		Connect to FWH and LPC SIO device.
NMI	150 Ω PU to V_{CC_CMOS}	Connect to CPUs.
OC0#		Connect to USB connector.
OC1#		Connect to USB connector.
PAR		Connect to all PCI devices.
PCICLK		Connect to clock synthesizer.
PCIRST#	33Ω series resistor to IDE connector.	Connect through buffer logic to MCH, P64H, FWH, LPC SIO, MECC, AGP and all PCI devices.
PDA[0:2]		Connect to primary IDE connector.
PDCS1#		Connect to primary IDE connector.
PDCS3#		Connect to primary IDE connector.
PDD[0:15]	10 KΩ PD to GND on PDD7.	Connect to primary IDE connector.
PDDACK#		Connect to primary IDE connector.

Table 19-9. ICH Connectivity (Sheet 3 of 4)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
PDDREQ	5.6 KΩ PD to GND	Connect to primary IDE connector.
PDIOR#		Connect to primary IDE connector.
PDIOW#		Connect to primary IDE connector.
PERR#/ GPIO7	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
PIORDY	1 KΩ PU to V_{CC5}	Connect to primary IDE connector.
PIRQA#	8.2 KΩ PU to $V_{CC3.3}$	Connect to AGP and all PCI devices.
PIRQB#	8.2 KΩ PU to $V_{CC3.3}$	Connect to AGP and all PCI devices.
PIRQC#	8.2 KΩ PU to $V_{CC3.3}$	Connect to AGP and all PCI devices.
PIRQD#	8.2 KΩ PU to $V_{CC3.3}$	Connect to AGP and all PCI devices.
PLOCK#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
PME#		Connect to AGP and all PCI devices.
PWRBTN#		Connect $V_{CC3.3SBY}$.
PWROK		Connect to PWROK logic.
RCIN#	8.2 KΩ PU to $V_{CC3.3}$	Connect to LPC SIO.
REQ[0:4]#	8.2 KΩ PU to $V_{CC3.3}$	Connect to PCI devices.
RI#		Connect to serial port and RI logic.
RTCRST#	CLR CMOS: 1 KΩ to GND.	NORMAL: generated from $V_{CC3.3SBY}$
RTCX1		Connect to clock crystal.
RTCX2		Connect to clock crystal.
SDA[0:2]		Connect to secondary IDE connector.
SDCS1#		Connect to secondary IDE connector.
SDCS3#		Connect to secondary IDE connector.
SDD[0:15]	10 KΩ PD to GND on SDD7.	Connect to secondary IDE connector.
SDDACK#		Connect to secondary IDE connector.
SDDREQ	5.6 KΩ PD to GND	Connect to secondary IDE connector.
SDIOR#		Connect to secondary IDE connector.
SDIOW#		Connect to secondary IDE connector.
SERIRQ	8.2 KΩ PU to $V_{CC3.3}$	Connect to LPC SIO.
SERR#	8.2 K PU to $V_{CC3.3}$	Connect to all PCI devices.
SIORDY	1 KΩ PU to V_{CC5}	Connect to secondary IDE connector.
SLP_S5#		Connect to Power Connectors
SMI#	150 Ω PU to V_{CC_CMOS}	Connect to CPUs.
SPKR		Connect to audio codec or speaker circuit.
STOP#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
STPCLK#	150 Ω PU to V_{CC_CMOS}	Connect to CPUs.
SUSCLK/ GPIO26		Connect to LEDs.
THRM#	1 KΩ PU to $V_{CC3.3}$	No additional connection required.

Table 19-9. ICH Connectivity (Sheet 4 of 4)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
TRDY#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
USBP0-		Connect to USB port.
USBP0+		Connect to USB port.
USBP1-		Connect to USB port.
USBP1+		Connect to USB port.
VBIAS		Connect to RTCX1 through a 10 MΩ resistor and to VCCRTC through a 2.2 nF capacitor.
VCCRTC		Connect to $V_{CC3.3SBY}$.
VCCSUS0/1		Connect to $V_{CC3.3SBY}$.
VCC5REF	1 KΩ PU to V_{CC5}.	Connect to $V_{CC3.3}$ via a schottky diode.

19.4.4 Firmware Hub (FWH)- 40Lead TSOP

Table 19-10. FWH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
CLK		Connect to clock synthesizer.
FGP[14:10]	8.2 KΩ PD to GND	
FWH[3:0]		Connect to GND.
FWH4		Connect to ICH and LPC SIO.
IC	8.2 KΩ PD to GND	
ID[3:0]		Connect to GND.
INIT#	150 Ω PU to V_{CC_CMOS}	Connect to CPUs and ICH.
NC[6:3]	N/C	
NC1	N/C	
NC[14:13]	N/C	
NC8	N/C	
RFU[36:32]	N/C	
RST#		Connect to all PCI devices off of the ICH.
TBL#		Connect to $V_{CC3.3}$.
VPP		Connect to $V_{CC3.3}$.
WP#	4.7 KΩ PU to $V_{CC3.3}$	

19.4.5 PCI 64-bit Hub (P64H)

If P64H is not used, refer to “Unused Hub Interface B” on page 10-5.

Table 19-11. P64H Connectivity (Sheet 1 of 2)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
ACK64#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
AD[63:0]	8.2 KΩ PU to $V_{CC3.3}$ on [64:32]	Connect to all PCI devices.
APICCLK		Connect to clock synthesizer.
APICD[1:0]	300 Ω x 2 PU to V_{CC_CMOS}	Connect to CPUs and ICH
BT_INTR#		Connect to ICH.
C/BE#[7:0]	8.2 KΩ PU to $V_{CC3.3}$	Connect to PCI devices.
CLK66		Connect to clock synthesizer
DEVSEL#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
FRAME#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
GNT#[1:0]	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
GNT[5:2]	N/C	
HLB[19:0]		Connect to MCH.
HLB_STB0		Connect to MCH
HLB_STB0#		Connect to MCH
HLB_STB1		Connect to MCH
HLB_STB1#		Connect to MCH
HLBRCOMP	30 Ω 1% PD to GND	
HUBREF		Connected to 2/3V_{TERM} HUBREF circuit.
IRDY#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
IRQ[23:0]	8.2 KΩ PU to $V_{CC3.3}$	Connect to PCI devices.
M66EN	0.01 µF capacitor to GND	Connect to PCI devices.
PAR	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
PAR64	8.2 K PU to $V_{CC3.3}$	Connect to all PCI devices.
PCIRST#	N/C	
PCLKFBIN		Connect to PCLKFBOUT.
PCLKFBOUT		Connect to PCLKFBIN via 33Ω series resistor.
PCLKOUT[1:0]		Connect to all PCI devices via 33Ω series resistor.
PCLKOUT[2:5]	N/C (unused)	
PERR#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
PLOCK#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
PVCC5REF	(5 V) 1 KΩ PU to V_{CC5}.	(5 V) Connect to $V_{CC3.3}$ via a schottky diode. (3 V) Connect to $V_{CC3.3}$.

Table 19-11. P64H Connectivity (Sheet 2 of 2)

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
REQ#[0:5]	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
REQ64#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
RSTIN#		Connect to ICH.
RSV1	8.2 KΩ PD to GND	
RSV2		No connect
RSV3	8.2 KΩ PD to GND	
RSV4		No connect
RSV5		No connect
RSV6		No connect
RSV7		No connect
RSV8		No connect
RSV9		No connect
RSV10		No connect
RSV11		No connect
RSV12		No connect
RSV13		No connect
RSV14		No connect
RSV15		No connect
SERR#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
STOP#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
TEST#	10 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
TRDY#	8.2 KΩ PU to $V_{CC3.3}$	Connect to all PCI devices.
VCC5REF	(5 V) 1 KΩ PU to V_{CC5}.	(5 V) Connect to $V_{CC3.3}$ via a schottky diode. (3 V) Connect to $V_{CC3.3}$.

AGTL+ Design Guidelines A

A.1 Pre-Layout Simulation

A.1.1 Methodology

Analog simulations are recommended for high speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working solution space that meets flight time and signal quality requirements. The layout recommendations in the previous sections are based on pre-layout simulations conducted at Intel. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the **device pads** for signal quality and at the **device pins** for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package, Z_0, and S_0 are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to minimum flight time, maximum flight time, and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnects. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

A.1.1.1. Simulation Criteria

Accurate simulations require that the actual range of parameters be used in the simulations. Intel has consistently measured the cross-sectional resistivity of the PCB copper to be approximately 1 Ω*mil^2/inch, not the 0.662 Ω*mil^2/inch value for annealed copper that is published in reference material. Using the 1 Ω*mil^2/inch value may increase the accuracy of lossy simulations.

Positioning drivers with faster edges closer to the middle of the network typically results in more noise than positioning them towards the ends. However, Intel has shown that drivers located in all positions (given appropriate variations in the other network parameters) can generate the worst-case noise margin. Intel recommends simulating the networks from all driver locations, and analyzing each receiver for each possible driver.

Analysis has shown that both fast and slow corner conditions must be run for both rising and falling edge transitions. The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum, causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. Slow corner models may produce minimum flight time violations on rising edges if the transition starts

from a higher V_{OL}. Intel highly recommends checking for minimum and maximum flight time violations with both the fast and slow corner models. The fast and slow corner I/O buffer models are contained in the processor and Intel 840 chipset electronic models provided by Intel.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. The package model must also be placed between a net and the input of a receiver model. Editing the simulator's net description or topology file generally does this.

Intel has found wide variation in noise margins when varying the stub impedance and the PCB's Z_0 and S_0. Intel therefore recommends that PCB parameters are controlled as tightly as possible, with a sampling of the allowable Z_0 and S_0 simulated. The Pentium III processor nominal effective line Impedance is 65 Ω ± 10% and the effective line impedance (Z_{EFF}) is 60 Ω ±10%. Intel recommends the baseboard nominal effective line impedance to be at 60 Ω ± 10% for the recommended layout guidelines to be effective. Intel recommends running uncoupled simulations using the Z_0 of the package stubs; and performing fully coupled simulations if increased accuracy is needed or desired. Accounting for cross-talk within the device package by varying the stub impedance was investigated and was not found to be sufficiently accurate. This led to the development of full package models for the component packages.

A.1.2 Place and Route Board

A.1.2.1. Estimate Component to Component Spacing for AGTL+ Signals

- Estimate the number of layers that will be required
- Determine the expected interconnect distances between each of the components on the AGTL+ bus.
- Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

The required bus frequency and the maximum flight time propagation delay on the PCB determine the maximum network length between the bus agents. The minimum network length is independent of the required bus frequency. Table 3 assumes values for CLK_{SKEW} and CLK_{JITTER}; these are parameters that are controlled by the system designer. In order to reduce system clock skew to a minimum, clock buffers that allow their outputs to be tied together are recommended. Intel strongly recommends running analog simulations to ensure that each design has adequate noise and timing margin.

A.1.2.2. Layout and Route Board

Route the board satisfying the estimated space and timing requirements. Stay within the solution space set from the pre-layout sweeps. Estimate the printed circuit board parameters from the placement and other information including the following general guidelines:

- Distribute V_{TT} with a power plane or a partial power plane. If this cannot be accomplished, use as wide a trace as possible and route the V_{TT} trace with the same topology as the AGTL+ traces.
- Keep the overall length of the bus as short as possible (but don't forget minimum component-to-component distances to meet hold times).

- Plan to minimize cross-talk with the following guidelines developed for the example topology given (signal spacing recommendations were based on fully coupled simulations - spacing may be decreased based upon the amount of coupled length):
  - — Use a spacing to line width to dielectric thickness ratio of at least 3:1:2. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%.
  - — Minimize the dielectric process variation used in the PCB fabrication.
  - — Eliminate parallel traces between layers not separated by a power or ground plane.

Table A-1 contains the trace width:space ratios assumed for this topology. The cross-talk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intra-group AGTL+ cross-talk involves interference between AGTL+ signals within the same group (See section “AGTL+ Design Guideline” on page 6-4 for a description of the different AGTL+ group types). Intergroup AGTL+ cross-talk involves interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ cross-talk is when CMOS and AGTL+ signals interfere with each other.

Table A-1. Trace Width:Space Guidelines

Cross-talk Type	Trace Width:Space Ratio
Intragroup AGTL+ (same group AGTL+)	2:1
Intergroup AGTL+ (different group AGTL+)	3:1
AGTL+ to non-AGTL+	3:1

The spacing between the various bus agents causes variations in trunk impedance and stub locations. These variations cause reflections that can cause constructive or destructive interference at the receivers. A reduction of noise may be obtained by a minimum spacing between the agents. Unfortunately, tighter spacing results in reduced component placement options and lower hold margins. Adjusting the inter-agent spacing may be one way to change the network’s noise margin, but mechanical constraints often limit the usefulness of this technique. Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.

There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require more attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two or more agents on the same clock edge, the two falling edge wave fronts will meet at some point on the bus and can sum to form a negative voltage. The ringback from this negative voltage can easily cross into the overdrive region. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

This document addresses AGTL+ layout for 133/100 MHz processor/Intel® 840 Chipset systems. Power distribution and chassis requirements for cooling, connector location, memory location, etc., may constrain the system topology and component placement location, therefore constraining the board routing. These issues are not directly addressed in this document.

A.1.2.3. Host Clock Routing

Host clock nets should be routed as point-to-point connections through a series resistor placed as close to the output pins of the clock driver as possible. The value of the series resistor is dependent on the clock driver characteristic impedance. Therefore, the clock driver to the Intel 82840 (MCH) requires additional trace length of approximately 3.5” to compensate for the additional skew required to phase-align with the clock driver to the FC-PGA Pentium III processor. The required 3.5” assumes a 161 ps/in board (microstrip) velocity.

A.1.3 Post-Layout Simulation

Following layout, extract the interconnect information for the board from the CAD layout tools. Run simulations to verify that the layout meets timing and noise requirements. A small amount of tuning may be required; experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required. The post layout simulations should take into account the expected variation for all interconnect parameters.

Intel specifies signal integrity **at the device pads** and therefore recommends running simulations at the device pads for signal quality. However, Intel specifies core timings **at the device pins,** so simulation results at the device pins should be used later to correlate simulation performance against actual system measurements.

A.1.3.1. Intersymbol Interference

Intersymbol Interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

Intersymbol Interference (ISI) occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can occur when the line is driven high, low, and then high in consecutive cycles (the opposite case is also valid). When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum V_{OL} before the next rising edge is driven. This results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycle. ISI effects do not necessarily span only three cycles so it may be necessary to simulate beyond three cycles for certain designs. After simulating and quantifying ISI effects, adjust the timing budget accordingly to take these conditions into consideration.

A.1.3.2. Cross-talk Analysis

AGTL+ cross-talk simulations can consider the processor core package, Intel 840 MCH package, and FC-PGA socket as non-coupled. Simulate the traces as lossless for worst case cross-talk and lossy where more accuracy is needed. Evaluate both odd and even mode cross-talk conditions.

AGTL+ Cross-talk simulation involves the following cases:

- Intra-group AGTL+ cross-talk
- Inter-group AGTL+ cross-talk
- Non-AGTL+ to AGTL+ cross-talk

A.1.3.3. Monte Carlo Analysis

Perform a Monte Carlo analysis on the extracted baseboard. Vary all parameters recommended for the pre-layout Monte Carlo analysis within the region that they are expected to vary. The range for some parameters will be reduced compared to the pre-layout simulations. For example, baseboard lengths L1 through L7 should no longer vary across the full min and max range on the final baseboard design. Instead, baseboard lengths should now have an actual route, with a length tolerance specified by the baseboard fabrication manufacturer.

A.1.4 Validation

Build systems and validate the design and simulation assumptions.

A.1.4.1. Measurements

Note that the AGTL+ specification for signal quality is at the **pad** of the component. The expected method of determining the signal quality is to run analog simulations for the pin and the pad. Then correlate the simulations at the pin against actual system measurements at the pin. Good correlation at the pin leads to confidence that the simulation at the pad is accurate. Controlling the temperature and voltage to correspond to the I/O buffer model extremes should enhance the correlation between simulations and the actual system.

A.1.5 Timing Requirements

The system timing for AGTL+ is dependent on many things. Each of the following elements combine to determine the maximum and minimum frequency the AGTL+ bus can support:

- The range of timings for each of the agents in the system.
  - — Clock to output [T_{CO}]. (Note that the system load is likely to be different from the specification load. The T_{CO} observed in the system might not be the same as the T_{CO} from the specification.)
- The minimum required setup time to clock [$T_{SU–MIN}$] for each receiving agent.
- The range of flight time between each component. This includes:
  - — The velocity of propagation for the loaded printed circuit board [S_{EFF}].
  - — The board loading impact on the effective T_{CO} in the system.
- The amount of skew and jitter in the system clock generation and distribution.
- Changes in flight time due to cross-talk, noise, and other effects.

A.1.5.1. Flight Time Simulation

As defined earlier, flight time is the time difference between a signal crossing V_{REF} at the input pin of the receiver, and the output pin of the driver crossing V_{REF} were it driving a **test load**. The timings in the tables and topologies discussed in this guideline assume the actual system load is 50 Ω and is **equal to the test load**. While the DC loading of the AGTL+ bus in a DP mode is closer to 25 Ω, AC loading is approximately 32 Ω since the driver effectively “sees” a 70 Ω termination resistor in parallel with a 60 Ω transmission line on the package.

Figure A-1. Test Load vs. Actual System Load

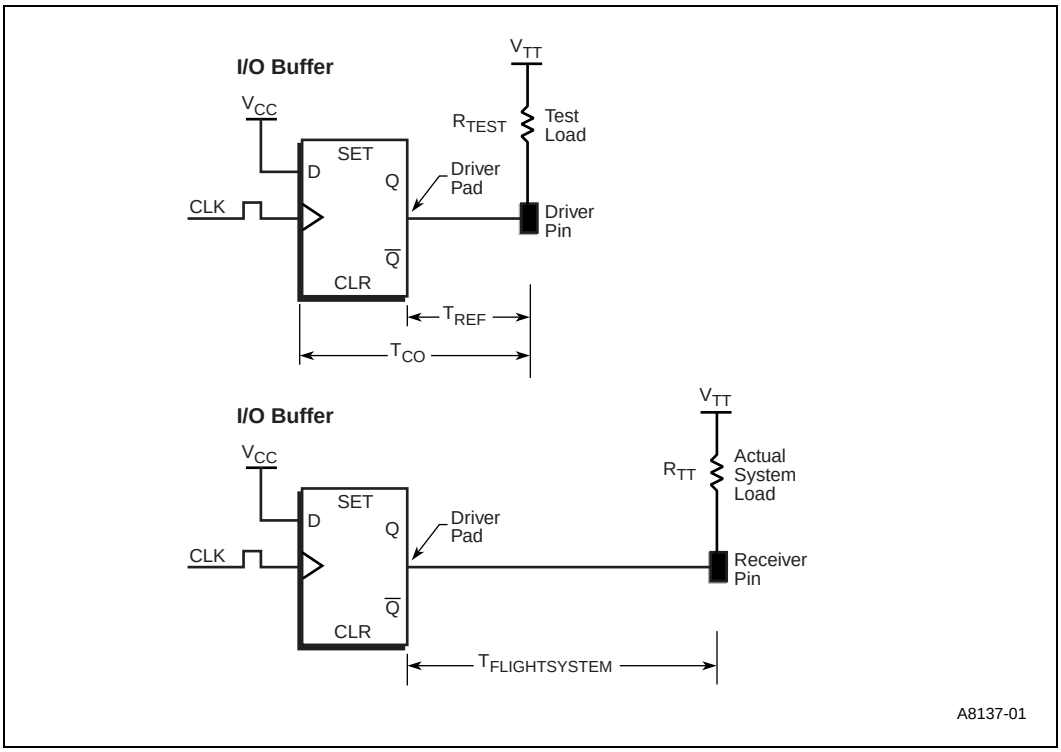


Figure A-1 shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical AGTL+ I/O buffer. T_{CO} timings are specified at the driver pin output. $T_{FLIGHT-SYSTEM}$ is usually reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver's input pin sees a valid data input. Since both timing numbers (T_{CO} and $T_{FLIGHT-SYSTEM}$) will include propagation time from the pad to the pin, it is necessary to subtract this time (T_{REF}) from the reported flight time to avoid double counting. T_{REF} is defined as the time that it takes for the driver output pin to reach the measurement voltage, V_{REF}, starting from the beginning of the driver transition at the pad. T_{REF} must be generated using the same test load for T_{CO}. Intel provides this timing value in the AGTL+ I/O buffer models.

In this manner, the following valid delay equation is satisfied:

Equation A-1. Valid Delay Equation

$$\text{Valid Delay} = T_{CO} + T_{FLIGHT-SYS} - T_{REF} = T_{CO-MEASURED} + T_{FLIGHT-MEASURED}$$

This valid delay equation is the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

A.1.5.2. Flight Time Hardware Validation

When a measurement is made on the actual system, T_{CO} and flight time do not need T_{REF} correction since these are the actual numbers. These measurements include all of the effects pertaining to the driver-system interface and the same is true for the T_{CO}. The addition of the measured T_{CO} and the measured flight time must be equal to the valid delay calculated above.

A.2 Theory

A.2.1 AGTL+

AGTL+ is the electrical bus technology used for the processor bus. This is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each load. The processor AGTL+ drivers contain a full-cycle active pull-up device to improve system timings. The AGTL+ specification defines:

- Termination voltage (V_{TT})
- Receiver reference voltage (V_{REF}) as a function of termination voltage (V_{TT})
- Processor termination resistance (R_{TT})
- Input low voltage (V_{IL})
- Input high voltage (V_{IH})
- NMOS on resistance (R_{ONN})
- PMOS on resistance (R_{ONP})
- Edge rate specifications
- Ringback specifications
- Overshoot/Undershoot specifications
- Settling Limit

A.2.2 Cross-Talk Theory

AGTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies that have traditionally been used in personal computer designs. This requires that designers using AGTL+ be more aware of cross-talk than they may have been in past designs.

Cross-talk is caused through capacitive and inductive coupling between networks. Cross-talk appears as both backward cross-talk and as forward cross-talk. Backward cross-talk creates an induced signal on a victim network that propagates in a direction opposite that of the aggressor's signal. Forward cross-talk creates a signal that propagates in the same direction as the aggressor's signal. On the AGTL+ bus, a driver on the aggressor network is not at the end of the network; therefore it sends signals in both directions on the aggressor's network. Figure A-2 shows a driver on the aggressor network and a receiver on the victim network that are not at the ends of the network. The signal propagating in each direction causes cross-talk on the victim network.

Figure A-2. Aggressor and Victim Networks

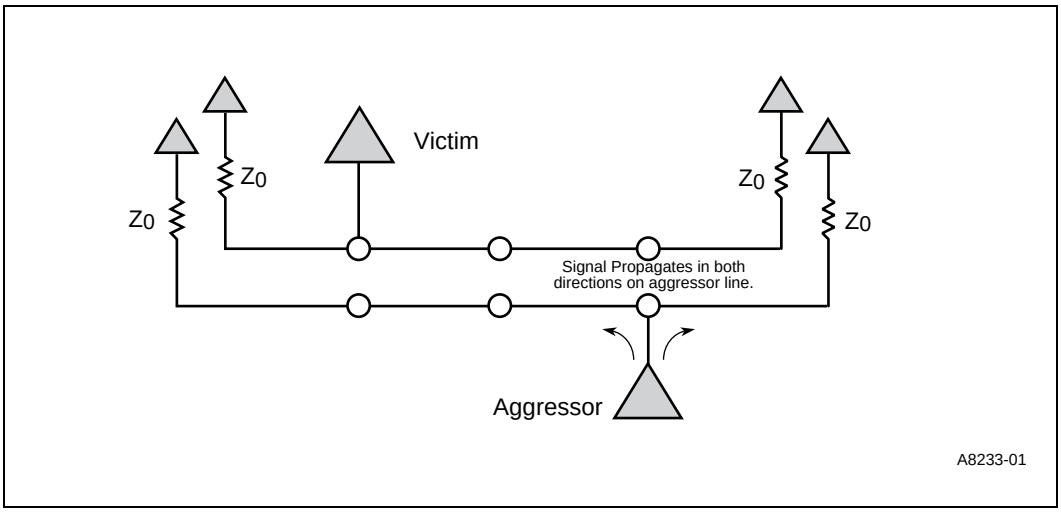
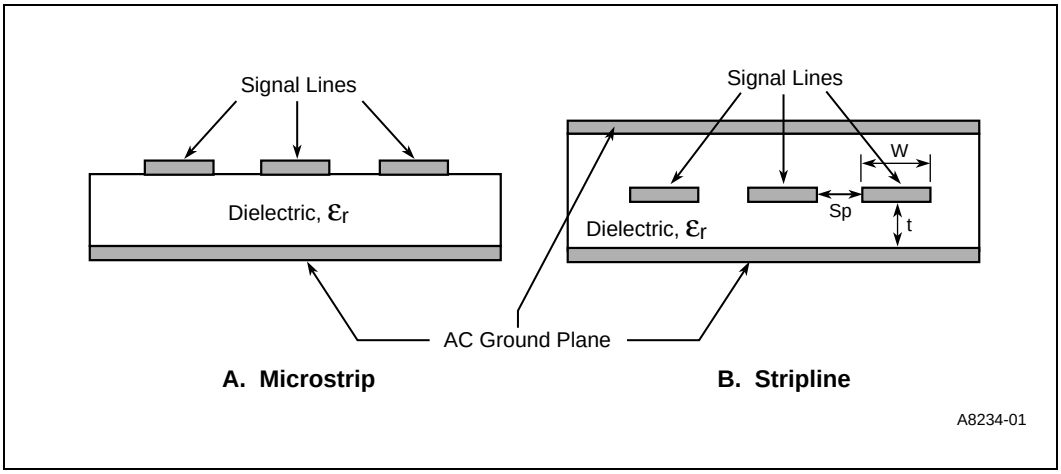


Figure A-3. Transmission Line Geometry: (A) Microstrip (B) Stripline



Additional aggressors are possible in the z-direction, if adjacent signal layers are not routed in mutually perpendicular directions. Because cross-talk-coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. The maximum cross-talk occurs when all the aggressors are switching in the same direction at the same time.

There is cross-talk internal to the IC packages, which can also affect the signal quality.

Backward cross-talk is present in both stripline and microstrip geometries (see Figure A-3). A way to remember which geometry is stripline and which is microstrip is that a stripline geometry requires stripping a layer away to see the signal lines. The backward coupled amplitude is proportional to the backward cross-talk coefficient, the aggressor's signal amplitude, and the coupled length of the network up to a maximum that is dependent on the rise/fall time of the aggressor's signal. Backward cross-talk reaches a maximum (and remains constant) when the

propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing, and the fall time on an unloaded coupled network, then:

$$Length\ for\ Max\ Backward\ Crosstalk = \frac{\frac{1}{2} \times Fall\ Time}{Board\ Delay\ Per\ Unit\ Length}$$

An example calculation if the fast corner fall time is 3 V/ns and board delay is 175 ps/inch (2.1 ns/foot) follows:

Fall time = 1.5 V/3 V/ns = 0.5 ns

Length for Max Backward Cross-talk

= ½ * 0.5 ns * 1000 ps/ns /175 ps/in

= 1.43 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This will cause backward cross-talk from segments on two sides of a driver. The pulses from the backward cross-talk travel toward each other and will meet and add at certain moments and positions on the bus. This can cause the voltage (noise) from cross-talk to double.

A.2.2.1. Potential Termination Cross-talk Problems

The use of commonly used pull-up resistor networks for AGTL+ termination may not be suitable. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks with separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

A.3 More Details and Insights

A.3.1 Textbook Timing Equations

The textbook equations used to calculate the propagation rate of a PCB are the basis for spreadsheet calculations for timing margin based on the component parameters. These equations are:

Equation A-2. Intrinsic Impedance

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (\Omega)$$

Equation A-3. Stripline Intrinsic Propagation Speed

$$S_{0\_STRIPLINE} = 1.017 * \sqrt{\varepsilon_r} \quad (\text{ns/ft})$$

Equation A-4. Microstrip Intrinsic Propagation Speed

$$S_{0\_MICROSTRIP} = 1.017 * \sqrt{0.475 * \varepsilon_r + 0.67} \quad (\text{ns/ft})$$

Equation A-5. Effective Propagation Speed

$$S_{EFF} = S_0 * \sqrt{1 + \frac{C_D}{C_0}} \quad (\text{ns/ft})$$

Equation A-6. Effective Impedance

$$Z_{EFF} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}} \quad (\Omega)$$

Equation A-7. Distributed Trace Capacitance

$$C_0 = \frac{S_0}{Z_0} \quad (\text{pF/ft})$$

Equation A-8. Distributed Trace Inductance

$$L_0 = 12 * Z_0 * S_0 \quad (\text{nH/ft})$$

Symbols for Equation A-2 through Equation A-8 are:

- S_0 is the speed of the signal on an unloaded PCB in ns/ft. This is referred to as the board propagation constant.
- $S_{0\_MICROSTRIP}$ and $S_{0\_STRIPLINE}$ refer to the speed of the signal on an unloaded microstrip or stripline trace on the PCB in ns/ft.
- Z_0 is the intrinsic impedance of the line in Ω and is a function of the dielectric constant (ε_r), the line width, line height and line space from the plane(s). The equations for Z_0 are not included in this document. See the *MECL System Design Handbook* by William R. Blood, Jr. for these equations.
- C_0 is the distributed trace capacitance of the network in pF/ft.
- L_0 is the distributed trace inductance of the network in nH/ft.
- C_D is the sum of the capacitance of all devices and stubs divided by the length of the network's trunk, not including the portion connecting the end agents to the termination resistors in pF/ft.
- S_{EFF} and Z_{EFF} are the effective propagation constant and impedance of the PCB when the board is loaded with the components.

A.3.2 Effective Impedance and Tolerance/Variation

The impedance of the PCB needs to be controlled when the PCB is fabricated. The method of specifying control of the impedance needs to be determined to best suit each situation. Using stripline transmission lines (where the trace is between two reference planes) is likely to give better results than microstrip (where the trace is on an external layer using an adjacent plane for reference with solder mask and air on the other side of the trace). This is in part due to the difficulty of precise control of the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase cross-talk.

The effective line impedance (Z_{EFF}) is recommended to be 60 Ω ±10%, where Z_{EFF} is defined by Equation 6.

A.3.3 Clock Routing

Analog simulations are required to ensure clock net signal quality and skew is acceptable. The system clock skew must be kept to a minimum (The calculations and simulations for the example topology given in this document have a total clock skew of 200 ps and 150 ps of clock jitter). For a given design, the clock distribution system, including the clock components, must be evaluated to ensure these same values are valid assumptions. Each processor's Electrical, Mechanical, and Thermal Specification specifies the clock signal quality requirements. To help meet these specifications, follow these general guidelines:

- Tie clock driver outputs if clock buffer supports this mode of operation.
- Match the electrical length and type of traces on the PCB (microstrip and stripline may have different propagation velocities).
- Maintain consistent impedance for the clock traces.
  - — Minimize the number of vias in each trace.
  - — Minimize the number of different trace layers used to route the clocks.
  - — Keep other traces away from clock traces.

- Lump the loads at the end of the trace if multiple components are to be supported by a single clock output.
- Have equal loads at the end of each network.

The **ideal** way to route each clock trace is on the same single inner layer, next to a ground plane, isolated from other traces, with the same total trace length, to the same type of single load, with an equal length ground trace parallel to it, and driven by a zero skew clock driver. When deviations from ideal are required, going from a single layer to a pair of layers adjacent to power/ground planes would be a good compromise. The fewer number of layers the clocks are routed on, the smaller the impedance difference between each trace is likely to be. Maintaining an equal length and parallel ground trace for the total length of each clock ensures a low inductance ground return and produces the minimum current path loop area. (The parallel ground trace will have lower inductance than the ground plane because of the mutual inductance of the current in the clock trace.)

A.4 Conclusion

AGTL+ routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will provide the designer with the best chance of avoiding the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.

Schematics B

The schematics on the following pages provide a reference design for a board using the FC-PGA Intel® Pentium® III processor with the Intel 840 chipset in a dual processor design.

Intel (R) Pentium (R) III Processor / 840 Development Board Schematics

REV B
2000

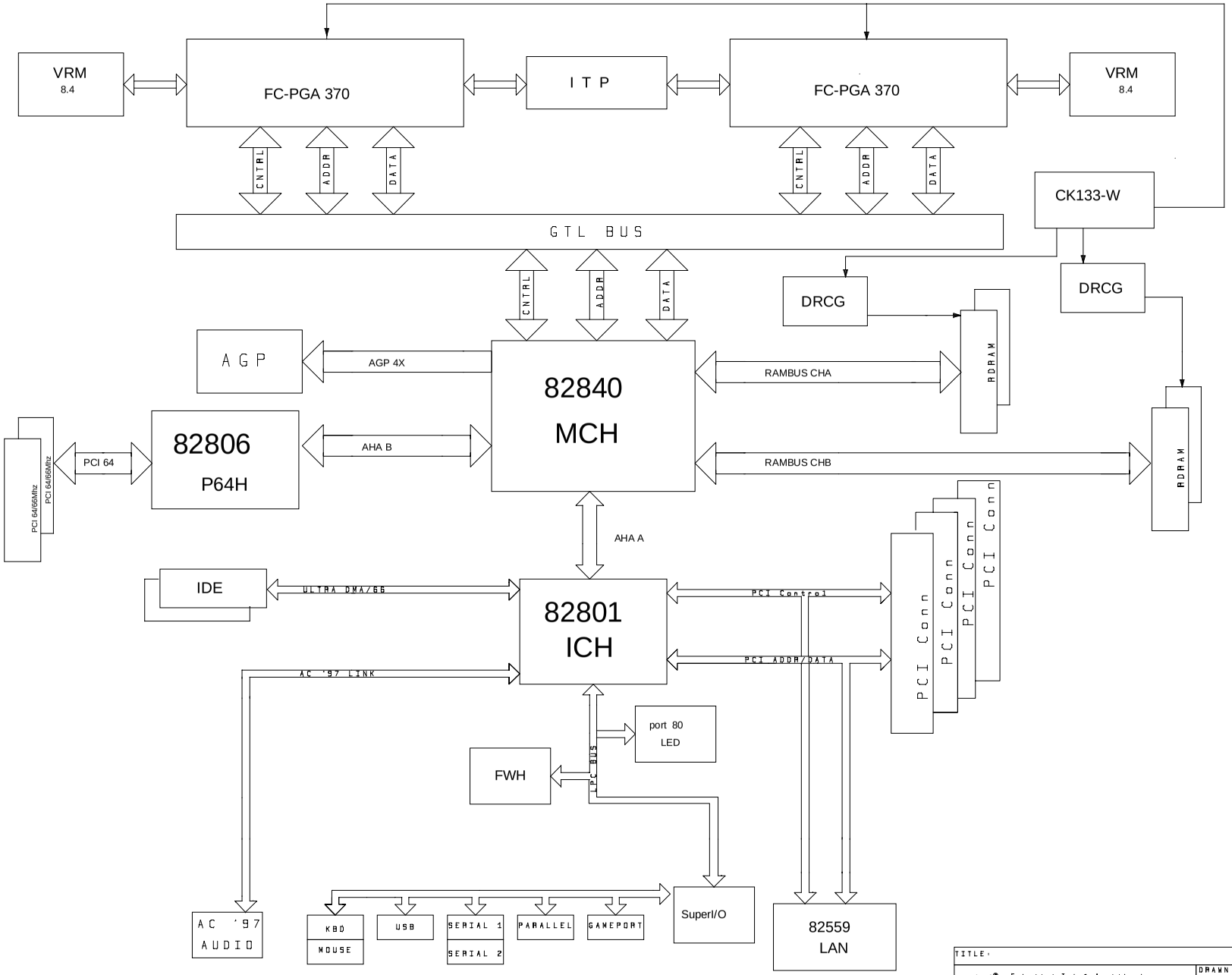
Contents

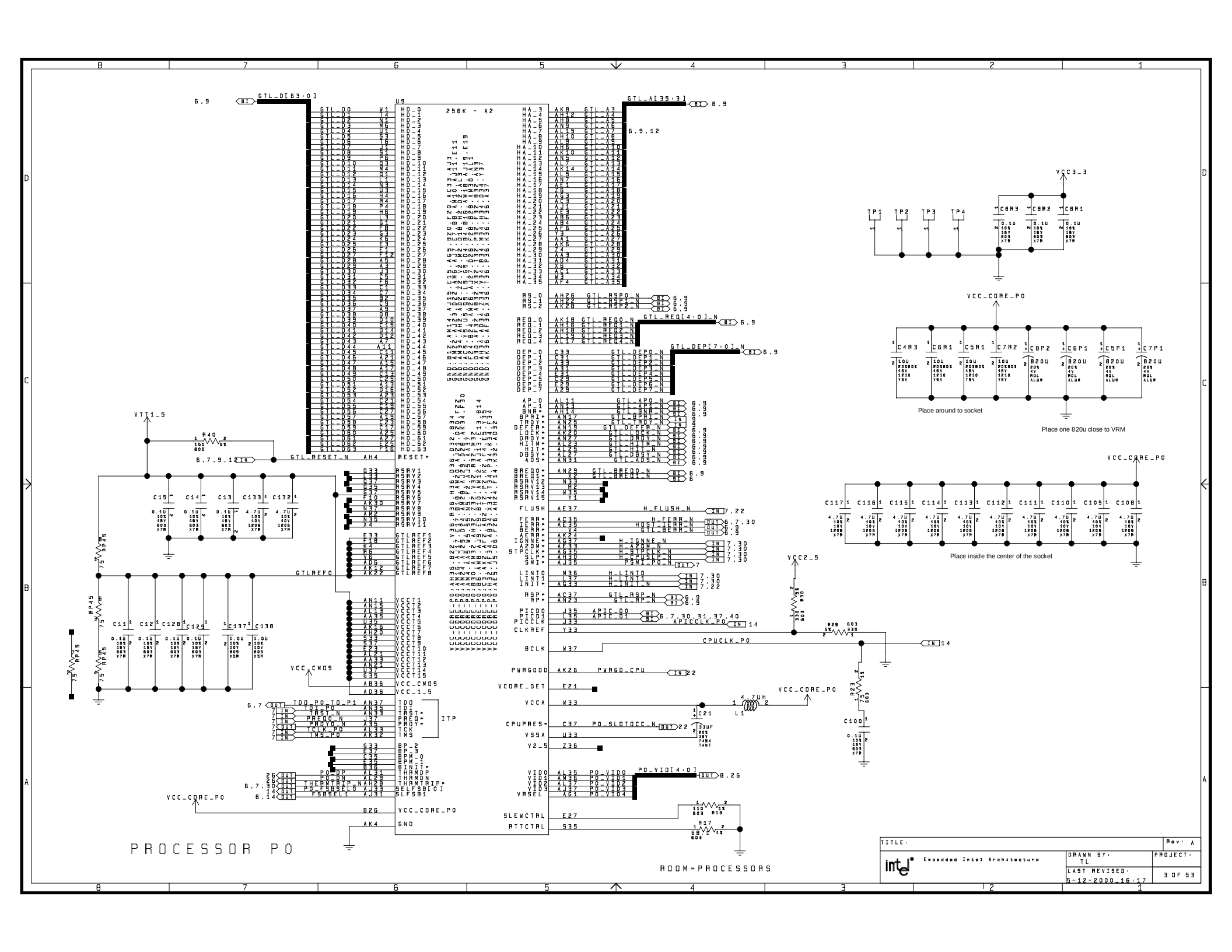
Revision History

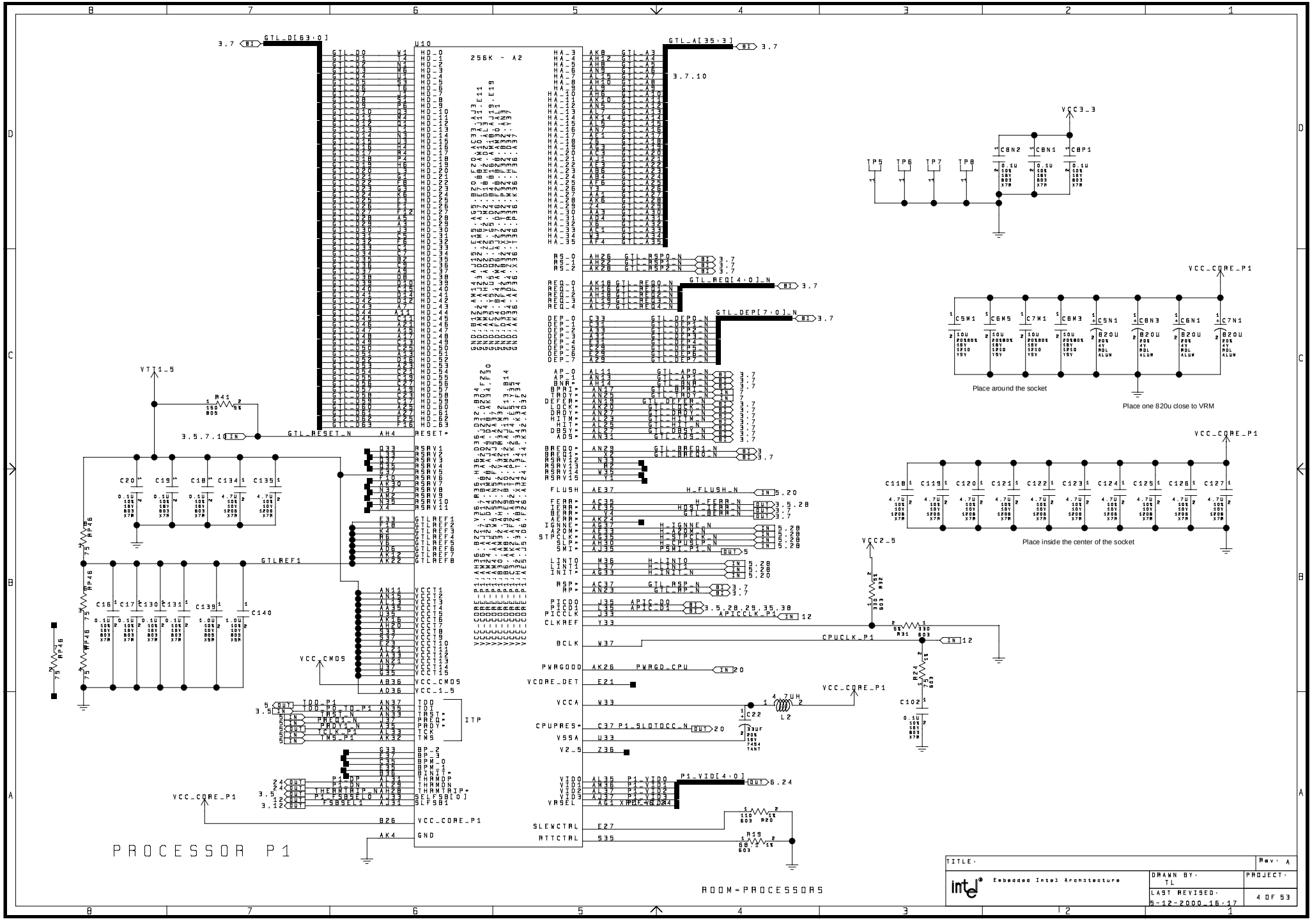
Rev A - Initial release
Rev B - Change ITP to work with American Arium
Change PSB ECC enable

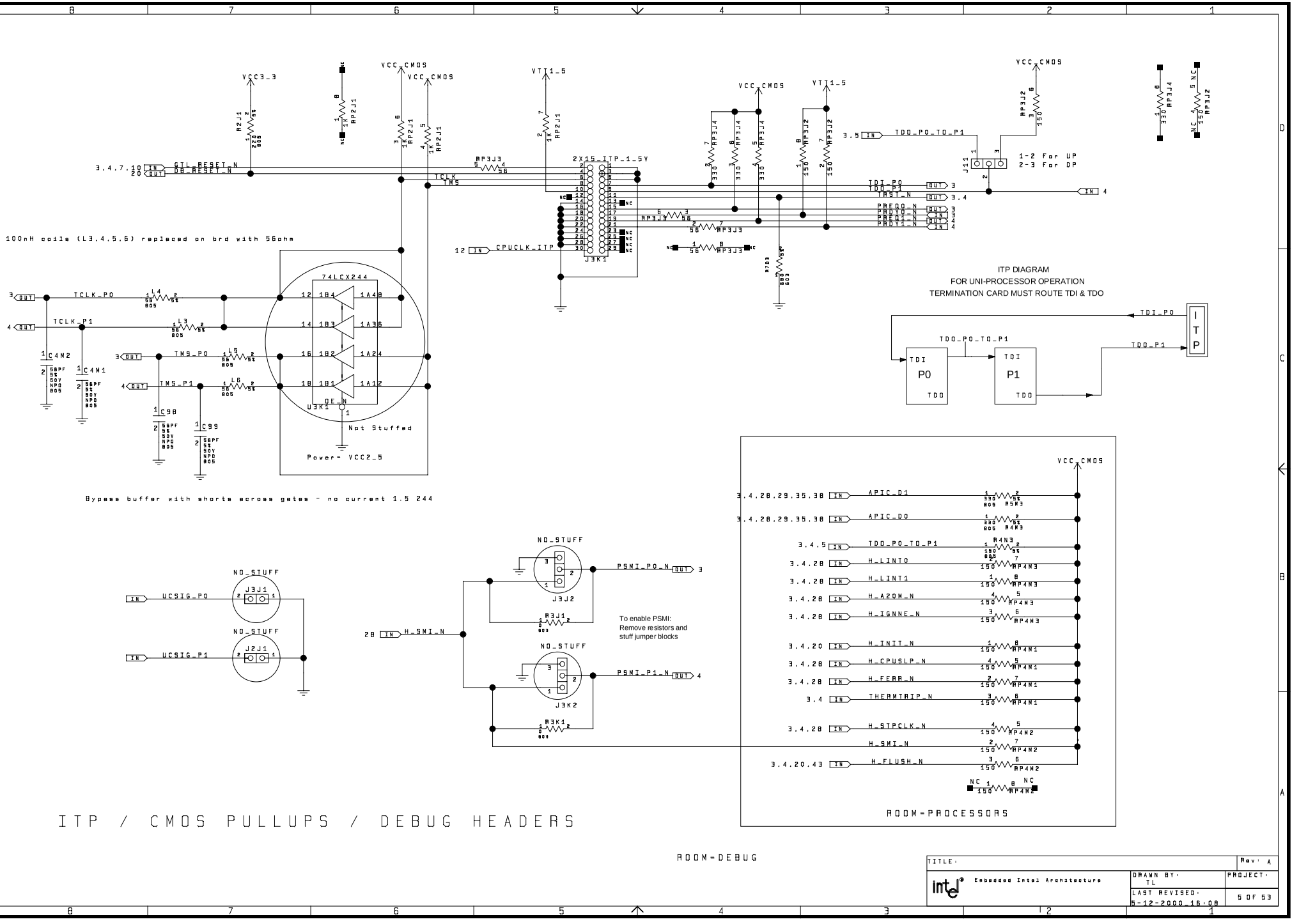
GTLREFA = 2/3 * 1.5V = 1.125V
GTLREFB = 2/3 * 1.5V = 1.125V
HUBREF_ICH= 1/2 * 1.8V = 0.9V
HUBREF_MCH= 1/2 * 1.8V = 0.9V
HUBREF_P64H= 2/3 * 1.8V = 1.35V
CHA_R_VREF= 0.777* 1.8V = 1.4V
CHB_R_VREF=0.777 * 1.8V = 1.4V

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 4-13-2000_11:59	1 OF 53


VRM
8.4
FC-PGA 370
I T P
FC-PGA 370
VRM
8.4
CNTRL
ADDR
DATA
CNTRL
ADDR
DATA
CK133-W
GTL BUS
CNTRL
ADDR
DATA
DRCG
DRCG
RDRAM
A G P
AGP 4X
82840
MCH
RAMBUS CHA
RDRAM
PCI 64/66Mhz
PCI 64/66Mhz
PCI 64
82806
P64H
AHA B
RAMBUS CHB
AHA A
IDE
ULTRA DMA/66
82801
ICH
PCI Control
PCI ADDR/DATA
PCI Conn
PCI Conn
PCI Conn
PCI Conn
AC '97 LINK
port 80
LED
FWH
LPC BUS
AC '97
AUDIO
KBD
MOUSE
USB
SERIAL 1
SERIAL 2
PARALLEL
GAMEPORT
SuperI/O
82559
LAN
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
5-12-2000_16:04
2 OF 53

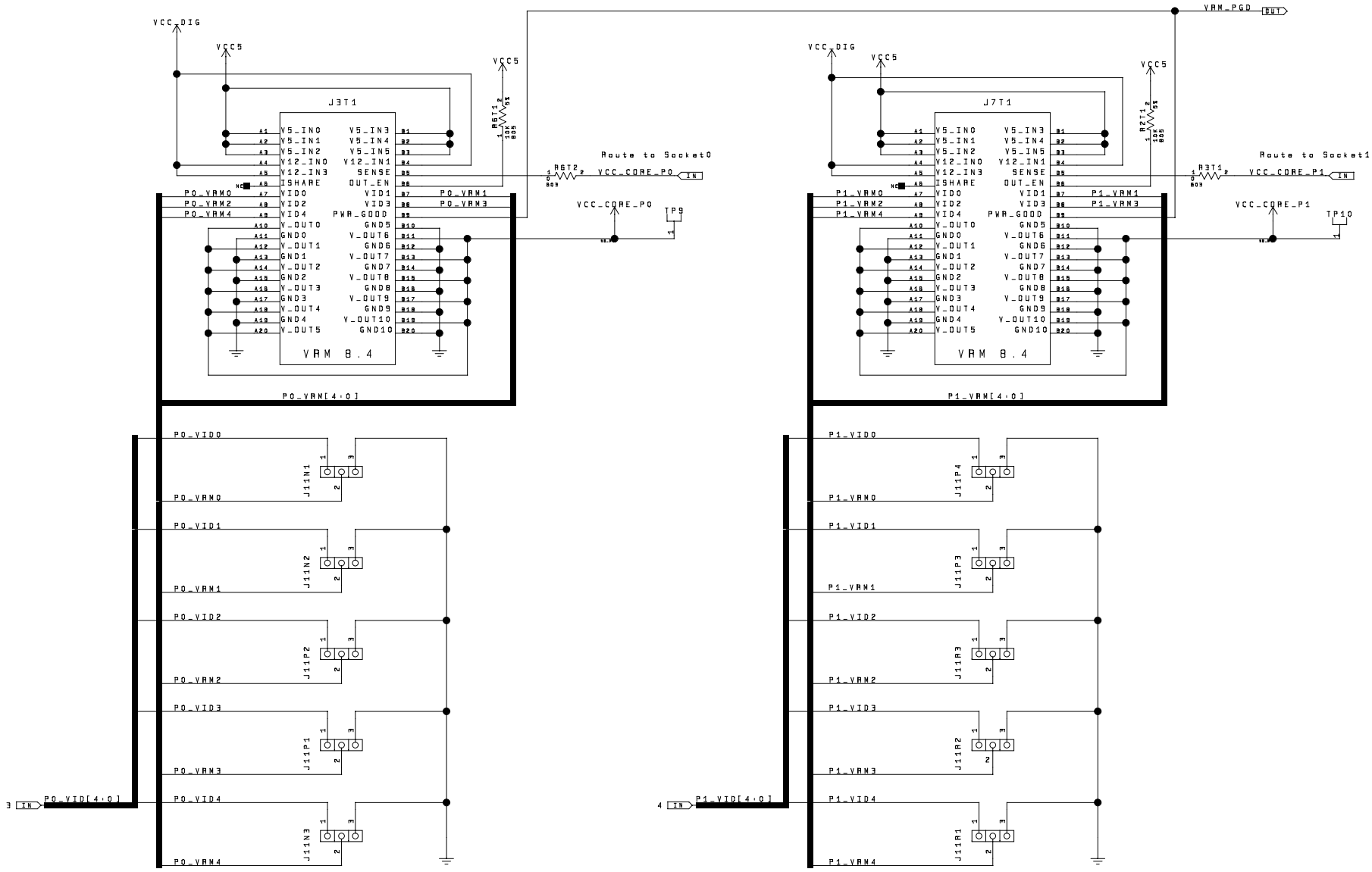

PROCESSOR PO
ROOM-PROCESSORS
Place around to socket
Place one 820u close to VRM
Place inside the center of the socket
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000 16:17
3 OF 53


PROCESSOR P1
ROOM=PROCESSORS
Place around the socket
Place one 820u close to VRM
Place inside the center of the socket
TITLE:
Rev: A
intel Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000_16:17
4 OF 53



ITP / CMOS PULLUPS / DEBUG HEADERS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	5 OF 53



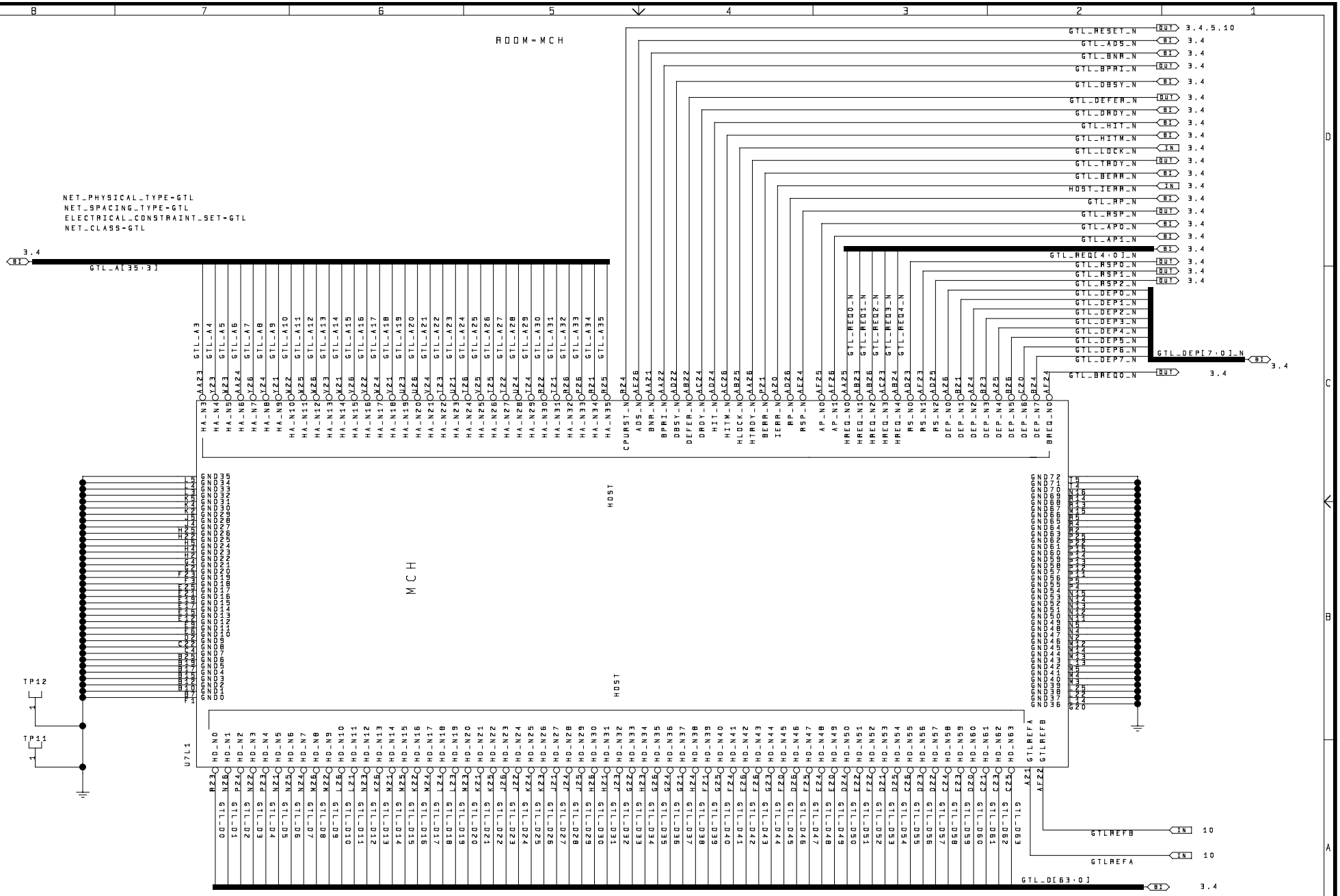
VID4 Must be grounded for production FC_PGA

Jumper position	1-2	2-3	No jumper
VRM VID[4:0]	CPU VID[4:0]	0	1

VRM HEADERS FOR PROCESSOR SOCKETS

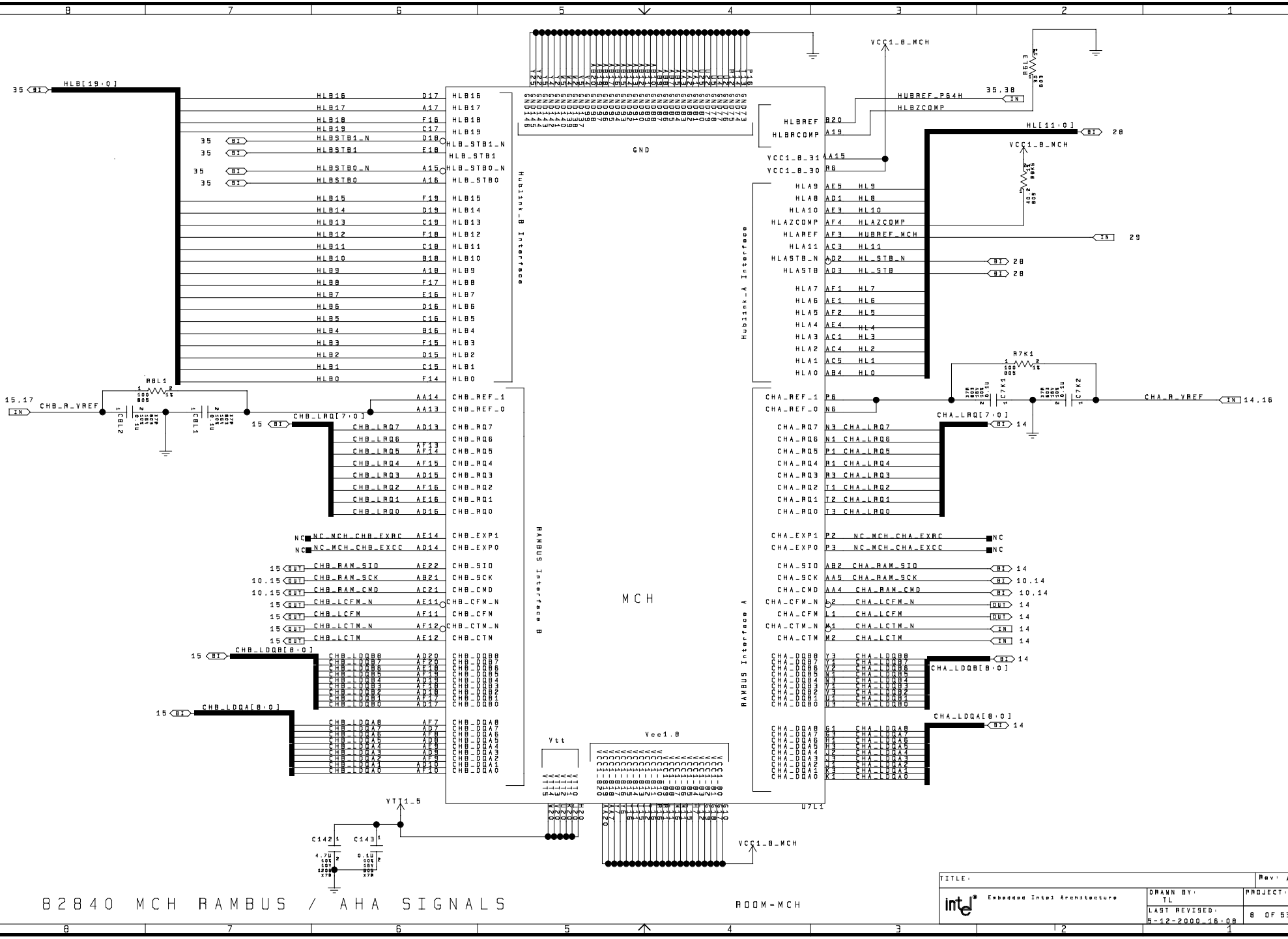
ROOM=VRM

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	6 OF 53



82840 MCH PSB SIGNALS

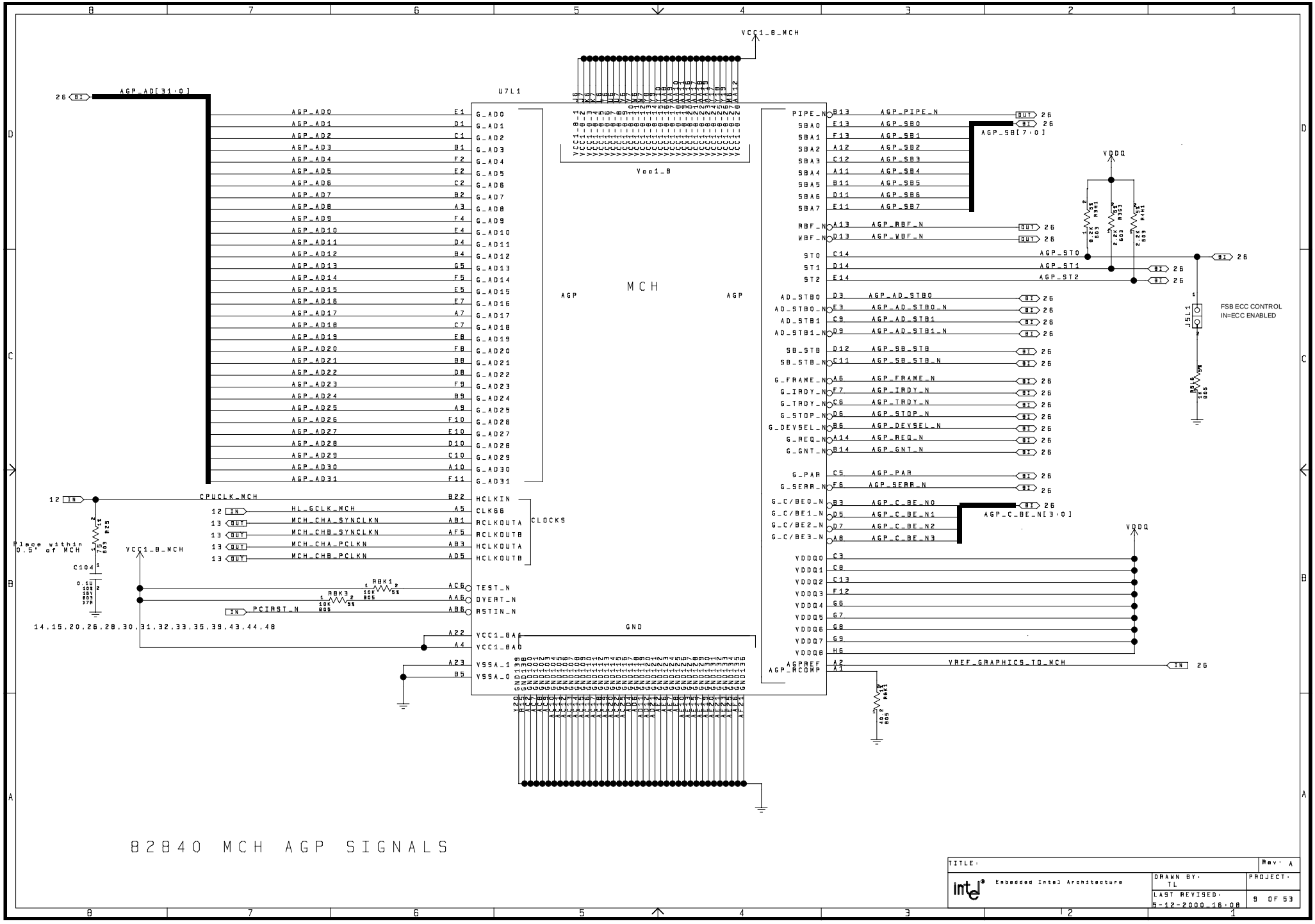
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:08
	7 OF 53

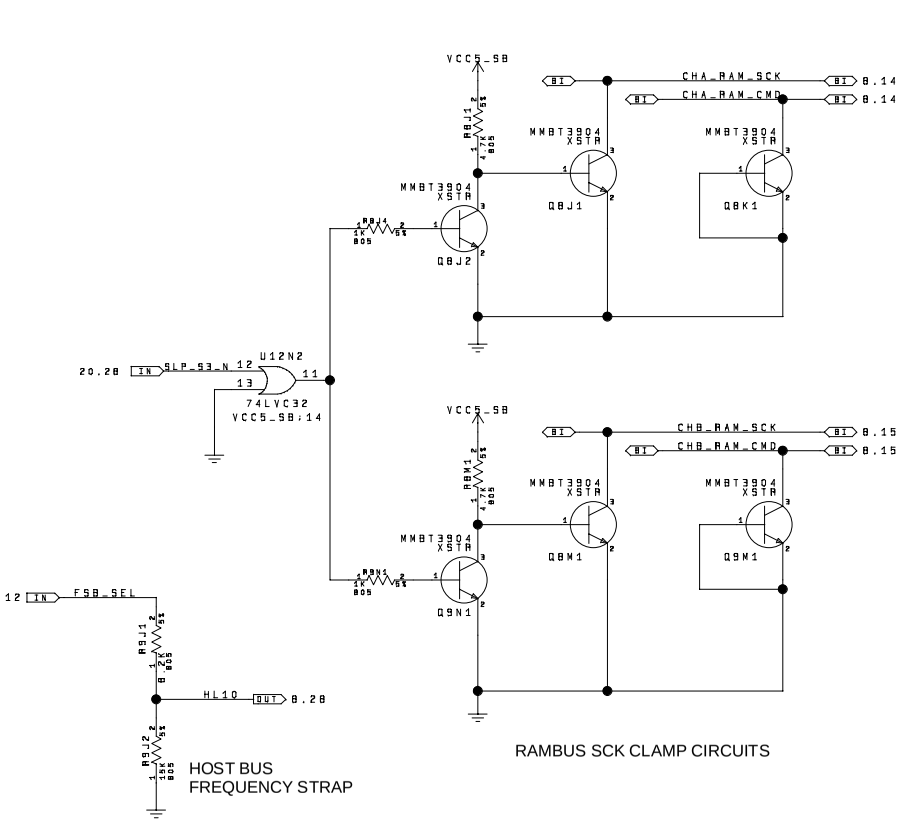


82840 MCH RAMBUS / AHA SIGNALS

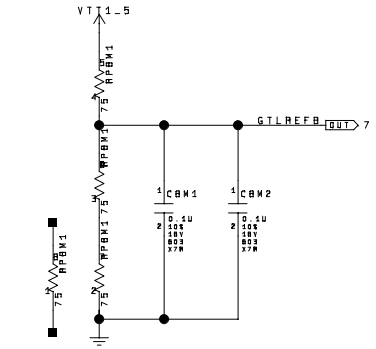
ROOM=MCH

TITLE:	Rev: A
intel Embedded Intel Architecture	PROJECT:
DRAWN BY: TL	
LAST REVISED: 5-12-2000_16:08	8 OF 53


VCC1_8_MCH
U7L1
MCH
AGP
AGP_AD[31:0]
AGP_SB[7:0]
CPUCLK_MCH
HL_GCLK_MCH
MCH_CHA_SYNCLKN
MCH_CHB_SYNCLKN
MCH_CHA_PCLKN
MCH_CHB_PCLKN
CLOCKS
PCIRST_N
GND
VDDQ
AGP_ST0
AGP_ST1
AGP_ST2
AGP_C_BE_N[3:0]
VREF_GRAPHICS_TO_MCH
FSB ECC CONTROL
IN=ECC ENABLED
Place within 0.5" of MCH
14.15.20.26.28.30.31.32.33.35.39.43.44.48
82840 MCH AGP SIGNALS
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000_16:08
9 OF 53

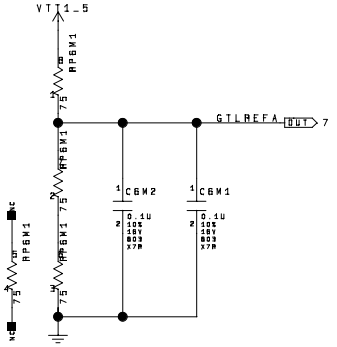


RAMBUS SCK CLAMP CIRCUITS



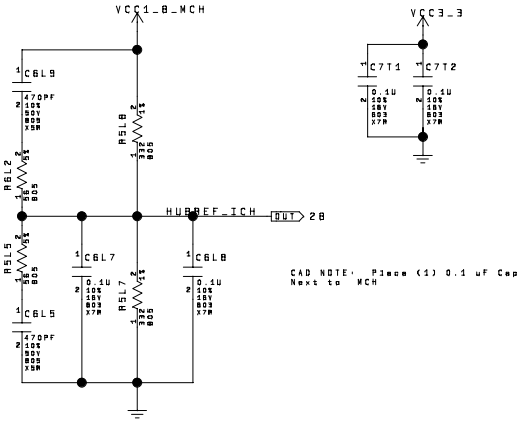
MCH GTLREFB GENERATION

Place close to MCH



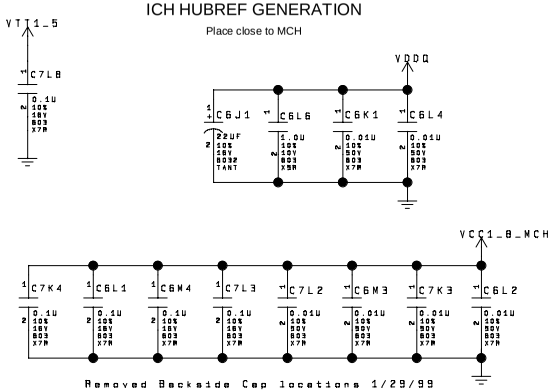
MCH GTLREFA GENERATION

Place close to MCH



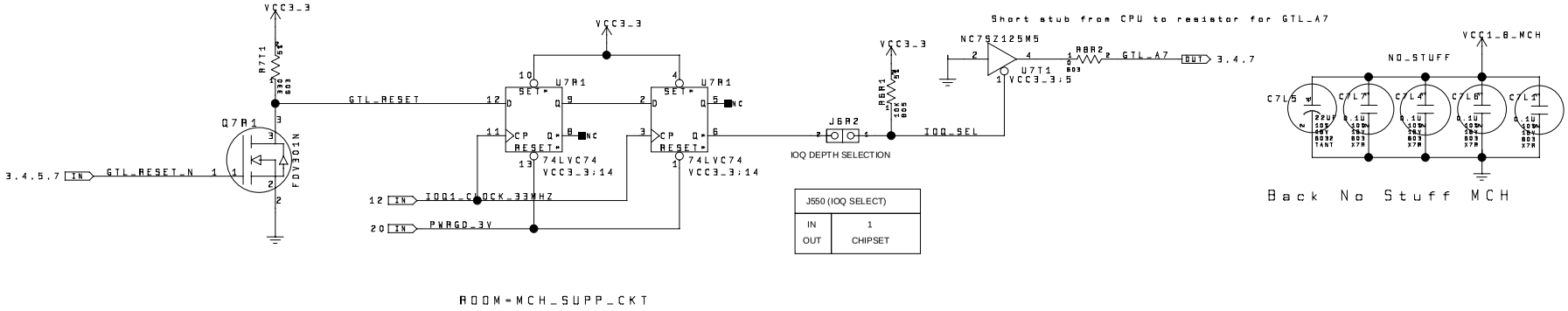
ICH HUBREF GENERATION

Place close to MCH



MCH DECOUPLING

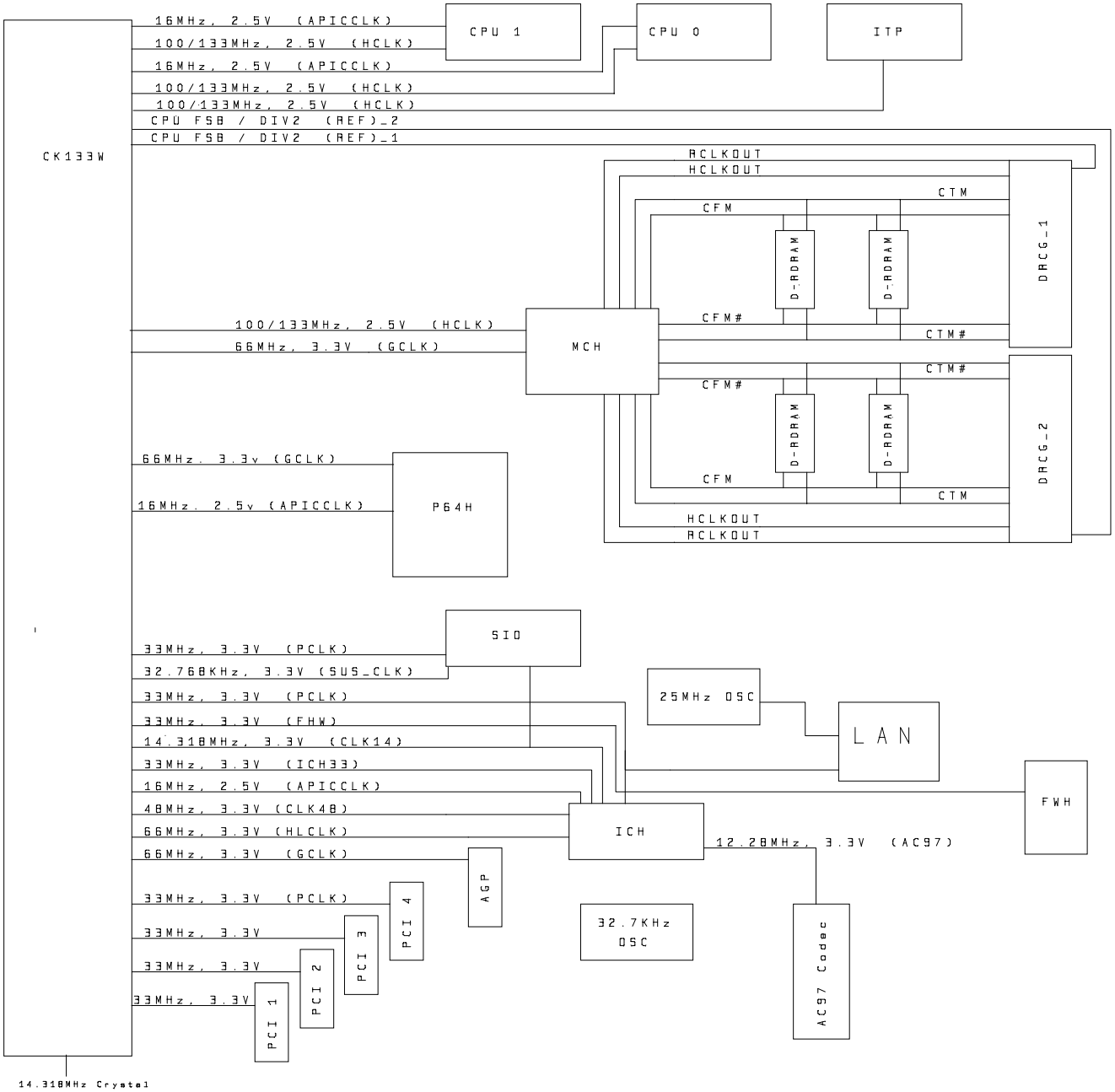
ROOM=MCH



ROOM=MCH_SUPP_CKT

82840 MCH DECOUPLING AND SUPPORT CIRCUITRY

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:08
	10 OF 53



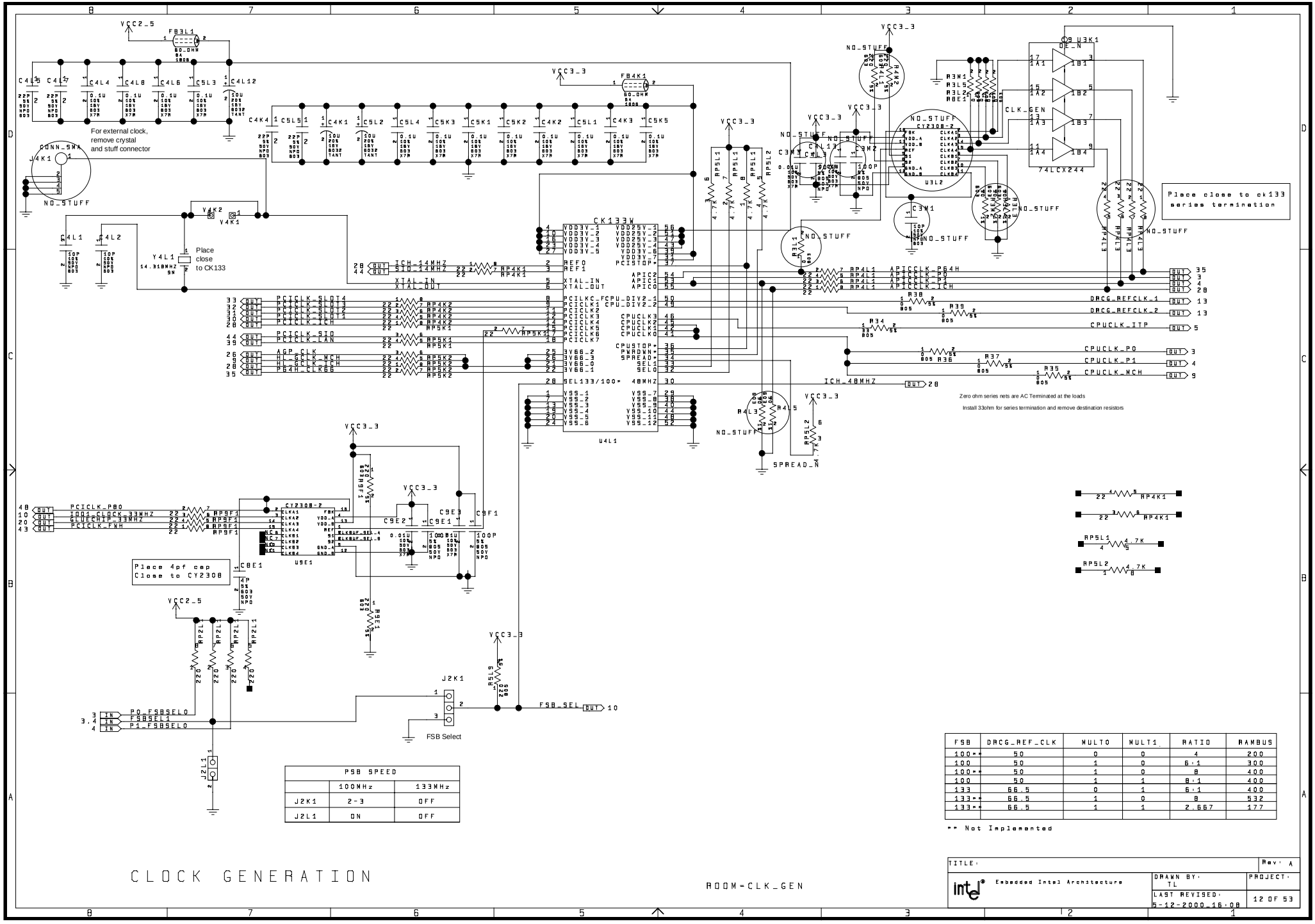
CLOCK DISTRIBUTION

5-12-2000_16:07

NOTES:

HCLK: 100/133MHz Processor & MCH FSB
GCLK: 66MHz, AGP, AHA, P64H
CTM/CFM: 300/400MHz, RDRAM-D, MCH RAC
APICCLK: 16.67MHz, APIC BUS
PCLK: 33MHz, PCI Bus & LPC Bus
CLK48: 48MHz, USB & SIO
CLK14: 14.318MHz, 8254 Timers
RTC: 32.768MHz, ICH
OSC: 14.318, ICH (ACPI Timer)
AC97: 12.288MHz, AC97 Audio Codec
ICH33: 33MHz, ICH (Free Running PCI)

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:07	11 OF 53

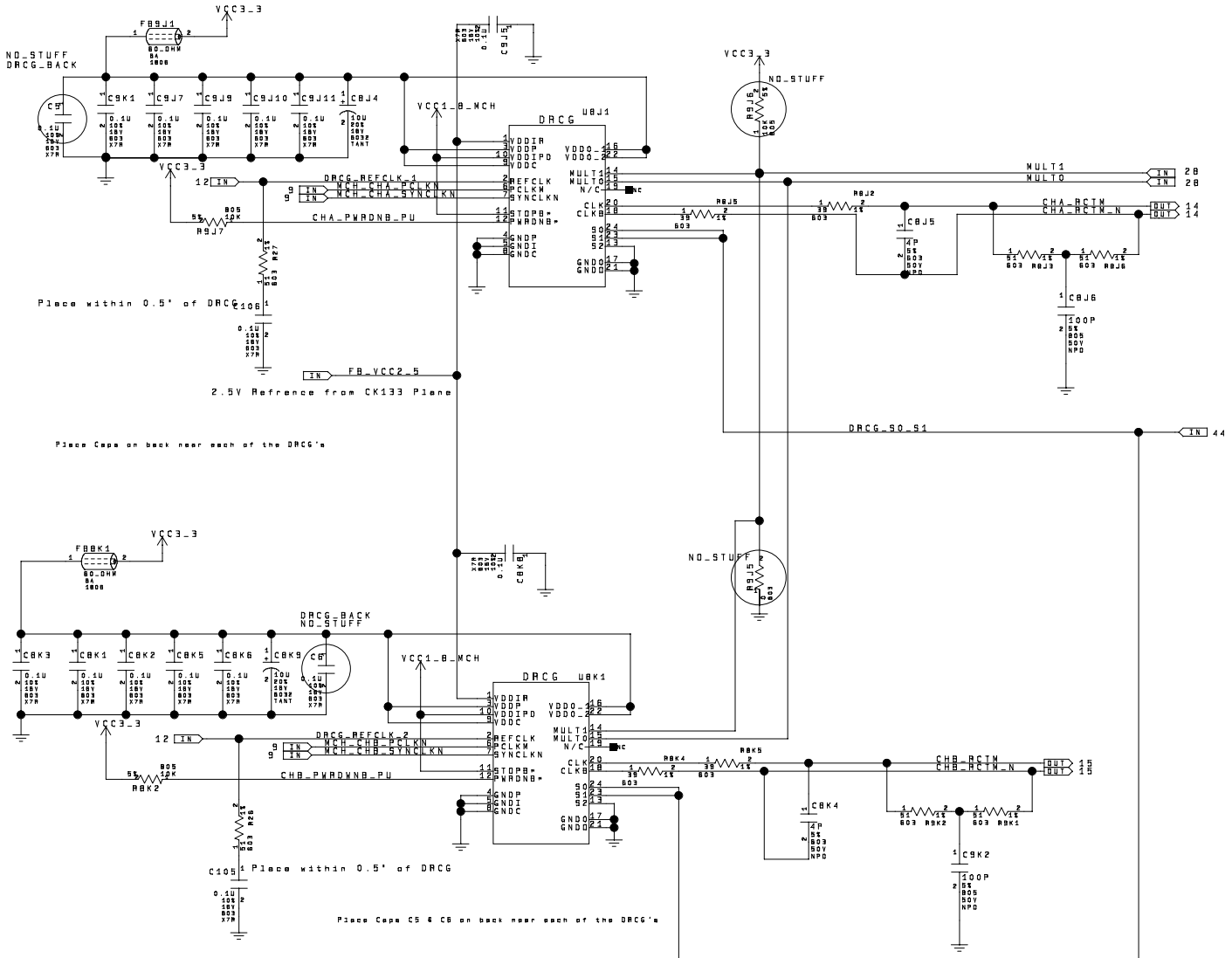


PSB SPEED		
	100MHz	133MHz
J2K1	2-3	OFF
J2L1	ON	OFF

FSB	DRCG_REF_CLK	MULT0	MULT1	RATIO	RAMBUS
100**	50	0	0	4	200
100	50	1	0	6:1	300
100**	50	1	0	8	400
100	50	1	1	8:1	400
133	66.5	0	1	6:1	400
133**	66.5	1	0	8	532
133**	66.5	1	1	2.667	177

** Not Implemented

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	12 OF 53



RAMBUS FREQUENCY SELECTION

FSB	DRCG_REF_CLK	MULT0	MULT1	RATIO	RAMBUS
100**	50	0	0	4	200
100	50	0	1	6	300
100**	50	1	0	8	400
100	50	1	1	8:1	400
133	66.5	0	1	6	400
133**	66.5	1	0	8	532
133**	66.5	1	1	2.667	177

** Not Implemented

RAMBUS DRCG MODE CONTROL

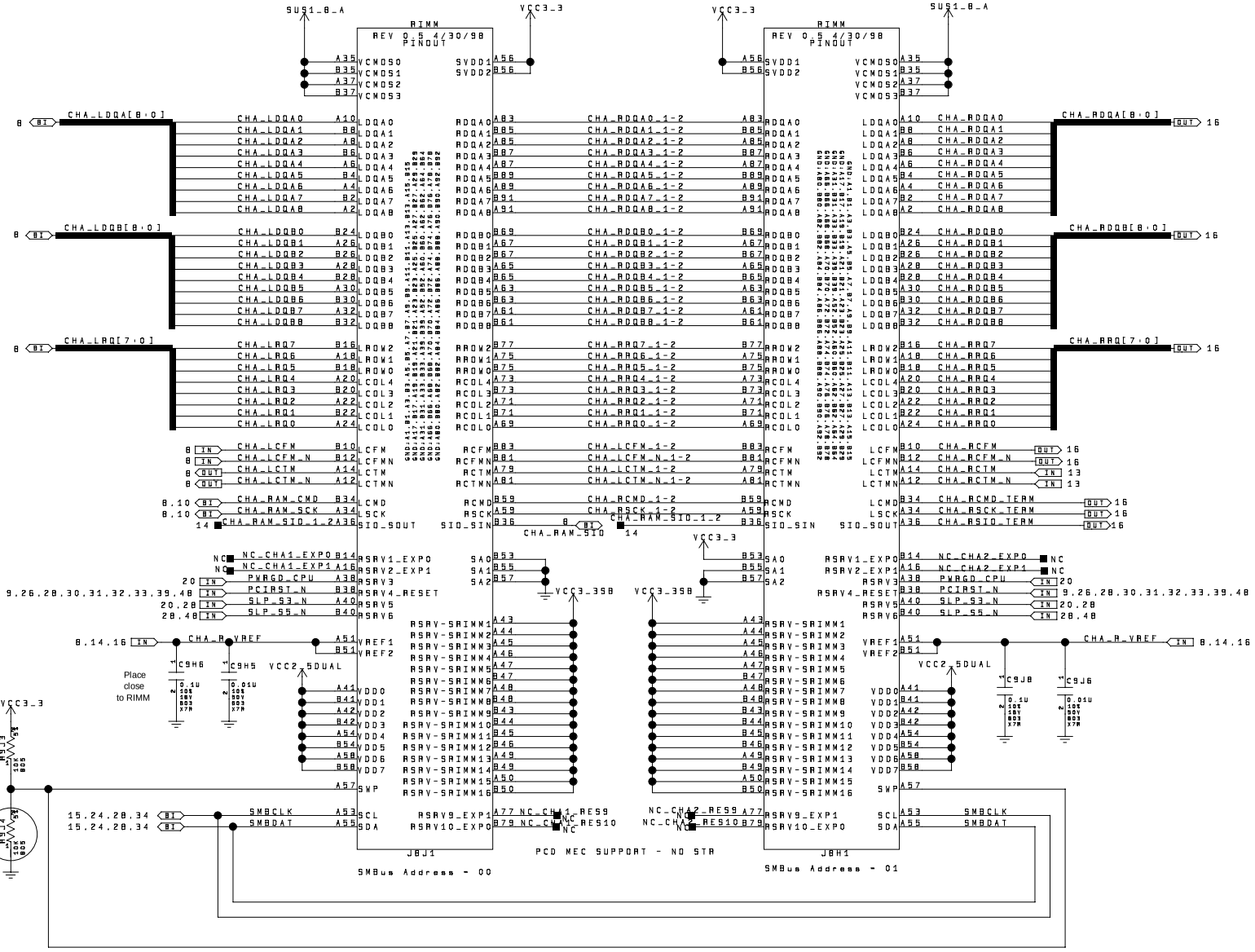
S0	S1	MODE
0	0	Normal
0	1	Output Enable Test
1	0	Bypass
1	1	Test

In Test Mode, Refclk is passed to the outputs

DRCG

ROOM=DRCG

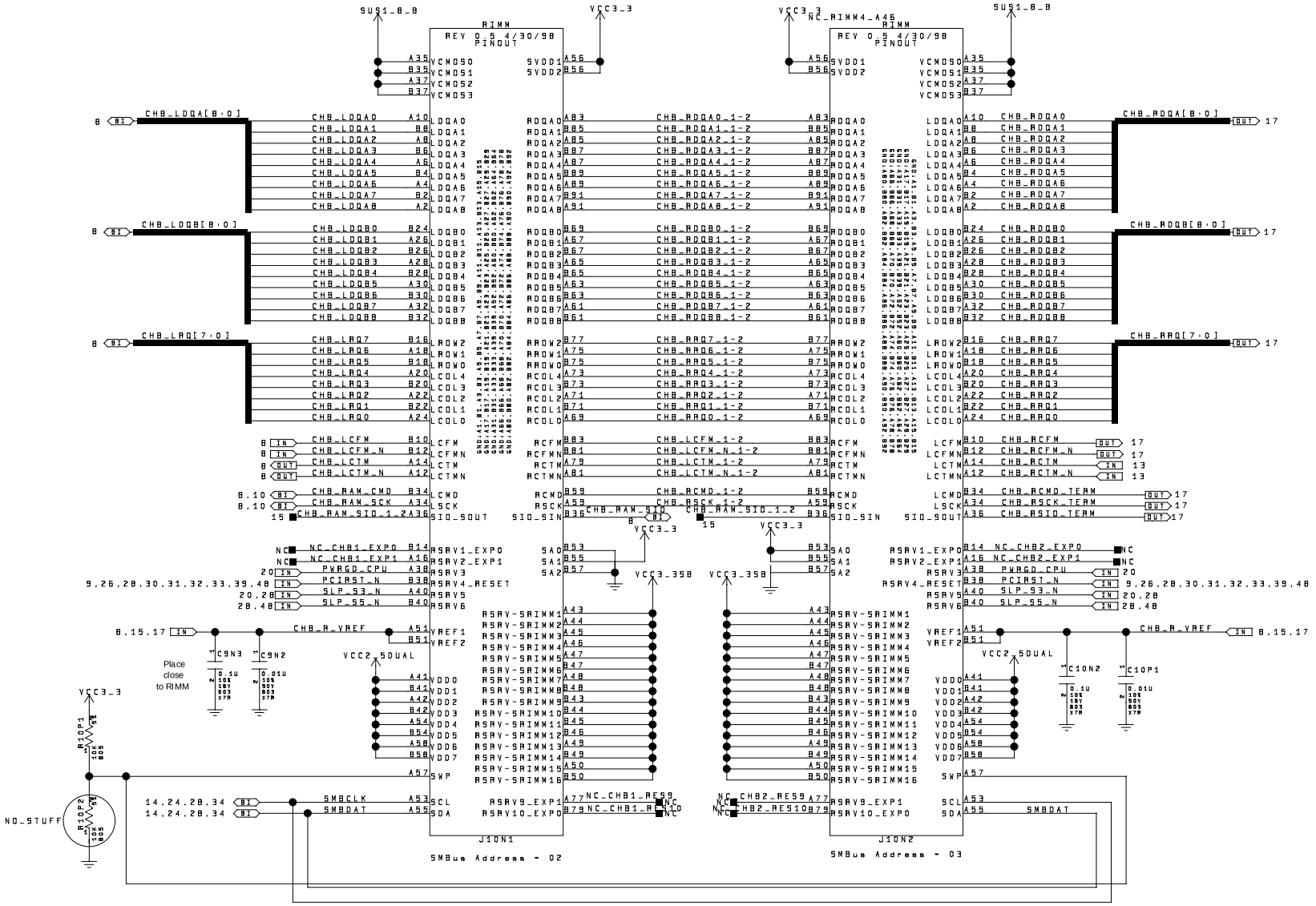
TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	13 OF 53



RIMM CHA CONNECTORS

ROOM=RIMM_CHA

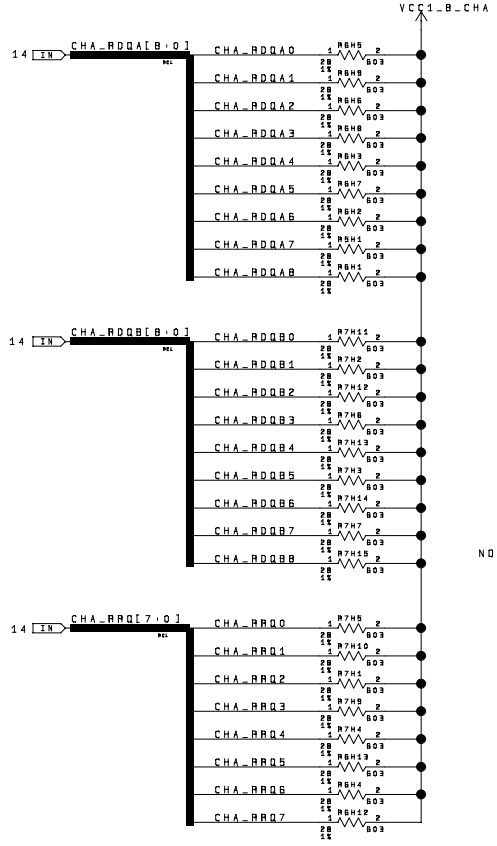
TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	14 OF 53

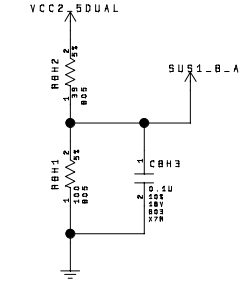


RIMM CHB CONNECTORS

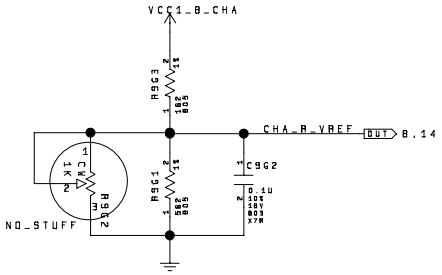
ROOM=RIMM_CHB

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:08	15 OF 53

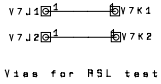




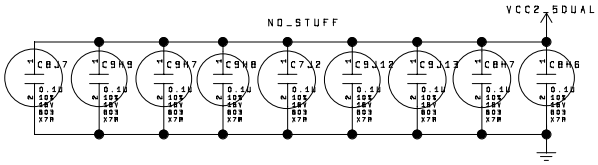
RAMBUS SUS1.8V GENERATION



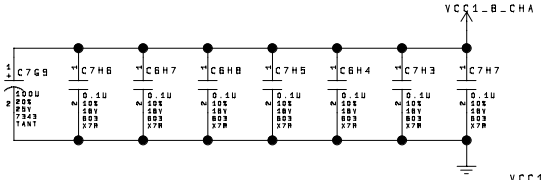
RAMBUS VREF GENERATION

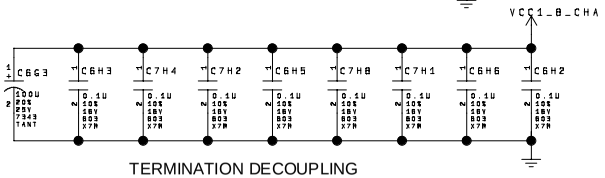


Vias for RSL test traces

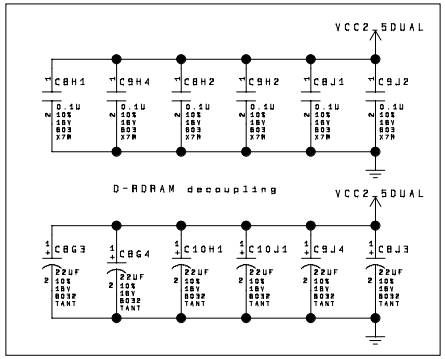


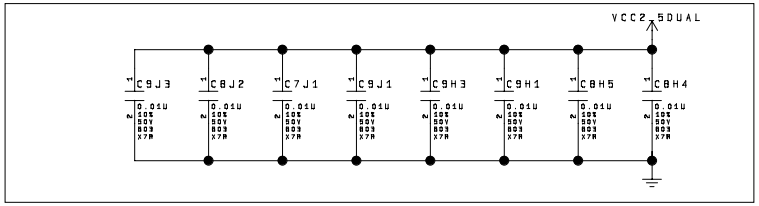
Back No Stuff Decouple



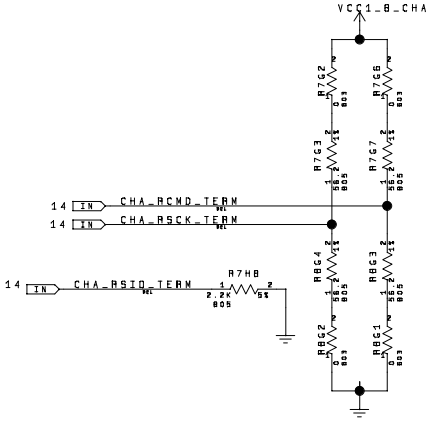


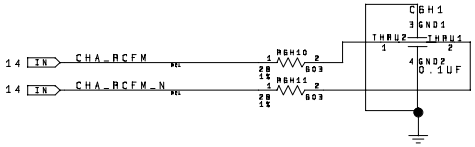
TERMINATION DECOUPLING
(one 0.1uF cap per 2 RSL lines)





RIMM DECOUPLING

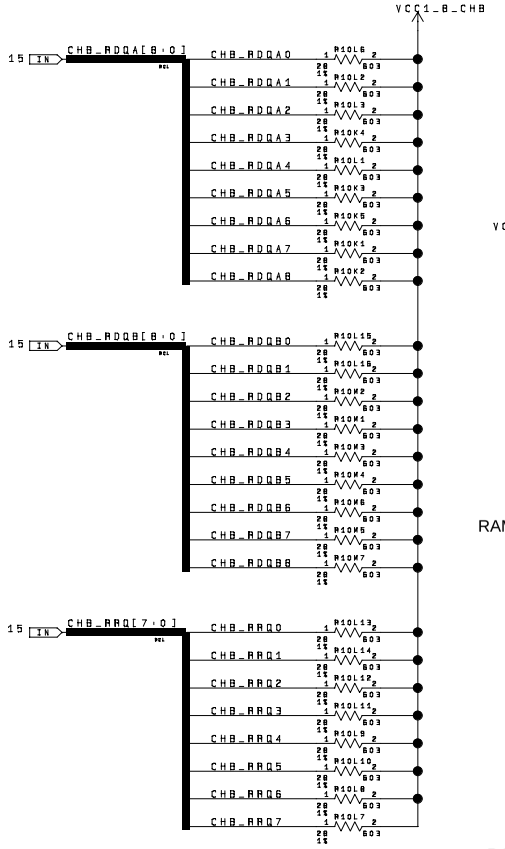


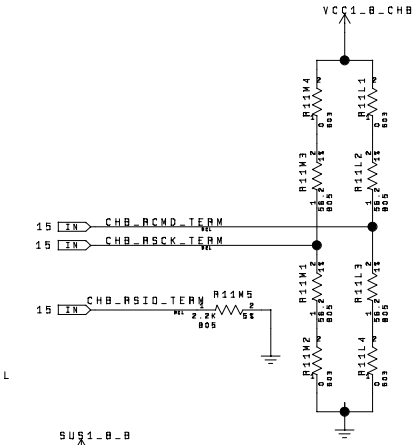


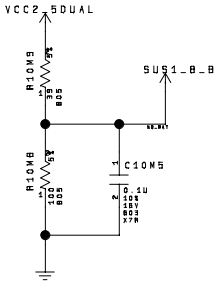
ROOM=RIMM_CHA

RDRAM CHA TERMINATION AND DECOUPLING

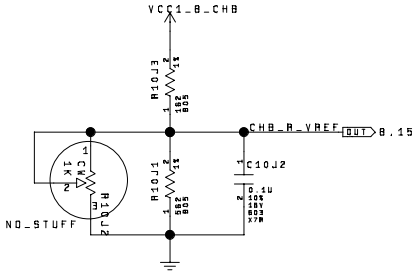
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	16 OF 53



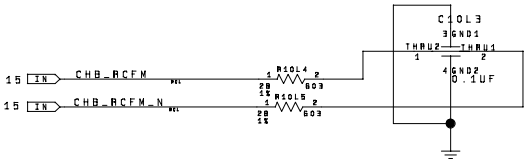


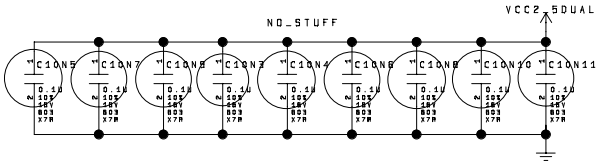


RAMBUS SUS1.8V GENERATION

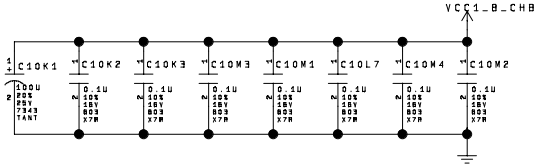


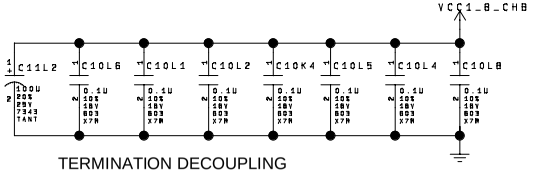
RAMBUS CHB VREF GENERATION



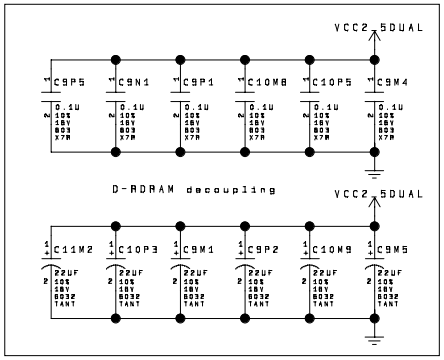


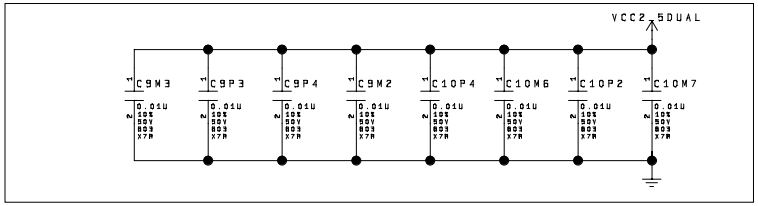
Back No Stuff Decouple





TERMINATION DECOUPLING
(one 0.1uF cap per 2 RSL lines)





RIMM DECOUPLING

ROOM=RIMM_CHB

RDRAM CHB TERMINATION AND DECOUPLING

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
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WTX POWER SUPPLY

VCC3_3SB

82559 LOM
SRIMMs
ADM1024
ICH, SIO
PCI32,PCI64, AMR

p.22

VCC5

CPUs,
VRMs,
AGP, PCI32, PCI64
AMR, Port 80,
USB, KBD/MS

VCC5_SB

WAKE ON LAN
COM1

VCC12

VRMs, FANs,
AGP, PCI32, AMR,
MIC AMP,PCI64
COM PORTs

VCC_DIG

VRM P0
VRM P1
RAMBUS ISR 2.5V

p.22

VCC3_3

CPUs,
CK133,
DRCG,
RIMMs,
AGP,ICH,
FWH,SIO,P64H
PCI32, PCI64, AMR
GAMEPORT

VCC-12

PCI32, PCI64, AMR
MIC AMP,
COM PORTs

VOLTAGE REGULATORS

VTT1_5

CPUs

p.21

VCC2_5DUAL

RIMMs

p.22

AUDVCC5

AD1881 AUDIO
LM4880 AMP

p.38

AGP1_5

AGP

p.21

VCC2_5

CK133
DRCG
ITP CLK BUFFER

p.22

SUS1_8A

RIMMs

p.16

VCC1_8

ICH, P64H

p.21

SUS1_8B

RIMMs

p.17

VCC1_8_MCH

MCH
DRCG

p.21

VCC_CMOS

CMOS PULLUPS

2.5V

p.22

VCC1_8_CHA
VCC1_8_CHB

RIMM TERM

p.17

VRMs

VCC_CORE_P0

CPU0

p.9

VCC_CORE_P1

CPU1

p.9

SWITCHED VOLTAGE PLANES

VDDQ

VCC3.3 / AGP1.5

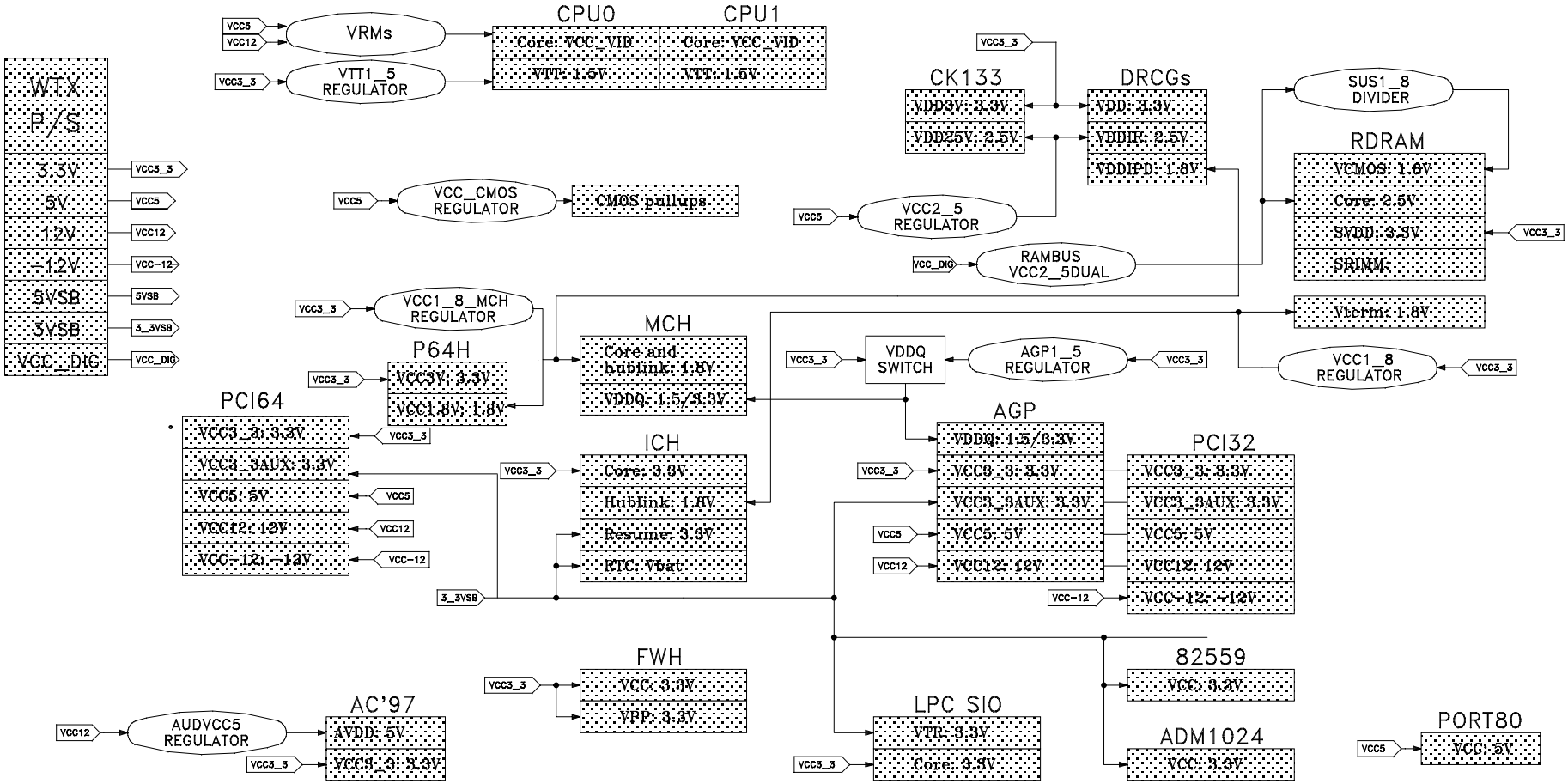
AGP
MCH

p.25

Note: Only major devices are listed in this diagram

POWER MANAGEMENT MAP

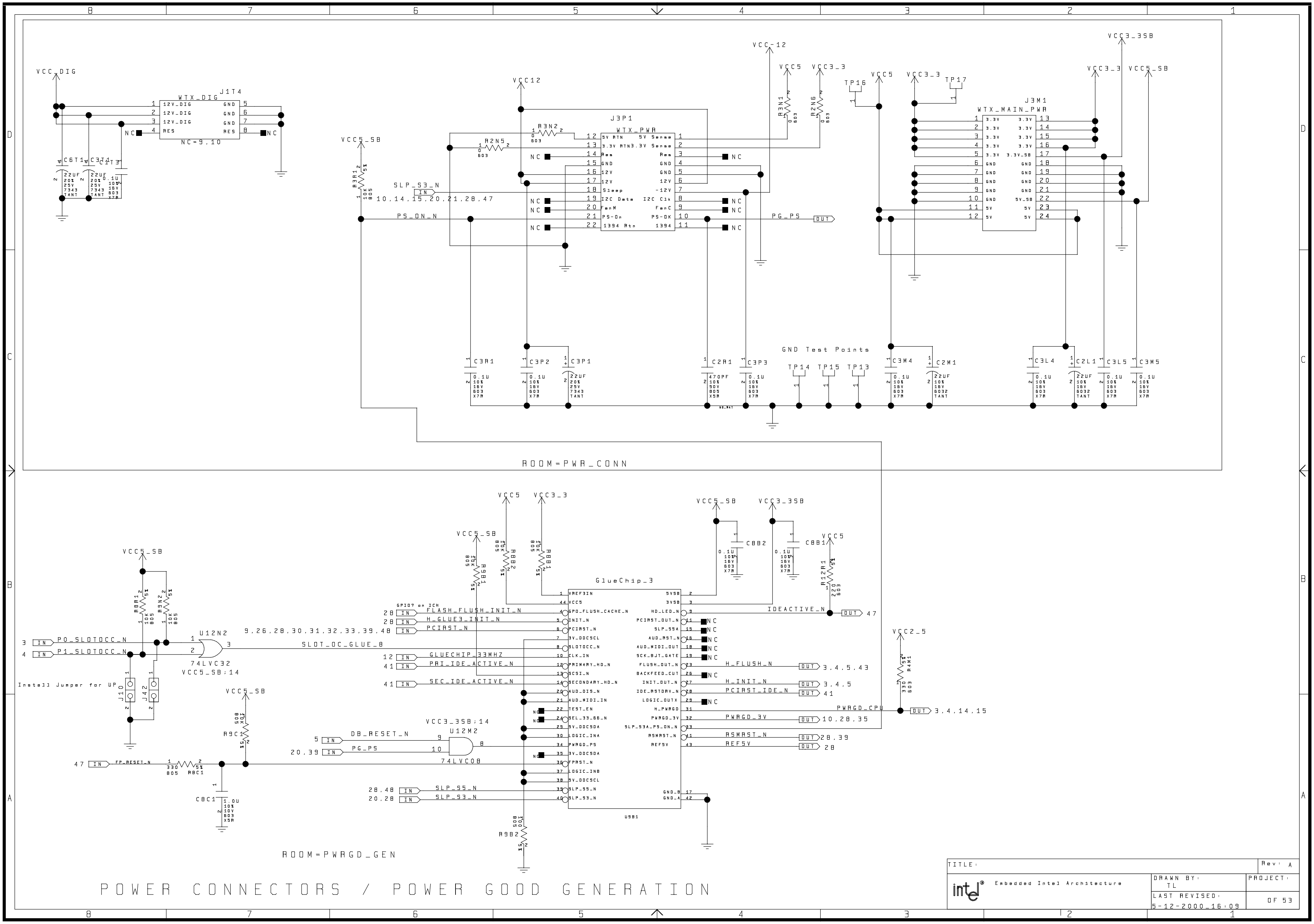
TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	OF 53



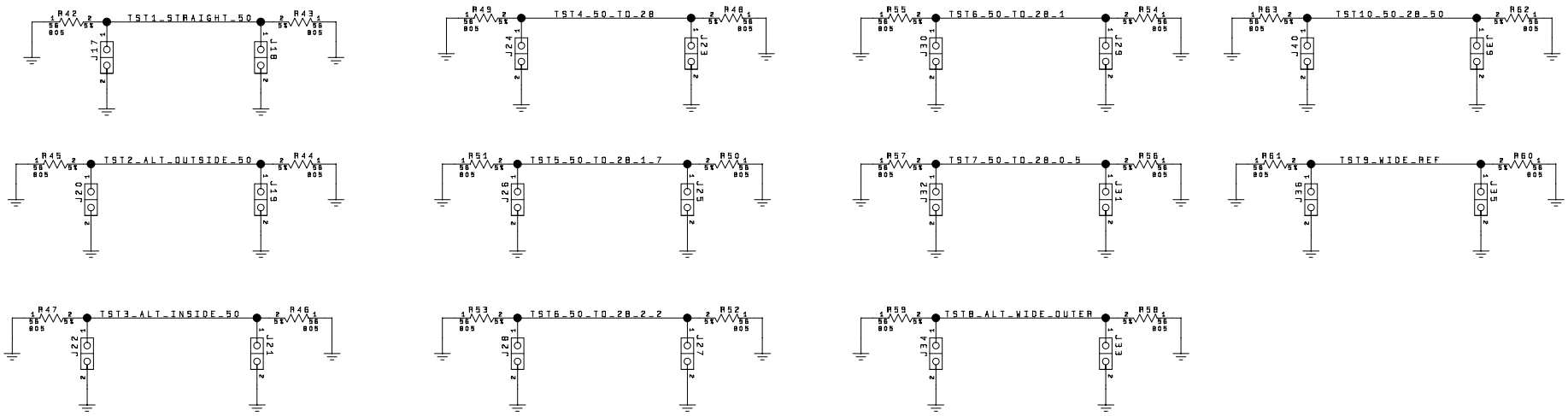
AHA: Vdd = 1.8V, Vref = 0.5 Vdd
RSL: Vtt=1.8V, Vref = 2/3 Vtt
GTL: Vtt=1.5V, Vref = 2/3 Vtt
AGP: Vdd= 1.5V or 3.3V, Vref= 0.5 Vagpdd (1.5V) or 0.4 Vagpdd (3.3V)

POWER DISTRIBUTION MAP

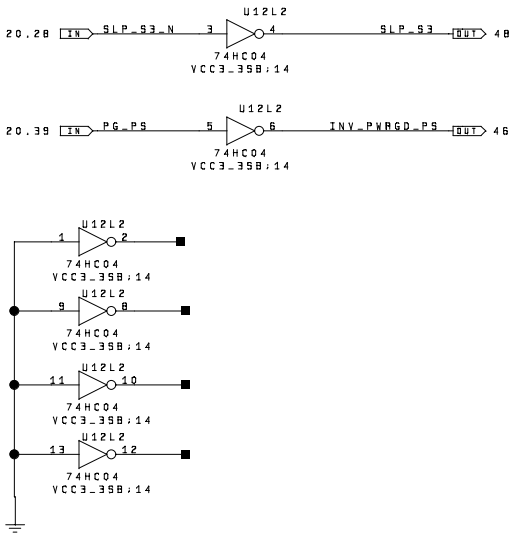
TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	19 OF 53



ROOM=PWR_CONN
ROOM=PWRGD_GEN
J1T4 WTX_DIG
J3P1 WTX_PWR
J3M1 WTX_MAIN_PWR
GlueChip_3
U9B1
U12N2 74LVC32
U12M2 74LVC08
GND Test Points
POWER CONNECTORS / POWER GOOD GENERATION
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
5-12-2000_16:09
OF 53



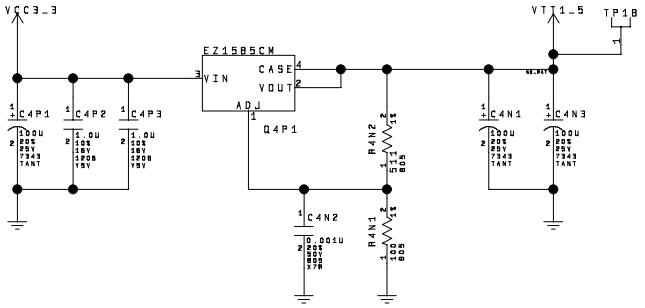
Impeadance Test Traces



POWER MANAGEMENT LOGIC

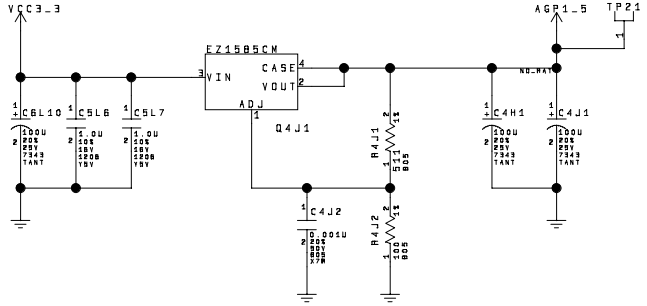
ROOM=PWR_MGMT_LOGIC

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	21 OF 53



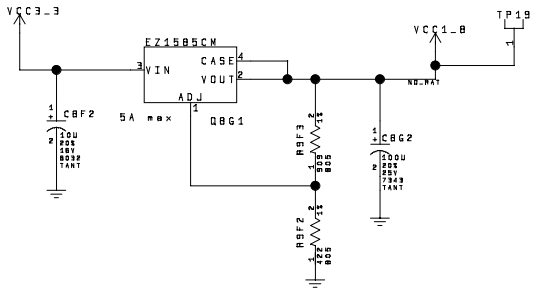
VTT 1.5V GENERATION

ROOM=VTT_1.5V_GEN



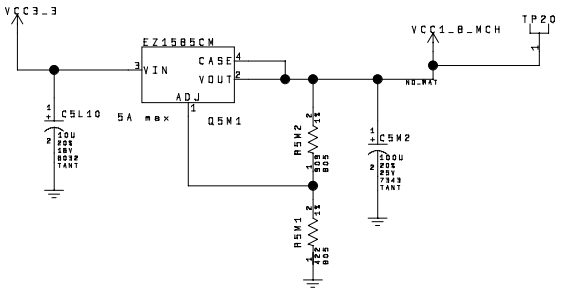
AGP 1.5V GENERATION

ROOM=AGP_1.5V_GEN



1.8V GENERATION

ROOM=1.8V_GEN

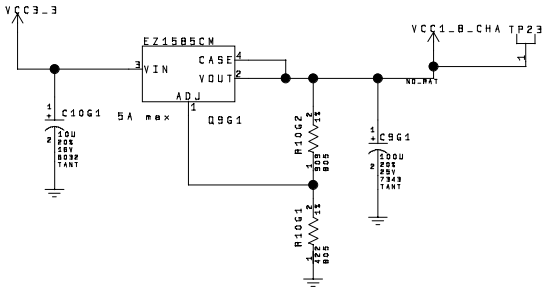


MCH 1.8V GENERATION

ROOM=MCH_1.8V_GEN

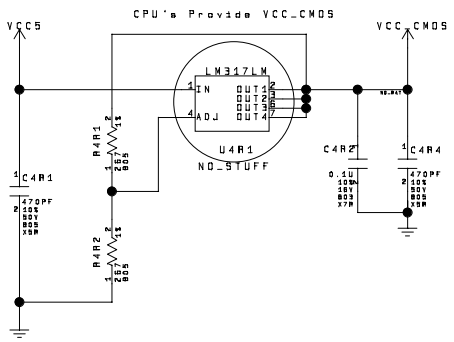
1.5V / 1.8V REGULATORS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	22 OF 53



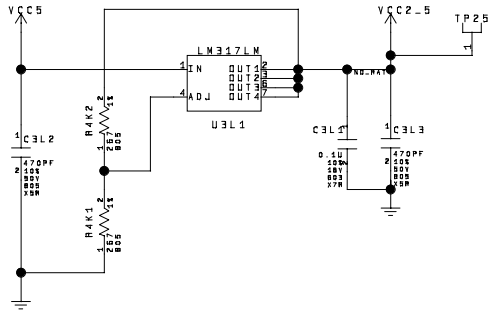
1.8V GENERATION FOR RAMBUS CHA TERM

ROOM=1.8V_GEN



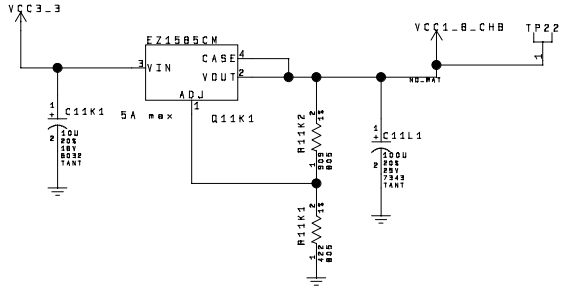
FSB CMOS VOLTAGE GENERATION

ROOM=FSB_CMOSV_GEN



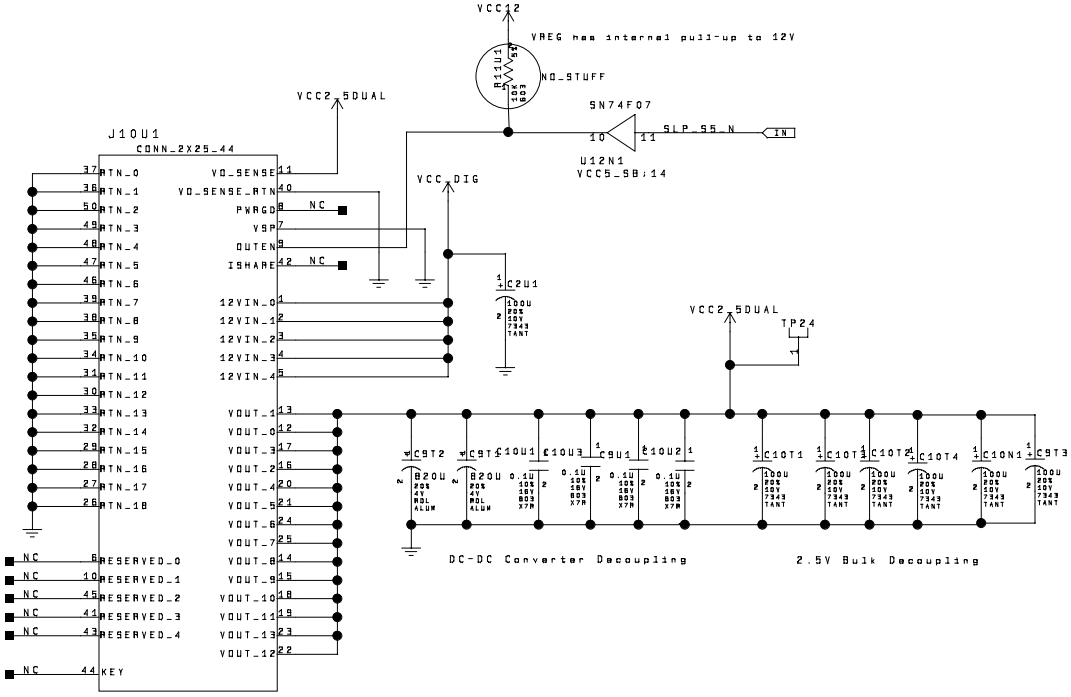
2.5V GENERATION

ROOM=2.5V_GEN



1.8V GENERATION FOR RAMBUS CHB TERM

ROOM=1.8V_GEN



RAMBUS 2.5V DUAL GENERATION

ROOM=RAMBUS_25_GEN

VCC_CMOS / 2.5V / 3.3V REGULATORS

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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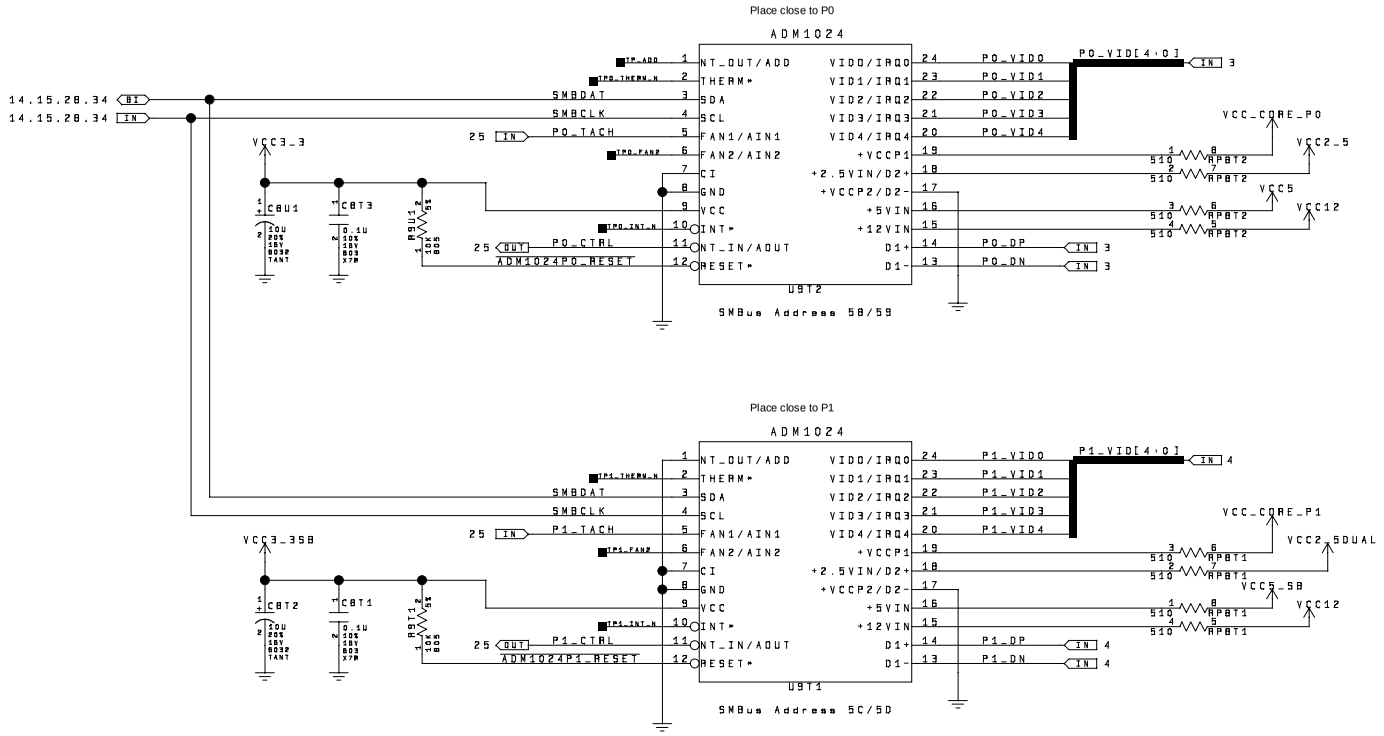
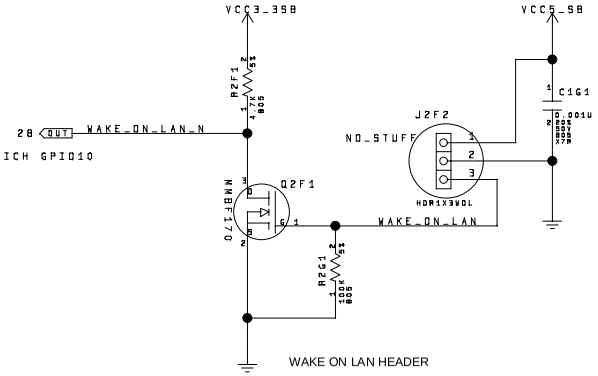


Not Populated

TEMP / VOLTAGE MONITORING

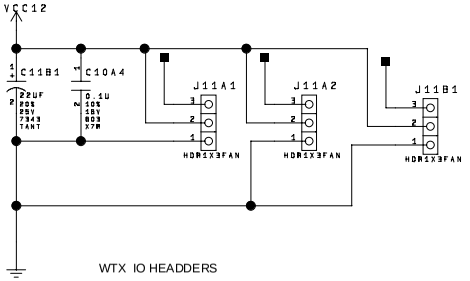
ROOM=PROCESSORS

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	OF 53

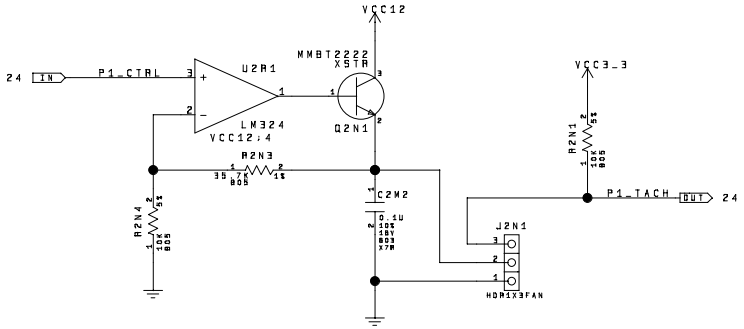


WAKE ON LAN HEADER

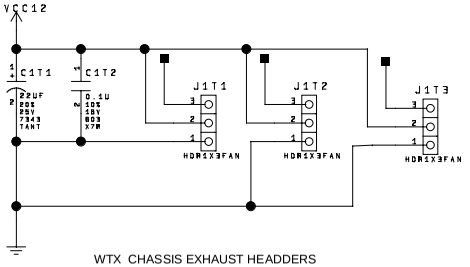
ROOM=82559



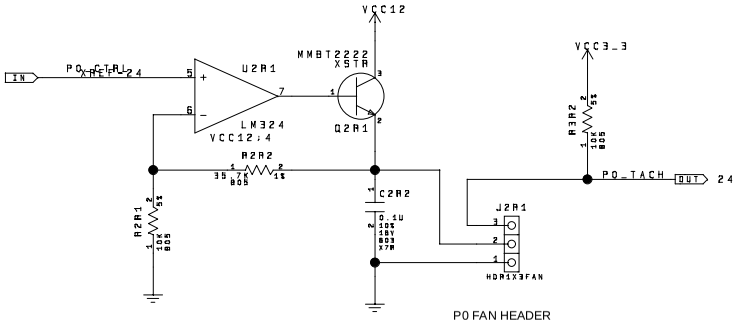
WTX IO HEADDERS



P1 FAN HEADER



WTX CHASSIS EXHAUST HEADDERS

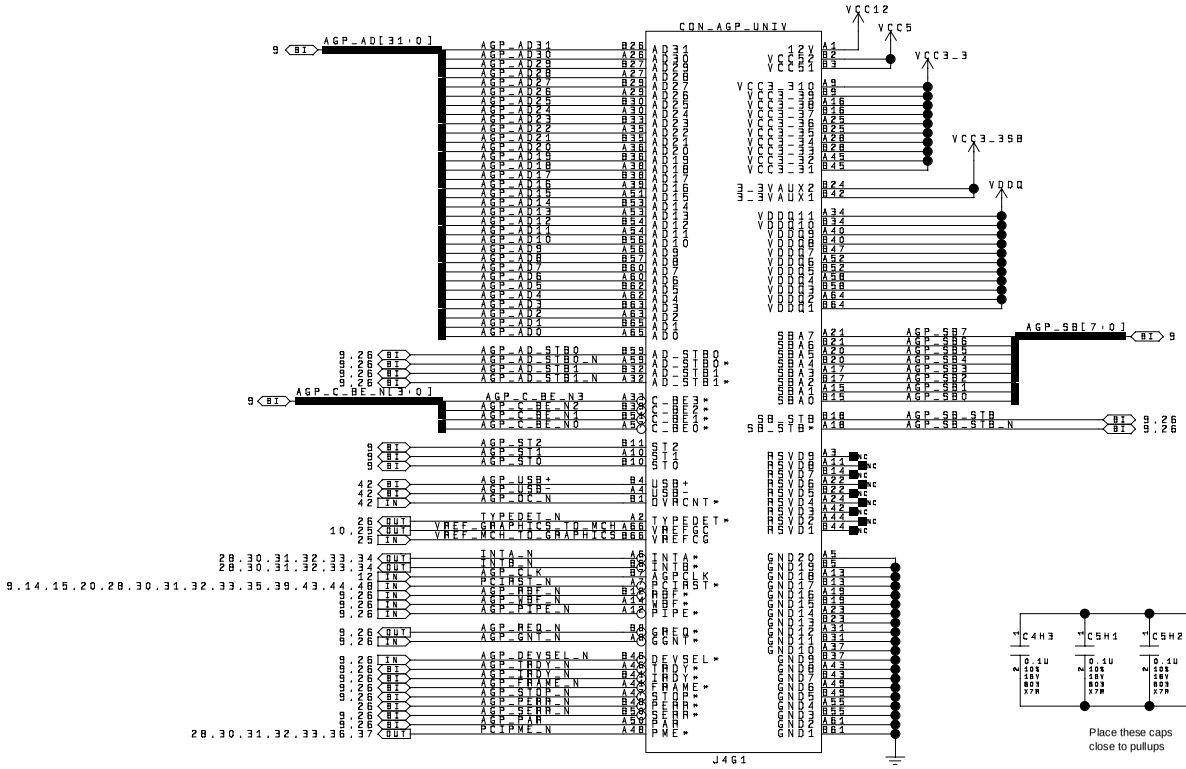


P0 FAN HEADER

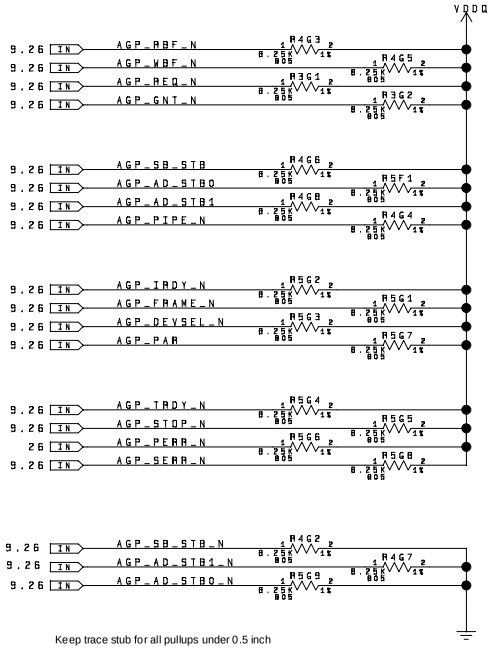
ROOM=PROCESSORS

WOL / FAN HEADERS

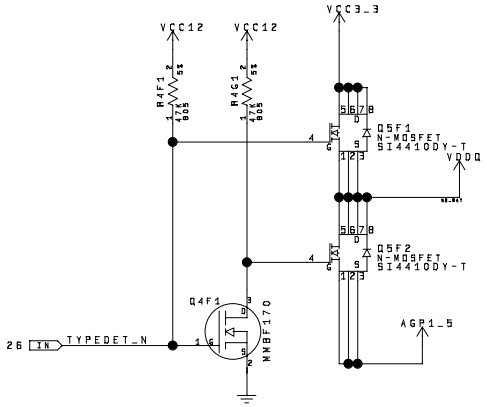
TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	OF 53



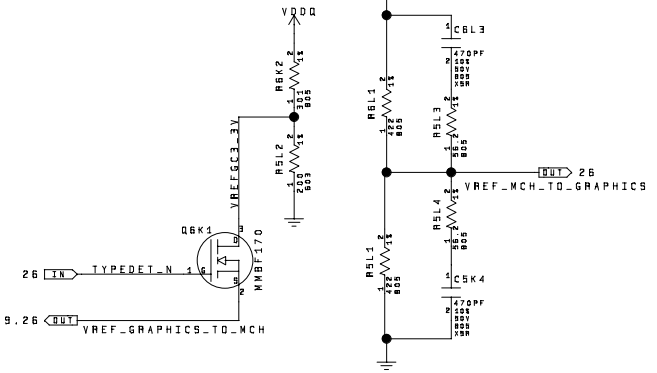
Place these caps
close to pullups



Keep trace stub for all pullups under 0.5 inch
Keep trace stub for STROBE pullups under 0.1 inch



AGP VDDQ SWITCH

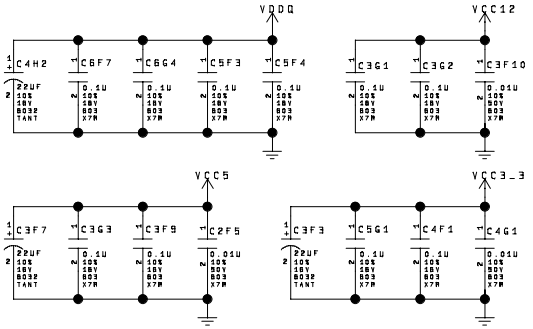


VREFGC generation for 3.3V AGP cards
Place close to MCH

VREFCG generation
Place close to MCH

AGP VREF GENERATION

ROOM=MCH



AGP DECOUPLING

AGP 4X

ROOM=AGP4X

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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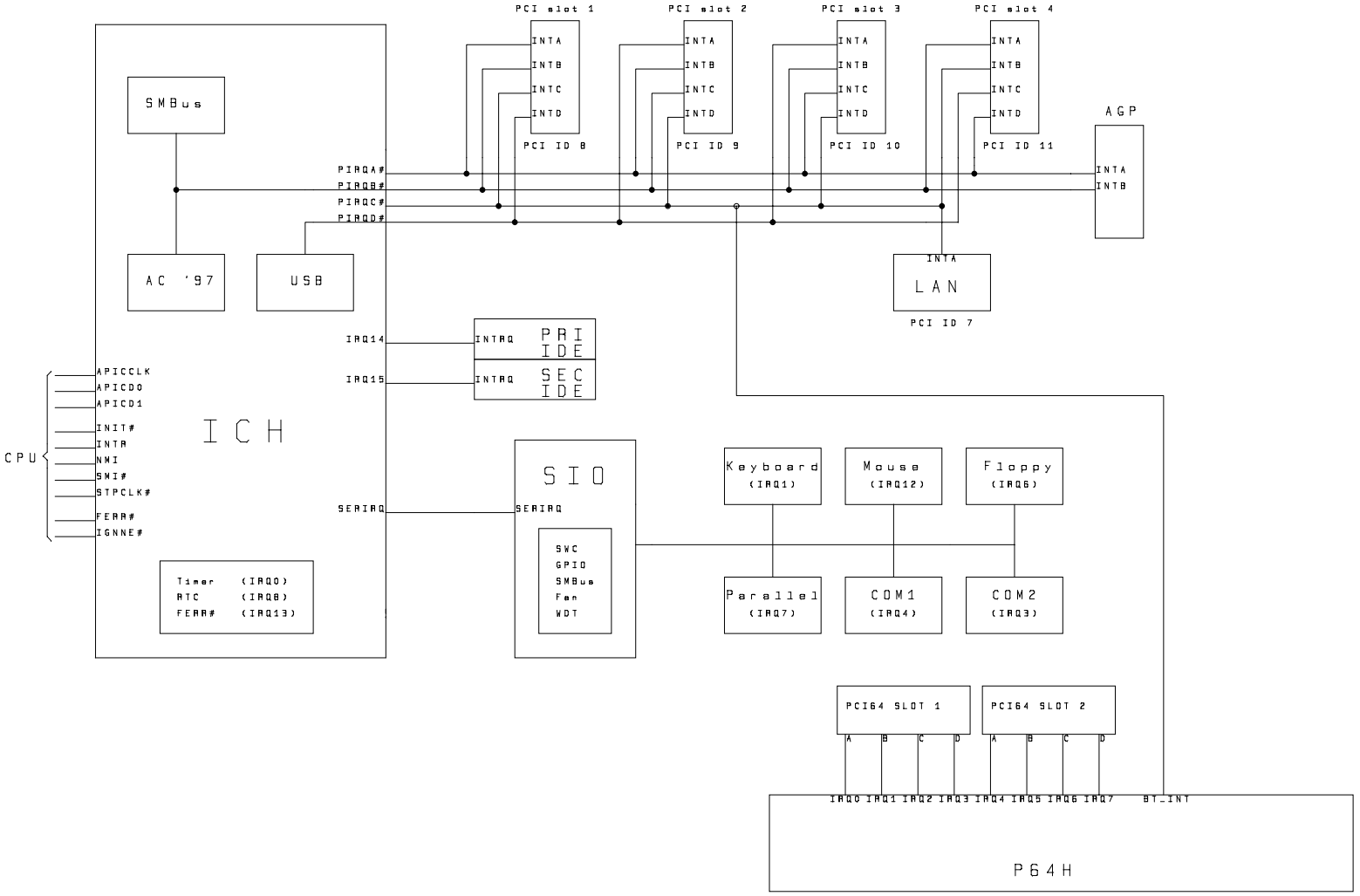
Interrupt Diagram



PCI / INTERRUPT DIAGRAM

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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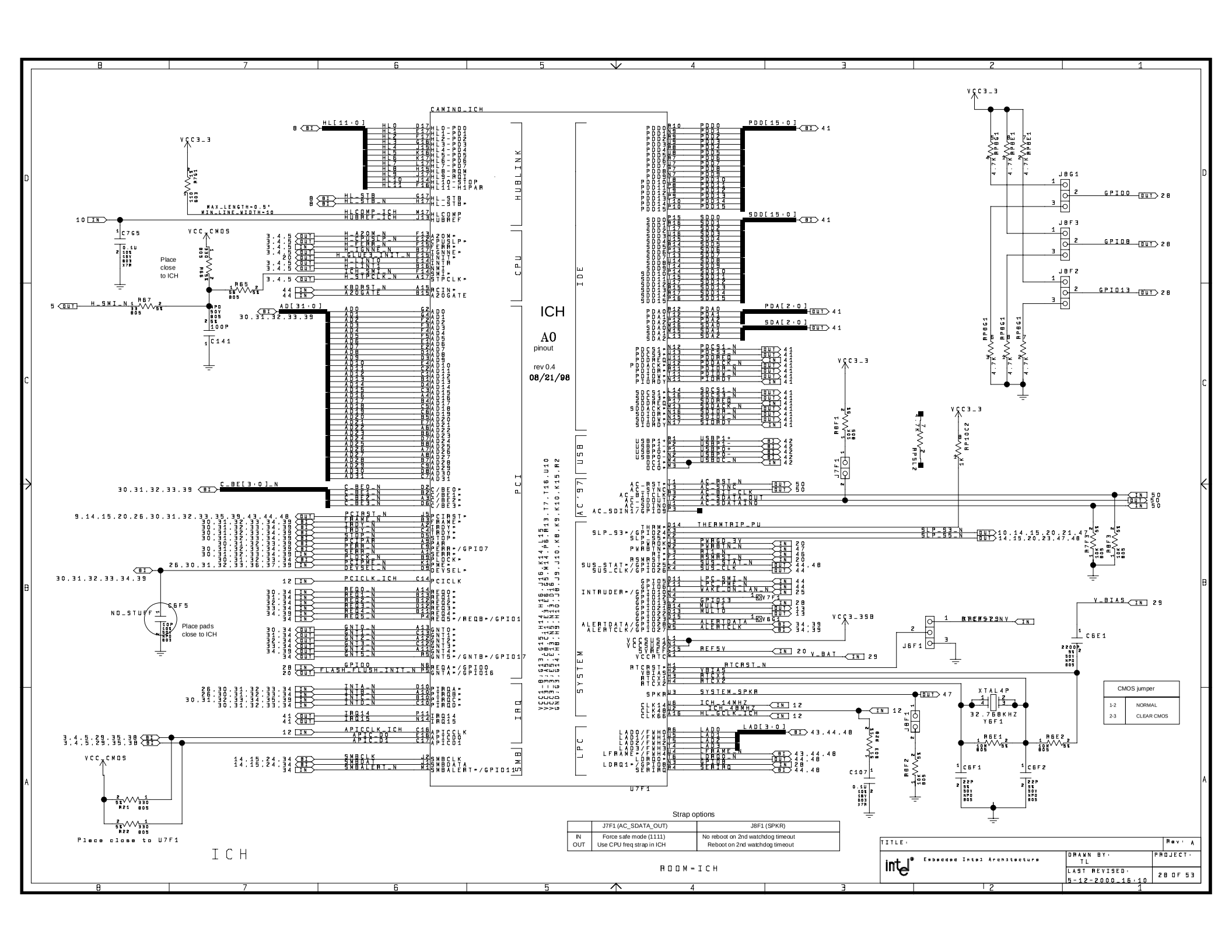
CAMINO_ICH
HUBLINK
CPU
IDE
PCI
USB
AC'97
SYSTEM
IRQ
SMB
LPC
ICH
A0
pinout
rev 0.4
08/21/98
U7F1
Place close to ICH
Place pads close to ICH
NO_STUFF
Place close to U7F1
Strap options
J7F1 (AC_SDATA_OUT)
J8F1 (SPKR)
IN
Force safe mode (1111)
No reboot on 2nd watchdog timeout
OUT
Use CPU freq strap in ICH
Reboot on 2nd watchdog timeout
CMOS jumper
1-2
NORMAL
2-3
CLEAR CMOS
ROOM=ICH
ICH
Embedded Intel Architecture
DRAWN BY: TL
LAST REVISED: 5-12-2000 16:10
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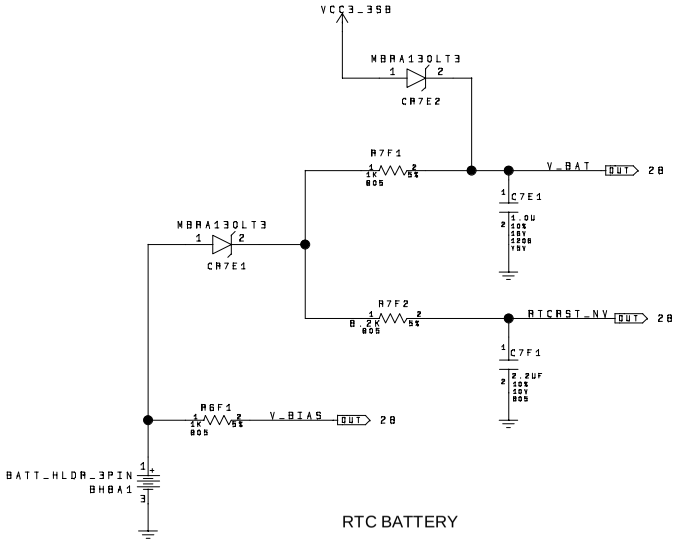
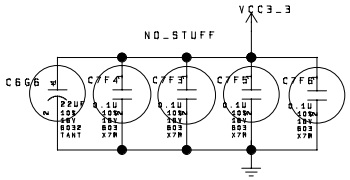
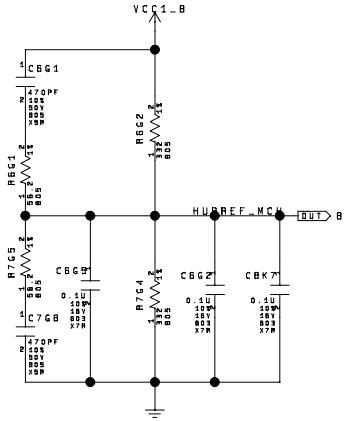
Rev: A



RTC BATTERY

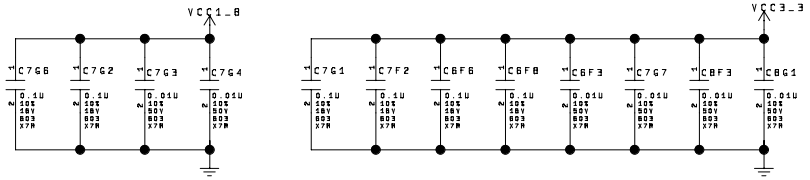


Back No Stuff ICH

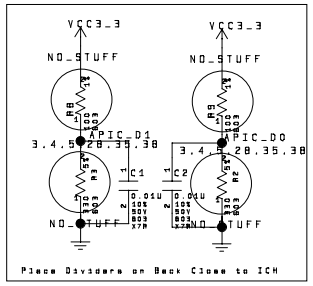


MCH HUBREF GENERATION

Place close to ICH



ICH DECOUPLING

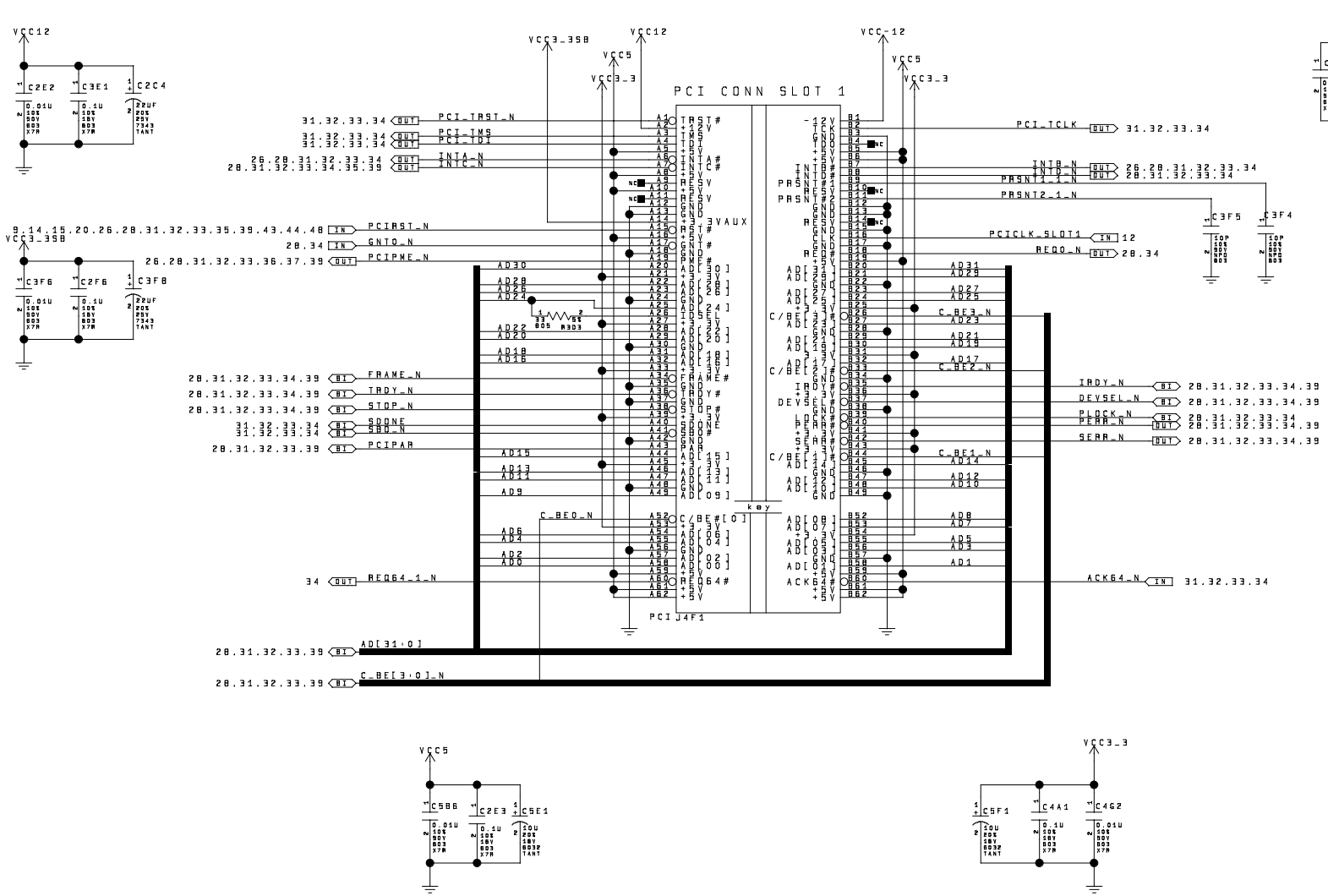


Place Dividers on Back Close to ICH

ROOM=ICH

ICH DECOUPLING AND SUPPORT CIRCUITRY

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	29 OF 53



PCI CONN SLOT 1

ROOM=PCI

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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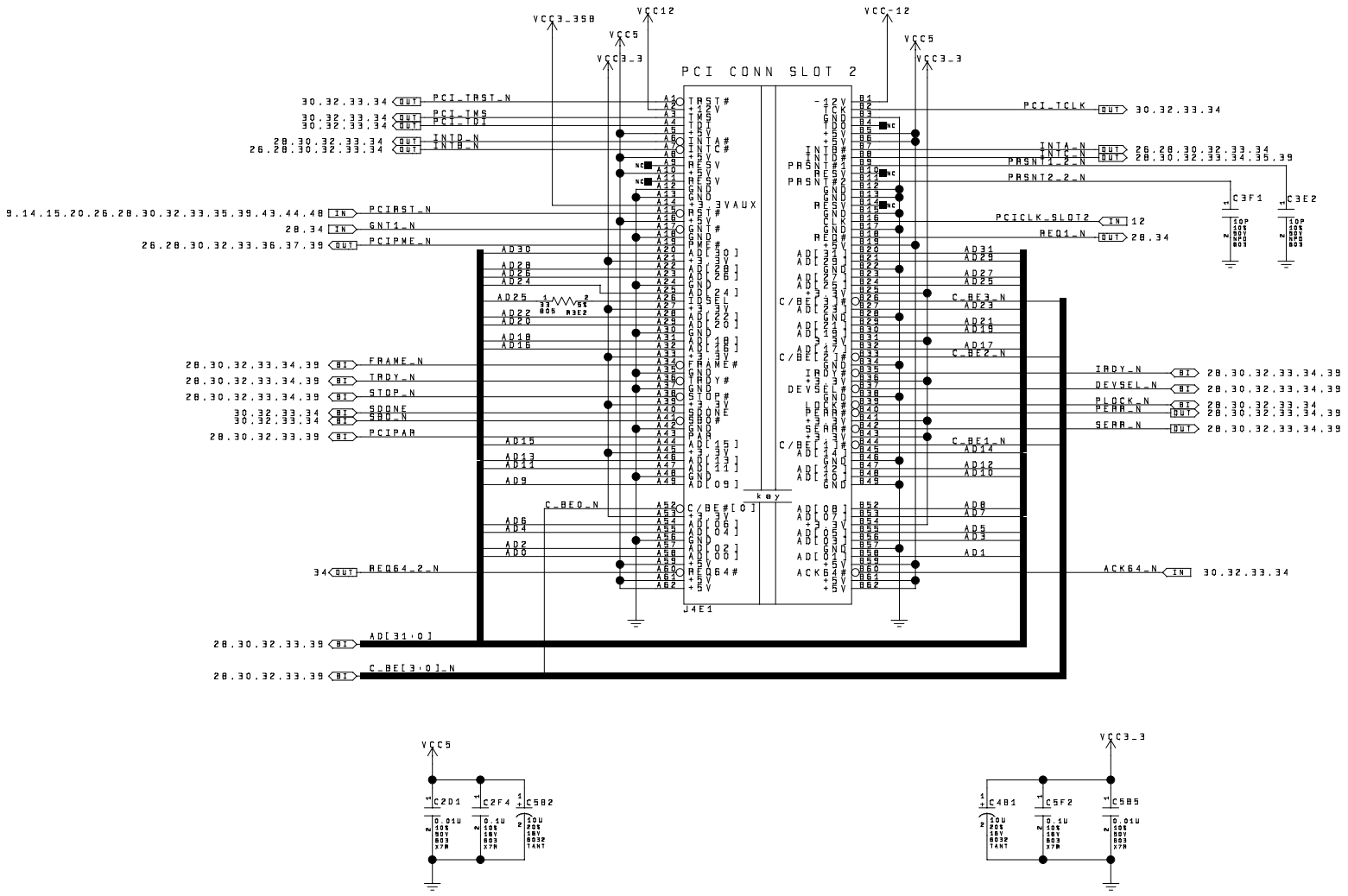
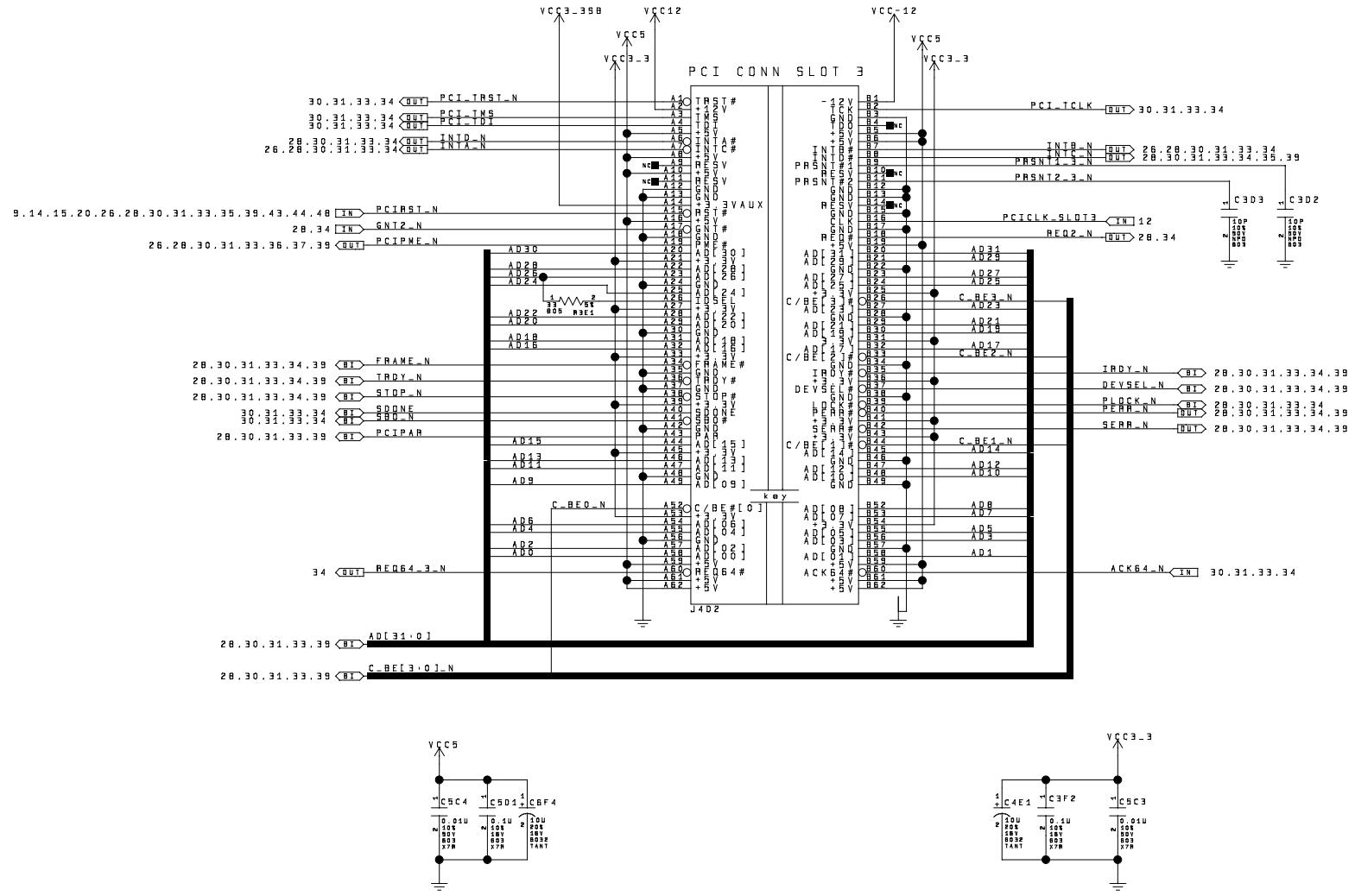


PCI CONN SLOT 2

ROOM=PCI

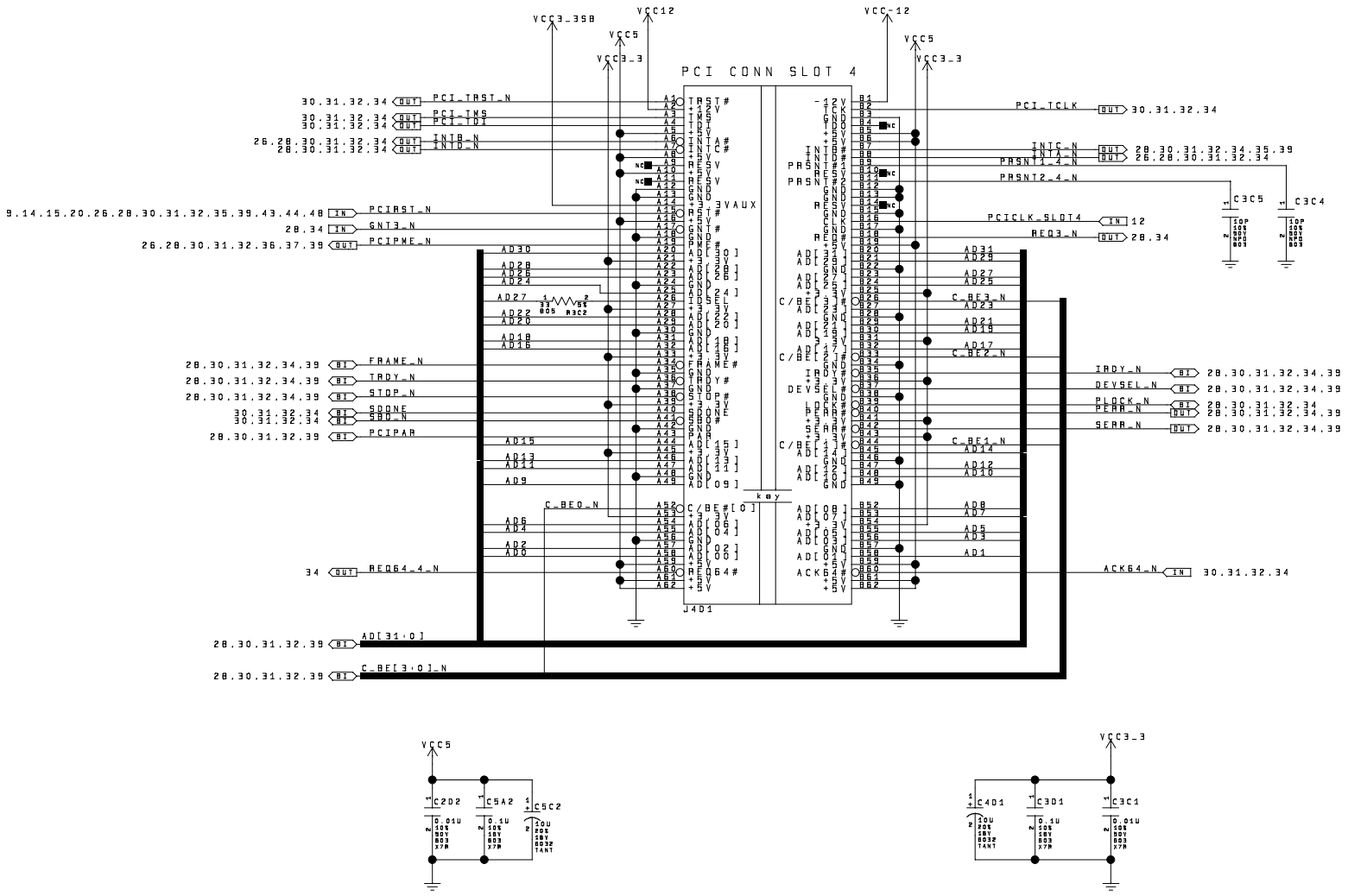
TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	31 OF 53



PCI CONN SLOT 3

ROOM=PCI

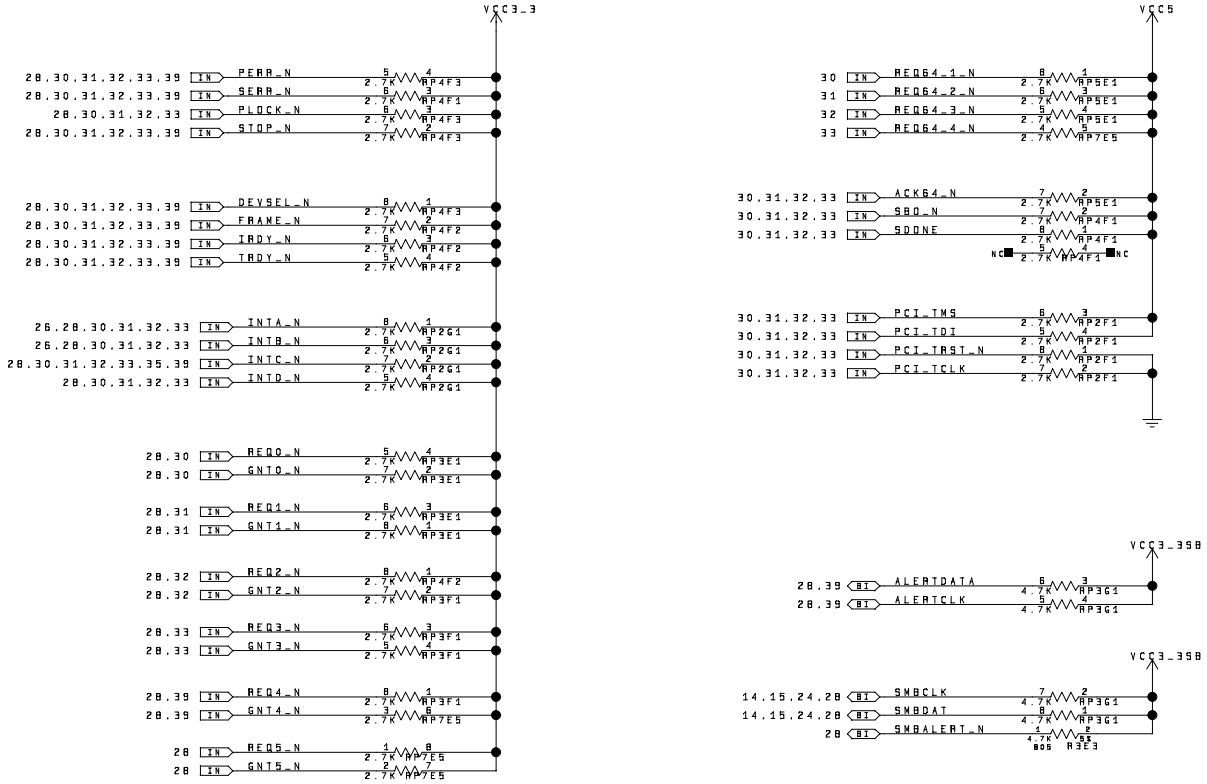
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
	32 OF 53



PCI CONN SLOT 4

ROOM=PCI

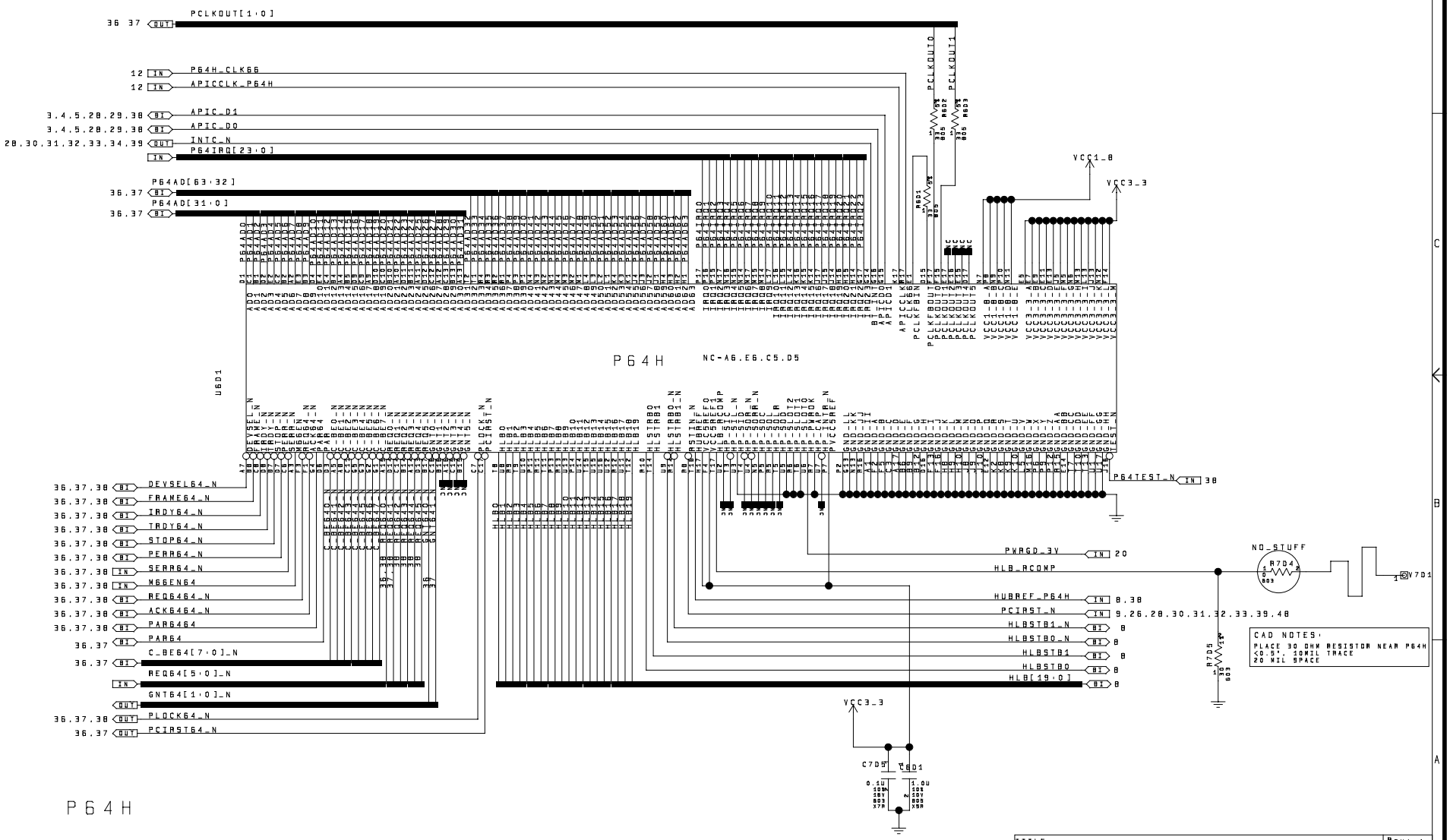
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
	33 OF 53



PCI PULLUPS

ROOM=PCI

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	34 OF 53


PCLKOUT[1:0]
P64H_CLK66
APICCLK_P64H
APIC_D1
APIC_D0
INIC_N
P64IRQ[23:0]
P64AD[63:32]
P64AD[31:0]
P64H
NC-A6,E6,C5,D5
U6D1
DEVSEL64_N
FRAME64_N
IRDY64_N
TRDY64_N
STOP64_N
PERR64_N
SERR64_N
M66EN64
REQ6464_N
ACK6464_N
PAR6464
PAR64
C_BE64[7:0]_N
REQ64[5:0]_N
GNT64[1:0]_N
PLOCK64_N
PCIRST64_N
P64TEST_N
PWRGD_3V
HLB_RCOMP
HUBREF_P64H
PCIRST_N
HLBSTB1_N
HLBSTB0_N
HLBSTB1
HLBSTB0
HLB[10:0]
VCC1_8
VCC3_3
R704
NO_STUFF
R705
CAD NOTES:
PLACE 30 OHM RESISTOR NEAR P64H
<0.5", 10MIL TRACE
20 MIL SPACE
C705
C801
ROOM=P64H
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 5-12-2000_16:09
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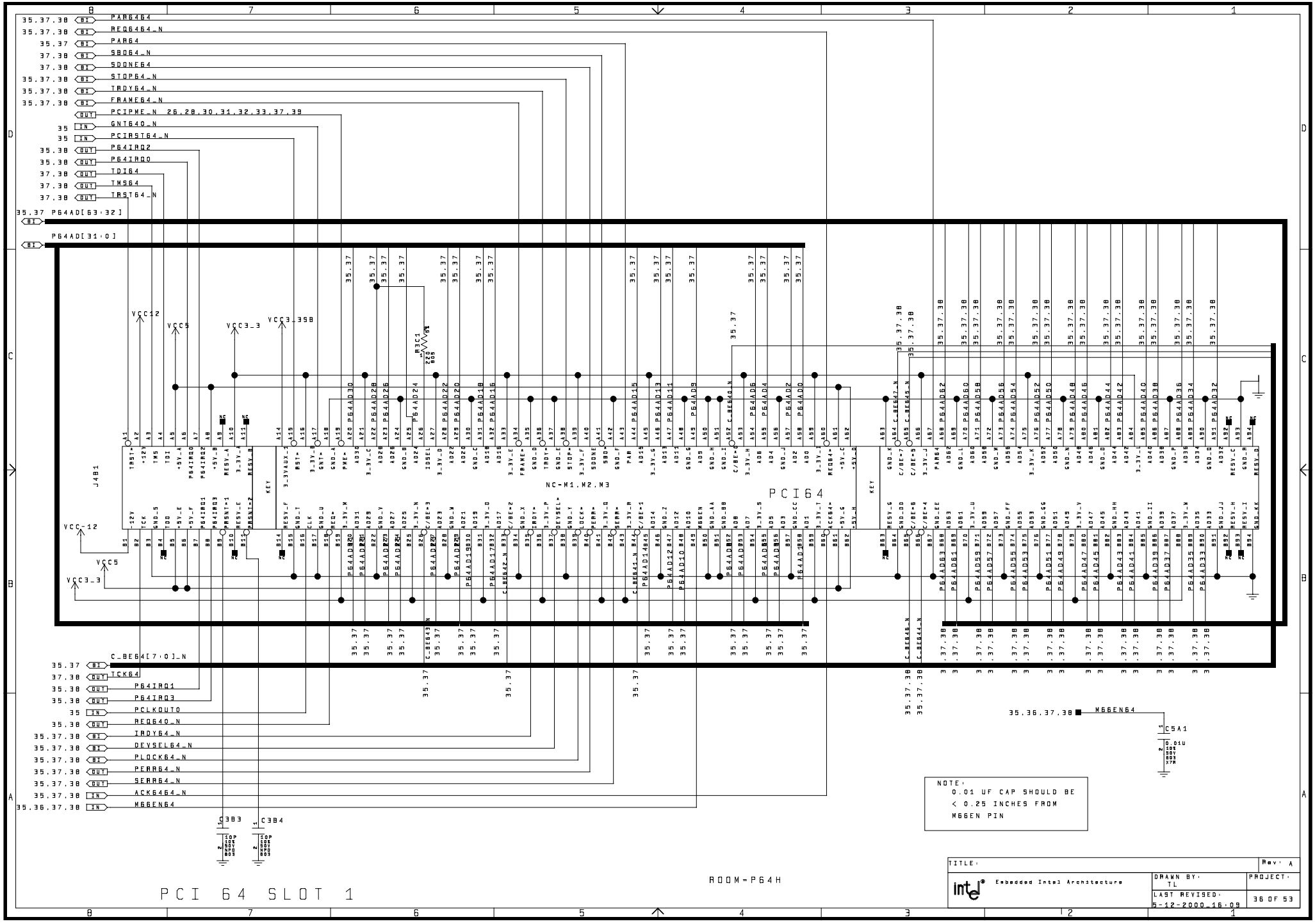
PAR6464
REQ6464_N
PAR64
SB064_N
SDONE64
STOP64_N
TRDY64_N
FRAME64_N
PCIPME_N 26,28,30,31,32,33,37,39
GNT640_N
PCIRST64_N
P64IRQ2
P64IRQ0
TDI64
TMS64
TRST64_N
P64AD[63:32]
P64AD[31:0]
VCC12
VCC5
VCC3_3
VCC3_3SB
R3C1
20.0K
J4B1
KEY
NC-M1,M2,M3
PCI64
C_BE64[7:0]_N
TCK64
P64IRQ1
P64IRQ3
PCLKOUT0
REQ640_N
IRDY64_N
DEVSEL64_N
PLOCK64_N
PERR64_N
SERR64_N
ACK6464_N
M66EN64
C3B3
C3B4
C5A1
0.01U
NOTE:
0.01 UF CAP SHOULD BE
< 0.25 INCHES FROM
M66EN PIN
PCI 64 SLOT 1
ROOM=P64H
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
5-12-2000 16:09
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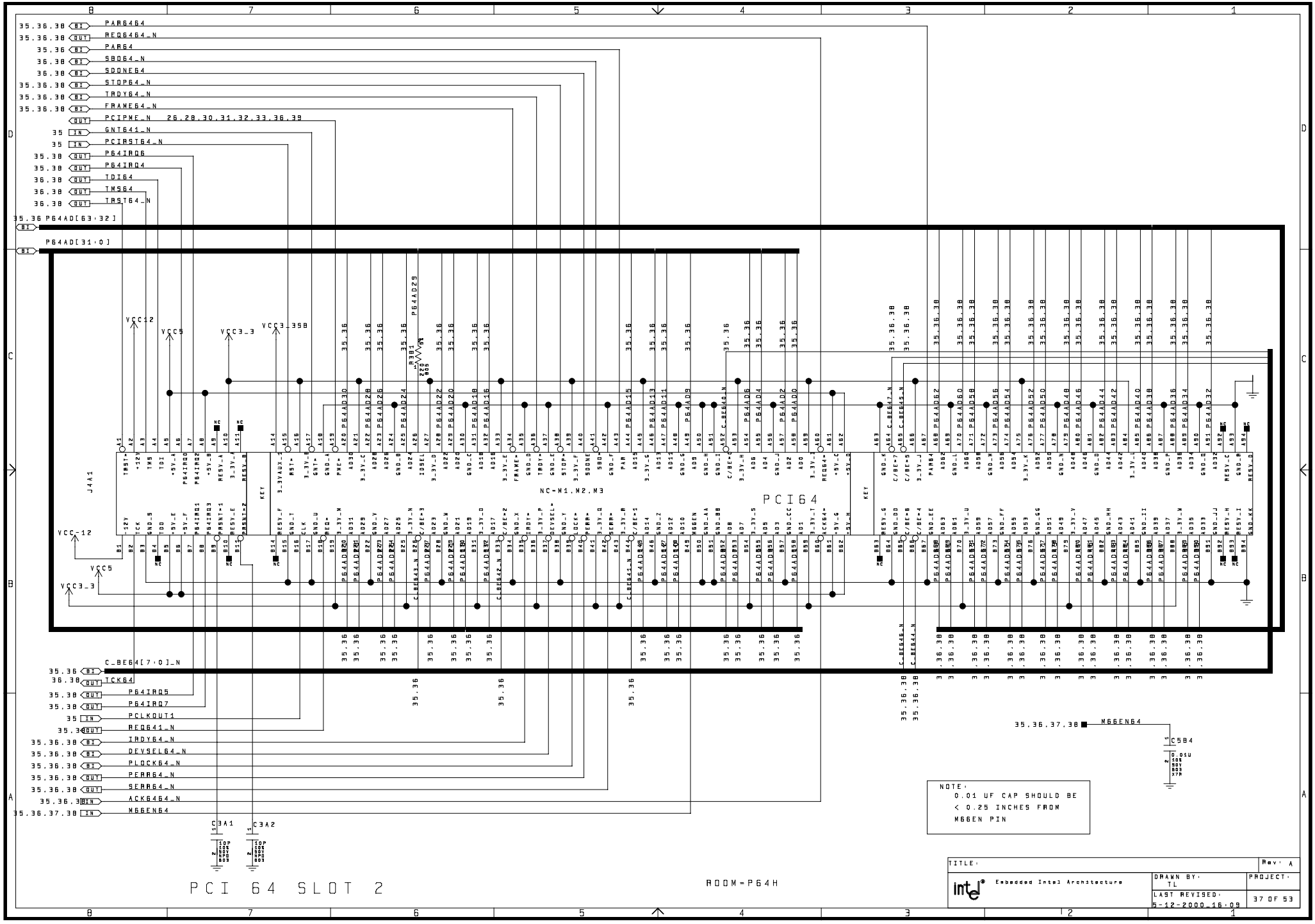
PAR64
REQ64_N
PAR64
SB064_N
SDONE64
STOP64_N
TRDY64_N
FRAME64_N
PCIPME_N
GNT64_N
PCIRST64_N
P64IRQ6
P64IRQ4
TDI64
TMS64
TRST64_N
P64AD[63:32]
P64AD[31:0]
C_BE64[7:0]_N
TCK64
P64IRQ5
P64IRQ7
PCLKOUT1
REQ64_N
IRDY64_N
DEVSEL64_N
PLOCK64_N
PERR64_N
SERR64_N
ACK64#_N
M66EN64
J4A1
KEY
PCI64
NC=M1,M2,M3
M66EN64
C584
0.01U
NOTE:
0.01 UF CAP SHOULD BE
< 0.25 INCHES FROM
M66EN PIN
C3A1
C3A2
PCI 64 SLOT 2
ROOM=P64H
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
5-12-2000_16:09
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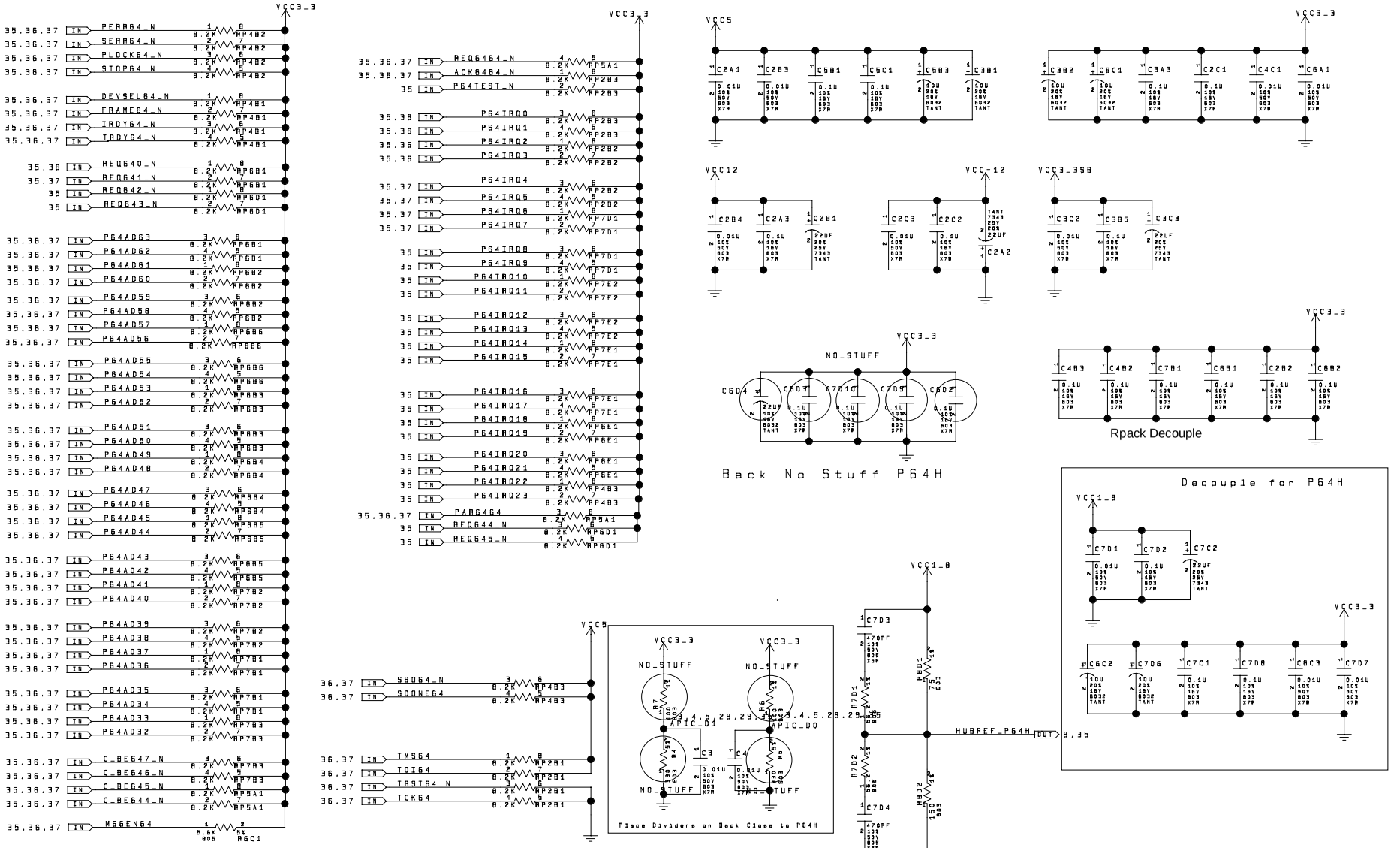
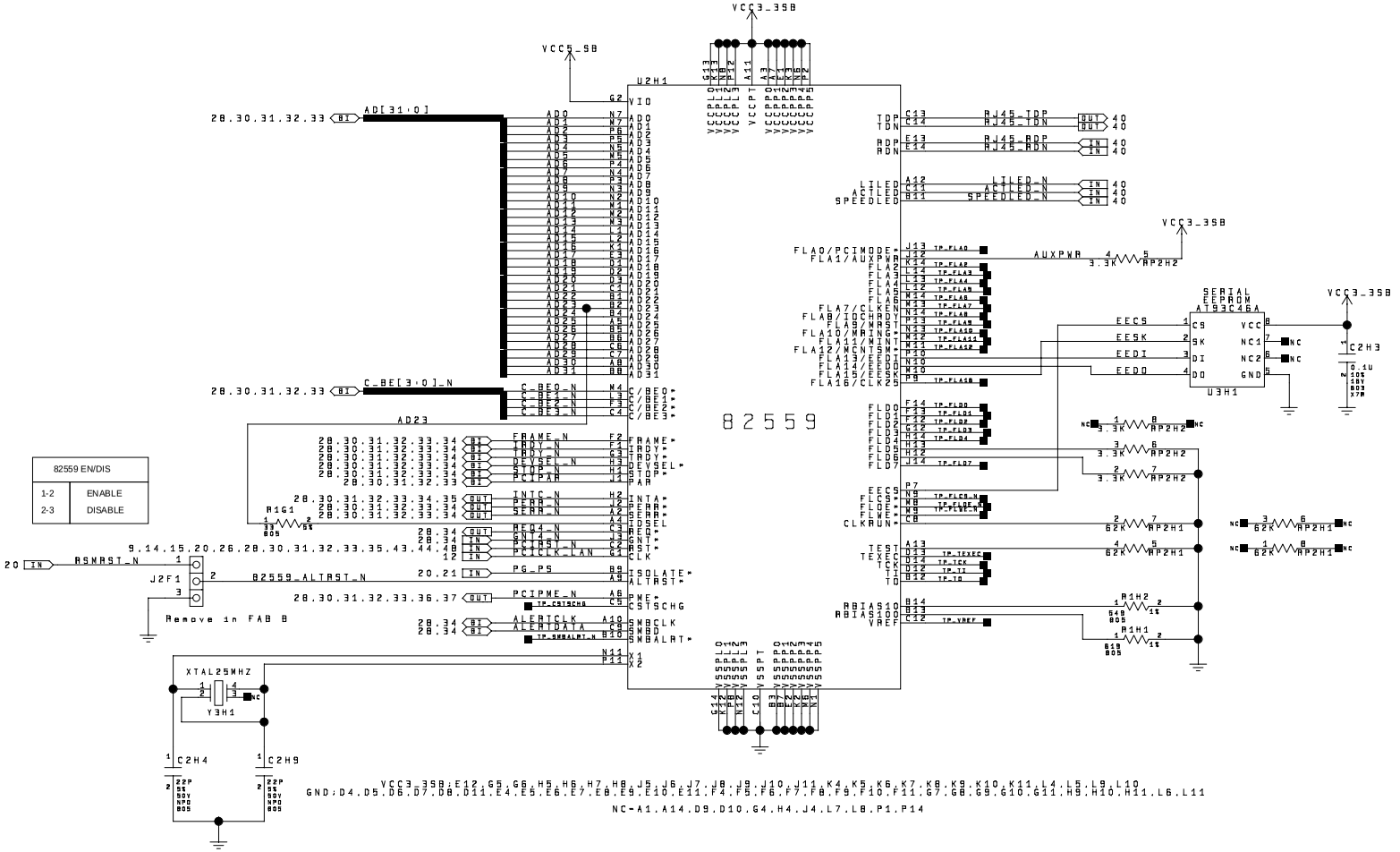


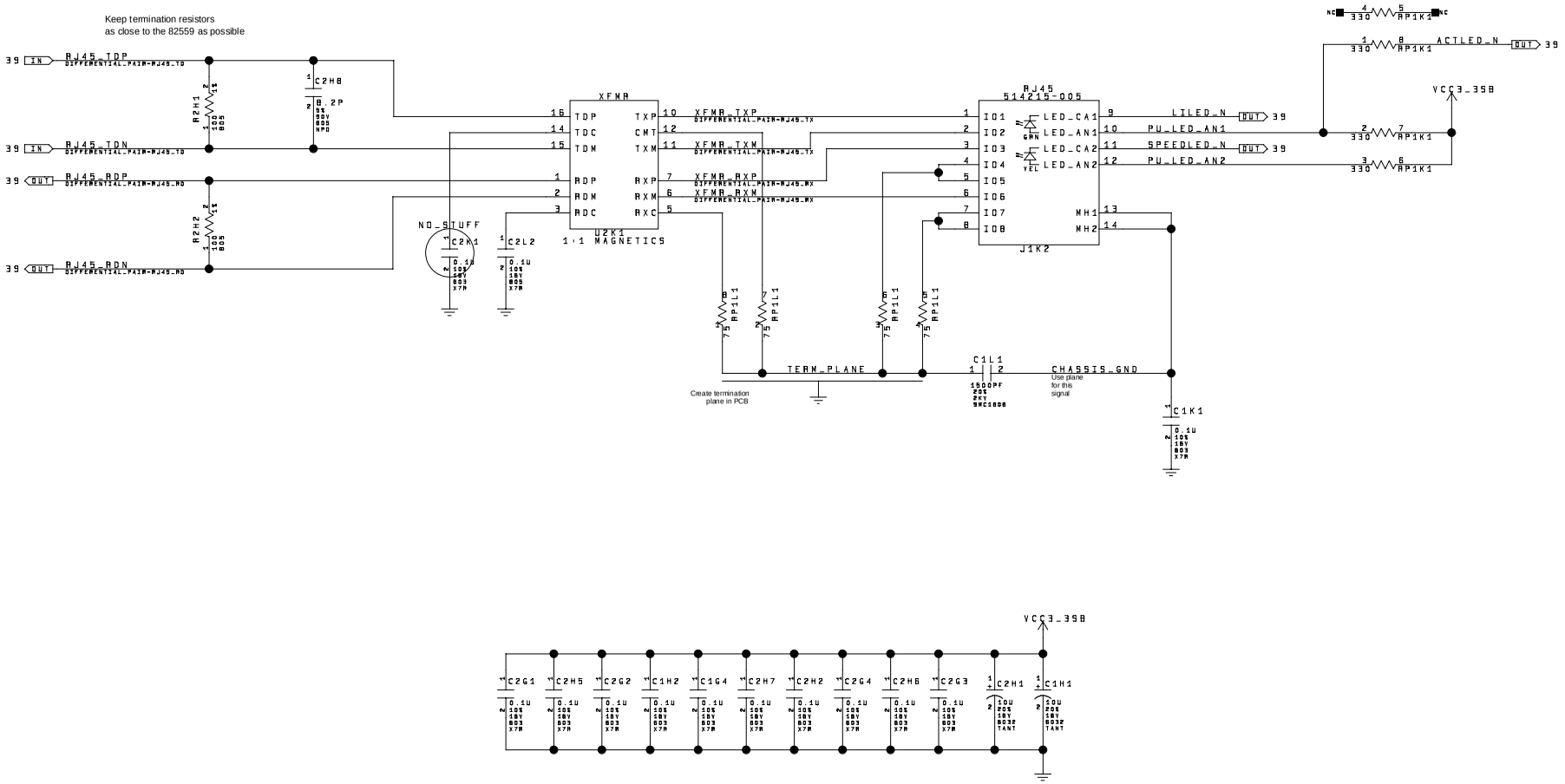
TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	38 OF 53



ETHERNET 82559ER

ROOM=82559

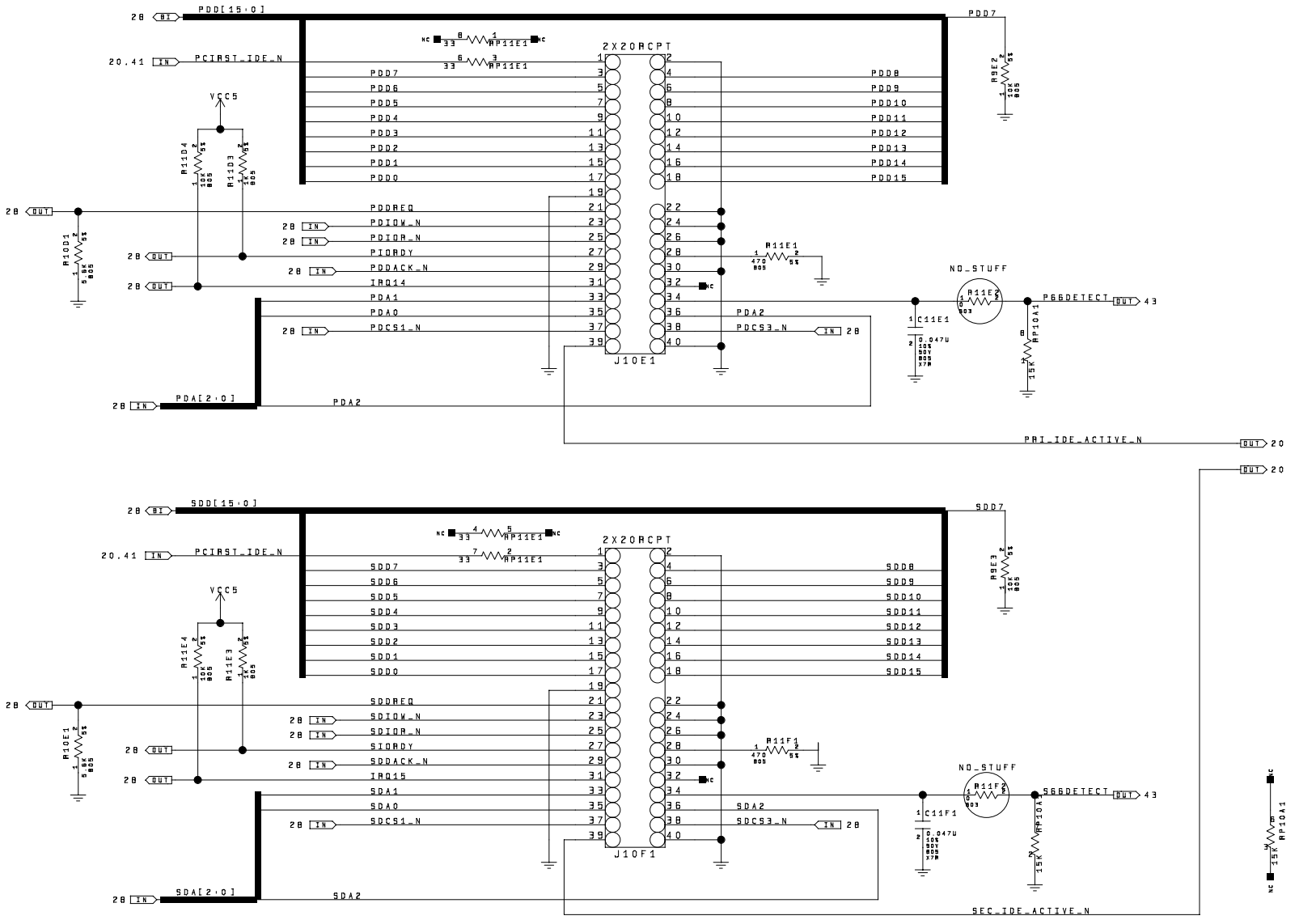
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	39 OF 53



ETHERNET CONNECTOR / DECOUPLING

ROOM=82559

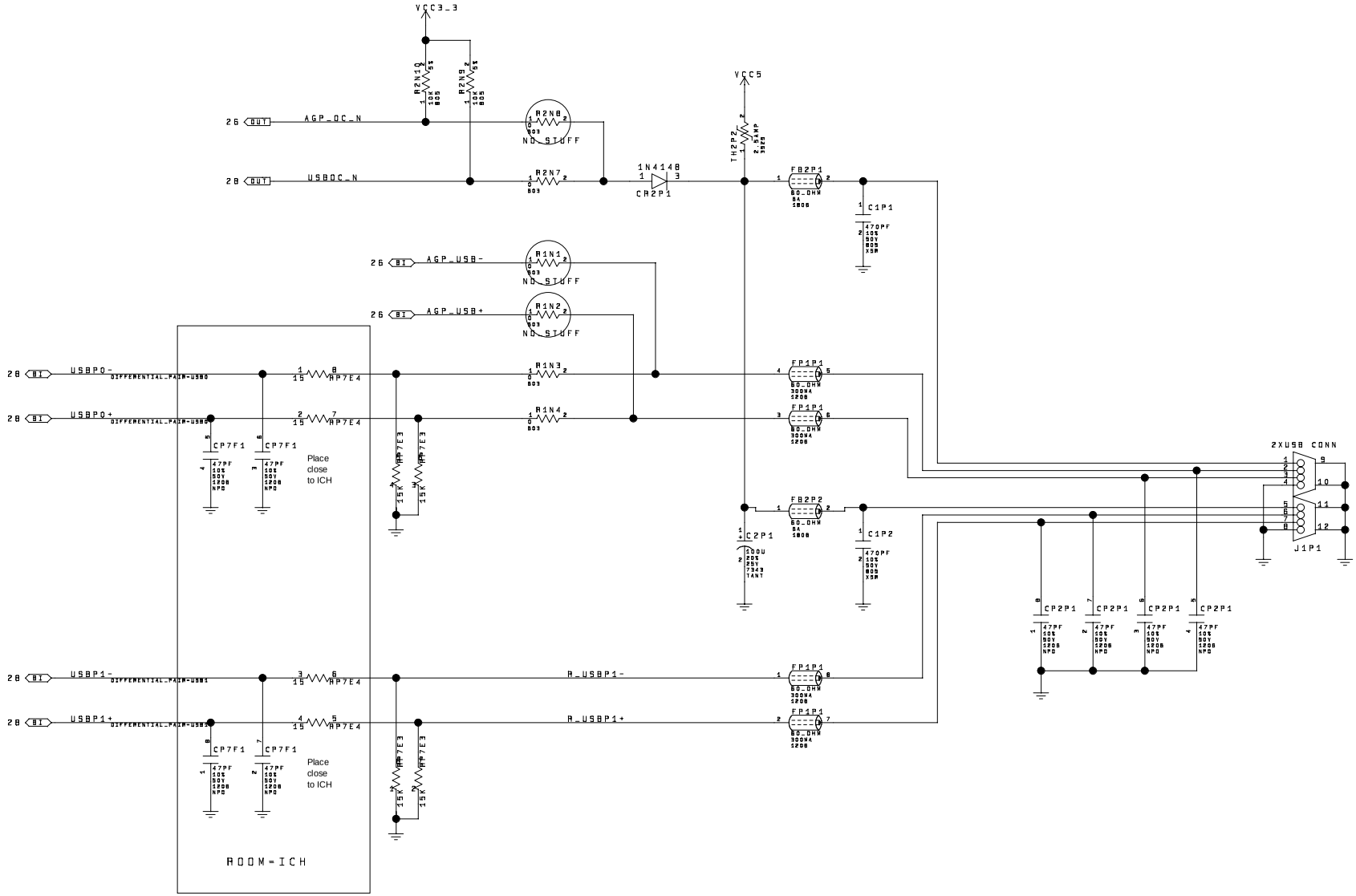
TITLE:		Rev: A
Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	40 OF 53



IDE CONNECTORS

ROOM=IDE_CONN

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	41 OF 53



USB CONNECTORS

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 5-12-2000_16:09
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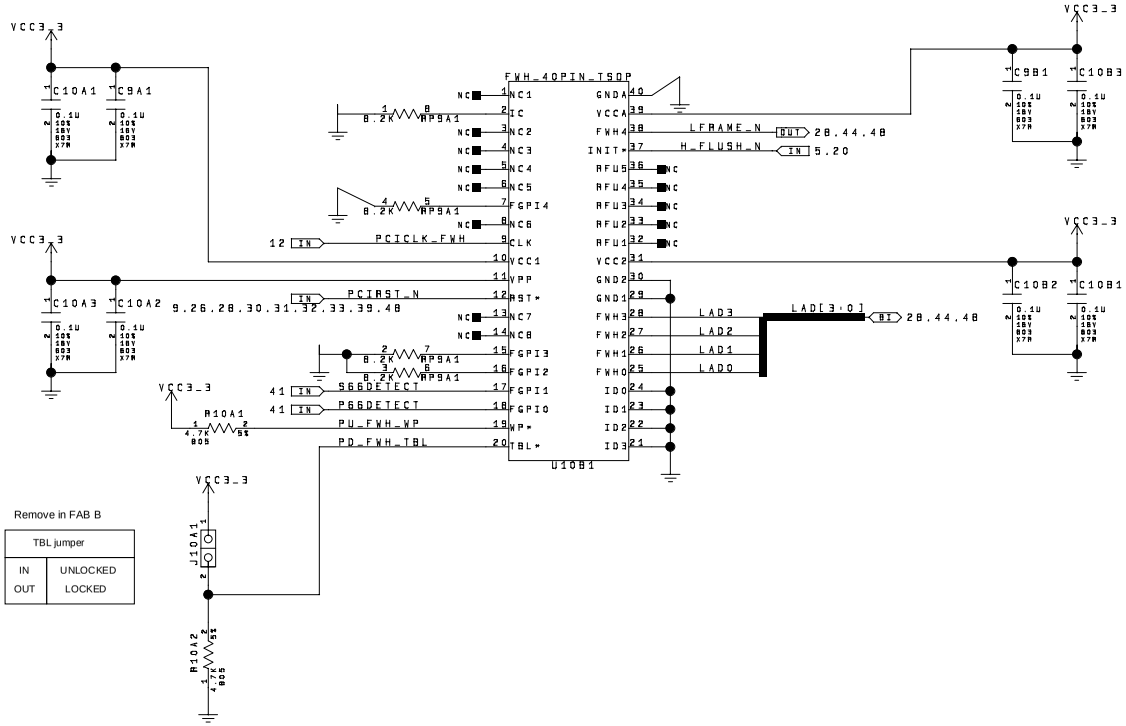


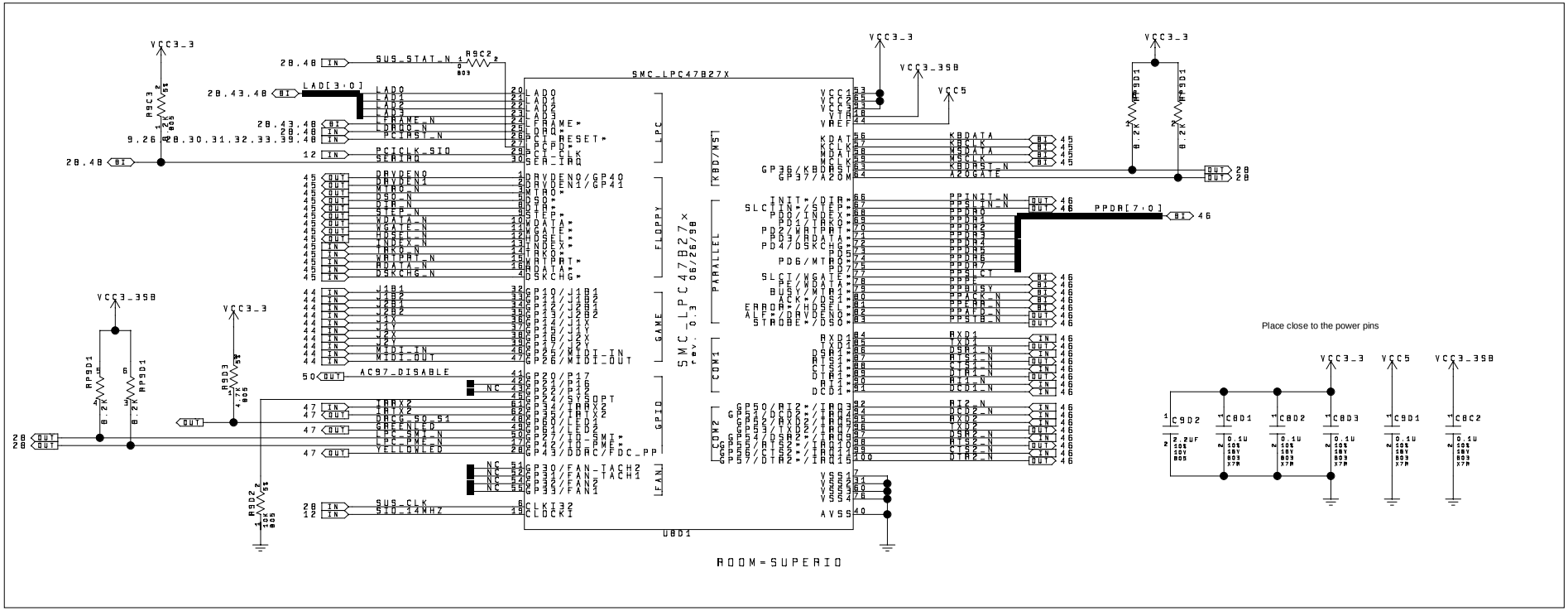
Remove in FAB B

TBL jumper	
IN	UNLOCKED
OUT	LOCKED

FWH

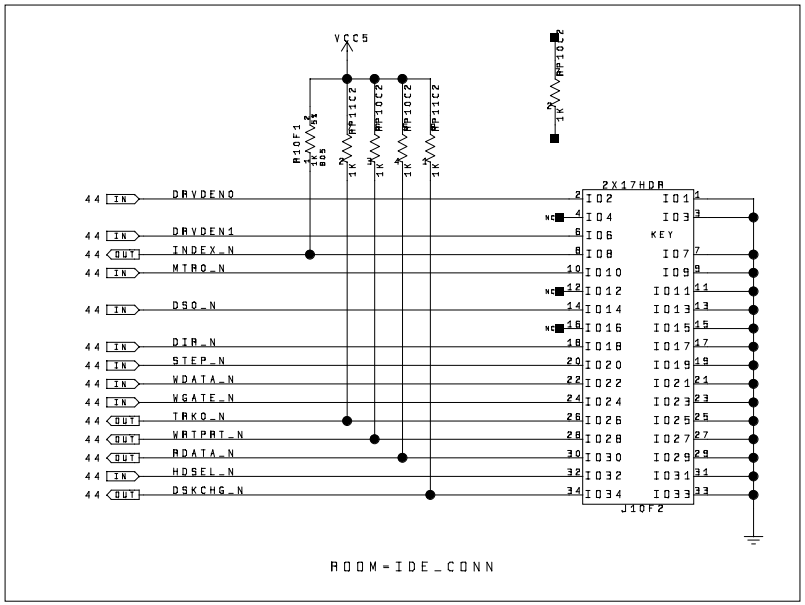
ROOM=FWH

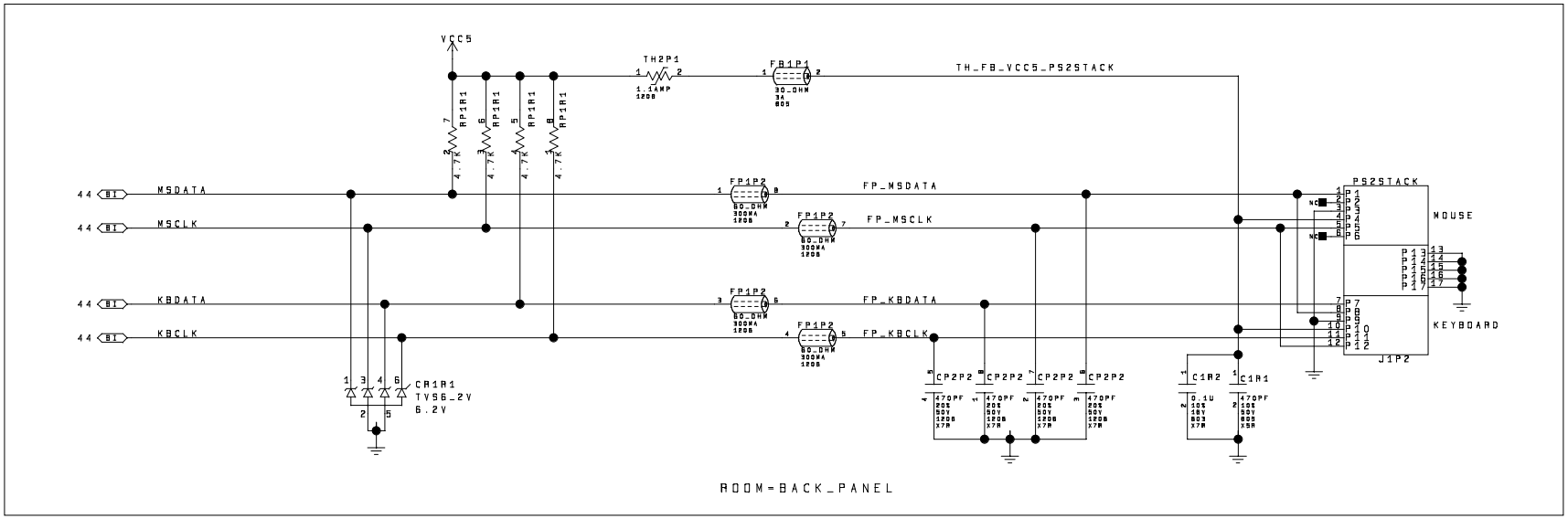
TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	43 OF 53



LPC SIO / GAMEPORT HEADER

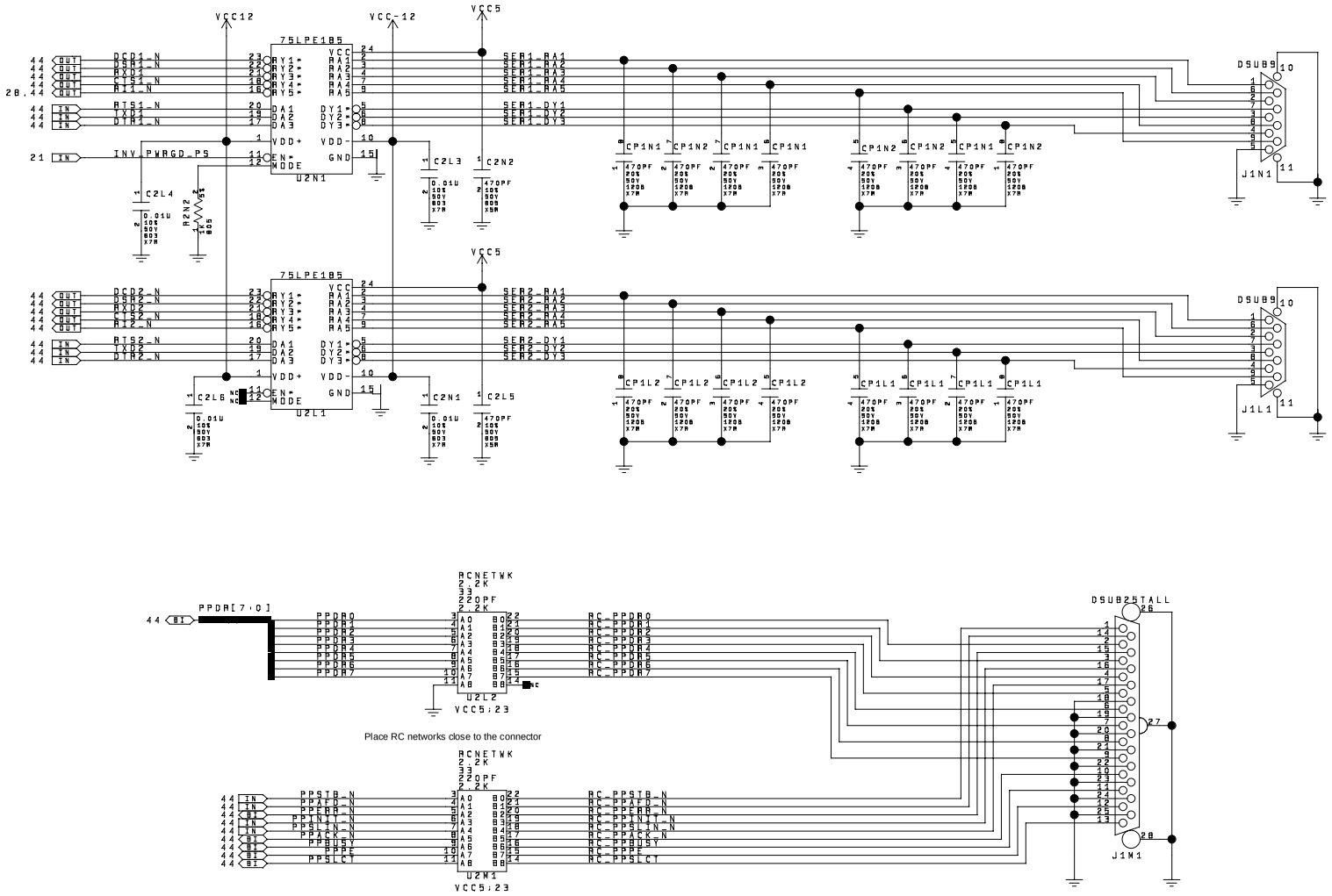
TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	44 OF 53





FLOPPY / KBD / MOUSE CONN

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	45 OF 53

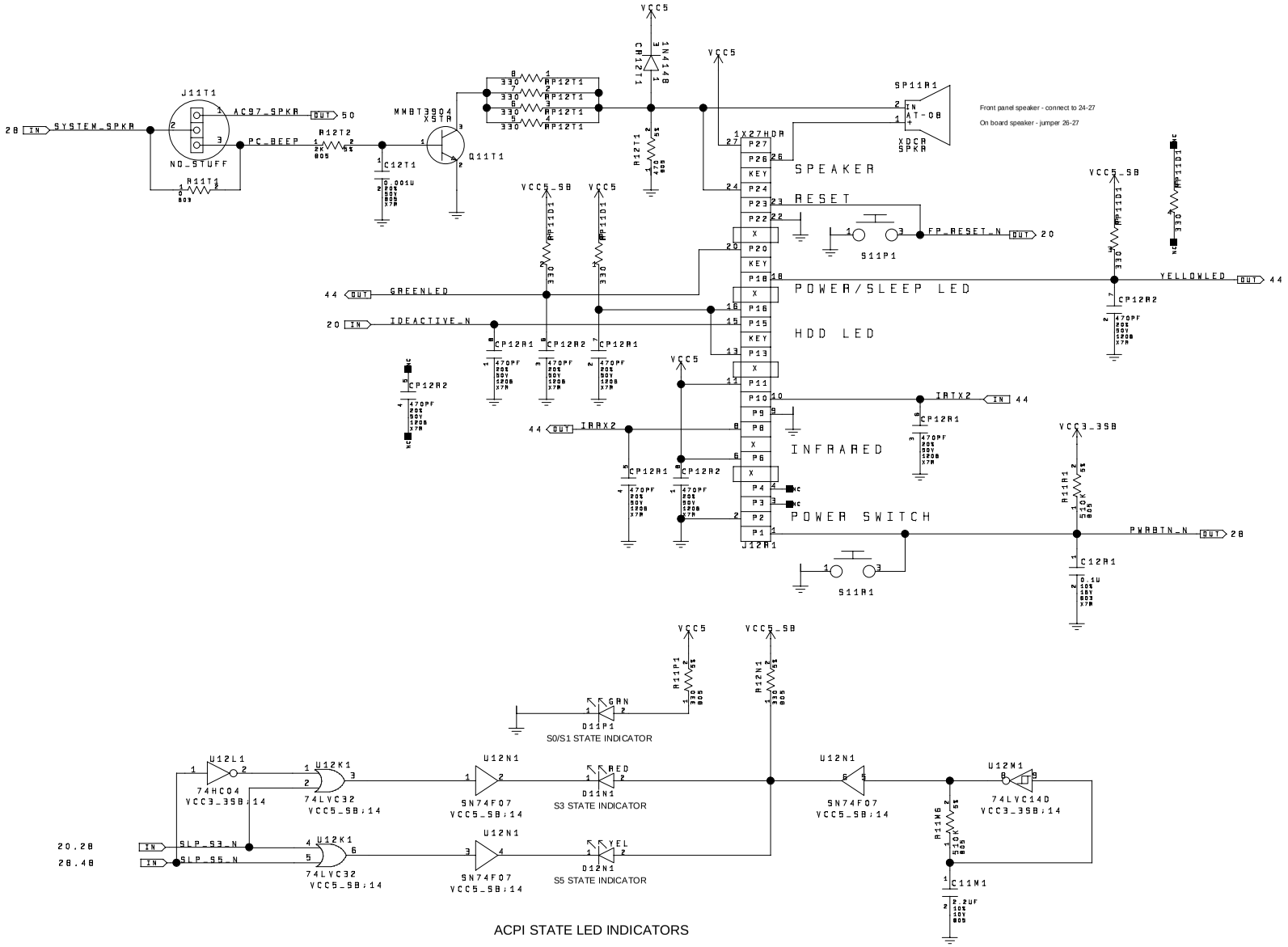


Place RC networks close to the connector

SERIAL / PARALLEL CONN

ROOM=BACK_PANEL

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	46 OF 53

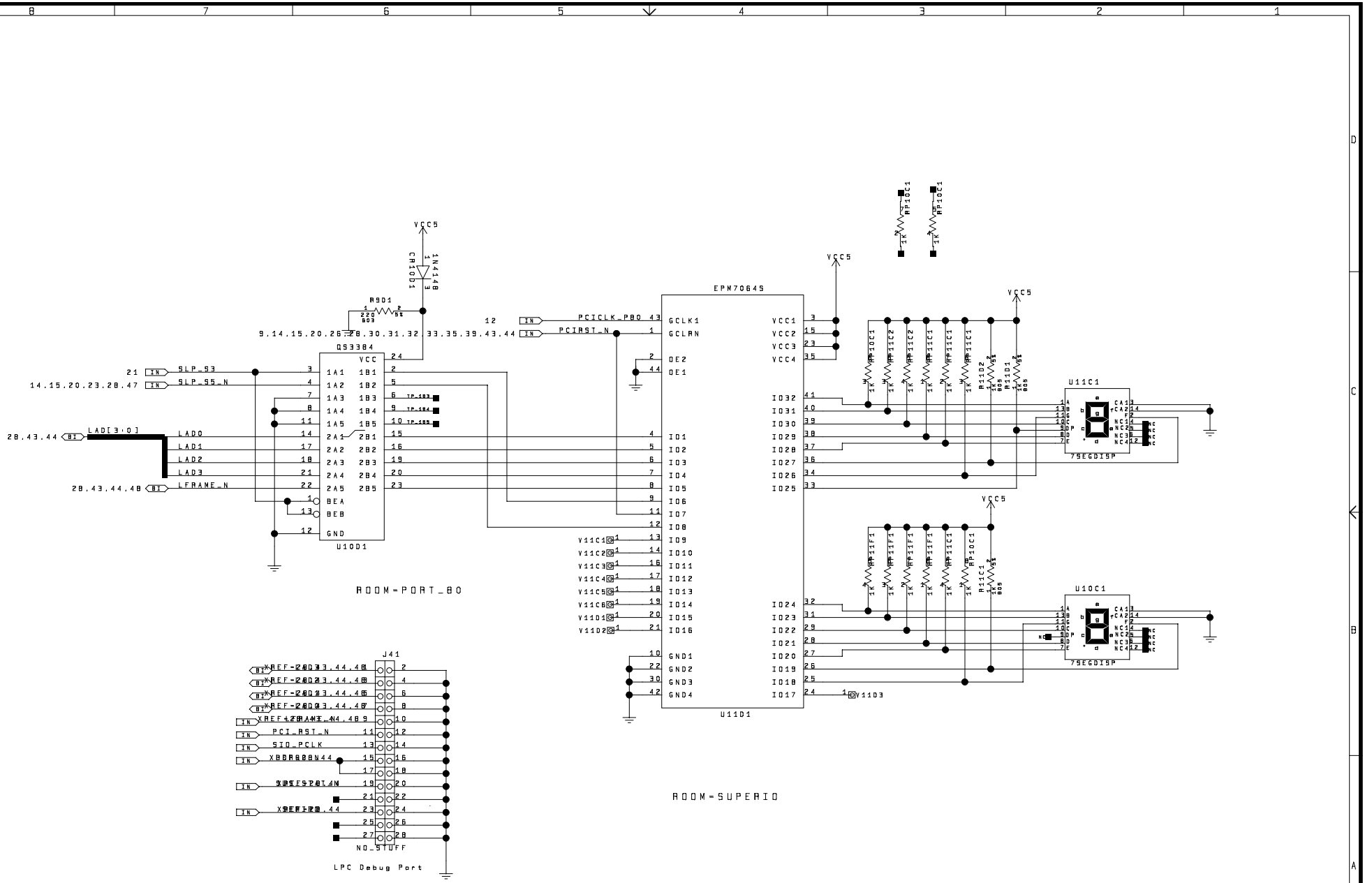


ACPI STATE LED INDICATORS

ROOM=FRONT_PANEL

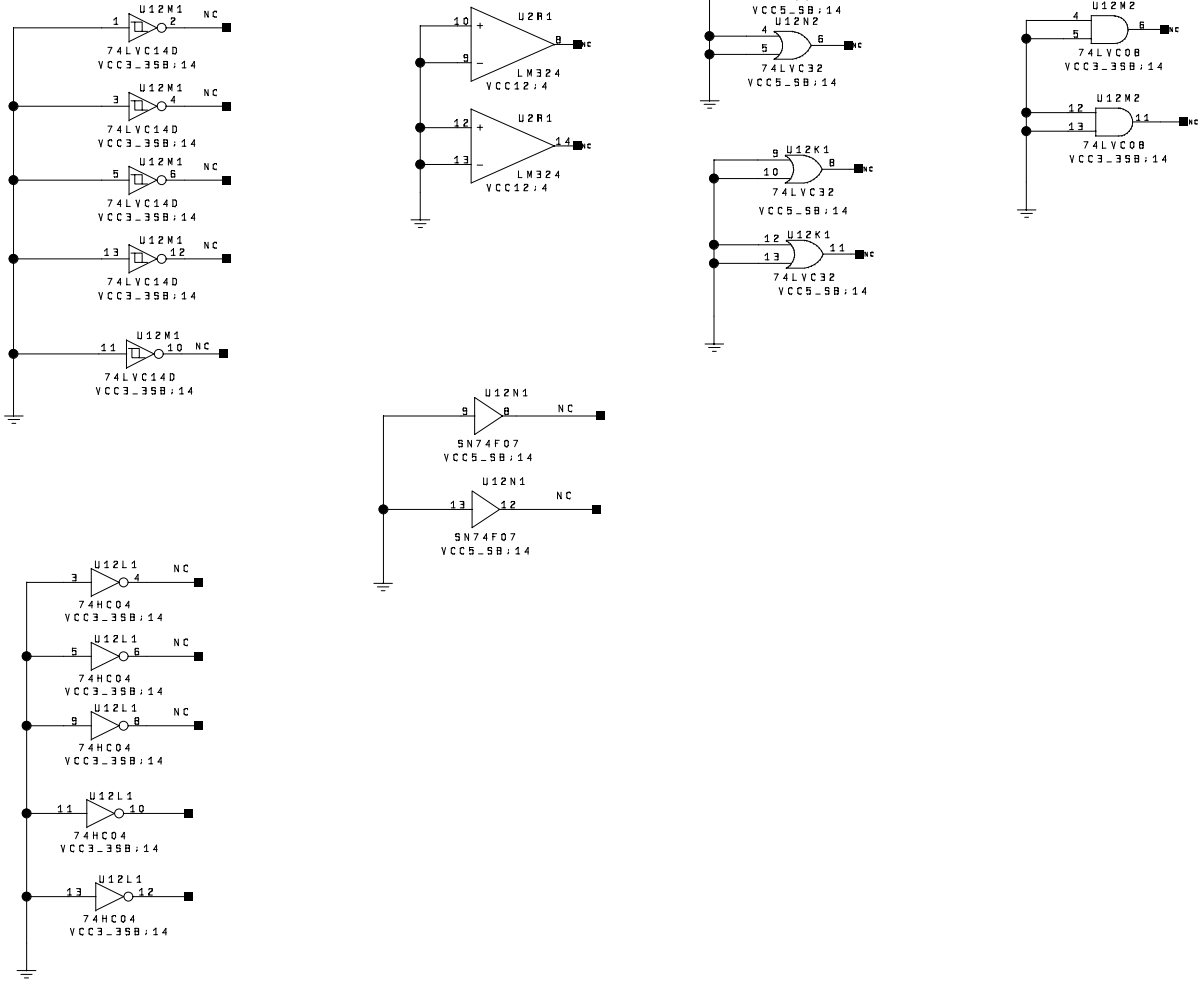
FRONT PANEL CONNECTOR / SPEAKER / ACPI LEDS

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	47 OF 53



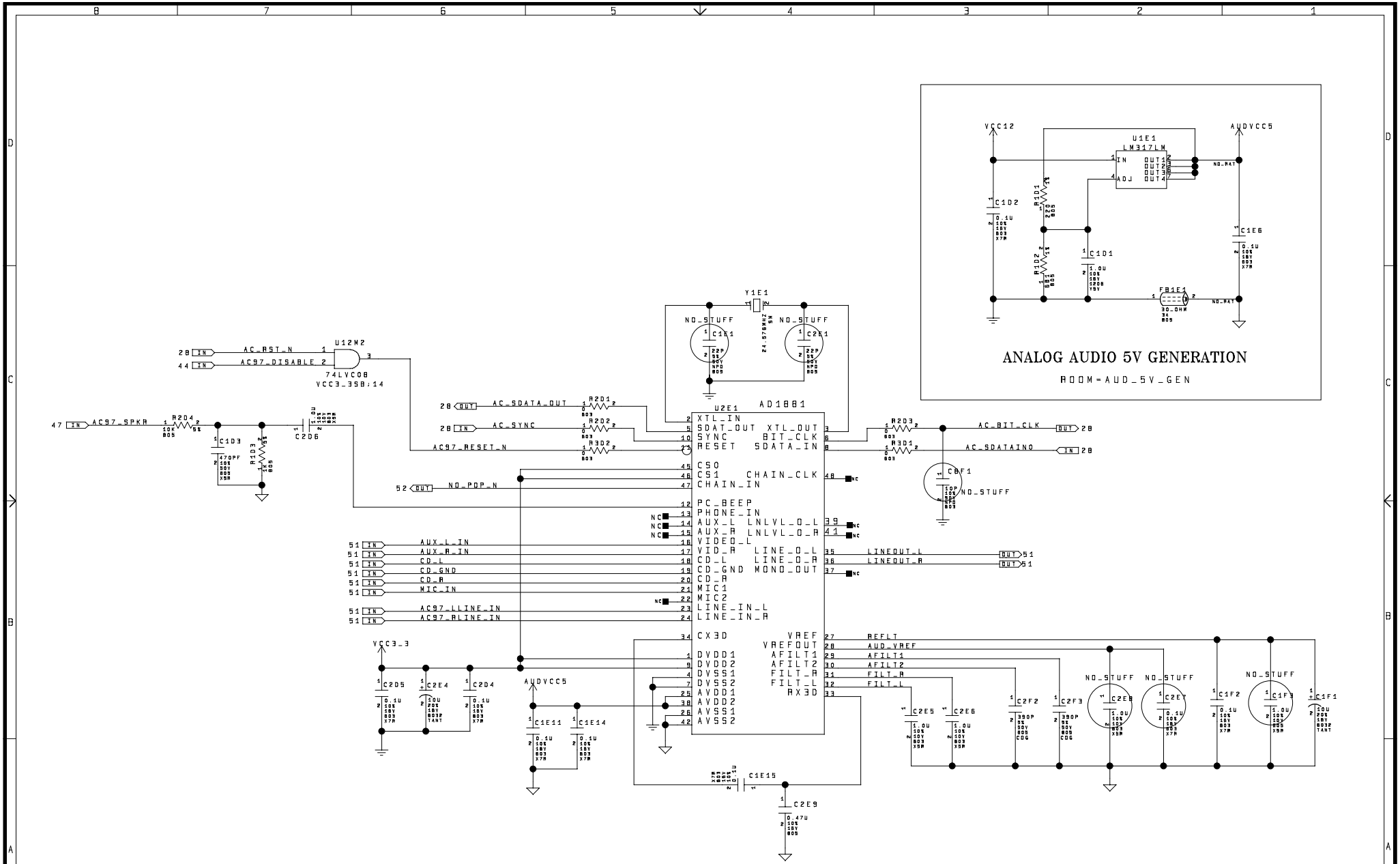
LPC / PORT 80 DISPLAY

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:09	48 OF 53



SPARE LOGIC

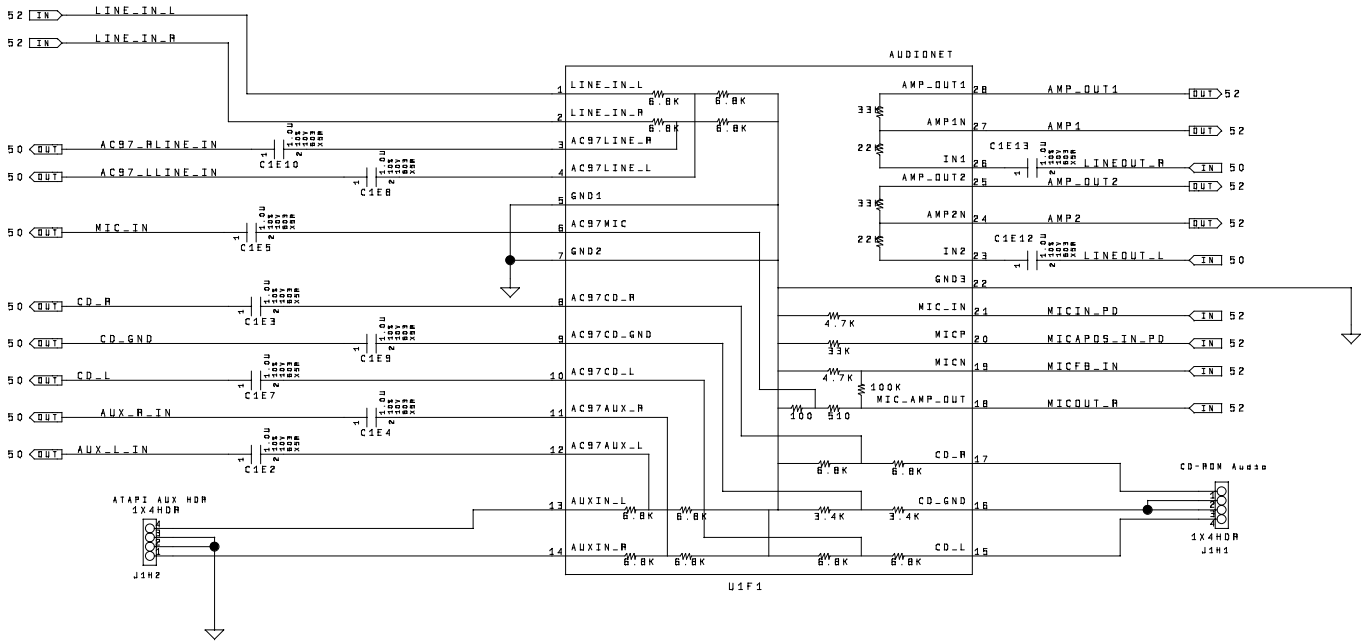
TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 5-12-2000_16:08	49 OF 53



AUDIO CODEC 97

ROOM=AUD_CODEC

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 5-12-2000_16:09	50 OF 53



AUDIO NET

ROOM=AUD_CODEC

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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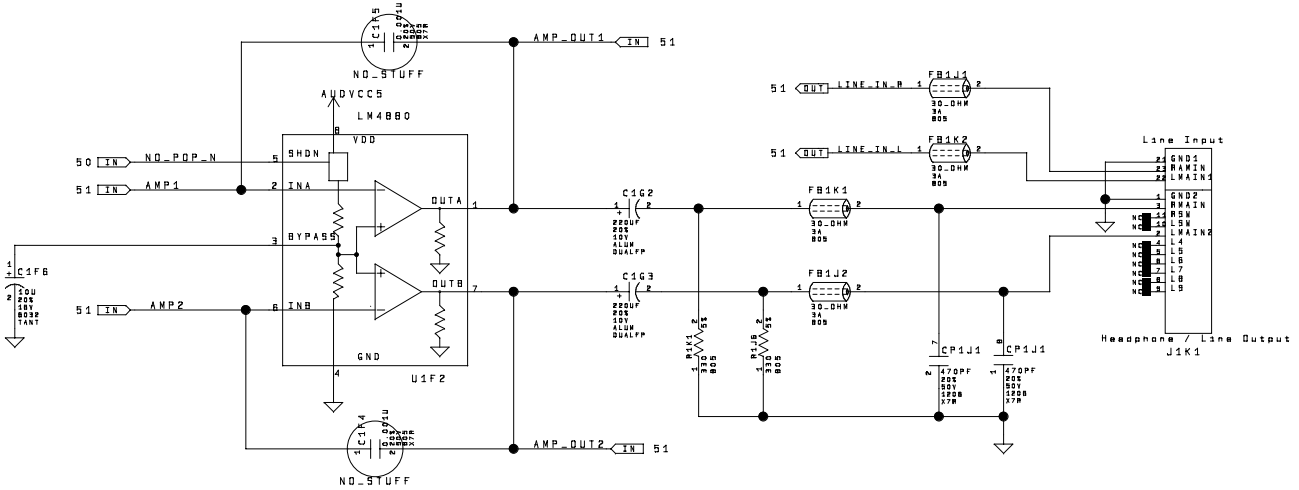

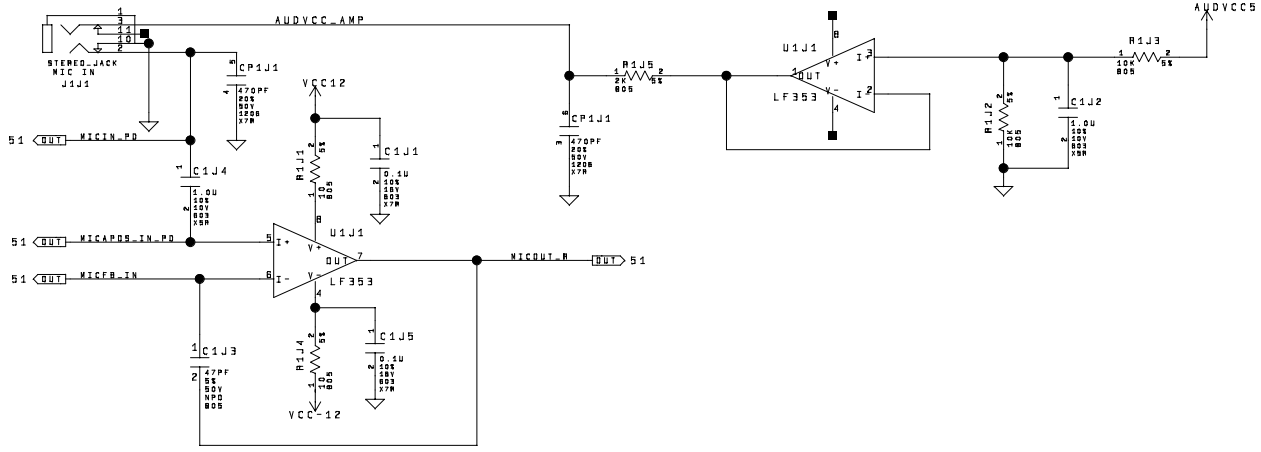

ROOM=BACK_PANEL

AUDIO LINE IN / LINE OUT / MIC IN

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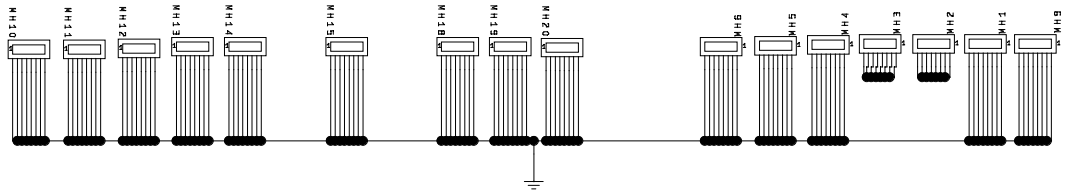

PCB MOUNTING HOLES

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