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Intel® 820 Chipset

Design Guide

July 2000

Intel® 820 Chipset Design Guide

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Revision History

Revision	Description	Date
-001	Initial Release.	November 1999
-002	• Added dual-processor schematics (Appendix B). • Uni-processor schematics have been updated (Appendix A). See the schematic revision history page at the end of Appendix A for details. - The following update is not in the schematic revision history. Cap C249 (schematic page 9) has been changed from 0.022 uF to 0.047 uF.	December 1999
-003	• Updated the text descriptions in the two paragraphs in Section 4.2.3, "MCH to DRCG". • Updated the first paragraph in Section 2.6.2.5, "RSL Signal Layer Alternation".	January 2000
-004	• Minor edits for clarity	July 2000

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Introduction

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Introduction 1

The Intel® 820 Chipset Design Guide provides design recommendations for systems using the Intel® 820 chipset. This includes motherboard layout and routing guidelines, system design issues and requirements, debug recommendations, and board schematics. The design recommendations should be used during system design. The guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

The Intel board schematics in Appendix A (uni-processor) and Appendix B (dual-processor) can be used as references for board designers. A feature list is provided at the beginning of each appendix. Although these schematics cover specific designs, the core schematics for each chipset component remains the same for most Intel® 820 chipset platforms. The appendices provides a set of reference schematics for each chipset component, in addition to common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. The design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- This chapter introduces the designer to the purpose and organization of this design guide, and provides a list of references of related documents. This chapter also provides an overview of the Intel® 820 chipset.

- Chapter 2, "Layout/Routing Guidelines"—This chapter provides a detailed set of motherboard layout and routing guidelines for designing an Intel® 820 chipset based platform. The motherboard functional units are covered (e.g., chipset component placement, system bus routing, system memory layout, display cache interface, hub interface, IDE, AC'97, USB, interrupts, SMBUS, PCD, LPC/FWH Flash BIOS, and RTC).

- Chapter 3, "Advanced System Bus Design"— AGTL+ guidelines and theory of operation are discussed. This chapter also provides more detail about the methodologies used to develop the guidelines.

- Chapter 4, "Clocking"— This chapter provides motherboard clocking guidelines (e.g., clock architecture, routing, capacitor sites, clock power decoupling, and clock skew).

- Chapter 5, "System Manufacturing"— This chapter includes board stackup requirements.

- Chapter 6, "System Design Considerations"— This chapter includes guidelines regarding power delivery, decoupling, thermal, and power sequencing.

- Appendix A, "Reference Board Schematics: Uni-Processor "— This appendix provides a set of schematics for Uni-processor designs. A feature list for the board design is also provided.

- Appendix B, "Reference Board Schematics: Dual-Processor "— This appendix provides a set of schematics for dual-processor designs. A feature list for the board design is also provided.

1.2 References

- *Intel® 820 Chipset: Intel® 82820 Memory Controller Hub (MCH)* Datasheet (Order Number: 290630)
- *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet (Order Number: 290655)
- *Intel® 82802AB/82802AC FirmWare Hub (FWH)* Datasheet (Order Number: 290658)
- *Pentium® II Processor AGTL+ Guidelines* (Order Number: 243330)
- *Pentium® II Processor Power Distribution Guideline (*Order Number: 243332)
- *Pentium® II Processor Developer's Manual* (Order Number: 243341)
- *Pentium® III Processor Specification Update* (latest off of website)
- *AP 907 Pentium III processor Power Distribution Guidelines* (Order Number 245085)
- *AP-585 Pentium II Processor AGTL+ Guidelines* (Order Number: 243330)
- *AP-587 Pentium II Processor Power Distribution Guidelines* (Order Number: 243332)
- *CK97 Clock Synthesizer Design Guidelines* (Order Number 243867)
- *PCI Local Bus Specification*, Revision 2.2
- *Universal Serial Bus Specification*, Revision 1.0
- *VRM 8.4 DC-DC Converter Design Guidelines* (when available)

1.3 System Overview

The Intel® 820 chipset is the third generation desktop chipset designed for Intel's SC242 architecture and the first chipset to support the 4X capability of the AGP 2.0 Interface Specification and 400 MHz Direct RDRAM. The 400 MHz, 16 bit, *double clocked* Direct RDRAM interface provides 1.6 GB/s access to main memory. A new chipset component interconnect, the hub interface, is designed into the Intel® 820 chipset to provide more efficient communication between chipset components.

Support of AGP 4X, 400 MHz Direct RDRAM and the hub interface provides a balanced system architecture for the Pentium III processor, minimizing bottlenecks and increasing system performance. By increasing memory bandwidth to 1.6 GB/s through the use of 400 MHz Direct RDRAM and increasing graphics bandwidth to 1 GB/s through the use of AGP 4X, the Intel® 820 chipset delivers the data throughput necessary to take advantage of the high performance provided by the powerful Pentium III processor.

In addition, the Intel® 820 chipset architecture enables a new security and manageability infrastructure through the Firmware Hub component.

The ACPI compliant Intel® 820 chipset platform can support the *Full-on, Stop Grant, Suspend to RAM, Suspend to Disk,* and *Soft-off* power management states. Through the use of an appropriate LAN device, Intel® 820 chipset also supports *Wake on LAN** for remote administration and troubleshooting.

The Intel® 820 chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of Intel chipsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the Intel® 820 chipset platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software*

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configurable AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices. The ISA bus can be implemented through the use of the optional 82380AB PCI-ISA bridge.

The Intel® 820 chipset contains two *core* components: the Memory Controller Hub (MCH) and the I/O Controller Hub (ICH). The MCH integrates the 133 MHz processor system bus controller, AGP 2.0 controller, 400 MHz Direct RDRAM controller and a high-speed hub interface for communication with the ICH. The ICH integrates an UltraATA/66 controller, USB host controller, LPC interface controller, FWH Flash BIOS interface controller, PCI interface controller, AC'97 digital controller and a hub interface for communication with the MCH. The Intel® 820 chipset provides the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the system bandwidth necessary to obtain peak performance with the Pentium lll processor.

1.3.1 Chipset Components

This section provides an overview of the 82820 Memory Controller Hub (MCH) and the 82801AA I/O Controller Hub (ICH). Additional functionality can be provided using the 82380AB PCI-ISA bridge.

Memory Controller Hub (MCH)

The MCH provides the interconnect between the Direct RDRAM and the system logic. It integrates the following functions:

- Support for single or dual SC242 processors with 100 MHz or 133 MHz System Bus

- 256 MHz, 300 MHz, 356 MHz or 400 MHz Direct RDRAM interface supporting 1 GB of Direct RDRAM

- 4X, 1.5V AGP interface (3.3V 1X, 2X and 1.5V 1X, 2X devices also supported)

- Downstream hub interface for access to the ICH

In addition, the MCH provides arbitration, buffering and coherency management for each of these interfaces. Refer to Chapter 2, "Layout/Routing Guidelines" for more information regarding these interfaces.

I/O Controller Hub (ICH)

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH integrates the following functions:

- Upstream hub interface for access to the MCH
- 2 channel Ultra ATA/66 Bus Master IDE controller
- USB controller
- I/O APIC
- SMBus controller
- FWH interface (FWH Flash BIOS)
- LPC interface
- AC'97 2.1 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Alert on LAN*

The ICH also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces. Refer to Chapter 2, "Layout/Routing Guidelines" for more information on these interfaces.

ISA Bridge (82380AB)

For legacy needs, ISA support is an optional feature of the Intel® 820 chipset. Implementations that require ISA support can benefit from the enhancements of the Intel® 820 chipset while "ISA-less" designs are not burdened with the complexity and cost of the ISA subsystem.

The Intel® 820 chipset platform with optional ISA support takes advantage of the 82380AB ISA bridge. The bridge is a PCI to ISA bridge and resides on the PCI bus of the ICH.

1.3.2   Bandwidth Summary

Table 1-1 provides a summary of the bandwidth requirements for the Intel® 820 chipset.

Table 1-1. Intel® 820 Chipset Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bytes)	Bandwidth (MB/s)
Processor Bus	133	1	133	8	1066
RDRAM	266/300/356/400	2	533/600/711/800	2	1066/1200/1422/1600
AGP 2.0	66	4	266	4	1066
Hub Interface	66	4	266	1	266
PCI 2.2	33	1	33	4	133

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1.3.3   System Configuration

The following figures show typical platform configurations using the Intel® 820 chipset.

Figure 1-1. Intel® 820 Chipset Platform Performance Desktop Block Diagram
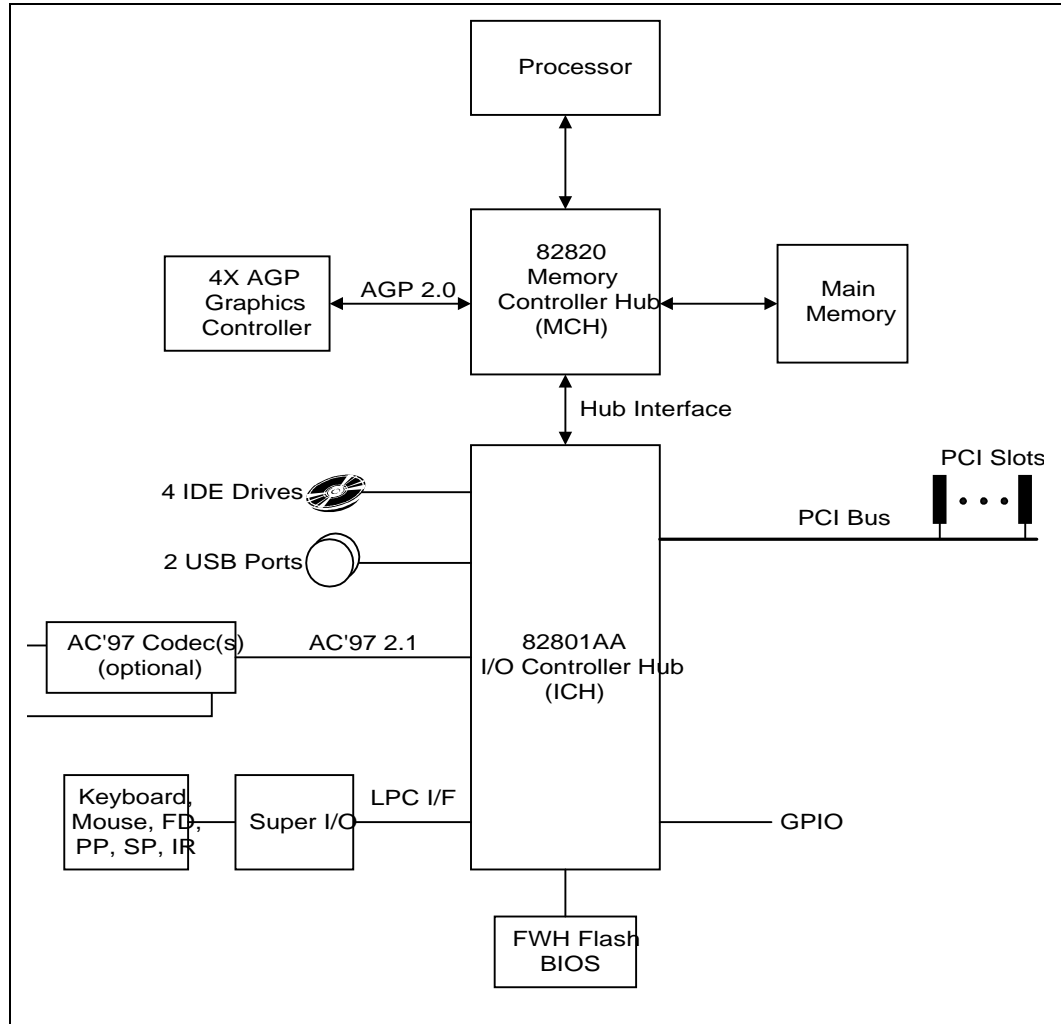
Figure 1-2. Intel® 820 Chipset Platform Performance Desktop Block Diagram (with ISA Bridge)
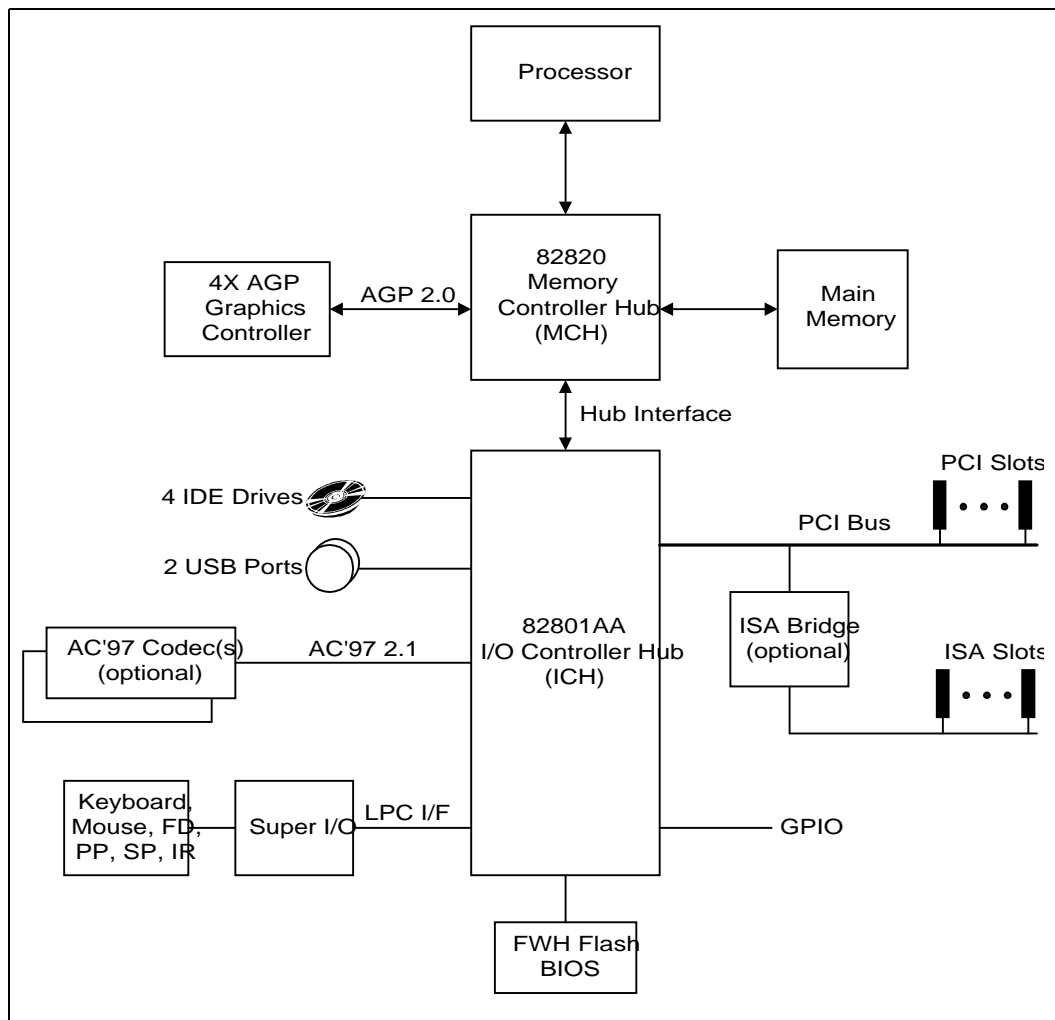
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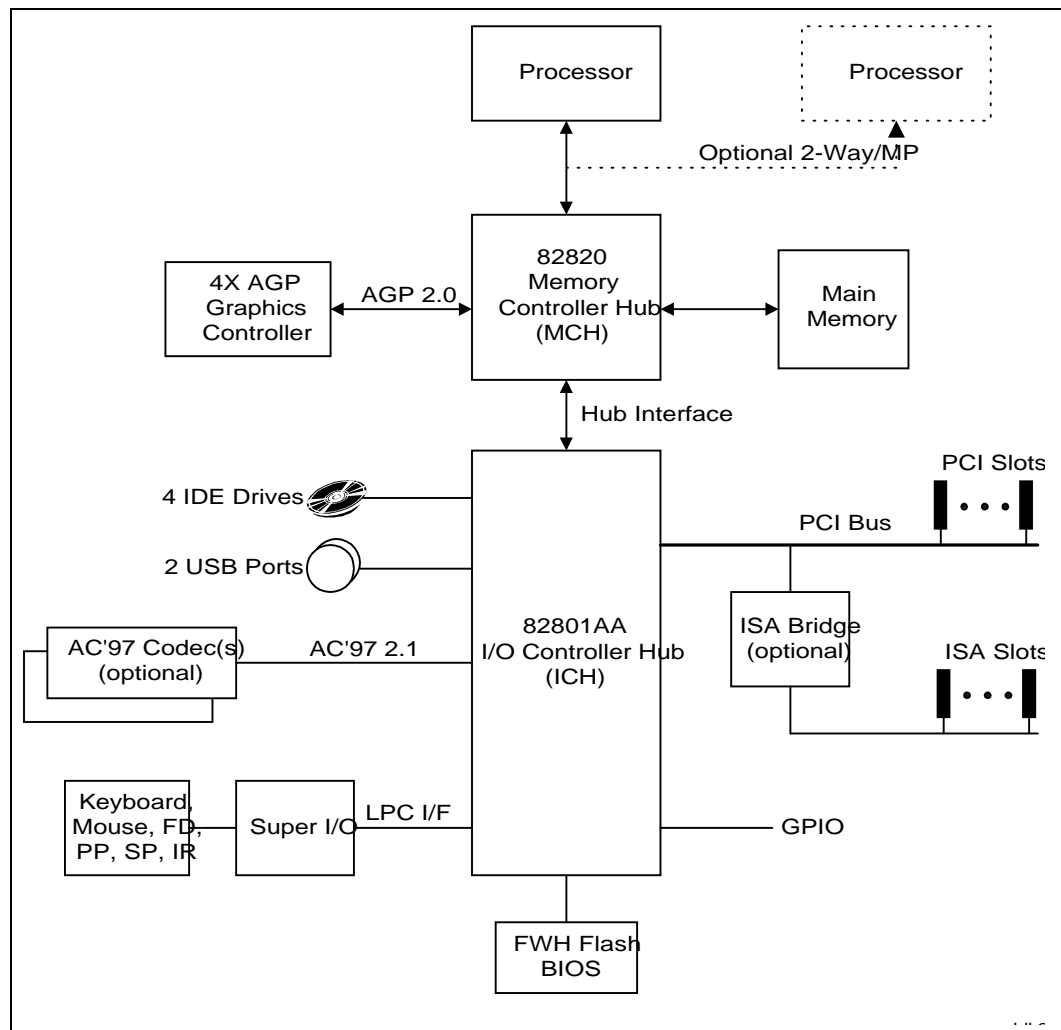
1.4 Platform Initiatives

1.4.1 Direct Rambus[*]

The Direct Rambus[*] (RDRAM) initiative provides the memory bandwidth necessary to obtain optimal performance from the Pentium III processor as well as a high-performance AGP graphics controller. The MCH RDRAM interface supports 266 MHz, 300 MHz, 356 MHz, and 400 MHz operation; the latter delivers 1.6 GB/s of theoretical memory bandwidth; twice the memory bandwidth of 100 MHz SDRAM systems. Coupled with the greater bandwidth, the RDRAM protocol, which is heavily pipelined, provides substantially more efficient data transfer. The RDRAM memory interface can achieve greater than 95% utilization of the 1.6 GB/s theoretical maximum bandwidth.

In addition to RDRAM's performance features, the new memory architecture provides enhanced power management capabilities. The *powerdown* mode of operation enables Intel® 820 chipset based systems to cost-effectively support *suspend-to-RAM*.

1.4.2 Streaming SIMD Extensions

The Pentium III processor provides 70 new Streaming SIMD (single instruction, multiple data) Extensions. The Pentium III new extensions are floating point SIMD extensions. Intel MMX™ technology provides integer SIMD extensions. The Pentium III processor new extensions complement the Intel MMX™ technology SIMD extensions and provide a performance boost to floating-point intensive 3D applications.

1.4.3 AGP 2.0

The AGP 2.0 interface, along with Direct Rambus[*] memory technology, allows graphics controllers to access main memory at over 1 GB/s; twice the AGP bandwidth of previous AGP platforms. AGP 2.0 provides the infrastructure necessary for *photorealistic 3D.* In conjunction with Direct Rambus[*] and the Pentium III processor new Streaming SIMD Extensions, AGP 2.0 delivers the next level of 3D graphics performance.

1.4.4 Hub Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC'97 and ATA/66, coupled with the existing USB, I/O requirements will begin to impact PCI bus performance. The Intel® 820 chipset's hub interface architecture ensures that the I/O subsystem, both PCI and the integrated I/O features (IDE, AC'97, USB, etc.), receives adequate bandwidth. By placing the I/O bridge on the hub interface instead of PCI, the hub architecture ensures that both the I/O functions integrated into the ICH and the PCI peripherals obtain the bandwidth necessary for peak performance. In addition, the hub interface's lower pin count allows a smaller package for the MCH and ICH.

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1.4.5 Manageability

The Intel® 820 chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

CPU Present Indicator

The ICH looks for the CPU to fetch the first instruction after reset. If the CPU does not fetch the first instruction, the ICH will reboot the system at the *safe-mode* frequency multiplier.

ECC Error Reporting

Upon detecting an ECC error, the MCH can send one of several messages to the ICH. The MCH can instruct the ICH to generate either an SMI#, NMI#, SERR#, or TCO interrupt.

Function Disable

The ICH provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect

The ICH provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The ICH can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

SMBus

The ICH integrates an SMBus controller. The SMBus provides an interface to manage peripherals (e.g., serial presence detection (SPD) on RIMMs and thermal sensors).

Alert on LAN*

The ICH supports Alert on LAN*. In response to a TCO event (intruder detect, thermal event, CPU not booting) the ICH sends a message over ALERTCLK and ALERTDATA. A LAN controller can decode this alert message and send a message over the network to alert the network manager.

1.4.6   AC'97

The *Audio Codec'97* (AC'97) Specification defines a digital link that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and an MC. The AC'97 Specification defines the interface between the system logic and the audio or modem codec known as the *AC'97 Digital Link*.

The ability to add cost-effective audio and modem solutions is important as the platform migrates away from ISA. In addition, the AC'97 audio and modem components are software configurable. This reduces configuration errors. Intel® 820 chipset's AC'97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC'97 digital link. Using Intel® 820 chipset's integrated AC'97 digital link reduces cost and eases migration from ISA.

By using an audio codec, the AC'97 digital link allows for cost-effective, high-quality, integrated audio on the Intel® 820 chipset platform. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC'97. Intel® 820 chipset's integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec (Figure 1-4a) or a modem with a modem codec (Figure 1-4b). For systems requiring both audio and a modem, there are two solutions. The audio codec and the modem codec can be integrated into a single Audio Modem Codec (AMC) (Figure 1-4c), or separate audio and modem codecs can be connected to the ICH (Figure 1-4d).

Modem implementation for different countries must be considered as telephone systems may vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the ICH is AC'97 Rev. 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

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Figure 1-4. (a-d) AC'97 Connections
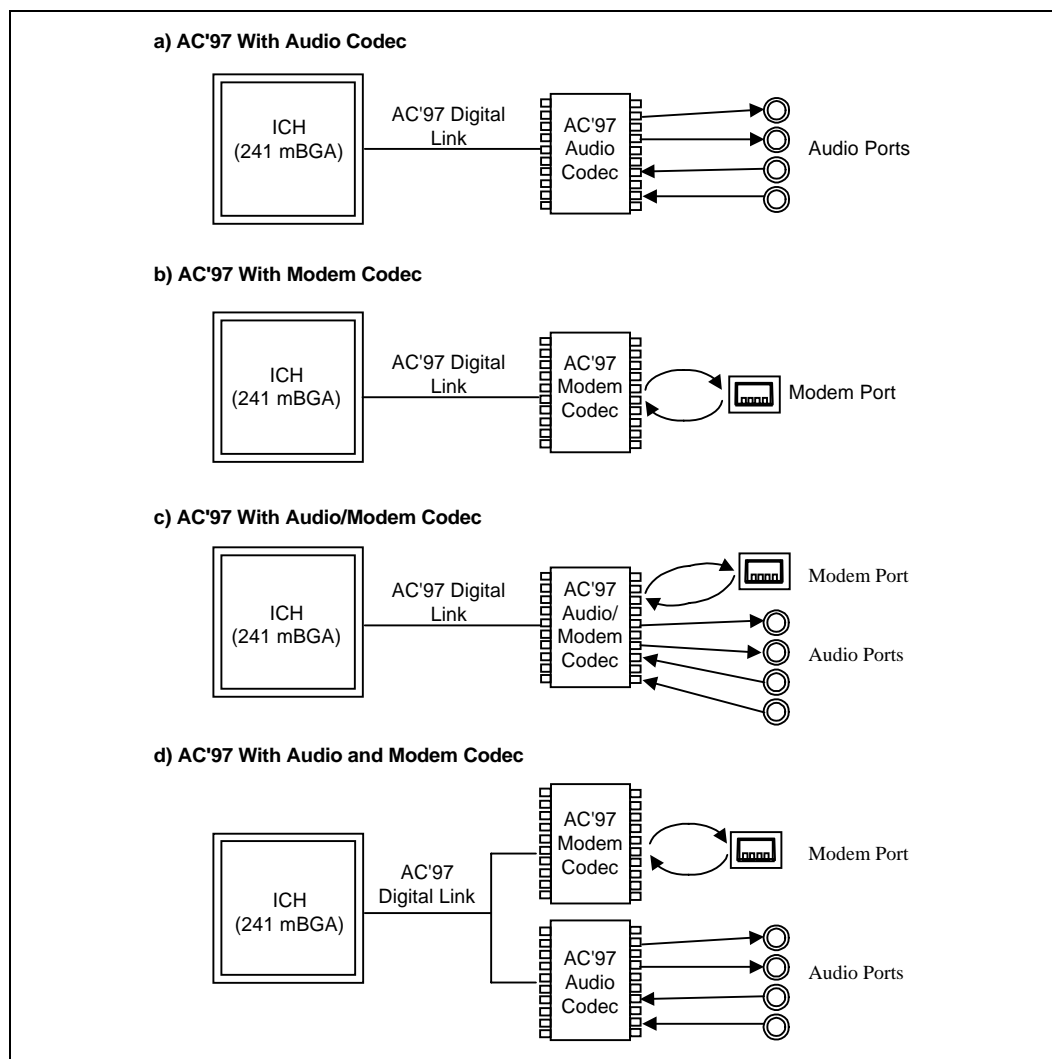
1.4.7 Low Pin Count (LPC) Interface

In the Intel® 820 chipset platform, the super I/O component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost super I/O designs. The LPC super I/O component requires the same feature set as traditional super I/O components. It should include a keyboard and mouse controller, floppy disk controller and serial and parallel ports. In addition to the super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your super I/O vendor for a comprehensive list of devices offered and features supported.

In addition, depending on system requirements, a device bay controller and USB hub could be integrated into the LPC super I/O component. For systems requiring ISA support, an ISA-IRQ to serial-IRQ converter is required. Potentially, this converter could be integrated into the super I/O.

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Layout and Routing Guidelines

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Layout/Routing Guidelines 2

This chapter documents motherboard layout and routing guidelines for Intel® 820 chipset based systems. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

Caution: **If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design.** Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely. **Any deviation from these guidelines must be simulated!**

2.1 General Recommendations

The trace impedance typically noted (i.e., $60\ \Omega \pm 10\%$) is the "nominal" trace impedance. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. In addition, the PCB should be fabricated as documented in Section 5.3, "Stackup Requirement" on page 5-1 of this document.

All recommendations in this section (except where noted) assume 5 mil wide traces. If trace width is greater than 5 mils then the trace spacing requirements must be adjusted accordingly (linearly). For example, this section recommends routing most AGP signals with 5 mil traces on 20 mil spaces (1:4). If 6 mil traces are used, then 24 mil spaces must be used (also 1:4). Using a wider trace (and therefore wider spaces) will make routing more difficult.

Additionally, these routing guidelines are created using the *stack-up* described in section Section 5.3, "Stackup Requirement" on page 5-1. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

2.2 Component Quadrant Layout

The quadrant layouts shown are approximate and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

Figure 2-1. MCH 324-uBGA Quadrant Layout (Top View)
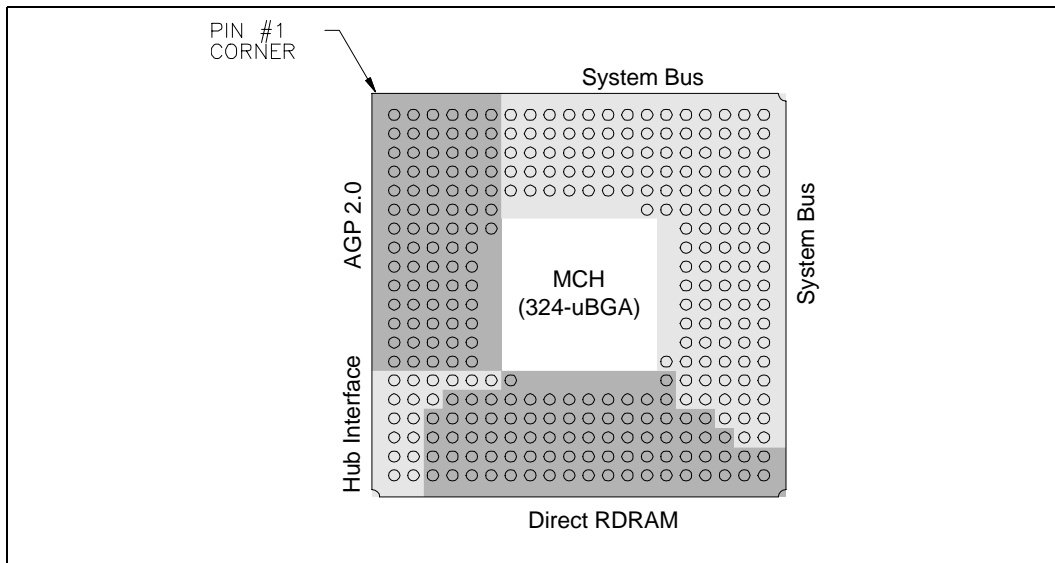
Figure 2-2. ICH 241-uBGA Quadrant Layout (Top View)
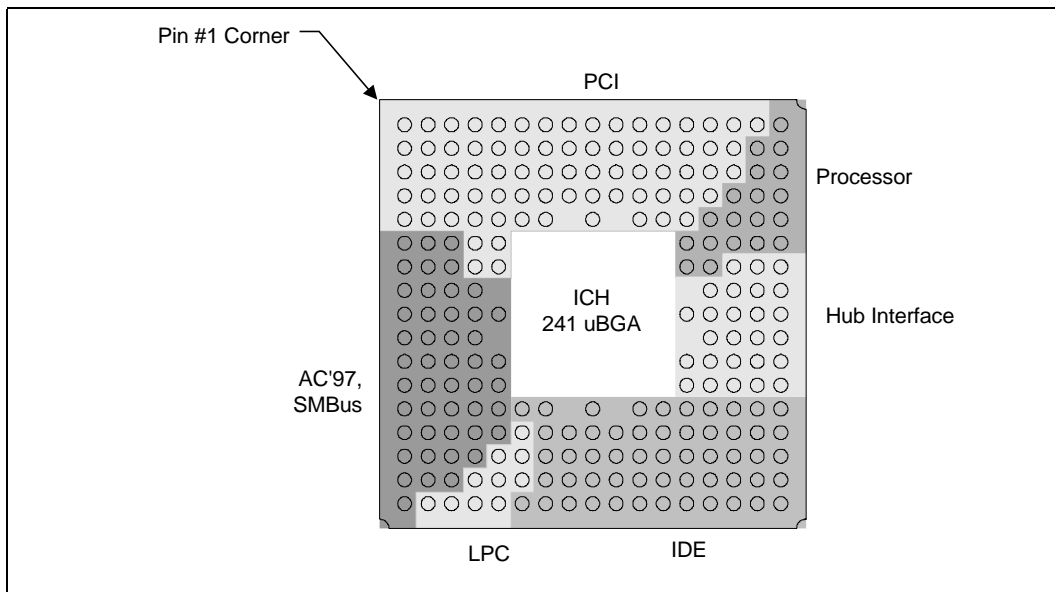
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2.3   Intel® 820 Chipset Component Placement

Notes:

1. The ATX placements and layouts shown in Figure 2-3 is recommended for single (UP) Intel® 820 chipset based system design.

2. The trace length limitation between critical connections will be addressed later in this document.

3. The figure is for *reference only.*

Figure 2-3. Sample ATX MCH/ICH Component Placement
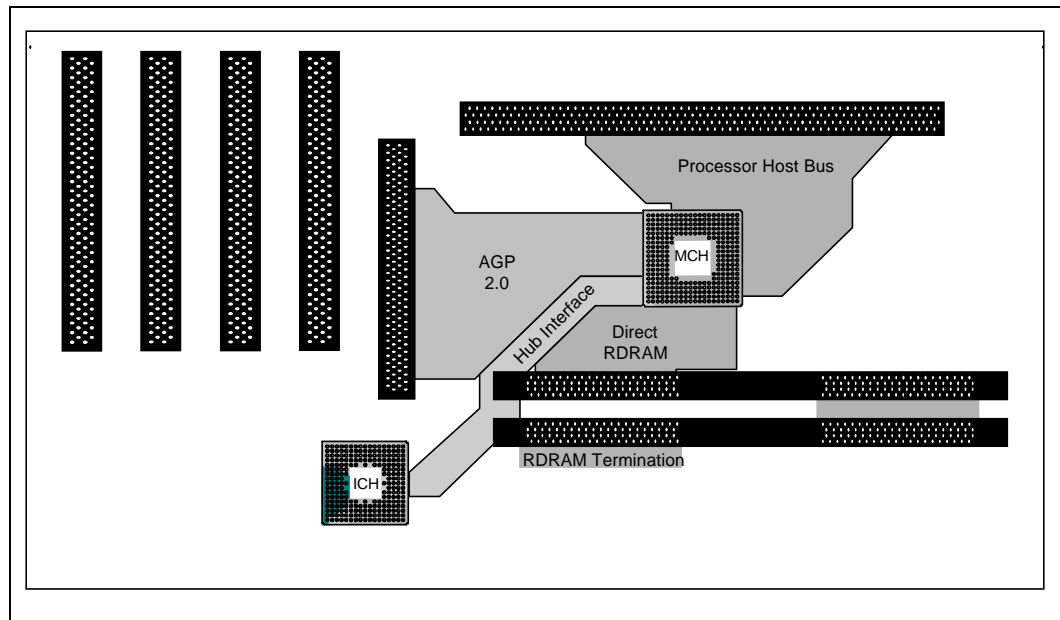
2.4 Core Chipset Routing Recommendations

Figure 2-4 and Figure 2-5 show MCH core routing examples.

Figure 2-4. Primary Side MCH Core Routing Example (ATX)

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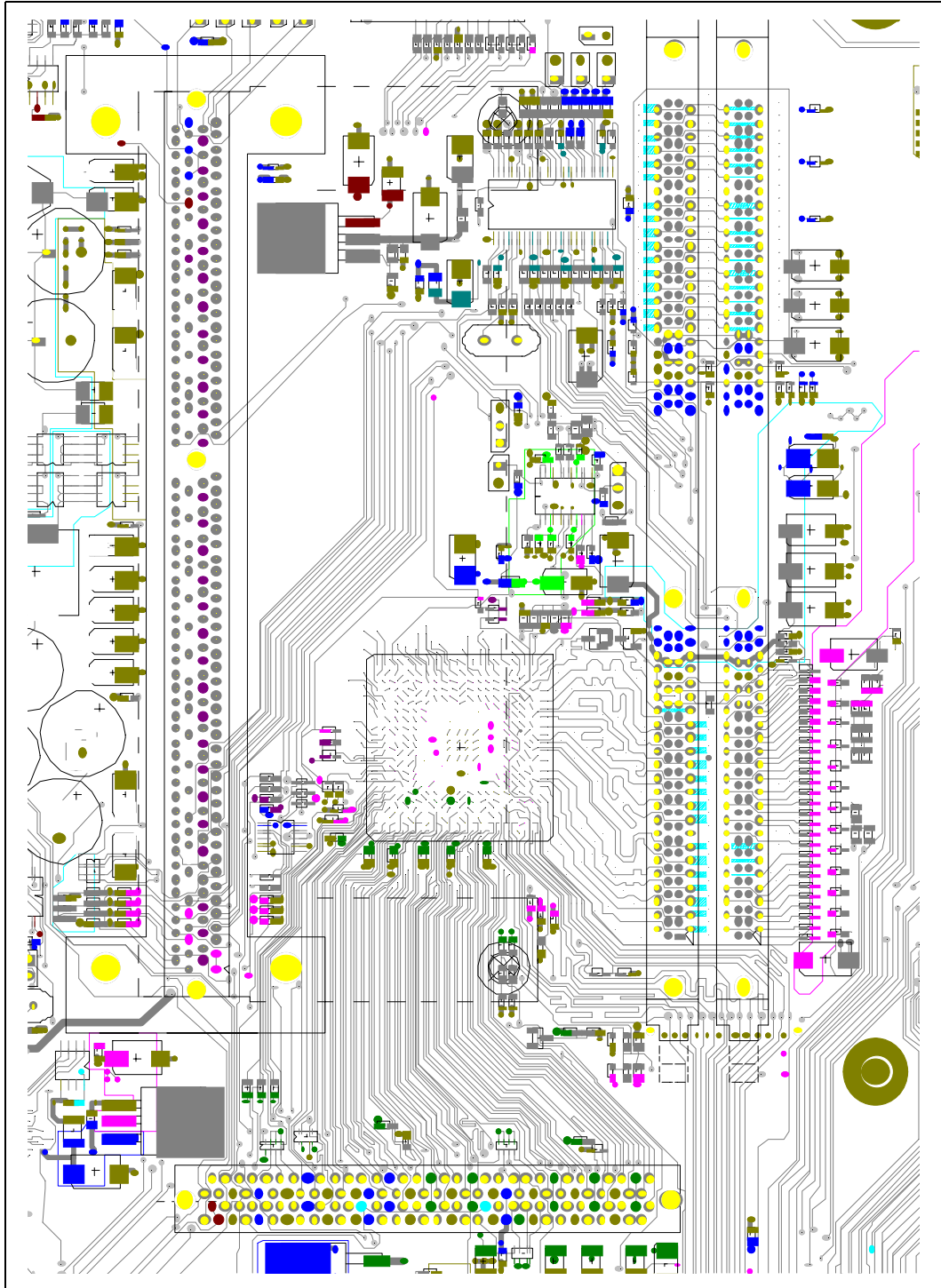
Figure 2-5. Secondary Side MCH Core Routing Example (ATX)
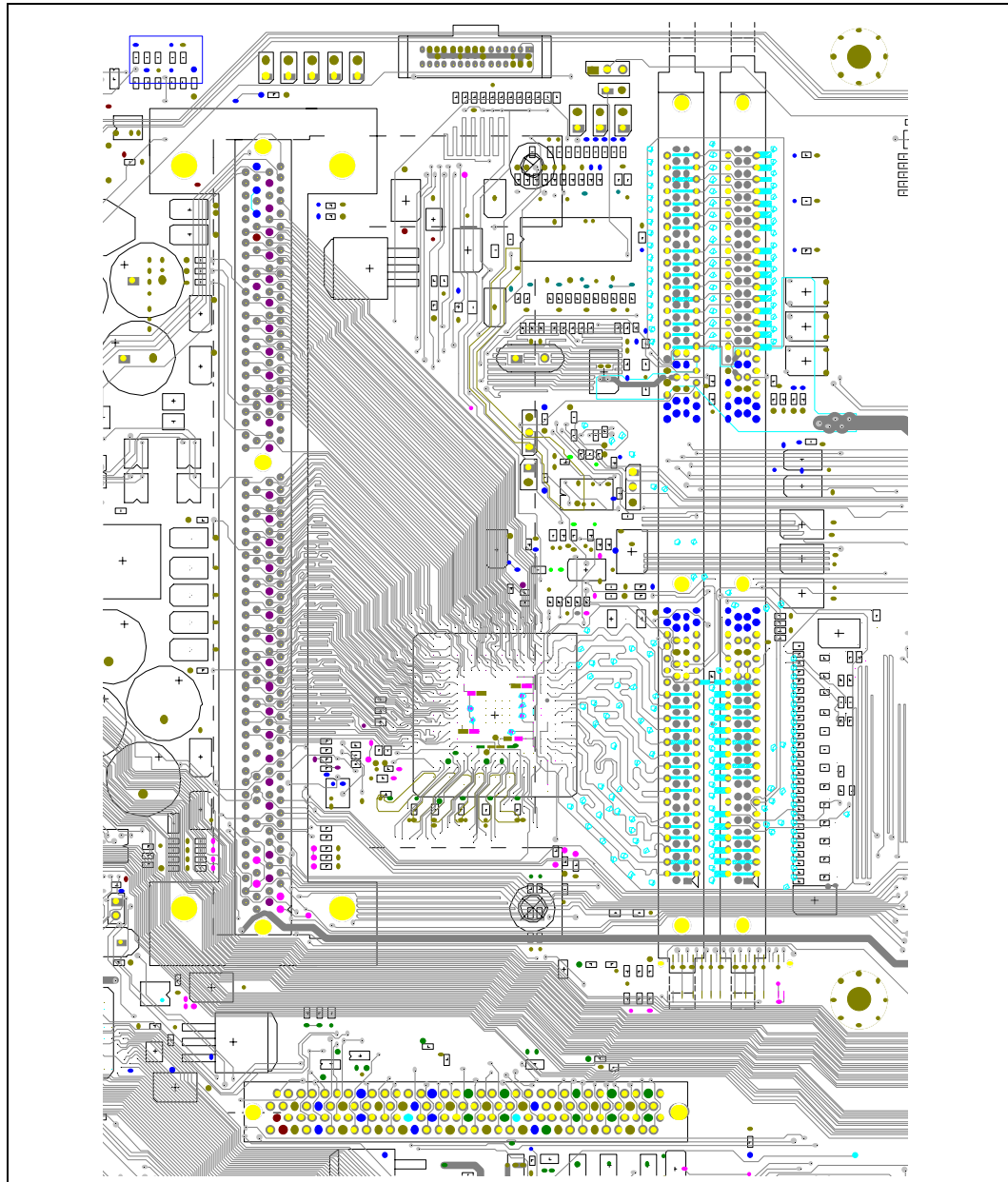
2.5   Source Synchronous Strobing

Source synchronous strobing is one of the technologies used in AGP 4X, Direct RDRAM and hub interface that allow very high data transfer rates. As buses get faster, and cycle times get shorter, the propagation delay is becoming a limiting factor in bus speed. Source synchronous strobing is used to minimize the impact of propagation delay (T_{prop}) on maximum bus frequency.

A source synchronous strobed interface uses strobe signals (instead of the clock) to indicate that data is valid. Refer to Figure 2-6 for an example.

Figure 2-6. Data Strobing Example
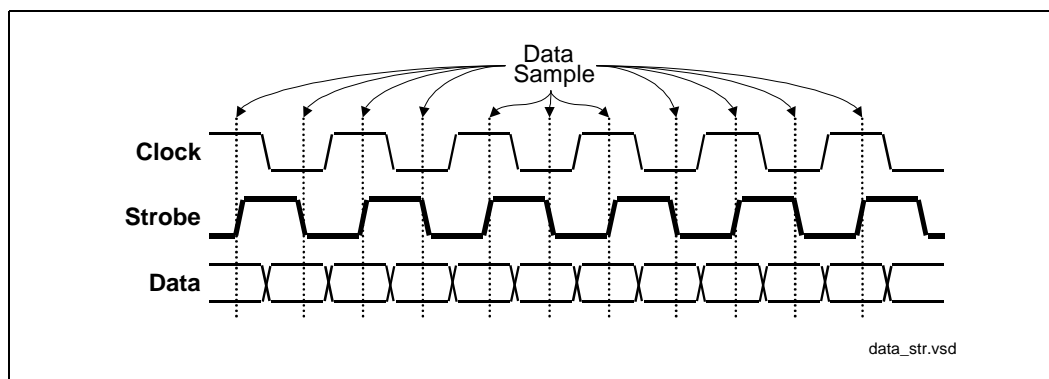
For a source synchronous strobed interface, it is *very important* that the strobe signals are routed carefully. These signals must be very clean (free of noise). Data signals are typically latched on the rising or falling edge of the strobe signal (or both). If there is noise on these signals, it could cause an extra "edge" to be detected, thus latching incorrect data. Refer to Figure 2-7 for examples.

Figure 2-7. Effect of Crosstalk on Strobe Signal
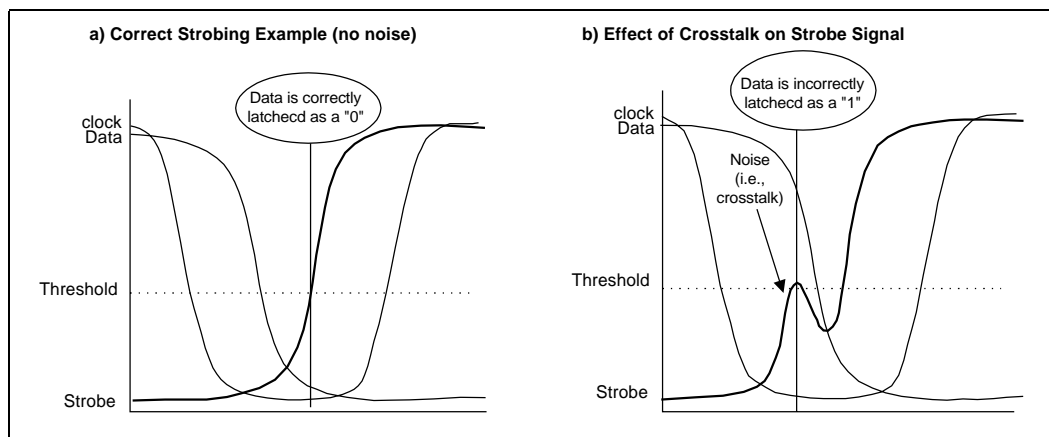
Some buses have more than one strobe (i.e., AGP). The AGP 1.0 specification (1X and 2X mode) employs 3 strobe signals. These three strobe signals are each used to strobe different *data* signals. That is, each strobe has an associated set of *data* signals. The associations for AGP 1.0 (AGP 2X) are documented in Table 2-1. Refer to Section 2.7, "AGP 2.0" on page 2-31 for more information on AGP 2.0 (AGP 4X, 1.5v).

Table 2-1. AGP 2X Data/Strobe Association

Data	Associated Strobe
AD[15:0] and C/BE[1:0]#	AD_STB0
AD[31:16] and C/BE[3:2]#	AD_STB1
SBA[7:0]	SB_STB

In this example, the lower address signals (AD[15:0]) are sampled on the rising and falling edges of AD_STB0, while the upper address signals (AD[31:16]) are sampled on the rising and falling edges of AD_STB1.

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When routing strobes and their associated data lines, trace length mismatch is very important (in addition to noise immunity). The primary benefit of source synchronous strobing is that the data and the strobe arrive at the receiver simultaneously. Thus, a strobe and its associated data signals have very critical length mismatch requirements. With well matched trace lengths (as well as matched impedance), the propagation delay for the strobe, and the propagation delay for the data will be very close. Hence, the strobe and the data arrive at the receiver simultaneously. For some interfaces, the trace length mismatch requirement is less than 0.25 inch.

2.6 Direct Rambus* Interface

The Direct Rambus* Channel is a multi-symbol interconnect. Due to the length of the interconnect and the frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. The driving device sends the next data out before the previous data has left the bus.

Figure 2-8. RIMM Diagram
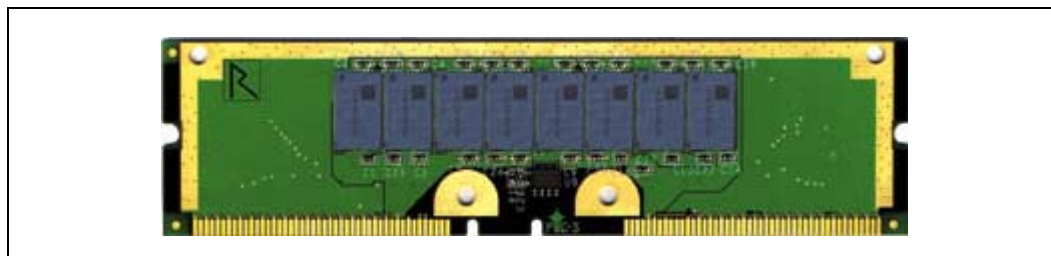
The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in reflected voltage levels is required. The interconnect transmission lines must be terminated at their characteristic impedance, or the reflected voltage resulting from a mismatch in impedance will degrade signal quality. These reflections will reduce noise and timing margins, and reduce the maximum operating frequency of the bus. Potentially, the reflections could create data errors.

Due to the tolerances of components such as PCBs, connectors, and termination resistors, there will be some reflected voltage on the interconnect. In this multi-symbol interconnect, timings are pattern dependent due to the reflections interfering with the next transfer.

Additionally, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source synchronous designs, the odd and even mode propagation velocity change creates skew between the clock and data or command lines which reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease crosstalk, as well as the other sources of skew.

To achieve these bus requirements, the Direct Rambus* channel is designed to operate as a transmission line; all components, including the individual RDRAMs, are incorporated into the design to create a uniform bus structure that can support up to 33 devices (including the MCH) running at 800 MegaTransfers/second (MT/s).

2.6.1   Stackup

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM interface to work properly. Maintaining 28 Ω (±10%) loaded impedance for every RSL (Direct Rambus* Signaling Level) signal has changed the requirements for trace width and prepreg thickness for the Intel® 820 chipset platform (refer to Section 5.3, "Stackup Requirement" on page 5-1).

Achieving a 28 Ω nominal impedance with a traditional 7 mil prepreg requires 28 mil wide traces. These traces are too wide to break out of the two rows of RSL balls on the MCH. To reduce trace width, a 4.5 mil thick prepreg is required. This thinner prepreg allows 18 mil wide traces to meet the 28 Ω (±10%) nominal impedance requirement. Refer to Section 5.3, "Stackup Requirement" on page 5-1 for detailed stackup requirements.

2.6.2   Direct Rambus* Layout Guidelines

The signals on the Direct Rambus* Channel are broken into three groups: RSL signals, CMOS signals, and Clocking signals. The signal groups are:

- RSL Signals
    - DQA[8:0]
    - DQB[8:0]
    - RQ[7:0]
- CMOS Signals
    - CMD (high-speed CMOS signal)
    - SCK (high-speed CMOS signal)
    - SIO
- Clocking Signals
    - CTM, CTM#
    - CFM, CFM#

2.6.2.1   RSL Routing

The RSL signals enter the first RIMM on the left side, propagate through the RIMM, and exit on the right. The signal continues through the rest of the existing RIMMs until it is terminated at V_{term}. All unpopulated slots must have continuity modules in place to ensure that the signals propagate to the termination.

Figure 2-9. RSL Routing Dimensions
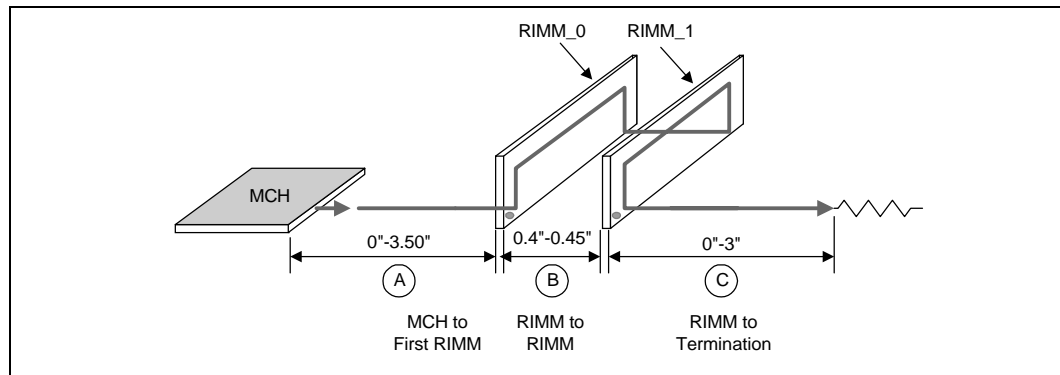
To maintain a nominal 28 Ω trace impedance, the RSL signals must be 18 mils wide. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace routed between adjacent RSL signals. The 10 mil ground isolation traces must be connected to ground with a via every 1". A 6 mil gap is required between the RSL signals and the ground isolation trace. These signals must be length matched to ±10 mils in line section "A" and ±2 mils in both line sections labeled "B" using the trace length matching methods in Section 2.6.2.6, "Length Matching Methods" on page 2-21. To ensure uniform trace lines, trace width variation must be uniform on all RSL signals at every neck-down for each line section. All RSL signals must have the same number of vias. It may be necessary to place vias on RSL signals where they are not necessary to meet this via loading requirement (i.e., dummy vias).

Table 2-2. Placement Guidelines for Motherboard Routing Lengths

Reference	Trace Description	Maximum Trace Length (in.)
A	MCH to first RIMM Connector	0" to 3.50"
B	RIMM to RIMM	0.4" – 0.45"
C	RIMM to Termination	0" to 3"

Figure 2-10 shows a top view of the trace width/spacing requirements for the RSL signals.

Figure 2-10. RSL Routing Diagram
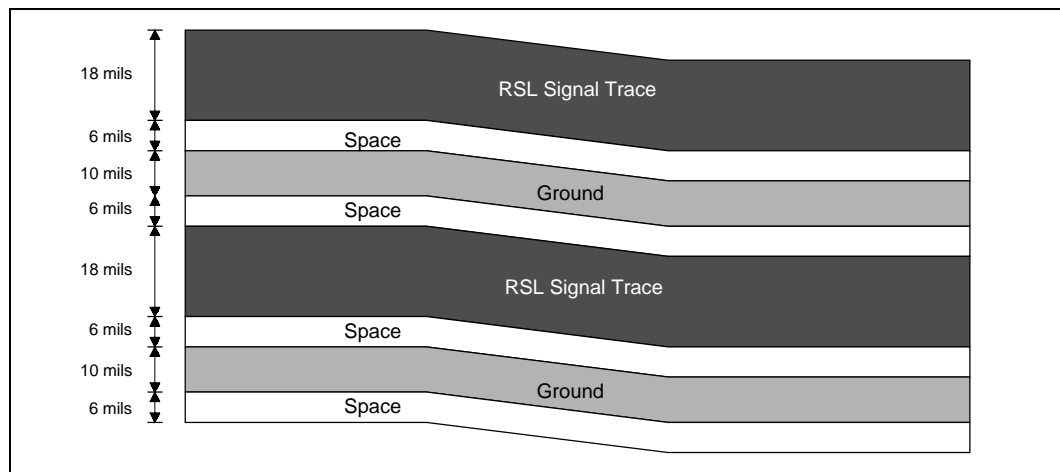
Figure 2-11 and Figure 2-12 show a top view of an example RSL breakout and route.

Figure 2-11. Primary Side RSL Breakout Example

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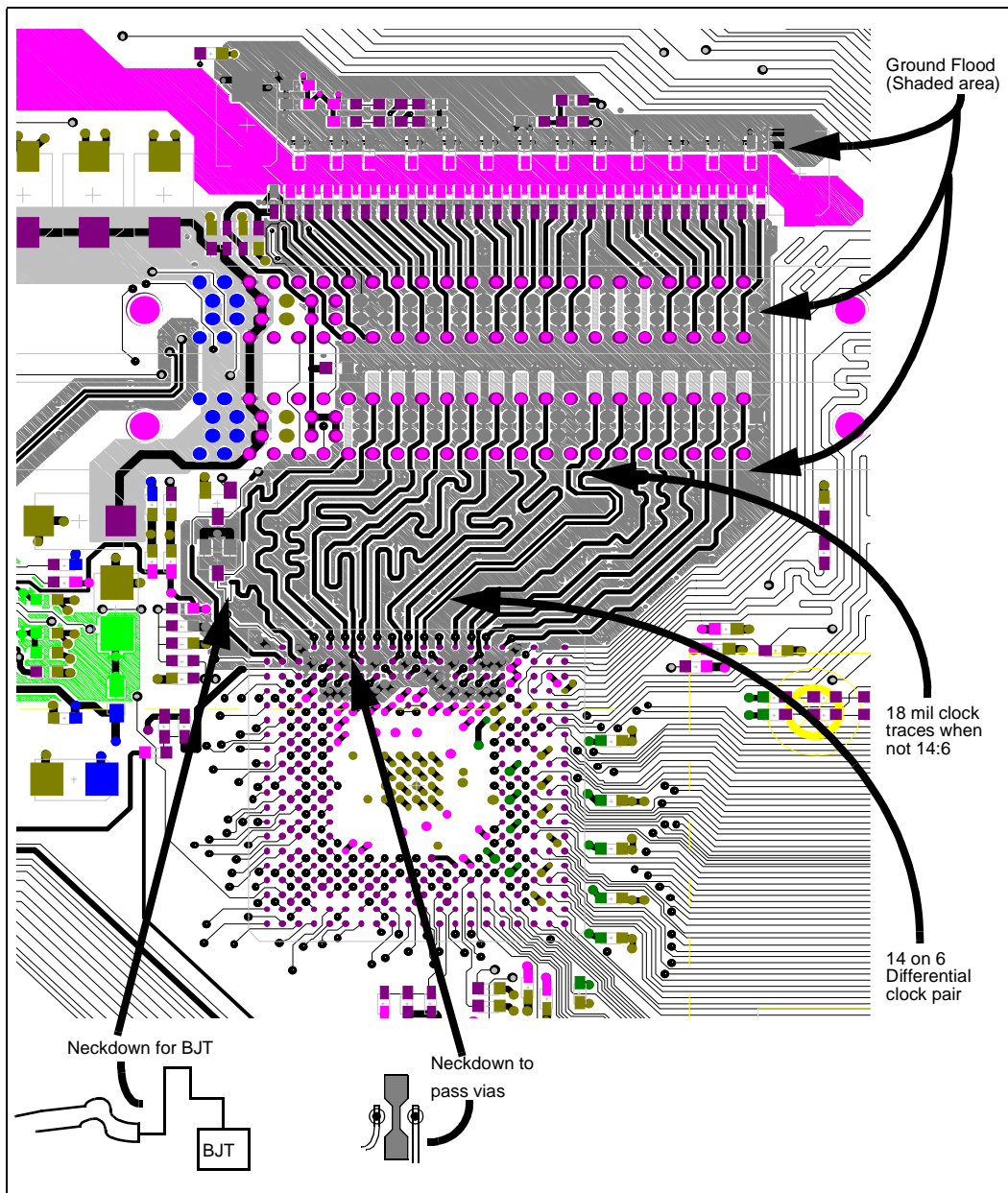
Figure 2-12. Secondary Side RSL Breakout Example
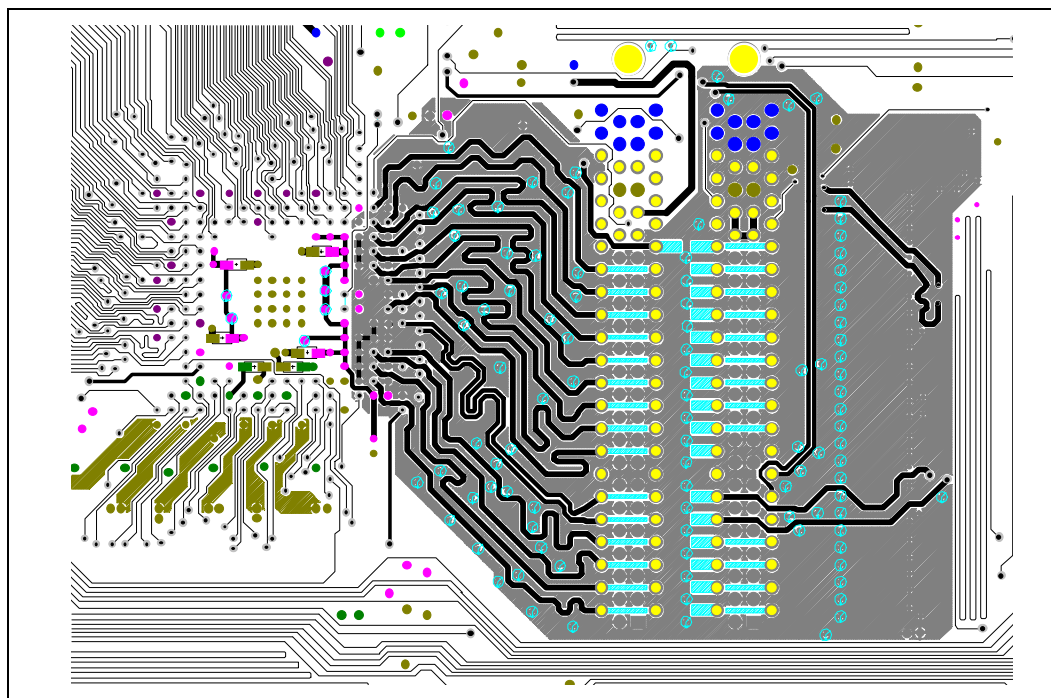
2.6.2.2   RSL Termination

All RSL signals must be terminated to 1.8V (Vterm) using 27Ω-2% or 28Ω-1% resistors at the end of the channel opposite the MCH. Resistor packs are acceptable. Vterm must be decoupled using high speed bypass capacitors (one 0.1 µF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, bulk capacitance is required. Assuming a linear regulator with approximate 20 ms response time, two 100 µF tantalum capacitors are recommended. The trace length between the last RIMM and the termination resistors should be less than 3". Length matching in this section of the channel is not required. The Vterm power island should be at LEAST 50 mils wide. This voltage does not need to be supplied during suspend-to-RAM.

Figure 2-13. Direct RDRAM Termination
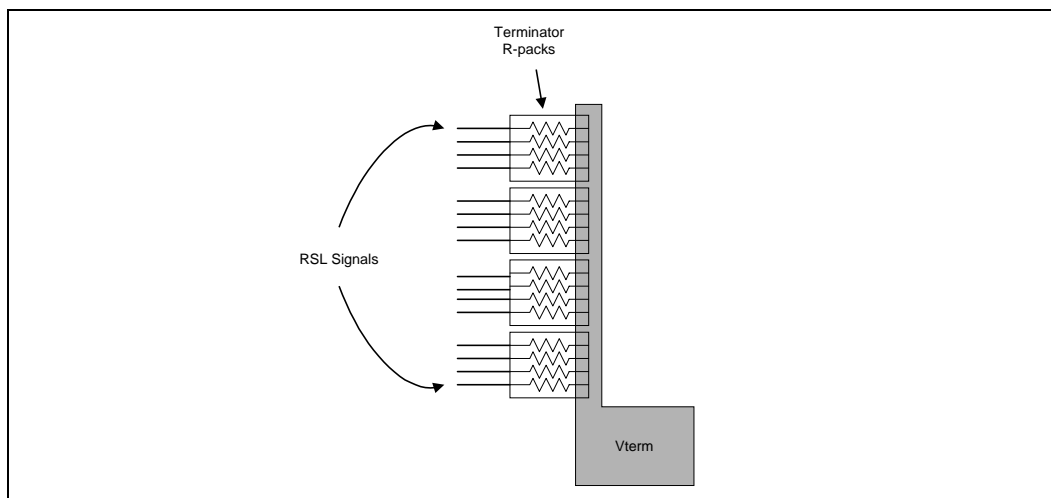
Note: It is necessary to compensate for the slight difference in electrical characteristics between a dummy via and a real via. Refer to Section 2.6.2.7, "VIA Compensation" on page 2-23 for more information on Via Compensation.

Figure 2-14. Direct Rambus* Termination Example

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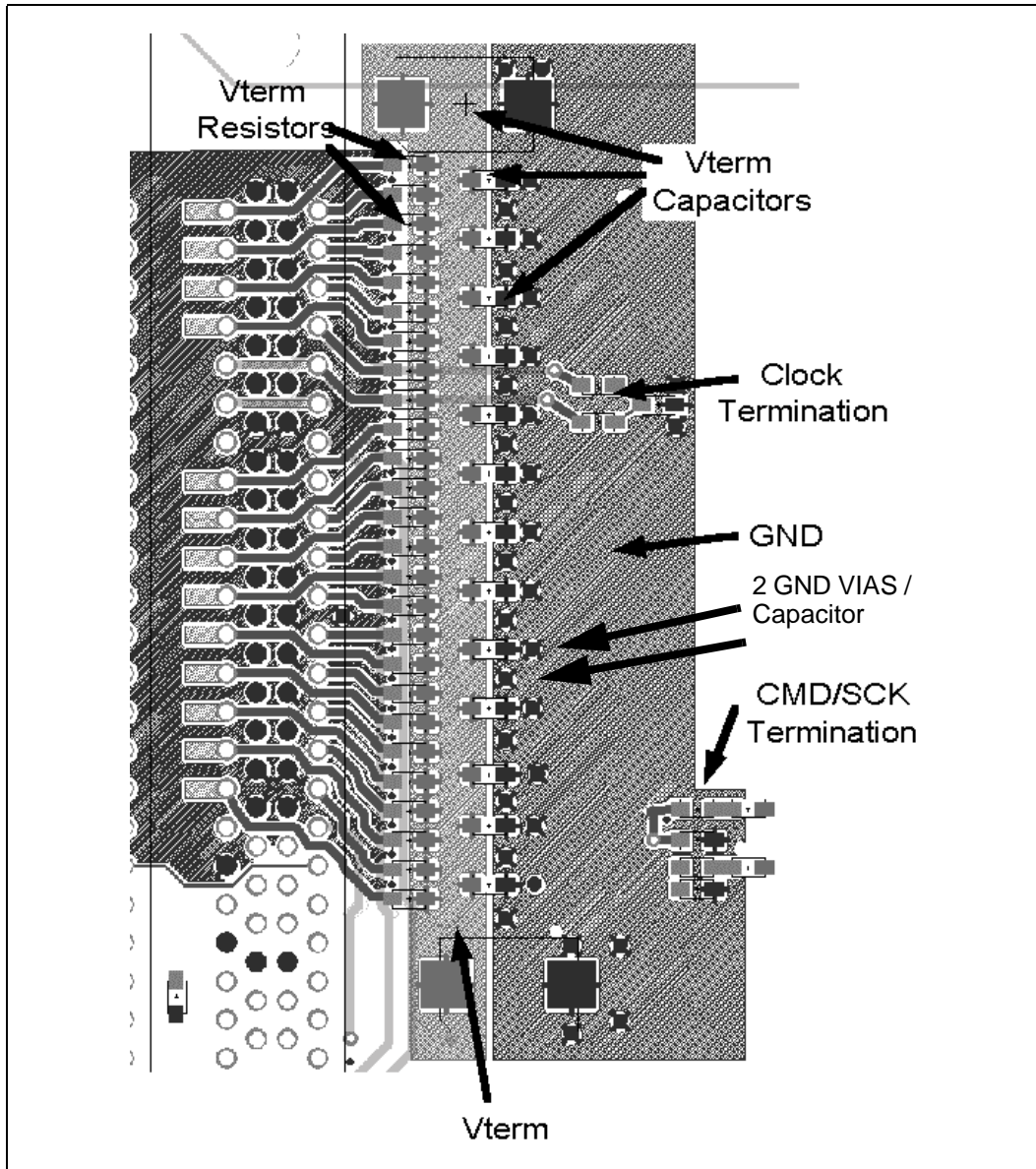
2.6.2.3 Direct Rambus* Ground Plane Reference

All RSL signals must be referenced to GND to provide an optimal current return path. The direct Rambus ground plane reference must be continuous to the Vterm capacitors. The ground reference island under the RSL signals must be continuous from the last RIMM to the back of the termination capacitors. Choose the reference island shape such that power delivery to the components is not compromised. The return current will flow through the Vterm capacitors into the ground island and under the RSL traces. Any split in the ground island will provide a sub-optimal return path. In a 4 layer board, this will require the Vterm island to be on an outer layer. The Vterm island should ALWAYS be placed on the top layer. Refer to Section 6.2, "Power Plane Splits" on page 6-7 for an example of power plane splits.

Figure 2-15. Incorrect Direct Rambus* Ground Plane Referencing
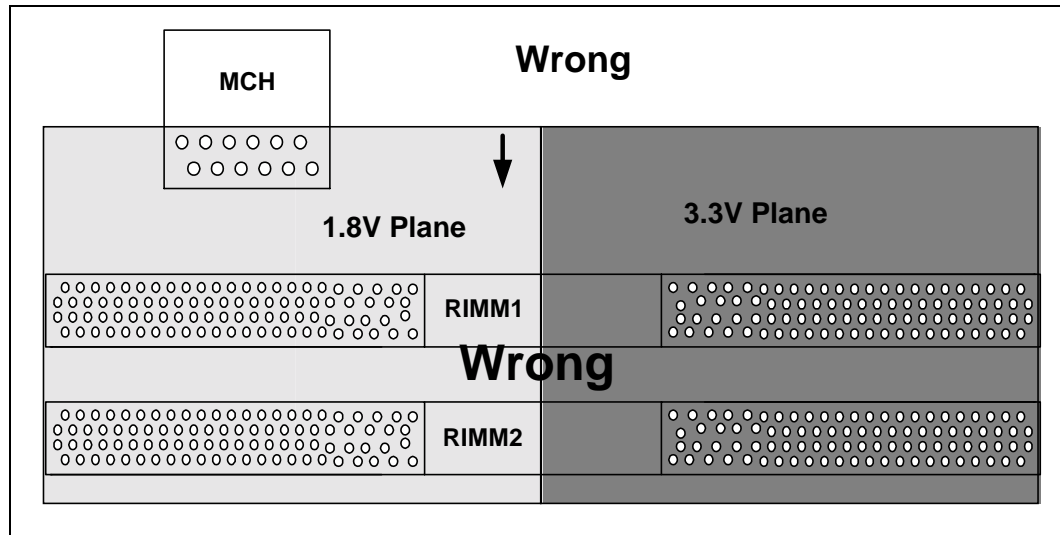
Figure 2-16. Direct Rambus Ground Plane Reference
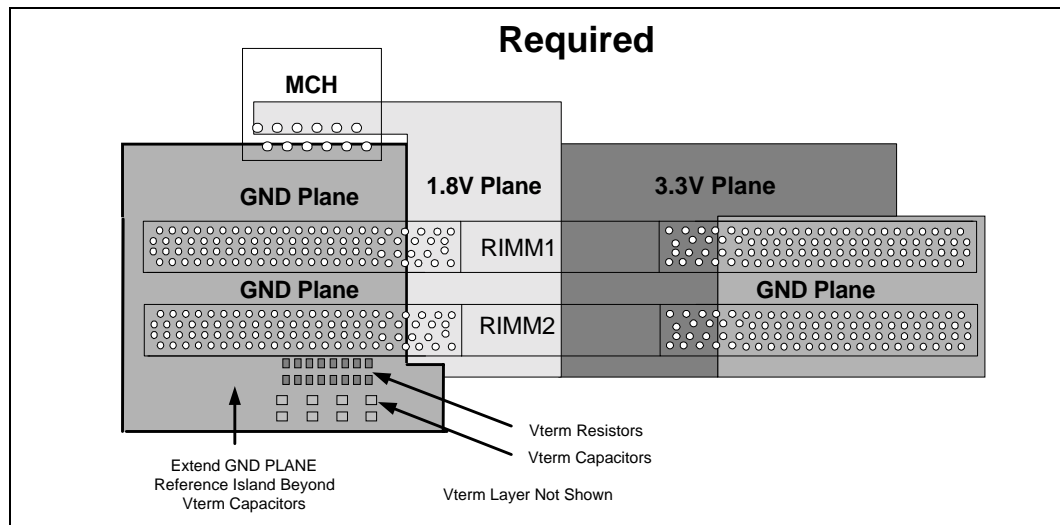
The ground reference island under the RSL signals MUST be connected to the ground pins on the RIMM connector and the ground vias used to connect the ground isolation on the 1st and 4th layers.

All 4 layers of the motherboard require correct grounding between the RSL signals on the motherboard:

- Layer 1 = Ground Isolation

- Layer 2 = Ground Plane

- Layer 3 = Ground Reference in the Power Plane

- Layer 4 = Ground Isolation

All ground vias and pins MUST be connected to all 4 layers.

2.6.2.4 Direct Rambus* Connector Compensation

The RIMM connector inductance causes an impedance discontinuity on the Direct Rambus* channel. This may reduce voltage and timing margin.

To compensate for the inductance of the connector, approximately 0.65 pF–0.85 pF compensating capacitive tab (C-TAB) is required on each RSL connector pin. This compensating capacitance must be added to the following connector pins at each connector:

LCTM	LCTM#
RCTM	RCTM#
LCFM	LCFM#
RCFM	RCFM#
LROW[2:0]	RROW[2:0]
LCOL[4:0]	RCOL[4:0]
RDQA[8:0]	LDQA[8:0]
RDQB[8:0]	LDQB[8:0]
SCK	CMD

This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector. The target value is approximately 0.65 pF–0.85 pF. The copper tab area for the recommended stackup was determined through simulation. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Equation is an approximation that can be used for calculating copper tab area on an outer layer.

Equation 2-1. Approximate Copper Tab Area Calculation

$$\text{Length*Width} = \text{Area} = C_{plate} * \text{Thickness of prepreg} / [(\varepsilon_0)\,(\varepsilon_r)\,(1.1)]$$

Where:

— $\varepsilon_0 = 2.25 \times 10^{-16}$ Farads/mil

— ε_r = Relative dielectric constant of prepreg material

— Thickness of prepreg = Stackup dependent

— Length, Width = Dimensions in mils of copper plate to be added

— Factor of 1.1 accounts for fringe capacitance.

Based on the stackup requirement in Section 5.3, "Stackup Requirement" on page 5-1 the copper tab area should be 2800 to 3600 sq mils. Different stackups require different copper tab areas. Table 2-3 shows example copper tab areas.

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Table 2-3. Copper Tab Area Calculation

Dielectric Thickness (D)	Separation Between Signal Trace & Copper Tab	Minimum Ground flood	Air Gap between Signal & GND Flood	Compen-sating Capacitance in pF	Copper Tab (C-TAB) Area (A) In sq mils	C-TAB Shape (mils)
4.5	6	10	6	0.65	2800	140 L x 20 W 70 L x 40 W

Based on Equation 1, the tab area is 2800 sq mils, where ε_r is 4.2 and D is 4.5. These values are based on 2116 prepreg material.

Note that more than one copper tab shape may be used. The tab dimensions are based on copper area over the ground plane. The actual length and width of the tabs may be different due to routing constraints (e.g., if tab must extend to center of hole, or antipad); however, each copper tab should have equivalent area. For example, the copper tabs in Figure 2-17 have the following dimensions, when measured tangent to the antipad:

Inner C-TAB = 140 (length) x 20(width)

Outer C-TAB = 70 (length) x 40 (width)

The following figures show a routing example of tab compensation capacitors. Note that ground floods around the RIMM pins must not be interrupted by the capacitor tabs, and they must be connected to avoid discontinuity in the ground plane as shown.

Figure 2-17. Connector Compensation Example

Intel®820 Chipset Design Guide
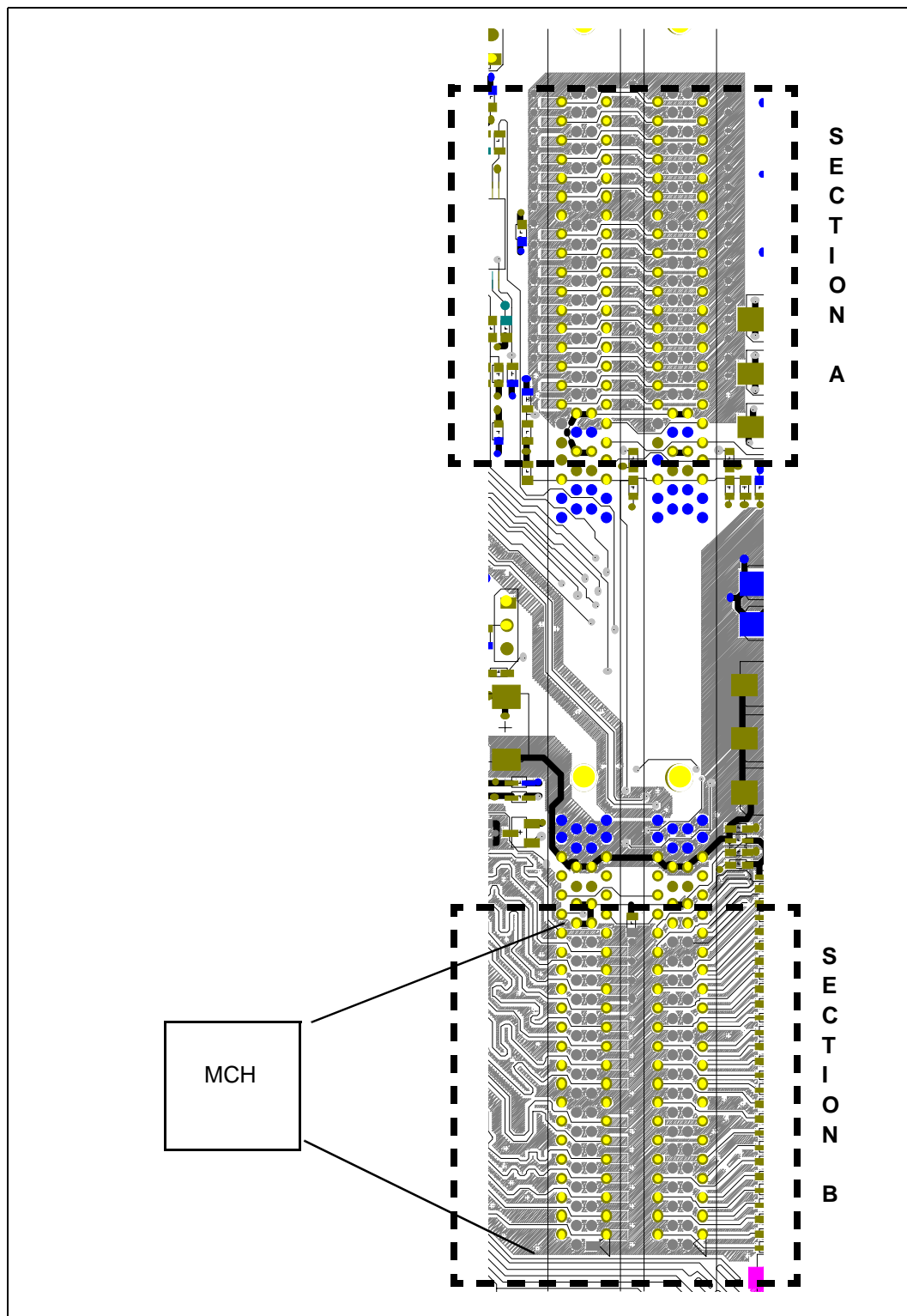
Figure 2-18. Section A[1], Top Layer
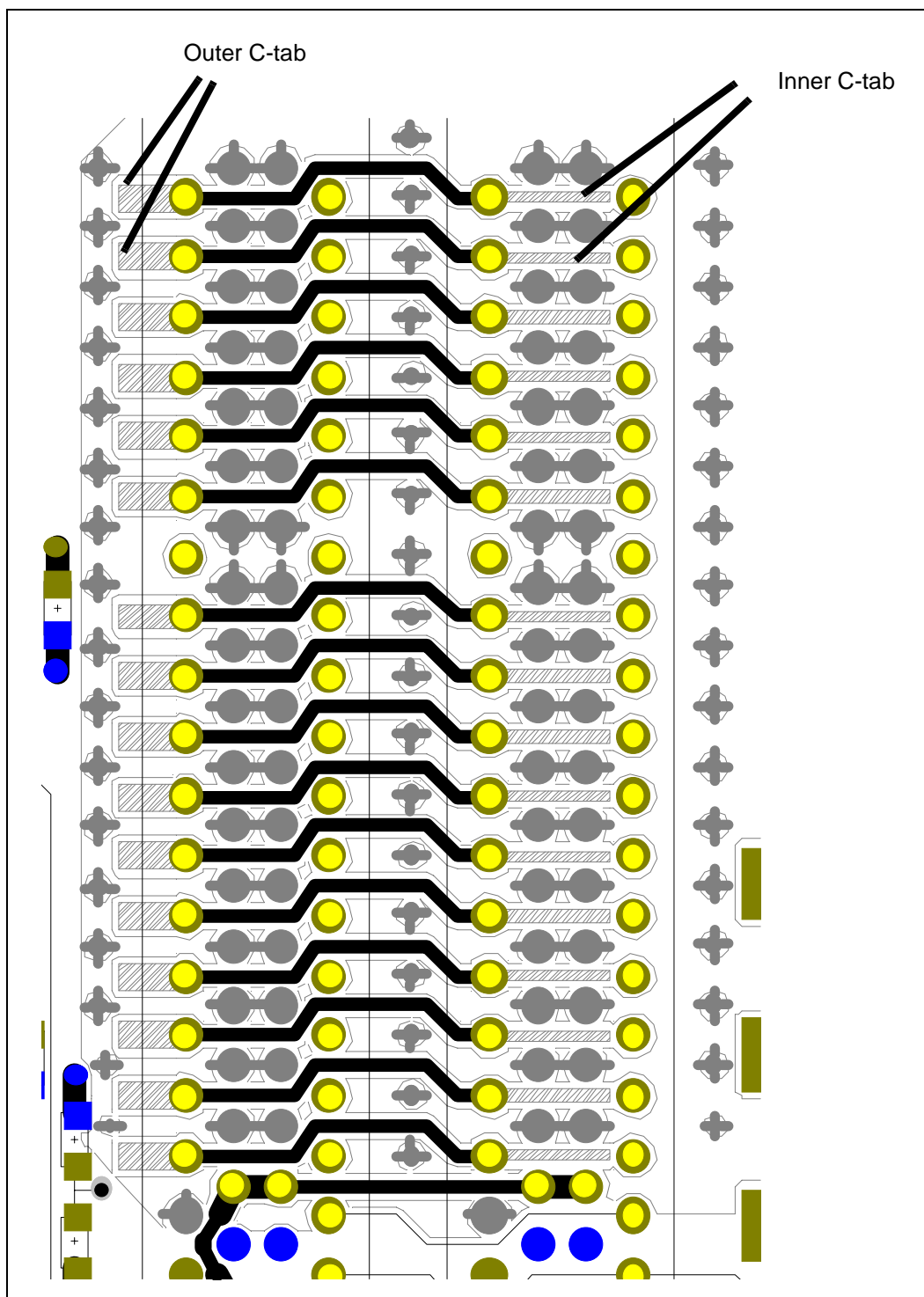
NOTES:
1. Refer to Figure 2-17. Ground flood removed from picture for clarity

Figure 2-19. Section A[1], Bottom Layer
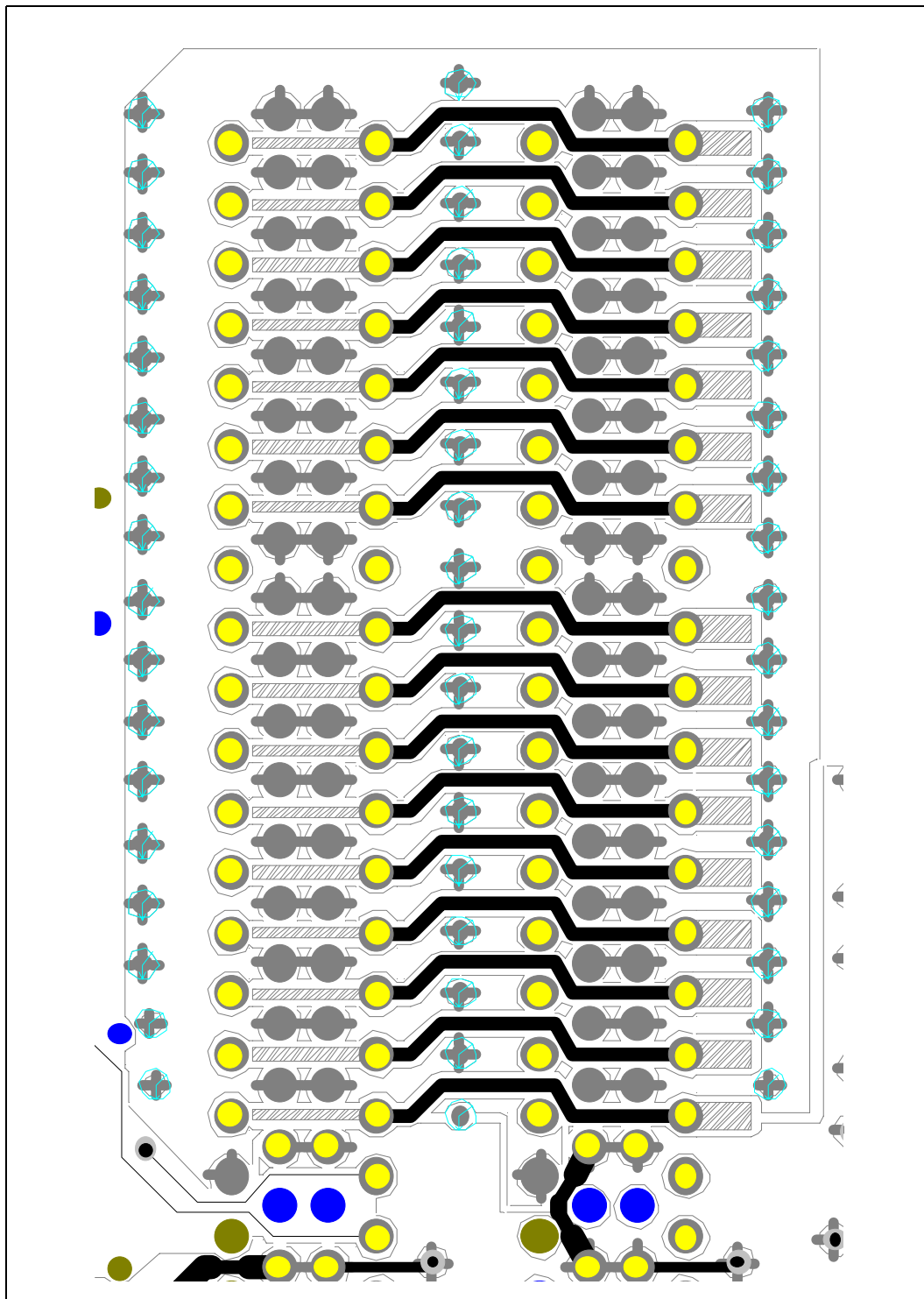
NOTES:
 1. Refer to Figure 2-17. Ground flood removed from picture for clarity

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Figure 2-20. Section B[1], Top Layer
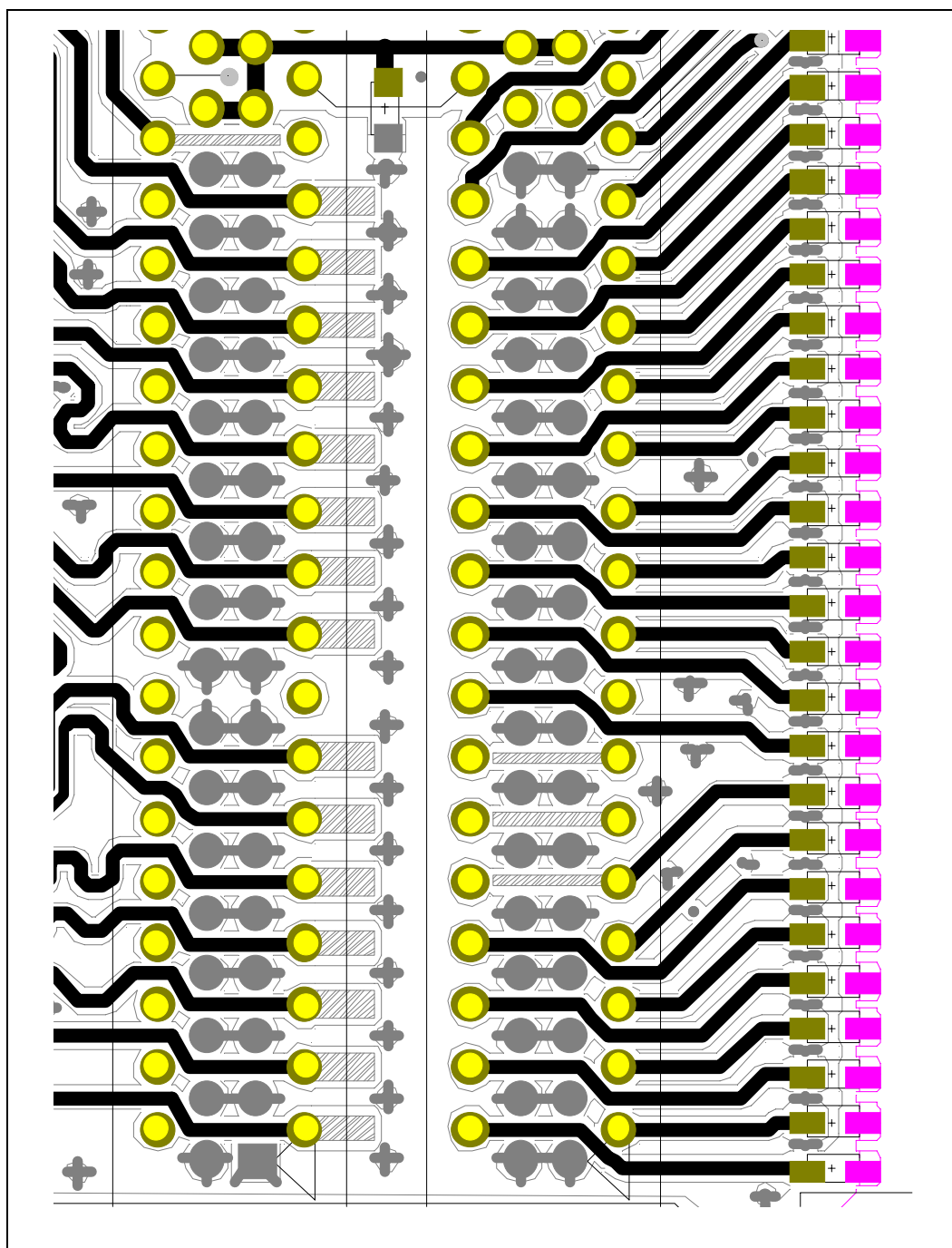
NOTES:
1. Refer to Figure 2-17. Ground flood removed from picture for clarity

Figure 2-21. Section B[1], Bottom Layer
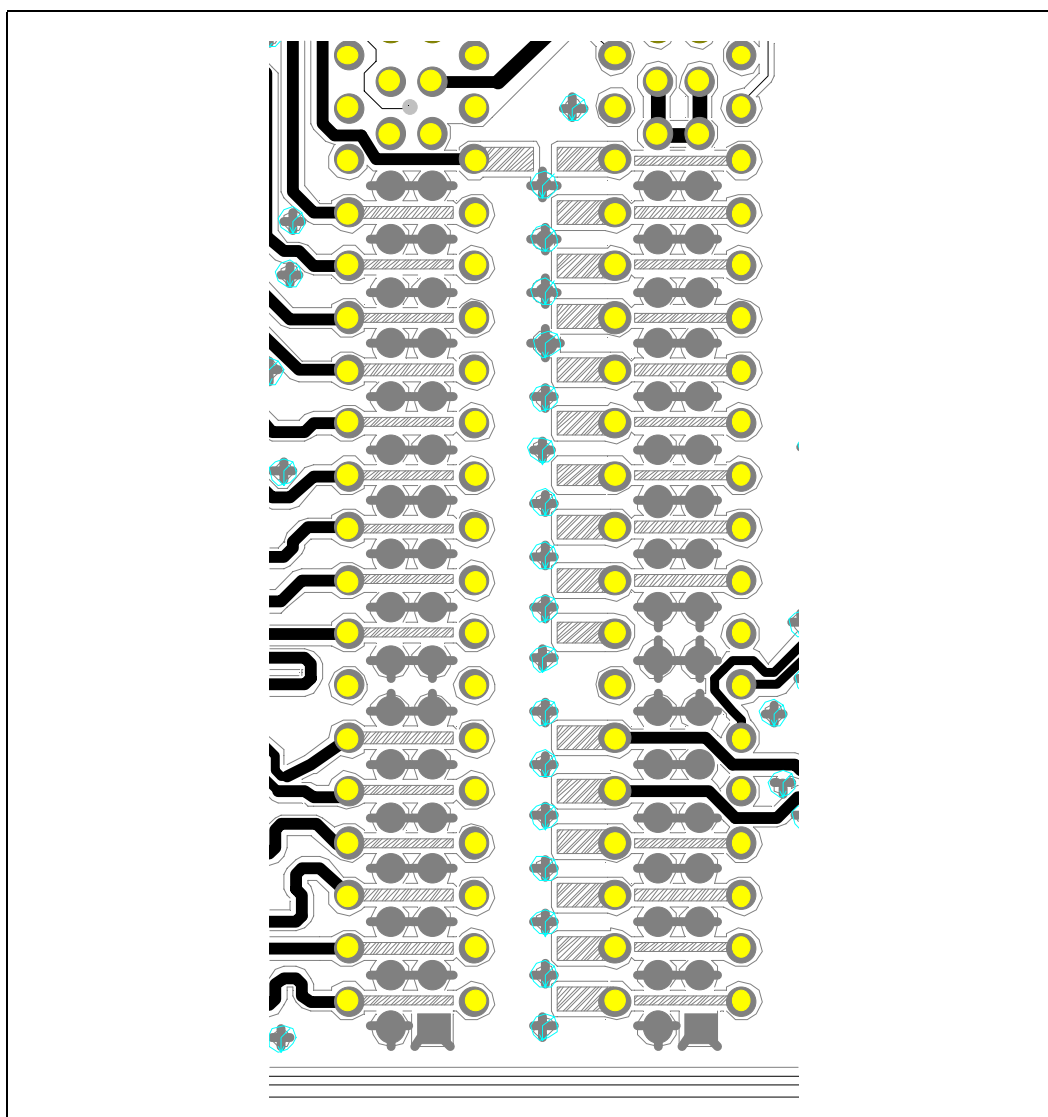
NOTES:
 1. Refer to Figure 2-17. Ground flood removed from picture for clarity

2.6.2.5 RSL Signal Layer Alternation

RSL signals must alternate layers as they are routed through the channel. If a signal is routed on the primary layer from the MCH to the first RIMM socket, it must be routed on the secondary layer from the first RIMM to the second RIMM as shown in Figure 2-22 (signal B). If a signal is routed on the secondary layer from the MCH to the first RIMM socket, it must be routed on the primary layer from the first RIMM to the second RIMM as shown in Figure 2-22 (signal A). Signals to the termination resistors can be routed on either layer from the last RIMM.

Figure 2-22. RSL Signal Layer Alternation
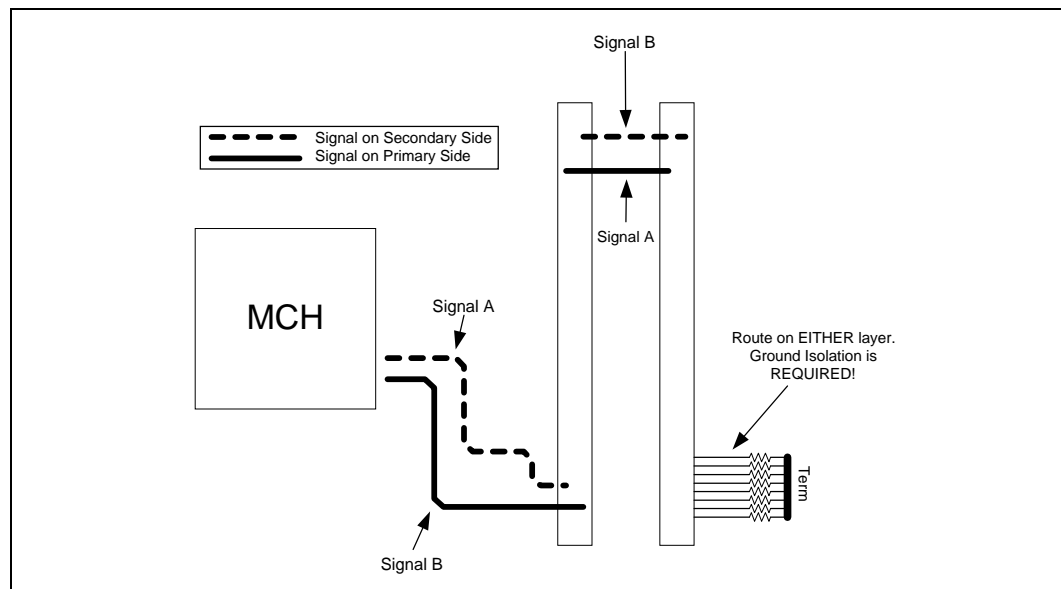
Table 2-4. RSL Routing Layer Requirements

	MCH to 1st RIMM	1st RIMM to 2nd RIMM
Method 1	Primary Side	Secondary Side
Method 2	Secondary Side	Primary Side

2.6.2.6   Length Matching Methods

In order to allow for greater routing flexibility, the RSL signals require *pad-to-pin* length matching between the MCH and the first connector. If the trace lengths are matched between the balls of the MCH and the pin of RIMM connector, the length mismatch between the pad (on the die) and the ball has not been accounted. However, given the *package dimension*, a representation of the length from the pad to the ball, the routing can compensate for this *package mismatch*. Therefore, the *board length mismatch* can be increased.

The RSL channel requires matching trace lengths from pad-to-pin within ±10 mils.

Given these definitions:

- *Package Dimension:* a representation of the length from the pad to the ball.
- *Board Trace Length:* the trace length on the board.
- *Nominal RSL Length:* the length to which all signals are matched. (note: there is not necessarily a trace that is EXACTLY to nominal length, but all RSL signals must be matched to within ±10mil of a nominal length). The *Nominal RSL Length* is an arbitrary length (within the limits of the routing guidelines) to which all the RSL signals will be matched (within 10 mils).

ALL RSL signals must meet the following equation.

Equation 2-2. RDRAM RSL Signal Trace Length Calculation

Package Dimension + Board Trace Length = Nominal RSL Length ± 10mils

Figure 2-23. RDRAM Trace Length Matching Example
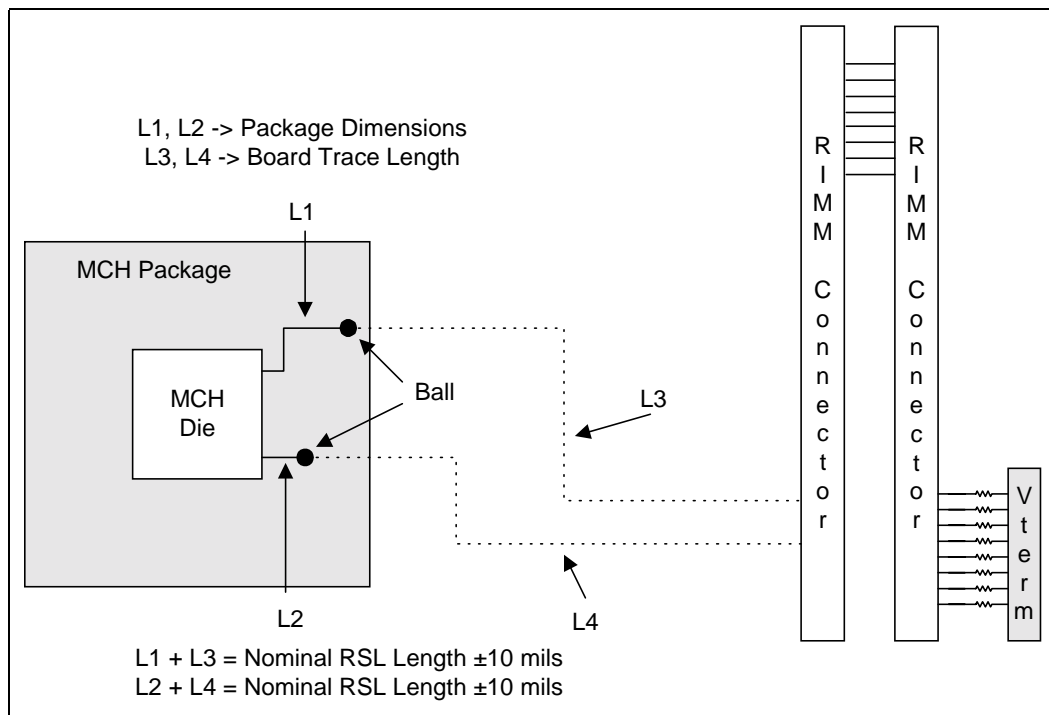
NOTE: Refer to the *Intel*® *820 Chipset: Intel*® *82820 Memory Controller Hub (MCH)* Datasheet for component package dimensions.

The RDRAM clocks (CTM, CTM#, CFM and CFM#) must be longer than the RDRAM signals due to their increased trace velocity (because they are routed as a differential pair). To calculate the length for each clock, the following formula should be used:

Equation 2-3. RDRAM Clock Signal Trace Length Calculation

Clock Length = Nominal RSL Signal Length (package + board) * 1.021

Using this formula, the clock signals will be 21 mils/inch longer than the Nominal Length. The lengthening of the clock signals, to compensate for their trace velocity change, ONLY applies to routing between the MCH and the first RIMM. The clock signals should be matched in length to the RSL signals between RIMMs. Refer to for more detailed clock routing guidelines.

The high-speed CMOS signals must be length matched to the RSL signals within 1200 mils (1.2 in) due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit.

It is necessary to compensate for the slight difference in electrical characteristics between a dummy via and a real via. Refer to the following section for more information on Via Compensation.

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2.6.2.7 VIA Compensation

As described in Section 2.8.2, "Strobe Signals" on page 2-44, all signals must have the same number of vias. As a result, each trace will have 1 via (near the BGA pad) because some of the RSL signals must be routed on the bottom of the motherboard. Therefore, it is necessary to place a dummy via on all signals that are routed on the top layer. Because the electrical characteristics of a dummy via do not match the electrical characteristics of a real via exactly, additional compensation must be performed on each signal that has a dummy via. Each signal with a dummy via must have 25 mils of additional trace length. That is: *a real via = a dummy via + 25 mils of trace length*.

This 25 mils of additional trace length must be added to each signal routed on the top layer after length matching, as documented in Section 2.6.2.6, "Length Matching Methods" on page 2-21.

Figure 2-24. "Dummy" Via vs. Real "Via"
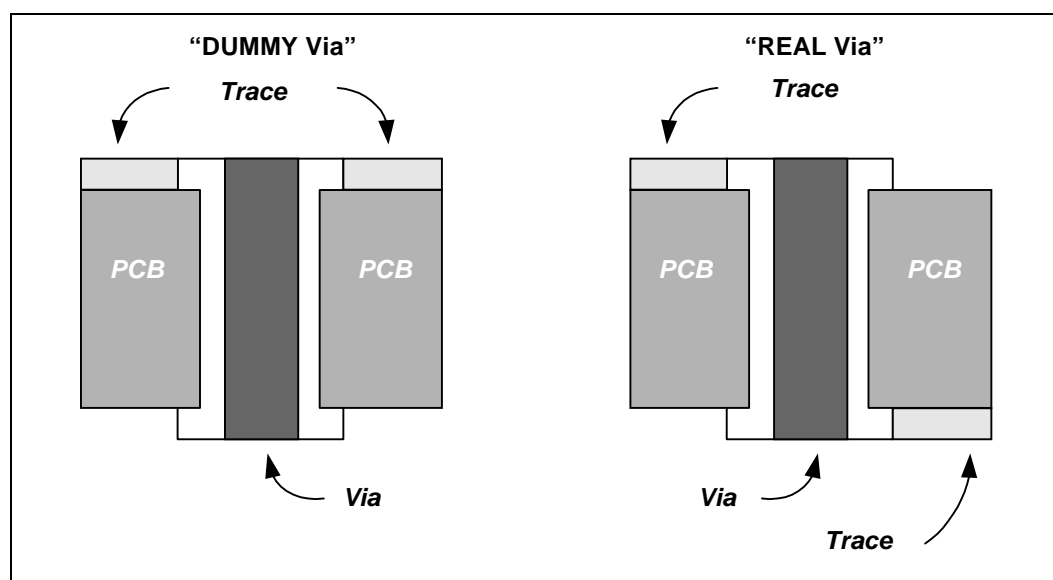
2.6.2.8 Length Matching & Via Compensation Example

Table 2-5 can be used to ensure that the RSL signals are the correct length.

Note: 2000 mils was chosen as an EXAMPLE Nominal RSL Length.

Table 2-5. Line Matching and Via Compensation Example[1,2,3,4,5,6,7,8,9,10]

Signal	Ball on MCH	Nominal RSL Length (mils)	Package Dimension (mils)	Motherboard Trace Length when Routed on Bottom (i.e., Real Via)		Motherboard Trace Length when Routed on Top (i.e., Dummy Via)		Recommended To Route On
				Min (mils)	Max (mils)	Min (mils)	Max (mils)	
				Formula A		**Formula B**		
DQA0	A13	2000	138.14	1851.86	1871.86	1876.86	1896.86	Top
DQA1	C13	2000	19.11	1970.89	1990.89	1995.89	2015.89	Bottom
DQA2	A14	2000	163.16	1826.84	1846.84	1851.84	1871.84	Top
DQA3	C14	2000	39.87	1950.13	1970.13	1975.13	1995.13	Bottom
DQA4	B14	2000	97.54	1892.46	1912.46	1917.46	1937.46	Top
DQA5	C15	2000	62.67	1927.33	1947.33	1952.33	1972.33	Bottom
DQA6	A15	2000	186.11	1803.90	1823.90	1828.90	1848.90	Top
DQA7	C16	2000	95.70	1894.30	1914.30	1919.30	1939.30	Bottom
DQA8	A16	2000	230.20	1759.81	1779.81	1784.81	1804.81	Top
DQB0	C7	2000	39.56	1950.44	1970.44	1975.44	1995.44	Bottom
DQB1	B7	2000	95.83	1894.17	1914.17	1919.17	1939.17	Top
DQB2	C6	2000	63.49	1926.51	1946.51	1951.51	1971.51	Bottom
DQB3	A6	2000	153.69	1836.31	1856.31	1861.31	1881.31	Top
DQB4	C5	2000	97.33	1892.67	1912.67	1917.67	1937.67	Bottom
DQB5	A5	2000	191.43	1798.57	1818.57	1823.57	1843.57	Top
DQB6	B5	2000	152.47	1837.53	1857.53	1862.53	1882.53	Bottom
DQB7	A4	2000	237.71	1752.29	1772.29	1777.29	1797.29	Top
DQB8	C4	2000	138.29	1851.71	1871.71	1876.71	1896.71	Bottom
RQ0	A7	2000	179.49	1810.51	1830.51	1835.51	1855.51	Top
RQ1	C8	2000	27.12	1962.88	1982.88	1987.88	2007.88	Bottom
RQ2	A8	2000	162.21	1827.79	1847.79	1852.79	1872.79	Top
RQ3	C9	2000	5.80	1984.20	2004.20	2009.20	2029.20	Bottom
RQ4	B9	2000	71.70	1918.30	1938.30	1943.30	1963.30	Top
RQ5	A9	2000	133.88	1856.12	1876.12	1881.12	1901.12	Bottom
RQ6	A10	2000	122.20	1867.81	1887.81	1892.81	1912.81	Top
RQ7	C10	2000	0.00	1990.00	2010.00	2015.00	2035.00	Bottom
				FORMULA C		**FORMULA D**		
CFM	A12	2000	132.37	1906.85		1932.37		Bottom
CFM#	B12	2000	64.63	1976.02		2001.54		Bottom
CTM	B11	2000	56.06	1984.76		2010.29		Top
CTM#	A11	2000	126.34	1913.01		1938.53		Top

NOTES:
1. Signals connecting to the *"A"* side of the RIMM connector (i.e., A1, A2, A3, etc.) should be routed on the top (primary side) of the motherboard;
2. Signals connecting to the "B" side of the RIMM connector should be routed on bottom (solder side).
3. These trace lengths ONLY apply from MCH to the 1st RIMM. All signals must match EXACTLY from RIMM to RIMM.
4. Clock trace lengths include 1.021 trace velocity factor.
5. Formula *A* min: Motherboard Trace = (Nominal RSL Length - Package Dimension) - 10 mil
6. Formula *A* max: Motherboard Trace = (Nominal RSL Length - Package Dimension) + 10 mil
7. Formula *B* min: Motherboard Trace = (Nominal RSL Length - Package Dimension) - 10 mil + 25 mil
8. Formula *B* max: Motherboard Trace = (Nominal RSL Length - Package Dimension) + 10 mil + 25 mil
9. Formula *C*: Motherboard Trace = (Nominal RSL Length - Package Dimension) * 1.021
10. Formula *D*: Motherboard Trace = (Nominal RSL Length - Package Dimension + 25 mil) * 1.021

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2.6.3 Direct Rambus[*] Reference Voltage

The Direct Rambus* reference voltage (RAMREF) must be generated as shown in Figure 2-25. RAMREF should be generated from a typical resistor divider using 2% tolerance resistors. Additionally, RAMREF must be decoupled locally at EACH RIMM connector, at the resistor divider and at the MCH. Finally, as shown in Figure 2-25, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with a 10 mil wide trace.

Figure 2-25. RAMRef Generation Example Circuit
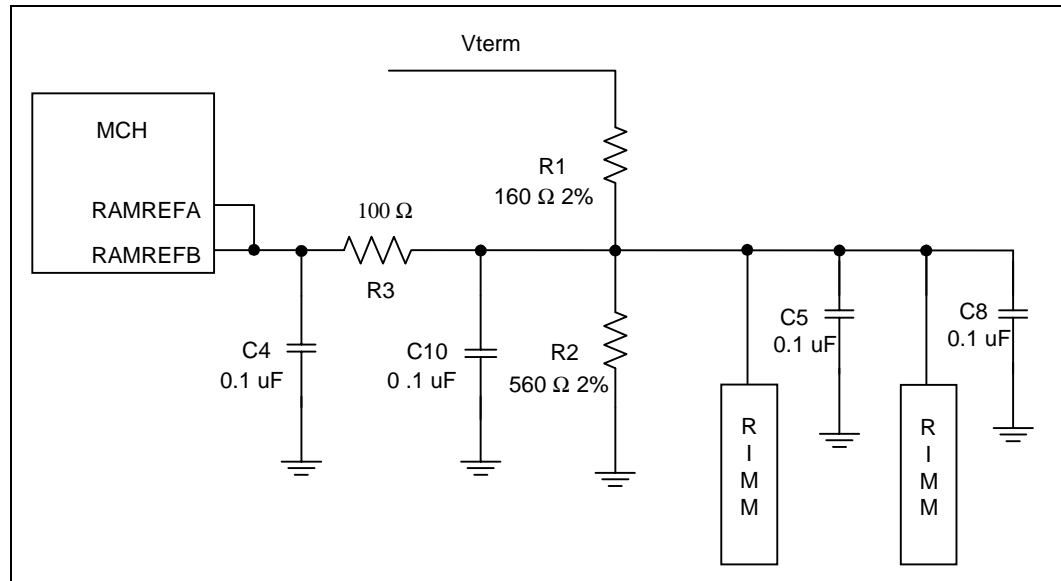
2.6.4 High-speed CMOS Routing

- The high-speed CMOS signals (CMD & SCK) must be routed using 28 Ω traces. Using the recommended stackup, these signals will be 18 mils wide.

- The high-speed CMOS signals must be length matched to the RSL signals within 1200 mils (1.2in) due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit.

- The high-speed CMOS signals require termination as shown in Figure 2-26 due to the buffer strengths in the MCH.

- The resistors must be 91 Ω pullup and 39 Ω pulldown; they also must 2% or better for S3 mode reliability. The trace impedances remain 28 Ω.

Figure 2-26. High-Speed CMOS Termination
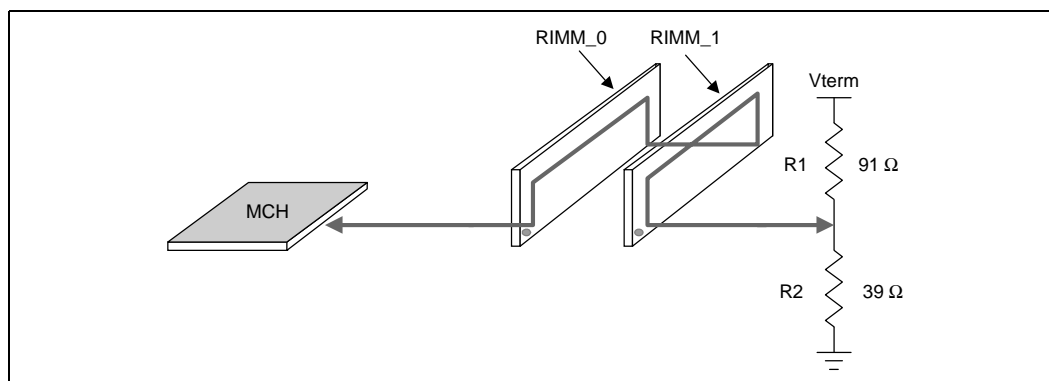
2.6.4.1   SIO Routing

The SIO signal must be routed from RIMM to RIMM as shown in Figure 2-17. The SIO signal requires a 2.2 KΩ – 10 KΩ terminating resistor on the SOUT pin of the last RIMM. SIO is routed with a standard 5 mil wide 60 Ω trace. The motherboard routing lengths for the SIO signal are the same as RSL signals (see Figure 2-17).

Figure 2-27. SIO Routing Example
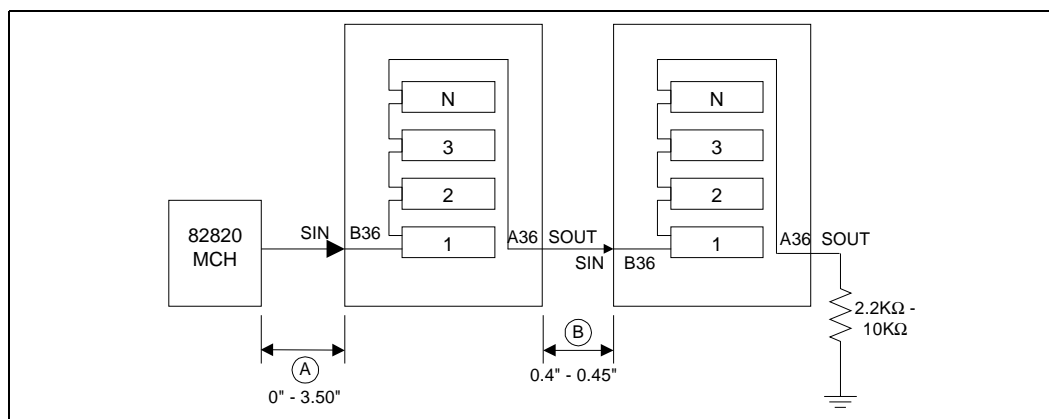
2.6.4.2   Suspend-to-RAM Shunt Transistor

When an Intel® 820 chipset system enters or exits Suspend-to-RAM, power will be ramping to the MCH (i.e., it will be powering-up or powering-down). When power is ramping, the state of the MCH outputs is not guaranteed. Therefore, the MCH could drive the CMOS signals and issue CMOS commands. One of the commands (the only one the RDRAMs would respond to) is the powerdown exit command. To avoid the MCH inadvertently taking the RDRAMs out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal must be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. This shunting can be accomplished using the NPN transistor shown in circuit shown in Figure 2-28. The transistor should have a Cobo of 4 pf or less (i.e., MMBT3904LT1).

In addition, to match the electrical characteristics on the SCK signal, the CMD signal needs a *dummy* transistor. This transistor's base should be tied to ground (i.e., always turned off).

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To minimize impedance discontinuities, the traces for CMD and SCK must have a neckdown from 18 mil traces to 5 mil traces for 175 mils on either side of the SCK/CMD attach point as shown in Figure 2-28.

Figure 2-28. RDRAM CMOS Shunt Transistor
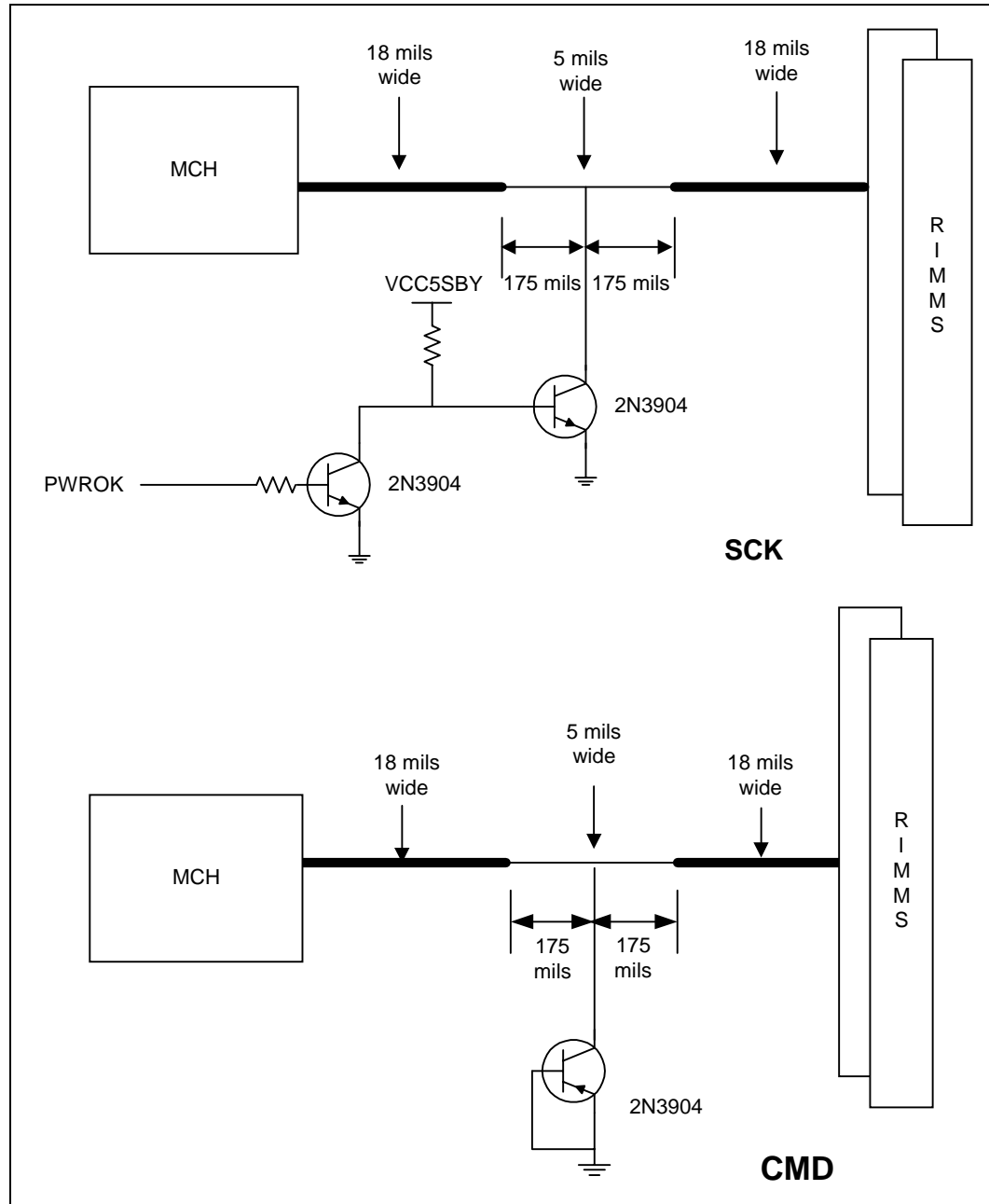
2.6.5 Direct Rambus* Clock Routing

Refer to Chapter 4, "Clocking" for Intel® 820 chipset platform Direct Rambus* clock routing guidelines.

2.6.6 Direct Rambus* Design Checklist

Use the following checklist as a final check to ensure the motherboard incorporates solid design practices. This list is only a reference. For correct operation, all of the design guidelines within this document must be followed.

Table 2-6. Signal List

RSL Signals	High-Speed CMOS Signals	Serial CMOS Signal	Clocks
DQA[8:0] DQB[8:0] RQ[7:0]	CMD SCK	SIO	CTM CTM# CFM CFM#

- Ground Isolation Well Grounded
  - Via to ground every ½ inch around edge of isolation island
  - Via to ground every ½ inch between RIMMs
  - Via to ground every ½ inch between signals (from MCH to first RIMM)
  - Via between every signal within 100mils of the MCH edge and the connector edge
  - No unconnected ground floods
  - All ground isolation at least 10 mils wide
  - Ground isolation fills between *serpentines*
  - Ground isolation not *broken* by C-TABs
  - Ground isolation connects to the ground pins in the middle of the RIMM connectors
  - Ground isolation vias connect on all 4 layers and should NOT have thermal reliefs
  - Ground pins in RIMM connector connect on all 4 layers
- Vterm Layout Yields Low Noise
  - Solid Vterm island is on top layer – do not split this plane
  - Ground island (for ground side of Vterm caps) is on top
  - Termination Resistors connect DIRECTLY to the Vterm island on the top layer (without vias)
  - Decoupling Vterm is CRITICAL!
  - Decoupling capacitors connect to top layer Vterm island and top layer ground island directly (see layout example)
  - Use AT LEAST 2 vias per decoupling capacitor in the top layer ground island
  - Use 2 x 100 uF TANTALUM capacitors to decouple Vterm (Aluminum/Electrolytic capacitors are too slow!)
  - High-frequency decoupling capacitors MUST be spread-out across the termination island so that all termination resistors are near high-frequency capacitors
  - 100uF TANTALUM capacitors should be at each end of the Vterm island
  - 100uF TANTALUM capacitors must be connected to Vterm island directly
  - 100uF TANTALUM capacitors must have AT LEAST 2 vias/cap to ground

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- — Vterm island should be 50 – 75 mils wide
- — Vterm island should not be broken
- — If any RSL signals are routed out of the last RIMM (towards termination) on the bottom side (even for a short distance), ensure Ground Reference Plane (on the third layer) is continuous under the termination resistors/capacitors
- — Ensure current path for power delivery to the MCH does not go through the Vterm island

- CTM/CTM# Routed Properly
  - — CTM/CTM# are routed differentially from DRCG to last RIMM
  - — CTM/CTM# are ground isolated from DRCG to last RIMM
  - — CTM/CTM# are ground referenced from DRCG to last RIMM
  - — Vias are placed in ground isolation and ground reference every ½"
  - — When CTM/CTM# serpentine together, they MUST maintain EXACTLY 6 mils spacing

- Clean DRCG Power Supply
  - — 3.3V DRCG power flood on the top layer. This should connect to each
  - — High frequency (0.1 uF) capacitors are near the DRCG power pins. One capacitor next to each power pin.
  - — 10uF bulk *tantalum* capacitor near DRCG connected directly to the 3.3V DRCG power flood on the top layer
  - — Ferrite bead isolating DRCG power flood from 3.3V main power also connecting directly to the 3.3VDRCG power flood on the top layer
  - — Use 2 vias on the ground side of each

- Good DRCG Output Network Layout
  - — Series resistors (39 Ω) should be VERY near CTM/CTM# pins
  - — Parallel resistors (51 Ω) should be very near series resistors
  - — CTM/CTM# should be 18mils wide from the CTM/CTM# pins to the resistors
  - — CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network
  - — When not 14 on 6, the clocks should be 18 mils wide
  - — Ensure CTM/CTM# are ground referenced and the ground reference is connected to the ground plane every ½" to 1"
  - — Ensure CTM/CTM# are ground isolated and the ground isolation is connected to the ground plane every ½" to 1"
  - — Ensure 15 pf EMI capacitors to ground are removed (the pads are not necessary and removing the pads provides more space for better placement of other components)
  - — Ensure the 4 pf EMI capacitor is implemented (but do not assemble the capacitor)

- Good RSL Transmission Lines
  - — RSL traces are 18 mils wide
  - — When RSL traces neck down to exit MCH BGA, the minimum width is 15 mils and the neckdown is no longer than 25 mils in length
  - — RSL traces do NOT neckdown when routing into the RIMM connector
  - — If tight serpentining is necessary, 10 mil ground isolation MUST be between serpentine segments (i.e., an RSL signal CAN NOT serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines).
  - — RSL traces do not cross power plane splits. RSL signals must also not be routed *on next to* a power plane splits (e.g., the RSL signals on the 4th layer can not be routed directly below the ground isolation split on the 3rd layer)
  - — Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times

— ALL RSL, CMD/SCK and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin

— All RSL signals are routed adjacent to a ground reference plane. This includes all signals from the last RIMM to the termination. If signals are routed on the bottom from the last RIMM to the termination, the ground reference plane on the 3rd layer MUST extend under these signals AND include the ground side of the Vterm decoupling capacitors.

— CTABs must not cross (or be on top of) power plane splits. They must be ENTIRELY referenced to ground.

— At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MCH (and the 1st RIMM) as possible. If possible connect the flood to the ground balls/pins on the MCH/connector.

- Clean V$_{REF}$ Routing

— Ensure 1 x 0.1 uF capacitor on V$_{REF}$ at each connector

— Use 10 mil wide trace (6 mils minimum)

— Do not route V$_{REF}$ near high-speed signals

- RSL Routing

— All signals must be length matched within ±10 mils of the Nominal RSL Length (note: use the table in the *Intel$^®$ 820 chipset: 82820 Memory Controller Hub (MCH)* Datasheet to verify trace lengths). Ensure that signals with a dummy via are compensated correctly.

— ALL RSL signals must have 1 via near the MCH BGA pad. Signals routed on the secondary side of the MB will have a "real via" while signals routed on the primary side will have a "dummy via". Additionally, all signals with a dummy via must have an additional trace length of 25 mils.

— "B" side RIMM connector signals are routed on the secondary side of the motherboard. "A" side RIMM connector signals are routed on the primary side of the motherboard.

— Signals must "alternate" layers as shown in the following table.

If Signal Routed from MCH to the 1st RIMM on:	Then Route Signal from 1st RIMM to Next RIMM on:
Primary Side	Secondary Side
Secondary Side	Primary Side

- Clock Routing

— Clock signals must be routed as a differential pair. The traces must be 14 mils wide and 6 mils apart (with no ground isolation) when they are routed as a differential pair. For very short sections under the MCH and under the 1st RIMM, it will not be possible to route as a differential pair. In these sections, the clocks signals MUST neck up to 18 mils and be ground isolated with at least 10 mils ground isolation.

— Clock signals must be length compensated (using the 1.021 length factor described in Section 2.7.3, "2X/4X Timing Domain Routing Guidelines" on page 2-33). Ensure that each clock pair is length matched within ±2 mils.

— When clock signals serpentine, they must serpentine together (to maintain differential 14:6 routing).

— 22 mils ground isolation required on each side of the differential pair.

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2.7   AGP 2.0

For detailed AGP Interface functionality (protocols, rules and signaling mechanisms, etc.) refer to the latest *AGP Interface Specification revision 2.0,* which can be obtained from http://www.agpforum.org. This document focuses only on specific Intel® 820 chipset platform recommendations.

The AGP Interface Specification revision 2.0 enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (4 data samples per clock) and 1.5 volt operation. In addition to these major enhancements, additional performance enhancement and clarifications, such as *fast write* capability, are included in the *AGP Interface Specification, Revision 2.0*. The Intel® 820 chipset is the first Intel chipset that supports the enhanced features of AGP 2.0.

The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. That is, data is sampled four times during each 66 MHz AGP clock. This means that each data cycle is ¼ of a 15 ns (66 MHz) clock or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66 MHz clock cycle; therefore, the data cycle time is 7.5 ns.

To allow for these high speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing (refer to Section 2.5, "Source Synchronous Strobing" on page 2-5). During 4X operation, the AGP interface uses differential source synchronous strobing.

With data cycle times as small as 3.75 ns, and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5V) requires even more noise immunity. For example, during 1.5V operation, V_{ilmax} is 570 mv. Without proper isolation, crosstalk could create signal integrity issues.

2.7.1   AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: *1X timing domain signals*, *2X/4X timing domain signals* and *miscellaneous signals*. Each group has different routing requirements. In addition, within the *2X/4X timing domain signals*, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. However, trace length matching requirements only need to be met within each set of 2X/4X timing domain signals.

Signal groups

- 1X Timing Domain
  — CLK (3.3V)
  — RBF#
  — WBF#
  — ST[2:0]
  — PIPE#
  — REQ#
  — GNT#
  — PAR
  — FRAME#
  — IRDY#
  — TRDY#
  — STOP#
  — DEVSEL#

- 2X/4X Timing Domain

  Set #1
  — AD[15:0]
  — C/BE[1:0]#
  — AD_STB0
  — AD_STB0# (used in 4X mode ONLY)

  Set #2
  — AD[31:16]
  — C/BE[3:2]#
  — AD_STB1
  — AD_STB1# (used in 4X mode ONLY)

  Set #3
  — SBA[7:0]
  — SB_STB
  — SB_STB# (used in 4X mode ONLY)

- Miscellaneous, Async
  — USB+
  — USB-
  — OVRCNT#
  — PME#
  — TYPDET#
  — PERR#
  — SERR#
  — INTA#
  — INTB#

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Table 2-7. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section the term *data* refers to AD[31:0], C/BE[3:0]# and SBA[7:0]. The term *strobe* refers to AD_STB[1:0], AD_STB#[1:0], SB_STB and SB_STB#. When the term *data* is used, it is referring to one of the three sets of data signals. When the term *strobe* is used, it is referring to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (*1X timing domain signals*, *2X/4X timing domain signals* and *miscellaneous signals)* will be addressed separately.

2.7.2   1X Timing Domain Routing Guidelines

- The AGP 1X timing domain signals (refer to Signal Groups previously shown) have a maximum trace length of 7.5 inches. This maximum applies to ALL of the signals listed as 1X timing domain signals in Signal Groups section.

- AGP 1X timing domain signals can be routed with 5 mil minimum trace separation.

- There are no trace length matching requirements for 1X timing domain signals.

2.7.3   2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

The maximum line length and length mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6") and the long AGP interfaces (e.g., > 6" and < 7.25") are documented separately. The maximum length allowed for the AGP interface is 7.25 inches.

Interfaces < 6"

If the AGP interface is less than 6 inches, a minimum 1:3 trace spacing is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched their associated strobe within ±0.5 inches. These guidelines are for designs that require less than 6 inches between the AGP connector and the MCH.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3" long, the data signals which are associated to those strobe signals (e.g., AD[15:0] and C/BE[2:0]#), can be 4.8" to 5.8" long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2" long, and the data signals which are associated to those strobe signals (e.g., SBA[7:0]), can be 3.7" to 4.7" long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1" (i.e., a strobe and its compliment must be the same length within 0.1").

Figure 2-29. AGP 2X/4X Routing Example for Interfaces < 6"
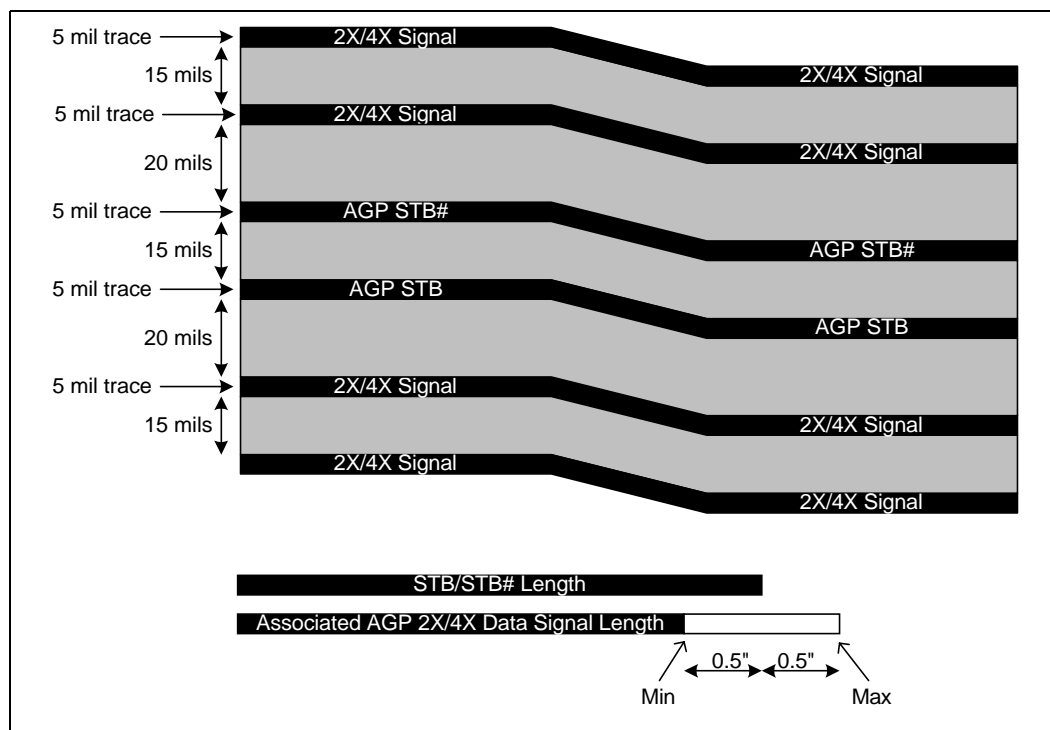
Interfaces > 6" and < 7.25"

Longer lines have more crosstalk; therefore, to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 6 inches and less than 7.25 inches, 1:4 routing is required for all data lines and strobes. For these designs, the line length mismatch must be less than ±0.125" within each signal group (between all data signals and the strobe signals).

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5" long, the data signals which are associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#), can be 6.475" to 6.625" long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2" long, and the data signals that are associated with those strobe signals (e.g., SBA[7:0]), can be 6.075" to 6.325" long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them.

This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1" (i.e., a strobe and its compliment must be the same length within 0.1").

All AGP Interfaces

The 2X/4X Timing Domain Signals can be routed with 5 mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.3" of the MCH package. When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

Reduce line length mismatch to insure added margin. In order to reduce trace to trace coupling (cross talk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

2.7.4   AGP 2.0 Routing Summary

Table 2-8. AGP 2.0 Routing Summary[1,2]

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	7.5"	5 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	7.25"	20 mils	±0.125"	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	7.25"	20 mils	±0.125"	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	7.25"	20 mils	±0.125"	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length
2X/4X Timing Domain Set#1	6"	15 mils[1]	±0.5"	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6"	15 mils[1]	±0.5"	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6"	15 mils[1]	±0.5"	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils
2. These guidelines apply to board stackups with 10% impedance tolerance

2.7.5 AGP Clock Routing

The maximum total AGP clock skew (between the MCH and the graphics component) is 1 ns for all data transfer modes. This 1 ns includes skew and jitter which originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but at all points on the clock edge that fall in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer). For Intel® 820 chipset platform AGP clock routing guidelines, refer to Chapter 4, "Clocking".

2.7.6 General AGP Routing Guidelines

The following routing guidelines are recommended for an optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the 82820 MCH. The guidelines below are not intended to replace thorough system validation on Intel® 820 chipset based products.

Recommendations

Decoupling

- For VDDQ decoupling, a minimum of six (6) 0.01 uF capacitors are required and at least four (4) must be within 70 mils of the outer row of balls on the MCH. (see Figure 2-30).

- Evenly distribute placement of decoupling capacitors among the AGP interface signal field.

- Use a low ESL ceramic capacitor (e.g., 0603 body type, X7R dielectric).

- In addition to the minimum decoupling capacitors, bypass capacitors should be placed at vias that transition AGP signals from one reference signal plane to another. *On a typical four layer PCB design the signals transition from one side of the board to the other.*

- One extra 0.01 uF capacitor is required per 10 vias. The capacitor should be placed as close to the center of the via field as possible.

- Ensure that the AGP connector is well decoupled as described in the *AGP Design Guide, Revision 1.0 (Section 1.5.3.3).*

Note: To add the decoupling capacitors close as possible to the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1" maximum).

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Figure 2-30. Top Signal Layer

Must add six 0.01 uF ceramic 603 Type Capacitors
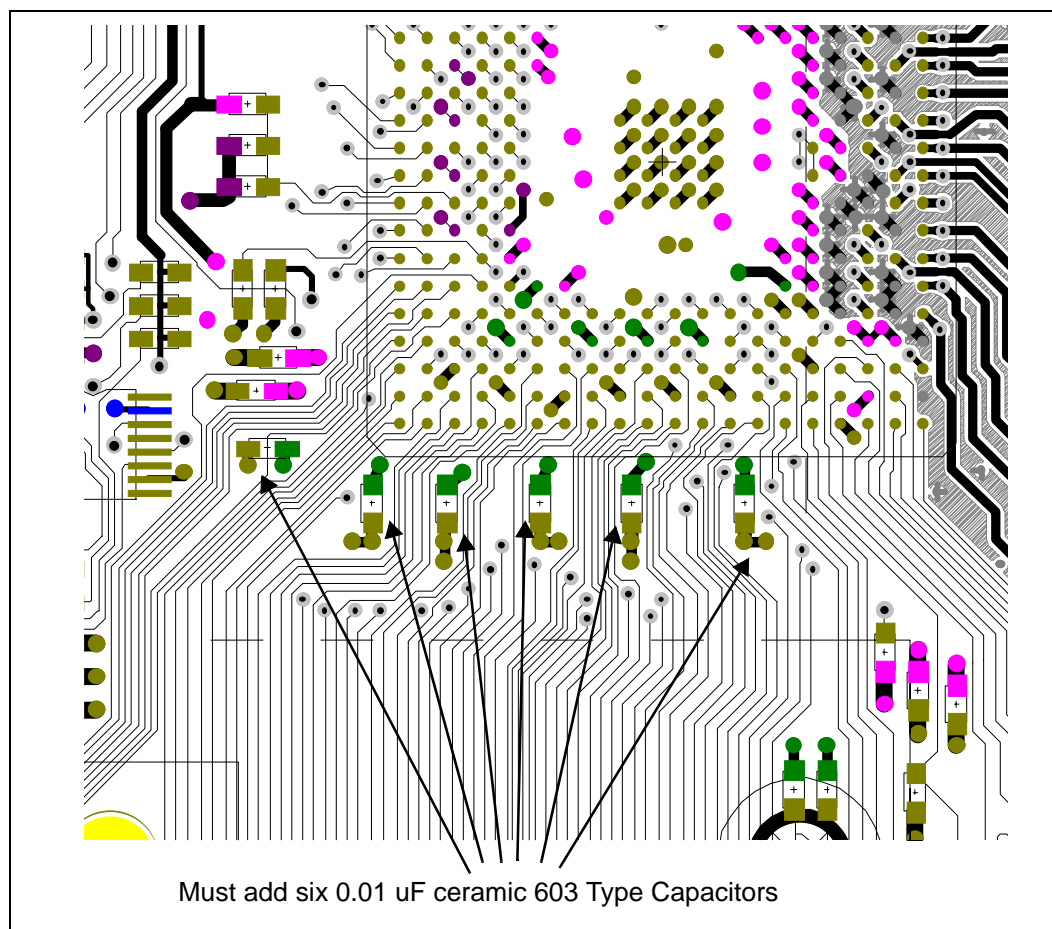
Ground Reference

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector (or to an AGP video controller if implemented as a "down" solution) utilizing a minimum number of vias on each net; AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT# and ST[2:0].

In addition to the minimum signal set listed above, it is strongly recommended that half of all your AGP signals be reference to ground depending on board layout. An ideal design would have the complete AGP interface signal field referenced to ground.

The recommendations above are not specific to any particular PCB stackup, but are applied to all Intel® Chipset designs.

2.7.7   VDDQ Generation and TYPEDET#

AGP specifies two separate power planes (VCC and VDDQ). VCC is the core power for the graphics controller. VCC is **always** 3.3V. VDDQ is the interface voltage. In AGP 1.0 implementations VDDQ was also 3.3V. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ as both are tied to the 3.3V power plane on the motherboard.

AGP 2.0 requires that these power planes be separate. In conjunction with the 4X data rate, the AGP 2.0 Interface Specification provides for low-voltage (1.5V) operation. The AGP 2.0 Specification implements a TYPEDET# (type detect) signal on the AGP connector that determines the operating voltage of the AGP 2.0 interface (VDDQ). The motherboard must provide either 1.5V or 3.3V to the add-in card depending on the state of the TYPEDET# signal (refer to Table 2-9. The 1.5V low-voltage operation applies ONLY to the AGP interface (VDDQ); VCC is **always** 3.3V.

Note: The motherboard provides 3.3V to the Vcc pins of the AGP connector. If the graphics controller needs a lower voltage, then the add-in card must regulate the 3.3V VCC voltage to the controller's requirements. The graphics controller may ONLY power AGP I/O buffers with the VDDQ power pins.

The TYPEDET# signal indicates whether the AGP 2.0 interface operates 1.5 volts or 3.3 volts. If TYPEDET# is floating (no connect) on an AGP add-in card, the interface is 3.3 volts. If TYPEDET# is shorted to ground, the interface is 1.5 volts.

Table 2-9. TYPDET#/VDDQ Relationship

TYPEDET# (on add-in card)	VDDQ (supplied by MB)
GND	1.5V
N/C	3.3V

As a result of this requirement, the motherboard must provide a *flexible* voltage regulator. This regulator must supply the appropriate voltage to the VDDQ pins on the AGP connector. For specific design recommendations, refer to the schematics in Appendix A, "Reference Design Schematics: Uni-Processor" and Appendix B, "Reference Design Schematics: Dual-Processor". VDDQ generation and AGP V_{REF} generation must be considered together. Before developing VDDQ generation circuitry, refer to the AGP 2.0 Interface Specification.

Figure 2-31 demonstrates one way to design the VDDQ voltage regulator. This regulator is a linear regulator with an external, low R_{DS-ON} FET. The source of the FET is connected to 3.3V. This regulator will convert 3.3V to 1.5V or pass 3.3V depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3V (not 5V) in order to control thermals (i.e., 5V regulated down to 1.5V with a linear regulator will dissipate approximately 7W at 2A). Because it must draw power from 3.3V and, in some situations, must simply pass that 3.3V to VDDQ (when a 3.3V add-in card is placed in the system), the regulator MUST use a low R_{dson} FET.

AGP 1.0 modified VDDQ3.3$_{min}$ to 3.1V. Using an ATX power supply; the 3.3V$_{min}$ is 3.168V. Therefore, 68 mV of drop is allowed across the FET at 2A. This corresponds to a FET with an R_{dson} of 34 mW.

How does the regulator switch? The feedback resistor divider is set to 1.5V. When a 1.5V card is placed in the system, the transistor is off and the regulator regulates to 1.5V. When a 3.3V card is placed in the system, the transistor is on, and the feedback is pulled to ground. When this happens, the regulator drives to gate of the FET to nearly 12V. This turns the FET on and passes 3.3V - 2A * R_{DS-ON} to VDDQ.

Figure 2-31. AGP VDDQ Generation Example Circuit
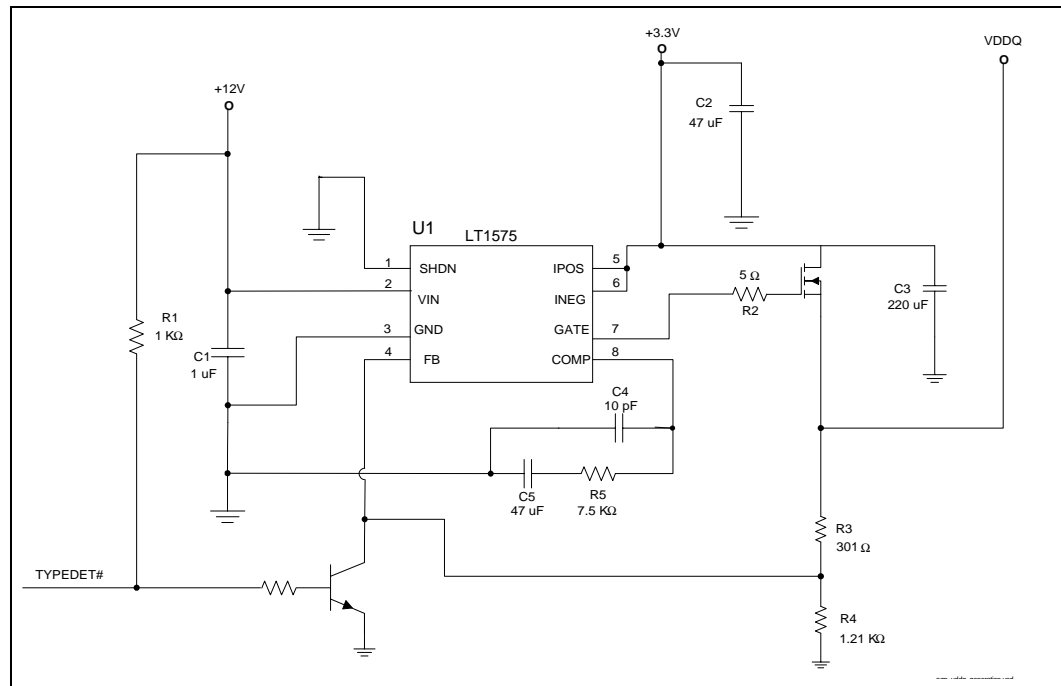
2.7.8 V_{REF} Generation for AGP 2.0 (2X and 4X)

V_{REF} generation for AGP 2.0 will be different depending on the AGP card type used. The 3.3V AGP cards generate V_{REF} locally (i.e., they have a resistor divider on the card that divides VDDQ down to V_{REF}) as shown in Figure 2-32. To account for potential differences between VDDQ and GND at the MCH and graphics controller, 1.5V cards use source generated V_{REF} (i.e., the V_{REF} signal is generated at the graphics controller and sent to the MCH, and another V_{REF} is generated at the MCH and sent to the graphics controller). Refer to Figure 2-32.

Both the graphics controller and the MCH are required to generate V_{REF} and distribute it through the connector (1.5V add-in cards only). There are two pins defined on the AGP 2.0 universal connector to allow this V_{REF} passing. These pins are:

- V_{REF}GC   - Vref from the graphics controller to the chipset
- V_{REF}CG   - Vref from the chipset to the graphics controller

To preserve the common mode relationship between the V_{REF} and data signals, it is important the routing of the two Vref signals must be matched in length to the strobe lines within 0.5 inches on the motherboard and within 0.25 inches on the add-in card.

The voltage divider networks consists of AC and DC elements as shown in the figure.

The V_{REF} divider network should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the V_{REF} signals must be a minimum of 25 mils to reduce cross-talk and maintain signal integrity.

During 3.3V AGP 2.0 operation, V_{REF} must be 0.4VDDQ. However, during 1.5V AGP 2.0 operation, Vref must be 0.5VDDQ. This requires a flexible voltage divider for V_{REF}. Various methods of accomplishing this exist, and one such example is shown in Figure 2-32.

Figure 2-32. AGP 2.0 VREF Generation & Distribution

+12V

1.5V AGP Card

R7 1K

Note: R7 is the same resistor seen in AGP VDDQ Generation Example Circuit Figure (R1)

TYPEDET#

VrefGC

R9 300 1%

R11 200 1%

VDDQ

500pF C8

U6

mosfet

VDDQ

AGP Device

REF

GND

VDDQ

REF **MCH**

GND

0.1uF C10

R6 1K

R5 82

R2 1K

R4 82

500pF C9

Place C10 close to the MCH

VrefCG

The resistor dividers should be placed near the MCH. Both VrefGC and VrefCG signals must be 5 mils wide and routed 25 mils from adjacent signals.

+12V

3.3V AGP Card

R7 1K

Note: R7 is the same resistor seen in AGP VDDQ Generation Example Circuit Figure (R1)

TYPEDET#

VrefGC

R9 300 1%

R11 200 1%

VDDQ

500pF C8

U6

mosfet

VDDQ

AGP Device

REF

GND

VDDQ

REF **MCH**

GND

0.1uF C10

R6 1K

R5 82

R2 1K

R4 82

500pF C9

Place C10 close to the MCH

VrefCG

The resistor dividers should be placed near the MCH. Both VrefGC and VrefCG signals must be 5 mils wide and routed 25 mils from adjacent signals.

The flexible V_{REF} divider shown in Figure 2-32 uses a FET switch to switch between the locally generated V_{REF} (for 3.3V add-in cards) and the source generated V_{REF} (for 1.5V add-in cards).

Usage of the source generated V_{REF} at the receiver is optional and is a product implementation issue which is beyond the scope of this document.

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2.7.9   Compensation

The MCH AGP interface supports resistive buffer compensation (RCOMP). Tie the GRCOMP pin to a 40 Ω 2% (or 39 Ω 1%) pull-down resistor (to ground) via a 10 mil wide, very short (<0.5") trace.

2.7.10   AGP Pull-ups

AGP control signals require pull-up resistors to VDDQ on the motherboard to ensure they contain stable values when no agent is actively driving the bus. The signals requiring pull-up resistors are:

- 1X Timing Domain Signals
    — FRAME#
    — TRDY#
    — IRDY#
    — DEVSEL#
    — STOP#
    — SERR#
    — PERR#
    — RBF#
    — PIPE#
    — REQ#
    — WBF#
    — GNT#
    — ST[2:0]

It is critical that these signals are pulled up to VDDQ (NOT 3.3V).

The trace stub to the pull-up resistor on 1X timing domain signals should be kept to less than 0.5 inch to avoid signal reflections from the stub.

The strobe signals require pull-up/pull-downs on the motherboard to ensure they contain stable values when no agent is driving the bus.

Note: INTA# and INTB# should be pulled to 3.3V – not VDDQ.

- 2X/4X Timing Domain Signals

    — AD_STB[1:0]   (pull-up to VDDQ)

    — SB_STB   (pull-up to VDDQ)

    — AD_STB[1:0]#   (pull-down to ground)

    — SB_STB#   (pull-down to ground)

The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept to less than 0.1 inch to avoid signal reflections from the stub.

The pull-up/pull-down resistor value requirements are shown in the table below:

Rmin	Rmax
4 KΩ	16 KΩ

The recommended AGP pull-up/pull-down resistor value is 8.2 KΩ.

2.7.10.1   AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3V tolerant during 1.5V operation:

- PME#
- INTA#
- INTB#
- GPERR#
- GSERR#
- CLK
- RST

The following signals on the AGP interface are 5V tolerant (refer to the USB specification):

- USB+
- USB-
- OVRCNT#

The following signal is a special AGP signal. It is either Grounded or No Connected on an AGP card.

- TYPEDET#

Note: **All other signals on the AGP interface are in the VDDQ group. They are not 3.3V tolerant during 1.5V AGP operation.**

2.7.11   Motherboard / Add-in Card Interoperability

Currently, there are three AGP connectors:

- 3.3V AGP connector
- 1.5V AGP connector
- Universal AGP connector.

To maximize add-in flexibility, implementing the universal connector in Intel® 820 chipset based system is strongly recommended. All add-in cards are either 3.3V or 1.5V cards. Due to timings, 4X transfers at 3.3V are not allowed.

Table 2-10. Connector/Add-in Card Interoperability

	1.5V Connector	3.3V Connector	Universal Connector
1.5V Card	Yes	No	Yes
3.3V Card	No	Yes	Yes

Table 2-11. Voltage/Data Rate Interoperability

	1X	2X	4X
1.5V VDDQ	Yes	Yes	Yes
3.3V VDDQ	Yes	Yes	No

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2.8 Hub Interface

The MCH and ICH ball assignments have been optimized to simplify hub interface routing. It is recommended that the hub interface signals be routed directly from the MCH to the ICH on the top signal layer (they do not need to be run through vias) (refer to).

The hub interface is broken into two signal groups: data signals and strobe signals. These groups are:

- Data Signals
    - HL[10:0]
- Strobe Signals
    - HL_STB
    - HL_STB#

Note: HL_STB/HL_STB# is a differential strobe pair.

There are no pull-ups or pull-downs required on the hub interface.

Each signal must be routed such that it meets the guidelines documented for the signal group to which it belongs.

Figure 2-33. Hub Interface Signal Routing Example
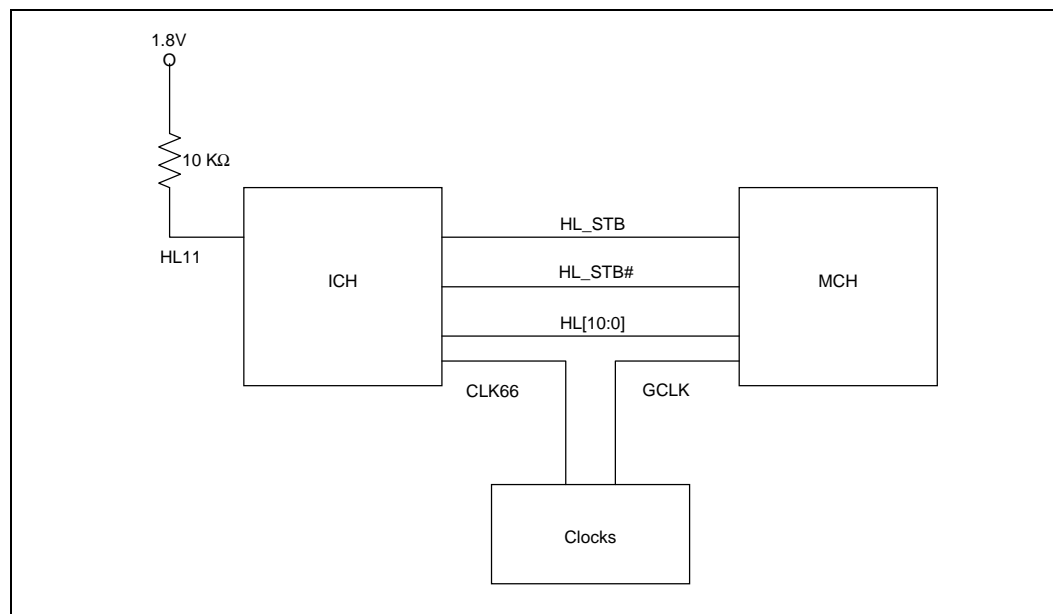
2.8.1   Data Signals

The Hub interface data signals (HL[10:0]) should be routed 5 on 20. These signals can be routed 5 on 15 for navigation around components or mounting holes. In order to break-out of the MCH uBGA and the ICH uBGA, the hub interface data signals can be routed 5 on 5. The signals must be separated to 5 on 20 within 300 mil of the uBGA package.

The maximum trace length for the hub interface data signals is 7". These signals must each be matched within ±0.1" of the HL_STB and HL_STB# signals.

2.8.2   Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 7" and the two strobes must be the same length. Additionally, the trace length for each data signal must be matched to the trace length of the strobes with ±0.1".

2.8.3   HREF Generation/Distribution

HREF is the hub interface reference voltage. It is $0.5 * 1.8V = 0.9V$ ±2%. It can be generated using a single HREF divider or locally generated dividers (as shown in Figure 2-34 and Figure 2-35). The resistors should be equal in value and rated at 1% tolerance (to maintain 2% tolerance on 0.9V). The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from minimum 100 ohm to maximum 1K ohm (300 ohm shown in example).

The single HREF divider should not be located more than 4" away from either MCH or ICH. If the single HREF divider is located more than 4" away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01 uF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor needs to be close to the component HREF pin.

Figure 2-34. Single Hub Interface Reference Divider Circuit

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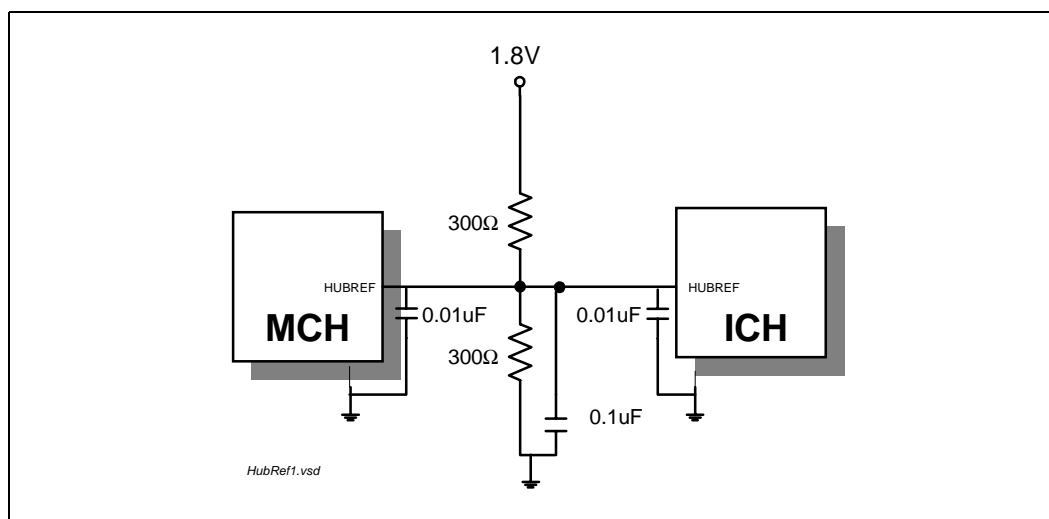
Figure 2-35. Locally generated Hub Interface Reference Dividers
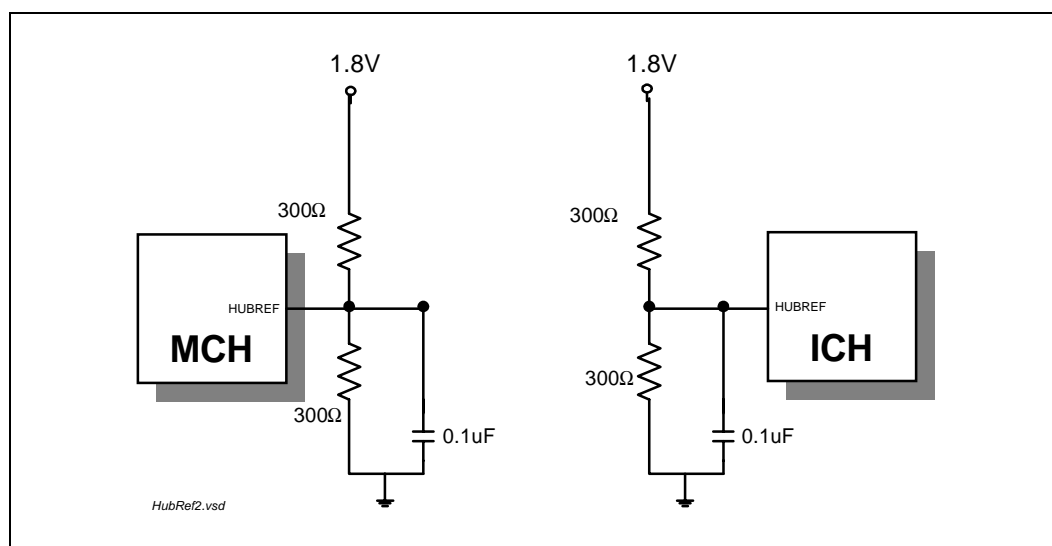
2.8.4 Compensation

There are two options for the ICH hub interface compensation (HLCOMP). HLCOMP is used by the ICH to adjust buffer characteristics to specific board characteristics. Refer to the ICH Datasheet for details on compensation. It can be used as either Impedance Compensation (ZCOMP) or Resistive Compensation (RCOMP). The guidelines are below:

- **RCOMP:** Tie the COMP pin to a 40 Ω 2% (or 39 Ω 1%) pull-up resistor (to 1.8V) via a 10 mil wide, very short (<0.5") trace.

- **ZCOMP:** The COMP pin must be tied to a 10 mil trace that is AT LEAST 18" long. This trace must be unterminated and care should be taken when routing the signal to avoid crosstalk (15–20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

The MCH also has a hub interface compensation pin. This signal (HLCOMP) can be routed using either the RCOMP method or ZCOMP method described for the ICH.

2.9 System Bus Design

2.9.1 100/133 MHz System Bus

First, determine the approximate location of the processor and the chip set on the base board. An example topology is shown in Figure 2-36. This example "star" topology is valid for 133 MHz and 100 MHz 2-way processor/Intel® 820 chipset designs. The 82820 MCH should be placed electrically in the center of the bus. The SC242 connectors should be placed on either end of the bus to allow the processors to terminate each end.

Table 2-12 below provides segment descriptions and length recommendations for the investigated topology shown in Figure 2-36. Segment lengths are defined at the pins of the devices or components. For 2-way processor / Intel® 820 chipset designs, a termination card must be placed in the unused slot when only one processor is populated. This is necessary to ensure signal integrity requirements are met.

Figure 2-36. Intel® Pentium® III Processor Dual Processor Configuration
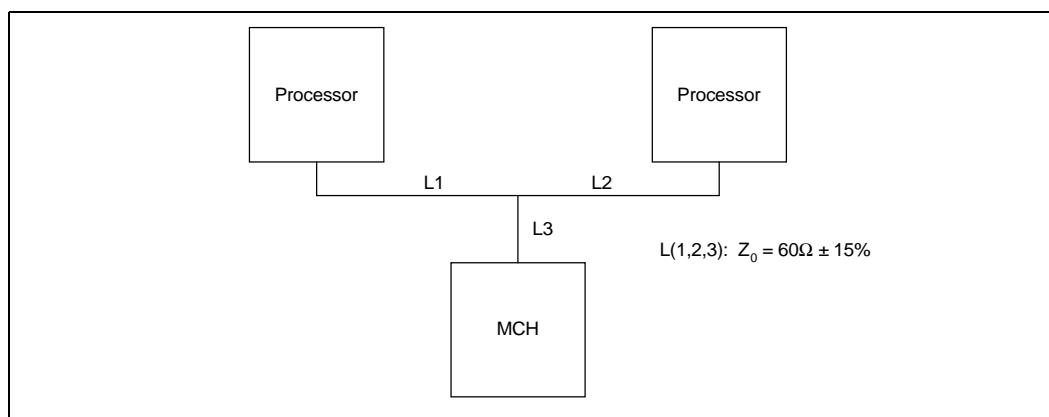
Table 2-12. Segment Descriptions and Lengths for Figure 2-36

Segment	Description	Min length (inches)	Max length (inches)
L1	SC242 connector to Centerpoint	1.5	3.0
L2	SC242 connector to Centerpoint	1.5	3.0
L3	Chip set breakout stub	0.0	1.5
L1+L3 or L2+L3	SC242 distance from MCH	2.0	4.5
L1 + L2	SC242 spacing		5.5

Figure 2-37 shows the topology and trace lengths required for single processor designs.

Figure 2-37. Intel® Pentium® III Processor Uni-Processor Configuration
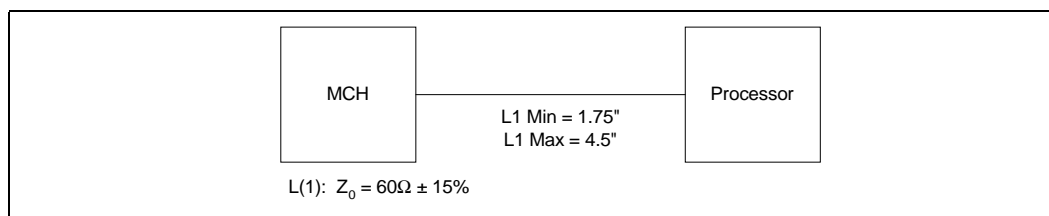
2.9.2   System Bus Ground Plane Reference

All system bus signals must be referenced to GND to provide optimal current return path. The
ground reference must be continuous from the MCH to the SC242 connector. This may require a
GND reference island on the plane layers closest to the signals. Any split in the ground island will
provide a sub-optimal return path. In a 4 layer board, this will require the VCCID island to be on an
outer signal layer. Figure 2-38 shows a four layer motherboard power plane with ground reference
for system bus signals.

Figure 2-38. Ground Plane Reference (Four Layer Motherboard)
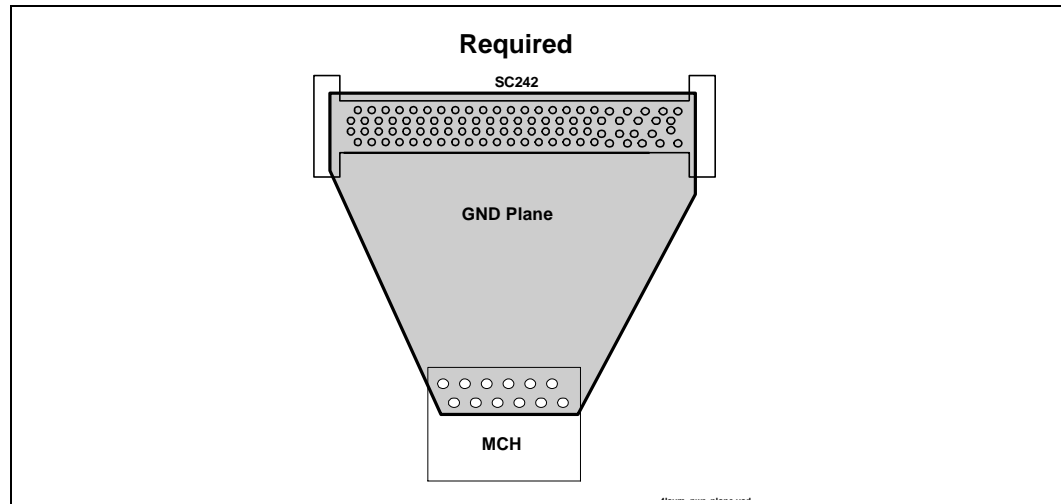
2.10   S.E.C.C. 2 Grounding Retention Mechanism (GRM)

Intel is enabling a new S.E.P.P. (Single Edge Processor Package) style retention mechanism which
will provide a grounding path for the heatsink on processors in the S.E.C.C. 2 package. This
solution is referred to as the S.E.C.C.2 (Single Edge Contact Cartidge 2) Grounding Retention
Mechanism (GRM). OEMs who choose to utilize this new solution will need to add grounding
pads on the primary side of the motherboard which will interface with the enabled GRM. If the
motherboard or heat sink do not have the proper interfaces, the GRM may not be utilized to its full
ability and damage could occur to the motherboard.

The most notable interface requirement to accommodate the GRM is the addition of grounding
pads around two of the Retention Mechanism (RM) mounting holes within the existing RM keep-
out zone on the motherboard. The other interface is a contact area on the heat sink flanges. The
interface size and locations for the motherboard are discussed in detail further in this section.

The reference design GRM is asymmetric, and requires 0.159" mounting holes. To minimize the
impact to trace routing, only two ground pads are required. This makes it necessary to key the
GRM to prevent the ground clips from being installed on the soldermask instead of the grounding
pads. This keying is accomplished by making the GRM asymmetric. The requirement for the
0.159" mounting holes is for the supported plastic fastener attachment mechanism.

Motherboard Interfaces

Figure 2-39 shows the Hole Locations and Keepout Zones For Support Components (from the motherboard surface to 0.100" above the motherboard surface.).

Figure 2-39. Hole Locations and Keepout Zones For Support Components[1,2]
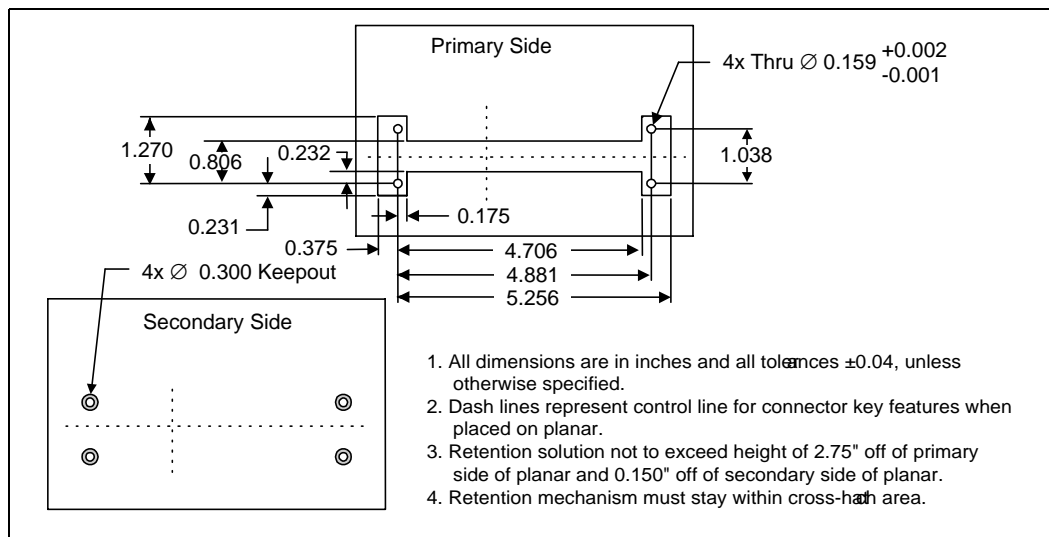
NOTES:
1. The dashed lines represent the centerlines for the connector keying features.
2. Drawing not to scale

Figure 2-40 shows the dimensions of the grounding pad needed to ground the heat sink.

Figure 2-40. Grounding Pad Dimensions for the SECC2 GRM
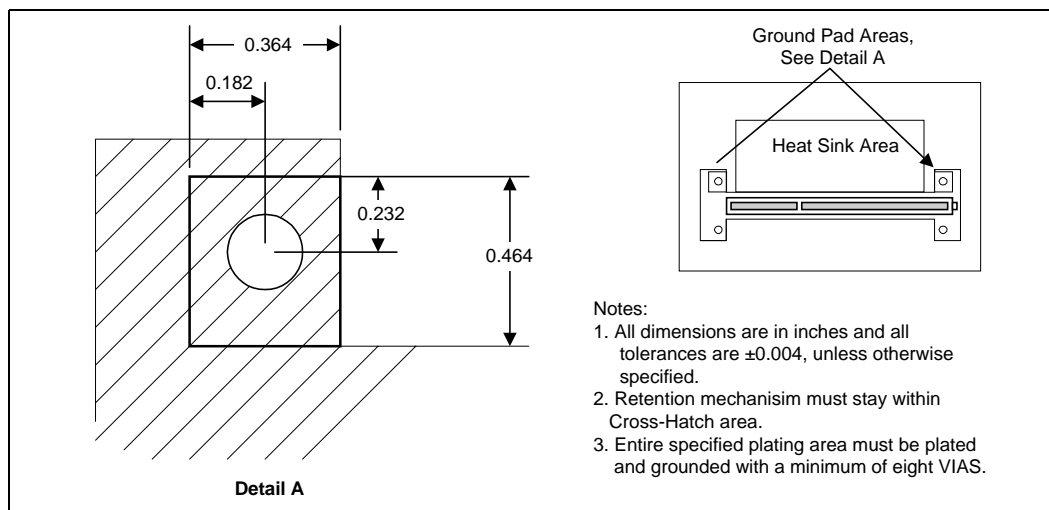
NOTE: Drawing not to scale.

It is not recommended to use the GRM without the minimum size ground pads in the correct locations. If the GRM is used without the correct pads, then there is a high risk that the metal clip that grounds to the motherboard will be touching the solder mask on the top layer of the board, and possibly short out traces immediately beneath the solder mask, resulting in board failure. The required thickness of the pad is less than 0.001" (using 1/2 oz. copper).

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2.11　Processor CMOS Pullup Values

Table 2-13 contains the pullup values for the Intel® Pentium® III processor with the Intel® 820 chipset. This table supports both single and dual processor configurations.

Table 2-13. Processor and 82820 MCH Connection Checklist[1,2]

CPU Pin	UP Pin Connection (CPU0)	DP Pin Connection (CPU1)
AGTL+ Signals		
A[35:3]# [1]	Connect A[31:3]# to MCH. Leave A[35:32]# as N/C (not supported by chipset).	Connect A[31:3]# to 2nd processor
ADS# [1]	Connect to MCH	Connect to 2nd processor
AERR#	Leave as N/C (not supported by chipset).	Leave as N/C
AP[1:0]#	Leave as N/C (not supported by chipset).	Leave as N/C
BERR#	Leave as N/C (not supported by chipset).	Leave as N/C
BINIT#	Leave as N/C (not supported by chipset).	Leave as N/C
BNR# [1]	Connect to MCH	Connect to 2nd processor
BP[3:2]#	Leave as N/C	Leave as N/C
BPM[1:0]	Leave as N/C	Leave as N/C
BPRI# [1]	Connect to MCH	Connect to 2nd processor
BREQ0# (BR0#)	10 Ω pull down to GND	See and
BREQ1# (BR1#)	Leave as N/C	See and
D[63:0]# [1]	Connect to MCH	Connect to 2nd processor
DBSY# [1]	Connect to MCH	Connect to 2nd processor
DEFER# [1]	Connect to MCH	Connect to 2nd processor
DEP[7:0]#	Leave as N/C (not supported by chipset).	Leave as N/C
DRDY# [1]	Connect to MCH	Connect to 2nd processor
HIT# [1]	Connect to MCH	Connect to 2nd processor
HITM# [1]	Connect to MCH	Connect to 2nd processor
LOCK# [1]	Connect to MCH	Connect to 2nd processor
REQ[4:0]# [1]	Connect to MCH	Connect to 2nd processor
RESET# [1]	Connect to MCH, 240 Ω series resistor to ITP	Connect to 2nd processor
RP#	Leave as N/C (not supported by chipset).	Leave as N/C
RS[2:0]# [1]	Connect to MCH	Connect to 2nd processor
RSP#	Leave as N/C (not supported by chipset).	Leave as N/C
TRDY# [1]	Connect to MCH	Connect to 2nd processor

Table 2-13. Processor and 82820 MCH Connection Checklist[1,2] (Continued)

CPU Pin	UP Pin Connection (CPU0)	DP Pin Connection (CPU1)
CMOS Signals		
A20M#	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
FERR#	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
FLUSH#	150 Ω pull up to Vcc2.5 (not used by chipset).	Connect to 2nd processor
IERR#	150 Ω pull up to Vcc2.5 if tied to custom logic or leave as N/C (not used by chipset).	Connect to 2nd processor
IGNNE#	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
INIT#	150 Ω pull up to Vcc2.5, connect to ICH and FWH Flash BIOS	Connect to 2nd processor
LINT0/INTR	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
LINT1/NMI	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
PICD[1:0]	150 Ω pull up to Vcc2.5, connect to ICH	Two 300–330 Ω pull ups to Vcc2.5 located at each end of trace. Connect to 2nd processor
PREQ#	~200–330 Ω pull up to Vcc2.5, connect to ITP pin 16	~200–330 Ω pull up to Vcc2.5, connect to ITP pin 20
PWRGOOD	150–330 Ω pull up to 2.5V, output from the PWRGOOD logic	Connect to 2nd processor
SLP#	150 Ω pull up to Vcc2.5, connect to ICH	
SMI#	150 Ω pull up to Vcc2.5, connect to ICH	
STPCLK#	150 Ω pull up to Vcc2.5, connect to ICH	
THERMTRIP#	150 Ω pull up to Vcc2.5 and connect to power off logic or ASIC, or leave as N/C	Connect to 2nd processor. Could tie separately to a monitoring ASIC.
TAP Signals		
PRDY#	150 Ω pull up to V_{TT}, 240 Ω series resistor to ITP pin 18	150 Ω pull up to V_{TT}, 240 Ω series resistor to ITP pin 22
TCK	1k Ω pull up to Vcc2.5, 47 Ω series resistor to ITP pin 5	Each processor should receive a separately buffered copy of TCK from the ITP. Tank circuit is optional for signal integrity. See
TDO	150 Ω pull up to Vcc2.5 and connect to ITP 10	TDO of CPU1 is connected to the ITP TDO pin 10. Pull up both sets of TDI/TDO nets as described.
TDI	~150–330 Ω pull up to Vcc2.5 and connect to ITP pin 8	TDI of CPU0 is connected to the ITP pin 8, TDI of CPU1 is connected to TDO of CPU0. Pull up both sets of TDI/TDO nets as described.
TMS	1 KΩ pull up to Vcc2.5, 47 Ω series resistor to ITP pin 7	Each processor should receive a separately buffered copy of TMS from the ITP. Tank circuit is optional for signal integrity. See
TRST#	~680 Ω pull down, connect to ITP pin 12	Connect to 2nd processor

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Table 2-13. Processor and 82820 MCH Connection Checklist[1,2] (Continued)

CPU Pin	UP Pin Connection (CPU0)	DP Pin Connection (CPU1)
Clock Signals		
BCLK	Connect to CK133. 22 – 33 Ω series resistor (Though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the MCH and processor.	Use separate BCLK from TAP and CPU0, or use ganged clock. Terminate as described.
PICCLK	Connect to CK133. 22 – 33 Ω series resistor (Though OEM needs to simulate based on driver characteristics)	Use separate PICCLK from CPU0. Terminate as described.
Other Signals		
BSEL0	100/133 MHz support: 220 Ω pull up to 3.3V, connected to PWRGOOD logic such that a logic low on BSEL0 negates PWRGOOD	Connect to 2nd processor
BSEL1	220 Ω pull up to 3.3V, connect to CK133 SEL133/100# pin. Connect to MCH HL10 pin via 8.2 KΩ series resistor.	Connect to 2nd processor
EMI[5:1]	Tie to GND. Zero ohm resistors are an option instead of direct connection to GND.	Implement in same manner as CPU0.
SLOTOCC#	Tie to GND, leave it N/C, or could be connected to powergood logic to gate system from powering on if no processor is present. If used, 1 KΩ – 10 KΩ pull up to any voltage.	Implement in same manner as CPU0.
TESTHI	1 K –100 KΩ pull up to Vcc2.5 If a legacy design pulls this up to VCC$_{CORE}$, use a 1 KΩ – 10 KΩ pull up	Implement in same manner as CPU0.
VID[4:0]	Connect to on-board VR or VRM. For on-board VR, 10 KΩ pull up to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.	Implement in same manner as CPU0. CPU0 and CPU1 should have different VR/VRMs.
Power		
VCC$_{CORE}$	Connect to core voltage regulator. Provide high & low frequency decoupling.	Implement in same manner as CPU0.
V$_{TT}$	Connect to 1.5V regulator. Provide high and low frequency decoupling.	Implement in same manner as CPU0.
No Connects		
Reserved	The following pins must be left as no-connects: A16, A47, A88, A113, A116, B12, B20, B76, and B112.	Implement in same manner as CPU0.

NOTES:
1. For single processor designs, the AGTL+ bus can be dual-ended or single-ended termination based on simulation results. Single-ended termination is provided by the processor.
2. This checklist supports Intel® Pentium® II processors at all current speeds, Intel® Pentium® III processors to a FMB guideline of 19.3A, and future Intel® Pentium® III processors to the current FMB guideline of 18.4A.

Figure 2-41. TCK/TMS Implementation Example for DP Designs
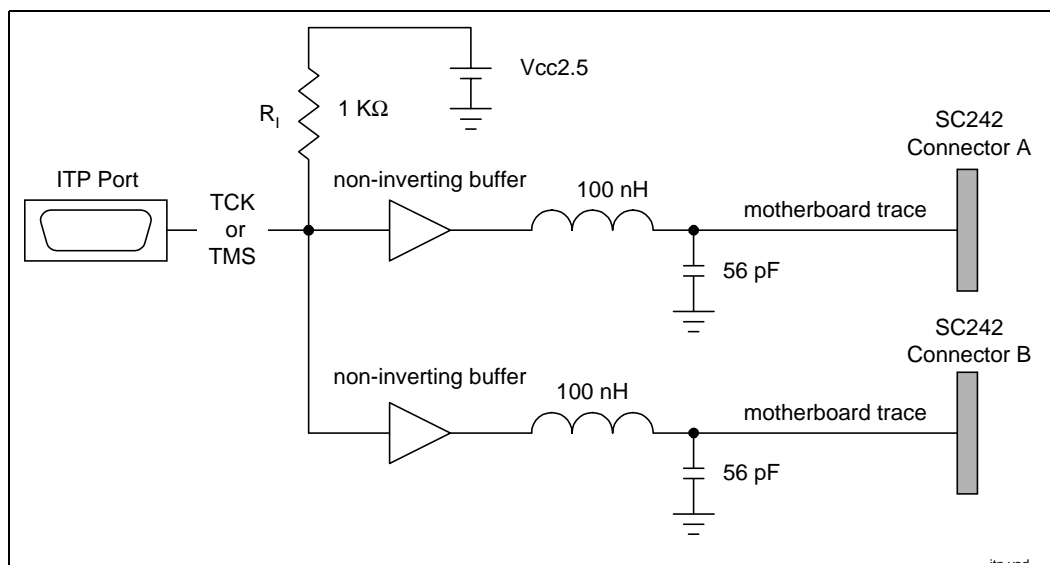
Table 2-14. Bus Request Connection Scheme for DP Intel® 820 Chipset Designs

Bus Signal	Agent 0 Pins	Agent 1 Pins
BREQ0#	BR0#	BR1#
BREQ1#	BR1#	BR0#

2.12   Additional Host Bus Guidelines

BREQ Pins

UP Systems: For uni-processor systems, the BREQ0 pin should be pulled down to ground through a 10 Ω resistor. The BREQ1 pin should be left as a no-connect.

Figure 2-42. Single Processor BREQ Strapping Requirements
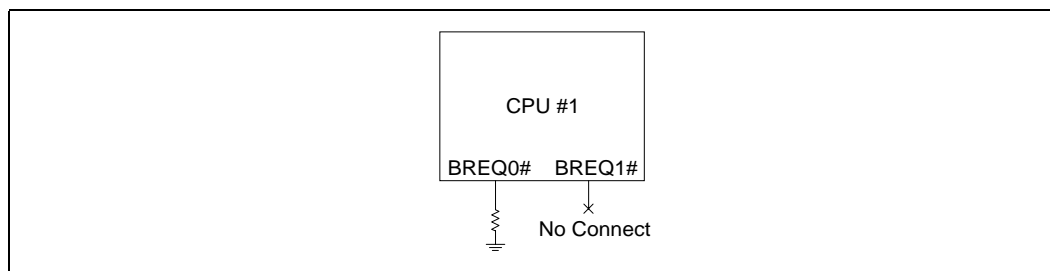
DP Systems: For dual processor systems, BREQ0# (to one of the processors) needs to be driven for *arbitration ID* strapping. Refer to Figure 2-43 for an example of the BREQ connections in a DP system. It is a requirement that the on-board logic tri-state BREQ0# after the arbitration ID strapping is complete. Additionally, BREQ0# and BREQ1# are *high-speed AGTL+* signals and the loading characteristics of the on-board logic must be considered even when the logic is tri-stated.

Figure 2-43. Dual-Processor BREQ Strapping Requirements
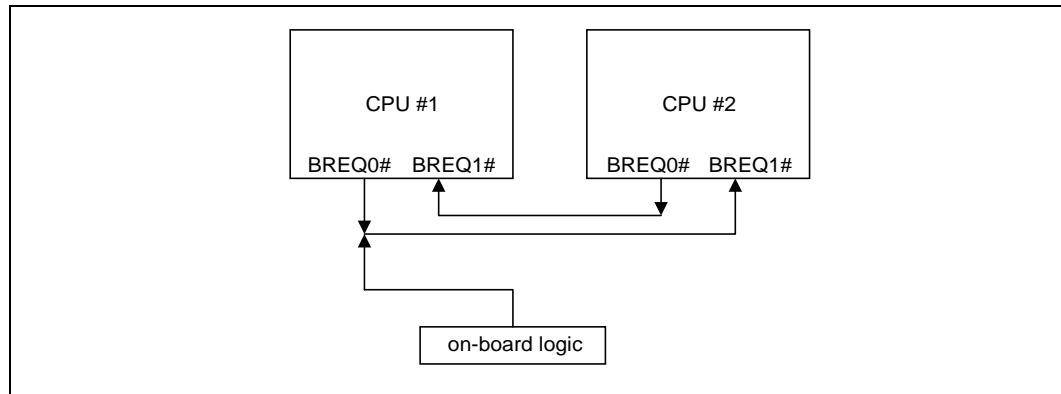
Figure 2-44. BREQ0# Circuitry for DP Systems
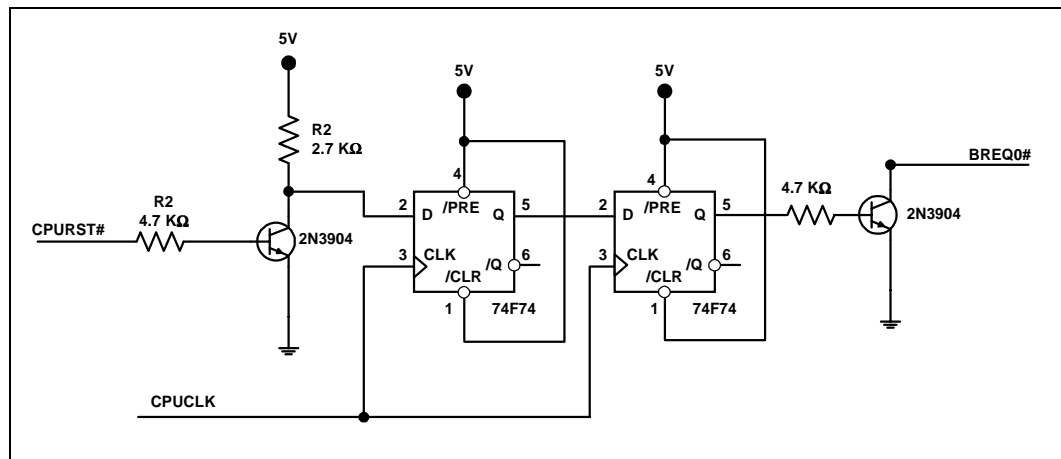
This circuit holds BREQ0 low for two clocks after the deassertion of reset. The 2N3904 connected to BREQ0 should be connected to the BREQ0 AGTL trace with a very short stub. Additionally, the series current limiting resistor on CPURESET should be attached to the CPURESET trace with a very short stub.

External Circuit Recommendation for HA7 Strapping for IOQ Depth of 1

For debug purpose, the external logic to set the IOQ depth of 1 on the front side bus may be needed. Do not add this circuit for production since overall system performance will be degraded. The external logic for HA7# strapping is very similar to the BREQ0 strapping that is described in the previous section.

The timing requirement of HA7# strapping is also similar to BREQ0 strapping for the hold time after the deassertion of RESET# (RSTIN# signal from MCH). The value of the strapping needs to be held for a minimum of 2 host clocks after the deassertion of RSTIN#. Refer to the latest version of the processor datasheets for complete description on the timing requirement.

The recommendation for the layout and the schematic example are shown below. Layout guidelines are:

- Place the transistor and stub as close as possible to MCH (or place the transistor pad on top of trace)

- The max stub for transistor is less than 0.25"

- The recommended loading of transistor is less than 5 pf.

- For dual processor design, the stub is recommended to place on the stub of the MCH and as close as possible to the MCH, and is less than 0.25"

Note: This circuit is only recommended for the debug situation that requires to set the IOQ depth equal to 1. For the production, do not add this circuit, since the overall system performance will be degraded. Also, Intel does not guarantee the above layout recommendation will work under the worst case condition.

Figure 2-45. HA7# Strapping Option Example Circuit (For Debug Purposes Only)
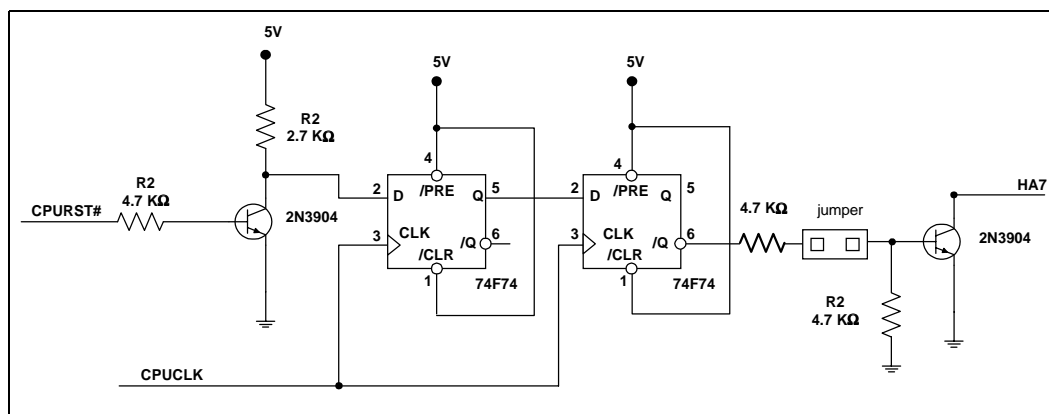
In-Target Probe (ITP)

It is important that all of the processor electrical characteristic requirements are met. It is recommended that prototype boards implement the ITP connector.

Logic Analyzer Interface (LAI)

Note that 1 KΩ resistors that are used to pull-up several processor signals in the schematics in Appendix A, "Reference Design Schematics: Uni-Processor" and Appendix B, "Reference Design Schematics: Dual-Processor" (e.g., HINIT#, IGNNE#, SMI#, etc.) preclude use of the Intel Pentium III processor LAI. The Intel Pentium III processor LAI will function correctly with these 1 KΩ pull-up resistors.

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Minimizing Crosstalk on the AGTL+ Interface

The following general rules will minimize the impact of crosstalk in the high speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 0.010" between traces wherever possible. It may be necessary to use tighter spacings when routing between component pins.

- Avoid parallelism between signals on adjacent layers.

- Since AGTL+ is a low signal swing technology, it is important to isolate AGTL+ signals from other signals by at least 0.025". This will avoid coupling from signals that have larger voltage swings, such as 5V PCI.

- Select a board stack-up that minimizes the coupling between adjacent signals.

- Route AGTL+ address, data and control signals in separate groups to minimize crosstalk between groups. The Pentium III processor uses a split transaction bus. In a given clock cycle, the address lines and corresponding control lines could be driven by a different agent than the data lines and their corresponding control lines.

Additional Considerations

- Distribute V_{TT} with a wide trace. A 0.050" minimum trace is recommended to minimize DC losses. Route the V_{TT} trace to all components on the host bus. Be sure to include decoupling capacitors. Guidelines for V_{TT} distribution and decoupling are contained in "Slot 1 Processor Power Distribution Guidelines."

- Place resistor divider pairs for V_{REF} generation at the MCH component. No V_{REF} generation is needed at the processor(s). V_{REF} is generated locally on the processor. Be sure to include decoupling capacitors. Guidelines for V_{REF} distribution and decoupling are contained in "Slot 1 Processor Power Distribution Guidelines."

- Special Case AGTL+ signals for simulation: There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require extra attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two agents on the same clock edge, the two falling wave fronts will meet at some point on the bus. This can create a large undershoot, followed by ringback which may violate the ringback specifications. This "wired-OR" situation should be simulated for the following signals: AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

2.13   Ultra ATA/66

This section contains guidelines for connecting and routing the ICH IDE interface. The ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH has integrated the 33 Ω series resistors that have been typically required on the IDE data signals running to the two ATA connectors.

The IDE interface can be routed with 5 mil traces on 5 mil spaces, and must be less than 8 inches long (from ICH to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5" shorter than the longest IDE signal (on that channel).

Cable

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.

- **Capacitance:** Less than 30 pF.

- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6" away from the end of the cable).

- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

- **ICH Placement:** The ICH must be placed equal to or less than 8 inches from the ATA connector(s).

- **PC99 requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft* PC99. CSEL signal needs to be pulled down at the host side by using a 470 Ω pull-down resistor for each ATA connector.

2.13.1   Ultra ATA/66 Detection

The Intel® 820 chipset supports many Ultra DMA modes including ATA/66. The Intel® 820 chipset needs to determine the installed IDE device mode and the type of cable to configure its own hardware and software to support it.

A new IDE cable is required for Ultra ATA/66. This cable is an 80 conductor cable; however the 40 pin connectors do not change. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground… All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

To determine if ATA/66 mode can be enabled, the Intel® 820 chipset requires the system BIOS to attempt to determine the cable type used in the system. The BIOS does this in one of two ways:

- Host Side Detection

- Device Side Detection

If the BIOS detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the Intel® 820 chipset and the IDE device. Otherwise, the BIOS can only enable modes that do not require an 80-conductor cable (e.g., Ultra ATA/33 Mode).

After determining the Ultra DMA mode to be used, the BIOS will configure the Intel® 820 chipset hardware and software to match the selected mode.

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2.13.2   Ultra ATA/66 Cable Detection

The Intel® 820 chipset can use two methods to detect the cable type. Each mode requires a different motherboard layout.

Host-Side Detection (BIOS Detects Cable Type Using GPIOs)

Host side detection requires the use of two GPI pins (1 per IDE controller). The proper way to connect the PDIAG/CBLID signal of the IDE connector to the host is shown in Figure 2-46. All IDE devices have a 10 KΩ pull-up resistor to 5 volts. The GPI and GPIO pins on the ICH and GPI pins on the FWH Flash BIOS are not 5 volt tolerant. This requires a resistor divider so that 5 volts will not be driven to the ICH or FWH Flash BIOS pins. The proper value of the series resistor is 15 KΩ (as shown in Figure 2-46). This creates a 10 KΩ / 15 KΩ resistor divider and produces approximately 3 volts for a logic high.

This mechanism allows the host, after diagnostics, to sample PDIAG/CBLID. If PDIAG/CBLIB is high then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG/CBLID is low then there is an 80-conductor cable in the system.

Figure 2-46. Host-Side IDE Cable Detection

Device-Side Detection (BIOS Queries IDE Drive for Cable Type)

Device side detection requires only a 0.047 uF capacitor on the motherboard as shown in Figure 2-47. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 drive will drive PDIAG/CBLID low and then release it (pulled up through a 10 KΩ resistor) The drive will sample the PDIAG signal after releasing it. In an 80-conductor cable, PDIAG/CBLID is not connected through and, therefore, the capacitor has no effect. In a 40-conductor cable, PDIAG/CBLID is connected though to the drive. Therefore, the signal rises more slowly. The drive can detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

Figure 2-47. Drive-Side IDE Cable Detection
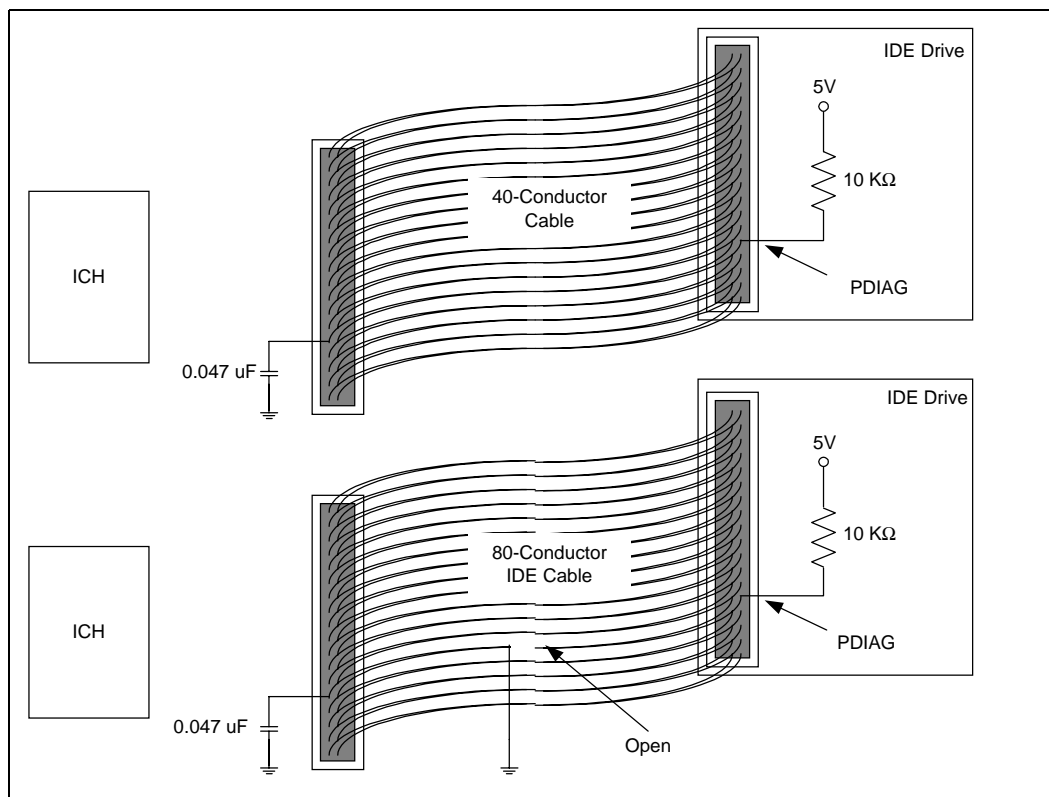
Layout for BOTH Host-Side and Drive-Side Cable Detection

It is possible to layout for both Host-Side and Drive-Side cable detection and decide the method to be used during assembly. Figure 2-48 shows the layout that allows for both host-side and drive-side detection.

- For Host-Side Detection:

  — R1 is a 0 Ω resistor
  — R2 is a 15 KΩ resistor
  — C1 is not stuffed

- For Drive-Side Detection:

  — R1 is not stuffed
  — R2 is not stuffed
  — C1 is a 0.047 uF capacitor

Figure 2-48. Layout for Host- or Drive-Side IDE Cable Detection
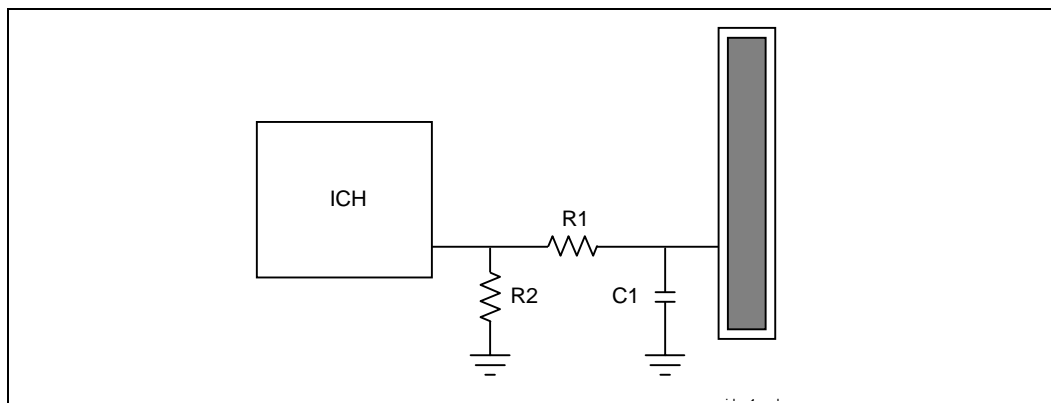
Figure 2-49. Ultra ATA/66 Cable

Black wires are ground
Grey wires are signals
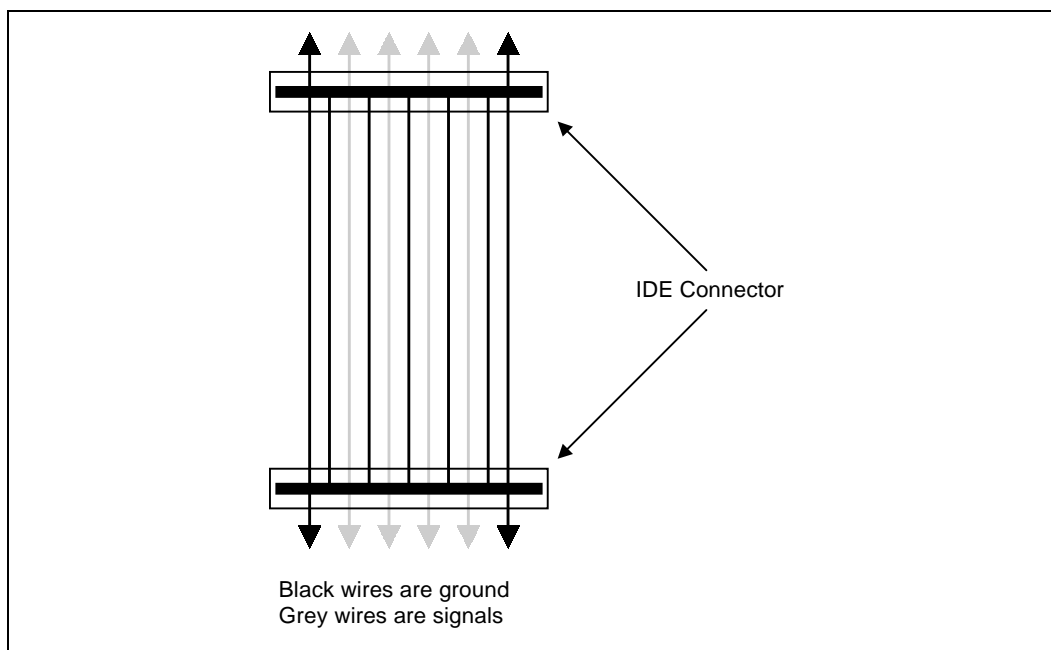
2.13.3   Ultra ATA/66 Pullup/Pulldown Requirements

- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.

- An 8.2 KΩ to 10 KΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC5.

- A 10 KΩ pull-down resistor is required on PDD7 and SDD7 (as required by the ATA-4 specification).

- A 5.6 KΩ pull-down resistor is required on PDDREQ# and SDDREQ# (as required by the ATA-4 specification).

- A 1K Ω pull-up resistor is required on PIORDY and SIORDY (as required by the ATA-4 specification).

Figure 2-50. Resistor Requirements for Primary IDE Connector

*Due to ringing, PCIRST# must be buffered.
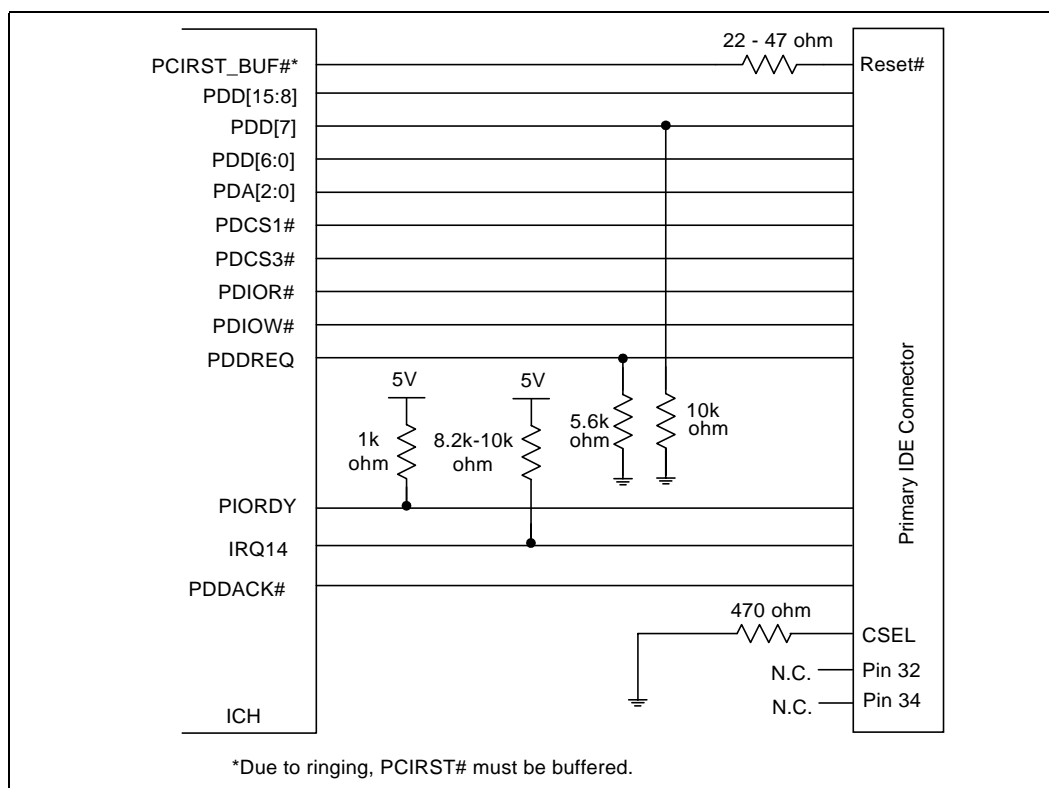
Figure 2-51. Resistor Requirements for Secondary IDE Connector
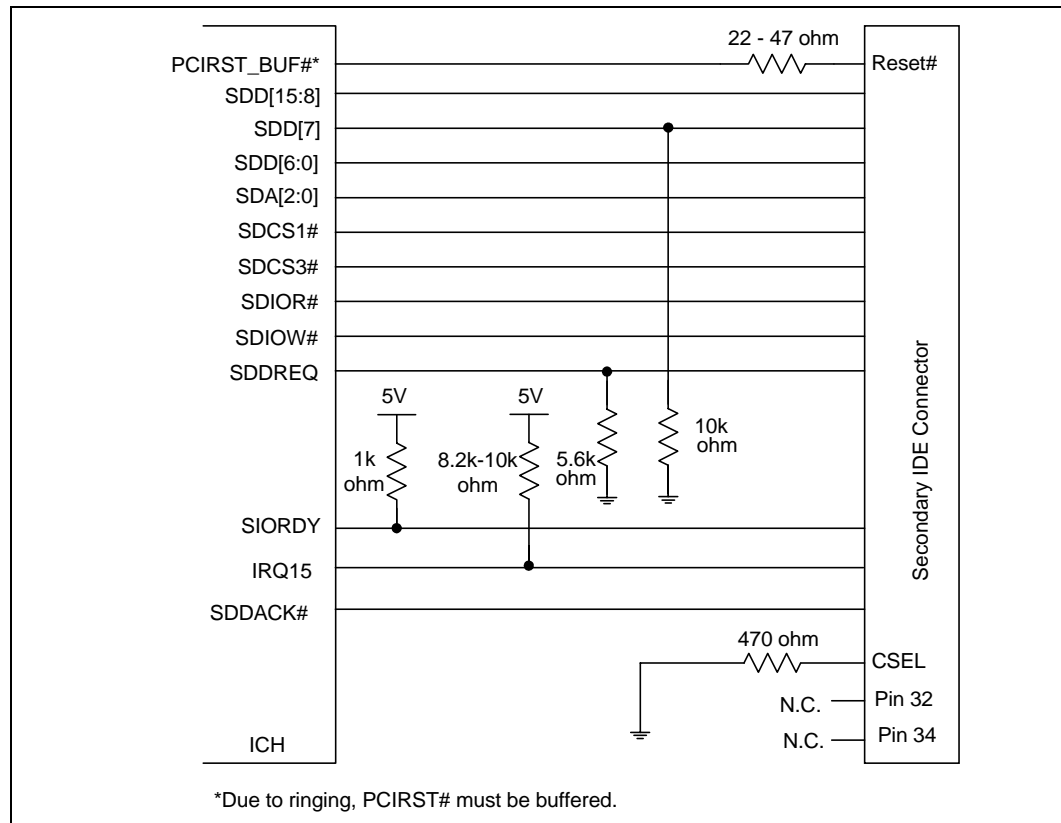
2.14   AC'97

The ICH implements an AC'97 2.1 compliant digital controller. Any codec attached to the ICH AC-link must be AC'97 2.1 compliant as well. Contact your codec IHV for information on 2.1 compliant products. The AC'97 2.1 specification is on the Intel website. The ICH supports the following combinations of codecs:

Table 2-15. ICH Codec Options

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in the table, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

Intel has developed a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM plug-in card options.

The AMR specification provides a mechanism for AC'97 codecs to be on a riser card. This is important for modem codecs as it helps ease international certification of the modem.

For increased part placement flexibility, there are two routing methods for the AC'97 interface: the *tee* topology and the *daisy-chain* topology. The AC'97 interface can be routed using 5 mil traces with 5 mil space between the traces.

Figure 2-52. Tee Topology AC'97 Trace Length Requirements
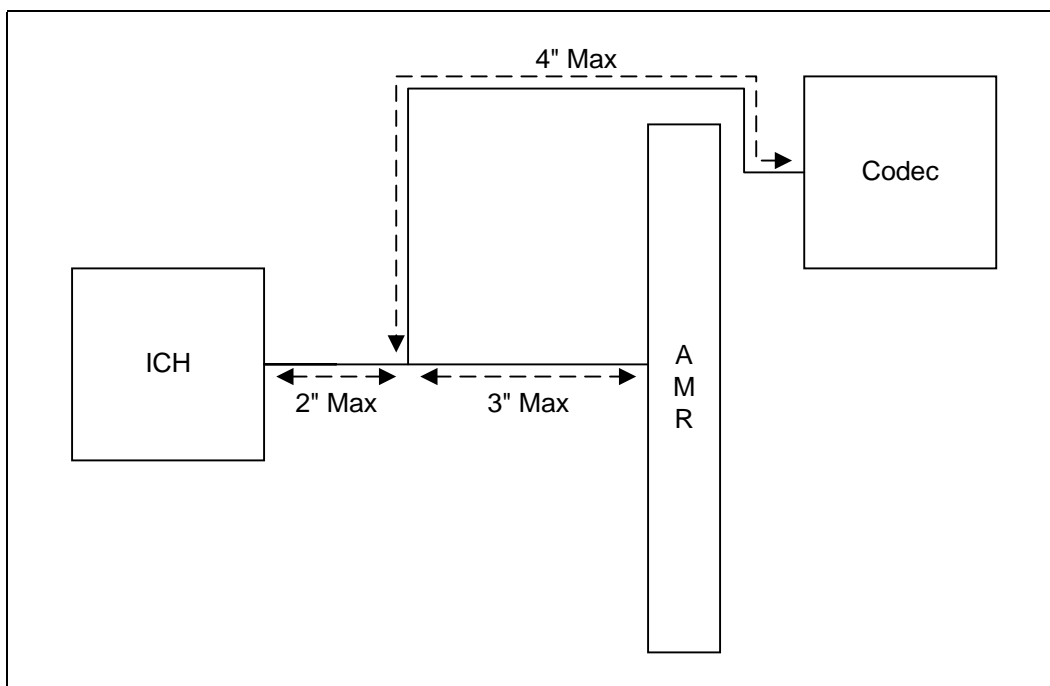
Figure 2-53. Daisy-Chain Topology AC'97 Trace Length Requirements

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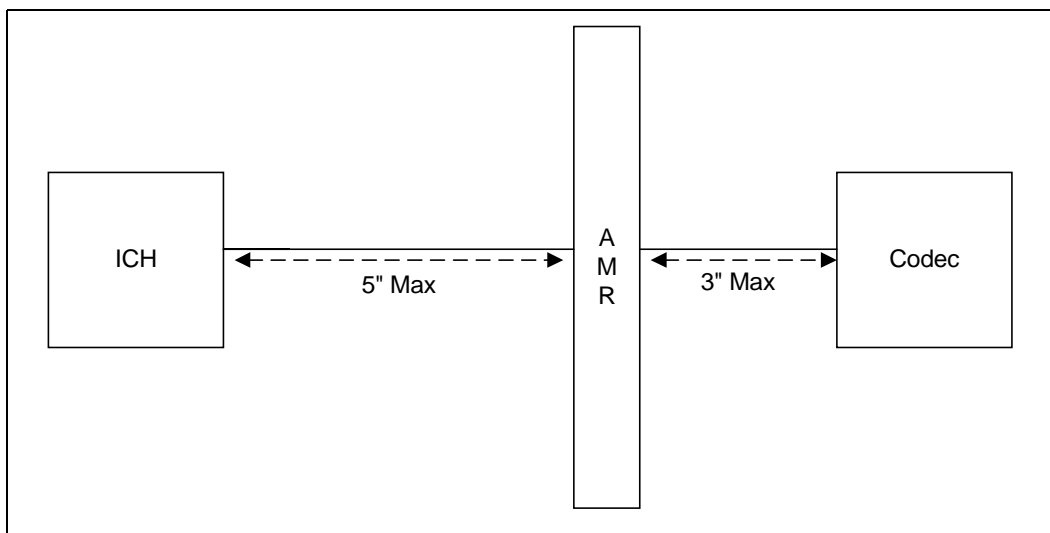
Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH), and any other codec present. That clock is used as the timebase for latching and driving data.

On the Intel® 820 chipset platform, the ICH supports Wake on Ring from S1, S3, and S4 via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH has weak pulldowns/pullups that are only enabled when the AC-Link Shut Off bit in the ICH is set. This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec. If there is an onboard codec only (i.e., no AMR), then the unused SDIN pin should have a weak (10 KΩ) pulldown to keep it from floating. If an AMR is used, any SDIN signal that could be no connected (e.g., with no codec, both can be NC), then both SDIN pins must have a 10 KΩ pulldown.

Table 2-16. AC'97 SDIN Pulldown Resistors

System Solution	Pullup Requirements
On-board Codec Only	Pulldown the SDIN pin that is NOT connected to the codec
AMR Only	Pulldown BOTH SDIN pins
BOTH AMR and On-board Codec	Pulldown any SDIN pin that could be NC*

NOTE: If the on-board codec can be disabled, both SDIN pins must have pulldowns. If the on-board codec can not be disabled, only the SDIN not connected to the on-board codec requires a pulldown.

2.14.1 AC'97 Signal Quality Requirements

In a lightly loaded system (e.g., single codec down), AC'97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented in order to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 50pF.

2.14.2 AC'97 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH0/ICH platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. These recommendations do not represent the only implementation or a complete checklist, but provides recommendations based on the ICH0/ICH platform.

- Codec Implementation
  - The motherboard can implement any valid combination of codecs on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on the AMR module; however, nothing precludes a modem codec on the motherboard.
  - Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH0/ICH platform.
  - If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground.
  - The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
  - Components (e.g., FET switches), buffers, or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so will potentially interfere with timing margins and signal integrity.
  - If the motherboard requires that an AMR module override a primary codec down, a means of preventing contention on the AC-link must be provided for the onboard codec.
  - The ICH0/ICH supports Wake on Ring* from S1-S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pulldowns will prevent the inputs from floating, therefore external resistors are not required. The ICH0/ICH does not wake from the S5 state via the AC'97 link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10 KΩ) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH0/ICH's internal pull-down resistors are enabled, and thus there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that has the potential of not being connected to a codec*. For example, if a dedicated audio codec is on the motherboard, and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. If however, the SDATAIN signal has no codec connected, or is connected to an AMR slot, or is connected to an onboard codec that can be hardware disabled, then the signal should have an external pull-down resistor to ground.
- AMR Slot Special Connections
  - AUDIO_MUTE#: No connect on the motherboard.
  - AUDIO_PWRDN: No connect on the motherboard. Codecs on the AMR card should implement a powerdown pin, per the AC'97 2.1 specification, to control the amplifier.
  - MONO_PHONE: Connect top onboard audio codec if supported.
  - MONO_OUT/PC_BEEP: Connect to SPKR output from the ICH0/ICH, or MONO_OUT from onboard codec.
  - PRIMARY_DN#: See discussion above.
  - +5VDUAL/+5VSB: Connect to VCC5 core on the motherboard, unless adequate power supply is available. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
  - S/P-DIF_IN: Connect to ground on the motherboard.
  - AC_SDATAIN[3:2]: No connect on the motherboard. The ICH0/ICH supports a maximum of two codecs, which should be attached to SDATAIN[1:0].
  - AC97_MSTRCLK: Connect to ground on the motherboard.
- The ICH0/ICH provides internal weak pulldowns. Therefore, the motherboard does not need to provide discrete pulldown resistors.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

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2.15   USB

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 KΩ pulldown resistors on both P+/P- data lines.

- 15 Ω series resistors should be placed as close as possible to the ICH (<1 inch). These series resistors are required for source termination of the reflected signal.

- 47 pF caps must be placed as close to the ICH as possible and on the ICH side of the series resistors on the USB data lines (P0+/-, P1+/-). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.

- 15 KΩ ±5% pulldown resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/-, P1+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.

- The trace impedance for the P0+/-, P1+/- signals should be 45 Ω (to ground) for each USB signal P+ or P-. Using the stackup recommended in section Section 5.3, "Stackup Requirement" on page 5-1. USB requires 9 mils traces. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.

- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI.

Figure 2-54 illustrates the recommended USB schematic.

Figure 2-54. USB Data Signals
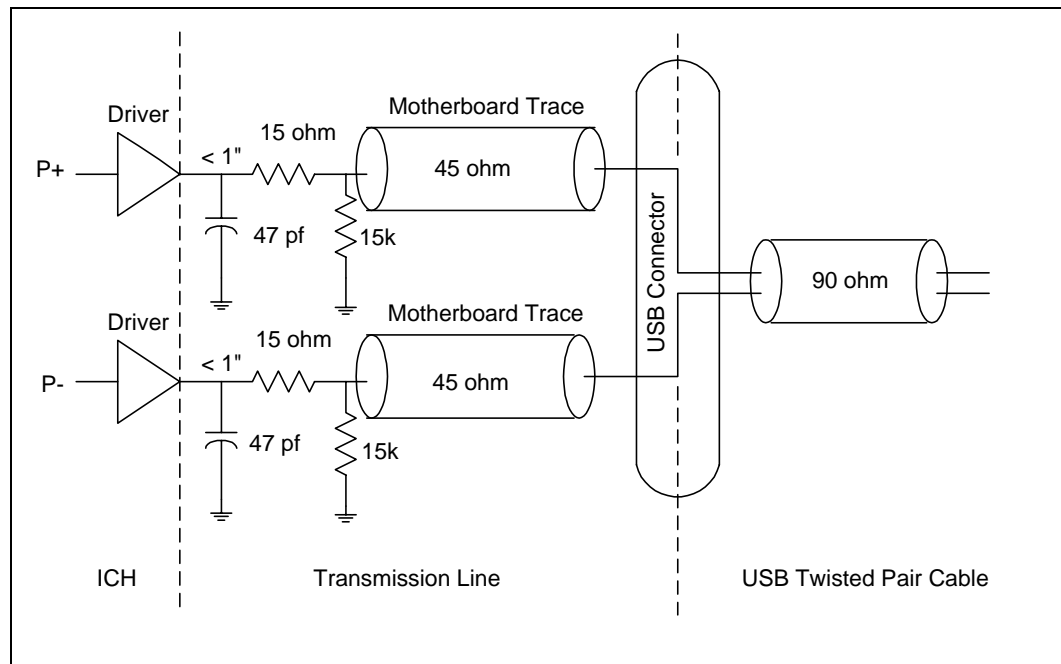
Recommended USB trace characteristics

- Impedance 'Z$_0$' = 45.4 Ω

- Line Delay = 160.2 ps

- Capacitance = 3.5 pF

- Inductance = 7.3 nH

- Res @ 20° C = 53.9 mOhm

2.16 ISA (82380AB)

2.16.1 ICH GPIO connected to 82380AB

At reset, the ICH LPC Bridge defaults to subtractive decode. Since the LPC bridge logically sits on PCI there will be two subtractive decode bridges in systems with the 82380AB (which is also a subtractive decode device). A GPO that defaults high (i.e., ICH GPO 21) must be connected to the NOGO signal on the 82380AB. Asserting NOGO prevents the 82380AB from subtractively decoding cycles on the PCI bus. The BIOS must configure the 82380AB, program the ICH to positively decode LPC cycles, and release the NOGO signal to the 82380AB.

2.16.2 Sub Class Code

Both the LPC Bridge and the 82380AB have the same Sub Class code indicating an ISA bridge. This can not be handled by the OS's PCI PnP code. The ICH provides the ability to hide IDSEL to the 82380AB. ICH A22 must be connected to the 82380AB IDSEL signal. After the BIOS configures the 82380AB, it will set a bit in the ICH that hides the 82380AB from the OS by not asserting the IDSEL (A22) to the 82380AB during OS enumeration.

2.17 IOAPIC Design Recommendation

UP systems not using the IOAPIC should follow these recommendations:

- On the ICH
    - Connect PICCLK directly to ground
    - Connect PICD0, PICD1 to ground through a 10 KΩ resistor
- On the CPU
    - PICCLK must be connected from the clock generator to the PICCLK pin on the processor
    - Connect PICD0 to 2.5V through 10 KΩ resistors
    - Connect PICD1 to 2.5V through 10 KΩ resistors

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2.18 SMBus/Alert Bus

The **Alert on LAN*** signals can be used as:

- **Alert on LAN* signals:** 4.7 KΩ pullup resistors to 3.3VSB are required.

- **GPIOs:** Pullup resistors to 3.3VSB and the signals must be allowed to change states on powerup (e.g., on power-up, the ICH drives *heartbeat* messages until the BIOS programs these signals as GPIOs). The value of the pullup resistors depends on the loading on the GPIO signal.

- **Not Used:** 4.7 KΩ pullup resistors to 3.3VSB are required.

If the SMBus is used only for the three SPD EEPROMs (one on each RIMM), both signals should be pulled up with a 4.7 KΩ resistor to 3.3V.

2.19 PCI

The ICH provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH supports six PCI Bus masters (excluding the ICH), by providing six REQ#/GNT# pairs. In addition, the ICH supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 2-55. PCI Bus Layout Example
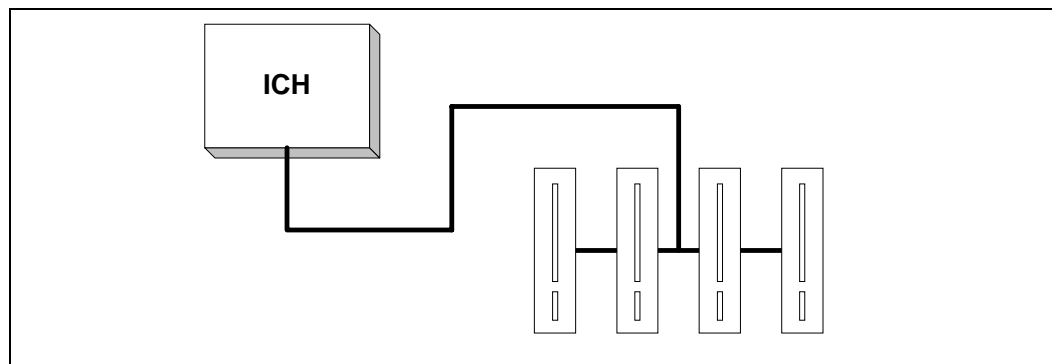
2.20 RTC

The ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time, and storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH. **This circuit is not the same as the circuit used for the PIIX4.**

2.20.1   RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 pins. Figure 2-56 documents the external circuitry that comprises the oscillator of the ICH RTC.

Figure 2-56. External Circuitry for the ICH RTC[2]
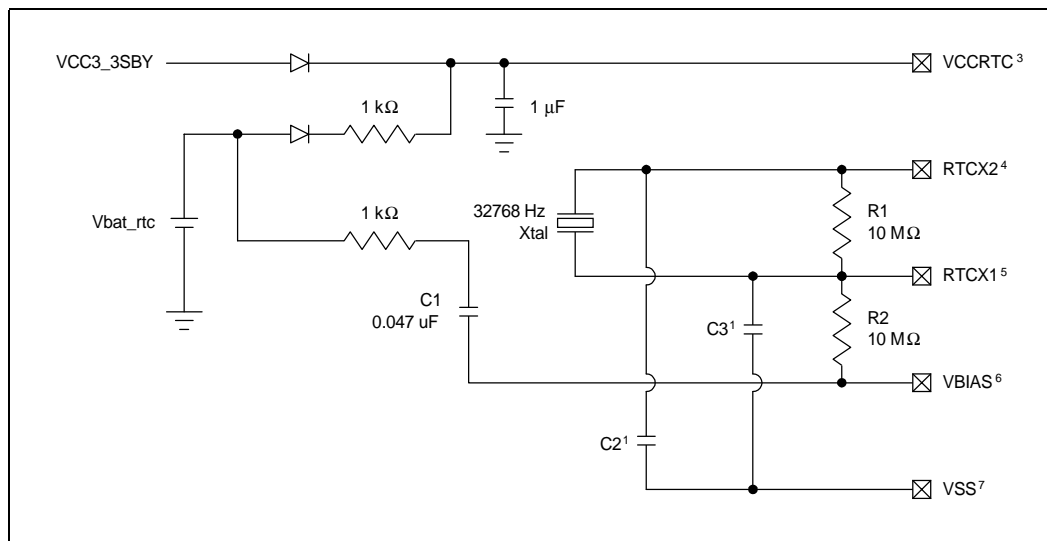
NOTES:
1. The exact capacitor value needs to based on what the crystal maker recommends.
2. This circuit is not the same as the one used for PIIX4.
3. VCC_{RTC}: Power for RTC Well
4. RTCX2: Crystal Input 2 – Connected to the 32.768 KHz crystal.
5. RTCX1: Crystal Input 1 – Connected to the 32.768 KHz crystal.
6. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
7. VSS: Ground

2.20.2   External Capacitors

To maintain the RTC accuracy, the external capacitor C1 needs to be 0.047 uF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

Equation 2-4 can be used to choose the external capacitance values (C2 and C3):

Equation 2-4. External Capacitance Calculation

$$Cload = (C2 * C3)/(C2+C3) + Cparasitic$$

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

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2.20.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible; around ¼ inch is sufficient.

- Minimize the capacitance between Xin and Xout in the routing.

- Put a ground plane under the XTAL components.

- Do not route switching signals under the external components (unless on the other side of the board).

- The oscillator VCC should be clean; use a filter, such as an RC lowpass, or a ferrite inductor.

2.20.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system.

Example batteries are Duracell 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 uA, the battery life will be at least:

170,000 uAh / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to the ICH via an isolation schottky diode circuit. The schottky diode circuit allows the ICH RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 2-57 is an example of a diode circuitry that is used.

Figure 2-57. Diode Circuit Connecting RTC External Battery
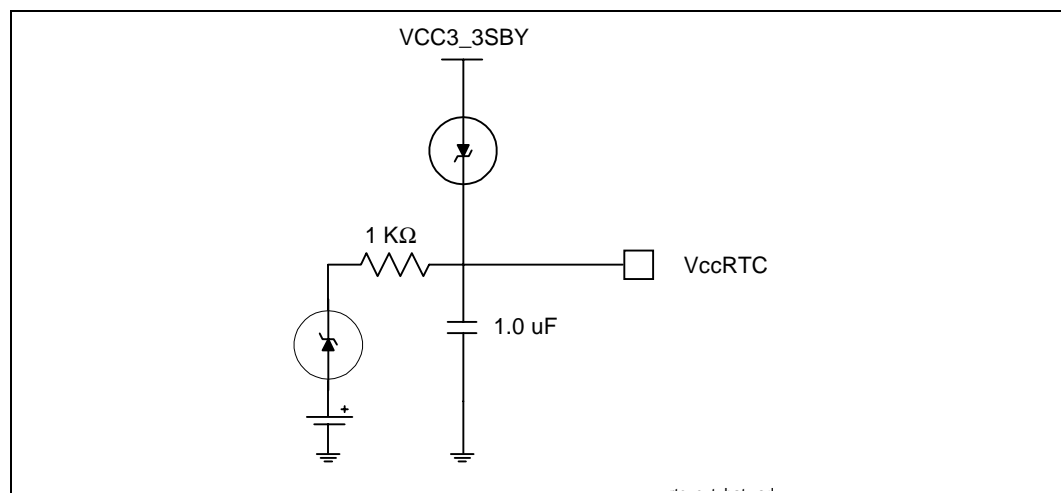
A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby increase the RTC accuracy.

2.20.5   RTC External RTCRST Circuit

The ICH RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10-20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

Figure 2-58. RTCRST External Circuit for the ICH RTC
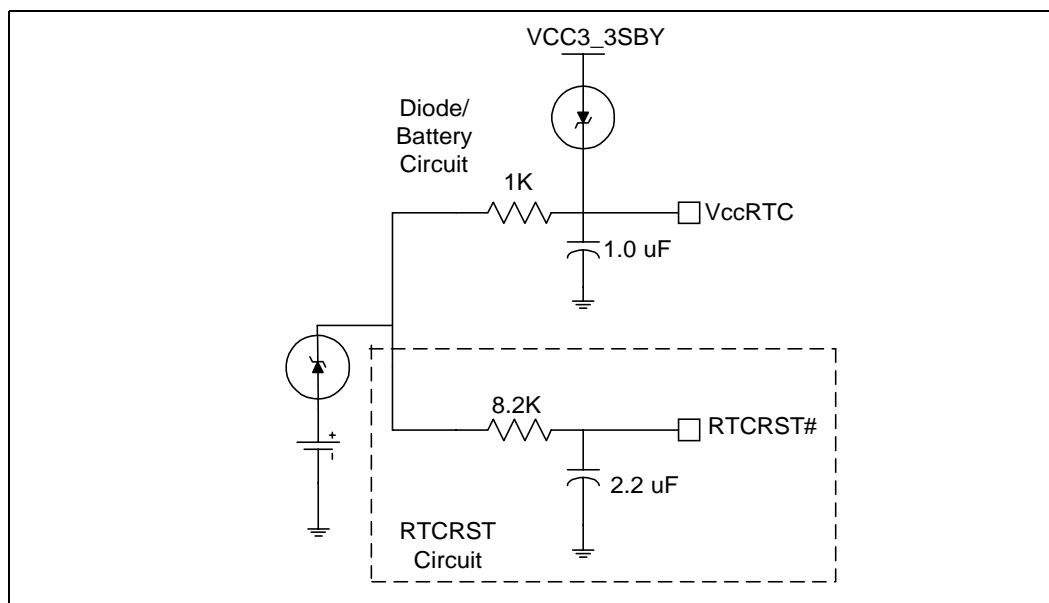
This RTCRST# circuit is combined with the diode circuit (Figure 2-57) which allows the RTC well to be powered by the battery when the system power is not available. Figure 2-56 is an example of this circuitry that is used in conjuction with the external diode circuit.

2.20.6   RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1", the shorter the better

- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them)

- Put a ground plane under all of the external RTC circuitry

- Do not route any switching signals under the external components (unless on the other side of the ground plane)

2.20.7   VBIAS DC Voltage and Noise Measurements

- Steady state VBIAS will be a DC voltage of about 0.38V ±0.06V.

- VBIAS will be "kicked" when the battery is inserted to about 0.7–1.0V, but it will come back to its DC value within a few ms.

- Noise on VBIAS must be kept to a minimum, 200 mV or less.

- VBIAS is very sensitive and cannot be directly probed; it can be probed through a 0.01 uF capacitor.

- Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely.

- To minimize noise of VBIAS, it is necessary to implement the routing guidelines described above and the required external RTC circuitry.

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3

Advanced System Bus Design

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Advanced System Bus Design 3

Section 2.9, "System Bus Design" on page 2-46 describes the recommendations for designing Intel® 820 chipset based platforms. This chapter discusses more detail about the methodology used to develop the guidelines. Section 3.2, "AGTL+ Design Guidelines" on page 3-4 discusses specific system guidelines. This is a step-by-step methodology that Intel has successfully used to design high performance desktop systems. Section 3.3, "Theory" on page 3-15 introduces the theories that are applicable to this layout guideline. Section 3.4, "More Details and Insight" on page 3-19 contains more details and insights. The items in Section 3.4 expand on some of the rationale for the recommendations in the step-by-step methodology. This section also includes equations that may be used for reference.

3.1 Terminology and Definitions

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to "assist" the pull-up resistors during the first clock of a low-to-high voltage transition. Additionally, the processor Single Edge Connector (S.E.C.) cartridge contains 56 Ω pull-up resistors to provide termination at each bus load.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. The results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the "slow" corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the "fast" corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.

Term	Definition
Cross-talk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.

- Backward Cross-talk - coupling which creates a signal in a victim network that travels in the opposite direction as the aggressor's signal.

- Forward Cross-talk - coupling which creates a signal in a victim network that travels in the same direction as the aggressor's signal.

- Even Mode Cross-talk - coupling from multiple aggressors when all the aggressors switch in the same direction that the victim is switching.

- Odd Mode Cross-talk - coupling from multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Edge Finger	The cartridge electrical contact that interfaces to the SC242 connector.
Flight Time	Flight Time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver.

More precisely, *flight time* is defined to be:

- The time difference between a signal at the input pin of a receiving agent crossing V_{REF} (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.), and the output pin of the driving agent crossing V_{REF} if the driver was driving the Test Load used to specify the driver's AC timings.

    See Section for details regarding flight time simulation and validation.

    The V_{REF} Guardband takes into account sources of noise that may affect the way an AGTL+ signal becomes valid at the receiver. See the definition of the V_{REF} Guardband.

- **Maximum and Minimum Flight Time** - Flight time variations can be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, cross-talk, V_{TT} noise, V_{REF} noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of *Simultaneous Switching Output (SSO)* and packaging effects.

- The **Maximum Flight Time** is the largest flight time a network will experience under all variations of conditions. Maximum flight time is measured at the appropriate V_{REF} Guardband boundary.

- The **Minimum Flight Time** is the smallest flight time a network will experience under all variations of conditions. Minimum flight time is measured at the appropriate V_{REF} Guardband boundary.

For more information on flight time and the V_{REF} Guardband, see the *Pentium® II Processor Developer's Manual.*

GTL+	GTL+ is the bus technology used by the Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See thePentium® II *Processor Developer's Manual* for more details of GTL+.

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Term	Definition
Network	The trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors.
Overdrive Region	Is the voltage range, at a receiver, located above and below V_{REF} for signal integrity analysis. See the *Intel® Pentium® II Processor Developer's Manual* for more details.
Overshoot	Maximum voltage allowed for a signal at the processor core pad. See each processor's datasheet for overshoot specification.
Pad	A feature of a semiconductor die contained within an internal logic package on the S.E.C cartridge substrate used to connect the die to the package bond wires. A pad is only observable in simulation.
Pin	A feature of a logic package contained within the S.E.C. cartridge used to connect the package to an internal substrate trace.
Ringback	Ringback is the voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, etc. See the respective processor's datasheet for ringback specification.
Settling Limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective processor's datasheet for settling limit specification.
Setup Window	Is the time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO) Effects	Refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "pushout"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, terminating at agent pads.
Undershoot	Maximum voltage allowed for a signal to extend below V_{ss} at the processor core pad. See the respective processor's datasheet for undershoot specifications.
Victim	A network that receives a coupled cross-talk signal from another network is called the victim network.
V_{REF} Guardband	A guardband (ΔV_{REF}) defined above and below V_{REF} to provide a more realistic model accounting for noise such as cross-talk, V_{TT} noise, and V_{REF} noise.

3.2 AGTL+ Design Guidelines

The following step-by-step guideline was developed for systems based on two processor loads and one Intel 82820 MCH load. Systems using custom chipsets will require timing analysis and analog simulations specific to those components.

The guideline recommended in this section is based on experience developed at Intel while developing many different Intel Pentium® Pro processor family and Intel Pentium lll processor-based systems. Begin with an initial timing analysis and topology definition. Perform pre-layout analog simulations for a detailed picture of a working "solution space" for the design. These pre-layout simulations help define routing rules prior to placement and routing. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

Guideline Methodology:

- Initial Timing Analysis
- Determine General Topology, Layout, and Routing
- Pre-Layout Simulation
  — Sensitivity sweep
  — Monte Carlo Analysis
- Place and Route Board
  — Estimate Component to Component Spacing for AGTL+ Signals
  — Layout and Route Board
- Post-Layout Simulation
  — Interconnect Extraction
  — Inter-Symbol Interference (ISI), Cross-talk, and Monte Carlo Analysis
- Validation
  — Measurements
  — Determining Flight Time

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3.2.1 Initial Timing Analysis

Perform an initial timing analysis of the system using Equation 3-1 and Equation 3-2 shown below. These equations are the basis for timing analysis. To complete the initial timing analysis, values for clock skew and clock jitter are needed, along with the component specifications. These equations contain a multi-bit adjustment factor, M_{ADJ}, to account for multi-bit switching effects such as SSO pushout or pull-in that are often hard to simulate. These equations **do not** take into consideration all signal integrity factors that affect timing. Additional timing margin should be budgeted to allow for these sources of noise.

Equation 3-1. Setup Time

$$T_{CO\_MAX} + T_{SU\_MIN} + CLK_{SKEW} + CLK_{JITTER} + T_{FLT\_MAX} + M_{ADJ} \leq \text{Clock Period}$$

Equation 3-2. Hold Time

$$T_{CO\_MIN} + T_{FLT\_MIN} - M_{ADJ} \geq T_{HOLD} + CLK_{SKEW}$$

Symbols used in Equation 3-1 and Equation 3-2:

— T_{CO_MAX} is the maximum clock to output specification[1].

— T_{SU_MIN} is the minimum required time specified to setup before the clock[1].

— CLK_{JITTER} is the maximum clock edge-to-edge variation.

— CLK_{SKEW} is the maximum variation between components receiving the same clock edge.

— T_{FLT_MAX} is the maximum flight time as defined in Section 3.1, "Terminology and Definitions" on page 3-1.

— T_{FLT_MIN} is the minimum flight time as defined in Section 3.1, "Terminology and Definitions" on page 3-1.

— M_{ADJ} is the multi-bit adjustment factor to account for SSO pushout or pull-in.

— T_{CO_MIN} is the minimum clock to output specification[1].

— T_{HOLD} is the minimum specified input hold time.

Note: The Clock to Output (T_{CO}) and Setup to Clock (T_{SU}) timings are both measured from the signals last crossing of V_{REF}, with the requirement that the signal does not violate the ringback or edge rate limits. See the respective Processor's datasheet and the *Pentium® II/ Processor Developer's Manual* for more details.

Solving these equations for T_{FLT} results in the following equations:

Equation 3-3. Maximum Flight Time

$$T_{FLT\_MAX} \leq \text{Clock Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ}$$

Equation 3-4. Minimum Flight Time

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ}$$

There are multiple cases to consider. Note that while the same trace connects two components, component A and component B, the minimum and maximum flight time requirements for component A driving component B as well as component B driving component A must be met. The cases to be considered are:

- Processor driving processor

- Processor driving chipset

- Chipset driving processor

A designer using components other than those listed above must evaluate additional combinations of driver and receiver.

Table 3-1. AGTL+ Parameters for Example Calculations[1,2]

IC Parameters	Intel® Pentium® III processor core at 133 MHz Bus	Intel 82820 MCH	Notes
Clock to Output maximum (T_{CO_MAX})	2.7	3.6	4
Clock to Output minimum (T_{CO_MIN})	-0.1	0.5	4
Setup time (T_{SU_MIN})	1.2	2.27	3,4
Hold time (T_{HOLD})	0.8	0.28	4

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only.** These timing parameters are subject to change. Please check the appropriate component documentation for valid timing parameter values.
3. T_{SU_MIN} = 1.9 ns assumes the **82**820 MCH sees a minimum edge rate equal to 0.3 V/ns.
4. The Pentium III substrate nominal impedance is set to 65 Ω ±15%. Future Pentium III processor substrate may be set at 60 Ω ±15%

Table 3-1 lists the AGTL+ component timings of the processors and 82820 MCH defined at the pins. These timings are for reference only.

Table 3-2 gives an example AGTL+ initial maximum flight time and Table 3-3 is an example minimum flight time calculation for a 133 MHz, 2-way Pentium III processor/Intel 820 chipset system bus. Note that assumed values for clock skew and clock jitter were used. Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.

Intel highly recommends adding margin as shown in the "M_{ADJ}" column to offset the degradation caused by SSO push-out and other multi-bit switching effects. The "Recommended T_{FLT_MAX}" column contains the recommended maximum flight time after incorporating the M_{ADJ} value. If edge rate, ringback, and monotonicity requirements are not met, flight time correction must first be performed as documented in the *Pentium® II Processor Developer's Manual* with the additional requirements noted in Section 3.5, "Definitions of Flight Time Measurements/Corrections and Signal Quality" on page 3-24. The commonly used "textbook" equations used to calculate the expected signal propagation rate of a board are included in Section 3.2, "AGTL+ Design Guidelines" on page 3-4.

Simulation and control of baseboard design parameters can ensure that signal quality and maximum and minimum flight times are met. Baseboard propagation speed is highly dependent on transmission line geometry configuration (stripline vs. microstrip), dielectric constant, and loading. This layout guideline includes high-speed baseboard design practices that may improve the amount

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of timing and signal quality margin. The magnitude of M_{ADJ} is highly dependent on baseboard design implementation (stackup, decoupling, layout, routing, reference planes, etc.) and needs to be characterized and budgeted appropriately for each design.

Table 3-2 and Table 3-3 are derived assuming:

- CLK_{SKEW} = 0.2 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets the CK98 clock driver specification is being used.)

- CLK_{JITTER} = 0.250 ns

Some clock driver components may not support ganging the outputs together. Be sure to verify with your clock component vendor before ganging the outputs. See the appropriate Intel 820 chipset documentation for details on clock skew and jitter specifications. Refer to Section 2.6.2, "Direct Rambus* Layout Guidelines" on page 2-8 and Chapter 4, "Clocking" for host clock routing details.

Table 3-2. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor[4]	Processor[4]	7.50	2.7	1.20	0.20	0.250	0.40	2.75
Processor[4]	82820 MCH	7.50	2.7	2.27	0.20	0.250	0.40	1.68
82820 MCH	Processor[4]	7.50	3.63	1.20	0.20	0.25	0.40	1.82

NOTES:
1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
    - SSO push-out or pull-in.
    - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
    - Cross-talk on the PCB and internal to the package can cause variation in the signals.
   There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:
    - The effective board propagation constant (S_{EFF}), which is a function of:
        - Dielectric constant (ε_r) of the PCB material.
        - The type of trace connecting the components (stripline or microstrip).
        - The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.
4. Processor values specified in this table are examples only. Refer to the appropriate processor datasheet for specification values.

Table 3-3. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor[2]	Processor[2]	0.8	0.2	-0.1	1.2
Processor[2]	82820 MCH	0.28	0.2	-0.1	.58
82820 MCH	Processor[2]	0.8	0.2	0.5	.5

NOTES:
1. All times in nanoseconds.
2. Processor values specified in this table are examples only. Refer to the appropriate processor datasheet for specification values.

3.2.2 Determine General Topology, Layout, and Routing Desired

After calculating the timing budget, determine the approximate location of the processor and the chipset on the base board (see).

3.2.3 Pre-Layout Simulation

3.2.3.1 Methodology

Analog simulations are recommended for high speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working "solution space" that meets flight time and signal quality requirements. The layout recommendations in the previous sections are based on pre-layout simulations conducted at Intel. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the **device pads** for signal quality and at the **device pins** for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

3.2.3.2 Sensitivity Analysis

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package, Z_0, and S_0 are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to minimum flight time, maximum flight time, and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

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3.2.3.3   Monte Carlo Analysis

Perform a Monte Carlo analysis to refine the passing solution space region. A Monte Carlo analysis involves randomly varying parameters (independent of one another) over their tolerance range. This analysis intends to ensure that no regions of failing flight time and signal quality exists between the extreme corner cases run in pre-layout simulations. For the example topology, vary the following parameters during Monte Carlo simulations:

- Lengths L1 through L3
- Termination resistance R_{TT} on the processor cartridge #1
- Termination resistance R_{TT} on the processor cartridge #2
- Z_0 of traces on processor cartridge #1
- Z_0 of traces on processor cartridge #2
- S_0 of traces on processor cartridge #1
- S_0 of traces on processor cartridge #2
- Z_0 of traces on baseboard
- S_0 of traces on baseboard
- Fast and slow corner processor I/O buffer models for cartridge #1
- Fast and slow corner processor I/O buffer models for cartridge #2
- Fast and slow package models for processor cartridge #1
- Fast and slow package models for processor cartridge #2
- Fast and slow corner 82820 MCH I/O buffer models
- Fast and slow 82820 MCH package models

3.2.3.4   Simulation Criteria

Accurate simulations require that the actual range of parameters be used in the simulations. Intel has consistently measured the cross-sectional resistivity of the PCB copper to be approximately 1 Ω*mil^2/inch, not the 0.662 Ω*mil^2/inch value for annealed copper that is published in reference material. Using the 1 Ω*mil^2/inch value may increase the accuracy of lossy simulations.

Positioning drivers with faster edges closer to the middle of the network typically results in more noise than positioning them towards the ends. However, Intel has shown that drivers located in all positions (given appropriate variations in the other network parameters) can generate the worst-case noise margin. Therefore, Intel recommends simulating the networks from all driver locations, and analyzing each receiver for each possible driver.

Analysis has shown that **both fast and slow corner conditions** must be run for both rising and falling edge transitions. The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum, causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. Slow corner models may produce minimum flight time violations on rising edges if the transition starts from a higher V_{OL}. So, Intel **highly recommends** checking for minimum and maximum flight time violations with both the fast and slow corner models. The fast and slow corner I/O buffer models are contained in the processor and Intel 820 chipset electronic models provided by Intel.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. Editing the simulator's net description or topology file generally does this.

Intel has found wide variation in noise margins when varying the stub impedance and the PCB's Z0 and S0. Intel therefore recommends that PCB parameters are controlled as tightly as possible, with a sampling of the allowable Z0 and S0 simulated. The Intel® Pentium® III processor nominal effective line impedance is 65 Ω ±15%. Future Intel® Pentium® III processor effective line impedance (Z_{EFF}) may be 60 Ω ±15%. Intel recommends the baseboard nominal effective line impedance to be at 60 Ω ±15% for the recommended layout guidelines to be effective. Intel also recommends running uncoupled simulations using the Z_0 of the package stubs; and performing fully coupled simulations if increased accuracy is needed or desired. Accounting for cross-talk within the device package by varying the stub impedance was investigated and was not found to be sufficiently accurate. This lead to the development of full package models for the component packages.

3.2.4 Place and Route Board

3.2.4.1 Estimate Component To Component Spacing for AGTL+ Signals

Estimate the number of layers that will be required. Then determine the expected interconnect distances between each of the components on the AGTL+ bus. Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

The required bus frequency and the maximum flight time propagation delay on the PCB determine the maximum network length between the bus agents. The minimum network length is independent of the required bus frequency. Table 3-2 and Table 3-3 assume values for CLK_{SKEW} and CLK_{JITTER} - parameters that are controlled by the system designer. To reduce system clock skew to a minimum, clock buffers that allow their outputs to be tied together are recommended. Intel strongly recommends running analog simulations to ensure that each design has adequate noise and timing margin.

3.2.4.2 Layout and Route Board

Route the board satisfying the estimated space and timing requirements. Also stay within the solution space set from the pre-layout sweeps. Estimate the printed circuit board parameters from the placement and other information including the following general guidelines:

- Distribute V_{TT} with a power plane or a partial power plane. If this cannot be accomplished, use as wide a trace as possible and route the V_{TT} trace with the same topology as the AGTL+ traces.

- Keep the overall length of the bus as short as possible (but do not forget minimum component-to-component distances to meet hold times).

- Plan to minimize cross-talk with the following guidelines developed for the example topology given (signal spacing recommendations were based on fully coupled simulations - spacing may be decreased based upon the amount of coupled length):

  — Use a spacing to line width to dielectric thickness ratio of at least 3:1:2. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%.

  — Minimize the dielectric process variation used in the PCB fabrication.

  — Eliminate parallel traces between layers not separated by a power or ground plane.

Figure 3-3 contains the trace width:space ratios assumed for this topology. The cross-talk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intra-group AGTL+ cross-talk involves interference between AGTL+ signals within the same group (See Section 3.4, "More Details and Insight" on page 3-19 for a description of the different AGTL+ group types). Intergroup AGTL+ cross-talk involves

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interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ cross-talk is when CMOS and AGTL+ signals interfere with each other.

Table 3-4. Trace Width Space Guidelines

Cross-talk Type	Trace Width:Space Ratio
Intragroup AGTL+ (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ (different group AGTL+)	5:15 or 6:18
AGTL+ to non-AGTL+	5:20 or 6:24

The spacing between the various bus agents causes variations in trunk impedance and stub locations. These variations cause reflections that can cause constructive or destructive interference at the receivers. A reduction of noise may be obtained by a minimum spacing between the agents. Unfortunately, tighter spacing results in reduced component placement options and lower hold margins. Therefore, adjusting the inter-agent spacing may be one way to change the network's noise margin, but mechanical constraints often limit the usefulness of this technique. Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.

There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require more attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two or more agents on the same clock edge, the two falling edge wave fronts will meet at some point on the bus and can sum to form a negative voltage. The ring-back from this negative voltage can easily cross into the overdrive region. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

This document addresses AGTL+ layout for both 1 and 2-way 133 MHz/100 MHz processor/ Intel® 820 chipset systems. Power distribution and chassis requirements for cooling, connector location, memory location, etc., may constrain the system topology and component placement location; therefore, constraining the board routing. These issues are not directly addressed in this document. contains a listing of several documents that address some of these issues.

3.2.4.3   Host Clock Routing

Host clock nets should be routed as point-to-point connections through a series resistor placed as close to the output pins of the clock driver as possible. The value of the series resistor is dependent on the clock driver characteristic impedance. However, a value of 33 Ω is a good starting point. Table 3-5 provides the trace length recommendations for this topology. "H" indicates the length of the host clock trace starting from the clock driver output pin and ending at the SC242 connector BCLK pin. Note that the clock route from the clock driver to the Intel 82820 MCH will require an additional trace length of approximately 4.6" to compensate for the additional propagation delay along the processor host clock path (SC242 connector plus processor cartridge trace). This value of 4.6" assumes a propagation speed of 180 ps/in.

Table 3-5. Host Clock Routing

Clock Net	Trace length
Clock driver to SC242 connector	H
Clock driver to Intel 82820 MCH	H + (clock delay from the processor edge to core) + connector delay

3.2.4.4   APIC Data Bus Routing

Intel recommends using the in-line topology shown in Figure 3-1 and Figure 3-2 for the APIC Data signals, PICD[1:0]. For dual-processor systems, the network should be dual-end terminated with 330 Ω resistors. The combined routing lengths of L1 plus L2 should be between 0.0" and 12.0".

Figure 3-1. PICD[1,0] Uni-Processor Topology
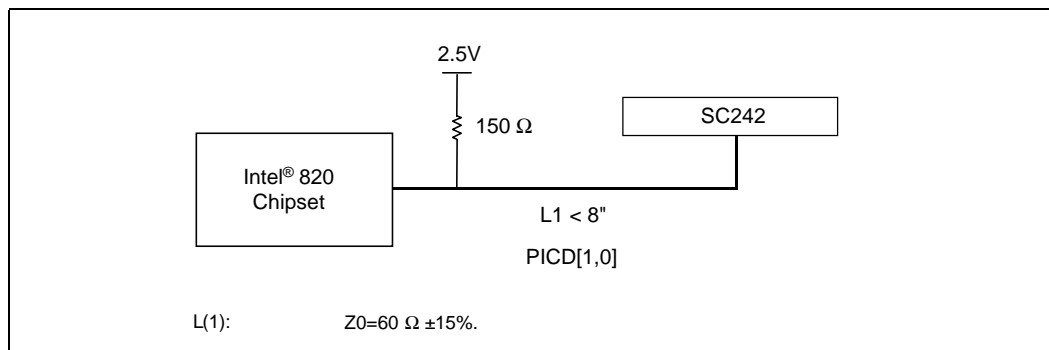
Figure 3-2. PICD[1,0] Dual-Processor Topology
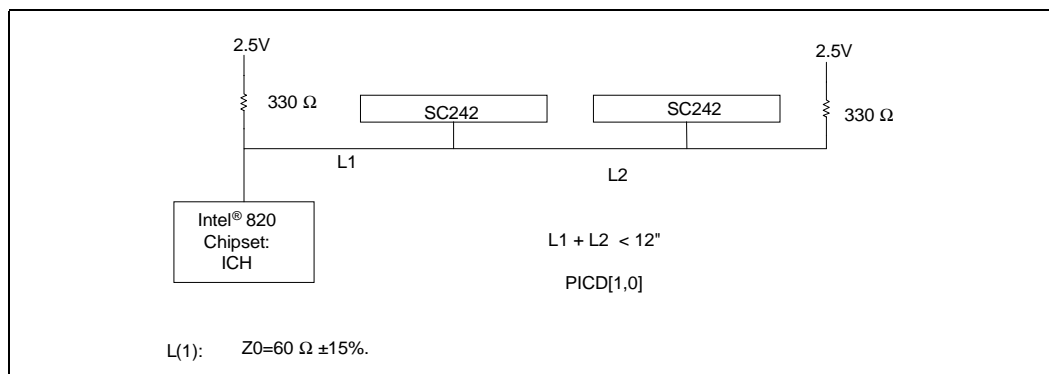
3.2.5 Post-Layout Simulation

Following layout, extract the interconnect information for the board from the CAD layout tools. Run simulations to verify that the layout meets timing and noise requirements. A small amount of "tuning" may be required; experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required. The post layout simulations should take into account the expected variation for all interconnect parameters.

Intel specifies signal integrity **at the device pads** and therefore recommends running simulations at the device pads for signal quality. However, Intel specifies core timings **at the device pins,** so simulation results at the device pins should be used later to correlate simulation performance against actual system measurements.

3.2.5.1 Intersymbol Interference

Intersymbol Interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

Intersymbol Interference (ISI) occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can occur when the line is driven high, low, and then high in consecutive cycles (the opposite case is also valid). When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum V_{OL} before the next rising edge is driven. This results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycle. ISI effects do not necessarily span only 3 cycles so it may be necessary to simulate beyond 3 cycles for certain designs. After simulating and quantifying ISI effects, adjust the timing budget accordingly to take these conditions into consideration.

3.2.5.2 Cross-Talk Analysis

AGTL+ cross-talk simulations can consider the processor core package, Intel 82820 MCH package, and SC242 connectors as non-coupled. Treat the traces on the processor cartridge and baseboard as fully coupled for maximum cross-talk conditions. Simulate the traces as lossless for worst case cross-talk and lossy where more accuracy is needed. Evaluate both odd and even mode cross-talk conditions.

AGTL+ Cross-talk simulation involves the following cases:

- Intra-group AGTL+ cross-talk
- Inter-group AGTL+ cross-talk
- Non-AGTL+ to AGTL+ cross-talk

3.2.5.3 Monte Carlo Analysis

Perform a Monte Carlo analysis on the extracted baseboard. Vary all parameters recommended for the pre-layout Monte Carlo analysis within the region that they are expected to vary. The range for some parameters will be reduced compared to the pre-layout simulations. For example, baseboard lengths L1 through L7 should no longer vary across the full min and max range on the final baseboard design. Instead, baseboard lengths should now have an actual route, with a length tolerance specified by the baseboard fabrication manufacturer.

3.2.6 Validation

Build systems and validate the design and simulation assumptions.

3.2.6.1 Measurements

Note that the AGTL+ specification for signal quality is at the **pad** of the component. The expected method of determining the signal quality is to run analog simulations for the pin and the pad. Then correlate the simulations at the pin against actual system measurements at the pin. Good correlation at the pin leads to confidence that the simulation at the pad is accurate. Controlling the temperature and voltage to correspond to the I/O buffer model extremes should enhance the correlation between simulations and the actual system.

3.2.6.2 Flight Time Simulation

As defined in Section 3.1, "Terminology and Definitions" on page 3-1, flight time is the time difference between a signal crossing V_{REF} at the input pin of the receiver, and the output pin of the driver crossing V_{REF} were it driving a test load. The timings in the tables and topologies discussed in this guideline assume the actual system load is 50 Ω and is equal to the test load. While the DC loading of the AGTL+ bus in a DP mode is closer to 25 Ω, AC loading is approximately 29 Ω since the driver effectively "sees" a 56 Ω termination resistor in parallel with a 60 Ω transmission line on the cartridge.

Figure 3-3. Test Load vs. Actual System Load
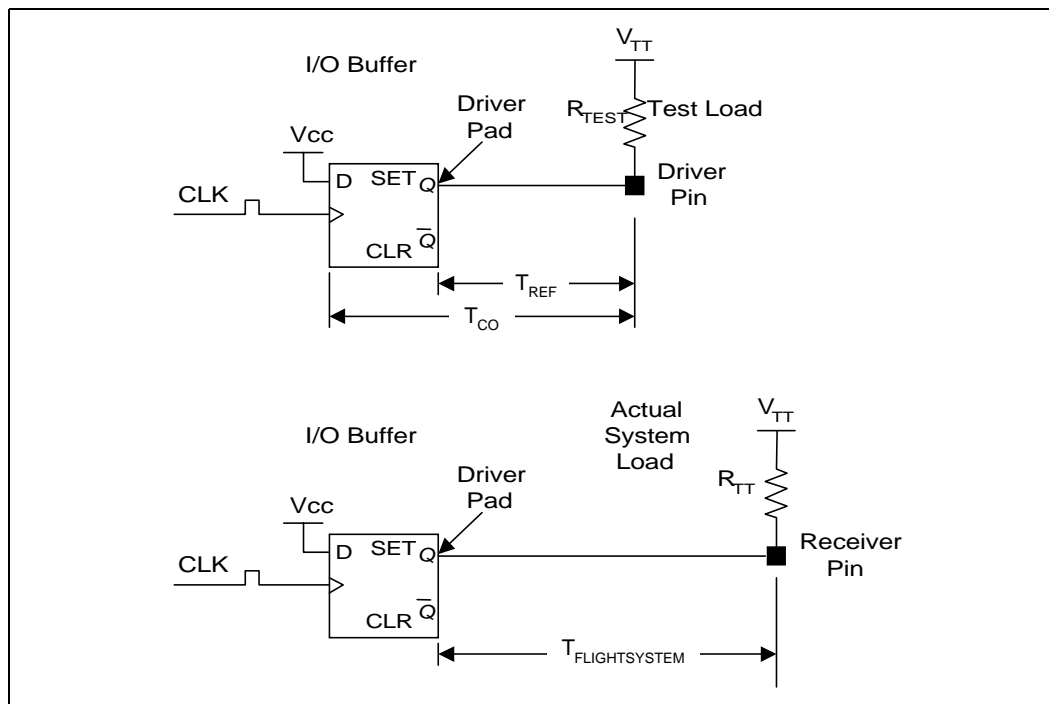
Figure 3-3 above shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical AGTL+ I/O buffer. T_{CO} timings are specified at the driver pin output. $T_{FLIGHT-SYSTEM}$ is usually reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver's input pin sees a valid data input. Since both timing numbers (T_{CO} and $T_{FLIGHT-SYSTEM}$) include propagation time from the pad to the pin, it is necessary to subtract this time (T_{REF}) from the reported flight time to avoid

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double counting. T_{REF} is defined as the time that it takes for the driver output pin to reach the measurement voltage, V_{REF}, starting from the beginning of the driver transition at the pad. T_{REF} must be generated using the same test load for T_{CO}. Intel provides this timing value in the AGTL+ I/O buffer models.

In this manner, the following *valid delay* equation is satisfied:

Equation 3-5. Valid Delay Equation

$$\text{Valid Delay} = T_{CO} + T_{FLIGHT\text{-}SYS} - T_{REF} = T_{CO\text{-}MEASURED} + T_{FLIGHT\text{-}MEASURED}$$

This valid delay equation is the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

3.2.6.3 Flight Time Hardware Validation

When a measurement is made on the actual system, T_{CO} and flight time do not need T_{REF} correction since these are the actual numbers. These measurements include all of the effects pertaining to the driver-system interface and the same is true for the T_{CO}. Therefore the addition of the measured T_{CO} and the measured flight time must be equal to the valid delay calculated above.

3.3 Theory

3.3.1 AGTL+

AGTL+ is the electrical bus technology used for the processor bus. This is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each load. The processor AGTL+ drivers contain a full-cycle active pull-up device to improve system timings. The AGTL+ specification defines:

- Termination voltage (V_{TT}).
- Receiver reference voltage (V_{REF}) as a function of termination voltage (V_{TT}).
- processor termination resistance (R_{TT}).
- Input low voltage (V_{IL}).
- Input high voltage (V_{IH}).
- NMOS on resistance (RON_N).
- PMOS on resistance (RON_P).
- Edge rate specifications.
- Ringback specifications.
- Overshoot/Undershoot specifications.
- Settling Limit.

3.3.2　Timing Requirements

The system timing for AGTL+ is dependent on many things. Each of the following elements combine to determine the maximum and minimum frequency the AGTL+ bus can support:

- The range of timings for each of the agents in the system.

  — Clock to output [T_{CO}]. (Note that the system load is likely to be different from the "specification" load therefore the T_{CO} observed in the system might not be the same as the T_{CO} from the specification.)

  — The minimum required setup time to clock [T_{SU_MIN}] for each receiving agent.

- The range of flight time between each component. This includes:

  — The velocity of propagation for the loaded printed circuit board [S_{EFF}].

  — The board loading impact on the effective T_{CO} in the system.

- The amount of skew and jitter in the system clock generation and distribution.

- Changes in flight time due to cross-talk, noise, and other effects.

3.3.3　Cross-talk Theory

AGTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies that have traditionally been used in personal computer designs. This requires that designers using AGTL+ be more aware of cross-talk than they may have been in past designs.

Cross-talk is caused through capacitive and inductive coupling between networks. Cross-talk appears as both backward cross-talk and as forward cross-talk. Backward cross-talk creates an induced signal on a victim network that propagates in a direction opposite that of the aggressor's signal. Forward cross-talk creates a signal that propagates in the same direction as the aggressor's signal. On the AGTL+ bus, a driver on the aggressor network is not at the end of the network; therefore it sends signals in both directions on the aggressor's network. Figure 3-4 shows a driver on the aggressor network and a receiver on the victim network that are not at the ends of the network. The signal propagating in each direction causes cross-talk on the victim network.

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Figure 3-4. Aggressor and Victim Networks
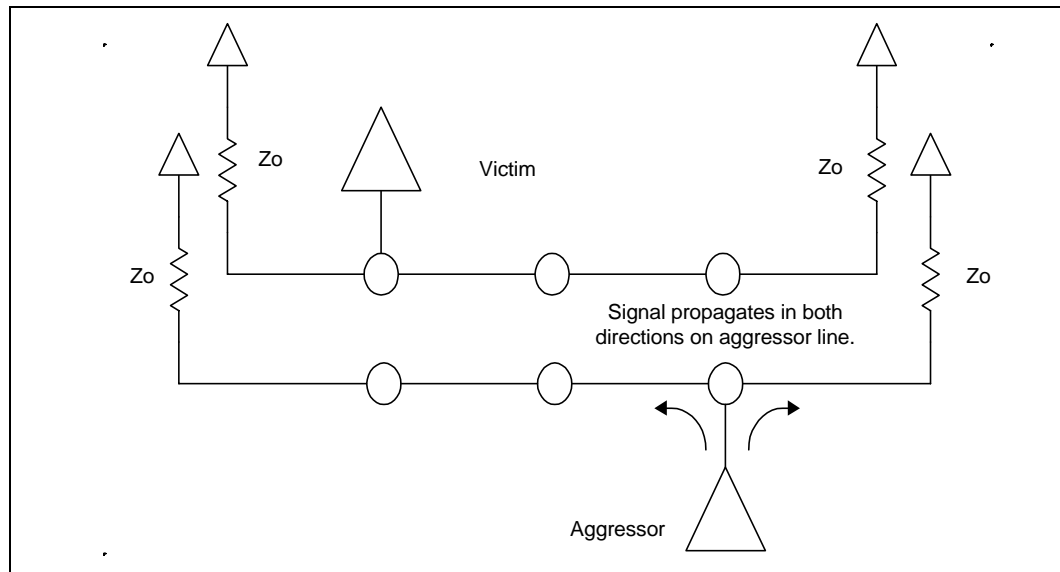
Figure 3-5. Transmission Line Geometry: (A) Microstrip (B) Stripline
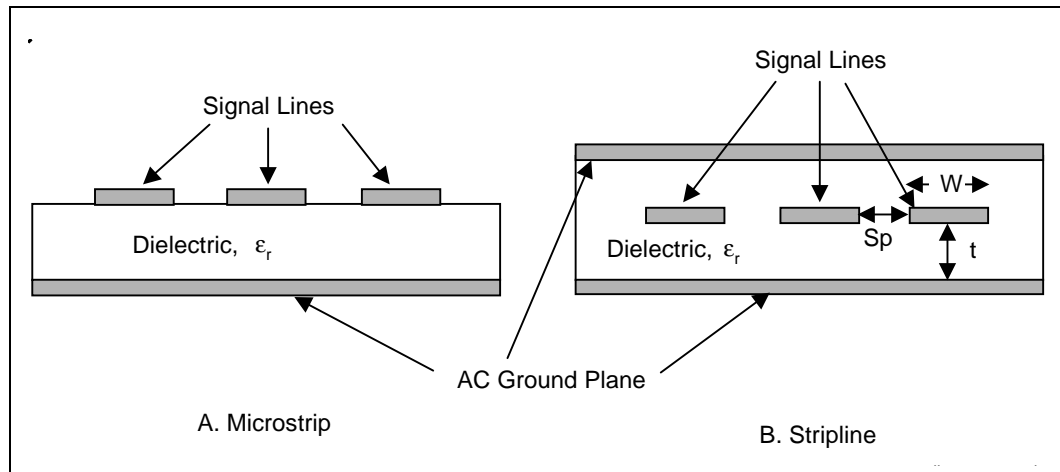
Additional aggressors are possible in the z-direction, if adjacent signal layers are not routed in mutually perpendicular directions. Because cross-talk-coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. The maximum cross-talk occurs when all the aggressors are switching in the same direction at the same time.

There is cross-talk internal to the IC packages, which can also affect the signal quality.

Backward cross-talk is present in both stripline and microstrip geometry's (see Figure 3-5). A way to remember which geometry is stripline and which is microstrip is that a stripline geometry requires **stripping** a layer away to see the signal lines. The backward coupled amplitude is proportional to the backward cross-talk coefficient, the aggressor's signal amplitude, and the coupled length of the network up to a maximum that is dependent on the rise/fall time of the aggressor's signal. Backward cross-talk reaches a maximum (and remains constant) when the

propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing, and the fall time on an unloaded coupled network, then:

$$LengthforMaxBackwardCrosstalk = \frac{\frac{1}{2} \times FallTime}{BoardDelayPerUnitLength}$$

An example calculation follows when the fast corner fall time is 3 V/ns and board delay is 175 ps/inch (2.1 ns/foot):

Fall time = 1.5 V÷3 V/ns = 0.5 ns

Length for Max Backward Cross-talk

= ½ * 0.5 ns * 1000 ps/ns ÷175 ps/in

= 1.43 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This causes backward cross-talk from segments on two sides of a driver. The pulses from the backward cross-talk travel toward each other and meet and **add** at certain moments and positions on the bus. This can cause the voltage (noise) from cross-talk to double.

3.3.3.1   Potential Termination Cross-Talk Problems

The use of commonly used "pull-up" resistor networks for AGTL+ termination may not be suitable. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks with separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

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3.4　More Details and Insight

3.4.1　Textbook Timing Equations

The "textbook" equations used to calculate the propagation rate of a PCB are the basis for spreadsheet calculations for timing margin based on the component parameters. These equations are:

Equation 3-6. Intrinsic Impedance

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (\Omega)$$

Equation 3-7. Stripline Intrinsic Propagation Speed

$$S_{0\_STRIPLINE} = 1.017 * \sqrt{\varepsilon_r} \quad (\text{ns/ft})$$

Equation 3-8. Microstrip Intrinsic Propagation Speed

$$S_{0\_MICROSTRIP} = 1.017 * \sqrt{0.475 * \varepsilon_r + 0.67} \quad (\text{ns/ft})$$

Equation 3-9. Effective Propagation Speed

$$S_{EFF} = S_0 * \sqrt{1 + \frac{C_D}{C_0}} \quad (\text{ns/ft})$$

Equation 3-10. Effective Impedance

$$Z_{EFF} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}} \quad (\Omega)$$

Equation 3-11. Distributed Trace Capacitance

$$C_0 = \frac{S_0}{Z_0} \quad (\text{pF/ft})$$

Equation 3-12. Distributed Trace Inductance

$$L_0 = 12 * Z_0 * S_0 \quad (\text{nH/ft})$$

Symbols for Equation 3-5 through Equation 3-12:

- S_0 is the speed of the signal on an unloaded PCB in ns/ft. This is referred to as the board propagation constant.

- $S_{0\ MICROSTRIP}$ and $S_{0\ STRIPLINE}$ refer to the speed of the signal on an unloaded microstrip or stripline trace on the PCB in ns/ft.

- Z_0 is the intrinsic impedance of the line in Ω and is a function of the dielectric constant (ε_r), the line width, line height and line space from the plane(s). The equations for Z_0 are not included in this document. See the *MECL System Design Handbook* by William R. Blood, Jr. for these equations.

- C_0 is the distributed trace capacitance of the network in pF/ft.

- L_0 is the distributed trace inductance of the network in nH/ft.

- C_D is the sum of the capacitance of all devices and stubs divided by the length of the network's trunk, not including the portion connecting the end agents to the termination resistors in pF/ft.

- S_{EFF} and Z_{EFF} are the effective propagation constant and impedance of the PCB when the board is "loaded" with the components.

3.4.2 Effective Impedance and Tolerance/Variation

The impedance of the PCB needs to be controlled when the PCB is fabricated. The method of specifying control of the impedance needs to be determined to best suit each situation. Using stripline transmission lines (where the trace is between two reference planes) is likely to give better results than microstrip (where the trace is on an external layer using an adjacent plane for reference with solder mask and air on the other side of the trace). This is in part due to the difficulty of precise control of the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase cross-talk.

The effective line impedance (Z_{EFF}) is recommended to be 60 Ω ±15%, where Z_{EFF} is defined by Equation 3-10.

3.4.3 Power/Reference Planes, PCB Stackup, and High Frequency Decoupling

3.4.3.1 Power Distribution

Designs using the Pentium III processor require several different voltages. The following paragraphs describe some of the impact of two common methods used to distribute the required voltages. Refer to the *Flexible Motherboard Power Distribution Guidelines* for more information on power distribution.

The most conservative method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes are used as an "AC ground" reference for traces to control trace impedance on the board, then the plane needs to be AC coupled to the system ground plane. This method may require more total layers in the PCB than other methods. A 1-ounce/ft^2 thick copper is recommended for all power and reference planes.

A second method of power distribution is to use partial planes in the immediate area needing the power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing area that can be used to route traces. These partial planes may also

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change the impedance of adjacent trace layers. (For instance, the impedance calculations may have been done for microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.)

3.4.3.2 Reference Planes and PCB Stackup

It is **strongly recommended** that baseboard stackup be arranged such that AGTL+ signals are referenced to a ground (VSS) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path that can lead to large SSO effects that degrade timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will expose the platform to a risk that is very hard to predict in pre-layout simulation. Figure 3-6 shows the ideal case where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

Figure 3-6. One Signal Layer and One Reference Plane
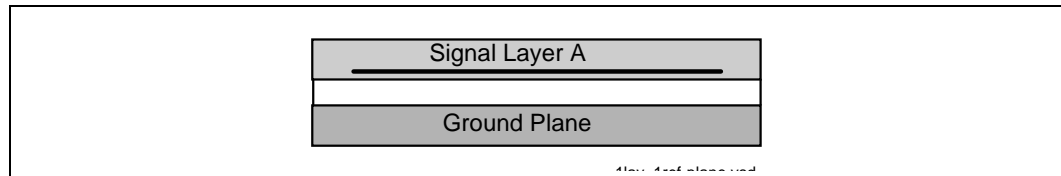
When it is not possible to route the entire AGTL+ signal on a single VSS referenced layer, there are methods to reduce the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 3-7). Figure 3-8 shows another method of minimizing layer switch discontinuities, but may be less effective than Figure 3-7. In this case, the signal still references the same type of reference plane (ground). In such a case, it is important to stitch (i.e., connect) the two ground planes together with vias in the vicinity of the signal transition via.

Figure 3-7. Layer Switch with One Reference Plane
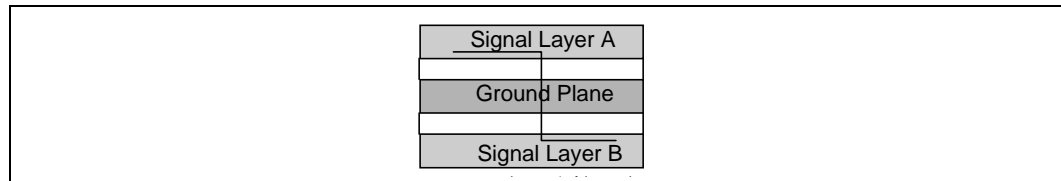
Figure 3-8. Layer Switch with Multiple Reference Planes (same type)
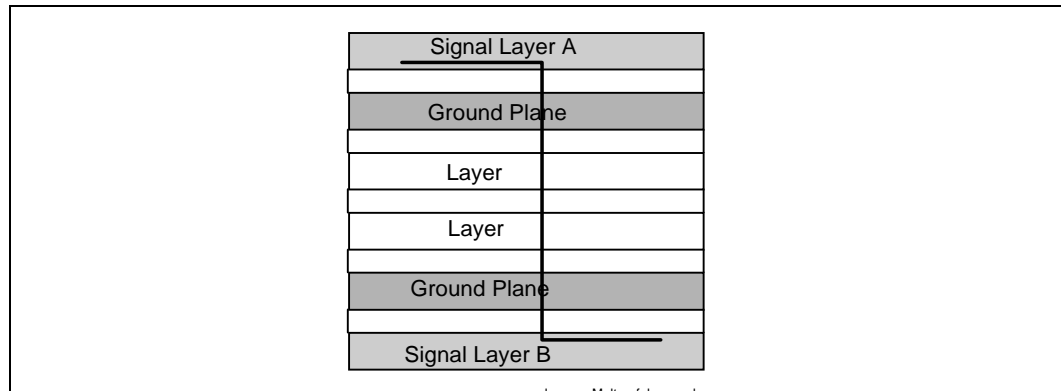
When routing and stackup constraints require that an AGTL+ signal reference VCC or multiple planes, special care must be given to minimize the SSO impact to timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling wherever the transitions occur, as shown in Figure 3-9 and Figure 3-10. Such decoupling should, again, be in the vicinity of the signal transition via and use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps it is recommended to space the VSS and VCC vias as close as possible and/or use dual vias since the via inductance may sometimes be higher than the actual capacitor inductance.

Figure 3-9. Layer Switch with Multiple Reference Planes
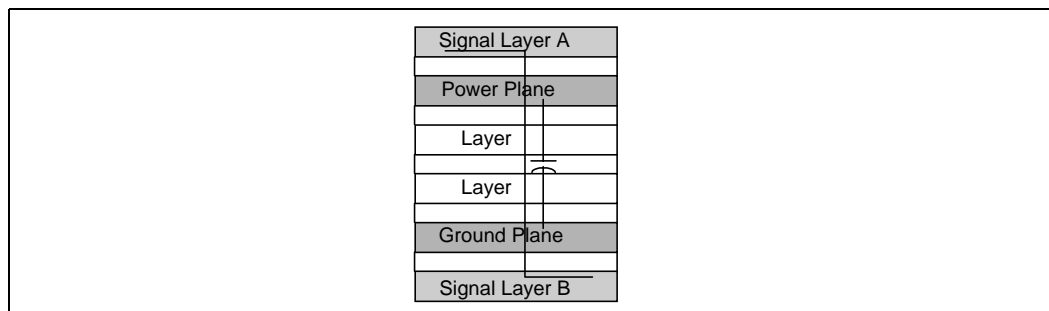
Figure 3-10. One Layer with Multiple Reference Planes
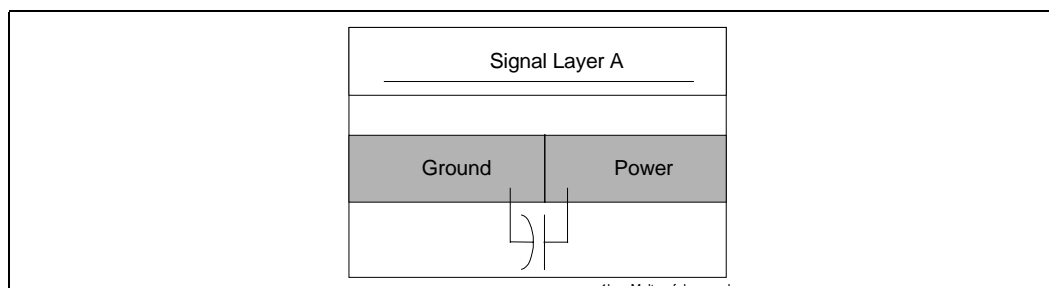
3.4.3.3 High Frequency Decoupling

This section contains several high frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will very likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities may also occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across VCC_{CORE} and ground at the SC242 connector interface on the baseboard will minimize the discontinuity in the signal's reference plane at this junction. Note that these additional high-frequency decoupling capacitors are in addition to the high-frequency decoupling already on the processor.

Transmission line geometry also influences the return path of the reference plane. The following are decoupling recommendations that take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling between all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 82820 MCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

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3.4.3.4 SC242 Connector

Intel studies indicate that the use of thermal reliefs on the connector pin layout pattern (especially ground pins) should be minimized. Such reliefs (cartwheels or wagon-wheels) increase the net ground inductance and reduce the integrity of the ground plane to which many signals are referenced. Increased ground inductance has been shown to aggravate SSO effects. Also, the anti-pad diameters (clearance holes in the planes) for the signal pins should be minimized since large anti-pads also reduce the integrity of the ground plane and increase inductance.

Some additional layout and EMI-reduction guidelines regarding the SC242 connector follow:

- Extend power/ground planes up to the SC242 connector pins.

- Extend the reference planes for AGTL+ and other controlled-impedance signals up to the SC242 connector pins.

- Minimize or remove thermal reliefs on power/ground pins.

- Route V_{TT} power with the widest signal trace or mini-plane as possible. Place decoupling caps across V_{TT} and ground in the vicinity of the connector pins.

- Use a ground plane under the principal component side of the baseboard (and secondary side if it contains active components).

- Distribute decoupling capacitors across power and ground pins evenly around the connector (less than 0.5 inch spacing) on the primary and secondary sides.

- Minimize serpentine traces on outer layers.

3.4.4 Clock Routing

Analog simulations are required to ensure clock net signal quality and skew is acceptable. The system clock skew must be kept to a minimum (The calculations and simulations for the example topology given in this document have a total clock skew of 200 ps and 150 ps of clock jitter). For a given design, the clock distribution system, including the clock components, must be evaluated to ensure these same values are valid assumptions. Each processor's datasheet specifies the clock signal quality requirements. To help meet these specifications, follow these general guidelines:

- Tie clock driver outputs if clock buffer supports this mode of operation.

- Match the electrical length and type of traces on the PCB (microstrip and stripline may have different propagation velocities).

- Maintain consistent impedance for the clock traces.

    — Minimize the number of vias in each trace.

    — Minimize the number of different trace layers used to route the clocks.

    — Keep other traces away from clock traces.

- Lump the loads **at the end** of the trace if multiple components are to be supported by a single clock output.

- Have equal loads at the end of each network.

The **ideal** way to route each clock trace is on the same single inner layer, next to a ground plane, isolated from other traces, with the same total trace length, to the same type of single load, with an equal length ground trace parallel to it, and driven by a zero skew clock driver. When deviations from ideal are required, going from a single layer to a pair of layers adjacent to power/ground planes would be a good compromise. The fewer number of layers the clocks are routed on, the smaller the impedance difference between each trace is likely to be. Maintaining an equal length

and parallel ground trace for the **total length of each** clock ensures a low inductance ground return and produces the minimum current path loop area. (The parallel ground trace will have lower inductance than the ground plane because of the mutual inductance of the current in the clock trace.)

3.5 Definitions of Flight Time Measurements/ Corrections and Signal Quality

Acceptable signal quality must be maintained over all operating conditions to ensure reliable operation. Signal Quality is defined by four parameters: Overshoot, Undershoot, Settling Limit, and Ringback. Timings are measured at the pins of the driver and receiver, while signal integrity is observed at the receiver chip pad. When signal integrity at the pad violates the following guidelines and adjustments need to be made to flight time, the adjusted flight time obtained at the chip pad can be assumed to have been observed at the package pin, usually with a small timing error penalty.

3.5.1 V_{REF} Guardband

To account for noise sources that may affect the way an AGTL+ signal becomes valid at a receiver, V_{REF} is shifted by ΔV_{REF} for measuring minimum and maximum flight times. The V_{REF} Guardband region is bounded by $V_{REF}-\Delta V_{REF}$ and $V_{REF}+\Delta V_{REF}$. ΔV_{REF} has a value of 100 mV, which accounts for the following noise sources:

- Motherboard coupling
- V_{TT} noise
- V_{REF} noise

3.5.2 Ringback Levels

The example topology covered in this guideline assumes ringback tolerance allowed to within 200 mV of 2/3 V_{TT}. Since V_{TT} is specified with approximate total ±11% tolerance, this implies a 2/3 V_{TT} (V_{REF}) range from approximately 0.89 V to 1.11 V. This places the absolute ringback limits at:

- 1.3 V (1.1 V + 200 mV) for rising edge ringback
- 0.69 V (0.89 V – 200 mV) for falling edge ringback

A violation of these ringback limits requires flight time correction as documented in the *Intel® Pentium® II Processor Developer's Manual.*

3.5.3 Overdrive Region

The overdrive region is the voltage range, at a receiver, from V_{REF} to V_{REF} + 200 mV for a low-to-high going signal and V_{REF} to V_{REF} - 200 mV for a high-to-low going signal. The overdrive regions encompass the V_{REF} Guardband. So, when V_{REF} is shifted by ΔV_{REF} for timing measurements, the overdrive region **does not** shift by ΔV_{REF}. Figure 3-11 depicts this relationship. Corrections for edge rate and ringback are documented in the *Intel® Pentium® II Processor Developer's Manual.* However, there is an exception to the documented correction method. The *Intel® Pentium® II Processor Developer's Manual* states that extrapolations should be made from the last crossing of the overdrive region back to V_{REF}. Simulations performed on this topology

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should extrapolate back to the appropriate V_{REF} Guardband boundary, and not V_{REF}. So, for maximum rising edge correction, extrapolate back to $V_{REF} + \Delta V_{REF}$. For maximum falling edge corrections, extrapolate back to $V_{REF} - \Delta V_{REF}$.

Figure 3-11. Overdrive Region and V_{REF} Guardband
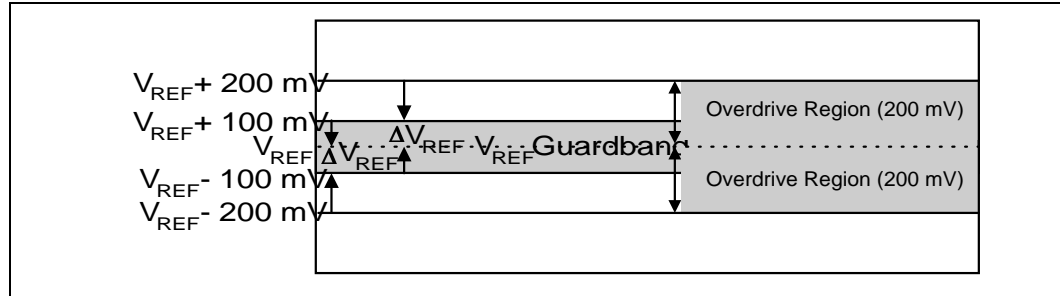
3.5.4 Flight Time Definition and Measurement

Timing measurements consist of minimum and maximum flight times to take into account that devices can turn on or off anywhere in a V_{REF} Guardband region. This region is bounded by $V_{REF}-\Delta V_{REF}$ and $V_{REF}+\Delta V_{REF}$. The minimum flight time for a rising edge is measured from the time the driver crosses V_{REF} when terminated to a test load, to the time when the signal first crosses $V_{REF}-\Delta V_{REF}$ at the receiver (see Figure 3-12). Maximum flight time is measured to the point where the signal first crosses $V_{REF}+\Delta V_{REF}$, assuming that ringback, edge rate, and monotonicity criteria are met. Similarly, minimum flight time measurements for a falling edge are taken at the $V_{REF}+\Delta V_{REF}$ crossing and maximum flight time is taken at the $V_{REF}-\Delta V_{REF}$ crossing.

Figure 3-12. Rising Edge Flight Time Measurement
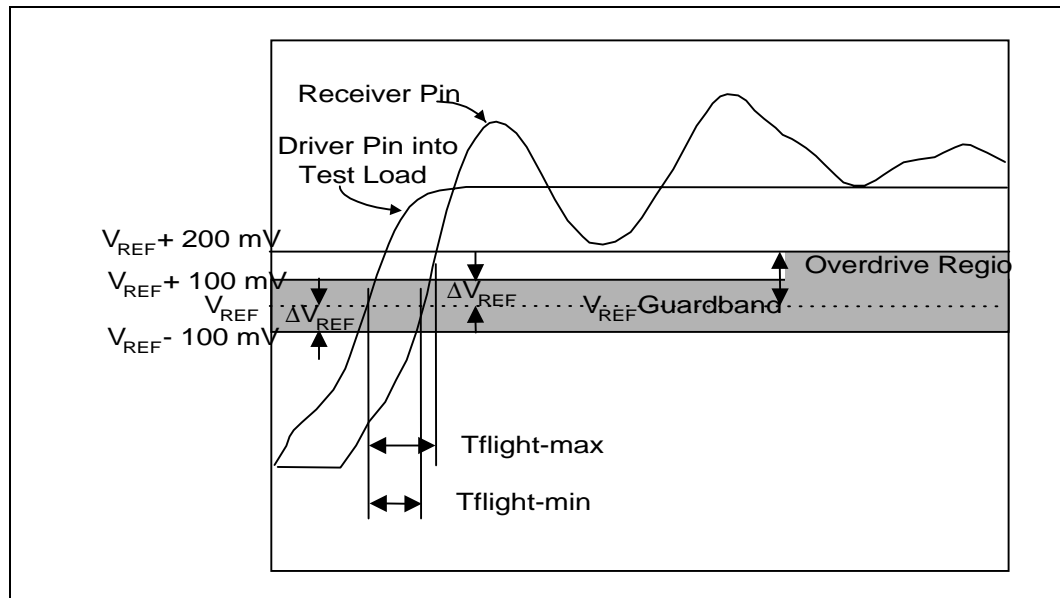
3.6 Conclusion

AGTL+ routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will provide the designer with the best chance of avoiding the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.

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Clocking

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Clocking 4

4.1 Clock Generation

There are two clock generator components required in an Intel® 820 chipset based system. The Direct Rambus* Clock Generator (DRCG) generates clock for the Direct Rambus* interface while the CK133 component generates clocks for the rest of the system. Clock synthesizers that meet the Intel CK98 Clock Specification are suitable for an Intel® 820 chipset based system. The CK133 generates the clocks listed in Table 4-1.

Table 4-1. Intel® 820 Chipset Platform System Clocks

Number	Name on CK133	Used for	Routed to	Name on Receiver	Frequency	Voltage
4	CPUCLK[0-3]	System Bus Clock	2 Processors	CLK	100/133 MHz	2.5V
			MCH	HCLKIN		
			ITP	BCLK		
3	APIC[0-2]	APIC Bus Clock	2 Processors	PICCLK	33 MHz	2.5V
			ICH	APICCLK		
8	PCICLK[1-7,F]	PCI Bus Clock	5 PCI Devices	CLK	33 MHz	3.3V
		PCI, LPC, FWH Flash BIOS Bus Clock	ICH	PCICLK		
		FWH Flash BIOS Interface Clock	FWH Flash BIOS	CLK		
		LPC Interface Clock	LPC	CLK		
4	3V66[0-3]	Hub Interface/AGP Bus Clock	MCH	CLK66	66 MHz	3.3V
		Hub Interface Clock	ICH	CLK66		
		AGP Bus Clock	AGP device/ slot	CLK		
		Unused	N/A	N/A		
2	REF[0-1]	Internal ICH Logic	ICH	CLK14	14 MHz	3.3V
		Internal Super I/O Logic	Super I/O	Vendor Specific		
1	48 MHz	USB	ICH	CLK48	48 MHz	3.3V
2	CPU_DIV2[0-1]	DRCG Reference Clock	DRCG	REFCLK	50/66 MHz	2.5V
		Unused	N/A	N/A		

The CK133 is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clock are 2.5V. As a result, the CK133 device requires both 3.3V and 2.5V. These power supplies should be a clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines.

The MCH uses the same clock for hub interface and AGP. It is important that the hub interface/AGP clocks are routed to ensure the skew requirements are met between:

- The MCH hub interface/AGP clock and the AGP connector (or device)

- The MCH hub interface/AGP clock and the ICH hub interface clock.

The DRCG reference clock operates at one-half the CPU clock frequency. It is an input into the DRCG and is used to generate the Direct RDRAM "Clock to Master" differential pair (CTM, CTM#).

The DRCG generates one pair of differential Direct RDRAM Clocks (CTM, CTM#) from the reference clock generated by the CK133. In addition, the DRCG uses phase information provided by the MCH to phase align the direct RDRAM clock with the CPU clocks. This phase alignment information is provided to the DRCG via the SYNCLKN and PCLKM pins.

Figure 4-1. Intel® 820 Chipset Platform Clock Distribution

* The free-running PCI clock should be connected to the ICH.
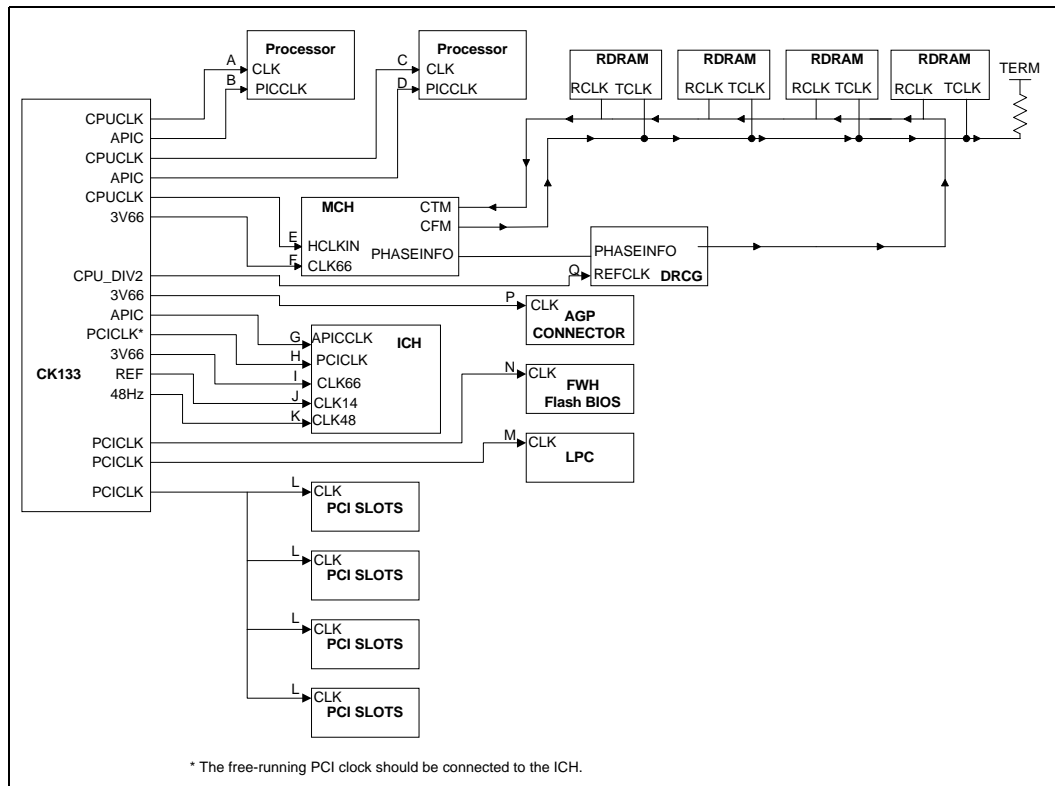
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Table 4-2. Intel® 820 Chipset Platform Clock Skews

Clock Symbols See Figure 4-1	Relationship	Skew						Notes
		Pin-to-Pin (ps)		Board (ps)		Total (ps)		
		Min	Max	Min	Max	Min	Max	
A leads C, A leads E (or C leads E)	SC242 HCLK to SC242 HCLK (DP ONLY) And SC242 HCLK to MCH HCLK (DP ONLY)	-175	+175	-125	+125	-300	+300	1, 7
A leads E	SC242 HCLK to MCH HCLK (UP ONLY)	0	0	-125	+125	-125	+125	2, 3, 7
P leads F	MCH CLK66 to AGP graphics device AGPCLK	0	0	-125	+125	-125	+125	4, 8
L leads another L (or L leads H)	PCICLK to PCICLK	-500	+500	-1500	+1500	-2000	+2000	
I leads H	ICH CLK66 leads ICH PCICLK	+1500	+4000	-500	+500	+1000	+4500	
F leads I	ICH CLK66 to MCH CLK66	-250	250	-125	+125	-375	+375	8
Worst case skew between H, L, M and N	Worst case FWHCLK, LPCCLK, PCICLK	-500	+500	-1500	+1500	-2000	+2000	5
B leads D, B leads G	Processor PICCLK leads Processor PICCLK And Processor PICCLK leads ICH APICCLK	-250	+250	-125	+125	-375	+375	6

NOTES:
1. DP Only
2. UP: MCH and CPU clock drivers are tied together to eliminate pin-to-pin skew. –175 and +175 pin-to-pin skew only apply to DP.
3. UP Only
4. Clock drivers tied together to eliminate pin-to-pin skew.
5. The skew between any PCICLK clocks on any two inputs in the system.
6. The skew between any APIC clocks on any two inputs in the system.
7. If SSC is enabled, an additional ±40ps must is added to the pin-to-pin skew
8. If SSC is enabled, an additional ±60ps must is added to the pin-to-pin skew

Figure 4-2 shows the Intel® 820 chipset clock length routing guidelines.

Figure 4-2. Intel® 820 Chipset Clock Routing Guidelines[1,2]

Note:
1. Tie 3V66 clock for the MCH to 3V66 clock for the AGP connector to eliminate pin-to-pin skew.
2. These calculations based on 150ps/in trace velocity.
3. The TBD value will be derived from the PCI Revision 2.2 Specification which allows for a maximum of ±2ns clock skew.
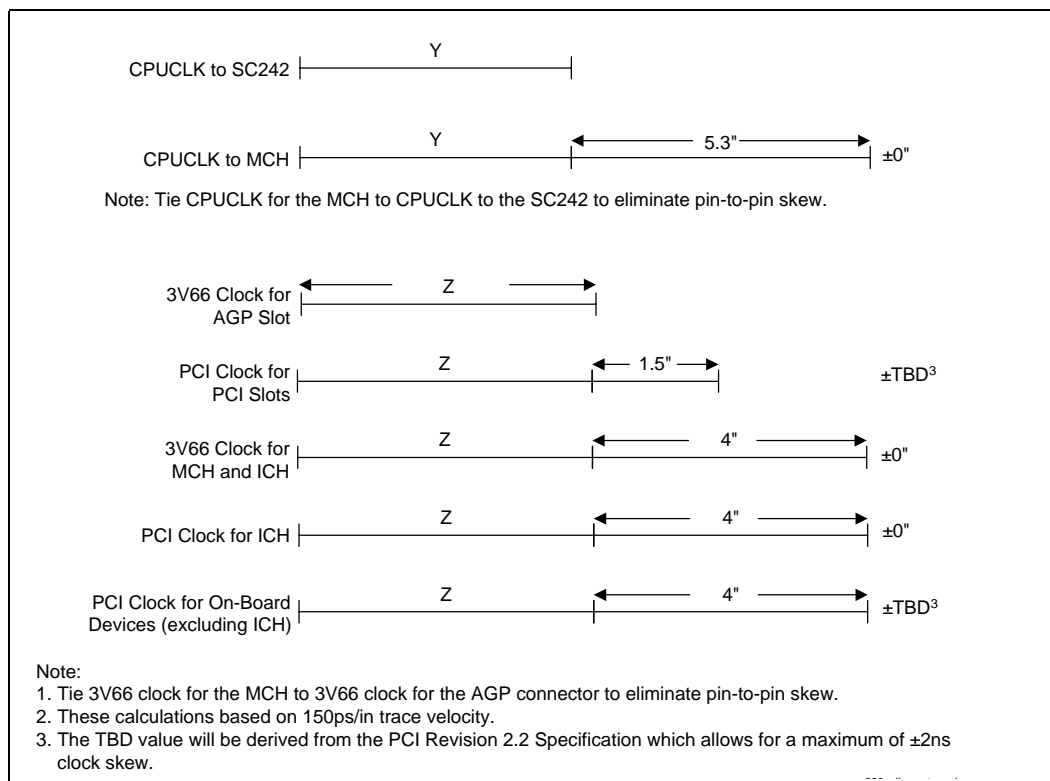
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Table 4-3. Intel® 820 Chipset Platform System Clock Cross-Reference

CK133/DRCG Pin Name	Component	Pin Name
PCICLK	PCI Slot	CLK
	PCI Slot	CLK
	PCI Slot	CLK
	PCI Slot	CLK
	PCI Slot	CLK
	ICH	PCICLK-F
	LPC Super I/O	CLK
	FWH Flash BIOS	CLK
3V66	MCH	GCLKIN
	ICH	CLK66
	AGP Connector (on-board device)	CLK
48 MHz	ICH	CLK48
CPUCLK	CPU	BCLK
	CPU	BCLK
	MCH	HCLKIN
CPU_div2	DRCG	Refclk
APIC	CPU	PICCLK
	CPU	PICCLK
	ICH	APICCLK
Clk/ClkB[1]	RDRAMs	
	MCH	CTM/CTM#
CFM/CFM#[1,2]	RDRAMs	
PclkM	MCH	HCLKOUT
SynclkN	MCH	RCLKOUT

NOTES:
1. Differential Clocking Pair
2. CFM/CFM# driven by MCH

4.2 Component Placement and Interconnection Layout Requirements

Detailed explanation of layout requirements for each interconnections are provided in the following sections:

- Crystal to CK133
- CK133 to DRCG
- MCH to DRCG
- DRCG to RDRAM channel

4.2.1 14.318 MHz Crystal to CK133

The distance between the crystal and the CK133 should be minimized. The maximum trace length is 500 mils.

4.2.2 CK133 to DRCG

- CPU_div2
- VDDIR – Used as a reference for 2.5V signaling

Figure 4-3. CK133 to DRCG Routing Diagram
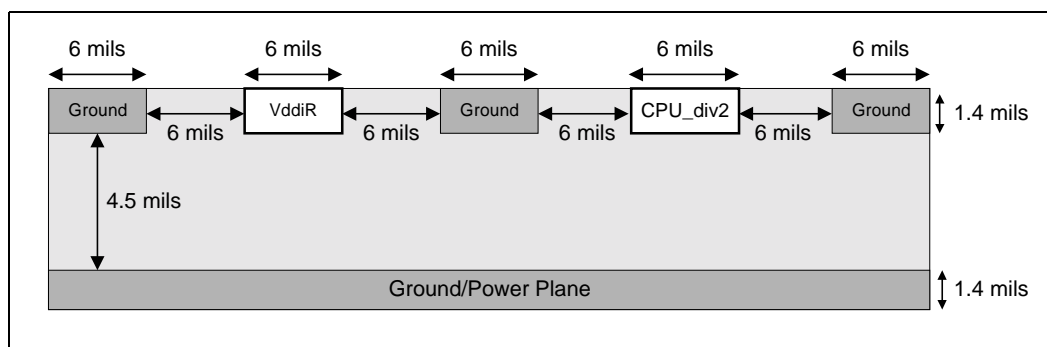
VddIR and CPU_div2 must be routed as shown in Figure 4-3. Note that the VddiR pin can be connected directly to 2.5V near the DRCG if the 2.5V plane extends near the DRCG. However, if a 2.5V trace must be used, it should originate at the CK133 and be routed as shown.

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4.2.3   MCH to DRCG

- PclkM
- PclkN
- VddIPD

Figure 4-4. MCH to DRCG Routing Diagram
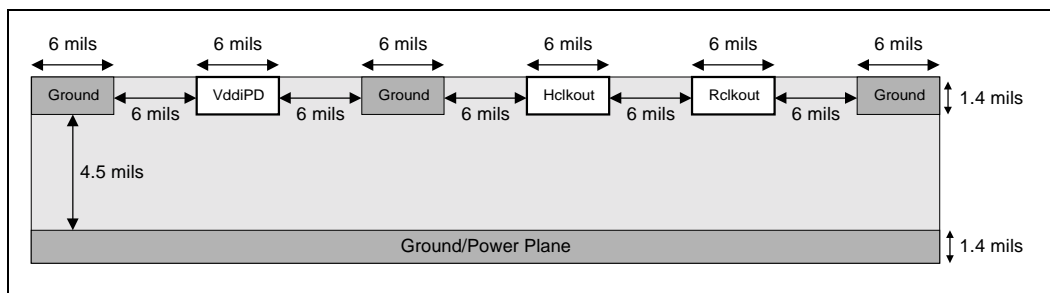
The Hclkout, Rclkout and VddiPD should be routed as shown in Figure 4-4. Note that the VddiPD pin can be connected directly to 1.8V near the DRCG if the 1.8V plane extends near the DRCG. However, if a 1.8V trace must be run, it should originate at the MCH and be routed as shown.

The maximum length for Hclkout and Rclkout is 6". Additionally, Hclkout and Rclkout must be length matched (to each other) within 50 mils. These signals should be routed on the same layer. If the signals must switch layers, then BOTH signals should change layers together.

If VddiPD is connected to the 1.8V plane using a via (e.g., a trace is not run from the MCH), Hclkout and Rclkout must still be routed differentially and ground isolated.

Figure 4-5. Direct Rambus* Clock Routing Dimensions
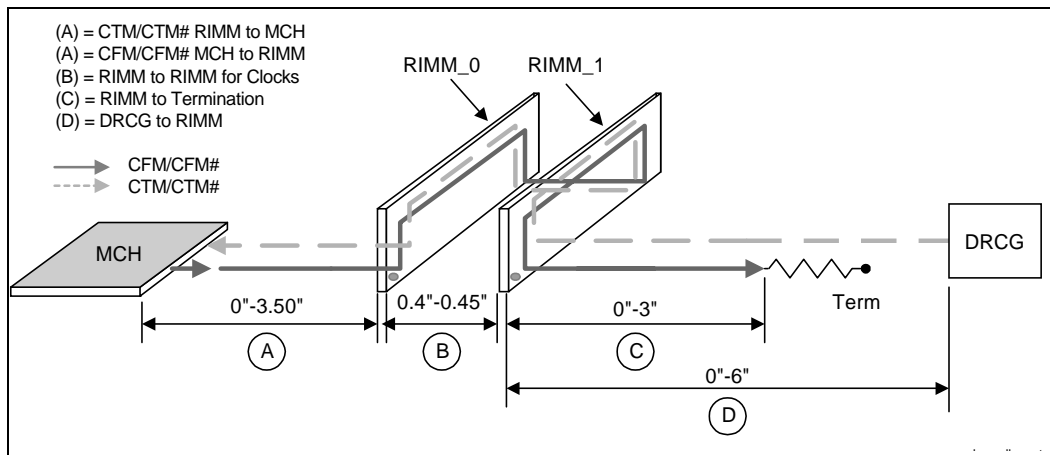
4.2.4 DRCG to RDRAM Channel

The Direct Rambus* clock signals (CTM/CTM# and CFM/CFM#) are high-speed, impedance matched transmission lines. The Direct Rambus* clocks begin at the end of the Direct Rambus* channel and propagate to the controller as CTM/CTM# (see Figure 4-5), where it loops back as CFM/CFM#. Table 4-4 lists the placement guidelines.

Table 4-4. Placement Guidelines for Motherboard Routing Lengths

Direct Rambus* Clock Routing Length Guidelines				
Clock	**From**	**To**	**Length (inches)**	**Section***
CTM/CTM#	DRCG	Last RIMM Connector	0.000 – 6.000	D
	RIMM	RIMM	0.400 – 0.450	B
	1st RIMM Connector	Chipset	0.000 – 3.500	A
CFM/CFM#	Chipset	1st RIMM Connector	0.000 – 3.500	A
	RIMM	RIMM	0.400 – 0.450	B
	Last RIMM Connector	Termination	0.000 – 3.000	C

NOTE: * Refer to Figure 4-5

Trace Geometry

In Sections labeled 'A' and 'D' (Figure 4-5) the clock signals (CTM/CTM# and CFM/CFM#) must be 14 mils wide and routed as shown in Figure 4-6. For all other sections ('B' and 'C') the clock signals must be routed with 18 mil wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via every 1". A 6 mil gap is required between the clock signals and the ground isolation traces. For the section labeled "A" in Figure 4-5, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clocks faster trace velocity as described in Section 2.6.2.1, "RSL Routing" on page 2-8. The CTM/CTM# and the CFM/CFM# differential signal pairs must be length matched to ±2 mils in line section labeled 'A' and for the line sections labeled 'B' using the trace length methods in Section 2.6.2.1, "RSL Routing" on page 2-8. For the section labeled 'D' the trace length matching for CTM/CTM# is ±2 mils, **and for the section labeled 'C', ±2 mil trace length matching is required for the CFM/CFM# signals.**

The CTM/CTM# signals must be ground referenced (with a continuous ground island/plane) from the DRCG to the Last RIMM.

4.2.5 Trace Length

For the section labeled "A" in Figure 4-5 (1st RIMM to MCH and MCH to 1st RIMM), CTM/CTM# and CFM/CFM# must be length matched within ±2 mils (exact trace length matching is recommended). **Package trace compensation (as described in** Section 2.6.2.1, "RSL Routing" on page 2-8**), via compensation, and RSL signal layer alternation must** also be completed on the clock signals. Additionally, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clocks faster trace velocity as described in Section 2.6.2.1.

For the line sections labeled 'B' (Figure 4-5) (RIMM to RIMM) the clock signals must be matched within ±2 mils to the trace length of every RSL signal. Exact length matching is preferred.

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For the line section labeled 'D' (DRCG to Last RIMM) the CTM/CTM# must be length matched within ±2 mils (exactly is recommended), **and for the section labeled 'C', ±2 mil trace length matching is required for the CFM/CFM# signals.**

Note: Total trace length matching for the entire CTM/CTM# signal trace (Sections A+B+D) and for the CFM/CFM# signal trace (Sections A+B) is ±2 mils (exact length matching is recommended).

Figure 4-6. Differential Clock Routing Diagram (Section 'A', 'C', & 'D')
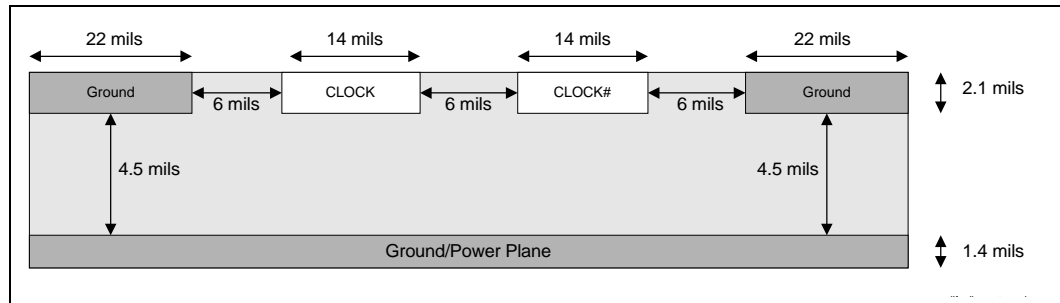
Figure 4-7. Non-Differential Clock Routing Diagram (Section 'B')
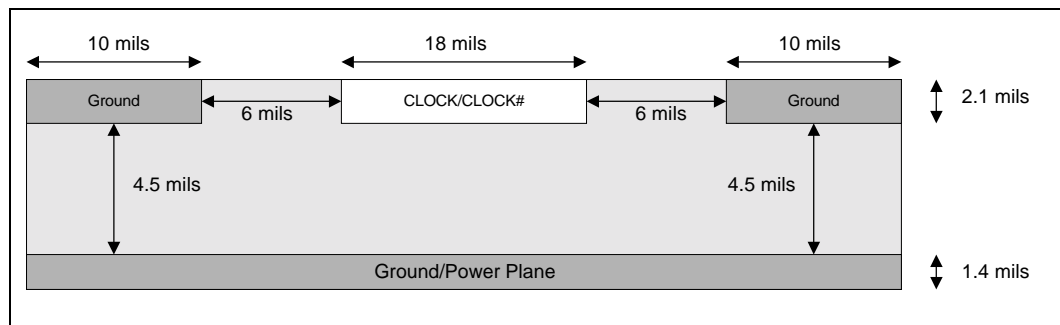
The CFM/CFM# differential pair signals require termination using either 27 Ω 1% or 28 Ω 2% resistors and a 0.1 uF capacitor as shown in Figure 4-8.

Figure 4-8. Termination for Direct Rambus* Clocking Signals CFM/CFM#
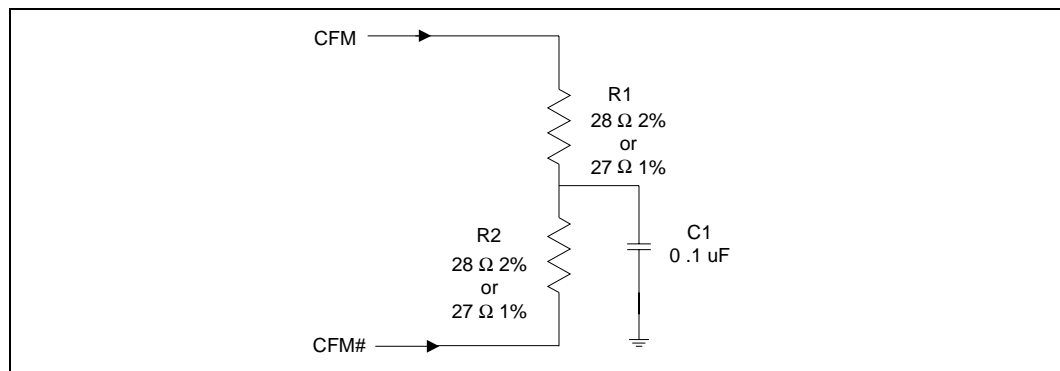
4.3 DRCG Impedance Matching Circuit

The external DRCG impedance matching circuit is shown in Figure 4-9. The values for the elements are listed in Table 4-5.

Figure 4-9. DRCG Impedance Matching Network
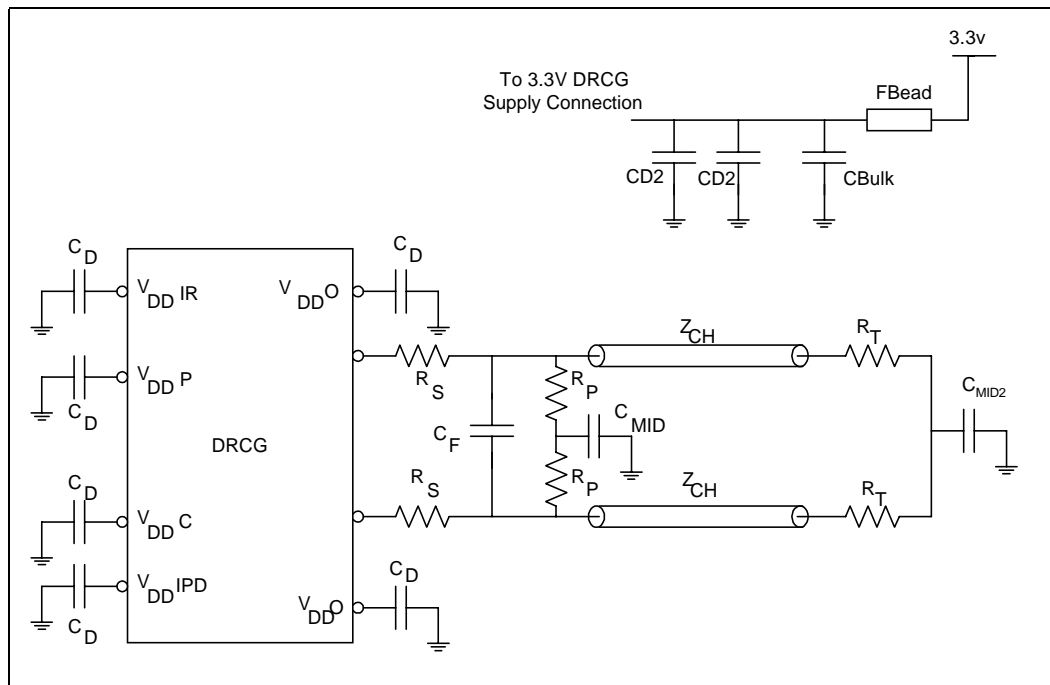
Table 4-5. External DRCG Component Values[1,2]

Component	Nominal Value	Notes
C_D	0.1 uF	Decoupling caps to ground
R_S	39 Ohms	Series termination resistor
R_P	51 Ohms	Parallel termination resistor
C_{MID}, C_{MID2}	0.1 uF	Virtual ground caps
R_T	27 Ohms	End of channel termination
C_F	4 pF	Do not stuff
FBead	50 Ohms at 100 MHz	Ferrite bead
CD2	0.1 uF	Additional 3.3V decoupling caps
CBulk	10 uF	Bulk cap on device side of ferrite bead

NOTES:
1. The ferrite bead and 10 uF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system.
2. 0.1 uF capacitors are better than 0.01 uF or 0.001 uF caps for DRCG decoupling.

The circuit shown in Figure 4-9 is required to match the impedance of the DRCG to the 28 Ω channel impedance. More detailed information can be found in the Direct Rambus Clock Generator Specification.

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4.3.1 DRCG Layout Example

Figure 4-10. DRCG Layout Example

Cmid - 100pF

EMI Cap - 4pF
Do Not Stuff

CTM/CTM# route on
bottom layer

Rs - 39Ω
(Keep trace from DRCG to
Rs VERY short)

Rp - 51Ω
(Keep trace from Rs
to Rp short)

Decoupling Cap - 0.1uF
(Place VERY Near DRCG 3.3V Pin!)

Decoupling Cap - 0.1uF
(Place VERY Near DRCG 3.3V Pin!)

3.3V-DRCG Flood
Flood 3.3V-DRCG on the top layer

around DRCG. Flood MUST include:
4 DRCG Power Pins
4 0.1uF Capacitors
1 10uF Bulk Capacitor
1 Isolation Ferrite Bead

Decoupling Cap - 0.1uF
(Place VERY Near DRCG 3.3V Pin!)

Decoupling Cap - 0.1uF
(Place VERY Near DRCG 3.3V Pin!)

Bulk Decoupling Cap - 10uF
(Place Near DRCG)

Ferrite Bead
(L22 in Reference Schematics)

4.4 AGP Clock Routing Guidelines

The AGP clock must be routed with 20 mil spacing to all other signals and it must meet the length guidelines in Figure 4-2.

4.5 Series Termination Resistors for CK133 Clock Outputs

All used outputs require series termination resistors. The recommended resistor value will be defined by simulations. The stub length to the CK133 of these resistors can be compromised to make room for decoupling caps. The rule is to keep all resistor stubs within 250 mils of the CK133. If routing rules allow, Rpacks can be used if power dissipation is not exceeded for the Rpack.

4.6 Unused Outputs

All unused clock outputs must be tied to ground through a series resistor approximately the impedance of the output buffer (shown below.) The intent of these resistors is to terminate the unused outputs to eliminate EMI.

Table 4-6. Unused Output Termination

Buffer Name	VCC Range (V)	Impedance (Ohms)	If Unused Output Termination to VSS
CPU, CPU_Div2, IOAPIC	2.375 - 2.625	13.5 - 45	30 Ohms
48 MHz, REF	3.135 - 3.465	20 - 60	40 Ohms
PCI, 3V66	3.135 - 3.465	12 - 55	33 Ohms

4.7 Decoupling Recommendation for CK133 and DRCG

Some CK133 vendors may integrate the XTAL_IN and XTAL_OUT frequency adjust capacitors. However, pads should be placed on the board for these external capacitors for testing/debug.

To further reduce jitter and voltage supply noise, the addition of a ferrite filter with 2 caps (10 uF and 0.1 uF) on both the 2.5V and 3.3V planes close to the clock devices is recommended. This applies to both DRCG and CK133.

4.8 DRCG Frequency Selection and the DRCG+

4.8.1 DRCG Frequency Selection Table and Jitter Specification

To allow additional flexibility in board design, Intel has enabled a variation of the DRCG labeled the *DRCG+*. The device has the same specifications, pinout and form-factor as the existing DRCG device document. There are two modifications made to the DRCG+.

1. The DRCG+ Mult[0:1] select table has changed to modify two of the multiplier ratios. The DRCG+ will support 133/356 MHz using 66 MHZ DRCG+ input clock and a 16/3 multiplier. An additional 9/2 multiplier allows 133/300 MHz (not supported by the Intel[®] 820 chipset). Support for 300 MHz and 400 MHz memory bus is unchanged. The following table lists the DRCG Ratio.

Table 4-7. DRCG Ratio

Mult[0:1]	DRCG	DRCG+
0:0	4:1	9:2
0:1	6:1	6:1
1:0	8:3	16:3
1:1	8:1	8:1

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2. The Intel® 820 chipset supports the following ratios and can be supported by the DRCG and DRCG+ or derivative devices. Contact your DRCG vendor for information on DRCG, DRCG+, and derivative products.

100 MHz Host Bus		133 MHz Host Bus	
Frequency	Multiplier	Frequency	Multiplier
100 / 300	6:1	133 / 266	4:1
100 / 400	8:1	133 / 356	16:3
		133 / 400	6:1

3. The jitter timing specifications are expanded to encompass both the component specification (for DRCG or derivative products) and the channel specification. Follow the component specification when measuring jitter at the DRCG output resistor. Follow the channel jitter guidelines when measuring jitter at the MCH or at the termination for CFM/CFM# on the RDRAM interface.

Output Frequency (MHz)	Component Jitter Specification	Channel Jitter Guidelines
400	50 ps	100 ps
356	60 ps	110 ps
300	70 ps	120 ps
266	80 ps	130 ps

4.8.2   DRCG+ Frequency Selection Schematic

DRCG+ frequency selection can be accomplished using two GPIOs connected to the MULT[0:1] pins as shown in Figure 4-11. This allows selection of all frequencies supported by the Intel® 820 chipset.

Figure 4-11. DRCG+ Frequency Selection
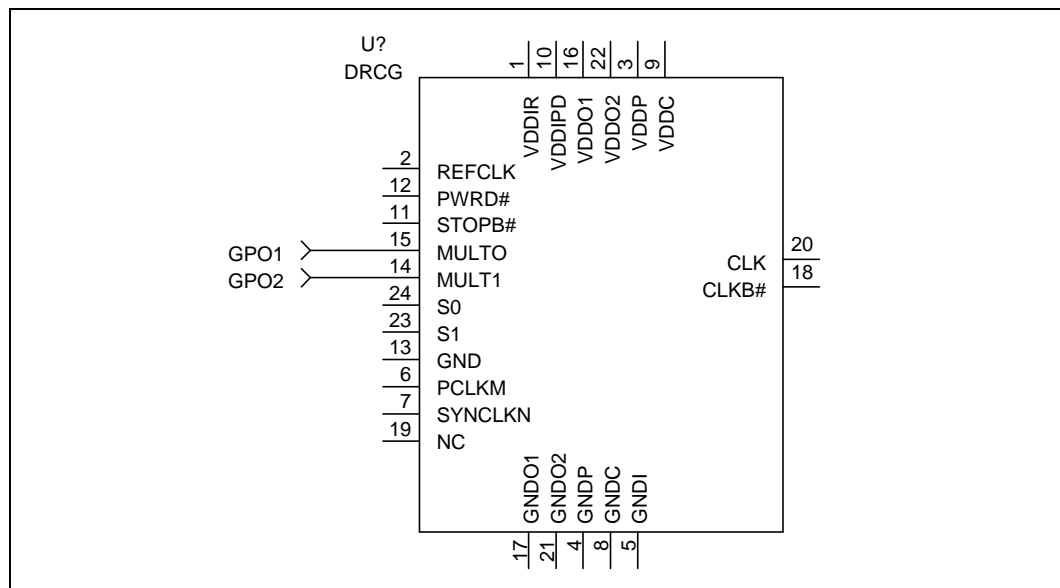
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**System
Manufacturing**

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System Manufacturing 5

5.1 In Circuit FWH Flash BIOS Programming

All cycles destined for the FWH Flash BIOS appear on PCI. The ICH hub interface to PCI Bridge puts all processor boot cycles out on PCI (before sending them out on the FWH Flash BIOS interface to the FWH Flash BIOS). If the ICH is set for subtractive decode, these boot cycles can be accepted by a positive decode agent out on PCI. The enables the ability to boot from of a PCI card that positively decodes these memory cycles. To boot from a PCI card it is necessary to keep the ICH in subtractive decode mode. If a PCI boot card is inserted and the ICH is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind the 82380AB. Once you have booted from the PCI card, you could potentially program the FWH Flash BIOS in circuit and program the ICH CMOS.

5.2 FWH Flash BIOS Vpp Design Guidelines

The Vpp pin on the FWH Flash BIOS is used for programming the flash cells. The FWH Flash BIOS supports Vpp of 3.3V or 12V. If Vpp is 12V, the flash cells will program about 50% faster than at 3.3V. However, the FWH Flash BIOS only supports 12V Vpp for 80 hours. The 12V Vpp would be useful in a programmer environment that is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3V on the motherboard.

5.3 Stackup Requirement

5.3.1 Overview

The Intel$^\circledR$ 820 chipset platform requires a board stackup with a 4.5 mil prepreg. This change in dimension (previously, typically 7 mil) is required because of the signaling environment used for Direct RDRAM, AGP 2.0 and hub interface. The RDRAM Channel is designed for 28 Ω and mismatched impedance will cause signal reflections which will reduce voltage and timing margins. For example, with a 2X clock at 400 MHz operation, which equals a 1.25 ns sampling window, only 100 ps is allotted for total channel timing error. Channel error results not only from PCB impedance, but also PCB and Z_0 process variation. Therefore, it is critical to attain the required 28 Ω impedance.

5.3.2 PCB Materials

PCB tolerances determine Z_0 variation. Those tolerances include trace width, pre-preg thickness, plating thickness, and dielectric constant. Pre-preg type impacts H tolerance and ε_r including single ply, 2-ply, and resin content.

To design to the correct Z_0 variation, PCB's typically need to meet the following (see Table 5-2):
- Height tolerance ±10% (~ 0.4 mil)
- Width tolerance ±2.5% (~ 0.4 mil)
- ε_r tolerance ±5% (~0.2)

Stackup Requirement: 28Ω ±10%

Figure 5-1. 28Ω Trace Geometry
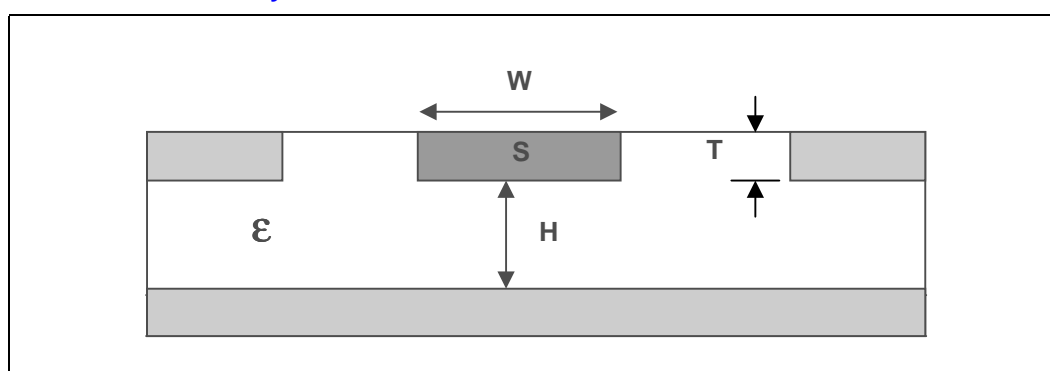
5.3.3 Design Process

To meet the tight tolerances required a good design process to use is:

- Specify the material to be used

- Calculate board geometries for the desired impedance - or use the example stackup provided

- Build test boards and coupons

- Measure board impedance using a TDR and follow Intel's Impedance Test Methodology Document (found on developer.intel.com)

- Measure geometries with cross-section

- Adjust design parameters and/or material as required

- Build a new board, re-measure the key parameters and be prepared to generate one or two board iterations

This process will require iteration: design, build, test, modify, build, test…

5.3.4 Test Coupon Design Guidelines

Characterization and understanding of the trace impedance is critical for delivering reliable systems at the increased bus frequencies. Incorporating a test coupon design into the motherboard makes testing simpler and more accurate. The test coupon pattern must match the probe type being used.

The location of the test coupon is listed in order of preference below:

- 1st Choice (Ideal Location) =   Memory section of the motherboard
- 2nd Choice   =   Any section of the motherboard
- 3rd Choice   =   Separate location in the panel

The Intel Impedance Test Methodology Document should be used to ensure boards are within the 28Ω ±10% requirement. The Intel Controlled Impedance Design and Test Document should be used for the test coupon design and implementation. These documents can be found at:

> http://developer.intel.com/design/chipsets/memory/rdram.htm

> — Select "Application Notes"

5.3.5 Recommended Stackup

Though numerous variations of stackup are possible, it is recommended that the following should be used as a starting point:

> W=18 mil, H=4.5 mil, T=2.0, 1 ply 2116 pre-preg

For other possibilities see Table 5-1 and following figures:

Table 5-1. 28Ω Stackup Examples

Sample	Zo	H	W	T	SM(max)	Resin %
1	27.1	4.3	18.0	2.1	0.6	53.0
2	28.1	3.8	18.5	1.6	1.2	72.0
3	28.6	4.8	19.0	2.5	0.7	61.0

5.3.6 Inner Layer Routing

Inner Layer Routing also has many possible stackups. For Inner Layer Routing, it is recommended to use the following as a starting point:

> W=13.5 mil, H1=7 mil, H2=5, T=1.2

With these parameters, initial TDR should fall within acceptable limits - 28 Ω ±10%

Figure 5-2 shows examples of both Stripline and Microstrip cross sections.

Figure 5-2. (a,b) Microstrip and Stripline Cross-section for 28 Ω Trace
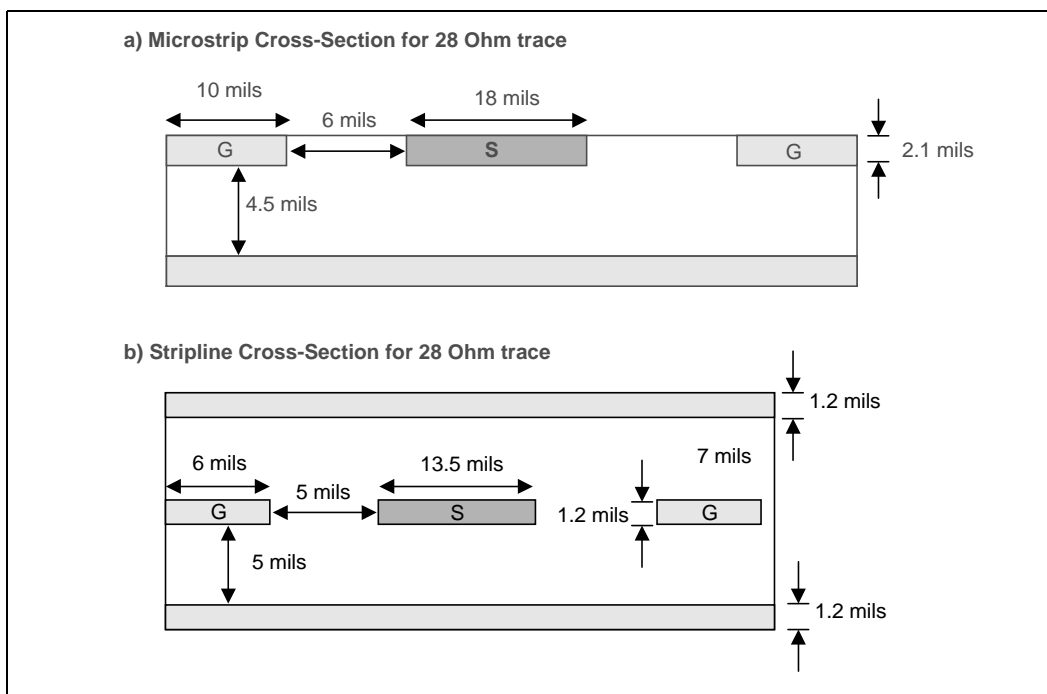
Note: Don't forget ground floods and stitching

5.3.7   Impedance Calculation Tools

The 3D Field Solvers (e.g., those by HP, Ansoft, Sonnet, and Polar) are the most accurate for calculating impedance. Z calculators based on equations (zcalc) are also fairly accurate. The differences are shown in Table 5-2.

Table 5-2. 3D Field Solver vs ZCALC

	#1	#2	#3	#4	#5	#6
H	4.5	4.5	4.2	4.8	4.5	4.5
W	18	18	18	18	17	19
W1	18.1	18.1	18.1	18.1	17.1	19.1
T	1.4	2.8	1.4	1.4	1.4	1.4
εr	4.5	4.5	4.5	4.5	4.5	4.5
Z0(3D)	29.0	28.4	27.6	30.4	30.2	27.9
Z0(zcalc)	29.1	28.7	27.7	30.4	30.2	28.0

5.3.8   Testing Board Impedance

The *Intel Impedance Test Methodology Document* should be used to ensure boards are within the 28 Ω ±10% requirement. This document can be found at: http://developer.intel.com.

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5.3.9 Board Impedance/Stackup Summary

1. ***7628 Cloth, 1 ply 0.007" when cured with 40% resin*** is the most popular and highest volume PCB in production today. This stackup will make routing impossible.

   - Fab Construction (4 Layers)
   - $Z_o = 70\ \Omega \pm 15\%$

Figure 5-3. 7 mil Stackup (Not Routable)

Component Side Layer: 1/2 oz Cu
7 Mil Prepreg
Ground Layer 2: 1 oz Cu

Not Routable   Total Thickness = 62 mils

Ground Layer 3: 1 oz Cu
7 Mil Prepreg
Solder Side Layer 4: 1/2 oz Cu
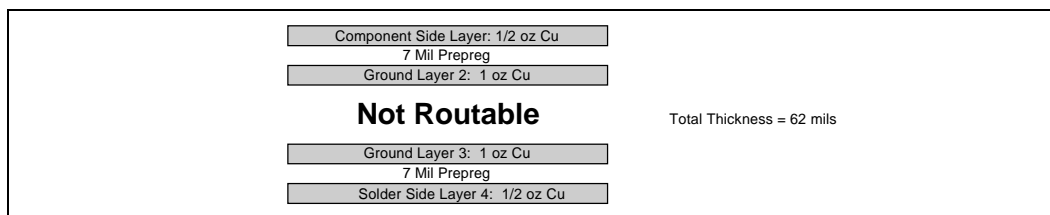
2. ***2116 Cloth, 1 ply 0.0045" when cured with 53% resin*** is the second largest volume in production today. Due to the impedance & layout requirement of traces for Direct RDRAM, AGP 2.0, and hub interface, this stackup is recommended for Intel[®] 820 chipset platform design.

   - Fab Construction (4 Layers)
   - $Z_o = 60\ \text{ohms} \pm 10\%$

Figure 5-4. 4.5 mil Stackup

Component Side Layer: 1/2 oz Cu
4.5 Mil Prepreg
Ground Layer 2: 1 oz Cu

~48 Mil Core   Total Thickness = 62 mils

Ground Layer 3: 1 oz Cu
4.5 Mil Prepreg
Solder Side Layer 4: 1/2 oz Cu

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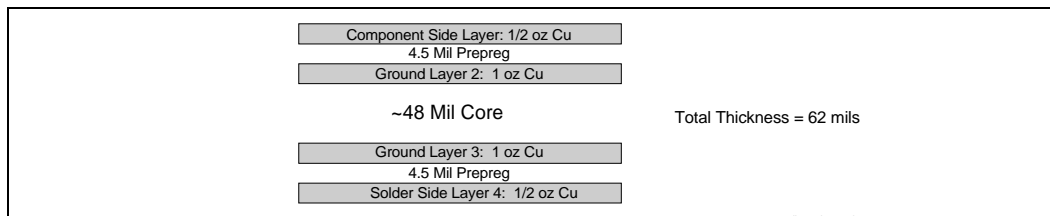
System Design Considerations

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System Design Considerations   6

6.1   Power Delivery

6.1.1   Terminology and Definitions

Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered. This state is used in the Reference Board (refer to Appendix A, "Reference Design Schematics: Uni-Processor" or Appendix B, "Reference Design Schematics: Dual-Processor") to satisfy the S3 ACPI power management state.
Full-power operation	During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (CPU stop-grant state) state.
Suspend operation	During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Power rails	An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, 5VSB. In addition to these power rails, several other power rails are created with voltage regulators on the Intel® 820 Chipset Reference Board.
Core power rail	A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed *directly* from the ATX power supply are: ±5V, ±12V and +3.3V.
Standby power rail	A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is: 5VSB (5V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator (on the Intel® 820 Chipset Reference Board, 3.3VSB is derived from 5V_DUAL).
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

6.1.2 Intel® 820 Chipset Customer Reference Board Power Delivery

Figure 6-1 shows the power delivery architecture for the Intel® 820 Chipset Reference Board. This power delivery architecture supports the "Instantly Available PC Design Guidelines" via the suspend-to-RAM (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH resume well, PCI wake devices (via 3.3V aux) and USB (USB can only be powered if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device's power requirements, both in suspend and in full-power. The power requirements must be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3V aux (and possibly other devices in the system), it is necessary to create a dual power rail.

Figure 6-1. Intel® 820 Chipset Power Delivery Example
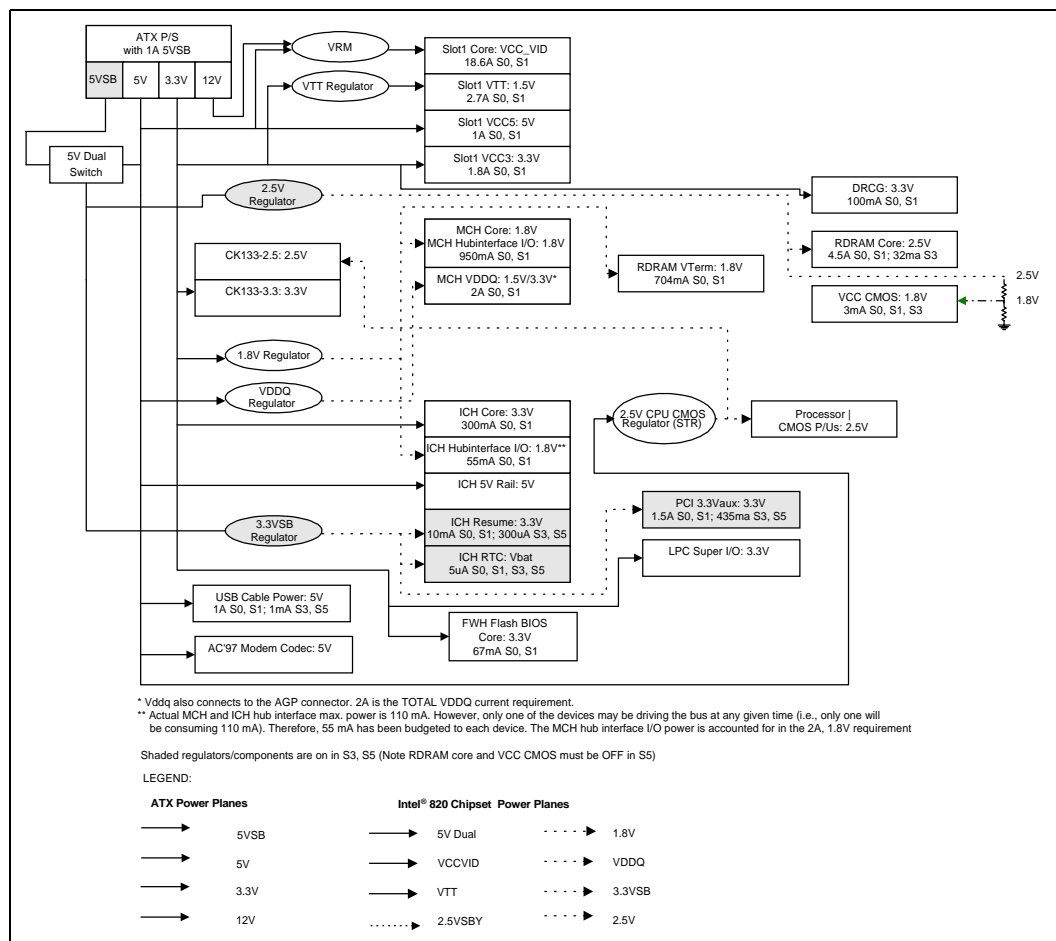
The examples given in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical, when deviating from these examples in any way, to consider the effect of the change.

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In addition to the power planes provided by the ATX power supply, an *instantly available* Intel® 820 chipset based system (using Suspend-to-RAM*)* requires 7 power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the Intel® 820 Chipset Reference Board will have a *5V Dual Switch*.

5V Dual Switch

This switch powers the *5V Dual plane* from the 5V core ATX supply during full-power operation. During Suspend-to-RAM*,* the 5V Dual plane is powered from the 5V Standby power supply.

Note: The voltage on the 5V Dual plane **is not 5V!** There is a resistive drop through the 5V Dual Switch that must be considered. Therefore, NO COMPONENTS should be connected directly to the 5V Dual plane. On the Intel® 820 chipset Reference Board, the only devices connected to the 5V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in a Intel® 820 chipset based system that does not support Suspend-to-RAM (STR).

VCC$_{VID}$

This power plane is used to power the SC242 processor. Refer to the latest revisions of:

- *VRM 8.4 DC-DC Converter Design Guidelines*
- *Slot 1 Power Delivery Guidelines*

Note: This regulator is required in ALL designs.

V$_{TT}$

This power plane is used to power the AGTL+ termination resistors. Refer to the latest revisions of:

- *Intel® Pentium® III Processor* Datasheet

Note: This regulator is required in ALL designs.

2.5VSBY

The 2.5VSBY power plane is used to power the RDRAM core and the VCMOS rail on the RDRAMs. The RDRAM core requires approximately 4.5A maximum average DC current at 2.5V (refer to Section 6.1.3, "64/72Mbit RDRAM Excessive Power Consumption" on page 6-5). In the Intel® 820 Chipset Reference Board, the 2.5VSBY plane is derived from the 5V Dual power plane using a switching regulator. It is important, that during the maximum load-step of 2A, the maximum voltage fluctuation is less than 50 mV. The maximum 2.5V tolerance is 125 mV, however during any 10 uS period, the voltage can not fluctuate more than 50 mV. The high-frequency bypassing requirements are met using capacitors on the RIMM itself. Low frequency bypass requirements vary depending on the voltage regulator used. Using a switching regulator, with a relatively slow response time, the low frequency bypass recommendation is: 8 100 uF bulk capacitors (0.1Ω ESR) near the RIMM connectors. These capacitors must be placed near the RIMM connector. Preferably spread the capacitors around where 2.5V connects to the RIMMs.

The VCMOS rail requires a maximum of 3ma at 1.8V. This rail MUST be powered during Suspend-to-RAM and therefore, the VCMOS rail can not be connected to the MCH core power. Because the current requirements of VCMOS are so low, a resistor divider can be used to generate VCMOS from 2.5VSBY. The resistor divider should be 36 Ω (top) / 100 Ω (bottom). Additionally, it should be bypassed with a 0.1 µF chip capacitor.

The Intel® 820 Chipset Reference Board is using a switching regulator from 5V Dual. It may be possible to use a linear regulator to regulate from 3.3VSB, however the thermal characteristics must be considered. Additionally, a low drop out linear regulator would be necessary. If 2.5VSBYis regulated from 3.3VSB, it is important the 3.3VSB regulator can supply enough current for all the 3.3VSB device requirements as well as the 2.5VSBY requirements.

Refer to the 1.8V power plane information for 1.8V and 2.5V power sequencing requirement.

Note: Refer to section Section 6.1.3, "64/72Mbit RDRAM Excessive Power Consumption" on page 6-5 for more details.

Note: This regulator is required in ALL designs, however in systems that do not support STR, the 2.5V rail would be powered from either the 3.3V or 5V core well.

1.8V

The 1.8V plane powers the MCH core, the ICH hub interface I/O buffers and the RDRAM termination resistors. This power plane has a total power requirement of approximately 1.7A. The 1.8V plane should be decoupled with a 0.1 uF and a 0.01 uF chip capacitor at *each* corner of the MCH and with a single 1 uF and 0.1 uF capacitor at the ICH. Additionally, the 1.8V plane should be decoupled at the RDRAM termination as shown in Section 2.6.2, "Direct Rambus* Layout Guidelines" on page 2-8.

Power MUST NOT be applied to the RDRAM termination resistors (Vterm) prior to applying power to the RDRAM Core (2.5VSBY in this design). This can be guaranteed by placing a Schottky diode between 1.8V and 2.5V as shown in Figure 6-2.

Figure 6-2. 1.8V and 2.5V Power Sequencing (Schottky Diode)
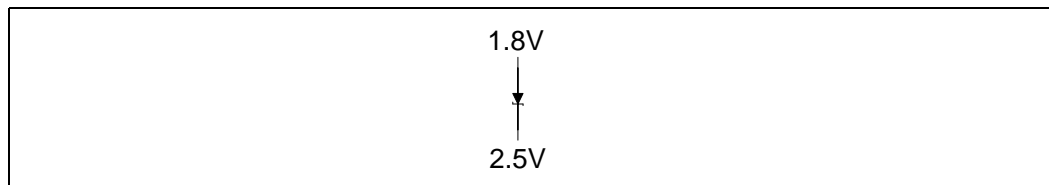
Note: This regulator is required in ALL designs.

VDDQ

The VDDQ plane is used to power the MCH AGP interface and the graphics component AGP interface. Refer to the *AGP Interface Specification Revision 2.0* (http://www.agpforum.org).

Note: This regulator is required in ALL designs (unless the design does not support 1.5V AGP, and therefore does not support 4X AGP).

For the consideration of component long term reliability, the following power sequence is required while the AGP interface of MCH is running at 3.3V. If the AGP interface is running at 1.5V, the following power sequence requirement is no longer applicable. The power sequence requirements are:

1. During the power-up sequence, the 1.8V must ramp up to 1.0V BEFORE 3.3V ramps up to 2.2V

2. During the power-down sequence, the 1.8V CAN NOT ramp below 1.0V BEFORE 3.3V ramps below 2.2V

3. The same power sequence recommendation also applies to the entrance and exit of S3 state, since MCH power is completely off during the S3 state.

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System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply. For further details on the voltage sequencing requirements, refer to the latest *Intel® 820 Chipset: 82820 Memory Controller Hub (MCH)* datasheet.

3.3VSB

The 3.3VSB plane powers the suspend well of the ICH and the PCI 3.3Vaux suspend power pins. The 3.3Vaux requirement state that during suspend, the system must deliver 375mA to each wake-enabled card and 20 mA to each non wake-enabled card. During full-power operation, the system must be able to supply 375 mA to EACH card. Therefore, the total current requirement is:

- Full-power Operation: 375 mA * number of PCI slots
- Suspend Operation: 375+20 * (number of PCI slots – 1)

In addition to the PCI 3.3V aux, the ICH suspend well power requirements must be considered as shown in Figure 6-1.

Note: This regulator is required in ALL designs.

2.5V

The 2.5V plane powers the CPU CMOS pull-up resistors. These pull-up resistors must not be powered when the system is in S3 (because the ICH core is powered down). Therefore, this power plane must be separate from the 2.5VSBY regulator. The total current requirement is approximately 180 mA. This power plane could also be implemented using a FET switch from 2.5VSBY (and controlled by SLP_S3#). If using a FET switch, the resistive drop across the FET switch should be considered.

Note: This regulator is not required in a Intel® 820 chipset based system that does not support Suspend-to-RAM (STR).

6.1.3   64/72Mbit RDRAM Excessive Power Consumption

Some 64/72Mbit RDRAM devices interpret non-broadcast, device-directed commands as broadcast commands. These commands are the SET_FAST_CLOCK, SET_RESET, and CLEAR_RESET commands. RDRAM devices consume more current during these initialization steps than during normal operation. As a result of these devices accepting device directed commands as broadcast commands, the device can not be reset/initialized serially. All devices must be reset/initialize simultaneously. This will result in excessive current draw during the initialization of memory. The amount of excessive current will depend on the number of devices and frequency used. The worst case current draw is 7.5A, in a system with 32 devices and a frequency of 400 MHz. There are two potential solutions:

1. Reduce the clock frequency during initialization (Section 6.1.3.1, "Option 1: Reduce the Clock Frequency During Initialization" on page 6-6);
2. Increase the current capability of the 2.5V voltage regulator (Section 6.1.3.2, "Option 2: Increase the Current Capability of the 2.5V Voltage Regulator" on page 6-6).

6.1.3.1 Option 1: Reduce the Clock Frequency During Initialization

Tie a single core well GPO with a default high state to both the S0 and S1 pins of the DRCG (i.e., tie S0 and S1 together and then connect to a GPO as shown in Figure 6-3). When the core power supply to the system is turned on, the DRCG enters a test mode and the output frequency will match the input REFCLK frequency. For details on this DRCG mode, refer to the latest DRCG specification. By slowing down the DRCG output clock, the power consumption from the 2.5V power supply is reduced. After the SetR/ClrR commands have been issued, the BIOS drives the GPO low to bring the DRCG back to normal operation.

Note: If a default low GPO is used, on power up, all the devices may come up in the standby state at full speed; thus, requiring more power.

Figure 6-3. Use a GPO to Reduce DRCG Frequency
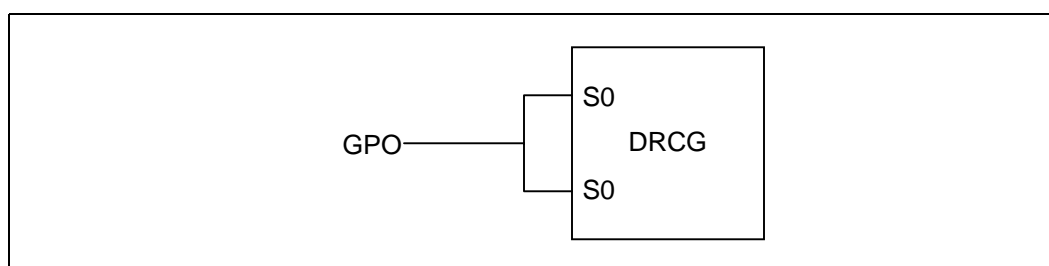
6.1.3.2 Option 2: Increase the Current Capability of the 2.5V Voltage Regulator

The second implementation option requires that the 2.5V power supply be modified to maintain the maximum amount of current required by a fully populated RDRAM channel (~7.5A).

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6.2 Power Plane Splits

Figure 6-4 shows an EXAMPLE of the power plane splits on an Intel® 820 chipset platform.

Figure 6-4. Power Plane Split Example
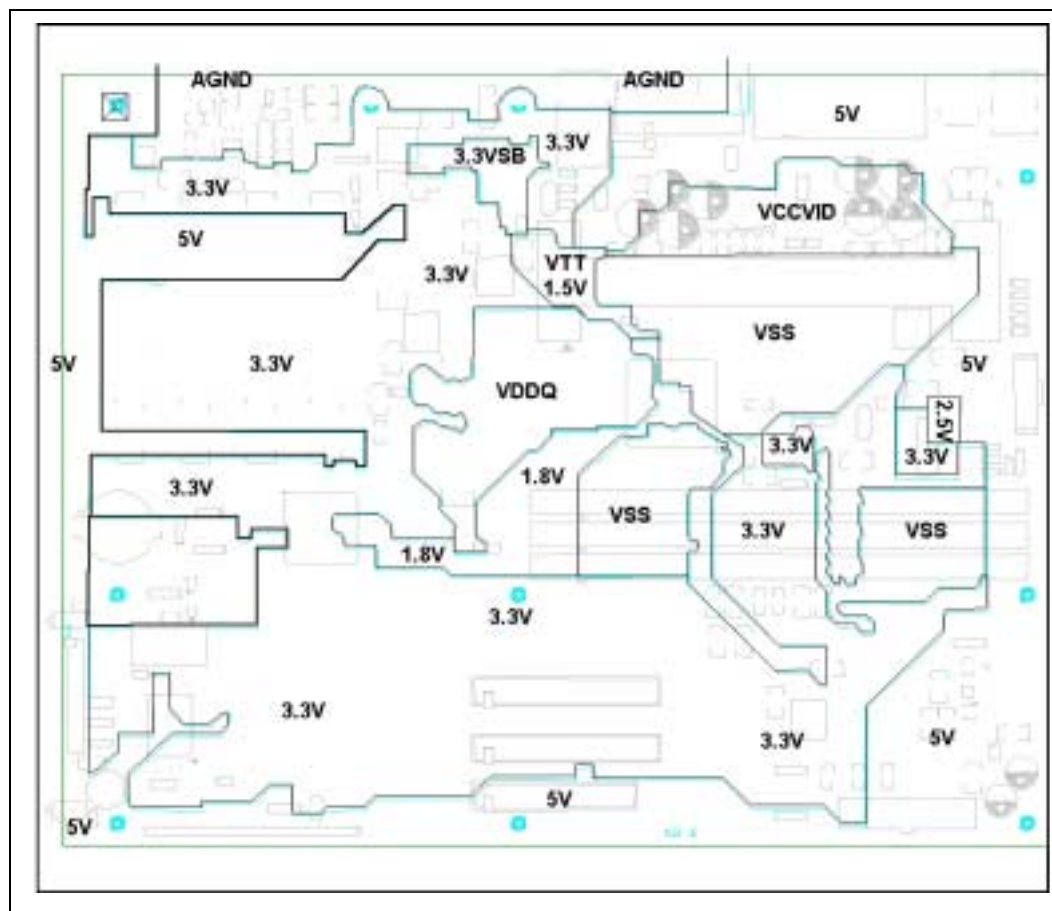
6.3 Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. Refer to the Intel® 820 Chipset Application Note: *Thermal Design Considerations,* for the thermal measurement methodology.

The thermal design power numbers for the MCH, MTH, and the ICH are listed in Table 6-1.

Table 6-1. Intel® 820 Chipset Component Thermal Design Power

Component	Thermal Design Power (133/400 MHz)
MCH	3.5W ±15%
MTH	2.5W ±15%
ICH	1.3W ±15%

6.4 Glue Chip 3 (Intel® 820 Chipset Glue Chip)

To reduce the component count and BOM cost of the Intel® 820 chipset platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The Glue Chip 3 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- PWROK signal generation
- Control circuitry for Suspend To RAM
- Power Supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for suspend to RAM
- 5V reference generation
- Flash FLUSH# / INIT# circuit
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for Audio MIDI signal
- Audio-disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test

More information regarding this component is available from the following vendors:

Table 6-2. Glue Chip 3 Vendors

Vendor Intel	Contact	Contact Information
Fujitsu Microelectronics	Customer Response Center	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 *fax:* 1-408-922-9179 *email:* fmicrc@fmi.fujitsu.com
Mitel Semiconductor	Mitel Semiconductor	http://www.mitelsemi.com

intel ®

A

Reference Board
Schematics: Uni-Processor

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intel®

Reference Design Schematics: Uni-Processor   *A*

A.1   Reference Design Feature Set

The reference schematics feature the following core feature set:

- Intel® 820 Chipset
    - — Memory Controller Hub (MCH)
    - — I/O Controller Hub (ICH)
    - — FWH Flash BIOS Interface
- Support for the Pentium III (SC242) Processor
    - — 100/133 MHz System Bus Frequency
    - — Debug Port
- IOAPIC Integrated into the ICH
- Direct RDRAM Memory Interface
    - — 266 MHz, 300 MHz, 356 MHz and 400 MHz Direct RDRAM Support
- 4 PCI Add-in Slots
    - — Via 4 REQ/GNT pairs (ICH supports 6 REQ#/GNT# pairs)
- AGP Universal Connector
    - — 3.3V - 1X,2X signaling
    - — 1.5V – 1X, 2X, 4X signaling
- 2 IDE Connectors with Ultra ATA/66 Support
- 2 USB Connectors
- ATX Power Connector
- LPC Ultra I/O
    - — Floppy Disk Controller
    - — 1 Parallel Port, 2 Serial Ports
    - — Keyboard Controller
- AC'97 Bus Connector and Audio Codec
- WfM Support
- Integrated System Management
- Integrated Power Management
    - — ACPI Rev. 1.0 Compliant
    - — APM Rev. 1.2 Compliant
- Pentium III on-board VRM 8.4 compliant regulator
- 4 Layer Design

INTEL(R) 820 CHIPSET
UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS
REV F (2 RIMM)

Note that these schematics are preliminary and are subject to change.

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The Intel 82820 chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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Block Diagram

Device Table

REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U20	74LVC06A	A, B, C	31
U14	74LVC07A	A, B, C	18, 29
U19	74LVC07A	A, C, D	18, 22
U3	74LVC08A	A, B	15, 31
U15	74LVC14a	A, B, C, D	31
U18	74LS132	B, C	29, 31
U13	82820 (ICH)		8, 9
U10	82820 (MCH)		6, 7
U5	82559		16
U8	93C46A		16
U2	AD1881		13
U11	CK133		5
U12	DRCG		5
U16	FWH		10
U4, U6	GD75232		25
U1	LM4880		14
U17	LPC47B27X		12
U9	ADM1021		3
U7	TPS2042		23

Processor Connector

HD#[63:0]

HA#[31:0]

J14

SC242

HD#0	B72	HD#0
HD#1	A73	HD#1
HD#2	B71	HD#2
HD#3	A72	HD#3
HD#4	B70	HD#4
HD#5	A71	HD#5
HD#6	B68	HD#6
HD#7	B67	HD#7
HD#8	A69	HD#8
HD#9	A68	HD#9
HD#10	A65	HD#10
HD#11	A64	HD#11
HD#12	B66	HD#12
HD#13	A63	HD#13
HD#14	A67	HD#14
HD#15	B64	HD#15
HD#16	A61	HD#16
HD#17	B63	HD#17
HD#18	B60	HD#18
HD#19	B59	HD#19
HD#20	B62	HD#20
HD#21	A60	HD#21
HD#22	B58	HD#22
HD#23	A59	HD#23
HD#24	A57	HD#24
HD#25	B56	HD#25
HD#26	B55	HD#26
HD#27	A56	HD#27
HD#28	B52	HD#28
HD#29	B54	HD#29
HD#30	A55	HD#30
HD#31	A53	HD#31
HD#32	B51	HD#32
HD#33	A51	HD#33
HD#34	B48	HD#34
HD#35	A52	HD#35
HD#36	B46	HD#36
HD#37	A49	HD#37
HD#38	B50	HD#38
HD#39	A45	HD#39
HD#40	B47	HD#40
HD#41	B42	HD#41
HD#42	A43	HD#42
HD#43	A48	HD#43
HD#44	B44	HD#44
HD#45	A44	HD#45
HD#46	A39	HD#46
HD#47	B43	HD#47
HD#48	B39	HD#48
HD#49	A40	HD#49
HD#50	B35	HD#50
HD#51	A41	HD#51
HD#52	B40	HD#52
HD#53	A36	HD#53
HD#54	B36	HD#54
HD#55	A33	HD#55
HD#56	B34	HD#56
HD#57	A37	HD#57
HD#58	B31	HD#58
HD#59	B38	HD#59
HD#60	A35	HD#60
HD#61	A32	HD#61
HD#62	B30	HD#62
HD#63	B32	HD#63

HA#3	B98	HA#3
HA#4	A100	HA#4
HA#5	A97	HA#5
HA#6	B99	HA#6
HA#7	B96	HA#7
HA#8	B95	HA#8
HA#9	A99	HA#9
HA#10	A96	HA#10
HA#11	B92	HA#11
HA#12	B94	HA#12
HA#13	A93	HA#13
HA#14	A95	HA#14
HA#15	B90	HA#15
HA#16	A92	HA#16
HA#17	B91	HA#17
HA#18	A91	HA#18
HA#19	A89	HA#19
HA#20	B86	HA#20
HA#21	B87	HA#21
HA#22	A85	HA#22
HA#23	A87	HA#23
HA#24	B83	HA#24
HA#25	B88	HA#25
HA#26	B82	HA#26
HA#27	A84	HA#27
HA#28	B84	HA#28
HA#29	B80	HA#29
HA#30	A81	HA#30
HA#31	A83	HA#31
HA#32	B79	
HA#33	A79	
HA#34	A80	
HA#35	B78	

VID0	B120	VID0
VID1	A120	VID1
VID2	A119	VID2
VID3	B119	VID3
VID4	A121	VID4

VID[4:0] 28

RS#0	B108	RS#0
RS#1	A112	RS#1
RS#2	B111	RS#2

RS#[2:0] 6

RSP# B115

REQ#0	B102	HREQ#0
REQ#1	B103	HREQ#1
REQ#2	A107	HREQ#2
REQ#3	A108	HREQ#3
REQ#4	B104	HREQ#4

HREQ#[4:0] 6

RP# B114

THRMDN B15 THRMDN_R R122 0K THRMDN
THRMDP B14 THRMDP_R R121 0K THRMDP

RESERVED3 B12
RESERVED2 A116
RESERVED1 A88
RESERVED0 A47

VCC3_3   VCC3_3

U9
ADM1021

3	DXP	
4	DXN	
		STBY#	15
		ADD0	10
		ADD1	6
1	NC1	
5	NC5	
9	NC9	
13	NC13	
16	NC16	
		SMBCLK	14	SMBCLK_CORE	9,11,32
		SMBDATA	12	SMBDATA_CORE	9,11,32
		ALERT#	11	THRM#	9

VCC2 2

GND8 8
GND7 7

THRMDP and THRMDN signals must be disconnected from onboard thermal sensor
during SECC2 thermal testing of the processor. Please see the "Pentium(R) II processor Single Edge
Contact Cartridge 2 Thermal Validation" document for further details.
Place R121,R122 very close to processor.

Processor Connector

ITP

VCC3_3 VCC2_5 VTT1_5   VCC2_5

R19 240
R157 1K
R167 1K
R171 1K
R145 330
R139 330
R142 150

ITP_PU_R

4,6 CPURST# R149 CPURST#_R
31 DBRESET# 240

J15

TMS_R   TCK_R

R152 47
R140 680
R138 240
R163 47

5   ITPCLK

TDI
TDO
TRST#
ITPREQ#   4
ITPRDY#_R
ITPPRDY#   4

R163 and R152 should be placed within 1" of ITP connector.

CPU Fan Header

VCC12

C80 0.1UF

JP16
1
2
3

VTT1_5   VCCVID   VCC5   VCC3_3

J14 A1 A3 B5 B9 B13 B17 B25 B29 B33 B37 B45 B49 B53 B57 B65 B69 B73 B77 B85 B89 B93 B97 B105 B109 B113 B117 B121

VTT1 VTT2 VTT3 VTT4 VCCP1 VCCP2 VCCP3 VCCP4 VCCP5 VCCP6 VCCP7 VCCP8 VCCP9 VCCP10 VCCP11 VCCP12 VCCP13 VCCP14 VCCP15 VCCP16 VCCP17 VCCP18 VCCP19 VCC5 VCC3_3 VCC3_1 VCC3_2 VCC3_3

A25 DEP#0
A27 DEP#1
B26 DEP#2
A28 DEP#3
B27 DEP#4
A29 DEP#5
A31 DEP#6
B28 DEP#7

B19 BP2#
A21 BP3#
A23 BPM0#
B24 BPM1#
A24 BINIT#

8,32 PICD0 A19 PICD0
8,32 PICD1 B22 PICD1
     PICCLK B18 PICCLK
5

B101 SLOTOCC#
A9 TDI
A11 TDO
B11 TRST#
B7 TCK
B10 TMS

EMI1 B61 EMI_1
EMI2 B100 EMI_2
EMI3 B81 EMI_3
EMI4 B1 EMI_4
EMI5 B41 EMI_5

R101 0K
R104 0K
R103 0K
R93 0K
R100 0K

5   CPUHCLK A75 BCLK
31   PWRGOOD A12 PWRGOOD
4,6 CPURST# B74 RESET#

SC242

AP0#   A117
AP1#   B116
BNR#   A101 BNR#   6
BPRI# A103 BPRI#   6
TRDY# A104 HTRDY#   6
DEFER# A105 DEFER#   6
LOCK# B106 HLOCK#   6
DRDY# B107 DRDY#   6
HITM# A109 HITM#   6
HIT#   B110 HIT#   6
DBSY# A111 DBSY#   6
HADS# A115 HADS#   6

PREQ# A20 ITPREQ#   4
PRDY# B23 ITPPRDY#   4
BREQ0# A76 BREQ#0   32
BREQ1# B75
RES4   B76
TESTHI A13 TESTHI   32

BSEL0 B21 VRM_PWRGD   28,31
BSEL1 A14 SEL133/100# 5,7

FLUSH# B2 FLUSH#   32

THMTRP# A15

A20M#   A5 A20M#   8,32
STPCLK# B6 STPCLK#   8,32
SLP#   B8 SLP#   8,32
SMI#   B3 SMI#   8,32
LINT0   A17 LINT0   8,32
LINT1   B16 LINT1   8,32
INIT#   B4 HINIT#   8,32
FERR#   A7 FERR#   8,10,32
IGNNE# A8 IGNNE#   8,32
IERR#   A4
BERR#   A77
AERR#   B118
RES0   A16
RES1   B20
RES2   B112
RES3   A113

GND0 GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25 GND26 GND27 GND28 GND29

A2 A6 A10 A18 A22 A26 A30 A34 A38 A42 A46 A50 A54 A58 A62 A66 A70 A74 A78 A82 A86 A90 A94 A98 A102 A106 A110 A114 A118

Clock Synthesizer

VCC3_3

Provide at least one 0.1uF decoupling cap per power pin.

VCC2_5

L20 FBHS01L
L21 FBHS01L

VCC_3_3_CK133_FB
VCC2_5_CK133_FB

C207 C215 C223 C186 C198 C206 C214 C170
0.1UF 0.1UF 0.1UF 0.1UF 0.1UF 0.1UF 0.1UF 10UF

C180 C190 C192 C199 C171
0.1UF 0.1UF 0.1UF 0.1UF 10UF

U11 CK133

VCC3_3

Y3 XTAL
14.318MHZ
C185 10PF
C189 10PF
CK133_XIN
CK133_XOUT

VCC3_3
R224 220

R206 10K
R203 10K
R202 10K
R197 10K
R196 10K
R192 10K

VDD3V_1 VDD3V_2 VDD3V_3 VDD3V_5 VDD3V_6 VDD3V_7
VDD25V_1 VDD25V_2 VDD25V_3 VDD25V_4

XTAL_IN
XTAL_OUT

2.5V

APIC0 53 PICCLK_R R155 22 PICCLK 4
APIC1 54 APICCLK_R R156 22 APICCLK 8
APIC2 55
CPU_DIV2_1 50 CPU_DIV2_1_R R148 22 CPU_DIV2
CPU_DIV2_2 49 CPU_DIV2_2_R
CPUCLK0 41 ITPCLK_R R188 22 ITPCLK 4
CPUCLK1 42 CPUHCLK_R R189 22 MCHCLK 6
CPUCLK2 45 R184 22 CPUHCLK 4
CPUCLK3 46 CPUCLK3_R

Keep stubs on unused outputs as short as possible.
Tie CPUCLK and MCHCLK outputs together.

R151 30

SEL133/100#
PCISTOP#
CPUSTOP#
CK133_PWRDWN#
SPREAD#
SEL1
SEL0

28 SEL133/100#
37 PCISTOP#
36 CPUSTOP#
35 PWRDWN#
34 SPREAD#
33 SEL1
32 SEL0

4,7 SEL133/100#

PCICLK_F 8 ICHPCLK_R R165 33 ICHPCLK 8
PCICLK1 9 PCLK1_R R164 33 PCLK1 20
PCICLK2 11 PCLK2_R R169 33 PCLK2 20
PCICLK3 12 PCLK3_R R183 33 PCLK3 21
PCICLK4 14 PCLK4_R R186 33 PCLK4 21
PCICLK5 15 PCLK5_R R187 33 PCLK5 21
PCICLK6 17 FWHPCLK_R R191 33 FWHPCLK 16
PCICLK7 18 SIO_PCLK7_R R194 33 SIO_PCLK7 10
3V66_0 21 MCH_CLK66_R33 R201 33 AGPCLK_CONN 19
3V66_1 22 MCH_CLK66_R R195 33 MCH_CLK66 7
3V66_2 25 ICH_CLK66_R R210 33 ICH_CLK66 9
3V66_3 26 TEST_CLK66_R R211 33 TEST_CLK6637
48MHZ 30 IHC_48MHZ_R R221 22 ICH_48MHZ 9
REF0 1 IHC_14MHZ_R R147 22 ICH_14MHZ 9
REF1 3 SIO_14MHZ_R R150 22 SIO_14MHZ 12

R166 30
R170 30

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12

JP17 JP15 JP14

JP19
JP19 is for debug only.

No stuff R106 for debug.
VCC3_3
VCC1_8
R220 33

VCC3_3
VCC2_5 VCC1_8

VDDIR pin on DRCG should be decoupled at the component with a 0.1uF cap.
CLKTM and CLKTM# RC network must use 5% or better tolerance components.

VCC3_3
L22 FBHS01L
VCC3_3_DRCG_FB

C364 82PF C208 0.1UF C196 0.1UF C204 0.1UF C220 0.1UF C209 10UF

Place C364 next to VDDP.

U12 DRCG+

VDDIR VDDIPD VDDO1 VDDO2 VDDP VDDC

MULT0_GPIO
R219 10K R204 10K R199 10K

VCC3_3

JP13 is for debug only. JP13

DRCG_PWRDWN# 12 REFCLK
11 STOPB#
15 MULT0
14 MULT1
24 S0
23 S1
13 GND
6 PCLKM
7 SYNCLKN
19 NC

DRCG_CTRL

CLK 20
CLKB# 18

DRCG_CLK R182 39-1% CLKTM 11
R185 51-1% R200 51-1%
C363 4PF
DRCG_CLKB R205 39-1% CLKTM# 11

No stuff C363

C205 0.1UF

R161 10K R217 10K

STOPB#
MULT0
MULT1
HCLKOUT 6
RCLKOUT 7

GND01 GND02 GNDP GNDC GNDI

JP11

9,12 MULT1_GPIO JP18

No stuff R161, JP11.

HOST BUS/RAMBUS	JP13	JP18
100/300	2-3	OUT
100/400	OUT	OUT
133/400	2-3	OUT
GPO CNTRL*	1-2	1-2

Sprd Spect	JP14
Enabled*	IN
Disabled	OUT

SEL133/100#	JP15	JP17	Function
0	IN	IN	All outputs Tri-State
0	IN	OUT	Reserved
0	OUT	IN	Active 100MHz, 48MHz PLL inactive
0	OUT	OUT	Active 100MHz, 48MHz PLL active
1	IN	IN	Test Mode
1	IN	OUT	Reserved
1	OUT	IN	Active 133MHz,48MHz PLL inactive
1	OUT	OUT	Active 133MHz,48MHz PLL active*

All jumpers may not be required, but are included for test purposes.

MCH

HUBREF 8,37

CONN_AGPREF

RAMREF_R

R168 100-1%

RAMREF 6,11

C194 19

C155

0.01UF

0.1UF

U10
MCH_096

C191 0.1UF

C203 0.1UF

GTLREF2 6
GTLREF1 6

VTT1_5

VTT1_5

R131 75-1%

R143 75-1%

GTLREF2

GTLREF1

R130 150-1%

R144 150-1%

C158 0.001UF

C183 0.001UF

HD#[63:0] 3

HD#0	R2	HD#0
HD#1	R1	HD#1
HD#2	R4	HD#2
HD#3	P5	HD#3
HD#4	T1	HD#4
HD#5	R5	HD#5
HD#6	V1	HD#6
HD#7	Y2	HD#7
HD#8	W1	HD#8
HD#9	U1	HD#9
HD#10	T2	HD#10
HD#11	Y3	HD#11
HD#12	W2	HD#12
HD#13	U3	HD#13
HD#14	Y1	HD#14
HD#15	U2	HD#15
HD#16	W4	HD#16
HD#17	W3	HD#17
HD#18	V4	HD#18
HD#19	U4	HD#19
HD#20	T3	HD#20
HD#21	Y4	HD#21
HD#22	Y5	HD#22
HD#23	T4	HD#23
HD#24	V5	HD#24
HD#25	T5	HD#25
HD#26	Y6	HD#26
HD#27	W5	HD#27
HD#28	U6	HD#28
HD#29	V6	HD#29
HD#30	W6	HD#30
HD#31	T6	HD#31
HD#32	W7	HD#32
HD#33	U7	HD#33
HD#34	Y8	HD#34
HD#35	Y7	HD#35
HD#36	T8	HD#36
HD#37	W8	HD#37
HD#38	T7	HD#38
HD#39	W9	HD#39
HD#40	U8	HD#40
HD#41	W10	HD#41
HD#42	Y10	HD#42
HD#43	V8	HD#43
HD#44	U9	HD#44
HD#45	Y9	HD#45
HD#46	W11	HD#46
HD#47	T9	HD#47
HD#48	Y11	HD#48
HD#49	T10	HD#49
HD#50	T12	HD#50
HD#51	U10	HD#51
HD#52	V10	HD#52
HD#53	W12	HD#53
HD#54	T11	HD#54
HD#55	U13	HD#55
HD#56	Y13	HD#56
HD#57	Y12	HD#57
HD#58	W14	HD#58
HD#59	U11	HD#59
HD#60	U12	HD#60
HD#61	Y14	HD#61
HD#62	V14	HD#62
HD#63	W13	HD#63

HOST

HOST

HUBREF E20
AGPREF U14
RAMREFA E11
RAMREFB E10
GTLREFA C3
GTLREFB V12

VCC1_8:D4,E6,F6,G6,E7,R6,R7,E8,E9,D10,D11,E12
VCC1_8:E13,E14,F14,T14,E15,P15,B17,C17,C19
VDDQ:F15,R15,J17,L17,N17,T17
GND:A1,A3,G3,J3,L3,N3,R3,V3,B4,D5,L5,U5,B6,D6,D7,V7,B8,D8
GND:D9,J9,K9,L9,M9,V9,B10,J10,K10,L10,M10,C11,J11,K11,L11
GND:M11,V11,C12,D12,J12,K12,L12,M12,B13,D13,V13,T13,D14
GND:B15,D15,B16,D16,E16,F16,A17,E18,V18,A19,H19,K19,M19
GND:P19,T19,D20

HA#[31:0] 3

HA#3	J1	HA#3
HA#4	H3	HA#4
HA#5	H4	HA#5
HA#6	G5	HA#6
HA#7	K2	HA#7
HA#8	H5	HA#8
HA#9	H2	HA#9
HA#10	J4	HA#10
HA#11	L1	HA#11
HA#12	J5	HA#12
HA#13	K1	HA#13
HA#14	J2	HA#14
HA#15	K5	HA#15
HA#16	K3	HA#16
HA#17	L4	HA#17
HA#18	K4	HA#18
HA#19	L2	HA#19
HA#20	N2	HA#20
HA#21	M3	HA#21
HA#22	M2	HA#22
HA#23	M1	HA#23
HA#24	N5	HA#24
HA#25	M4	HA#25
HA#26	P1	HA#26
HA#27	N1	HA#27
HA#28	P2	HA#28
HA#29	P3	HA#29
HA#30	N4	HA#30
HA#31	M5	HA#31

VDDQ

C187 470PF

MCH_AGPREF_CV

R154 1K-1%

R160 80.6-1%

MCH_AGPREF

19

R159 1K-1%

R153 80.6-1%

C182 470PF

MCH_AGPREF_CG

Place MCH_AGPREF circuit near the MCH.

CPURST#	P4	CPURST# 4
ADS#	D2	HADS# 4
BNR#	F5	BNR# 4
BPRI#	G1	BPRI# 4
DBSY#	D1	DBSY# 4
DEFER#	F2	DEFER# 4
DRDY#	F1	DRDY# 4
HIT#	D3	HIT# 4
HITM#	E1	HITM# 4
HLOCK#	F3	HLOCK# 4
HTRDY#	F4	HTRDY# 4

RS#[2:0] 3

RS#0	E5	RS#0
RS#1	C1	RS#1
RS#2	E2	RS#2

HREQ#[4:0] 3

HREQ#0	H1	HREQ#0
HREQ#1	G4	HREQ#1
HREQ#2	E4	HREQ#2
HREQ#3	E3	HREQ#3
HREQ#4	G2	HREQ#4

VCC1_8

R180 40.2-1%

HCLKIN V2 MCHCLK 5

RSTIN# F20 PCIRST# 8,10,11,12,16,19,20,21,22

HLCOMP A18 MCH_HLCOMP

TEST/GRCOMP T15 GRCOMP

R129 40.2-1%

Place R129 and R180 less than 0.5" from MCH using 10 mil trace.

VCC1_8

R190 162-1%

RAMREF 6,11

R181 562-1%

MCH

U10
MCH_096

GAD[31:0]

19

GAD0	F17	G_AD0
GAD1	G18	G_AD1
GAD2	G17	G_AD2
GAD3	G19	G_AD3
GAD4	G16	G_AD4
GAD5	G20	G_AD5
GAD6	H17	G_AD6
GAD7	H18	G_AD7
GAD8	J20	G_AD8
GAD9	J16	G_AD9
GAD10	K17	G_AD10
GAD11	K18	G_AD11
GAD12	J18	G_AD12
GAD13	L19	G_AD13
GAD14	K20	G_AD14
GAD15	L18	G_AD15
GAD16	M17	G_AD16
GAD17	P18	G_AD17
GAD18	M16	G_AD18
GAD19	P17	G_AD19
GAD20	N16	G_AD20
GAD21	P20	G_AD21
GAD22	P16	G_AD22
GAD23	R20	G_AD23
GAD24	T20	G_AD24
GAD25	R17	G_AD25
GAD26	U17	G_AD26
GAD27	T16	G_AD27
GAD28	U18	G_AD28
GAD29	T18	G_AD29
GAD30	U20	G_AD30
GAD31	U19	G_AD31

AGP

GC/BE#[3:0]

19

GC/BE#0	H16	G_C/BE#0
GC/BE#1	L20	G_C/BE#1
GC/BE#2	N18	G_C/BE#2
GC/BE#3	R16	G_C/BE#3

19,32	GFRAME#	L16	G_FRAME#
19,32	GDEVSEL#	N19	G_DEVSEL#
19,32	GIRDY#	N20	G_IRDY#
19,32	GTRDY#	M20	G_TRDY#
19,32	GSTOP#	M18	G_STOP#
19,32	GPAR	K16	G_PAR
19,32	GREQ#	U15	G_REQ#
19,32	GGNT#	Y16	G_GNT#
19,32	PIPE#	W16	PIPE#

| 5 | MCH_CLK66 | W18 | CLK66 |

| 19,32 | RBF# | V16 | RBF# |
| 19,32 | WBF# | V15 | WBF# |

ST[2:0]

ST0	W15	ST0
ST1	Y15	ST1
19	ST2	Y17	ST2

19,32	ADSTB0	J19	AD_STB0
19,32	ADSTB#0	H20	AD_STB#0
19,32	ADSTB1	R18	AD_STB1
19,32	ADSTB#1	R19	AD_STB#1
19,32	SBSTB	Y20	SB_STB
19,32	SBSTB#	Y19	SB_STB#

AGP

VCC1_8

C361 0.1UF
C359 0.1UF
C360 0.1UF
C362 0.1UF

No stuff. For test only.

HUB

HL0	F19	HL0
HL1	F18	HL1
HL2	E17	HL2
HL3	E19	HL3
HL4	B20	HL4
HL5	B19	HL5
HL6	B18	HL6
HL7	A20	HL7
HL8	D17	HL8
HL9	C18	HL9
HL10	D18	HL10

HL[10:0]
8

| HL_STB | D19 | HL_STB | 8,37 |
| HL_STB# | C20 | HL_STB# | 8,37 |

7,8,37   HL10   R209   SEL133/100#   4,5
8.2K

R227 8.2K

VCC3_3SBY
R248 4.7K

| RCLKOUT | B1 | RCLKOUT | 5 |
| HCLKOUT | A2 | HCLKOUT | 5 |

VCC3_3SBY

DQA0	A13	LDQA0
DQA1	C13	LDQA1
DQA2	A14	LDQA2
DQA3	C14	LDQA3
DQA4	B14	LDQA4
DQA5	C15	LDQA5
DQA6	A15	LDQA6
DQA7	C16	LDQA7
DQA8	A16	LDQA8

LDQA[8:0]   11

U14   VCC
9,16,29,31   PWROK   13   12   PWROK_CTRL   7
SN74LVC07A   GND

DQB0	C7	LDQB0
DQB1	B7	LDQB1
DQB2	C6	LDQB2
DQB3	A6	LDQB3
DQB4	C5	LDQB4
DQB5	A5	LDQB5
DQB6	B5	LDQB6
DQB7	A4	LDQB7
DQB8	C4	LDQB8

LDQB[8:0]   11

MEMORY

LSCK and LCMD must neck down to 5 mils for 175 mils at Q10 and Q9 attach points.
Place Q10 and Q9 as close as possible to MCH.

VCC5SBY

RQ0	A7	LCOL0
RQ1	C8	LCOL1
RQ2	A8	LCOL2
RQ3	C9	LCOL3
RQ4	B9	LCOL4

LCOL[4:0]   11

R346   4.7K

RQ5	A9	LROW0
RQ6	A10	LROW1
RQ7	C10	LROW2

LROW[2:0]   11

LSCK   11

CTM	B11	LCLKTM	11
CTM#	A11	LCLKTM#	11
CFM	A12	LCLKFM	11
CFM#	B12	LCLKFM#	11

MMBT3904LT1   Q10
C   3   1   B
E   2

SCK_CTRL

7   PWROK_CTRL   B   Q14   MMBT3904LT1

CMD	B3		LCMD 11
SCK	B2		
SIO	C2	LSIO	11

Q9   MMBT3904LT1

SBA0	W20	SBA0
SBA1	V17	SBA1
SBA2	Y18	SBA2
SBA3	W17	SBA3
SBA4	V20	SBA4
SBA5	W19	SBA5
SBA6	V19	SBA6
SBA7	U16	SBA7

SBA[7:0]   19

ICH

U13
ICH_096

ICH_A

AD[31:0]   16,20,21

AD0	G2	AD0
AD1	G4	AD1
AD2	F2	AD2
AD3	F3	AD3
AD4	F4	AD4
AD5	F5	AD5
AD6	E1	AD6
AD7	E2	AD7
AD8	D1	AD8
AD9	D3	AD9
AD10	E4	AD10
AD11	C2	AD11
AD12	C1	AD12
AD13	B1	AD13'
AD14	D4	AD14
AD15	C3	AD15
AD16	A4	AD16
AD17	B4	AD17
AD18	C5	AD18
AD19	C6	AD19
AD20	B5	AD20
AD21	E7	AD21
AD22	A6	AD22
AD23	B6	AD23
AD24	D7	AD24
AD25	B8	AD25
AD26	A7	AD26
AD27	A8	AD27
AD28	B7	AD28
AD29	C9	AD29
AD30	D8	AD30
AD31	C7	AD31

PCI

C_BE#[3:0]   16,20,21

C_BE#0	D2	CBE0#
C_BE#1	B2	CBE1#
C_BE#2	A3	CBE2#
C_BE#3	D6	CBE3#

16,20,21,32 DEVSEL# D9 DEVSEL#
16,20,21,32 FRAME# B3 FRAME#
16,20,21,32 IRDY# A2 IRDY#
16,20,21,32 TRDY# C4 TRDY#
16,20,21,32 STOP# D5 STOP#
16,20,21 PAR A9 PAR
6,10,11,12,16,19,20,21,22 PCIRST# J5 PCIRST#
20,21,32 PLOCK# B9 PLOCK#
16,20,21,32 SERR# A1 SERR#
16,20,21,32 PERR# E9 PERR#/GPIO7
16,19,20,21 PCI_PME# K1 PME#
21,32 REQ#A N6 GPIO0/REQ#A
21,32 GNT#A P5 GPIO16/GNT#A

5 ICHPCLK C14 PCICLK

VCC1_8:G13,H14,K14,G15,L15,H16,J16
VCC3_3:C11,E13,N13,R13,M14,D16,T16
VCC3_3:E3,A5,E5,G5,N5,E6,P6,T7,C8,U10
GND:R2,G3,H8,J8,K8,H9,J9,K9,H10,J10,K10,G14,K15

CPU

A20M#	F13	A20M#	4,32
CPUSLP#	E12	SLP#	4,32
FERR#	F15	FERR#	4,32
IGNNE#	B17	IGNNE#	4,32
INIT#	E15	HINIT#	4,10,32
INTR	E14	LINT0	4,32
NMI	B16	LINT1	4,32
SMI#	F14	SMI#	4,32
STPCLK#	A17	STPCLK#	4,32
RCIN#	A15	KBRST#	12,32
A20GATE	B15	A20GATE	12,32

HUB

HL[10:0]

HL0	D17	HL0
HL1	E17	HL1
HL2	F17	HL2
HL3	G16	HL3
HL4	J15	HL4
HL5	K16	HL5
HL6	K17	HL6
HL7	L17	HL7
HL8	H15	HL8
HL9	J17	HL9
HL10	J14	HL10
HL11	F16	HL11_TP
HL_STB	G17	HL_STB	7,37
HL_STB#	H17	HL_STB#	7,37
HLCOMP	M17	ICH_HLCOMP
HUBREF	J13

7

TP1

Place R239 less than 0.5" from the ICH using a 10 mil trace.

VCC1_8
R239
40.2-1%

HUBREF 6,8,37

C237
0.01UF

Place C237 close to ICH.

IRQ

PIRQA#	D10	PIRQ#A	16,19,20,21,32
PIRQB#	A10	PIRQ#B	19,20,21,32
PIRQC#	B10	PIRQ#C	20,21,32
PIRQD#	C10	PIRQ#D	20,21,32
IRQ14	P11	IRQ14	22,32
IRQ15	N14	IRQ15	22,32
APICCLK	C16	APICCLK	5
APICD0	E16	PICD0	4,32
APICD1	C17	PICD1	4,32
SERIRQ	R4	SERIRQ	12,21,32

PCI

REQ#0	A14	PREQ#0	20,32
REQ#1	B13	PREQ#1	20,32
REQ#2	B12	PREQ#2	21,32
REQ#3	D12	PREQ#3	16,32
REQ#4	B11	PREQ#4	32
GPIO1/REQ#B/REQ#5	P4	PREQ#5	21,32
GNT#0	A13	PGNT#0	20,32
GNT#1	C13	PGNT#1	20,32
GNT#2	A12	PGNT#2	21,32
GNT#3	C12	PGNT#3	16,32
GNT#4	A11	PGNT#4	32
GPIO17/GNT#B/GNT#5	R5	PGNT#5	21,32

VCC1_8
R225
301-1%

HUBREF 6,8,37
R226
301-1%
C218
0.1UF

Place HUBREF circuit between MCH and ICH

HUBREF voltage = 0.9V +/- 2%

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
ICH

REV: 1.01

intel® PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY:
PROJECT:
LAST REVISED: 11-24-1999_11:14
SHEET: 8 OF 36

ICH

U13
ICH_096
ICH_B

VCC3_3SBY
VCC_RTC_JP
VCC3_3SBY
VCC5_REF
VCC3_3
VCC5

CR4 BAT17
R245 1K
C246 1UF
VBAT_CR
RTC_RST_JP
JP20 1
3 2
RTC_CLR
R241 8.2K
R233 1K
C247 2.2UF
R250 1K
VBAT_RC
C249 0.047UF
VBAT_RTC
CR5 BAT17
BAT1
Use CR2032 battery.

R247 10M
R249 10M
Y4 XTAL 32.768KHZ
C250 12PF
C251 12PF

Strap	JP26
No WD Reboot	IN
Reboot on WD*	OUT

Strap	JP5
Safe Mode	IN
ICH strap*	OUT

CMOS	JP20
Normal*	1-2
Clear	2-3

VCCRTC G1
VCCSUS N1
VCCSUS1 L1
VCCSREF C15
C234 1UF
C233 0.1UF
CR3 BAT17
R220 1K

R231 8.2K THRM# 3 — D14 THRM#
SLP_S3# 29,31 — K3 GPIO24/SLP_S3#
SLP_S5# 30 — K2 GPIO25/SLP_S5#
PWROK 7,16,29,31 — J3 PWROK
PWRBTN# 18 — M2 PWRBTN#
ICH_RI# 25 — L3 RI#
RSMRST# — F1 RSMRESET#
MULT1_GPIO 17,31 — L4 GPIO25/SUSSTAT#
GPIO26_FPLED 5,12 — K4 SUSCLK/GPIO26

SMBDATA_CORE 3,11,32 — J1 SMBDATA
SMBCLK_CORE 3,11,32 — J2 SMBCLK
SMB_ALERT 32 — M1 GPIO11/SMBALERT#

LPC_SMI# 12 — E11 GPIO6
LPC_PME# 12 — D11 GPIO5
INTRUDER# R232 8.2K — J4 GPIO10/INTRUDER#
RTCRST# — H1 RTCRST#
VBIAS — H2 VBIAS
RTCX1 — H3 RTCX1
RTCX2 — H4 RTCX2

SYSTEM

ICH_CLK66 5 — A16 CLK66
ICH_14MHZ 5 — U6 CLK14
ICH_48MHZ 5 — U6 CLK48

AC_RST# 15 — T1 AC_RST#
AC_SYNC 13,15 — T3 AC_SYNC
AC_BITCLK 13,15 — R3 AC_BIT_CLK
AC_SDATAOUT 9,13,15 — T2 AC_SDOUT
AC_SDATAIN0 13,15 — U1 ACSDIN0
AC_SDATAIN1 15 — P3 GPIO9/AC_SDIN1
SPKR 9,18 — U3 SPKR

AC97

GPIO12 R212 8.2K — N4 GPIO12
GPIO13 R215 8.2K — L2 GPIO13
GPIO21 — B14 GPIO21
MULT0_GPIO 5 — D13 GPIO22
GPIO23_FPLED 18 — D15 GPIO23
ALERTCLK_SBY 16,32 — M5 GPIO27/ALERT_CLK
ALERTDATA_SBY 16,32 — L5 GPIO28/ALERT_DATA

GPIO

PCI_TEST 21 R98 0K
DRCG_CTRL 5 R162 0K
No stuff R98.

LAD0/FWH0 10,12 — R6 LAD0/FWH0
LAD1/FWH1 10,12 — U5 LAD1/FWH1
LAD2/FWH2 10,12 — T5 LAD2/FWH2
LAD3/FWH3 10,12 — T4 LAD3/FWH3
LDRQ#0 12 — T6 LDRQ0#
GPIO8 R238 8.2K — N3 GPIO8/LDRQ1#
LFRAME#/FWH4 10,12 — U4 LFRAME#/FWH4

LPC

USBP1P 23 — R1 USBP1+
USBP1N 23 — P2 USBP1-
USBP0P 23 — P1 USBP0+
USBP0N 23 — N2 USBP0-
OC#1 23 — M4 OC1#
OC#0 23 — M3 OC0#

USB

PDCS1# N12 PDCS#1 → 22
SDCS1# L14 SDCS#1 → 22
PDCS3# U13 PDCS#3 → 22
SDCS3# L16 SDCS#3 → 22
PDA0 R12 PDA0
PDA1 T12 PDA1
PDA2 P12 PDA2 PDA[2:0] → 22
SDA0 M16 SDA0
SDA1 M15 SDA1
SDA2 L13 SDA2 SDA[2:0] → 22
PDDREQ U11 PDREQ → 22
SDDREQ P17 SDREQ → 22
PDDACK# U12 PDDACK# → 22
SDDACK# M13 SDDACK# → 22
PDIOR# R11 PDIOR# → 22
SDIOR# N16 SDIOR# → 22
PDIOW# T11 PDIOW# → 22
SDIOW# N15 SDIOW# → 22
PIORDY N11 PIORDY → 22
SIORDY N17 SIORDY → 22

PDD[15:0]
PDD0 R10 PDD0
PDD1 N9 PDD1
PDD2 R9 PDD2
PDD3 U9 PDD3
PDD4 R8 PDD4
PDD5 U8 PDD5
PDD6 R7 PDD6
PDD7 U7 PDD7
PDD8 P7 PDD8
PDD9 N7 PDD9
PDD10 T8 PDD10
PDD11 P8 PDD11
PDD12 T9 PDD12
PDD13 P9 PDD13
PDD14 T10 PDD14
PDD15 P10 PDD15 → 22

IDE

SDD[15:0]
SDD0 P15 SDD0
SDD1 R16 SDD1
SDD2 T17 SDD2
SDD3 U16 SDD3
SDD4 U15 SDD4
SDD5 R14 SDD5
SDD6 P13 SDD6
SDD7 T13 SDD7
SDD8 U14 SDD8
SDD9 T14 SDD9
SDD10 P14 SDD10
SDD11 T15 SDD11
SDD12 U17 SDD12
SDD13 R15 SDD13
SDD14 R17 SDD14
SDD15 P16 SDD15 → 22

SPKR 9,18
JP26
SPKR_STRAP
VCC3_3
R90 2.7K
R341 2.7K
AC_SDOUT_STRAP
JP5
AC_SDATAOUT 9,13,15

R254 8.2K
R317 8.2K

FWH

Do not tie Vpp to 12V. Vpp should be tied to VCC3_3 for onboard programming.

VCC3_3

C300 0.1UF   C305 0.1UF

VCC3_3

VCC3_3

C301 0.1UF   C298 0.1UF   C297 0.1UF   C308 0.1UF

U16

Pin	Name		Name	Pin	
1	NC1		GNDA	40	
2	IC	FWH_IC	VCCA	39	
3	NC3		FWH4	38	LFRAME#/FWH4 → 9,12
4	NC4		INIT#	37	HINIT# → 4,8,32
5	NC5		RFU36	36	
6	NC6		RFU35	35	
7	FGPI4	FGPI4	RFU34	34	
8	NC8		RFU33	33	
9	CLK	FWHPCLK	RFU32	32	
10	VCC10		VCC31	31	
11	VPP	VPP_R	GND30	30	
12	RST#	PCIRST#	GND29	29	
13	NC13		FWH3	28	LAD3/FWH3 → 9,12
14	NC14		FWH2	27	LAD2/FWH2 → 9,12
15	FGPI3		FWH1	26	LAD1/FWH1 → 9,12
16	FGPI2		FWH0	25	LAD0/FWH0 → 9,12
17	FGPI1		ID0	24	
18	FGPI0		ID1	23	
19	WP#		ID2	22	
20	TBL#		ID3	21	

FWH

R296 8.2K
R298 8.2K
R299 0K   6,8,11,12,16,19,20,21,22
R300 8.2K
R303 8.2K

22 S66DETECT
22 P66DETECT

R305 0K
R306 0K

For drive side detection, stuff R304,R307. No stuff R305,R306.
For host side detection, stuff R304,R305,R306,R307.

R304 15K
R307 15K

VCC3_3

VCC3_3

R308 4.7K   WPROT

JP21

Top Block Lock

TBLK_LCK

R310 4.7K

FWH	JP21
OUT	Locked
IN	Unlocked*

2 RIMM Sockets

As shown, RIMMs are 184-pin connectors.

MR2OUT

R500
8.2K

J16 RIMM

LDQA0	A10	LDQA0	
LDQA1	B8	LDQA1	
LDQA2	A8	LDQA2	
LDQA3	B6	LDQA3	
LDQA4	A6	LDQA4	
LDQA5	B4	LDQA5	
LDQA6	A4	LDQA6	
LDQA7	B2	LDQA7	
LDQA8	A2	LDQA8	
LDQB0	B24	LDQB0	
LDQB1	A26	LDQB1	
LDQB2	B26	LDQB2	
LDQB3	A28	LDQB3	
LDQB4	B28	LDQB4	
LDQB5	A30	LDQB5	
LDQB6	B30	LDQB6	
LDQB7	A32	LDQB7	
LDQB8	B32	LDQB8	

LDQA[8:0] 7
LDQB[8:0] 7

LROW[2:0] 7
LROW2 B16 LROW2
LROW1 A18 LROW1
LROW0 B18 LROW0
LCOL[4:0] 7
LCOL4 A20 LCOL4
LCOL3 B20 LCOL3
LCOL2 A22 LCOL2
LCOL1 B22 LCOL1
LCOL0 A24 LCOL0

LCLKFM B10 LCFM 7
LCLKFM# B12 LCFM# 7
LCLKTM A14 LCTM 7
LCLKTM# A12 LCTM# 7

LCMD B34 LCMD 7
LSCK A34 LSCK 7
LSIO B36 SIO/SIN 7

RAMREF A51 VREFA 6,11
B51 VREFB
SMBCLK_CORE A53 SCL 3,9,11,32
SMBDATA_CORE A55 SDA
A57 SWP 3,9,11,32
B56 SVDDB
A56 SVDDA

C228
0.1UF

VCC3_3
R229
4.7K

SWP

R228
4.7K
Do not stuff R228

C169
0.1UF
VCC3_3

RCMD B59 RCMD_A B59 RCMD
RSCK A59 RSCK_A A59 RSCK
SIO/SOUT A36 MR1OUT 11 A36 SIO/SOUT

RDQA0 A83 RDQA0_A A83 RDQA0
RDQA1 B85 RDQA1_A B85 RDQA1
RDQA2 A85 RDQA2_A A85 RDQA2
RDQA3 B87 RDQA3_A B87 RDQA3
RDQA4 A87 RDQA4_A A87 RDQA4
RDQA5 B89 RDQA5_A B89 RDQA5
RDQA6 A89 RDQA6_A A89 RDQA6
RDQA7 B91 RDQA7_A B91 RDQA7
RDQA8 A91 RDQA8_A A91 RDQA8
RDQB0 B69 RDQB0_A B69 RDQB0
RDQB1 A67 RDQB1_A A67 RDQB1
RDQB2 B67 RDQB2_A B67 RDQB2
RDQB3 A65 RDQB3_A A65 RDQB3
RDQB4 B65 RDQB4_A B65 RDQB4
RDQB5 A63 RDQB5_A A63 RDQB5
RDQB6 B63 RDQB6_A B63 RDQB6
RDQB7 A61 RDQB7_A A61 RDQB7
RDQB8 B61 RDQB8_A B61 RDQB8

RROW0 B75 RROW0_A B75 RROW0
RROW1 A75 RROW1_A A75 RROW1
RROW2 B77 RROW2_A B77 RROW2
RCOL0 A69 RCOL0_A A69 RCOL0
RCOL1 B71 RCOL1_A B71 RCOL1
RCOL2 A71 RCOL2_A A71 RCOL2
RCOL3 B73 RCOL3_A B73 RCOL3
RCOL4 A73 RCOL4_A A73 RCOL4

RCFM B83 RCFM_A B83 RCFM
RCFM# B81 RCFMN_A B81 RCFM#
RCTM A79 RCTM_A A79 RCTM
RCTM# A81 RCTMN_A A81 RCTM#

SA0 B53 VCC3_3 B53 SA0
SA1 B55 B55 SA1
SA2 B57 B57 SA2

RSRV4/RESET B38 B38 RSRV4/RESET

PCIRST# 6,8,10,12,16,19,20,21,22

J18 RIMM

LDQA0	A10	TERM_DQA0
LDQA1	B8	TERM_DQA1
LDQA2	A8	TERM_DQA2
LDQA3	B6	TERM_DQA3
LDQA4	A6	TERM_DQA4
LDQA5	B4	TERM_DQA5
LDQA6	A4	TERM_DQA6
LDQA7	B2	TERM_DQA7
LDQA8	A2	TERM_DQA8
LDQB0	B24	TERM_DQB0
LDQB1	A26	TERM_DQB1
LDQB2	B26	TERM_DQB2
LDQB3	A28	TERM_DQB3
LDQB4	B28	TERM_DQB4
LDQB5	A30	TERM_DQB5
LDQB6	B30	TERM_DQB6
LDQB7	A32	TERM_DQB7
LDQB8	B32	TERM_DQB8

TERM_DQA[8:0] 33
TERM_DQB[8:0] 33

LROW2 B16 TERM_ROW2
LROW1 A18 TERM_ROW1
LROW0 B18 TERM_ROW0
LCOL4 A20 TERM_COL4
LCOL3 B20 TERM_COL3
LCOL2 A22 TERM_COL2
LCOL1 B22 TERM_COL1
LCOL0 A24 TERM_COL0

TERM_ROW[2:0] 33
TERM_COL[4:0] 33

LCFM B10 CLKFM
LCFM# B12 CLKFM#
LCTM A14 CLKTM
LCTM# A12 CLKTM#

R287 28-1% CTERM_RIMM
R286 28-1%
5
5
C291
0.1UF

LCMD B34 TERM_CMD 33
LSCK A34 TERM_SCK 33
SIO/SIN B36 MR1OUT11

VREFA A51
VREFB B51
SCL A53
SDA A55
SWP A57
SVDDB B56
SVDDA A56

VCC3_3
C165 0.1UF

SMBCLK_CORE 3,9,11,32
SMBDATA_CORE 3,9,11,32

RAMREF 6,11

C256 0.1UF   C243 0.1UF   C236 0.1UF

VCMOS1_8SBY:A35,A37,B35,B37
VCC2_5SBY:A41,A42,A54,A58,B41,B42,B54,B58
GND:A1,A3,A5,A7,A9,A11,A13,A15,A17,A29,A21,A23,A25,A27,A19,A31,A33,A39
GND:A52,A60,A62,A64,A66,A68,A70,A72,A74,A76,A78,A80,A82,A84,A86,A88,A90,A92
GND:B1,B3,B5,B7,B9,B11,B13,B15,B17,B29,B21,B23,B25,B27,B19,B31,B33,B39
GND:B52,B60,B62,B64,B66,B68,B70,B72,B74,B76,B78,B80,B82,B84,B86,B88,B90,B92
RSV_,SRIMM: NC:A43,A44,A45,A46,A47,A48,A49,A50,B43,B44,B45,B46,B47,B48,B49,B50
RSV_EXP: NC:A16,A77,B14,B79
RSV_SPARE: NC:A38,A40,B40

NC:A43,A44,A45,A46,A47,A49,A50,B43,B44,B45,B46,B47,B48,B49,B50 RSV_SRIMM:
GND:B52,B60,B62,B64,B66,B68,B70,B72,B74,B76,B78,B80,B82,B84,B86,B88,B90,B92
GND:B1,B3,B5,B7,B9,B11,B13,B15,B17,B29,B21,B23,B25,B27,B19,B31,B33,B39
GND:A1,A3,A5,A7,A9,A11,A13,A15,A17,A29,A21,A23,A25,A27,A19,A31,A33,A39
GND:A52,A60,A62,A64,A66,A68,A70,A72,A74,A76,A78,A80,A82,A84,A86,A88,A90,A92
VCC2_5SBY:A41,A42,A54,A58,B41,B42,B54,B58
VCMOS1_8SBY:A35,A37,B35,B37
NC:A38,A40,B40 RSV_SPARE:
NC:A16,A77,B14,B79 RSV_EXP:

SMBCLK_CORE 3,9,11,32
SMBDATA_CORE 3,9,11,32

Super I/O

U17

SIO
LPC47B27X

LPC I/F
PARALLEL PORT I/F
KYBD/MSE I/F
INFRARED I/F
SERIAL PORT 1
SERIAL PORT 2
FDC I/F
CLOCKS

VREF 44
VTR 18
VCC1 53
VCC2 65
VCC3 93

VCC5
VCC3_3

LFRAME#/FWH4 24 — LFRAME#   9,10,12
LAD3/FWH3 23 — LAD3   9,10,12
LAD2/FWH2 22 — LAD2   9,10,12
LAD1/FWH1 21 — LAD1   9,10,12
LAD0/FWH0 20 — LAD0   9,10,12
LDRQ#0 25 — LDRQ#0   9,12
PCIRST# 26 — LRESET#   6,8,10,11,12,16,19,20,21,22
LPCPD# 27 — LPCPD#
LPC_PME# 17 — PME#   9
SERIRQ 30 — SERIRQ   8,12,21,32
SIO_PCLK7 29 — PCI_CLK   5,12

INIT# 66 — PAR_INIT# 24
SLCTIN# 67 — SLIN# 24
PD7 75 — PDR7 24
PD6 74 — PDR6
PD5 73 — PDR5
PD4 72 — PDR4
PD3 71 — PDR3
PD2 70 — PDR2
PD1 69 — PDR1
PD0 68 — PDR0
SLCT# 77 — SLCT 24
PE 78 — PE 24
BUSY 79 — BUSY 24
ACK# 80 — ACK# 24
ERROR# 81 — ERR# 24
ALF# 82 — AFD# 24
STROBE# 83 — STB# 24

PDR[7:0] 24

KBDAT 56 — KDAT   26
KBCLK 57 — KCLK   26
MDAT 58 — MDAT   26
MCLK 59 — MCLK   26
KBRST# 63 — KBDRST   8,32
A20GATE 64 — A20GATE   8,32

IRRX 61 — IRRX2/GP34   18
IRTX 62 — IRTX2/GP35   18

FAN2/GP32 54 — PWM2 18
FAN1/GP33 55 — PWM1 18
FDC_PP/DDRC/GP43 28

RXD0 84 — RXD1   25
TXD0 85 — TXD1   25
DSR#0 86 — DSR1#   25
RTS#0 87 — RTS1#   25
CTS#0 88 — CTS1#   25
DTR#0 89 — DTR1#   25
RI#0 90 — RI1#   25
DCD#0 91 — DCD1#   25

RXD1 95 — RXD2_IRRX   25
TXD1 96 — TXD2_IRTX   25
DSR#1 97 — DSR2#   25
RTS#1 98 — RTS2#   25
CTS#1 99 — CTS2#   25
DTR#1 100 — DTR2#   25
RI#1 92 — RI2#   25
DCD#1 94 — DCD2#   25

DRVDEN#1 2 — DRVDEN1   26
DRVDEN#0 1 — DRVDEN0   26
MTR#0 3 — MTR0#   26
DS#0 5 — DS0#   26
DIR# 8 — DIR#   26
STEP# 9 — STEP#   26
WDATA# 10 — WDATA#   26
WGATE# 11 — WGATE#   26
HDSEL# 12 — HDSEL#   26
INDEX# 13 — INDEX#   26
TRK#0 14 — TRK0#   26
WRTPRT# 15 — WRTPRT#   26
RDATA# 16 — RDATA#   26
DSKCHG# 4 — DSKCHG#   26

GP60/LED1 48
GP61/LED2 49
GP27/IO_SMI# 50 — LPC_SMI# 9
GP30/FAN_TACH2 51 — TACH2 18
GP31/FAN_TACH1 52 — CPU_TACH1

GP25/MIDI_IN 46 — MIDI_IN 27
GP26/MIDI_OUT 47 — MIDI_OUT 27

GP10/J1B1 32 — J1BUTTON1 27
GP11/J1B2 33 — J1BUTTON2 27
GP12/J2B1 34 — J2BUTTON1 27
GP13/J2B2 35 — J2BUTTON2 27
GP14/J1X 36 — JOY1X 27
GP15/J1Y 37 — JOY1Y 27
GP16/J2X 38 — JOY2X 27
GP17/J2Y 39 — JOY2Y 27
GP20/P17 41 — KEYLOCK# 18
GP21/P16 42
GP22/P12 43

GP24/SYSOPT 45 — SYSOPT

CLKI32 6 — CLKI32
CLOCKI 19 — SIO_14MHZ   5

GND1 7
GND2 31
GND3 60
GND4 76
AVSS 40

VCC3_3
R315 4.7K
26 VCC5_KBMS_J

RP5
4.7K
1 2 3 4
8 7 6 5

VCC5
VCC3_3

C309 0.1UF
C348 0.1UF
C321 0.1UF
C313 0.1UF
C323 0.1UF
C349 2.2UF

Place next to VREF.   Place decoupling caps near each power pin.

C320 470PF
C317 470PF

VCC3_3
R313 4.7K

R312 4.7K
Pulldown on SYSOPT for IO address of 0x02E

LPC header. For debug only.

J20

9,10,12 LAD3/FWH3 1 2
9,10,12 LAD2/FWH2 3 4
9,10,12 LAD1/FWH1 5 6
9,10,12 LAD0/FWH0 7 8
9,10,12 LFRAME#/FWH4 9 10
6,8,10,11,12,16,19,20,21,22 PCIRST# 11 12
5,12 SIO_PCLK7 13 14
9,12 LDRQ#0 15 16
17 18
5,9 MULT1_GPIO 19 20
21 22
8,12,21,32 SERIRQ 23 24
25 26
27 28

AC'97 Audio

VR2
MC78M05CDT

VCC12

VCC5_AUDIO → 13,14

C62 0.1UF
C83 10UF
C57 10UF
C48 0.1UF
L17

No stuff C358.
C358 0.1UF

VCC3_3

C77 0.1UF
C49 0.1UF
C21 0.1UF

VCC5_AUDIO → 13,14

AGND   AGND   AGND

VCC3_3

0.1UF
C76

18 → AC97_SPKR   R67 10K   AC97_SPKR_R

R66 1K
C85 0.1UF

1UF-TANT C70   AC97_SPKR_C   12

U2

DVDD1 1
DVSS1 4
DVSS2 7
DVDD2 9
AVDD2 38
AVSS2 42
AVDD1 25
AVSS1 26
NC40 40
NC44 44
NC43 43

AD1881

14 → LINE_IN_R   24 LINE_IN_R
14 → LINE_IN_L   23 LINE_IN_L
14 → MIC_IN   21 MIC1
                 22 MIC2
14 → CD_R   20 CD_R
14 → CD_L   18 CD_L
14 → CD_REF   19 CD_REF
                 17 VIDEO_R
                 16 VIDEO_L
                 14 AUX_L
                 15 AUX_R
15 → MONO_PHONE 2 C63 1 1UF-TANT   MONO_PHONE_C 13 PHONE
15 → MONO_OUT   2 C12 1 MONO_OUT_C 37 MONO_OUT
                 1UF-TANT
14 →   36 LINE_OUT_R
14 →   35 LINE_OUT_L
14 → LNLVL_OUT_R 41 LNLVL_OUT_R
14 → LNLVL_OUT_L 39 LNLVL_OUT_L

PC_BEEP

RESET#   11 PRI_DWN_RST#_R   R31 0K   PRI_DWN_RST# → 15
SDATA_OUT   5 AC_SDATAOUT_R 0K R77   AC_SDATAOUT → 9,15
SDATA_IN   8 AC_SDATAIN_R R116 0K   AC_SDATAIN0 → 9,15
SYNC   10 AC_SYNC_R   0K R106   AC_SYNC → 9,15
BIT_CLK   6 AC_BITCLK_R   R56 0K   AC_BITCLK → 9,15
                              0K

Series resistors are for test purposes only.

CS1 46
CS0 45
CHAIN_CLK 48
EAPD 47

C84 10PF
No stuff C84.

VCC3_3

R29 100K No stuff

EAPD → 14

R28 100K No stuff

AFILT1 29
AFILT2 30
FILT_L 31
FILT_R 32
CX3D 34
RX3D 33
VREF 27
VREFOUT 28
XTL_IN 2
XTL_OUT 3

AFILT1_C
AFILT2_C
FILT_L_C
FILT_R_C
CX3D_C
RX3D_C
AC_VREF_C
AUD_VREFOUT → 14
AC_XTAL_IN → 14
AC_XTAL_OUT

C19 270PF-NPO
C18 270PF-NPO
C7 1UF-TANT
C15 1UF
C13 1UF
C16 0.1UF
C17 0.047UF
C20 0.1UF
C9 10UF-TANT

Y1 XTAL
1 2
24.576MHZ
C95 22PF
C94 22PF

AGND   AGND   AGND

AC'97 Audio

Stereo HP/Spkr out

HP_OUTA
C10 100UF
HP_OUTA_C
L4
HP_OUTA HP30
HP29
HP28
HP_OUTB HP27
HP26
J5
DB15_AUD_STK

C3 100UF
HP_OUTB_C
L1

C24 10PF-NPO
C11 10PF-NPO
AGND

AGND AGND

Microphone Input

AUD_VREFOUT
R7 2.2K
MIC_IN_R

13 MIC_IN
C27 1UF-TANT
MIC_IN_C
R9 1K

C34 0.01UF
AGND

C28 10PF-NPO
AGND

L5

MIC_IN_R M20
M19
M18
M17
M16
J5
DB15_AUD_STK
AGND

C8 100PF
R4 20K

U1 LM4880
1 OUTA   VDD 8
2 INA   OUTB 7
3 BYPASS INB 6
4 GND   SHUTDN 5

VCC5_AUDIO 13
HP_OUTB
EAPD 13

C4 100PF
R2 20K

C14 0.1UF
AGND

Line_In Analog Input

13 LNLVL_OUT_R
C6 1UF-TANT
LNLVL_R_C
R1 20K
LNLVL_R_R
AC_BYPASS
AGND

13 LNLVL_OUT_L
C13 1UF-TANT
LNLVL_L_C
R3 20K

C2 1UF
AGND

LNLVL_L_R

13 LINE_IN_R
C23 1UF-TANT
LINE_IN_R_C
L2
LINE_IN_R_E LI25
LI24
LI23
LINE_IN_L_E LI22
LI21
J5
DB15_AUD_STK

13 LINE_IN_L
C25 1UF-TANT
LINE_IN_L_C
L3

C22 10PF-NPO
C26 10PF-NPO
AGND AGND
AGND

CD Analog Input

J4
1 CD_L_J
2 CD_REF_J
3
4 CD_R_J

R52 4.7K
CD_L_C
C59 1UF
CD_L 13

R27 4.7K
CD_REF_C
C58 1UF
CD_REF 13

R18 4.7K
CD_R_C
C50 1UF
CD_R 13

R51 4.7K
R30 4.7K
R25 4.7K
AGND AGND AGND

AC'97 Audio/Modem Riser

AC'97_RISER
AMR_CONNECTOR

J8

Pin	Signal (B)		Signal (A)	Pin
B1	AUDIO_MUTE#		AUDIO_PWRDWN	A1
B2	GND[0] (ISOLATED)		MONO_PHONE	A2
B3	MONO_OUT/PC_BEEP		RESV[5]	A3
B4	RESV[1]		RESV[6]	A4
B5	RESV[2]		RESV[7]	A5
B6	PRIMARY_DN#		GND[7]	A6
B7	-12V		+5VDUAL/5VSBY	A7
B8	GND[1]		USB_OC	A8
B9	+12V		GND[8]	A9
B10	GND[2]		USB+	A10
B11	+5VD		USB-	A11
	KEY		KEY	
	KEY		KEY	
B12	GND[3]		GND[9]	A12
B13	RESV[3]		S/P_DIF_IN	A13
B14	RESV[4]		GND[10]	A14
B15	+3.3VD		+3VDUAL/3VSBY	A15
B16	GND[4]		GND[11]	A16
B17	AC97_SDATA_OUT		AC97_SYNC	A17
B18	AC97_RESET#		GND[12]	A18
B19	AC97_SDATA_IN3		AC97_SDATA_IN1	A19
B20	GND[5]		GND[13]	A20
B21	AC97_SDATA_IN2		AC97_SDATA_IN0	A21
B22	GND[6]		GND[14]	A22
B23	AC97_MSTRCLK		AC97_BITCLK	A23

VCC3_3SBY

R68 4.7K

VCC3_3SBY

U3
SN74LVC08A
PRI_DWN_RST#   4 PRI_DWN_U
13
PRI_DWN#

13   MONO_OUT

JP2

VCC3_3 VCC5 VCC12 VCC12-

VCC5

VCC3_3SBY

MONO_PHONE   13

AC97_OC#   23
AC97_USB+   23
AC97_USB-   23

AC_SYNC   9,13

AC_SDATAIN1_R   R113 0K   AC_SDATAIN1   9
AC_SDATAIN0   9,13
AC_BITCLK   9,13

R108 10K
R125 10K

9,13   AC_SDATAOUT
9   AC_RST#

Audio Down	JP2
Enable*	1-2
Disable	2-3

LAN

U5

82559

AD[31:0] 8,20,21

Pin	Signal
N7	AD0
M7	AD1
P6	AD2
P5	AD3
N5	AD4
M5	AD5
P4	AD6
N4	AD7
P3	AD8
N3	AD9
N2	AD10
M1	AD11
M2	AD12
M3	AD13
L1	AD14
L2	AD15
K1	AD16
E3	AD17
D1	AD18
D2	AD19
D3	AD20
C1	AD21
B1	AD22
B2	AD23
B4	AD24
A5	AD25
B5	AD26
B6	AD27
C6	AD28
C7	AD29
A8	AD30
B8	AD31

C_BE#[3:0] 8,20,21

Pin	Signal
M4	C/BE0#
L3	C/BE1#
F3	C/BE2#
C4	C/BE3#

Top bus signals (VCC):
VCCPL[0] G13, VCCPL[1] K13, VCCPL[2] N8, VCCPL[3] P12, VCCPT A11
VCCPP[0] A3, VCCPP[1] A7, VCCPP[2] E1, VCCPP[3] K3, VCCPP[4] N6, VCCPP[5] P2
VCC[0] E12, VCC[1] G5, VCC[2] G6, VCC[3] H5, VCC[4] H6, VCC[5] H7, VCC[6] H8, VCC[7] J5, VCC[8] J6, VCC[9] J7, VCC[10] J8, VCC[11] J9, VCC[12] J10, VCC[13] J11, VCC[14] K4, VCC[15] K5, VCC[16] K6, VCC[17] K7, VCC[18] K8, VCC[19] K9, VCC[20] K10, VCC[21] K11, VCC[22] L4, VCC[23] L5, VCC[24] L9, VCC[25] L10

VCC3_3SBY

Signal	Pin	Net	→
FRAME#	F2	FRAME#	8,20,21,32
IRDY#	F1	IRDY#	8,20,21,32
TRDY#	G3	TRDY#	8,20,21,32
DEVSEL#	H3	DEVSEL#	8,20,21,32
STOP#	H1	STOP#	8,20,21,32
PAR	J1	PAR	8,20,21
INTA#	H2	PIRQ#A	8,19,20,21,32
PERR#	J2	PERR#	8,20,21,32
SERR#	A2	SERR#	8,20,21,32
IDSEL	A4	AD20_RLAN / AD20	8,16 (R75 100)
REQ#	C3	PREQ#3	8,32
GNT#	J3	PGNT#3	8,32
RST#	C2	PCIRST#	7,9,29,3
CLK	G1	PCLK5	6,8,10,11,12,19,20,21,22 / 5
ISOLATE#	B9	PWROK	7,9,29,3
ALTRST#	A9	LAN_RSMRST#	17
SMBCLK	A10	ALERTCLK_SBY	9,32
SMBD	C9	ALERTDATA_SBY	9,32
VIO	G2		
X1	N11	LAN_X1	
X2	P11	LAN_X2	

Right side signals:

Signal	Pin	Net
LILED	A12	LILED → 17
ACTLED	C11	ACTLED → 17
SPEEDLED	B11	SPEEDLED → 17
TDP	C13	TDP → 17
TDN	C14	TDN → 17
RDP	E13	RDP → 17
RDN	E14	RDN → 17
SMBALRT#	B10	
CSTSCHG	C5	
PME#	A6	PCI_PME# → 8,19,20,21
FLA0/PCIMODE#	J13	
FLA1/AUXPWR	J12	AUXPWR
FLA2	K14	
FLA3	L14	
FLA4	L13	
FLA5	L12	
FLA6	M14	
FLA7	M13	
FLA8/IOCHRDY	N14	
FLA9/MRST	P13	
FLA10/MRING#	N13	
FLA11/MINT	M12	
FLA12/MCNTSM#	M11	
FLA13/EEDI	P10	EEDI
FLA14/EEDO	N10	EEDO
FLA15/EESK	M10	EESK
FLA16	P9	
FLD0	F14	
FLD1	F13	
FLD2	F12	
FLD3	G12	
FLD4	H14	
FLD5	H13	FLD5
FLD6	H12	FLD6
FLD7	J14	
EECS	P7	EECS
FLCS#	N9	
FLOE#	M8	
FLWE#	M9	
CLKRUN#	C8	CLKRUN#_LAN
TEST	A13	TEST_LAN
TEXEC	D13	
TCK	D14	
TI	D12	
TO	B12	
RBIAS10	B14	RBIAS10
RBIAS100	B13	RBIAS100
VREF	C12	

VCC3_3SBY R59 3.3K

U8 93C46
- 3 EEDI (VCC 8)
- 4 EEDO (NC2 7)
- 2 EESK (NC1 6)
- 1 EECS (GND 5)

VCC3_3SBY

No stuff R57, R58
R58 3.3K
R57
R11 62K
R14 3.3K
R16 549
R15 619

Y2 XTAL 25MHZ
C101 22PF   C96 22PF
VCC5SBY

Bottom VSS pins:
VSSPL[0] G14, VSSPL[1] K12, VSSPL[2] P8, VSSPL[3] N12, VSSPT C10
VSSPP[0] B3, VSSPP[1] B7, VSSPP[2] E2, VSSPP[3] K2, VSSPP[4] M6, VSSPP[5] N1
VSS[0] D4, VSS[1] D5, VSS[2] D6, VSS[3] D7, VSS[4] D8, VSS[5] D11, VSS[6] E4, VSS[7] E5, VSS[8] E6, VSS[9] E7, VSS[10] E8, VSS[11] E10, VSS[12] E11, VSS[13] F4, VSS[14] F5, VSS[15] F6, VSS[16] F7, VSS[17] F8, VSS[18] F10, VSS[19] F11, VSS[20] G7, VSS[21] G8, VSS[22] G9, VSS[23] G10, VSS[24] G11, VSS[25] H9, VSS[26] H10, VSS[27] H11, VSS[28] L6, VSS[29] L7, VSS[30] L8, VSS[31] L11

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.01
LAN CONTROLLER	
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
LAST REVISED: 11-18-1999_10:48	SHEET: 16 OF 36

LAN

Place termination resistors close to 82559.

No stuff C61, C79.

No stuff JP1,JP3,JP4,R60,R73,R78.

For debug only. Hold LAN in reset.

No stuff C5.
C5 must be rated at 1500V.

No stuff C31.

82559 LAN	J17
Enable*	1-2
Disable	2-3

TD_C
TDP
R26 49.9-1%
R20 49.9-1%
TDN
RDP
R62 49.9-1%
RD_C
R63 49.9-1%
RDN
C61 0.1UF
C79 0.1UF

J2 RJMAG
TD+ 10
TD- 12
RD+ 9
RD- 7
RJ-4 3
RJ-5 4
RJ-7 5
RJ-8 6
RJ-45
TXC 2
RXC 1
SHLD1 17
SHLD2 18
TDC 11
RDC 8

14
13 LILED 16,17
16
15 ACTLED 16,17

VCC3_3
R61 330 LI_CR
R64 330 ACT_CR

RJ4_J
RJ_7_J
TXC_J
RXC_J
TDC_J
RDC_J

R6 75
R5 75
R8 75
R10 75
C31 0.1UF
C78 0.1UF

XC_R
C5 470PF

VCC3_3
R73 330 LI_J
R78 330 ACT_J
R60 330 SPEED_J
JP3
JP4
JP1

LILED 16,17
ACTLED 16,17
SPEEDLED 16

J17
RSMRST# 1
LAN_RSMRST# 2
3
9,31
16

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
LAN
REV: 1.01

PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY:
PROJECT:
LAST REVISED: 11-18-1999_10:48
SHEET: 17 OF 36

System

No stuff.
For test only

ICH has internal pullup and debounce on PWRBTN#

SW1

R252 1M

R257 0K

PWRBTN# 9

C267 1UF   No stuff. For test only

PWRBTN_FP#

VCC5 VCC5

R345 10K   R344 10K

VCC3_3

U19
SN74LVC07A

IDEACTP# 22   IDE_ACTIVE

VCC3_3

U19
SN74LVC07A

IDEACTS# 22

JP25

SPKR 9   AC97_SPKR 13

PC_BEEP

Onboard Spkr	JP25
Enable*	2-3
Disable	1-2

R350 2.2K   P_BEEP

Speaker Circuit

SPKR_Q

Q15 MMBT3904LT1

R352 68

R353 68

C353 0.1UF

VCC3_3SBY

R289 330

SBY_LED_CR

CR7

Onboard LED indicates the standby well is on
to prevent hot swapping memory.
For debug only.

VCC3_3SBY

VCC3_3

100K R359

VCC5   C350 0.1UF 50V   C356 10UF 16V

IRRX 12
IRTX 12   IRTX_R 82
R357

R358 4.7K

R356 470

HDLED_R

C354 470PF   C355 470PF

VCC3_3   VCC5

R355 220   PLED_R

10K R354

KEYLOCK# 12

SPKR_FP

VCC5

SP1
1 + POS
2   NEG
SPKR_ONBOARD

J25

INFRARED

KEY

POWER SW.

H.D. LED

KEY

POWER LED

KEY

KEYLOCK

KEY   SPEAKER

FNT_PNL_CONN

VCC3_3SBY

VCC3_3SBY   R253 330

VCC3_3SBY

VCC3_3SBY   R246 330

VCC3_3SBY

GPIO23_FPLED 9   U14
SN74LVC07A

LED_PU0

CR6
DUAL_COLOR

LED_PU1

U14
SN74LVC07A   GPIO26_FPLED 9

R234 4.7K

TACH2

VCC12   VCC3_3

C316 0.1UF

JP22
1
2
3

R316 4.7K

TACH2 12

PWM1

VCC12   VCC3_3

C327 0.1UF

JP24
1
2
3

R329 4.7K

PWM1 12

PWM2

VCC12   VCC3_3

C322 0.1UF

JP23
1
2
3

R326 4.7K

PWM2 12

PWM outputs from SIO need power buffers for driving fan inputs.

AGP Connector

VCC3_3   VDDQ   VCC12

SBA[7:0]
7
7   ST[2:0]

VCC5

J13
AGP4XU_20

B1	OVRCNT#	AGP_OC#	23		12V	A1	
B2	5V_A				TYPEDET#	A2	TYPEDET#	19,29
B3	5V_B				RESV_A	A3	
B4	USB+	USBAGP+	23		USB-	A4	USBAGP-	23
B5	GND_K				GND_A	A5	
B6	INTB#				INTA#	A6	
B7	CLK	AGPCLK_CONN	5		RST#	A7	PCIRST#	6,8,10,11,12,16,20,21,22
B8	REQ#	GREQ#	7,32		GNT#	A8	GGNT#	7,32
B9	VCC3_3_F				VCC3_3_A	A9	
B10	ST0	ST0			ST1	A10	ST1
B11	ST2	ST2			RESV_B	A11	
B12	RBF#	RBF#	7,32		PIPE#	A12	PIPE#	7,32
B13	GND_L				GND_B	A13	
B14	RESV_H				WBF#	A14	WBF#	7,32
B15	SBA0	SBA0			SBA1	A15	SBA1
B16	VCC3_3_G				VCC3_3_B	A16	
B17	SBA2	SBA2			SBA3	A17	SBA3
B18	SB_STB	SBSTB	7,32		SB_STB#	A18	SBSTB#	7,32
B19	GND_M				GND_C	A19	
B20	SBA4	SBA4			SBA5	A20	SBA5
B21	SBA6	SBA6			SBA7	A21	SBA7
B22	RESV				RESV_C	A22	
B23	GND_N				GND_D	A23	
B24	3_3VAUX1				RESV_D	A24	
B25	VCC3_3_H				VCC3_3_C	A25	
B26	AD31	GAD31			AD30	A26	GAD30
B27	AD29	GAD29			AD28	A27	GAD28
B28	VCC3_3_I				VCC3_3_D	A28	
B29	AD27	GAD27			AD26	A29	GAD26
B30	AD25	GAD25			AD24	A30	GAD24
B31	GND_O				GND_E	A31	
B32	AD_STB1	ADSTB1	7,32		AD_STB1#	A32	ADSTB#1	7,32
B33	AD23	GAD23			C/BE3#	A33	GC/BE#3
B34	VDDQ_F				VDDQ_A	A34	
B35	AD21	GAD21			AD22	A35	GAD22
B36	AD19	GAD19			AD20	A36	GAD20
B37	GND_P				GND_F	A37	
B38	AD17	GAD17			AD18	A38	GAD18
B39	C/BE2#	GC/BE#2			AD16	A39	GAD16
B40	VDDQ_G				VDDQ_B	A40	
B41	IRDY#	GIRDY#	7,32		FRAME#	A41	GFRAME#	7,32
B42	3_3VAUX2				RESV_E	A42	
B43	GND_Q				GND_G	A43	
B44	RESV_K				RESV_F	A44	
B45	VCC3_3_J				VCC3_3_E	A45	
B46	DEVSEL#	GDEVSEL#	7,32		TRDY#	A46	GTRDY#	7,32
B47	VDDQ_H				STOP#	A47	GSTOP#	7,32
B48	PERR#	GPERR#	32		PME#	A48	PCI_PME#	8,16,20,21
B49	GND_R				GND_H	A49	
B50	SERR#	GSERR#	32		PAR	A50	GPAR	7,32
B51	C/BE1#	GC/BE#1	32		AD15	A51	GAD15
B52	VDDQ_I				VDDQ_C	A52	
B53	AD14	GAD14			AD13	A53	GAD13
B54	AD12	GAD12			AD11	A54	GAD11
B55	GND_S				GND_I	A55	
B56	AD10	GAD10			AD9	A56	GAD9
B57	AD8	GAD8			C/BE0#	A57	GC/BE#0
B58	VDDQ_J				VDDQ_D	A58	
B59	AD_STB0	ADSTB0	7,32		AD_STB0#	A59	ADSTB#0	7,32
B60	AD7	GAD7	7,32		AD6	A60	GAD6
B61	GND_T				GND_J	A61	
B62	AD5	GAD5			AD4	A62	GAD4
B63	AD3	GAD3			AD2	A63	GAD2
B64	VDDQ_K				VDDQ_E	A64	
B65	AD1	GAD1			AD0	A65	GAD0
B66	VREF_CG	MCH_AGPREF	6		VREF_GC	A66	

PIRQ#B   8,20,21,32
PIRQ#A   8,16,20,21,32

VCC3_3SBY

AGPREF circuitry should be placed close to MCH.

VDDQ
R193   301-1%
CON_AGPREF_Q
Q8   2N7002LT1
R208   200-1%
TYPEDET#   19,29
CONN_AGPREF   6

7 GAD[31:0]
7 GC/BE#[3:0]

PCI Connectors
0 and 1

For pullups, see 4.3.3 of PCI 2.1 Specification

PCI Slot 0
J10
PCI3_CON

PCI Slot 1
J9
PCI3_CON

VCC3_3
VCC12- VCC5
VCC5 VCC12

VCC3_3
VCC12- VCC5
VCC5

VCC5 VCC5
VCC12

5.6K R76
R79 5.6K

R72
5.6K

R74
5.6K

PTCK
20,21
PTRST# 20,21
PTMS 20,21
PTDI 20,21
PIRQ#A 8,16,19,20,21,32
PIRQ#C 8,20,21,32
8,19,20,21,32 PIRQ#B
8,20,21,32 PIRQ#D
20 PRSNT#11
20 PRSNT#12
VCC3_3SBY
5 PCLK1
PCIRST# 6,8,10,11,12,16,19,20,21,22
PGNT#0 8,32
8,32 PREQ#0
PCI_PME# 8,16,19,20,21

PTCK
20,21 PTCK
PTRST# 20,21
PTMS 20,21
PTDI 20,21
PIRQ#B 8,19,20,21,32
PIRQ#D 8,20,21,32
8,20,21,32 PIRQ#C
8,16,19,20,21,32 PIRQ#A
20 PRSNT#21
20 PRSNT#22
VCC3_3SBY
5 PCLK2
PCIRST# 6,8,10,11,12,16,19,20,21,22
PGNT#1 8,32
8,32 PREQ#1
PCI_PME# 8,16,19,20,21

AD31 B20 A20 AD30
AD29 B21 A21
B22 A22 AD28
AD27 B23 A23 AD26
AD25 B24 A24
B25 A25 AD24
C_BE#3 B26 A26 R_AD16 20
AD23 B27 A27
B28 A28 AD22
AD21 B29 A29 AD20
AD19 B30 A30
B31 A31 AD18
AD17 B32 A32 AD16
C_BE#2 B33 A33
B34 A34 FRAME# 8,16,20,21,32
8,16,20,21,32 IRDY# B35 A35
B36 A36 TRDY# 8,16,20,21,32
8,16,20,21,32 DEVSEL# B37 A37
B38 A38 STOP# 8,16,20,21,32
8,20,21,32 PLOCK# B39 A39
8,16,20,21,32 PERR# B40 A40 SDONEP1 20
B41 A41 SBOP1 20
8,16,20,21,32 SERR# B42 A42
B43 A43 PAR 8,16,20,21
C_BE#1 B44 A44 AD15
AD14 B45 A45
B46 A46 AD13
AD12 B47 A47 AD11
AD10 B48 A48
B49 A49 AD9

key

AD8 B52 A52 C_BE#0
AD7 B53 A53
B54 A54 AD6
AD5 B55 A55 AD4
AD3 B56 A56
B57 A57 AD2
AD1 B58 A58 AD0
B59 A59
20 PU1_ACK64# B60 A60 PU1_REQ64# 20
B61 A61
B62 A62

AD31 B20 A20 AD30
AD29 B21 A21
B22 A22 AD28
AD27 B23 A23 AD26
AD25 B24 A24
B25 A25 AD24
C_BE#3 B26 A26 R_AD17 20
AD23 B27 A27
B28 A28 AD22
AD21 B29 A29 AD20
AD19 B30 A30
B31 A31 AD18
AD17 B32 A32 AD16
C_BE#2 B33 A33
B34 A34 FRAME#
IRDY# B35 A35
B36 A36 TRDY#
DEVSEL# B37 A37
B38 A38 STOP#
PLOCK# B39 A39
PERR# B40 A40 SDONEP2
B41 A41 SBOP2
SERR# B42 A42
B43 A43 PAR
C_BE#1 B44 A44 AD15
AD14 B45 A45
B46 A46 AD13
AD12 B47 A47 AD11
AD10 B48 A48
B49 A49 AD9

key

AD8 B52 A52 C_BE#0
AD7 B53 A53
B54 A54 AD6
AD5 B55 A55 AD4
AD3 B56 A56
B57 A57 AD2
AD1 B58 A58 AD0
B59 A59
20 PU2_ACK64# B60 A60 PU2_REQ64# 20
B61 A61
B62 A62

VCC5
RP12
20 SDONEP1 1 8
20 SDONEP2 2 7
20 SBOP1 3 6
20 SBOP2 4 5
5.6K

C117 0.1UF
20 PRSNT#11
C123 0.1UF
20 PRSNT#12
C113 0.1UF
20 PRSNT#21
C122 0.1UF
20 PRSNT#22

VCC5
R178
20 PU1_ACK64# 2.7K
R179
20 PU1_REQ64# 2.7K
R176
20 PU2_ACK64# 2.7K
R177
20 PU2_REQ64# 2.7K

8,16 AD16 R120 R_AD16 20
100
8,16 AD17 R119 R_AD17 20
100

8,16,21 C_BE#[3:0]
8,16,21 AD[31:0]

PCI Connectors
2 and 3

This page is a schematic diagram showing PCI Connectors 2 and 3 for an Intel 820 chipset reference board.

J9 must be furthest from the processor.

PCI Slot 2
J12
PCI3_CON

PCI Slot 3
J11
PCI3_CON

IDE Connectors

Primary IDE

PDD[15:0]

	J22
PCIRST_BUF#	
	R333 PCIRST#_RP1
	33

VCC5

PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15

R336 1K

	19	20	
PDREQ	21	22	
	23	24	PDIOW#
PIORDY	25	26	PDIOR#
	27	28	IDE_JP
PDDACK#	29	30	
IRQ14	31	32	
PDA1	33	34	P66DETECT
PDA0	35	36	
PDCS#1	37	38	PDCS#3
IDEACTP#	39	40	
PDA2			

R335 5.6K
R337 470
R334 10K

C329 0.047UF

PDA[2:0]

Secondary IDE

SDD[15:0]

	J21
PCIRST_BUF#	
	R318 PCIRST#_RS1
	33

VCC5

SDD7	3	4	SDD8
SDD6	5	6	SDD9
SDD5	7	8	SDD10
SDD4	9	10	SDD11
SDD3	11	12	SDD12
SDD2	13	14	SDD13
SDD1	15	16	SDD14
SDD0	17	18	SDD15

R321 1K

	19	20	
SDREQ	21	22	
	23	24	SDIOW#
SIORDY	25	26	SDIOR#
	27	28	IDE_JS
SDDACK#	29	30	
IRQ15	31	32	
SDA1	33	34	S66DETECT
SDA0	35	36	
SDCS#1	37	38	SDCS#3
IDEACTS#	39	40	
SDA2			

R320 5.6K
R322 470
R319 10K

C318 0.047UF

SDA[2:0]

For drive side detection, stuff C329,C318.
For host side detection, no stuff C329,C318.
P66DETECT and S66DETECT can be connected to a GPI for BIOS cable detection.

VCC3_3

VCC3_3
R351 8.2K

U19
VCC
PCIRST# 5 6 PCIRST_BUF#
6,8,10,11,12,16,19,20,21
GND
SN74LVC07A

USB Connectors

VCC3_3

R83
300K

AC97_OC#   15

R82
0K   Do Not Stuff

USBPWR1_F

L11
2   1

C99
68UF-TANT

C44
0.1UF

C98, C99 must have low ESR.

USBV0

VCC3_3   VCC5

R86
4.7K

C102
0.1UF

USBP0N   9

R240
15-1%

USBD0N_R

R501
0K

USBD0N

USBP0P   9

R242
15-1%

USBD0P_R

R502
0K

USBD0P

USBG0

10K
R87

OC#0   9

OC#0_RC

U7
TPS2042

2 IN   OUT1 7
8 OC#1 OUT2 6
5 OC#2 EN#1 3
1 GND   EN#2 4

C239
47PF

C241
47PF

R49
15K

R47
15K

R50
0K

R48
0K

Do Not Stuff

C38
470PF

L7
1

J3
USB_STK

1 VCC0
2 DATA0-
3 DATA0+
4 GND0
5 VCC1
6 DATA1-
7 DATA1+
8 GND1

VCC3_3

C109
0.1UF

AC97_USB+   15

AC97_USB-   15

VCC3_3

R91
4.7K

10K
R97

OC#1   9

OC#1_RC

USBPWR2_F

L10
2   1

C98
68UF-TANT

C43
0.1UF

C42
47PF

C40
47PF

C41
47PF

C39
47PF

C39-C42 for test and debug only.
Place caps close to connector.

C120
0.1UF

VCC3_3

R92
300K   Do Not Stuff

R88
0K

USBV1

AGP_OC#   19

USBP1N   9

R243
15

USBP1N_R

R46
0K

USBD1N

USBP1P   9

R244
15

USBP1P_R

R44
0K

USBD1P

USBG1

C244
47PF

C245
47PF

R45
15K

R43
15K

R41
0K

R42
0K

Do Not Stuff

C37
470PF

L6
1

USBAGP+   19

USBAGP-   19

15 ohm resistors and 47pf caps should be within 1" of ICH

Parallel Port

Serial Ports

COM2 is a 2x5 pin header for a cabled port.

Keyboard/Mouse/Floppy

Floppy Connector

VCC5

RP17
1K

R328
1K

VCC5

F1
1.0A

VCC5_KBMS_F

L15

VCC5_KBMS_J

J1

12 KBDAT
L16
KBDAT_FB

12 KBCLK
L12
KBCLK_FB

GND_KBMS_C

12 MDAT
L14
MDAT_FB

12 MCLK
L13
MCLK_FB

PS/2 Kybd

PS/2 Mse

GND_KBMS_FB

C45 100PF
C33 100PF
C32 100PF
C46 100PF
C47 0.1UF

L9

L7

J23

12 DRVDEN#0
12 DRVDEN#1
12 INDEX#
12 MTR#0
12 DS#0
12 DIR#
12 STEP#
12 WDATA#
12 WGATE#
12 TRK#0
12 WRTPRT#
12 RDATA#
12 HDSEL#
12 DSKCHG#

Game Port

VCC5 VCC5 VCC5 VCC5 VCC5 VCC5

VCC5

R39 4.7K   R35 4.7K   R37 1K   R36 1K   R32 1K   R33 1K

J5
DB15_AUD_STK
31

J1BUTTON1   12
J2BUTTON1   12
JOY1X   12
JOY2X   12
MIDI_OUT   12
JOY2Y   12
JOY1Y   12
J2BUTTON2   12
J1BUTTON2   12
MIDI_IN   12

R21 2.2K 5%
R22 2.2K 5%
R34 47
R23 2.2K 5%
R24 2.2K 5%
R38 47

JOY1X_R
JOY2X_R
MIDI_OUT_R
JOY2Y_R
JOY1Y_R
MIDI_IN_R

1
9
2
10
3
11
4
12
5
13
6
14
7
15
8
32

C69 0.01UF 25V 10%
C68 0.01UF 25V 10%
C67 0.01UF 25V 10%
C66 0.01UF 25V 10%

C56 470PF
C55 247PF 50V
C54 247PF 50V
C53 470PF
C52 247PF 50V
C51 247PF 50V

Tie game port capacitors together and to SIO AVSS. Tie to system ground at only a single point.

VRM

VRM requirements are based on VRM8.4 spec .

VCC12

VCC3_3 VCC5

R332
220

R53
5.6K

VRM_PWRGD → 4,31

VCC5

R71
5.1-5%

PVCC_R

L19
1UH

DO3316P-102

C97
1UF-X7R

Place caps next to output FETs.
C82,C87,C107,C111 must support >6A of RMS current.

VRM_VCC5

C118, C119 must be next to FETs.

R80
10K

C140
10UF

C90
0.1UF

C87
1200UF

C111
1200UF

C107
1200UF

C82
1200UF

C72
0.01UF

R54
2.7K

VRM_IMAX

C118
1UF-X7R

VCCVID

VR3

OUTEN   19 OUTEN   VCC PVCC   IMAX   7   VRM_IMAX
VID0   18 VID0   PWRGD   13
VID1   17 VID1   FAULT#   12   VRM_FAULT
VID2   16 VID2   G1   20   VRM_G1
VID3   15 VID3   IFB   8   VRM_IFB   R65
VID4   14 VID4   G2   1   VRM_G2   20
                                            VFB   11

VID[4:0]

3 >

Q3 SI4410DY
Q2 SI4410DY

IFB_Q

L18
1.0UH-20A
ETQP6F0R8L

COMP SS SGND GND SENSE VFB

LTC1753 10

VRM_COMP

C115
1UF-X7R

Q4 SI4410DY
Q5 SI4410DY

C73
150PF

R55
8.2K

C75
0.1UF

C86
0.1UF
No Stuff C106

C71
1000PF

VRM_COMP_R

VRM_SS

VRM_VFB

JP6 JP8 JP10 JP7 JP9

VID Override Jumpers

C74
0.01UF

C100
2200UF

C93
2200UF

C103
2200UF

C110
2200UF

Sanyo 4SP2200M

Voltage Regulators

VCC 5V DUAL VOLTAGE SWITCHER

The VCC5DUAL plane should not drive any logic components requiring 5V.
It should be used only for further regulation of lower voltage power planes
because the true voltage of VCC5DUAL will not remain constant
Rdson of the FET is not negligible for large currents

AGP VDDQ VOLTAGE REGULATOR

SN74LVC07A has 5V input and output tolerance.

VTT 1.5 VOLTAGE REGULATOR

VCC 1.8 VOLTAGE REGULATOR

VCC2_5 VOLTAGE REGULATOR

VCC3_3SBY VOLTAGE REGULATOR

Route VR6 GND to VDDQ output caps and then via to ground.
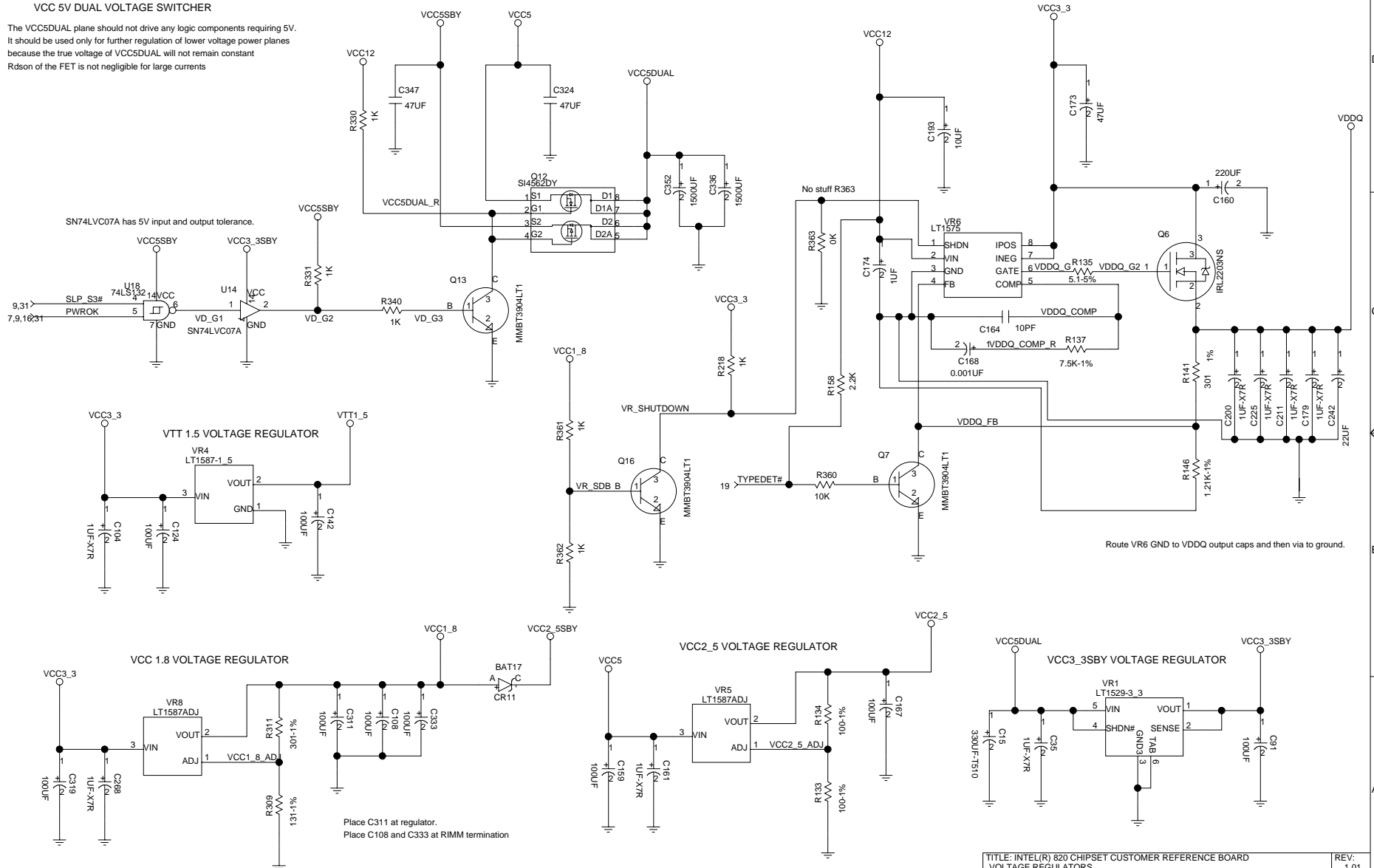
Place C311 at regulator.
Place C108 and C333 at RIMM termination

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
VOLTAGE REGULATORS
REV: 1.01

PCD PLATFORM DESIGN
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LAST REVISED: 11-18-1999_11:24
SHEET: 29 OF 36

Voltage Regulators

VCC 2.5 Standby Voltage Regulator

VCC5DUAL

C315 1UF-X7R
C314 100UF

VCC2_5SBY_TG
VCC2_5SBY_SW

VR7
LT1435

Q11
SI4966DY

VCMOS Generator For Rambus

VCC2_5SBY

VR7 LT1435	Pin		Pin	
SFB	4		13	VIN
COSC	1		16	TG
RUN/SS	2		14	SW
ITH	3		12	INTVCC
SGND	5		15	BOOST
VOSENSE	6		11	BG
EXTVCC	9		10	PGND
SENSE-	7		8	SENSE+

VCC2_5SBY_COSC
VCC2_5SBY_RUN
VCC2_5SBY_ITH

CR8
MMBD914LT1

SLP_S5#   9

VCC2_5SBY_INTVCC
V_BOOST

A   CMDSH-3
CR9

VCC2_5SBY_BG

L23
10UH
CDRH127-6R1

R325
0.01

Do not stuff C304.

VCC2_5SBY_L
100-1%

R297
100-1%

MBRS130LT3
CR10

R301
100-1%

C304
100PF

R302
11K

R294
10K

C325 330UF
C326 330UF
T510

C295 68PF
C294 0.1UF
C296 330PF
C293 100PF

R295 10K
SBY_ITH_R

C292 100PF
C299 1000PF

C306 4.7UF
C307 0.1UF
C312 0.1UF

R259 35.7-1%
VCMOS1_8SBY

R258 100-1%
C263 0.1UF

VCC2_5SBY

Do not stuff C292.

VCC2_5SBY_SENSE+
VCC2_5SBY_SENSE-
VCC2_5SBY_VOSENSE

Power Connector

ITP Reset circuit. For debug only.

74LVC14A has 5V input tolerance.

VCC3_3SBY   VCC3_3SBY   VCC3_3SBY

U15 14   U15 14   U3 14
1   3   POK_U3
2 POK_U1   4 POK_U2   3
74LVC14A   74LVC14A   SN74LVC08A
2

DBRESET#

4   330 ohm pullup to VCC3_3 located on CPU sheet.

R339 0K

ATX Connector

VCC5SBY   VCC12-   VCC3_3

VCC3_3SBY
R347
4.7K
VCC5SBY
VCC5

VCC12

J24

U20 14 VCC
SLP_S3# 5   6 SLP_S3
GND
SN74LVC06A

9,29

11	3_3V11	3_3V1	1
12	-12V	3_3V2	2
13	GND13	GND3	3
14	PS_0N	ATX 5V4	4
15	GND15	GND5	5
16	GND16	5V6	6
17	GND17	GND7	7
18	-5V	PW_OK	8
19	5V19	5VSB	9
20	5V20	12V	10

SN74LVC06A has 5V output tolerance.

VCC2_5

VCC3_3SBY
R96
330

SN74LVC06A has 5V input tolerance.

U20 14 VCC
1   2 PWRGOOD 4
GND
SN74LVC06A

VCC5SBY

ATX_PWOK   R342   ATX_PWOK_R
0K

No stuff R342 when ITP is used.

U18
74LS132 14 VCC
9
10   8 PWROK_INV
7 GND

VCC3_3SBY
R349
4.7K

U20 14 VCC
3   4 PWROK 7,9,16,29
GND
SN74LVC06A

VCC3_3SBY

R348
1M No stuff.
For test only

Reset Button

VRM_PWRGD

4,28

220 ohm pullup to VCC3_3 is located on VRM sheet.

SW2

JP12

RSTBTN_SW   R343
22

C335   C328
0.01UF   10UF

VCC3_3SBY   VCC3_3SBY   VCC3_3SBY

R251
22K
RSMRST_U

U15 14   U15 14
5   9
6 RSMRST   8 RSMRST# 9,17
74LVC14A   74LVC14A

C266
1UF

R288
1M
No stuff.
For test only

Resume Reset circuitry
using a 22 msec delay
and Schmitt trigger logic.

PCI/AGP Pullups/Pulldowns

PCI

VCC5

RP6
8 [1] PIRQ#C 8,20,21
7 [2] PIRQ#D 8,20,21
6 [3]
5 [4]
2.7K

RP10
8 [1] FRAME# 8,16,20,21
7 [2] IRDY# 8,16,20,21
6 [3] TRDY# 8,16,20,21
5 [4] DEVSEL# 8,16,20,21
2.7K

RP11
8 [1] STOP# 8,16,20,21
7 [2] PLOCK# 8,20,21
6 [3] PERR# 8,16,20,21
5 [4] SERR# 8,16,20,21
2.7K

R112
PREQ#0 8,20   2.7K
R111
PREQ#1 8,20   2.7K
R115
PREQ#2 8,21   2.7K
R216
PREQ#3 8,16   2.7K
R213
PREQ#4 8   2.7K
R109
PREQ#5 8,21   2.7K

VCC3_3

RP16
8 [1] PGNT#1 8,20
7 [2] PGNT#0 8,20
6 [3] PGNT#3 8,16
5 [4] PGNT#2 8,21
8.2K

R214
PGNT#4 8   8.2K
R256
PGNT#5 8,21   8.2K
R114
REQ#A 8,21   8.2K
R105
GNT#A 8,21   8.2K
R81
PIRQ#A 8,16,19,20,2   8.2K
R89
PIRQ#B 8,19,20,21   8.2K

VCC5

R338
IRQ14 8,22   8.2K
R323
IRQ15 8,22   8.2K

VCC3_3

R235
SMBCLK_CORE 3,9,11   4.7K
R237
SMBDATA_CORE 3,9,11   4.7K

VCC3_3SBY

R236
SMB_ALERT 9   4.7K
R13
ALERTCLK_SBY 9,16   4.7K
R12
ALERTDATA_SBY 9,16   4.7K

PROCESSOR

VCC2_5

R128
PICD0 4,8   150
R124
PICD1 4,8   150
R84
FLUSH# 4   150
R85
STPCLK# 4,8   150
R94
SMI# 4,8   150
R123
FERR# 4,8   150

VCC2_5

R126
A20M# 4,8   150

RP7
8 [1] LINT0 4,8
7 [2] LINT1 4,8
6 [3] IGNNE# 4,8
5 [4] HINIT# 4,8,10
150

VCC2_5

R127
TESTHI 4   100K

R95
SLP# 4,8   150

R102
BREQ#0 4   10

VCC3_3

R324
KBRST# 8,12   8.2K
R327
A20GATE 8,12   8.2K
R314
SERIRQ 8,12,21   8.2K

AGP

VDDQ

RP15
8 [1] GIRDY# 7,19
7 [2] GDEVSEL# 7,19
6 [3] GPERR# 19
5 [4] GSERR# 19
8.2K

RP14
1 [8] GFRAME# 7,19
2 [7] GTRDY# 7,19
3 [6] GSTOP# 7,19
4 [5] GPAR 7,19
8.2K

RP9
8 [1]
7 [2] RBF# 7,19
6 [3] SBSTB# 7,19
5 [4] SBSTB 7,19
8.2K

GREQ# 7,19

RP8
1 [8]
2 [7] GGNT# 7,19
3 [6] PIPE# 7,19
4 [5] WBF# 7,19
8.2K

R198
ADSTB0 7,19   8.2K
R132
ADSTB1 7,19   8.2K

R505
ST0 7,19   8.2K
R506
ST1 7,19   8.2K
R507
ST2 7,19   8.2K

R207
ADSTB#0 7,19   8.2K
R136
ADSTB#1 7,19   8.2K

Rambus Termination

VCC1_8

TERM_DQA[8:0]   11

TERM_DQA0	R277	28
TERM_DQA1	R279	28
TERM_DQA2	R278	28
TERM_DQA3	R281	28

C280 0.1UF
C278 0.1UF
C281 0.1UF

TERM_DQA4	R280	28
TERM_DQA5	R283	28
TERM_DQA6	R282	28
TERM_DQA7	R285	28

C282 0.1UF
C283 0.1UF

TERM_DQB[8:0]   11

TERM_DQA8	R284	28
TERM_DQB0	R268	28
TERM_DQB1	R267	28
TERM_DQB2	R266	28

C273 0.1UF
C275 0.1UF

TERM_DQB3	R265	28
TERM_DQB4	R264	28
TERM_DQB5	R263	28
TERM_DQB6	R262	28

C274 0.1UF
C276 0.1UF

TERM_ROW[2:0]   11

TERM_DQB7	R261	28
TERM_DQB8	R260	28
TERM_ROW0	R275	28
TERM_ROW1	R274	28

C279 0.1UF
C271 0.1UF

TERM_COL[4:0]   11

TERM_ROW2	R276	28
TERM_COL0	R269	28
TERM_COL1	R271	28
TERM_COL2	R270	28

C269 0.1UF
C277 0.1UF

| TERM_COL3 | R273 | 28 |
| TERM_COL4 | R272 | 28 |

NOTE :

Use one 0.1uF cap
per two RSL signals.

Stuff C270,C272 with 0 ohm resistors.

VCC1_8

R293 90.9-1%
R291 90.9-1%

TERM_CMD   11
TERM_SCK   11

R292 39.2-1%
R290 39.2-1%

Decoupling

MCH Decoupling

VCC1_8

C157 0.1UF
C212 0.1UF
C201 0.01UF
C156 0.01UF
C213 0.01UF
C202 0.01UF
C221 0.1UF
C197 0.1UF

VCC1_8

C257 0.1UF
C265 0.1UF
C184 0.1UF
C260 0.1UF

Place these caps on solder side

VDDQ

C261 0.01UF
C262 0.01UF

Place these caps on solder side

For chipset decoupling, use 0.1UF and 0.01UF decoupling capacitor at each corner of the device. If there is room, add 0.01UF capacitors in the middle of each quad.

VDDQ

C344 0.01UF
C343 0.01UF
C166 0.01UF
C162 0.01UF
C367 0.01UF
C368 0.01UF

Place VDDQ capacitors within 70 mils of outer balls of MCH.

ICH Decoupling

VCC3_3

C253 0.1UF
C231 0.1UF
C232 0.1UF
C248 0.1UF
C254 0.01UF
C224 0.01UF
C230 0.01UF
C252 0.01UF

82559 Decoupling.

VCC3_3SBY

C30 0.1UF
C29 0.1UF
C60 0.1UF
C105 0.1UF
C88 4.7UF
C290 4.7UF

RIMM Decoupling

VCC2_5SBY

C303 100UF
C210 100UF
C285 100UF
C219 100UF
C258 0.1UF

VCC2_5SBY

C288 100UF
C284 100UF
C289 100UF
C302 100UF
C365 0.1UF
C366 0.1UF

VCMOS1_8SBY

C226 0.1UF
C264 0.1UF
C235 0.1UF

Place a VCMOS1_8SBY 0.1uF cap at each RIMM.

Place 100uF caps, 0.1 ohm ESR, among RIMM connectors.

Un-used Gates

VCC3_3SBY

U3 SN74LVC08A 9 10 14 8
U3 SN74LVC08A 12 13 14 11

VCC3_3SBY

U15 74LVC14A 11 14 10
U15 74LVC14A 13 14 12

VCC3_3SBY

VCC3_3SBY

U14 SN74LVC07A 9 14 VCC 8 GND
U14 SN74LVC07A 11 14 VCC 10 GND

VCC5SBY

U18 74LS132 2 14 VCC 3 7 GND
U18 74LS132 12 13 14 VCC 11 7 GND

VCC3_3SBY

U20 SN74LVC06A 9 14 VCC 8 GND
U20 SN74LVC06A 11 14 VCC 10 GND
U20 SN74LVC06A 13 14 VCC 12 GND

VCC3_3

U19 SN74LVC07A 3 14 VCC 4 GND
U19 SN74LVC07A 11 14 VCC 10 GND
U19 SN74LVC07A 13 14 VCC 12 GND

Decoupling

VCC3_3 Decoupling

VCC3_3

C216	0.1UF
C125	0.1UF
C143	0.1UF
C153	0.1UF
C154	0.1UF
C151	0.1UF
C181	0.1UF
C238	0.1UF
C188	0.1UF
C114	0.1UF

VCC3_3 Decoupling

VCC3_3

C310	0.1UF
C351	0.1UF
C146	0.1UF
C175	0.1UF
C145	0.1UF
C177	0.1UF
C144	0.1UF
C176	0.1UF
C178	0.1UF
C147	0.1UF

VCC2_5 Decoupling

VCC2_5

C172	0.1UF
C195	0.1UF
C106	0.1UF
C152	0.1UF
C163	0.1UF

Bulk Power Decoupling

VCC3_3

C330	0.1UF
C337	0.1UF

C338 1 + 2 22UF

VCC5

C332	0.1UF
C341	0.1UF

C342 1 + 2 22UF

VCC12

C345	0.1UF
C334	0.1UF

C346 1 + 2 22UF

VCC12-

C339	0.1UF
C331	0.1UF
C36	0.1UF
C89	0.1UF

C340 2 + 1 22UF

Core Voltage Decoupling

VCCVID

C137	10UF
C136	10UF
C131	10UF
C139	10UF
C134	10UF

VCCVID

C135	10UF
C141	10UF
C132	10UF
C138	10UF
C133	10UF

VCC3_3SBY

C357	0.1UF
C65	0.1UF
C259	0.1UF
C64	0.1UF
C240	0.1UF

Termination Decoupling

VTT1_5

C127	0.1UF
C129	0.1UF
C150	0.1UF
C149	0.1UF
C128	0.01UF
C130	0.01UF
C115	0.01UF
C148	0.01UF

Place caps at VTT pins on Slot 1 connector.

Revision History

Revision 1.01

Pg 6   Modified MCH_AGPREF circuit, changed 432 ohm to 1K ohm and 62 ohm to 80.6 ohm.
Changed value of capacitor C194 from 0.1uF to 0.01uF.

Pg 8   Modified HUBREF circuit, deleted R222, R223 & C217, changed C218 from 470pF to 0.1uF.

Pg 11   Modified RIMM connectors to eliminate 3.3V, added 0.1uF decoup caps to SVDDA & SVDDB on each RIMM.

Pg 33   Modified CMD and SCK termination values. Removed 470pF capacitors, Changed 93 ohm to 90.9 ohm,
and changed 39 ohm to 39.2 ohm resistors.

Pg 34   Deleted 3.3V decoupling for RIMM connectors. Added solder side decoup for MCH.
Changed VDDQ cap values from 0.1uF to 0.01uF.

Hub Link Connector
For debug only.

J26   PROBE CONNECTOR

5	TEST_CLK66
7,8	HL0
7,8	HL1
7,8	HL2
7,8	HL3
7,8	HL9
7,8	HL_STB
7,8	HL_STB#
7,8	HL10
7,8	HL8
7,8	HL4
7,8	HL5
7,8	HL6
7,8	HL7

HUBREF   6,8

VCC1_8

P08-050-SL-A-G

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD

REV: 1.01

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B
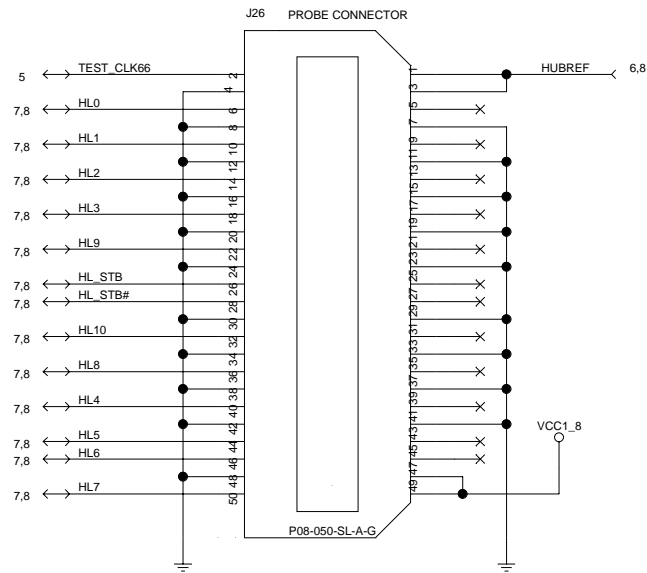
Reference Board
Schematics: Dual-Processor

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intel

Reference Design Schematics: Dual-Processor B

B.1 Reference Design Feature Set

The reference schematics feature the following core feature set:

- Intel® 820 Chipset
    - Memory Controller Hub (MCH)
    - I/O Controller Hub (ICH)
    - FWH Flash BIOS interface
- Support for the two Pentium III (SC242) Processors
    - 100/133 MHz System Bus Frequency
    - Debug Port
- IOAPIC Integrated into the ICH
- Direct RDRAM Memory Interface
    - 266 MHz, 300 MHz, 356 MHz and 400 MHz Direct RDRAM Support
    - 2 RIMM Sockets
- 4 PCI Add-in Slots
    - Via 4 REQ/GNT pairs (ICH supports 6 REQ#/GNT# pairs)
- AGP Universal Connector
    - 3.3V - 1X,2X signaling
    - 1.5V – 1X, 2X, 4X signaling
- 2 IDE Connectors with Ultra ATA/66 Support
- 2 USB Connectors
- ATX Power Connector
- LPC Ultra I/O
    - Floppy Disk Controller
    - 1 Parallel Port, 2 Serial Ports
    - Keyboard Controller
- AC'97 Bus Connector and Audio Codec
- WfM Support
- Integrated System Management
- Integrated Power Management
    - ACPI Rev. 1.0 Compliant
    - APM Rev. 1.2 Compliant
- Pentium III on-board VRM 8.4 compliant regulator
- 4 Layer Design

INTEL(R) 820 CHIPSET
DUAL PROCESSOR CUSTOMER REFERENCE SCHEMATICS

Note that these schematics are preliminary and are subject to change.

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TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03

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SHEET: 1 OF 38

Block Diagram
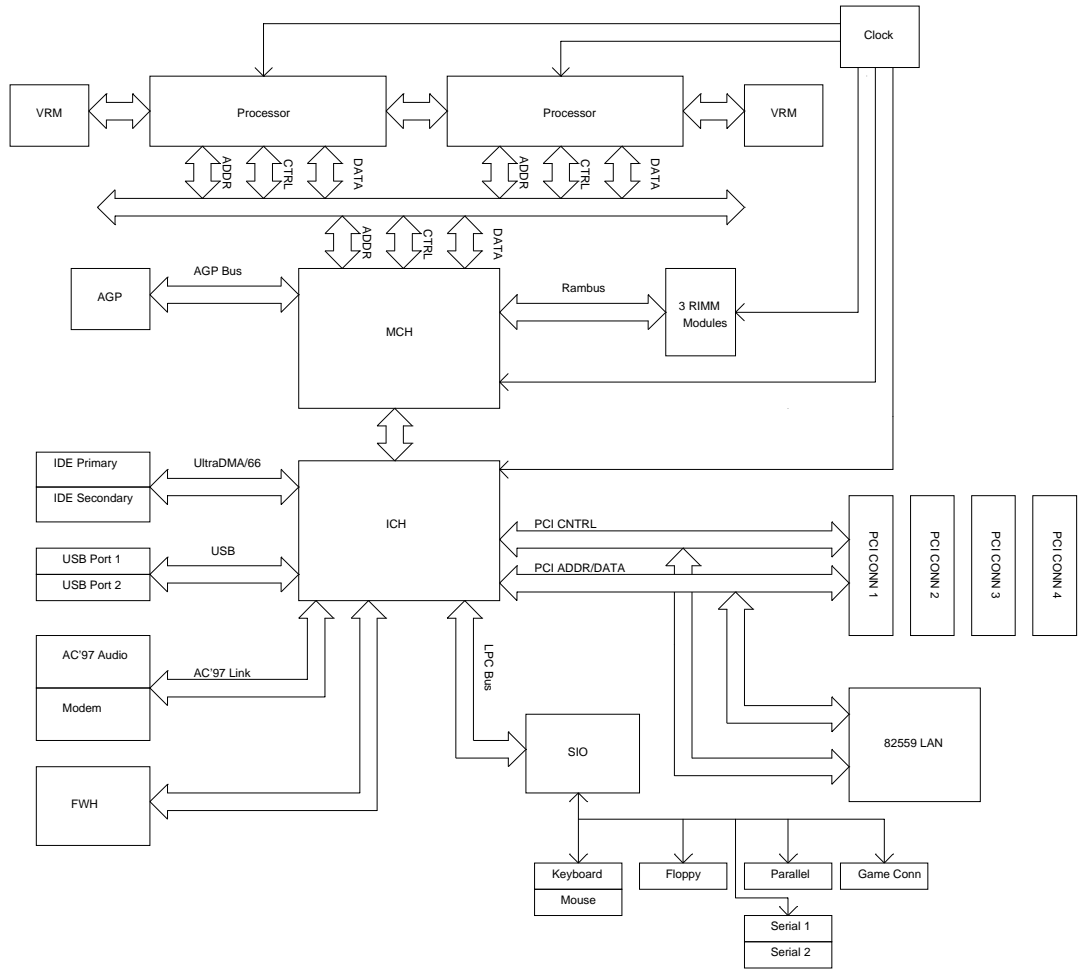
Device Table

REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U20	74LVC06A	A, B, C, D, E, F	33, 36
U14	74LVC07A	A, B, C, D, E, F	9,20,31,36
U19	74LVC07A	A, B, C, D, E, F	20,24,36
U3	74LVC08A	A, B, C, D	36, 33, 17
U9	74LVC08A	A, B	33
U26	74LVC08A	A	33
U15	74LVC14a	A, B, C, D, E, F	33, 36
U23	74LVC14a	A, B, C, D	33
U18	74LS132	A, B, C, D	31, 33, 36
U22	74LVC07A	A, B	33
U25	74F74	A, B	4
U13	82801 (ICH)		10, 11
U10	82820 (MCH)		8, 9
U5	82559		18
U24	93C46A		18
U2	AD1881		15
U11	CK133		7
U12	DRCG		7
U16	FWH		12
U4, U6	GD75232		27
U1	LM4880		16
U17	LPC47B27X		14
U21	ADM1021		3
U8	ADM1021		5
U7	TPS2042		25

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD
BLOCK DIAGRAM

REV: 3.03

PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY:

PROJECT:

LAST REVISED: 11-29-1999_14:43

SHEET: 2 OF 38

Processor Connector 0

HD#[63:0] 5,8

HA#[31:0] 5,8

J15

SC242

Signal	Pin	Signal
HD#0	B72	HD#0
HD#1	A73	HD#1
HD#2	B71	HD#2
HD#3	A72	HD#3
HD#4	B70	HD#4
HD#5	A71	HD#5
HD#6	B68	HD#6
HD#7	B67	HD#7
HD#8	A69	HD#8
HD#9	A68	HD#9
HD#10	A65	HD#10
HD#11	A64	HD#11
HD#12	B66	HD#12
HD#13	A63	HD#13
HD#14	A67	HD#14
HD#15	B64	HD#15
HD#16	A61	HD#16
HD#17	B63	HD#17
HD#18	B60	HD#18
HD#19	B59	HD#19
HD#20	B62	HD#20
HD#21	A60	HD#21
HD#22	B58	HD#22
HD#23	A59	HD#23
HD#24	A57	HD#24
HD#25	B56	HD#25
HD#26	B55	HD#26
HD#27	A56	HD#27
HD#28	B52	HD#28
HD#29	B54	HD#29
HD#30	A55	HD#30
HD#31	A53	HD#31
HD#32	B51	HD#32
HD#33	A51	HD#33
HD#34	B48	HD#34
HD#35	A52	HD#35
HD#36	B46	HD#36
HD#37	A49	HD#37
HD#38	B50	HD#38
HD#39	A45	HD#39
HD#40	B47	HD#40
HD#41	B42	HD#41
HD#42	A43	HD#42
HD#43	A48	HD#43
HD#44	B44	HD#44
HD#45	A44	HD#45
HD#46	A39	HD#46
HD#47	B43	HD#47
HD#48	B39	HD#48
HD#49	A40	HD#49
HD#50	B35	HD#50
HD#51	A41	HD#51
HD#52	B40	HD#52
HD#53	A36	HD#53
HD#54	B36	HD#54
HD#55	A33	HD#55
HD#56	B34	HD#56
HD#57	A37	HD#57
HD#58	B31	HD#58
HD#59	B38	HD#59
HD#60	A35	HD#60
HD#61	A32	HD#61
HD#62	B30	HD#62
HD#63	B32	HD#63

Signal	Pin	Signal
HA#3	B98	HA#3
HA#4	A100	HA#4
HA#5	A97	HA#5
HA#6	B99	HA#6
HA#7	B96	HA#7
HA#8	B95	HA#8
HA#9	A99	HA#9
HA#10	A96	HA#10
HA#11	B92	HA#11
HA#12	B94	HA#12
HA#13	A93	HA#13
HA#14	A95	HA#14
HA#15	B90	HA#15
HA#16	A92	HA#16
HA#17	B91	HA#17
HA#18	A91	HA#18
HA#19	A89	HA#19
HA#20	B86	HA#20
HA#21	B87	HA#21
HA#22	A85	HA#22
HA#23	A87	HA#23
HA#24	B83	HA#24
HA#25	B88	HA#25
HA#26	B82	HA#26
HA#27	A84	HA#27
HA#28	B84	HA#28
HA#29	B80	HA#29
HA#30	A81	HA#30
HA#31	A83	HA#31
HA#32	B79	
HA#33	A79	
HA#34	A80	
HA#35	B78	

Signal	Pin	Signal
VID0	B120	VID0
VID1	A120	VID1
VID2	A119	VID2
VID3	B119	VID3
VID4	A121	VID4

VID[4:0] 30

Signal	Pin	Signal
RS#0	B108	RS#0
RS#1	A112	RS#1
RS#2	B111	RS#2

RS#[2:0] 5,8

RSP# B115

Signal	Pin	Signal
REQ#0	B102	HREQ#0
REQ#1	B103	HREQ#1
REQ#2	A107	HREQ#2
REQ#3	A108	HREQ#3
REQ#4	B104	HREQ#4

HREQ#[4:0] 5,8

RP# B114

THRMDN B15 THRMDN_R   R19 0K   THRMDN
THRMDP B14 THRMDP_R   R100 0K   THRMDP

RESERVED3 B12
RESERVED2 A116
RESERVED1 A88
RESERVED0 A47

THRMDP and THRMDN signals must be disconnected from onboard thermal sensor during SECC2 thermal testing of the processor. Please see the "Pentium(R) II processor Single Edge Contact Cartridge 2 Thermal Validation" document for further details.
Place R19, R100 very close to processor.

U21
ADM1021

VCC3_3
VCC3_3
VCC2 2

Pin	Signal
3	DXP
4	DXN
1	NC1
5	NC5
9	NC9
13	NC13
16	NC16
15	STBY#
10	ADD0
6	ADD1
14	SMBCLK
12	SMBDATA
11	ALERT#

GND8 GND7 8 7

SMBCLK_CORE 5,11,13,34
SMBDATA_CORE 5,11,13,34
THRM# 5,11

Processor Connector 0

ITP

SC242

ITP Config	JP33	JP34
Single CPU0	1-2	1-2
Dual CPU	2-3	1-2
Single CPU1	2-3	2-3

R7 and R11 should be placed within 1" of ITP connector.

CPU TACH0

Processor Connector 1

HD#[63:0]

3,8

HA#[31:0]

3,8

J120

SC242

Signal	Pin	Signal
HD#0	B72	HD#0
HD#1	A73	HD#1
HD#2	B71	HD#2
HD#3	A72	HD#3
HD#4	B70	HD#4
HD#5	A71	HD#5
HD#6	B68	HD#6
HD#7	B67	HD#7
HD#8	A69	HD#8
HD#9	A68	HD#9
HD#10	A65	HD#10
HD#11	A64	HD#11
HD#12	B66	HD#12
HD#13	A63	HD#13
HD#14	A67	HD#14
HD#15	B64	HD#15
HD#16	A61	HD#16
HD#17	B63	HD#17
HD#18	B60	HD#18
HD#19	B59	HD#19
HD#20	B62	HD#20
HD#21	A60	HD#21
HD#22	B58	HD#22
HD#23	A59	HD#23
HD#24	A57	HD#24
HD#25	B56	HD#25
HD#26	B55	HD#26
HD#27	A56	HD#27
HD#28	B52	HD#28
HD#29	B54	HD#29
HD#30	A55	HD#30
HD#31	A53	HD#31
HD#32	B51	HD#32
HD#33	A51	HD#33
HD#34	B48	HD#34
HD#35	A52	HD#35
HD#36	B46	HD#36
HD#37	A49	HD#37
HD#38	B50	HD#38
HD#39	A45	HD#39
HD#40	B47	HD#40
HD#41	B42	HD#41
HD#42	A43	HD#42
HD#43	A48	HD#43
HD#44	B44	HD#44
HD#45	A44	HD#45
HD#46	A39	HD#46
HD#47	B43	HD#47
HD#48	B39	HD#48
HD#49	A40	HD#49
HD#50	B35	HD#50
HD#51	A41	HD#51
HD#52	B40	HD#52
HD#53	A36	HD#53
HD#54	B36	HD#54
HD#55	A33	HD#55
HD#56	B34	HD#56
HD#57	A37	HD#57
HD#58	B31	HD#58
HD#59	B38	HD#59
HD#60	A35	HD#60
HD#61	A32	HD#61
HD#62	B30	HD#62
HD#63	B32	HD#63

Signal	Pin	Signal
HA#3	B98	HA#3
HA#4	A100	HA#4
HA#5	A97	HA#5
HA#6	B99	HA#6
HA#7	B96	HA#7
HA#8	B95	HA#8
HA#9	A99	HA#9
HA#10	A96	HA#10
HA#11	B92	HA#11
HA#12	B94	HA#12
HA#13	A93	HA#13
HA#14	A95	HA#14
HA#15	B90	HA#15
HA#16	A92	HA#16
HA#17	B91	HA#17
HA#18	A91	HA#18
HA#19	A89	HA#19
HA#20	B86	HA#20
HA#21	B87	HA#21
HA#22	A85	HA#22
HA#23	A87	HA#23
HA#24	B83	HA#24
HA#25	B88	HA#25
HA#26	B82	HA#26
HA#27	A84	HA#27
HA#28	B84	HA#28
HA#29	B80	HA#29
HA#30	A81	HA#30
HA#31	A83	HA#31
HA#32	B79	
HA#33	A79	
HA#34	A80	
HA#35	B78	

VID0	B120	VID1[0]
VID1	A120	VID1[1]
VID2	A119	VID1[2]
VID3	B119	VID1[3]
VID4	A121	VID1[4]

VID1[4:0] 30

RS#0	B108	RS#0
RS#1	A112	RS#1
RS#2	B111	RS#2

RS#[2:0] 3,8

RSP# B115

REQ#0	B102	HREQ#0
REQ#1	B103	HREQ#1
REQ#2	A107	HREQ#2
REQ#3	A108	HREQ#3
REQ#4	B104	HREQ#4

HREQ#[4:0] 3,8

RP# B114

| THRMDN | B15 | THRMDN1_R |
| THRMDP | B14 | THRMDP1_R |

R121 0K   THRMDN1
R122 0K   THRMDP1

RESERVED3	B12	
RESERVED2	A116	
RESERVED1	A88	
RESERVED0	A47	

VCC3_3   VCC3_3

U8
ADM1021

VCC2 2

| 3 | DXP |
| 4 | DXN |

1	NC1
5	NC5
9	NC9
13	NC13
16	NC16

STBY#	15
ADD0	10
ADD1	6
SMBCLK	14	SMBCLK_CORE	3,11,13,34
SMBDATA	12	SMBDATA_CORE	3,11,13,34
ALERT#	11	THRM#	3,11

GND8 GND7

THRMDP and THRMDN signals must be disconnected from onboard thermal sensor
during SECC2 thermal testing of the processor. Please see the "Pentium(R) II processor Single Edge
Contact Cartridge 2 Thermal Validation" document for further details.
Place R121, R122 very close to processor.

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV:
PROCESSOR CONNECTOR   3.03

intel® PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY: PROJECT:

LAST REVISED: SHEET:
11-30-1999_9:57   5 OF 38

Processor Connector 1

CPU TACH1

SC242

VCC5 VCC5 VCC5

R101 2.7K   R102 2.7K

CPUHCLK 4,7

U25
2 D1 VCC 14
3 CLK1 Q1 5
1 CLR1# Q1# 6
4 PR1#
12 D2 Q2 9
11 CLK2 Q2# 8
13 CLR2#
10 PR2# GND 7
74F74

R392 1K

Q16 2N3904

BREQ#0 4,6

VCC3_3

R390 8.2K

Q17 2N3904

CPURST# 4,6,8   R103 4.7K

VCC12

C110 0.1UF

JP32
1
2
3

J120
A1 VTT1
A3 VTT2
B5 VTT3
B9 VTT4
B13 VCCP1
B17 VCCP2
B25 VCCP3
B29 VCCP4
B33 VCCP5
B37 VCCP6
B45 VCCP7
B49 VCCP8
B53 VCCP9
B57 VCCP10
B65 VCCP11
B69 VCCP12
B73 VCCP13
B77 VCCP14
B85 VCCP15
B89 VCCP16
B93 VCCP17
B97 VCCP18
B105 VCCP19
B109 VCC5
B113 VCC3_3
B117 VCC3_1
B121 VCC3_2

VTT1_5   VCCVID1   VCC5   VCC3_3

A25 DEP#0
A27 DEP#1
B26 DEP#2
A28 DEP#3
B27 DEP#4
A29 DEP#5
A31 DEP#6
B28 DEP#7

B19 BP2#
A21 BP3#
A23 BPM0#
B24 BPM1#
A24 BINIT#   BINIT# 4

PICD0 A19 PICD0 4,10,34
PICD1 B22 PICD1 4,10,34
PICCLK1 B18 PICCLK 7

SLOTOCC1# B101 SLOTOCC# 33
TDO_0 A9 TDI 4
TDO_1 A11 TDO 4
TRST# B11 TRST# 4
TCK_R B7 TCK 4 R395 47
TMS_R B10 TMS1 4 R391 47

EMI1_1 B61 EMI_1
EMI1_2 B100 EMI_2
EMI1_3 B81 EMI_3
EMI1_4 B1 EMI_4
EMI1_5 B41 EMI_5

R138 0K R139 0K R140 0K R142 0K R145 0K

CPUHCLK1 A75 BCLK 7
PWRGOOD A12 PWRGOOD 4,33
CPURST# B74 RESET# 4,6,8

A117 AP0#
B116 AP1#
A101 BNR#   BNR# 4,8
A103 BPRI#   BPRI# 4,8
A104 TRDY#   HTRDY# 4,8
A105 DEFER#   DEFER# 4,8
B106 LOCK#   HLOCK# 4,8
B107 DRDY#   DRDY# 4,8
A109 HITM#   HITM# 4,8
B110 HIT#   HIT# 4,8
A111 DBSY#   DBSY# 4,8
A115 HADS#   HADS# 4,8

A20 PREQ#   ITPREQ1# 4
B23 PRDY#   ITPRDY1# 4
A76 BREQ0#   BREQ#1 4
B75 BREQ1#   BREQ#0 4,6
B76 RES4
A13 TESTHI   TESTHI1 34
B21 BSEL0
A14 BSEL1   SEL133/100# 4,7,9
B2 FLUSH#   FLUSH# 4,34

A15 THMTRP#

A5 A20M#   A20M# 4,10,34
B6 STPCLK#   STPCLK# 4,10,34
B8 SLP#   SLP# 4,10,34
B3 SMI#   SMI# 4,10,34
A17 LINT0   LINT0 4,10,34
B16 LINT1   LINT1 4,10,34
B4 INIT#   HINIT# 4,10,34
A7 FERR#   FERR# 4,10,12,34
A8 IGNNE#   IGNNE# 4,10,34
A4 IERR#
A77 BERR#
B118 AERR#
A16 RES0
B20 RES1
B112 RES2
A113 RES3

R389 220

VCC3_3

GND0...GND29

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
PROCESSOR CONNECTOR
intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-29-1999_14:45
SHEET: 6 OF 38

Clock Synthesizer

VCC3_3

Provide at least one 0.1uF decoupling cap per power pin.

VCC2_5

L20 FBHS01L 1 2
L21 FBHS01L 1 2

VCC_3_3_CK133_FB
VCC2_5_CK133_FB

C207 C215 C223 C186 C198 C206 C214 C170
0.1UF 0.1UF 0.1UF 0.1UF 0.1UF 0.1UF 0.1UF 10UF

C180 C190 C192 C199 C171
0.1UF 0.1UF 0.1UF 0.1UF 10UF

U11 CK133

Y3 XTAL 14.318MHZ
C185 10PF   C189 10PF

CK133_XIN
CK133_XOUT

VCC3_3

R206 10K R203 10K R202 10K R197 10K R196 10K R192 10K R224 220

5 XTAL_IN
6 XTAL_OUT

VDD3V_1 VDD3V_2 VDD3V_3 VDD3V_5 VDD3V_6 VDD3V_7
VDD25V_1 VDD25V_2 VDD25V_3 VDD25V_4

2.5V

APIC0 53 PICCLK_R R155 22 PICCLK 4
APIC1 54 APICCLK_R R156 22 APICCLK 10
APIC2 55 PICCLK1_R R148 22 PICCLK1 6
CPU_DIV2_1 50 CPU_DIV2_1_R R151 22 CPU_DIV2
CPU_DIV2_2 49 CPU_DIV2_2_R
CPUCLK0 41 ITPCLK_R R188 22 ITPCLK 4
CPUCLK1 42 CPUHCLK_R R189 22 MCHCLK 8
CPUCLK2 45 R184 22 CPUHCLK 4,6
CPUCLK3 46 CPUHCLK1_R R170 22 CPUHCLK1

PCICLK_F 8 ICHPCLK_R R165 33 ICHPCLK 10
PCICLK1 9 PCLK1_R R164 33 PCLK1 22
PCICLK2 11 PCLK2_R R169 33 PCLK2 22
PCICLK3 12 PCLK3_R R183 33 PCLK3 23
PCICLK4 14 PCLK4_R R186 33 PCLK4 23
PCICLK5 15 PCLK5_R R187 33 PCLK5 18
PCICLK6 17 FWHPCLK_R R191 33 FWHPCLK 12
PCICLK7 18 SIO_PCLK7_R R194 SIO_PCLK7
3V66_0 21 MCH_CLK66 R33 R201 AGPCLK_CONN 21
3V66_1 22 R195 33 MCH_CLK66 9
3V66_2 25 ICH_CLK66_R R210 33 ICH_CLK66 11
3V66_3 26 TEST_CLK66_R R211 33 TEST_CLK66 11
48MHZ 30 IHC_48MHZ_R R221 22 ICH_48MHZ 11
REF0 1 IHC_14MHZ_R R147 22 ICH_14MHZ 11
REF1 3 SIO_14MHZ_R R150 22 SIO_14MHZ 14

R166 30

28 SEL133/100#   4,6,9 SEL133/100#
37 PCISTOP#   PCISTOP#
36 CPUSTOP#   CPUSTOP#
35 PWRDWN#   CK133_PWRDWN#
34 SPREAD#   SPREAD#
33 SEL1   SEL1
32 SEL0   SEL0

VSS1 VSS2 VSS3 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12

JP17 JP15 JP14

VCC3_3

Keep stubs on unused outputs as short as possible.
Tie CPUCLK and MCHCLK outputs together.

VDDIR pin on DRCG should be decoupled at the component with a 0.1uF cap.
CLKTM and CLKTM# RC network must use 5% or better tolerance components.

VCC2_5   VCC1_8   VCC3_3

L22 FBHS01L 1 2

VCC3_3_DRCG_FB

C208 C196 C204 C220 C209
0.1UF 0.1UF 0.1UF 0.1UF 10UF

U12 DRCG

VDDIR VDDIPD VDDO1 VDDO2 VDDP VDDC

MULT0_GPIO 11
R219 10K R204 10K R199 10K

REFCLK 2
DRCG_PWRDWN# 12 PWRDN#
STOPB# 11 STOPB#
MULT0 15 MULT0
MULT1 14 MULT1
24 S0
23 S1
13 GND
HCLKOUT 6 PCLKM
RCLKOUT 7 SYNCLKN
NC 19

CLK 20 DRCG_CLK R182 39-1% CLKTM 13
CLKB# 18 DRCG_CLKB# R185 51-1% R200 51-1% C80 4PF

GND01 GND02 GNDP GNDC GNDI

No stuff R106 for debug.
VCC1_8

R220 33

JP13 is for debug only. JP13
1 2 3

VCC3_3
R161 10K R217 10K

DRCG_CTRL 11

JP11

No stuff R161, JP11.

MULT1_GPIO 11,14 JP18
1 2 3

R205 39-1%
CLKTM_RD
CLKTM# 13
No stuff C80
C205 0.1UF

HOST

HOST BUS/RAMBUS	JP13	JP18
100/300	2-3	OUT
100/400	OUT	OUT
133/400	2-3	OUT
GPO CNTRL*	1-2	OUT

Sprd Spect	JP14
Enabled*	IN
Disabled	OUT

SEL133/100#	JP15	JP17	Function
0	IN	IN	All outputs Tri-State
0	IN	OUT	Reserved
0	OUT	IN	Active 100MHz, 48MHz PLL inactive
0	OUT	OUT	Active 100MHz, 48MHz PLL active
1	IN	IN	Test Mode
1	IN	OUT	Reserved
1	OUT	IN	Active 133MHz,48MHz PLL inactive
1	OUT	OUT	Active 133MHz,48MHz PLL active*

All jumpers may not be required, but are included for test purposes.

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
CLOCK SYNTHESIZER

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
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LAST REVISED: 11-29-1999_14:46   SHEET: 7 OF 38

MCH

10   HUBREF
C194   21
0.01UF
C155
0.1UF

CONN_AGPREF

RAMREF_R   R168   100-1%   RAMREF   8,13
C191   0.1UF
C203   0.1UF

GTLREF2   8
GTLREF1   8

U10
MCH_096

VTT1_5   VTT1_5
R131 75-1%   R143 75-1%
GTLREF2   GTLREF1
C158   C183
R130 150-1%   0.001UF   R144 150-1%   0.001UF

HD#[63:0]   3,5

Signal	Pin
HD#0	R2
HD#1	R1
HD#2	R4
HD#3	P5
HD#4	T1
HD#5	R5
HD#6	V1
HD#7	Y2
HD#8	W1
HD#9	U1
HD#10	T2
HD#11	Y3
HD#12	W2
HD#13	U3
HD#14	Y1
HD#15	U2
HD#16	W4
HD#17	W3
HD#18	V4
HD#19	U4
HD#20	T3
HD#21	Y4
HD#22	Y5
HD#23	T4
HD#24	V5
HD#25	T5
HD#26	Y6
HD#27	W5
HD#28	U6
HD#29	V6
HD#30	W6
HD#31	T6
HD#32	W7
HD#33	U7
HD#34	Y8
HD#35	Y7
HD#36	T8
HD#37	W8
HD#38	T7
HD#39	W9
HD#40	U8
HD#41	W10
HD#42	Y10
HD#43	V8
HD#44	U9
HD#45	Y9
HD#46	W11
HD#47	T9
HD#48	Y11
HD#49	T10
HD#50	T12
HD#51	U10
HD#52	V10
HD#53	W12
HD#54	T11
HD#55	U13
HD#56	Y13
HD#57	Y12
HD#58	W14
HD#59	U11
HD#60	U12
HD#61	Y14
HD#62	V14
HD#63	W13

HUBREF   E20
AGPREF   U14
RAMREFB   E10
RAMREFA   E11
GTLREFB   C3
GTLREFA   V12

HA#[31:0]   3,5

Signal	Pin
HA#3	J1
HA#4	H3
HA#5	H4
HA#6	G5
HA#7	K2
HA#8	H5
HA#9	H2
HA#10	J4
HA#11	L1
HA#12	J5
HA#13	K1
HA#14	J2
HA#15	K5
HA#16	K3
HA#17	L4
HA#18	K4
HA#19	L2
HA#20	N2
HA#21	M3
HA#22	M2
HA#23	M1
HA#24	N5
HA#25	M4
HA#26	P1
HA#27	N1
HA#28	P2
HA#29	P3
HA#30	N4
HA#31	M5

VDDQ
C187 470PF   MCH_AGPREF_CV
R154 1K-1%   R160 80.6-1%
MCH_AGPREF   21
R149 1K-1%   R153 80.6-1%
C182 470PF   MCH_AGPREF_CG

Place MCH_AGPREF circuit near the MCH.

HOST   HOST

Signal	Pin	
CPURST#	P4	4,6
ADS#	D2	HADS# 4,6
BNR#	F5	4,6
BPRI#	G1	4,6
DBSY#	D1	4,6
DEFER#	F2	4,6
DRDY#	F1	4,6
HIT#	D3	4,6
HITM#	E1	4,6
HLOCK#	F3	4,6
HTRDY#	F4	4,6

RS#[2:0]   3,5
RS#0   E5
RS#1   C1
RS#2   E2

HREQ#[4:0]   3,5
HREQ#0   H1
HREQ#1   G4
HREQ#2   E4
HREQ#3   E3
HREQ#4   G2

VCC1_8
R180 40.2-1%

HCLKIN   V2   MCHCLK   7
RSTIN#   F20   PCIRST#   10,12,13,14,18,21,22,23,24
HLCOMP   A18   MCH_HLCOMP
TEST/GRCOMP   T15   GRCOMP   R129 40.2-1%

Place R129 and R180 less than 0.5" from MCH using 10 mil trace.

VCC1_8
R190 162-1%
RAMREF   8,13
R181 562-1%

VCC1_8:E6,D4,E6,F6,G6,E7,R6,R7,E8,E9,D10,D11,E12
VCC1_8:E13,E14,F14,T14,E15,P15,B17,C17,C19
VDDQ:F15,R15,J17,L17,N17,T17
GND:A1,A3,G3,J3,L3,N3,R3,V3,B4,D5,L5,U5,B6,D6,D7,V7,B8,D8
GND:D9,J9,K9,L9,M9,V9,B10,J10,K10,L10,M10,C11,J11,K11,L11
GND:M11,V11,C12,D12,J12,K12,L12,M12,B13,D13,V13,T13,D14
GND:B15,D15,B16,D16,E16,F16,A17,E18,V18,A19,H19,K19,M19
GND:P19,T19,D20

MCH

U10
MCH_096

GAD[31:0]

21 ←

GAD0	F17	G_AD0
GAD1	G18	G_AD1
GAD2	G17	G_AD2
GAD3	G19	G_AD3
GAD4	G16	G_AD4
GAD5	G20	G_AD5
GAD6	H17	G_AD6
GAD7	H18	G_AD7
GAD8	J20	G_AD8
GAD9	J16	G_AD9
GAD10	K17	G_AD10
GAD11	K18	G_AD11
GAD12	J18	G_AD12
GAD13	L19	G_AD13
GAD14	K20	G_AD14
GAD15	L18	G_AD15
GAD16	M17	G_AD16
GAD17	P18	G_AD17
GAD18	M16	G_AD18
GAD19	P17	G_AD19
GAD20	N16	G_AD20
GAD21	P20	G_AD21
GAD22	P16	G_AD22
GAD23	R20	G_AD23
GAD24	T20	G_AD24
GAD25	R17	G_AD25
GAD26	U17	G_AD26
GAD27	T16	G_AD27
GAD28	U18	G_AD28
GAD29	T18	G_AD29
GAD30	U20	G_AD30
GAD31	U19	G_AD31

AGP

GC/BE#[3:0]

21 ←

GC/BE#0	H16	G_C/BE#0
GC/BE#1	L20	G_C/BE#1
GC/BE#2	N18	G_C/BE#2
GC/BE#3	R16	G_C/BE#3

21,34 ←	GFRAME#	L16	G_FRAME#
21,34 ←	GDEVSEL#	N19	G_DEVSEL#
21,34 ←	GIRDY#	N20	G_IRDY#
21,34 ←	GTRDY#	M20	G_TRDY#
21,34 ←	GSTOP#	M18	G_STOP#
21,34 ←	GPAR	K16	G_PAR
21,34 →	GREQ#	U15	G_REQ#
21,34 ←	GGNT#	Y16	G_GNT#
21,34 →	PIPE#	W16	PIPE#

| 7 | MCH_CLK66 | W18 | CLK66 |

| 21,34 ← | RBF# | V16 | RBF# |
| 21,34 ← | WBF# | V15 | WBF# |

	ST0	W15	ST0
	ST1	Y15	ST1
ST[2:0]	ST2	Y17	ST2

21 ←

21,34 ←	ADSTB0	J19	AD_STB0
21,34 ←	ADSTB#0	H20	AD_STB#0
21,34 ←	ADSTB1	R18	AD_STB1
21,34 ←	ADSTB#1	R19	AD_STB#1
21,34 →	SBSTB	Y20	SB_STB
21,34 →	SBSTB#	Y19	SB_STB#

AGP

HUB

HL0	F19	HL0
HL1	F18	HL1
HL2	E17	HL2
HL3	E19	HL3
HL4	B20	HL4
HL5	B19	HL5
HL6	B18	HL6
HL7	A20	HL7
HL8	D17	HL8
HL9	C18	HL9
HL10	D18	HL10

HL[10:0] → 10

9,10 ← HL10 ●—— R209 8.2K —— SEL133/100# → 4,6,7

R227 8.2K

| HL_STB | D19 | HL_STB | ↔ 10 |
| HL_STB# | C20 | HL_STB# | ↔ 10 |

| RCLKOUT | B1 | RCLKOUT | → 7 |
| HCLKOUT | A2 | HCLKOUT | → 7 |

VCC3_3SBY

DQA0	A13	LDQA0
DQA1	C13	LDQA1
DQA2	A14	LDQA2
DQA3	C14	LDQA3
DQA4	B14	LDQA4
DQA5	C15	LDQA5
DQA6	A15	LDQA6
DQA7	C16	LDQA7
DQA8	A16	LDQA8

LDQA[8:0] → 13

VCC3_3SBY

R248 4.7K

U14
11,18,31,33 PWROK 13   VCC 12 PWROK_CTRL 9
SN74LVC07A GND

DQB0	C7	LDQB0
DQB1	B7	LDQB1
DQB2	C6	LDQB2
DQB3	A6	LDQB3
DQB4	C5	LDQB4
DQB5	A5	LDQB5
DQB6	B5	LDQB6
DQB7	A4	LDQB7
DQB8	C4	LDQB8

LDQB[8:0] → 13

MEMORY

LSCK and LCMD must neck down to 5 mils for 175 mils at Q10 and Q9 attach points. Place Q10 and Q9 as close as possible to MCH.

VCC5SBY

RQ0	A7	LCOL0
RQ1	C8	LCOL1
RQ2	A8	LCOL2
RQ3	C9	LCOL3
RQ4	B9	LCOL4

LCOL[4:0] → 13

RQ5	A9	LROW0
RQ6	A10	LROW1
RQ7	C10	LROW2

LROW[2:0] → 13

R346 4.7K

LSCK ↔ 13

Q10
MMBT3904LT1

SCK_CTRL

CTM	B11	LCLKTM	→ 13
CTM#	A11	LCLKTM#	→ 13
CFM	A12	LCLKFM	→ 13
CFM#	B12	LCLKFM#	→ 13

9 PWROK_CTRL B

Q14
MMBT3904LT1

CMD	B3
SCK	B2
SIO	C2	LSIO	→ 13

LCMD 13

Q9
MMBT3904LT1

SBA0	W20	SBA0
SBA1	V17	SBA1
SBA2	Y18	SBA2
SBA3	W17	SBA3
SBA4	V20	SBA4
SBA5	W19	SBA5
SBA6	V19	SBA6
SBA7	U16	SBA7

SBA[7:0] → 21

VCC1_8

C361 0.1UF
C359 0.1UF
C360 0.1UF
C362 0.1UF

No stuff. For test only.

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ICH

U13
ICH_096

ICH_A

AD[31:0] 18,22,23

Pin	Signal
G2	AD0
G4	AD1
F2	AD2
F3	AD3
F4	AD4
F5	AD5
E1	AD6
E2	AD7
D1	AD8
D3	AD9
E4	AD10
C2	AD11
C1	AD12
B1	AD13'
D4	AD14
C3	AD15
A4	AD16
B4	AD17
C5	AD18
C6	AD19
B5	AD20
E7	AD21
A6	AD22
B6	AD23
D7	AD24
B8	AD25
A7	AD26
A8	AD27
B7	AD28
C9	AD29
D8	AD30
C7	AD31

PCI

C_BE#[3:0] 18,22,23

Pin	Signal
D2	CBE0#
B2	CBE1#
A3	CBE2#
D6	CBE3#

From	Signal	Pin
18,22,23,34	DEVSEL#	D9
18,22,23,34	FRAME#	B3
18,22,23,34	IRDY#	A2
18,22,23,34	TRDY#	C4
18,22,23,34	STOP#	D5
18,22,23	PAR	A9
8,12,13,14,18,21,22,23,24	PCIRST#	J5
22,23,34	PLOCK#	B9
18,22,23,34	SERR#	A1
18,22,23,34	PERR#/GPIO7	E9
18,21,22,23	PME#	K1
23,34	GPIO0/REQ#A	N6
23,34	GPIO16/GNT#A	P5

7 ICHPCLK C14 PCICLK

CPU

Pin	Signal	To
F13	A20M#	4,6,34
E12	SLP#	4,6,34
F15	FERR#	4,6,34
B17	IGNNE#	4,6,34
E15	HINIT#	4,6,12,34
E14	LINT0	4,6,34
B16	LINT1	4,6,34
F14	SMI#	4,6,34
A17	STPCLK#	4,6,34
A15	KBRST#	14,34
B15	A20GATE	14,34

HUB

HL[10:0]

Pin	Signal	To
D17	HL0	
E17	HL1	
F17	HL2	
G16	HL3	
J15	HL4	
K16	HL5	
K17	HL6	
L17	HL7	
H15	HL8	
J17	HL9	
J14	HL10	9
F16	HL11_TP	TP1
G17	HL_STB	9
H17	HL_STB#	9
M17	ICH_HLCOMP	
J13	HUBREF	8,10

Place R239 less than 0.5" from the ICH using a 10 mil trace.

VCC1_8
R239 40.2-1%
C237 0.01UF
Place C237 close to ICH.

IRQ

Pin	Signal	To
D10	PIRQ#A	18,21,22,23,34
A10	PIRQ#B	21,22,23,34
B10	PIRQ#C	22,23,34
C10	PIRQ#D	22,23,34
P11	IRQ14	24,34
N14	IRQ15	24,34
C16	APICCLK	7
E16	PICD0	4,6,34
C17	PICD1	4,6,34
R4	SERIRQ	14,23,34

VCC1_8
R225 301-1%

8,10 HUBREF

R226 301-1%
C218 0.1UF

PCI

Pin	Signal	To
A14	PREQ#0	22,34
B13	PREQ#1	22,34
B12	PREQ#2	23,34
D12	PREQ#3	18,34
B11	PREQ#4	34
P4	PREQ#5	23,34
A13	PGNT#0	22,34
C13	PGNT#1	22,34
A12	PGNT#2	23,34
C12	PGNT#3	18,34
A11	PGNT#4	34
R5	PGNT#5	23,34

VCC1_8,G13,H14,K14,G15,L15,H16,J16
VCC3_3;C11,E13,N13,R13,M14,D16,T16
VCC3_3;E3,A5,E5,G5,N5,E6,P6,T7,C8,U10
GND;R2,G3,H8,J8,K8,H9,J9,K9,H10,J10,K10,G14,K15

Place HUBREF circuit between MCH and ICH
HUBREF voltage = 0.9V +/- 2%

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV:
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ICH

ICH_B

U13
ICH_096

VCC3_3SBY · VCC_RTC_JP · VCC3_3SBY · VCC5_REF · VCC3_3 · VCC5

Strap table

Strap	JP26
No WD Reboot	IN
Reboot on WD*	OUT

Strap	JP5
Safe Mode	IN
ICH strap*	OUT

CMOS	JP20
Normal*	1-2
Clear	2-3

SYSTEM

Signal	Pin	ICH name
THRM# 3,5	D14	THRM#
SLP_S3#	K3	GPIO24/SLP_S3#
SLP_S5#	K2	SLP_S5#
PWROK	J3	PWROK
PWRBTN#	M2	PWRBTN#
ICH_RI#	L3	RI#
RSMRST#	F1	RSMRESET#
MULT1_GPIO	L4	GPIO25/SUSSTAT#
GPIO26_FPLED	K4	SUSCLK/GPIO26
SMBDATA_CORE	J1	SMBDATA
SMBCLK_CORE	J2	SMBCLK
SMB_ALERT	M1	GPIO11/SMBALERT#
LPC_SMI#	E11	GPIO6
LPC_PME#	D11	GPIO5
INTRUDER#	J4	GPIO10/INTRUDER#
RTCRST#	H1	RTCRST#
VBIAS	H2	VBIAS
RTCX1	H3	RTCX1
RTCX2	H4	RTCX2

AC97

Signal	Pin	ICH name
ICH_CLK66	A16	CLK66
ICH_14MHZ	U6	CLK14
ICH_48MHZ	U2	CLK48
AC_RST#	T1	AC_RST#
AC_SYNC	T3	AC_SYNC
AC_BITCLK	R3	AC_BIT_CLK
AC_SDATAOUT	T2	AC_SDOUT
AC_SDATAIN0	U1	ACSDIN0
AC_SDATAIN1	P3	GPIO9/AC_SDIN1
SPKR	U3	SPKR

GPIO

Signal	Pin	ICH name
GPIO12	N4	GPIO12
GPIO13	L2	GPIO13
GPIO21	B14	GPIO21
MULT0_GPIO	D13	GPIO22
GPIO23_FPLED	D15	GPIO23
ALERTCLK_SBY	M5	GPIO27/ALERT_CLK
ALERTDATA_SBY	L5	GPIO28/ALERT_DATA

LPC

Signal	Pin	ICH name
LAD0/FWH0	R6	LAD0/FWH0
LAD1/FWH1	U5	LAD1/FWH1
LAD2/FWH2	T5	LAD2/FWH2
LAD3/FWH3	T4	LAD3/FWH3
LDRQ#0	T6	LDRQ0#
GPIO8	N3	GPIO8/LDRQ1#
LFRAME#/FWH4	U4	LFRAME#/FWH4

USB

Signal	Pin	ICH name
USBP1P	R1	USBP1+
USBP1N	P2	USBP1-
USBP0P	P1	USBP0+
USBP0N	N2	USBP0-
OC#1	M4	OC1#
OC#0	M3	OC0#

IDE

Signal	Pin	IDE name	
PDCS1#	N12	PDCS#1	24
SDCS1#	L14	SDCS#1	24
PDCS3#	U13	PDCS#3	24
SDCS3#	L16	SDCS#3	24
PDA0	R12	PDA0	
PDA1	T12	PDA1	PDA[2:0] 24
PDA2	P12	PDA2	
SDA0	M16	SDA0	
SDA1	M15	SDA1	SDA[2:0] 24
SDA2	L13	SDA2	
PDDREQ	U11	PDREQ	24
SDDREQ	P17	SDREQ	24
PDDACK#	U12	PDDACK#	24
SDDACK#	M13	SDDACK#	24
PDIOR#	R11	PDIOR#	24
SDIOR#	N16	SDIOR#	24
PDIOW#	T11	PDIOW#	24
SDIOW#	N15	SDIOW#	24
PIORDY	N11	PIORDY	24
SIORDY	N17	SIORDY	24

PDD[15:0]

Signal	Pin	PDD name
PDD0	R10	PDD0
PDD1	N9	PDD1
PDD2	R9	PDD2
PDD3	U9	PDD3
PDD4	R8	PDD4
PDD5	U8	PDD5
PDD6	R7	PDD6
PDD7	U7	PDD7
PDD8	P7	PDD8
PDD9	N7	PDD9
PDD10	T8	PDD10
PDD11	P8	PDD11
PDD12	T9	PDD12
PDD13	P9	PDD13
PDD14	T10	PDD14
PDD15	P10	PDD15

SDD[15:0]

Signal	Pin	SDD name
SDD0	P15	SDD0
SDD1	R16	SDD1
SDD2	T17	SDD2
SDD3	U16	SDD3
SDD4	U15	SDD4
SDD5	R14	SDD5
SDD6	P13	SDD6
SDD7	T13	SDD7
SDD8	U14	SDD8
SDD9	T14	SDD9
SDD10	P14	SDD10
SDD11	T15	SDD11
SDD12	U17	SDD12
SDD13	R15	SDD13
SDD14	R17	SDD14
SDD15	P16	SDD15

VCCRTC G1 · VCCSUS N1 · VCCSUS1 L1 · VCCSREF C15

Component references: CR4 BAT17, R245 1K, C246 1UF, VBAT_CR, R241 8.2K, CR5 BAT17, R250 1K, VBAT_RC, C247 2.2UF, R233 1K, C249 0.047UF, VBAT_RTC, BAT1, Use CR2032 battery., R247 10M, R249 10M, Y4 XTAL 32.768KHZ, C250 12PF, C251 12PF, R231 8.2K, R254 8.2K, R317 8.2K, R232 8.2K, R212 8.2K, R215 8.2K, R98 0K, R162 0K, R238 8.2K, R90 2.7K, R341 2.7K, C234 1UF, C233 0.1UF, CR3 BAT17, R220 1K

JP20 RTC_RST_JP · RTC_CLR
PCI_TEST · DRCG_CTRL · SPKR · SPKR_STRAP · AC_SDOUT_STRAP · AC_SDATAOUT
JP26 · JP5

FWH

Do not tie Vpp to 12V. Vpp should be tied to VCC3_3 for onboard programming.

VCC3_3

C300 0.1UF
C305 0.1UF

VCC3_3

VCC3_3

C301 0.1UF C298 0.1UF C297 0.1UF C308 0.1UF

U16

Pin	Name		Name	Pin	
1	NC1		GNDA	40	
2	IC	FWH_IC	VCCA	39	
3	NC3		FWH4	38	LFRAME#/FWH4 11,14
4	NC4		INIT#	37	HINIT# 4,6,10,34
5	NC5		RFU36	36	
6	NC6	FGPI4	RFU35	35	
7	FGPI4		RFU34	34	
8	NC8		RFU33	33	
9	CLK	FWHPCLK	RFU32	32	
10	VCC10		VCC31	31	
11	VPP	VPP_R	GND30	30	
12	RST#	PCIRST#	GND29	29	
13	NC13		FWH3	28	LAD3/FWH3 11,14
14	NC14		FWH2	27	LAD2/FWH2 11,14
15	FGPI3		FWH1	26	LAD1/FWH1 11,14
16	FGPI2		FWH0	25	LAD0/FWH0 11,14
17	FGPI1		ID0	24	
18	FGPI0		ID1	23	
19	WP#		ID2	22	
20	TBL#		ID3	21	

FWH

R296 8.2K
R298 8.2K
R299 0K 8,10,13,14,18,21,22,23,24
R300 8.2K
R303 8.2K

24 S66DETECT
24 P66DETECT

R305 0K
R306 0K

For drive side detection, stuff R304,R307. No stuff R305,R306.
For host side detection, stuff R304,R305,R306,R307.

R304 15K
R307 15K

VCC3_3

VCC3_3

R308 4.7K WPROT

JP21

Top Block Lock

TBLK_LCK

R310 4.7K

FWH	JP21
OUT	Locked
IN	Unlocked*

RIMM Sockets

For MTH down solution, this sheet should be replaced by Appendix A (sheets 38-41).

As shown, RIMMs are 184-pin connectors.

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RIMM SOCKETS

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Super I/O

LPC I/F

PARALLEL PORT I/F

SIO

LPC47B27X

KYBD/MSE I/F

INFRARED I/F

SERIAL PORT 1

SERIAL PORT 2

FDC I/F

CLOCKS

U17

Signal	Pin	Port
LFRAME#/FWH4	24	LFRAME#
LAD3/FWH3	23	LAD3
LAD2/FWH2	22	LAD2
LAD1/FWH1	21	LAD1
LAD0/FWH0	20	LAD0
LDRQ#0	25	LDRQ#
PCIRST#	26	LRESET#
LPCPD#	27	LPCPD#
LPC_PME#	17	PME#
SERIRQ	30	SERIRQ
SIO_PCLK7	29	PCI_CLK

11,12,14 LFRAME#/FWH4
11,12,14 LAD3/FWH3
11,12,14 LAD2/FWH2
11,12,14 LAD1/FWH1
11,12,14 LAD0/FWH0
11,14 LDRQ#0
8,10,12,13,14,18,21,22,23,24 PCIRST#

10,14,23,34 SERIRQ
7,14 SIO_PCLK7

VCC5   VCC3_3

44 VREF
18 VTR
53 VCC1
65 VCC2
93 VCC3

Signal	Pin	Port
PAR_INIT#	66	INIT#
SLIN#	67	SLCTIN#
PDR7	75	PD7
PDR6	74	PD6
PDR5	73	PD5
PDR4	72	PD4
PDR3	71	PD3
PDR2	70	PD2
PDR1	69	PD1
PDR0	68	PD0
SLCT	77	SLCT
PE	78	PE
BUSY	79	BUSY
ACK#	80	ACK#
ERR#	81	ERROR#
AFD#	82	ALF#
STB#	83	STROBE#

PDR[7:0]

26

KBDAT 56 KDAT
KBCLK 57 KCLK
MDAT 58 MDAT
MCLK 59 MCLK
28 KBDAT
28 KBCLK
28 MDAT
28 MCLK

KBRST# 63 KBDRST
A20GATE 64 A20GATE
10,34 KBRST#
10,34 A20GATE

IRRX 61 IRRX2/GP34
IRTX 62 IRTX2/GP35
20 IRRX
20 IRTX

C320   C317
470PF 470PF

RXD0 84 RXD1
TXD0 85 TXD1
DSR#0 86 DSR1#
RTS#0 87 RTS1#
CTS#0 88 CTS1#
DTR#0 89 DTR1#
RI#0 90 RI1#
DCD#0 91 DCD1#
27 (all)

RXD1 95 RXD2_IRRX
TXD1 96 TXD2_IRTX
DSR#1 97 DSR2#
RTS#1 98 RTS2#
CTS#1 99 CTS2#
DTR#1 100 DTR2#
RI#1 92 RI2#
DCD#1 94 DCD2#
27 (all)

DRVDEN#1 2 DRVDEN1
DRVDEN#0 1 DRVDEN0
MTR#0 3 MTR0#
DS#0 5 DS0#
DIR# 8 DIR#
STEP# 9 STEP#
WDATA# 10 WDATA#
WGATE# 11 WGATE#
HDSEL# 12 HDSEL#
INDEX# 13 INDEX#
TRK#0 14 TRK0#
WRTPRT# 15 WRTPRT#
RDATA# 16 RDATA#
DSKCHG# 4 DSKCHG#
28 (all)

CLKI32 6
CLOCKI 19
SIO_14MHZ
7

FAN2/GP32 54 PWM2
FAN1/GP33 55 PWM1
20

FDC_PP/DDRC/GP43 28

GP60/LED1 48
GP61/LED2 49
GP27/IO_SMI# 50 LPC_SMI#
GP30/FAN_TACH2 51 CPU_TACH2
GP31/FAN_TACH1 52 CPU_TACH1
11

GP25/MIDI_IN 46 MIDI_IN
GP26/MIDI_OUT 47 MIDI_OUT
29

GP10/J1B1 32 J1BUTTON1
GP11/J1B2 33 J1BUTTON2
GP12/J2B1 34 J2BUTTON1
GP13/J2B2 35 J2BUTTON2
GP14/J1X 36 JOY1X
GP15/J1Y 37 JOY1Y
GP16/J2X 38 JOY2X
GP17/J2Y 39 JOY2Y
GP20/P17 41 KEYLOCK#
GP21/P16 42
GP22/P12 43
29 (all)
20 KEYLOCK#

GP24/SYSOPT 45 SYSOPT
Pulldown on SYSOPT for IO address of 0x02E

R312 4.7K

VCC3_3 VCC3_3
R157 4.7K   R313 4.7K

GND1 7
GND2 31
GND3 60
GND4 76
AVSS 40

VCC5   VCC3_3
C309   C348 C321 C313 C323   C349
0.1UF 0.1UF 0.1UF 0.1UF 0.1UF 2.2UF
Place next to VREF.   Place decoupling caps near each power pin.

28 VCC5_KBMS_J
VCC3_3
R315 4.7K
RP5 4.7K

LPC header. For debug only.

J20

Signal	1	2	
LAD3/FWH3	1	2	
LAD2/FWH2	3	4	
LAD1/FWH1	5	6	
LAD0/FWH0	7	8	
LFRAME#/FWH4	9	10	
PCIRST#	11	12	
SIO_PCLK7	13	14	
LDRQ#0	15	16	
	17	18	
MULT1_GPIO	19	20	
	21	22	
SERIRQ	23	24	
	25	26	
	27	28	

11,12,14 (LAD signals)
8,10,12,13,14,18,21,22,23,24 PCIRST#
7,14 SIO_PCLK7
11,14 LDRQ#0
7,11 MULT1_GPIO
10,14,23,34 SERIRQ

AC'97 Audio

AC'97 Audio

Stereo HP/Spkr out

HP_OUTA — C10 1 2 — HP_OUTA_C 1 — L4 2 — HP_OUTA_FB — HP30 J5
100UF
HP29
HP28
HP_OUTB_C 1 — L1 2 — HP_OUTB_FB — HP27
C3 1 2
100UF
HP26
DB15_AUD_STK
AGND

10PF-NPO C11 1 2
10PF-NPO C24 1 2
AGND AGND

Microphone Input

15 — AUD_VREFOUT — R163 2.2K — MIC_IN_R
MIC_IN_FB — M20 J5
M19
M18
M17
M16
15 — MIC_IN — C27 1 2 — MIC_IN_C — R9 1K — 2 L5 1 — DB15_AUD_STK
1UF-TANT
C34 0.01UF
C28 1 2 10PF-NPO
AGND AGND AGND

C8 100PF
R360 20K
U1 LM4880
1 OUTA VDD 8 — VCC5_AUDIO — 15
2 INA OUTB 7 — HP_OUTB — 15
3 BYPASS INB 6
4 GND SHUTDN 5 — EAPD — 15

100PF
R362 20K
C4

15 — LNLVL_OUT_R — C6 1 2 — LNLVL_R_C — R171 20K — LNLVL_R_R
1UF-TANT
15 — LNLVL_OUT_L — C13 1 2 — LNLVL_L_C — R361 20K
1UF-TANT
AC_BYPASS

C2 2 1 1UF
AGND
AGND

C14 1 2 0.1UF
AGND

Line_In Analog Input

15 — LINE_IN_R — C23 1 2 — LINE_IN_R_C — 1 L2 2 — LINE_IN_R_FB LI25 J5
1UF-TANT
LI24
LI23
15 — LINE_IN_L — C25 1 2 — LINE_IN_L_C — 1 L3 2 — LINE_IN_L_FB LI22
1UF-TANT
LI21
DB15_AUD_STK
AGND

10PF-NPO C22 1 2
10PF-NPO C26 1 2
AGND AGND

LNLVL_L_R

CD Analog Input

J4
1 CD_L_J — R52 4.7K — CD_L_C — C59 2 1 — CD_L — 15
2 CD_REF_J
3 — R27 4.7K — CD_REF_C — C58 2 1 — CD_REF — 15
4 CD_R_J — R167 4.7K — CD_R_C — C50 2 1 — CD_R — 15
1UF

R51 4.7K
R30 4.7K
R25 4.7K
AGND AGND AGND

AC'97 Audio/Modem Riser

VCC3_3SBY   VCC3_3 VCC5 VCC12 VCC12-

VCC3_3SBY

R68
4.7K

U3
14
6
4 PRI_DWN_U
5
PRI_DWN_RST#
15
SN74LVC08A

15 MONO_OUT

PRI_DWN#

3 1
JP2
2

J8

B1	AUDIO_MUTE#	AUDIO_PWRDWN	A1	
B2	GND[0] (ISOLATED)	MONO_PHONE	A2	MONO_PHONE 15
B3	MONO_OUT/PC_BEEP	RESV[5]	A3	
B4	RESV[1]	RESV[6]	A4	VCC5
B5	RESV[2]	RESV[7]	A5	
B6	PRIMARY_DN#	GND[7]	A6	
B7	-12V	+5VDUAL/5VSBY	A7	
B8	GND[1]	USB_OC	A8	AC97_OC# 25
B9	+12V	GND[8]	A9	
B10	GND[2]	USB+	A10	AC97_USB+ 25
B11	+5VD	USB-	A11	AC97_USB- 25
	KEY	KEY		
	KEY	KEY		
B12	GND[3]	GND[9]	A12	VCC3_3SBY
B13	RESV[3]	S/P_DIF_IN	A13	
B14	RESV[4]	GND[10]	A14	
B15	+3.3VD	+3VDUAL/3VSBY	A15	
B16	GND[4]	GND[11]	A16	
B17	AC97_SDATA_OUT	AC97_SYNC	A17	AC_SYNC 11,15
B18	AC97_RESET#	GND[12]	A18	
B19	AC97_SDATA_IN3	AC97_SDATA_IN1	A19	AC_SDATAIN1_R R113 0K AC_SDATAIN1 11
B20	GND[5]	GND[13]	A20	
B21	AC97_SDATA_IN2	AC97_SDATA_IN0	A21	AC_SDATAIN0 11,15
B22	GND[6]	GND[14]	A22	
B23	AC97_MSTRCLK	AC97_BITCLK	A23	AC_BITCLK 11,15

AC'97_RISER
AMR_CONNECTOR

11,15 AC_SDATAOUT
11 AC_RST#

Audio Down	JP2
Enable*	1-2
Disable	2-3

R108 10K
R125 10K

LAN

U5

82559

G13 K13 N8 P12 A11 — A3 A7 E1 K3 N6 P2 — E12 G5 G6 H5 H6 H7 H8 J5 J6 J7 J8 J9 J10 J11 K4 K5 K6 K7 K8 K9 K10 K11 L4 L5 L9 L10

Signal	Pin	Label
AD0	N7	AD0
AD1	M7	AD1
AD2	P6	AD2
AD3	P5	AD3
AD4	N5	AD4
AD5	M5	AD5
AD6	P4	AD6
AD7	N4	AD7
AD8	P3	AD8
AD9	N3	AD9
AD10	N2	AD10
AD11	M1	AD11
AD12	M2	AD12
AD13	M3	AD13
AD14	L1	AD14
AD15	L2	AD15
AD16	K1	AD16
AD17	E3	AD17
AD18	D1	AD18
AD19	D2	AD19
AD20	D3	AD20
AD21	C1	AD21
AD22	B1	AD22
AD23	B2	AD23
AD24	B4	AD24
AD25	A5	AD25
AD26	B5	AD26
AD27	B6	AD27
AD28	C6	AD28
AD29	C7	AD29
AD30	A8	AD30
AD31	B8	AD31

AD[31:0] 10,22,23

VCCPL[0] VCCPL[1] VCCPL[2] VCCPL[3] VCCPT VCCPP[0] VCCPP[1] VCCPP[2] VCCPP[3] VCCPP[4] VCCPP[5] VCC[0] VCC[1] VCC[2] VCC[3] VCC[5] VCC[7] VCC[8] VCC[9] VCC[10] VCC[11] VCC[12] VCC[13] VCC[14] VCC[15] VCC[16] VCC[17] VCC[18] VCC[19] VCC[20] VCC[21] VCC[22] VCC[23] VCC[24] VCC[25]

VCC3_3SBY

C_BE#[3:0] 10,22,23

Signal	Pin	Label
C_BE#0	M4	C/BE0#
C_BE#1	L3	C/BE1#
C_BE#2	F3	C/BE2#
C_BE#3	C4	C/BE3#

Signal	Source	Pin	Label
FRAME#	10,22,23,34	F2	FRAME#
IRDY#	10,22,23,34	F1	IRDY#
TRDY#	10,22,23,34	G3	TRDY#
DEVSEL#	10,22,23,34	H3	DEVSEL#
STOP#	10,22,23,34	H1	STOP#
PAR	10,22,23	J1	PAR
PIRQ#A	10,22,23,34	H2	INTA#
PERR#	10,21,22,23,34	J2	PERR#
SERR#	10,22,23,34	A2	SERR#
AD20 — R75 100 — AD20_RLAN	10,18,22,23	A4	IDSEL
PREQ#3	10,34	C3	REQ#
PGNT#3	10,34	J3	GNT#
PCIRST#	10,34	C2	RST#
PCLK5	7	G1	CLK

Signal	Source	Pin	Label
PWROK	9,11,31,33	B9	ISOLATE#
LAN_RSMRST#	19	A9	ALTRST#
ALERTCLK_SBY	11,34	A10	SMBCLK
ALERTDATA_SBY	11,34	C9	SMBD
		G2	VIO
LAN_X1		N11	X1
LAN_X2		P11	X2

VCC5SBY

Y2 XTAL 25MHZ

C101 22PF   C96 22PF

8,10,12,13,14,21,22,23,24

Pin	Label	Net	Ref
A12	LILED	LILED	19
C11	ACTLED	ACTLED	19
B11	SPEEDLED	SPEEDLED	19
C13	TDP	TDP	19
C14	TDN	TDN	19
E13	RDP	RDP	19
E14	RDN	RDN	19

Signal	Pin	Net
SMBALRT#	B10	x
CSTSCHG	C5	x
PME#	A6	PCI_PME# → 10,21,22,23

VCC3_3SBY R59 3.3K

Signal	Pin	Net
FLA0/PCIMODE#	J13	
FLA1/AUXPWR	J12	AUXPWR
FLA2	K14	x
FLA3	L14	x
FLA4	L13	x
FLA5	L12	x
FLA6	M14	x
FLA7	M13	x
FLA8/IOCHRDY	N14	x
FLA9/MRST	P13	x
FLA10/MRING#	N13	x
FLA11/MINT	M12	x
FLA12/MCNTSM#	M11	x
FLA13/EEDI	P10	EEDI
FLA14/EEDO	N10	EEDO
FLA15/EESK	M10	EESK
FLA16	P9	x
FLD0	F14	x
FLD1	F13	x
FLD2	F12	x
FLD3	G12	x
FLD4	H14	x
FLD5	H13	FLD5
FLD6	H12	FLD6
FLD7	J14	x
EECS	P7	EECS
FLCS#	N9	x
FLOE#	M8	x
FLWE#	M9	x
CLKRUN#	C8	CLKRUN#_LAN
TEST	A13	TEST_LAN
TEXEC	D13	x
TCK	D14	x
TI	D12	x
TO	B12	x
RBIAS10	B14	RBIAS10
RBIAS100	B13	RBIAS100
VREF	C12	x

VCC3_3SBY

U24 93C46

EEDI — 3 EEDI, VCC 8
EEDO — 4 EEDO, NC2 7 — x
EESK — 2 EESK, NC1 6 — x
EECS — 1 EECS, GND 5

No stuff R57, R58
R58 3.3K
R57
R363 62K
R14 3.3K
R16 549
R15 619

VSSPL[0..3] VSSPT VSSPP[0..5] VSS[0..31]

G14 K12 P8 N12 — C10 — B3 B7 F2 K2 M6 N1 — D4 D5 D6 D7 D8 D11 E4 E5 F6 F7 F8 F9 F10 E11 F4 F5 F6 F7 F8 F9 F10 E11 G7 G8 G9 G10 G11 H9 H10 H11 L6 L11

LAN

Place termination resistors close to 82559.

No stuff C61, C79.

TD_C
RD_C

C61 0.1UF
C79 0.1UF

18 TDP
18 TDN
18 RDP
18 RDN

R26 49.9-1%
R20 49.9-1%
R62 49.9-1%
R364 49.9-1%

J2 RJMAG

10 TD+
12 TD-
9 RD+
7 RD-
3 RJ-4
4 RJ-5
5 RJ-7
6 RJ-8

RJ-45

14
13 LILED
16
15 ACTLED

18,19
18,19

TXC RXC SHLD1 SHLD2 TDC RDC

2 1 17 18 11 8

RJ4_J
RJ_7_J
TXC_J
RXC_J
TDC_J
RDC_J

R6 75
R365 75
R8 75
R10 75

XC_R

C31 0.1UF
C78 0.1UF

No stuff C5.
C5 must be rated at 1500V.

C5 470PF

No stuff C31.

VCC3_3

R61 330
R366 330

LI_CR
ACT_CR 330

VCC3_3

R73 330
R78 330
R60 330

LI_J
ACT_J
SPEED_J

JP3 JP4 JP1

No stuff JP1,JP3,JP4,R60,R73,R78.

18,19 LILED
18,19 ACTLED
18 SPEEDLED

For debug only. Hold LAN in reset.

J18

11,33 RSMRST# 1
18 LAN_RSMRST# 2
3

82559 LAN	J17
Enable*	1-2
Disable	2-3

System

No stuff.
For test only

ICH has internal pullup and debounce on PWRBTN#

R252 1M
VCC3_3SBY

SW1
R257 0K
PWRBTN# 11

C267 1UF
No stuff. For test only

PWRBTN_FP#

VCC3_3
R359 100K
C350 0.1UF 50V
C356 10UF 16V
VCC5 C5

IRRX 14
IRTX 14
IRTX_R 82
R357 5%
R358 4.7K 5%

J25
1 INFRARED
2
3
4
5 KEY
6
7
8 POWER SW.
9

R356 470
HDLED_R
10
11
12
13 KEY H.D. LED
14
15
16 KEY
17 POWER LED
18 KEY
19
20 KEY
21
22 KEYLOCK
23
24 KEY SPEAKER
25
26
FNT_PNL_CONN

VCC5 VCC5
R345 10K R344 10K

VCC3_3
U19
1   2
SN74LVC07A
VCC GND
VCC3_3

IDEACTP# 24
IDE_ACTIVE

U19
9   8
SN74LVC07A
VCC GND
IDEACTS# 24

C354 470PF C355 470PF

VCC3_3 VCC5
R354 10K

R355 220
PLED_R

KEYLOCK# 14

SPKR_FP

JP25
1 AC97_SPKR 15
2 SPKR 11
3 PC_BEEP

Speaker Circuit
SPKR_Q
R352 68
R353 68

Q15 MMBT3904LT1
C 3
B 1
E 2

R350 2.2K
P_BEEP

C353 0.1UF

VCC5
SP1
1 + POS
2 NEG
SPKR_ONBOARD

Onboard Spkr	JP25
Enable*	2-3
Disable	1-2

VCC3_3SBY
R289 330
SBY_LED_CR
CR7

Onboard LED indicates the standby well is on
to prevent hot swapping memory.
For debug only.

VCC3_3SBY VCC3_3SBY VCC3_3SBY
R253 330 R246 330

U14 VCC
GPIO23_FPLED 11
SN74LVC07A
3   4
GND
LED_PU0
1   2
CR6
DUAL_COLOR
LED_PU1
U14 VCC
6   5
GND
SN74LVC07A
GPIO26_FPLED 11

R234 4.7K

TACH2
VCC12
C316 0.1UF
VCC3_3
R316 4.7K
JP22
1
2
3
TACH2

PWM1
VCC12
C327 0.1UF
VCC3_3
R329 4.7K
JP24
1
2
3
PWM1 14

PWM2
VCC12
C322 0.1UF
VCC3_3
R326 4.7K
JP23
1
2
3
PWM2 14

PWM outputs from SIO need power buffers for driving fan inputs.

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
SYSTEM

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY:
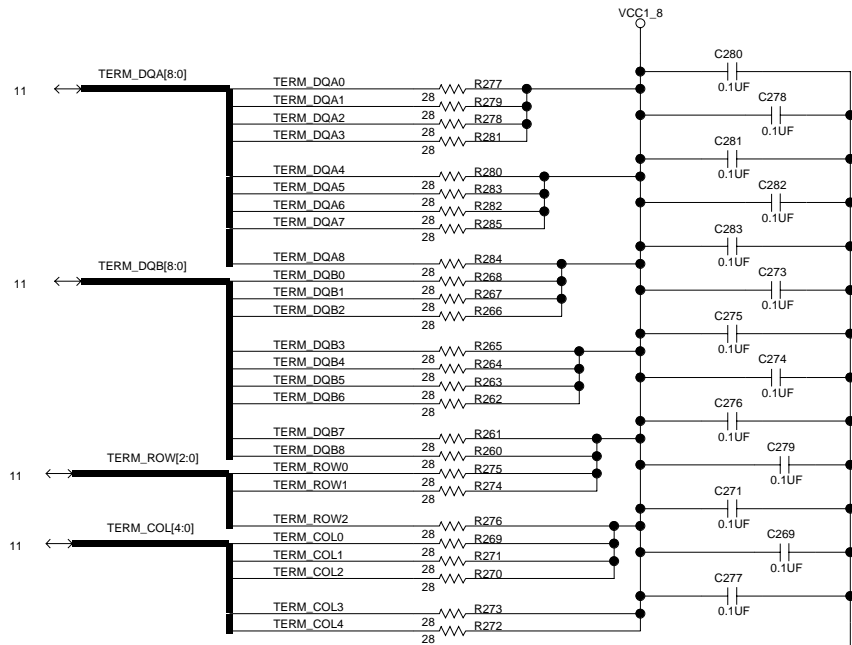PROJECT:
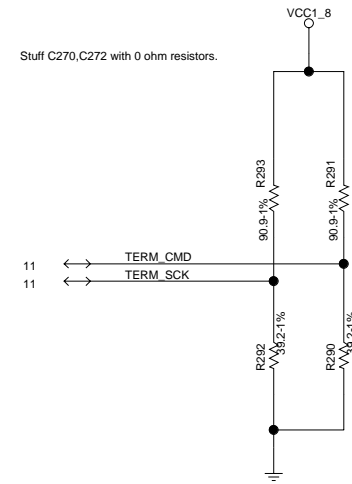LAST REVISED: 11-29-1999_14:46
SHEET: 20 OF 38

AGP Connector

VCC3_3　VDDQ　VCC12

SBA[7:0]

ST[2:0]

B pin	Signal		Signal	A pin	
	AGP_OC#	B1 OVRCNT#	12V	A1	
25		B2 5V_A	TYPEDET#	A2	TYPEDET# → 21,31
		B3 5V_B	RESV_A	A3	
25	USBAGP+	B4 USB+	USB-	A4	USBAGP- → 25
		B5 GND_K	GND_A	A5	
		B6 INTB#	INTA#	A6	
	AGPCLK_CONN	B7 CLK	RST#	A7	PCIRST#
7	GREQ#	B8 REQ#	GNT#	A8	GGNT# → 9,34
		B9 VCC3_3_F	VCC3_3_A	A9	
	ST0	B10 ST0	ST1	A10	ST1
	ST2	B11 ST2	RESV_B	A11	
	RBF#	B12 RBF#	PIPE#	A12	PIPE# → 9,34
		B13 GND_L	GND_B	A13	
		B14 RESV_H	WBF#	A14	WBF# → 9,34
	SBA0	B15 SBA0	SBA1	A15	SBA1
		B16 VCC3_3_G	VCC3_3_B	A16	
	SBA2	B17 SBA2	SBA3	A17	SBA3
	SBSTB	B18 SB_STB	SB_STB#	A18	SBSTB# → 9,34
		B19 GND_M	GND_C	A19	
	SBA4	B20 SBA4	SBA5	A20	SBA5
	SBA6	B21 SBA6	SBA7	A21	SBA7
		B22 RESV	RESV_C	A22	
		B23 GND_N	GND_D	A23	
		B24 3_3VAUX1	RESV_D	A24	
		B25 VCC3_3_H	VCC3_3_C	A25	
	GAD31	B26 AD31	AD30	A26	GAD30
	GAD29	B27 AD29	AD28	A27	GAD28
		B28 VCC3_3_I	VCC3_3_D	A28	
	GAD27	B29 AD27	AD26	A29	GAD26
	GAD25	B30 AD25	AD24	A30	GAD24
		B31 GND_O	GND_E	A31	
	ADSTB1	B32 AD_STB1	AD_STB1#	A32	ADSTB#1 → 9,34
	GAD23	B33 AD23	C/BE3#	A33	GC/BE#3
		B34 VDDQ_F	VDDQ_A	A34	
	GAD21	B35 AD21	AD22	A35	GAD22
	GAD19	B36 AD19	AD20	A36	GAD20
		B37 GND_P	GND_F	A37	
	GAD17	B38 AD17	AD18	A38	GAD18
	GC/BE#2	B39 C/BE2#	AD16	A39	GAD16
		B40 VDDQ_G	VDDQ_B	A40	
	GIRDY#	B41 IRDY#	FRAME#	A41	GFRAME# → 9,34
		B42 3_3VAUX2	RESV_E	A42	
		B43 GND_Q	GND_G	A43	
		B44 RESV_K	RESV_F	A44	
		B45 VCC3_3_J	VCC3_3_E	A45	
	GDEVSEL#	B46 DEVSEL#	TRDY#	A46	GTRDY# → 9,34
		B47 VDDQ_H	STOP#	A47	GSTOP# → 9,34
	GPERR#	B48 PERR#	PME#	A48	PCI_PME# → 10,18,22,23
		B49 GND_R	GND_H	A49	
	GSERR#	B50 SERR#	PAR	A50	GPAR → 9,34
	GC/BE#1	B51 C/BE1#	AD15	A51	GAD15
		B52 VDDQ_I	VDDQ_C	A52	
	GAD14	B53 AD14	AD13	A53	GAD13
	GAD12	B54 AD12	AD11	A54	GAD11
		B55 GND_S	GND_I	A55	
	GAD10	B56 AD10	AD9	A56	GAD9
	GAD8	B57 AD8	C/BE0#	A57	GC/BE#0
		B58 VDDQ_J	VDDQ_D	A58	
	ADSTB0	B59 AD_STB0	AD_STB0#	A59	ADSTB#0 → 9,34
	GAD7	B60 AD7	AD6	A60	GAD6
		B61 GND_T	GND_J	A61	
	GAD5	B62 AD5	AD4	A62	GAD4
	GAD3	B63 AD3	AD2	A63	GAD2
		B64 VDDQ_K	VDDQ_E	A64	
	GAD1	B65 AD1	AD0	A65	GAD0
	MCH_AGPREF	B66 VREF_CG	VREF_GC	A66	

J13　AGP4XU_20

PIRQ#B → 10,22,23,34

PIRQ#A → 10,18,22,23,34

8,10,12,13,14,18,22,23,24

VCC5

VCC3_3SBY

9 GAD[31:0]
9 GC/BE#[3:0]

AGPREF circuitry should be placed close to MCH.

VDDQ

R193　301-1%

CON_AGPREF_Q

Q8　2N7002LT1

R208　200-1%

TYPEDET# ← 21,31

CONN_AGPREF → 8

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV:
AGP CONNECTOR　3.03

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY:	PROJECT:
LAST REVISED: 11-30-1999_10:10	SHEET: 21 OF 38

PCI Connectors
0 and 1

For pullups, see 4.3.3 of PCI 2.1 Specification

PCI Slot 0 J12 PCI3_CON

	B1	A1	
PTCK	B2	A2	PTRST# 22,23
22,23	B3	A3	PTMS 22,23
	B4	A4	PTDI 22,23
	B5	A5	
	B6	A6	PIRQ#A 10,18,21,22,23,34
PIRQ#B 10,21,22,23,34	B7	A7	PIRQ#C 10,22,23,34
PIRQ#D 10,22,23,34	B8	A8	
PRSNT#11 22	B9	A9	
	B10	A10	
PRSNT#12 22	B11	A11	
	B12	A12	VCC3_3SBY
	B13	A13	
	B14	A14	
	B15	A15	PCIRST# 8,10,12,13,14,18,21,22,23,24
PCLK1 7	B16	A16	
	B17	A17	PGNT#0 10,34
PREQ#0 10,34	B18	A18	
	B19	A19	PCI_PME# 10,18,21,22,23
AD31	B20	A20	AD30
AD29	B21	A21	
	B22	A22	AD28
AD27	B23	A23	AD26
AD25	B24	A24	
	B25	A25	AD24
C_BE#3	B26	A26	R_AD16 22
AD23	B27	A27	
	B28	A28	AD22
AD21	B29	A29	AD20
AD19	B30	A30	
	B31	A31	AD18
AD17	B32	A32	AD16
C_BE#2	B33	A33	
	B34	A34	FRAME# 10,18,22,23,34
IRDY# 10,18,22,23,34	B35	A35	
	B36	A36	TRDY# 10,18,22,23,34
DEVSEL# 10,18,22,23,34	B37	A37	
	B38	A38	STOP# 10,18,22,23,34
PLOCK# 10,22,23,34	B39	A39	
PERR# 10,18,22,23,34	B40	A40	SDONEP1 22
	B41	A41	SBOP1 22
SERR# 10,18,22,23,34	B42	A42	
	B43	A43	PAR 10,18,22,23
C_BE#1	B44	A44	AD15
AD14	B45	A45	
	B46	A46	AD13
AD12	B47	A47	AD11
AD10	B48	A48	
	B49	A49	AD9
AD8	B52	A52	C_BE#0
AD7	B53	A53	
	B54	A54	AD6
AD5	B55	A55	AD4
AD3	B56	A56	
	B57	A57	AD2
AD1	B58	A58	AD0
	B59	A59	
PU1_ACK64# 22	B60	A60	PU1_REQ64# 22
	B61	A61	
	B62	A62	

PCI Slot 1 J11 PCI3_CON

	B1	A1	
PTCK	B2	A2	PTRST# 22,23
22,23	B3	A3	PTMS 22,23
	B4	A4	PTDI 22,23
	B5	A5	
	B6	A6	PIRQ#B 10,21,22,23,34
PIRQ#C 10,22,23,34	B7	A7	PIRQ#D 10,22,23,34
PIRQ#A 10,18,21,22,23,34	B8	A8	
PRSNT#21 22	B9	A9	
	B10	A10	
PRSNT#22 22	B11	A11	
	B12	A12	VCC3_3SBY
	B13	A13	
	B14	A14	
	B15	A15	PCIRST# 8,10,12,13,14,18,21,22,23,24
PCLK2 7	B16	A16	
	B17	A17	PGNT#1 10,34
PREQ#1 10,34	B18	A18	
	B19	A19	PCI_PME# 10,18,21,22,23
AD31	B20	A20	AD30
AD29	B21	A21	
	B22	A22	AD28
AD27	B23	A23	AD26
AD25	B24	A24	
	B25	A25	AD24
C_BE#3	B26	A26	R_AD17 22
AD23	B27	A27	
	B28	A28	AD22
AD21	B29	A29	AD20
AD19	B30	A30	
	B31	A31	AD18
AD17	B32	A32	AD16
C_BE#2	B33	A33	
	B34	A34	FRAME#
IRDY#	B35	A35	
	B36	A36	TRDY#
DEVSEL#	B37	A37	
	B38	A38	STOP#
PLOCK#	B39	A39	
PERR#	B40	A40	SDONEP2
	B41	A41	SBOP2
SERR#	B42	A42	
	B43	A43	PAR
C_BE#1	B44	A44	AD15
AD14	B45	A45	
	B46	A46	AD13
AD12	B47	A47	AD11
AD10	B48	A48	
	B49	A49	AD9
AD8	B52	A52	C_BE#0
AD7	B53	A53	
	B54	A54	AD6
AD5	B55	A55	AD4
AD3	B56	A56	
	B57	A57	AD2
AD1	B58	A58	AD0
	B59	A59	
PU2_ACK64# 22	B60	A60	PU2_REQ64# 22
	B61	A61	
	B62	A62	

VCC5 VCC5
VCC3_3
VCC5
5.6K R367
R79 5.6K
PTRST# 22,23
R72 5.6K

RP12
SDONEP1 22	1	8	
SDONEP2 22	2	7	
SBOP1 22	3	6	
SBOP2 22	4	5	

5.6K

VCC5

C117 0.1UF
PRSNT#11 22

C123 0.1UF
PRSNT#12 22

C113 0.1UF
PRSNT#21 22

C122 0.1UF
PRSNT#22 22

VCC5
PU1_ACK64# 22 R178 2.7K
PU1_REQ64# 22 R179 2.7K
PU2_ACK64# 22 R176 2.7K
PU2_REQ64# 22 R177 2.7K

AD16 10,18,22,23 R120 100 R_AD16 22
AD17 10,18,22,23 R119 100 R_AD17 22

C_BE#[3:0] 10,18,23
AD[31:0] 10,18,23

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV:
PCI CONNECTORS 1 AND 2   3.03

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY: PROJECT:
LAST REVISED: SHEET:
11-29-1999_14:46 22 OF 38

PCI Connectors
2 and 3

PCI Slot 2
J10
PCI3_CON
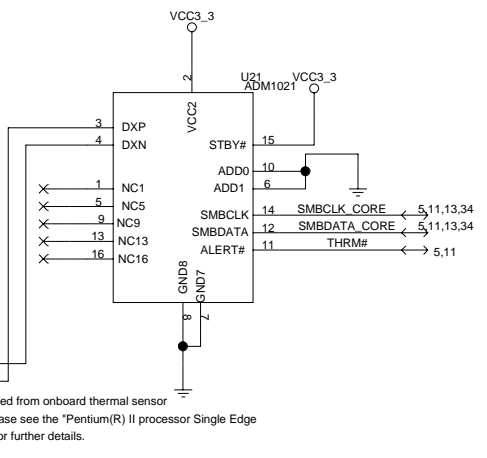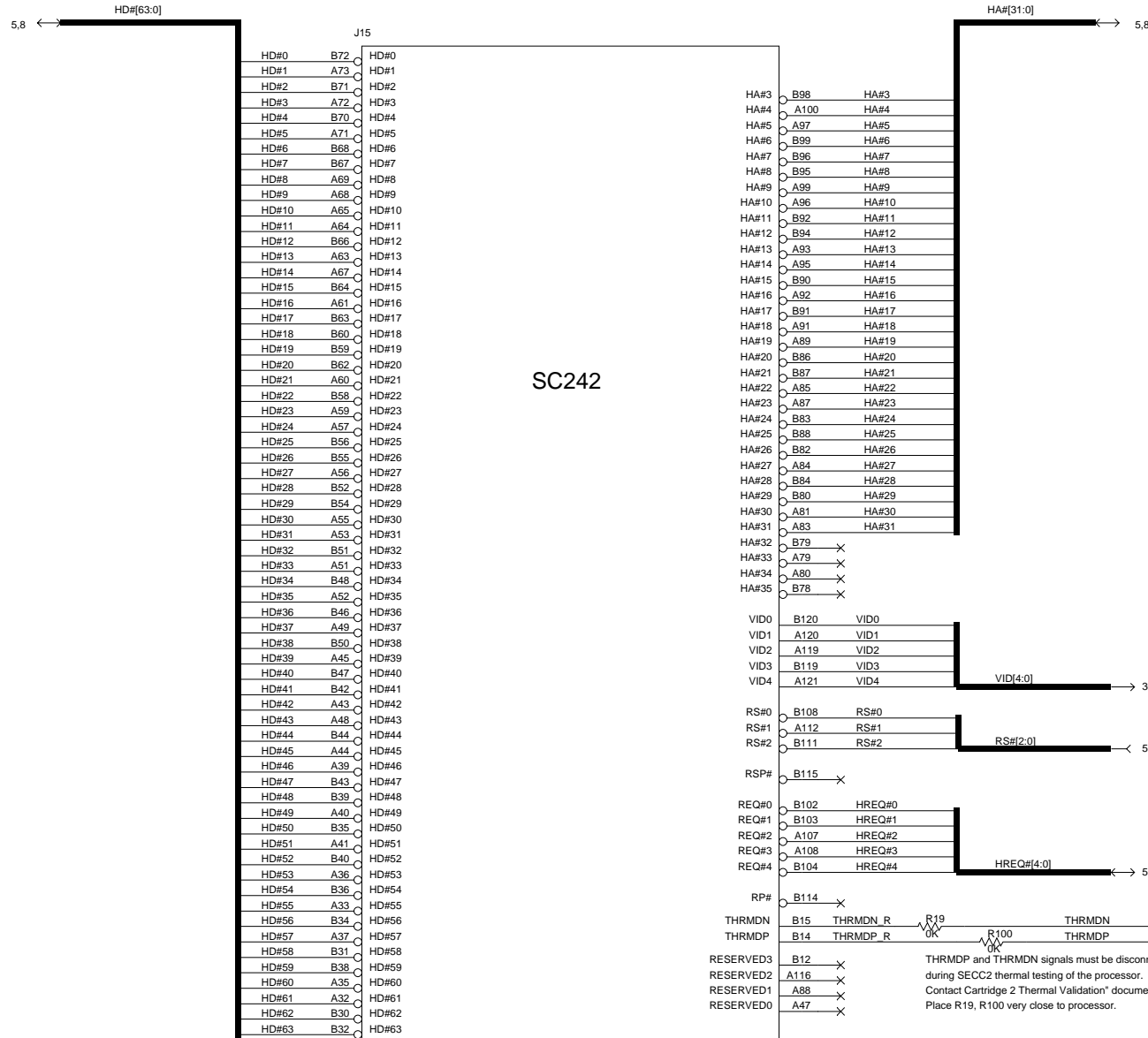
B1	A1	PTRST# → 22,23
B2	A2	
B3	A3	PTMS → 22,23
B4	A4	PTDI → 22,23
B5	A5	
B6	A6	PIRQ#D → 10,22,23,34
B7	A7	PIRQ#B → 10,21,22,23,34
B8	A8	
B9	A9	
B10	A10	PCI_TEST for debug only 11
B11	A11	
B12	A12	VCC3_3SBY
B13	A13	
B14	A14	
B15	A15	PCIRST# → 8,10,12,13,14,18,21,22,23,24
B16	A16	
B17	A17	PGNT2 → 10,34
B18	A18	
B19	A19	PCI_PME# → 10,18,21,22,23

PTCK 22,23
PIRQ#A 10,18,21,22,23,34
PIRQ#C 10,22,23,34
PRSNT31 23
PRSNT32 23
PCLK3 7
PREQ2 10,34

PCI Slot 3
J9
PCI3_CON

J9 must be furthest from the processor.

B1	A1	PTRST# → 22,23
B2	A2	
B3	A3	PTMS → 22,23
B4	A4	PTDI → 22,23
B5	A5	
B6	A6	PIRQ#C → 10,22,23,34
B7	A7	PIRQ#A → 10,18,21,22,23,34
B8	A8	
B9	A9	
B10	A10	
B11	A11	GNT#A_R
B12	A12	
B13	A13	
B14	A14	VAUX_JP
B15	A15	PCIRST# → 8,10,12,13,14,18,21,22,23,24
B16	A16	
B17	A17	PGNT5 → 10,34
B18	A18	
B19	A19	PCI_PME# → 10,18,21,22,23

PTCK 22,23
PIRQ#D 10,22,23,34
PIRQ#B 10,21,22,23,34
PRSNT41 23
PRSNT42 23
PCLK4 7
PREQ5 10,34

SERIRQ for debug only
10,14,34 SERIRQ   R255 0K   SERIRQ_RB 14

GNT#A for debug only
R99 0K   GNT#A 10,34   VCC3_3SBY

R107 0K
R110 0K   REQ#A 10,34
No Stuff R110.
REQ#A for debug only

RP13
SDONEP3 1 — 8 23
SDONEP4 2 — 7 23
SBOP3   3 — 6 23
SBOP4   4 — 5 23
5.6K

VCC5

C112 0.1UF   PRSNT31 23
C121 0.1UF   PRSNT32 23
C116 0.1UF   PRSNT41 23
C126 0.1UF   PRSNT42 23

VCC5

PU3_ACK64# R174 2.7K 23
PU3_REQ64# R175 2.7K 23
PU4_ACK64# R172 2.7K 23
PU4_REQ64# R173 2.7K 23

AD23 R118 100 R_AD23   10,18,22,23
AD22 R117 100 R_AD22   10,18,22,23 23

PCI Slot 2 signals (left block):
AD31 B20, A20 AD30
AD29 B21, A21
B22, A22 AD28
AD27 B23, A23 AD26
AD25 B24, A24
B25, A25 AD24
C_BE#3 B26, A26
AD23 B27, A27
B28, A28 AD22
AD21 B29, A29 AD20
AD19 B30, A30 AD18
B31, A31 AD16
AD17 B32, A32
C_BE#2 B33, A33
B34, A34 FRAME# → 10,18,22,23,34
IRDY# B35, A35
B36, A36 TRDY# → 10,18,22,23,34
DEVSEL# B37, A37
B38, A38 STOP# → 10,18,22,23,34
PLOCK# B39, A39
PERR# B40, A40 SDONEP3 23
B41, A41 SBOP3 23
SERR# B42, A42
B43, A43 PAR → 10,18,22,23
C_BE#1 B44, A44 AD15
AD14 B45, A45
B46, A46 AD13
AD12 B47, A47 AD11
AD10 B48, A48
B49, A49 AD9
key
AD8 B52, A52 C_BE#0
AD7 B53, A53
B54, A54 AD6
AD5 B55, A55 AD4
AD3 B56, A56
B57, A57 AD2
AD1 B58, A58 AD0
B59, A59
PU3_ACK64# 23 B60, A60 PU3_REQ64# 23
B61, A61
B62, A62

IRDY# 10,18,22,23,34
DEVSEL# 10,18,22,23,34
PLOCK# 10,22,23,34
PERR# 10,18,22,23,34
SERR# 10,18,22,23,34

PCI Slot 3 signals (right block):
AD31 B20, A20 AD30
AD29 B21, A21
B22, A22 AD28
AD27 B23, A23 AD26
AD25 B24, A24
B25, A25 AD24
C_BE#3 B26, A26 R_AD22 23
AD23 B27, A27
B28, A28 AD22
AD21 B29, A29 AD20
AD19 B30, A30 AD18
B31, A31 AD16
AD17 B32, A32
C_BE#2 B33, A33
B34, A34 FRAME#
IRDY# B35, A35
B36, A36 TRDY#
DEVSEL# B37, A37
B38, A38 STOP#
PLOCK# B39, A39
PERR# B40, A40 SDONEP4 23
B41, A41 SBOP4 23
SERR# B42, A42
B43, A43 PAR
C_BE#1 B44, A44 AD15
AD14 B45, A45
B46, A46 AD13
AD12 B47, A47 AD11
AD10 B48, A48
B49, A49 AD9
key
AD8 B52, A52 C_BE#0
AD7 B53, A53
B54, A54 AD6
AD5 B55, A55 AD4
AD3 B56, A56
B57, A57 AD2
AD1 B58, A58 AD0
B59, A59
PU4_ACK64# 23 B60, A60 PU4_REQ64# 23
B61, A61
B62, A62

VCC3_3 VCC12- VCC5 VCC3_3 VCC5 VCC12
VCC3_3 VCC12- VCC5 VCC3_3 VCC5 VCC12

C_BE#[3:0] 10,18,22
AD[31:0] 10,18,22

IDE Connectors

Primary IDE

Secondary IDE

PDD[15:0]

J22

R333
33

PCIRST#_RP1
PCIRST_BUF#

VCC5

R336
1K

PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15

2

PDREQ
PDIOW#
PDIOR#
PIORDY
PDDACK#
IRQ14
PDA1
PDA0
PDCS#1
IDEACTP#
PDA2

R335
5.6K

R334
10K

19 20
21 22
23 24
25 26
27 28   IDE_JP
29 30
31 32
33 34
35 36
37 38   PDCS#3
39 40

P66DETECT 12

R337
470

C329
0.047UF

11 PDA[2:0]

SDD[15:0]

J21

R318
33

PCIRST#_RS1
PCIRST_BUF#

VCC5

R321
1K

SDD7	3	4	SDD8
SDD6	5	6	SDD9
SDD5	7	8	SDD10
SDD4	9	10	SDD11
SDD3	11	12	SDD12
SDD2	13	14	SDD13
SDD1	15	16	SDD14
SDD0	17	18	SDD15

2

SDREQ
SDIOW#
SDIOR#
SIORDY
SDDACK#
IRQ15
SDA1
SDA0
SDCS#1
IDEACTS#
SDA2

R320
5.6K

R319
10K

19 20
21 22
23 24
25 26
27 28   IDE_JS
29 30
31 32
33 34
35 36
37 38   SDCS#3
39 40

S66DETECT 12

R322
470

C318
0.047UF

11 SDA[2:0]

For drive side detection, stuff C329,C318.
For host side detection, no stuff C329,C318.
P66DETECT and S66DETECT can be connected to a GPI for BIOS cable detection.

VCC3_3

VCC3_3

R351
8.2K

U19

PCIRST#
8,10,12,13,14,18,21,22,23

5 VCC 6   PCIRST_BUF#   24

GND

SN74LVC07A

USB Connectors

VCC3_3

R83
300K

AC97_OC# 17

R82
0K
Do Not Stuff

VCC3_3   VCC5

R86
4.7K

C102
0.1UF

U7
TPS2042

2	IN	OUT1	7
8	OC#1	OUT2	6
5	OC#2	EN#1	3
1	GND	EN#2	4

OC#0 11
10K
R87
OC#0_RC

C109
0.1UF

VCC3_3

R91
4.7K

OC#1 11
10K
R97
OC#1_RC

C120
0.1UF

VCC3_3

R368
300K
Do Not Stuff

R88
0K

AGP_OC# 21

USBPWR1_F

L11

C99
68UF-TANT

C44
0.1UF

C98, C99 must have low ESR.

USBP0N 11
R240
15-1%
USBD0N_R
R377
0K
USBD0N

USBP0P 11
R242
15-1%
USBD0P_R
R378
0K
USBD0P

USBV0

C239
47PF

C241
47PF

R49
15K

R47
15K

R50
0K

R48
0K
Do Not Stuff

AC97_USB+ 17

AC97_USB- 17

USBG0

C38
470PF

L7

USBPWR2_F

L10

C98
68UF-TANT

C43
0.1UF

USBV1

USBP1N 11
R243
15
USBP1N_R
R46
0K
USBD1N

USBP1P 11
R244
15
USBP1P_R
R44
0K
USBD1P

USBG1

C244
47PF

C245
47PF

R45
15K

R43
15K

R41
0K

R42
0K
Do Not Stuff

C37
470PF

L6

USBAGP+ 21

USBAGP- 21

15 ohm resistors and 47pf caps should be within 1" of ICH

J3
USB_STK

1	VCC0
2	DATA0-
3	DATA0+
4	GND0
5	VCC1
6	DATA1-
7	DATA1+
8	GND1

Place caps close to connector.
C39-C42 for test and debug only.

C42
47PF

C41
47PF

C40
47PF

C39
47PF

Parallel Port

VCC5

CR1
1 ▷ 3   VCC5_DB25_CR
MMBD914LT1

R40 2.2K

RP1 2.2K
RP2 2.2K
RP3 2.2K
RP4 2.2K

J6
DB25_DB9_STK

SLCT   14 ←   P13
P25
PE   14 ←   P12
P24
BUSY   14 ←   P11
P23
ACK#   14 ←   P10
P22
P9
PDR[7:0]   14 ←   P21
P8

RP19
PDR7   1   8   PDR7_R   P20
PDR6   2   7   PDR6_R   P7
PDR5   3   6   PDR5_R   P19
PDR4   4   5   PDR4_R   P6
33   P18

RP18
PDR3   1   8   PDR3_R   P5
PDR2   2   7   PDR2_R   P17
SLIN#   14 →   3   6   SLIN#_R   P4
PAR_INIT#   14 →   4   5   PAR_INIT#_R   P16
33   P3
ERR#   14 ←   P15
P2
P14
P1

RP20
PDR1   8   1   PDR1_R
PDR0   7   2   PDR0_R
AFD#   14 →   6   3   AFD#_R
STB#   14 →   5   4   STB#_R
33

C81 180PF
CP2 180PF
CP2 180PF
CP2 180PF
CP2 180PF
CP2 180PF
180PF
180PF
CP3 180PF
180PF
CP3 180PF
CP3 180PF
CP3 180PF
180PF
CP4 180PF
180PF
CP4 180PF
CP4 180PF
CP4 180PF
180PF
CP5 180PF
180PF
CP5 180PF
CP5 180PF
CP5 180PF

Serial Ports

U4 — GD75232

VCC5 — 20 VCC
VCC12 — 1 VCC12

DCD#0	19 RY0	RA0 2	DCD0_C
RXD0	18 RY1	RA1 3	DSR0_C
DSR#0	17 RY2	RA2 4	RXD0_C
DTR#0	16 DA0	DY0 5	RTS0_C
TXD0	15 DA1	DY1 6	TXD0_C
CTS#0	14 RY3	RA3 7	CTS0_C
RTS#0	13 DA2	DY2 8	DTR0_C
RI#0	12 RY4	RA4 9	RI0_C
	11 GND	VCC-12 10	VCC12-

COM1 — J6 DB25_DB9_STK

A1	DCD
A6	DSR
A2	RXD
A7	RTS
A3	TXD
A8	CTS
A4	DTR
A9	RI
A5	GND

Capacitors: CP1 100PF, CP8 100PF (various)

Q1 2N7002LT1
R369 10K
VCC3_3SBY
R70 47K
R69 47K
C92 1UF

CR2 BAT54C
RI_CR
RI_Q

11 ICH_RI#

U6 — GD75232

VCC5 — 20 VCC
VCC12 — 1 VCC12

DCD#1	19 RY0	RA0 2	DCD1_C
RXD1	18 RY1	RA1 3	RXD1_C
DSR#1	17 RY2	RA2 4	DSR1_C
DTR#1	16 DA0	DY0 5	DTR1_C
TXD1	15 DA1	DY1 6	TXD1_C
CTS#1	14 RY3	RA3 7	CTS1_C
RTS#1	13 DA2	DY2 8	RTS1_C
RI#1	12 RY4	RA4 9	RI1_C
	11 GND	VCC-12 10	VCC12-

COM2 — J7

1	2
3	4
5	6
7	8
9	10

Capacitors: CP7 100PF, CP6 100PF (various)

COM2 is a 2x5 pin header for a cabled port.

Keyboard/Mouse/Floppy

VCC5

RP17

Floppy Connector

1K

R328 1K

VCC5

F1
1.0A

VCC5_KBMS_F

L15

VCC5_KBMS_J 14

J1

KBDAT
L16
KBDAT_FB

KBCLK
L12
KBCLK_FB

GND_KBMS_C

PS/2 Kybd

MDAT
L14
MDAT_FB

MCLK
L13
MCLK_FB

PS/2 Mse

GND_KBMS_FB

C45 100PF
C33 100PF
C32 100PF
C46 100PF
C47 0.1UF

L9

J23

14 DRVDEN#0
14 DRVDEN#1
14 INDEX#
14 MTR#0
14 DS#0
14 DIR#
14 STEP#
14 WDATA#
14 WGATE#
14 TRK#0
14 WRTPRT#
14 RDATA#
14 HDSEL#
14 DSKCHG#

Game Port

VCC5   VCC5   VCC5   VCC5   VCC5   VCC5   VCC5

R39 4.7K   R35 4.7K   R37 1K   R36 1K   R32 1K   R33 1K

J5
DB15_AUD_STK
31

Signal	Pin
	1
	9
J1BUTTON1	2
J2BUTTON1	10
JOY1X — JOY1X_R	3
JOY2X — JOY2X_R	11
MIDI_OUT — MIDI_OUT_R	4
	12
JOY2Y_R	5
	13
JOY1Y_R	6
	14
	7
MIDI_IN_R	15
	8
	32

14 ← J1BUTTON1
14 ← J2BUTTON1
14 ← JOY1X
14 ← JOY2X
14 ← MIDI_OUT
14 ← JOY2Y
14 ← JOY1Y
14 ← J2BUTTON2
14 ← J1BUTTON2
14 ← MIDI_IN

R21 2.2K 5%   JOY1X_R
R22 2.2K 5%   JOY2X_R
R34 47   MIDI_OUT_R
R23 2.2K 5%   JOY1Y_R
R24 2.2K 5%
R38 47   MIDI_IN_R

C69 0.01UF 25V 10%
C68 0.01UF 25V 10%
C67 0.01UF 25V 10%
C66 0.01UF 25V 10%

C56 470PF
C55 47PF 50V
C54 47PF
C53 470PF
C52 47PF 50V
C51 47PF 50V

Tie game port capacitors together and to SIO AVSS. Tie to system ground at only a single point.

VRM

VRM requirements are based on VRM8.4 spec .

VCC5

L19
1UH
DO3316P-102

Place caps next to output FETs.
C82,C87,C107,C111 must support >6A of RMS current.

VRM_VCC5

R80 10K
C140 10UF
C90 0.1UF
C87 1200UF
C111 1200UF
C107 1200UF
C82 1200UF

VCC12
R71 5.1-5%
PVCC_R
C97 1UF-X7R

VCC3_3 VCC5
R332 220
R53 5.6K

VRM_PWRGD → 33

C118, C119 must be next to FETs.

C72 0.01UF
R54 2.7K
VRM_IMAX

C118 1UF-X7R

Q3 SI4410DY
Q2 SI4410DY

VCCVID

VID[4:0]
3

VID0
VID1
VID2
VID3
VID4

RP21
1 8
2 7
3 6
4 5
0K

R398 0K

VID0_R
VID1_R
VID2_R
VID3_R
VID4_R

VID Override Jumpers
Default JP6-JP10 OUT.
Remove RP21, R398 for VID override.

JP6 JP8 JP10 JP7 JP9

VR3

OUTEN 19 OUTEN
VID0_R 18 VID0
VID1_R 17 VID1
VID2_R 16 VID2
VID3_R 15 VID3
VID4_R 14 VID4

VCC PVCC

COMP SS SGND GND SENSE

LTC1753

VRM_COMP

C73 150PF
R55 8.2K
C75 0.1UF
C86 0.1UF
No Stuff C106
C71 1000PF

VRM_COMP_R
C74 0.01UF

IMAX 7 VRM_IMAX
PWRGD 13 VRM_FAULT
FAULT# 12
G1 20 VRM_G1
IFB 8 VRM_IFB
G2 1 VRM_G2
VFB 11 VRM_VFB

R65 20

IFB_Q
L18
1.0UH-20A
ETQP6F0R8L

Q4 SI4410DY
Q5 SI4410DY
C119 1UF-X7R

C100 2200UF
C93 2200UF
C103 2200UF
C366 2200UF

Sanyo 4SP2200M

VCCVID1 VCC12 VCC5
VCC5 VCC12 VCCVID1
VCC3_3 VCC3_3

J14
VRM8_4

A1 V5_IN0   V5_IN3 B1
A2 V5_IN1   V5_IN4 B2
A3 V5_IN2   V5_IN5 B3
A4 V12_IN0 V12_IN1 B4
A5 V12_IN2 RSV   B5
A6 ISHARE   OUT_EN B6
A7 VID0   VID1   B7
A8 VID2   VID3   B8
A9 VID4   PWR_GOOD B9
A10 V_OUT0   GND0   B10
A11 GND0   V_OUT6 B11
A12 V_OUT1   GND6   B12
A13 GND1   V_OUT7 B13
A14 V_OUT2   GND7   B14
A15 GND2   V_OUT8 B15
A16 V_OUT3   GND8   B16
A17 GND3   V_OUT9 B17
A18 V_OUT4   GND9   B18
A19 GND4   V_OUT10 B19
A20 V_OUT5   GND10   B20

R371 10K
R370 220

30 VID1_0R
30 VID1_2R
30 VID1_4R

VID1_1R 30
VID1_3R 30

VRM1_PWRGD 33

VID1[4:0]
5

VID1[0]
VID1[1]
VID1[2]
VID1[3]
VID1[4]

RP24
1 8
2 7
3 6
4 5
0K

R104 0K

VID1_0R 30
VID1_1R 30
VID1_2R 30
VID1_3R 30
VID1_4R 30

JP16 JP27 JP29 JP28 JP30

VID Override Jumpers
Default JP16, JP27-JP30 OUT.
Remove RP24, R104 for VID override.

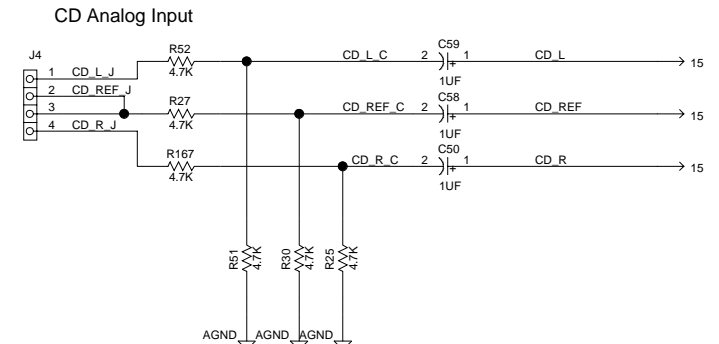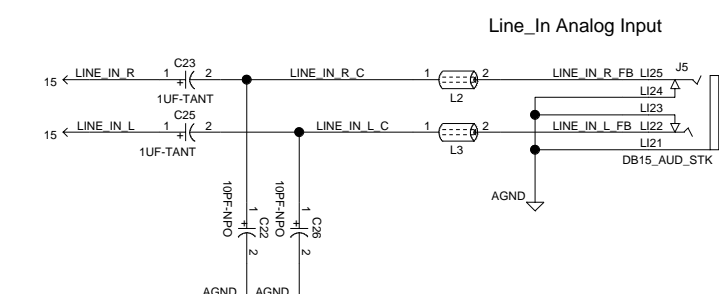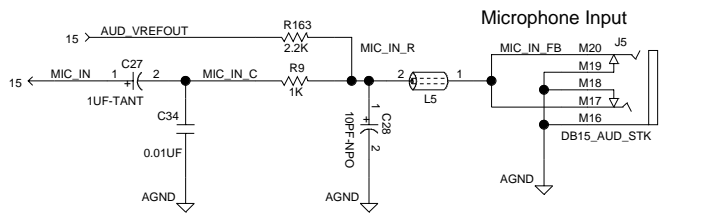TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV:
VRM   3.03

intel® PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
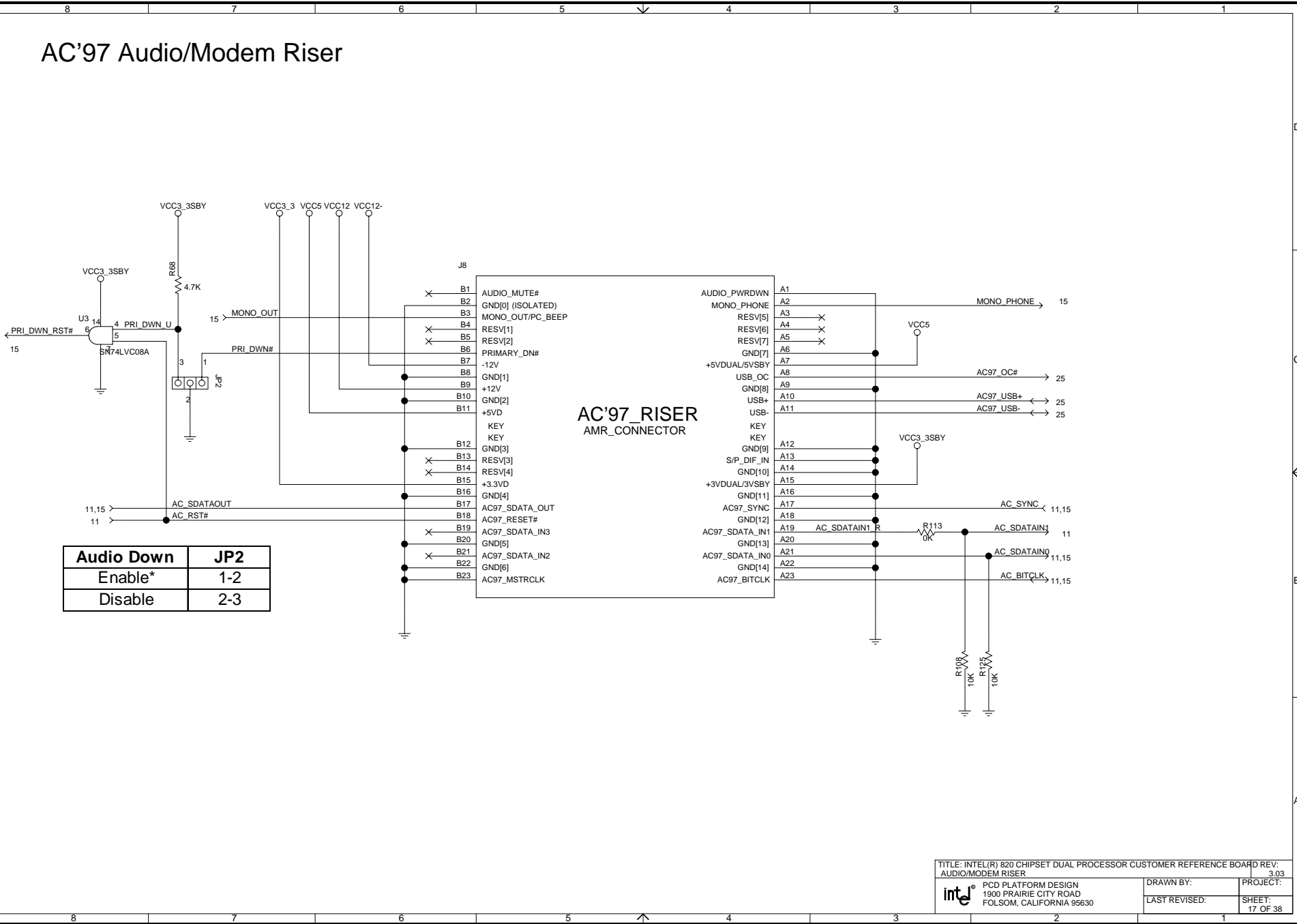
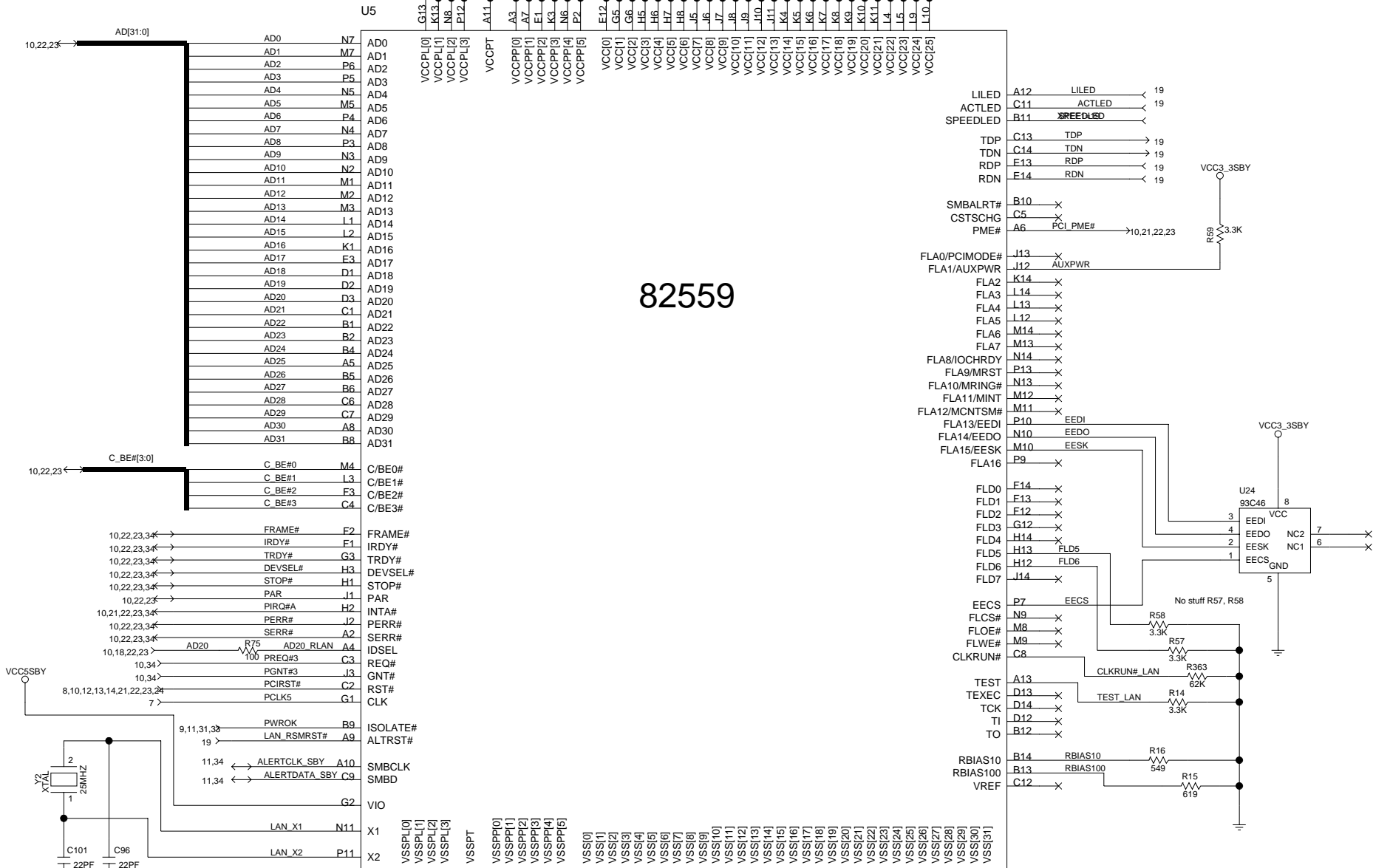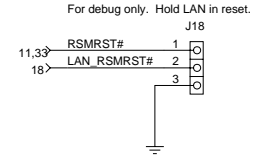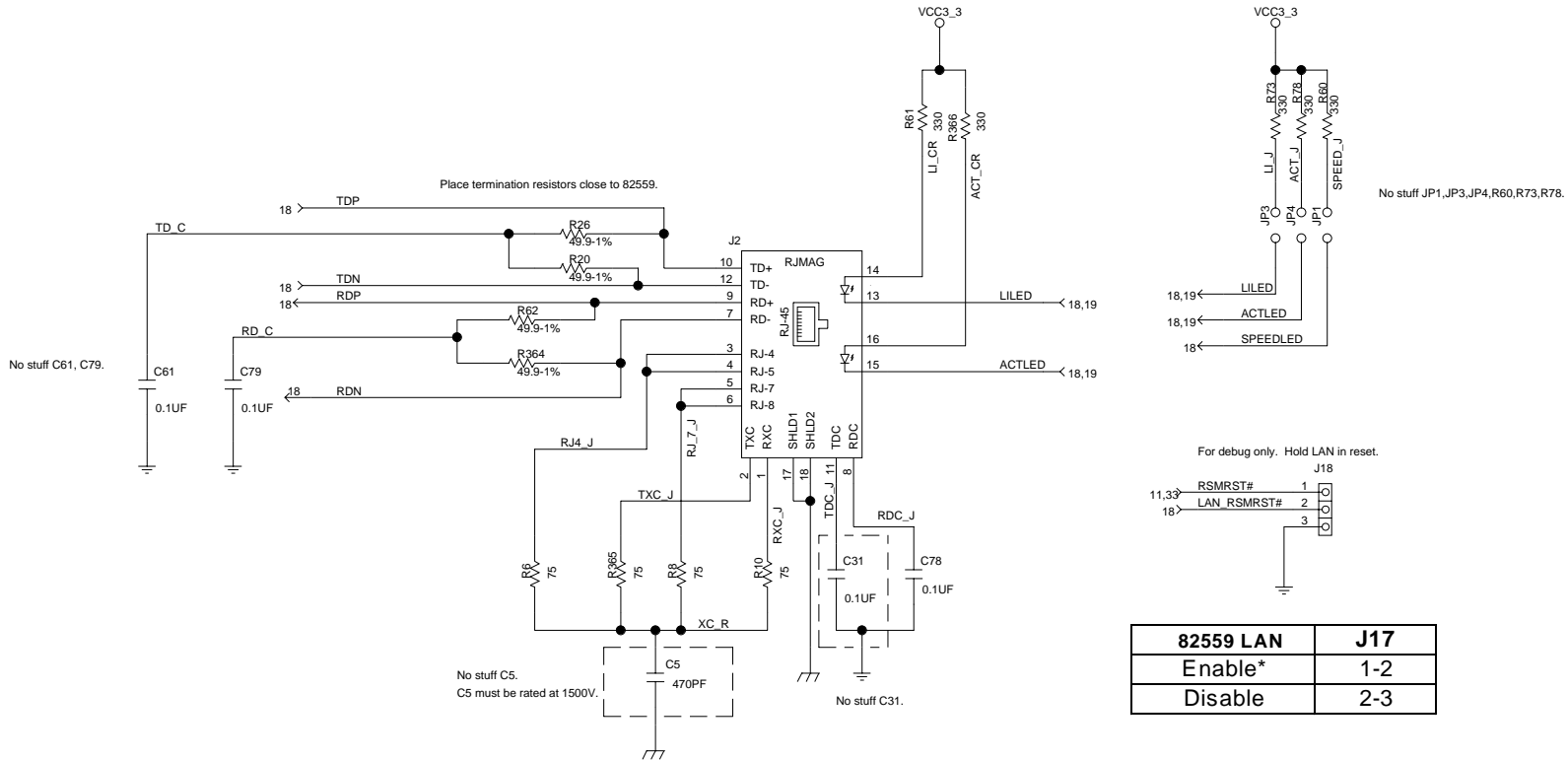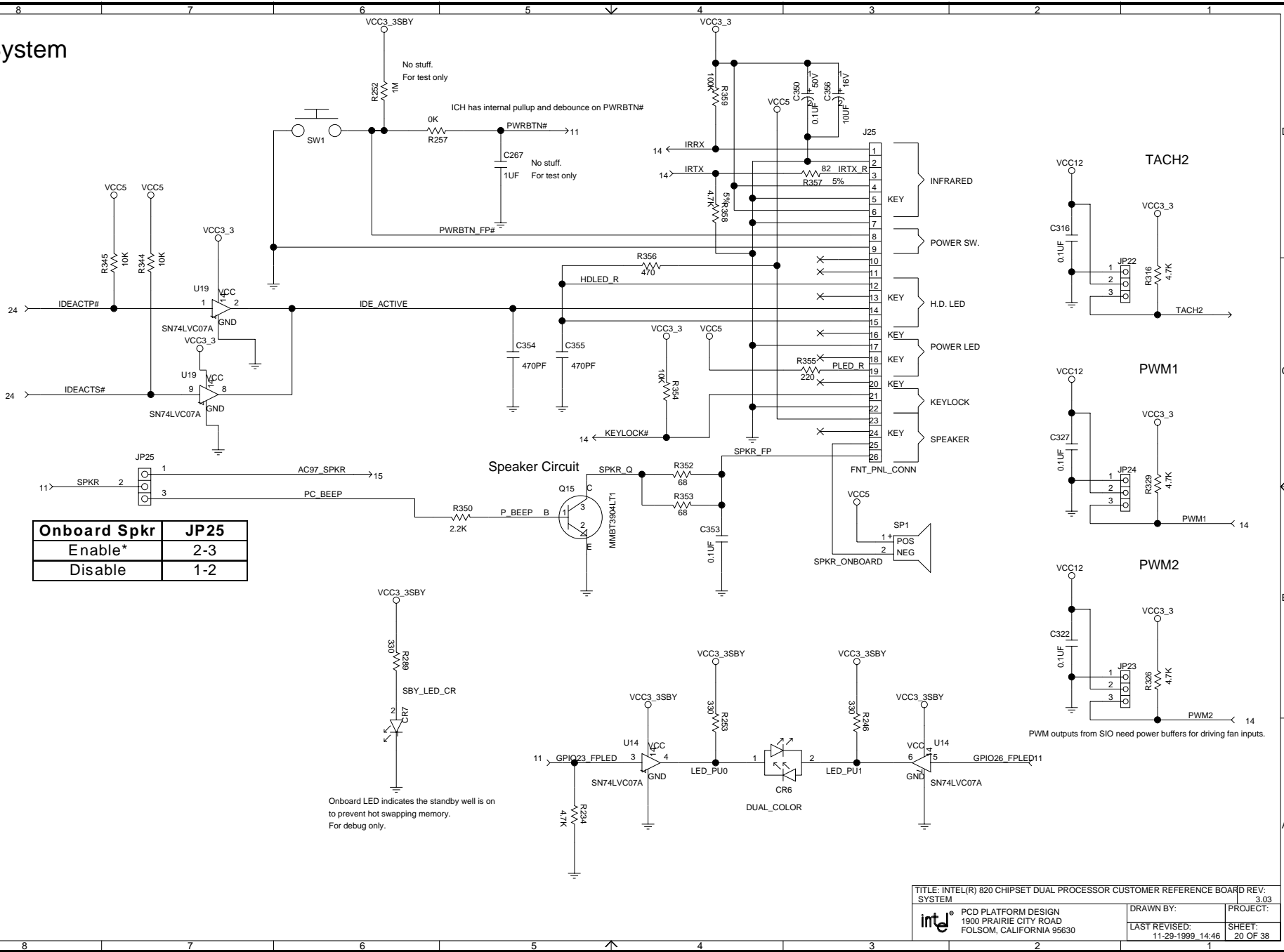DRAWN BY: PROJECT:

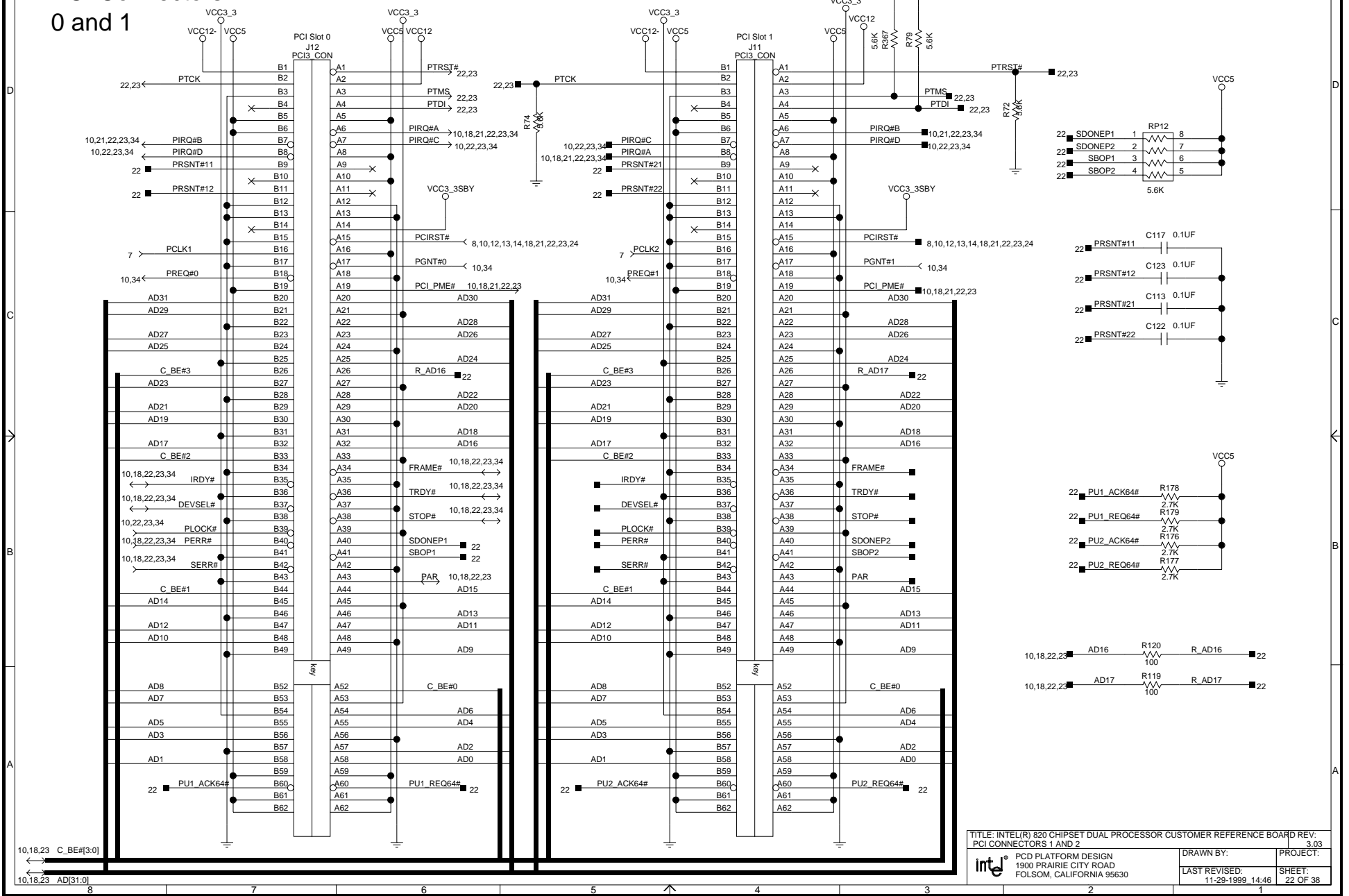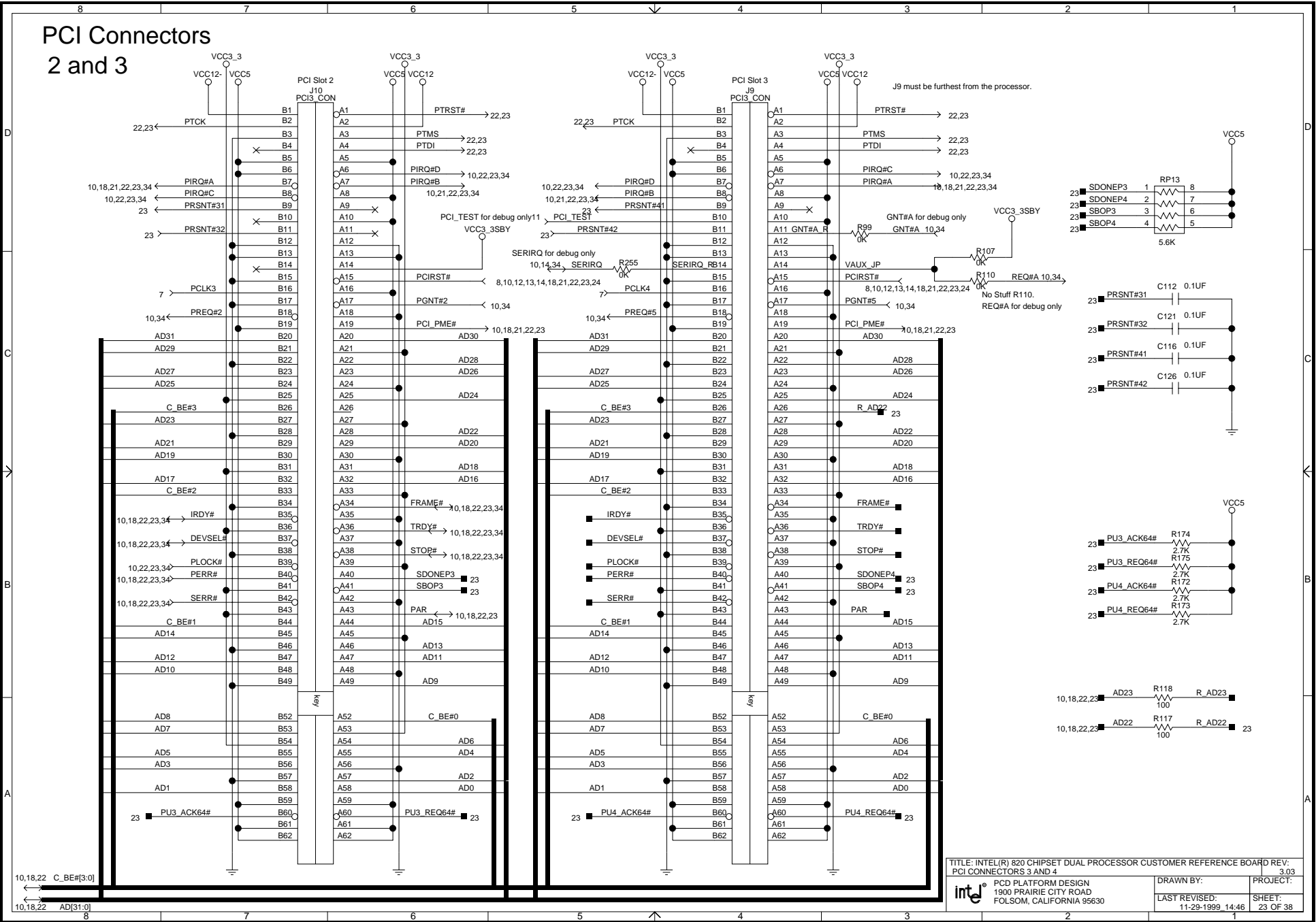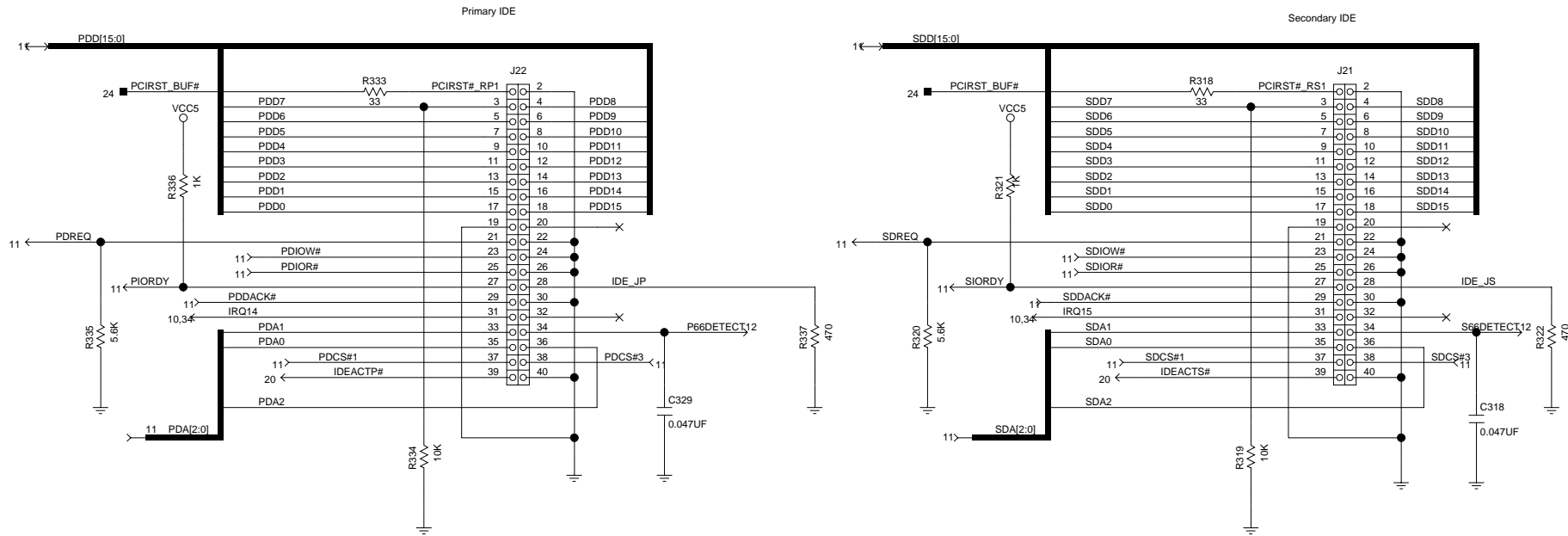LAST REVISED: SHEET:
11-29-1999_14:46   30 OF 38

Voltage Regulators

VCC 5V DUAL VOLTAGE SWITCHER

The VCC5DUAL plane should not drive any logic components requiring 5V.
It should be used only for further regulation of lower voltage power planes
because the true voltage of VCC5DUAL will not remain constant
Rdson of the FET is not negligible for large currents

SN74LVC07A has 5V input and output tolerance.

VCC12
VCC5SBY
VCC5
VCC5DUAL

C347 47UF
C324 47UF
R330 1K

VCC5SBY
VCC3_3SBY
U18 74LS132
U14 SN74LVC07A
VCC

SLP_S3# 11,33
PWROK 9,11,18,33
VD_G1
VD_G2
VD_G3
R331 1K
R340 1K

Q13 MMBT3904LT1
VCC5DUAL_R

Q12 SI4562DY
S1 D1
G1 D1A
S2 D2
G2 D2A

VCC3_3

C352 1500UF
C336 1500UF

VCC1_8
R381 1K
R382 1K
R383 1K

Q18 MMBT3904LT1

TYPEDET# 21
R379 10K
TYPEDET_R#

Q7 MMBT3904LT1

AGP VDDQ VOLTAGE REGULATOR

VCC3_3
VCC12
VDDQ

C193 10UF
C173 47UF

220UF
C160

VR6 LT1575
SHDN IPOS
VIN   INEG
GND   GATE   VDDQ_G R135 5.1-5%   VDDQ_G2
FB   COMP

C174 1UF
R158 2.2K

VDDQ_COMP
C164 10PF
VDDQ_COMP_R R137 7.5K-1%
C168 47UF

Q6 IRL2203NS

VDDQ_FB

R141 301 1%
C200 1UF-X7R
C225 1UF-X7R
C211 1UF-X7R
C179 1UF-X7R
C242 22UF

R146 1.21K-1%

Route VR6 GND to VDDQ output caps and then via to ground.

VTT 1.5 VOLTAGE REGULATOR

VCC3_3
VTT1_5

VR4 LT1585A-1_5
VOUT
VIN
GND

C104 1UF-X7R
C124 100UF
C142 100UF

VCC 1.8 VOLTAGE REGULATOR

VCC3_3
VCC1_8
VCC2_5SBY
BAT17 CR11

VR8 LT1587ADJ
VOUT
VIN
ADJ   VCC1_8_ADJ

R311 301-1%
R309 131-1%

C319 100UF
C268 1UF-X7R
C311 100UF
C368 100UF
C372 100UF

Place C311 at regulator.
Place C108, C333 at RIMMs

VCC2_5 VOLTAGE REGULATOR

VCC5
VCC2_5

VR5 LT1587ADJ
VOUT
VIN
ADJ   VCC2_5_ADJ

R134 100-1%
R133 100-1%

C159 100UF
C161 1UF-X7R
C167 100UF

VCC3_3SBY VOLTAGE REGULATOR

VCC5DUAL
VCC3_3SBY

VR1 LT1529-3_3
VIN   VOUT
SHDN# SENSE
GND   TAB

C15 330UF-T510
C35 1UF-X7R
C91 100UF

Voltage Regulators

VCC 2.5 Standby Voltage Regulator

VCC5DUAL

C315 1UF-X7R
C314 100UF

VCC2_5SBY_TG
VCC2_5SBY_SW

VR7
LT1435

4	SFB	VIN	13
1	COSC	TG	16
2	RUN/SS	SW	14
3	ITH	INTVCC	12
5	SGND	BOOST	15
6	VOSENSE	BG	11
9	EXTVCC	PGND	10
7	SENSE-		
8	SENSE+		

VCC2_5SBY_COSC
VCC2_5SBY_RUN
VCC2_5SBY_ITH

CR8
3   1
MMBD914LT1

11   SLP_S5#

C295 68PF
C294 0.1UF

C296 330PF
C293 100PF
R295 SBY_ITH_R 10K

C292 100PF

C299 1000PF

VCC2_5SBY_INTVCC
V_BOOST
C306 4.7UF
C307 0.1UF
C312 0.1UF
CR9
CMDSH-3
VCC2_5SBY_BG

D3 D4 S2
Q11
SI4966DY
D1 S1 G1
D2

MBRS140T3
CR10

L23
10UH
CDRH125

VCC2_5SBY_L

R325
0.01

R297 100-1%
R301 100-1%

Do not stuff C304.

C304 100PF

R302 11K
R294 10K

C325 330UF
C326 330UF

VCC2_5SBY

AVX 330uF
TPS x2

VCC2_5SBY_SENSE+
VCC2_5SBY_SENSE-
VCC2_5SBY_VOSENSE

Do not stuff C292.

VCMOS Generator For Rambus

VCC2_5SBY

R259 35.7-1%

VCMOS1_8SBY

R258 100-1%
C263 0.1UF

Power Connector

ITP Reset circuit. For debug only.

74LVC14A has 5V input tolerance.

VCC3_3SBY   VCC3_3SBY   VCC3_3SBY

U15   POK_U1   U15   POK_U2   U3   POK_U3
74LVC14A   74LVC14A   SN74LVC08A

DBRESET#

330 ohm pullup to VCC3_3 located on CPU sheet.

R339 0K

ATX Connector

VCC5SBY   VCC12-   VCC3_3

VCC5SBY

VCC5M   VCC12

VCC3_3SBY

R347 4.7K

VCC5

J24

11   3_3V11   3_3V1   1
12   -12V   3_3V2   2
13   GND13   GND3   3
14   PS_0N   5V4   4
15   GND15   GND5   5
16   GND16   5V6   6
17   GND17   GND7   7
18   -5V   PW_OK   8
19   5V19   5VSB   9
20   5V20   12V   10

ATX

11,31   SLP_S3#   U20 VCC   SLP_S3
SN74LVC06A

SN74LVC06A has 5V output tolerance.

VCC2_5

VCC3_3SBY

R96 330

SN74LVC06A has 5V input tolerance.

U20 VCC
SN74LVC06A

PWRGOOD 4,6

ATX_PWOK   R342 0K   ATX_PWOK_R

No stuff R342 when ITP is used.

U18
74LS132 VCC
9
10   GND

PWROK_INV

VCC3_3SBY

R349 4.7K

VCC3_3SBY

U20 VCC
SN74LVC06A

PWROK 9,11,18,31

220 ohm pullup to VCC3_3 is located on VRM sheet.

VCC3_3SBY

VCC3_3SBY

U23   30   VRM_PWRGD   U9
74LVC14A   SN74LVC08A

4   SLOTOCC0#

VCC3_3SBY

U22
74LVC32

VCC3_3SBY

U9
SN74LVC08A

VCC3_3SBY

R251 22K   RSMRST_U

VCC3_3SBY

U15
74LVC14A

RSMRST

VCC3_3SBY

U15
74LVC14A

RSMRST#   11,19

R348 1M   No stuff.
For test only

VCC3_3SBY

U23   30   VRM1_PWRGD   U26
74LVC14A   SN74LVC08A

6   SLOTOCC1#

VCC5SBY

C266 1UF

R288 1M

No stuff.
For test only

Reset Button

SW2   RSTBTN_SW   R343 22

JP12

R372 220K

C335 0.01UF   C328 10UF

VCC3_3SBY

U23
74LVC14A   RS_SCH

VCC3_3SBY

U23
74LVC14A

Resume Reset circuitry
using a 22 msec delay
and Schmitt trigger logic.

PCI/AGP Pullups/Pulldowns

PCI

VCC5

RP6		
PIRQ#C	7	8	1
PIRQ#D	6	3
	5	4

2.7K

10,22,23 PIRQ#C
10,22,23 PIRQ#D

RP10		
FRAME#	8	1
IRDY#	7	2
TRDY#	6	3
DEVSEL#	5	4

2.7K

10,18,22,23 FRAME#
10,18,22,23 IRDY#
10,18,22,23 TRDY#
10,18,22,23 DEVSEL#

RP11		
STOP#	8	1
PLOCK#	7	2
PERR#	6	3
SERR#	5	4

2.7K

10,18,22,23 STOP#
10,22,23 PLOCK#
10,18,22,23 PERR#
10,18,22,23 SERR#

10,22 PREQ#0 — R112 2.7K
10,22 PREQ#1 — R111 2.7K
10,23 PREQ#2 — R115 2.7K
10,18 PREQ#3 — R216 2.7K
10 PREQ#4 — R213 2.7K
10,23 PREQ#5 — R109 2.7K

VCC3_3

RP16		
PGNT#1	8	1
PGNT#0	7	2
PGNT#3	6	3
PGNT#2	5	4

8.2K

10,22 PGNT#1
10,22 PGNT#0
10,18 PGNT#3
10,23 PGNT#2

10 PGNT#4 — R214 8.2K
10,23 PGNT#5 — R256 8.2K
10,23 REQ#A — R114 8.2K
10,23 GNT#A — R105 8.2K
10,18,21,22,23 PIRQ#A — R81 8.2K
10,21,22,23 PIRQ#B — R89 8.2K

VCC5

10,24 IRQ14 — R338 8.2K
10,24 IRQ15 — R323 8.2K

VCC3_3

3,5,11,13 SMBCLK_CORE — R235 4.7K
3,5,11,13 SMBDATA_CORE — R237 4.7K

VCC3_3SBY

11 SMB_ALERT — R236 4.7K
11,18 ALERTCLK_SBY — R13 4.7K
11,18 ALERTDATA_SBY — R12 4.7K

PROCESSOR

VCC2_5

4,6,10 PICD0 — R128 150
4,6,10 PICD1 — R124 150
4,6 FLUSH# — R84 1K
4,6,10 STPCLK# — R85 1K
4,6,10 SMI# — R374 1K
4,6,10 FERR# — R123 1K

VCC2_5

4,6,10 A20M# — R126 1K

RP7		
LINT0	8	1
LINT1	7	2
IGNNE#	6	3
HINIT#	5	4

1K

4,6,10 LINT0
4,6,10 LINT1
4,6,10 IGNNE#
4,6,10,12 HINIT#

VCC2_5

6 TESTHI1 — R393 100K
4 TESTHI — R127 100K
4,6,10 SLP# — R373 1K

VCC3_3

10,14 KBRST# — R324 8.2K
10,14 A20GATE — R327 8.2K
10,14,23 SERIRQ — R314 8.2K

AGP

VDDQ

RP15		
GIRDY#	8	1
GDEVSEL#	7	2
GPERR#	6	3
GSERR#	5	4

8.2K

9,21 GIRDY#
9,21 GDEVSEL#
21 GPERR#
21 GSERR#

RP14		
GFRAME#	1	8
GTRDY#	2	7
GSTOP#	3	6
GPAR	4	5

8.2K

9,21 GFRAME#
9,21 GTRDY#
9,21 GSTOP#
9,21 GPAR

RP9		
RBF#	7	8	1
SBSTB#	6	3
SBSTB	5	4

8.2K

9,21 RBF#
9,21 SBSTB#
9,21 SBSTB

9,21 GREQ#

RP8		
	1	8
GGNT#	2	7
PIPE#	3	6
WBF#	4	5

8.2K

9,21 GGNT#
9,21 PIPE#
9,21 WBF#

9,21 ADSTB0 — R198 8.2K
9,21 ADSTB1 — R132 8.2K
9,21 ST0 — R385 8.2K
9,21 ST1 — R384 8.2K
9,21 ST2 — R394 8.2K

9,21 ADSTB#0 — R207 8.2K — R136 8.2K
9,21 ADSTB#1 — R136 8.2K

Rambus Termination

VCC1_8

TERM_DQA[8:0]

13

TERM_DQA0 R277
TERM_DQA1 28 R279
TERM_DQA2 28 R278
TERM_DQA3 28 R281
          28

TERM_DQA4 R280
TERM_DQA5 28 R283
TERM_DQA6 28 R282
TERM_DQA7 28 R285
          28

TERM_DQB[8:0]

13

TERM_DQA8 R284
TERM_DQB0 28 R268
TERM_DQB1 28 R267
TERM_DQB2 28 R266
          28

TERM_DQB3 R265
TERM_DQB4 28 R264
TERM_DQB5 28 R263
TERM_DQB6 28 R262
          28

TERM_ROW[2:0]

13

TERM_DQB7 R261
TERM_DQB8 28 R260
TERM_ROW0 28 R275
TERM_ROW1 28 R274
          28

TERM_COL[4:0]

13

TERM_ROW2 R276
TERM_COL0 28 R269
TERM_COL1 28 R271
TERM_COL2 28 R270
          28

TERM_COL3 R273
TERM_COL4 28 R272
          28

C280 0.1UF
C278 0.1UF
C281 0.1UF
C282 0.1UF
C283 0.1UF
C273 0.1UF
C275 0.1UF
C274 0.1UF
C276 0.1UF
C279 0.1UF
C271 0.1UF
C269 0.1UF
C277 0.1UF

NOTE :

Use one 0.1uF cap
per two RSL signals.

VCC1_8

R293 90.9-1%
R291 90.9-1%

13 TERM_CMD
13 TERM_SCK

R292 39.2-1%
R290 39.2-1%

Decoupling

MCH Decoupling

VCC1_8

C157	0.1UF
C212	0.1UF
C201	0.1UF
C166	0.1UF
C156	0.01UF
C213	0.01UF
C202	0.01UF
C162	0.01UF

VCC1_8

C222	0.1UF
C227	0.1UF
C229	0.1UF
C258	0.1UF

Place these caps on solder side

VDDQ

C165	0.1UF
C255	0.1UF

Place these caps on solder side
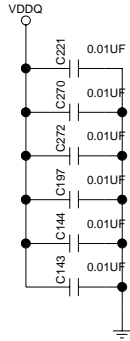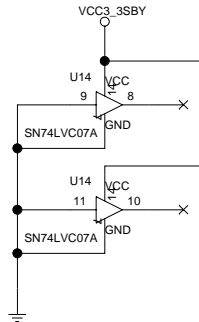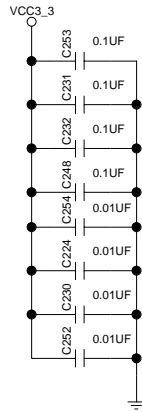
For chipset decoupling, use 0.1UF and 0.01UF decoupling capacitor at each corner of the device. If there is room, add 0.01UF capacitors in the middle of each quad.
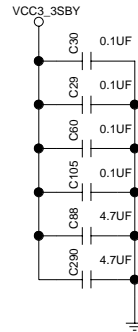
VDDQ

C221	0.01UF
C270	0.01UF
C272	0.01UF
C197	0.01UF
C144	0.01UF
C143	0.01UF

Place VDDQ capacitors within 70 mils of outer balls of MCH.

ICH Decoupling

VCC3_3

C253	0.1UF
C231	0.1UF
C232	0.1UF
C248	0.1UF
C254	0.01UF
C224	0.01UF
C230	0.01UF
C252	0.01UF

82559 Decoupling.

VCC3_3SBY

C30	0.1UF
C29	0.1UF
C60	0.1UF
C105	0.1UF
C88	4.7UF
C290	4.7UF

RIMM Decoupling

VCC2_5SBY

C303	100UF
C210	100UF
C285	100UF
C219	100UF

VCC2_5SBY

C288	100UF
C284	100UF
C289	100UF
C302	100UF

VCMOS1_8SBY

C226	0.1UF
C264	0.1UF
C235	0.1UF

Place a VCMOS1_8SBY 0.1uF cap at each RIMM.

Place 100uF caps, 0.1 ohm ESR, among RIMM connectors.

Un-used Gates

VCC3_3SBY — U3 SN74LVC08A (9,10,14 → 8)
U3 SN74LVC08A (12,13,14 → 11)

VCC3_3SBY — U15 74LVC14A (11,14 → 10)
U15 74LVC14A (13,14 → 12)

VCC3_3SBY — U20 SN74LVC06A (9,14 VCC → 8 GND)
U20 SN74LVC06A (11,14 VCC → 10 GND)
U20 SN74LVC06A (13,14 VCC → 12 GND)

VCC3_3 — U19 SN74LVC07A (3,VCC → 4 GND)
U19 SN74LVC07A (11,VCC → 10 GND)
U19 SN74LVC07A (13,VCC → 12 GND)

VCC3_3SBY — U14 SN74LVC07A (9,VCC → 8 GND)
U14 SN74LVC07A (11,VCC → 10 GND)

VCC5SBY — U18 74LS132 (2,14VCC → 3, 7 GND)
U18 74LS132 (12,13,14VCC → 11, 7 GND)

Bulk Decoupling

VCC3_3 Decoupling   VCC3_3 Decoupling   VCC2_5 Decoupling   Bulk Power Decoupling   Termination Decoupling

VCC3_3   VCC3_3   VCC2_5   VCC3_3   VCC5   VTT1_5

VCC3_3 Decoupling (first column)
- C341 0.1UF
- C340 0.1UF
- C339 0.1UF
- C338 0.1UF
- C337 0.1UF
- C334 0.1UF
- C333 0.1UF
- C332 0.1UF
- C331 0.1UF
- C330 0.1UF

VCC3_3 Decoupling (second column)
- C310 0.1UF
- C259 0.1UF
- C240 0.1UF
- C238 0.1UF
- C216 0.1UF
- C195 0.1UF
- C188 0.1UF
- C181 0.1UF
- C178 0.1UF
- C177 0.1UF

VCC2_5 Decoupling
- C176 0.1UF
- C175 0.1UF
- C172 0.1UF
- C163 0.1UF
- C154 0.1UF

Bulk Power Decoupling VCC3_3
- C148 0.1UF
- C147 0.1UF
- C370 22UF 1 2

Bulk Power Decoupling VCC5
- C146 0.1UF
- C145 0.1UF
- C369 22UF 1 2

VCC12
- C141 0.1UF
- C139 0.1UF
- C371 22UF 1 2

VCC12-
- C138 0.1UF
- C137 0.1UF
- C367 22UF 2 1

Termination Decoupling VTT1_5
- C136 0.1UF
- C135 0.1UF
- C134 0.1UF
- C133 0.1UF
- C132 0.01UF
- C131 0.01UF
- C130 0.01UF
- C129 0.01UF

Place caps at VTT pins on Slot 1 connector.

Core Voltage Decoupling

VCCVID   VCCVID   VCCVID1   VCCVID1   VCC3_3SBY

VCCVID (first)
- C65 10UF
- C128 10UF
- C127 10UF
- C125 10UF
- C115 10UF

VCCVID (second)
- C64 10UF
- C114 10UF
- C108 10UF
- C106 10UF
- C89 10UF

VCCVID1 (first)
- C364 10UF
- C342 10UF
- C343 10UF
- C344 10UF
- C345 10UF

VCCVID1 (second)
- C365 10UF
- C346 10UF
- C351 10UF
- C357 10UF
- C363 10UF

VCC3_3SBY
- C153 0.1UF
- C152 0.1UF
- C151 0.1UF
- C150 0.1UF
- C149 0.1UF

Revision History

Pg 8   Modified MCH_AGPREF circuit, changed 432 ohm to 1K ohm and 62 ohm to 80.6 ohm.
Changed value of capacitor C194 from 0.1uF to 0.01uF.

Pg 10   Modified HUBREF circuit, deleted R222, R223 & C217, changed C218 from 470pF to 0.1uF.

Pg 13   Modified RIMM connectors to eliminate 3.3V, added 0.1uF decoup caps to SVDDA & SVDDB on each RIMM.

Pg 35   Modified CMD and SCK termination values. Removed 470pF capacitors, Changed 93 ohm to 90.9 ohm,
and changed 39 ohm to 39.2 ohm resistors.

Pg 36   Deleted 3.3V decoupling for RIMM connectors. Added solder side decoup for MCH.
Changed VDDQ cap values from 0.1uF to 0.01uF.

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