



# Intel<sup>®</sup> 440EX AGPset

## Design Guide

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*April 1998*



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## Revision History

<b>Date of Revision</b>	<b>Revision</b>	<b>Description</b>
April 1998	001	Initial Release

# Introduction

# 1

This information is being provided to Intel customers designing with the Intel® 440EX AGPset. The Intel® 440EX AGPset is the Basic PC solution for the Pentium® II processor platform.

The guidelines in this document are provided in conjunction with the *Intel® 440LX AGPset Design Guide*. The *Intel® 440LX AGPset Design Guide* should be followed in all areas except those listed in this document.

The 82443EX is a full featured 82443LX with the following exceptions:

- 1.0.1 Maximum of 2 DIMM sockets
- 1.0.2 Maximum of 3 PCI slots (4-PCI masters including PIIX4)
- 1.0.3 NO ECC
- 1.0.4 Single processor with no support for IOAPIC
- 1.0.5 Nand Tree Test Mode not supported

## 1.1 Reference Documents

- Intel® 440EX AGPset datasheet  
(www: order number 290616)
- Intel® 440LX AGPset Design Guide  
(<http://developer.intel.com/design/pcisets/designex>)
- Intel® 440LX AGPset Application Notes and Specification Updates  
([www.intel.com](http://www.intel.com))

## 1.2 82443EX/82443LX Pin Differences

Pin differences between the 82443LX and 82443EX are as follows:

Ball Number	82443LX Name	82443LX Type of Pin	82443EX Name	Relationship to Reduced Feature
AF13	SRAS2#	O	NC	1.0.1
AF10	SCAS2#	O	NC	1.0.1
AC19	RCSA4#	O	NC	1.0.1
AB17	RCSA5#	O	NC	1.0.1
AF9	WE2#		NC	1.0.1
AC12	WE3#		NC	1.0.1
AD14	MAB0	O	NC	1.0.1
AF14	MAB1	O	NC	1.0.1
AE14	RCSA6#/MAB2	O	NC	1.0.1
AB14	RCSA7#/MAB3	O	NC	1.0.1
AE15	SCAS3#/MAB4	O	NC	1.0.1
AF15	SRAS3#/MAB5	O	NC	1.0.1
AA19	RCSB0#/MAB6	O	NC	1.0.1
AF16	RCSB1#/MAB7	O	NC	1.0.1
AB19	RCSB2#/MAB8	O	NC	1.0.1
AE16	RCSB3#/MAB9	O	NC	1.0.1
AF18	RCSB4#/MAB10	O	NC	1.0.1
AD18	RCSB5#/MAB11	O	NC	1.0.1
AB18	RCSB6#/MAB12	O	NC	1.0.1
AD17	RCSB7#/MAB13	O	NC	1.0.1
AF12	CDQB1#	O	NC	1.0.1
AE12	CDQB5#	O	NC	1.0.1
B12	GNT3#	O	NC	1.0.2
D12	GNT4#	O	NC	1.0.2
B13	REQ3#	I	TM1 (PU)	1.0.2
D13	REQ4#	I	TM2 (PU)	1.0.2, 1.0.5
U23	ECCERR#	O	NC	1.0.3
AD8	MECC0		NC	1.0.3
AE8	MECC1		NC	1.0.3
AF22	MECC2		NC	1.0.3
AB21	MECC3		NC	1.0.3
AC8	MECC4		NC	1.0.3
AB9	MECC5		NC	1.0.3
AE22	MECC6		NC	1.0.3
AD22	MECC7		NC	1.0.3
V24	WSC#	O	NC	1.0.4

### NOTES:

1. All pins labeled NC are NO CONNECTS and should not be connected on the motherboard
2. All pins labeled (PU) should be connected to a 4.7K to 10K ohm pull-up resistor to 3.3V on the motherboard.

## 1.3 82443EX/82443LX Register Differences

Register changes between the 82443LX and 82443EX are shown below. These specific register/bit combinations are now Reserved and should be set to their default state to support the Intel 440EX AGPset. Refer to the *Intel® 440EX AGPset* datasheet for more detail.

Register Name	Address Offset	Change To
PACCFG - PAC Configuration Register (Device 0)	50-51h	Bit 15 - Set to "1" Bit 14 - Reserved/Default Bit 13:11 - Reserved/Default Bit 8:7 - Reserved/Default Bit 6 - Reserved/Default Bit 4:3 - Reserved/Default Bit 2 - Reserved Bit 1:0 - Reserved/Default
MBSC - Memory Buffer Strength Control Register (Device 0)	6C-6Fh	Bit 23:22 - Reserved/Default Bit 13:12 - Reserved/Default Bit 11:10 - Reserved/Default Bit 5:4 - Reserved/Default Bit 3:2 - Reserved/Default Bit 1:0 - Reserved/Default
ERRCMD - Error Command Register (Device 0)	90h	Bit 1 - Reserved/Default Bit 0 - Reserved/Default
ERRSTS0 - Error Status Register 0 (Device 0)	91h	Bit 7:0 - Reserved/Default

## 1.4 Additional Information

All Intel® 440LX AGPset Applications Notes and Specification Updates apply to the Intel® 440EX AGPset. These documents are available on the WEB or through Intel Field Representatives.

<http://developer.intel.com/pcisets>

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