Intel® 810 Chipset

Design Guide

June 1999

Order Number: 290657-001

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Revision History

Revision	Description	Date
-001	Initial Release.	6/99

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Introduction

Introduction 1

This design guide provides motherboard design guidelines for Intel® 810 chipset systems. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. In addition to design guidelines, this document discusses Intel® 810 chipset system design issues (e.g., thermal requirements).

Chapters 1-7 provide generalized guidelines and Appendices A and B provide information on Intel's Customer Reference Board (CRB), including a complete set of schematics. The included schematics can be used as a reference for board designers. While the schematics cover specific designs, the core schematics will remain the same for most Intel® 810 chipset platforms.

The debug recommendations should be consulted when debugging an Intel® 810 chipset system; however, the debug recommendations should be understood before completing board design to ensure that the debug port, in addition to other debug features, will be implemented correctly.

Note: Unless otherwise specified, GMCH refers to both the 82810 and 82810-DC100 components.

Note: Unless otherwise specified, ICH refers to both the 82801AA (ICH) and 82801AB (ICH0) components.

1.1 About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. The design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- This chapter introduces the designer to the organization and purpose of this design guide, and provides a list of references of related documents. This chapter also provides an overview of the Intel® 810 chipset.
- Chapter 2, "Layout/Routing Guidelines"—This chapter provides a detailed set of motherboard layout and routing guidelines. The motherboard functional units are covered (e.g., chipset component placement, system bus routing, system memory layout, display cache interface, hub interface, IDE, AC'97, USB, interrupts, SMBUS, PCD, LPC/FWH, and RTC).
- Chapter 3, "Clocking"— This chapter provides motherboard clocking guidelines (e.g., clock architecture, routing, capacitor sites, clock power decoupling, and clock skew).
- Chapter 4, "System Design Considerations"— This chapter includes guidelines regarding power deliver, decoupling, thermal, and power sequencing.
- Chapter 5, "Design Checklist"— This chapter provides a design review checklist. ATA/66 detection, calculation of pullup/pulldown resistors, minimizing RTC ESD, and power management signals are also discussed.
- Chapter 6, "Flexible Motherboard Guidelines"— This chapter includes guidelines regarding power deliver, decoupling, thermal, and power sequencing.
- Chapter 7, "Third Party"— This chapter includes information regarding various third-party vendors who provide products to support the Intel® 810 chipset.

- Appendix A, "PCI Devices/Functions/Registers/Interrupts"— This appendix lists the PCI devices and functions supported by the Intel® 810 chipset. Also included are a list of component PCI Vendor ID, Device ID, Revision ID, Class code, Sub-class code, and Programming Interface code values. In addition, component APIC interrupt and ISA/PCI IRQs are listed.
- Appendix B, "Bill-of-Materials (BOM)"— This appendix provides a Bill-of-Materials for the Customer Reference Board (CRB) described in Appendix C.
- Appendix C, "Customer Reference Board (CRB)"— This appendix provides information on the CRB including a complete set of schematics.
- Appendix D, "Reference Information"— This appendix provides additional information relative to the Intel® 810 chipset.

1.1.1 Terminology and Definitions

Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered. This state is used in the Intel® 810 chipset CRB to satisfy the S3 ACPI power management state.
Full-power operation	During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state (S0) and the processor Stop Grant state (S1).
Suspend operation	During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports three suspend states: processor Stop Grant (S1), Suspend-to-RAM (S3) and Soft-off (S5).
Power rails	An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, +5VSB. In addition to these power rails, several other power rails are created with voltage regulators on the Intel® 810 chpset CRB.
Core power rail	A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed *directly* from the ATX power supply are: ±5V, ±12V and +3.3V.
Standby power rail	A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is 5VSB (5V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator (on the Intel® 810 chipset CRB, 3.3VSB is derived from 5V_DUAL).
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation.

1.1.2 References

- *Intel® 82810 Chipset: Intel® 82810/82810-DC100 Graphics and Memory Controller (GMCH)* Datasheet (Order Number: 290656)
- *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet (Order Number: 290655)
- *Intel® 82801 FirmWare Hub (FWH)* Datasheet (Order Number: 290658)
- *Intel® Celeron Processor* Datasheet (Order Number: 243658)
- Intel® 810 Chipset Clock Synthesizer/Driver Specification
- *VRM 8.2 DC-DC Converter Design Guidelines* (Order Number: 243733)
- *PPGA 370 Power Delivery Guidelines*
- *Pentium® II Processor AGTL+ Guidelines* (Order Number: 243330)
- *Pentium® II Processor Power Distribution Guideline (*Order Number: 243332)
- *Pentium® II Processor Developer's Manual* (Order Number: 243341)
- *Pentium® II Processor at 350 MHz and 400 MHz* Datasheet (Order Number: 243657)
- *PCI Local Bus Specification*, Revision 2.2
- *Universal Serial Bus Specification*, Revision 1.0
- *VRM 8.2 DC-DC Converter Design Guidelines*.

1.2 System Overview

The Intel® 810 chipset is the first generation Integrated Graphics chipset designed for the Intel® Celeron™ processor. The graphics accelerator architecture consists of dedicated multi-media engines executing in parallel to deliver high performance 3D, 2D, and motion compensation video capabilities. An integrated centralized memory arbiter allocates memory bandwidth to multiple system agents to optimize system memory utilization. A new chipset component interconnect, the hub interface, is designed into the Intel® 810 chipset to provide an efficient communication channel between the memory controller hub and the I/O hub controller.

The Intel® 810 chipset architecture also enables a new security and manageability infrastructure through the Firmware Hub component.

An ACPI compliant Intel® 810 chipset platform can support the *Full-on (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4),* and *Soft-off (S5)* power management states. Through the use of an appropriate LAN device, the Intel® 810 chipset also supports *wake-on-LAN** for remote administration and troubleshooting.

The Intel® 810 chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the Intel® 810 chipset platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC’97 allows the OEM to use *software configurable* AC’97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices.

The Intel® 810 chipset contains three core components:

- Host Controller
  - 82810 Graphics and Memory Controller Hub (GMCH)
  - 82810-DC100 Graphics and Memory Controller Hub (GMCH)
- I/O Controller Hub
  - 82801AA (ICH)
  - 82801AB (ICH0)
- 82802 Firmware Hub (FWH)

The GMCH integrates a 66/100MHz, P6 family system bus controller, integrated 2D/3D graphics accelerator, 100 MHz SDRAM controller and a high-speed hub interface for communication with the I/O Controller Hub (ICH). The integrates an Ultra ATA/33 (82801AB ICH0) or Ultra ATA/66 (82801AA ICH) controller, USB host controller, LPC interface controller, FWH interface controller, PCI interface controller, AC'97 digital controller and a hub interface for communication with the GMCH.

The Intel® Celeron™ processor PPGA is the next addition to the Intel® Celeron™ processor product line. The Intel® Celeron™ processor PPGA implements a Dynamic Execution micro-architecture and executes MMX™ media technology instructions for enhanced media and communication performance.

The Intel® Celeron™ processor PPGA is based on a P6 family processor core, but is provided in a Plastic Pin Grid Array (PPGA) package for use in low cost systems in the Basic PC market segment. The Intel® Celeron™ processor PPGA utilizes the AGTL+ system bus used by the Pentium II processor with support limited to single processor-based systems. The Intel® Celeron™ processor PPGA includes an integrated 128 KB second level cache with separate 16K instruction and 16K data level one caches. The second level cache is capable of caching 4 GB of system memory.

1.2.1 Graphics and Memory Controller Hub (GMCH)

The GMCH (82810 and 82810-DC100) provides the interconnect between the SDRAM and the rest of the system logic:

- 421 Mini BGA
- Integrated Graphics controller
- 230 MHz RAMDAC
- Support for Intel® Celeron™ processors with a 66 MHz or 100 MHz system bus.
- 100 MHz SDRAM interface supporting 64 MB/256 MB/512 MB with 16Mb/64Mb/128Mb SDRAM technology
- Optional 4 MB Display Cache (82810-DC100 only)
- Downstream hub interface for access to the ICH
- TV-Out/Flat Panel Display support

1.2.2 I/O Controller Hub (82801AA ICH / 82801AB ICH0)

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system:

- 241 Mini BGA
- Upstream hub interface for access to the GMCH
- PCI 2.2 interface (4 PCI Req/Grant Pairs for 82801AB ICH0, 6 PCI Req/Grant Pairs for 82801AA ICH)
- Bus Master IDE controller; supports either Ultra ATA/33 (82801AB ICH0) or Ultra ATA/66 (82801AA ICH)
- USB controller
- SMBus controller
- FWH interface
- LPC interface
- AC’97 2.1 interface
- Integrated System Management Controller
- Alert-on-LAN (82801AA ICH only)
- Interrupt controller

1.2.3 Firmware Hub (FWH)

The 82802 FWH component is a key element to enabling a new security and manageability infrastructure for the PC platform. The device operates under the FWH interface and protocol. The hardware features of this device include:

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 GPI’s

1.2.4 System Configurations

Figure 1-1. Intel® 810 Chipset Non Display Cache Configuration

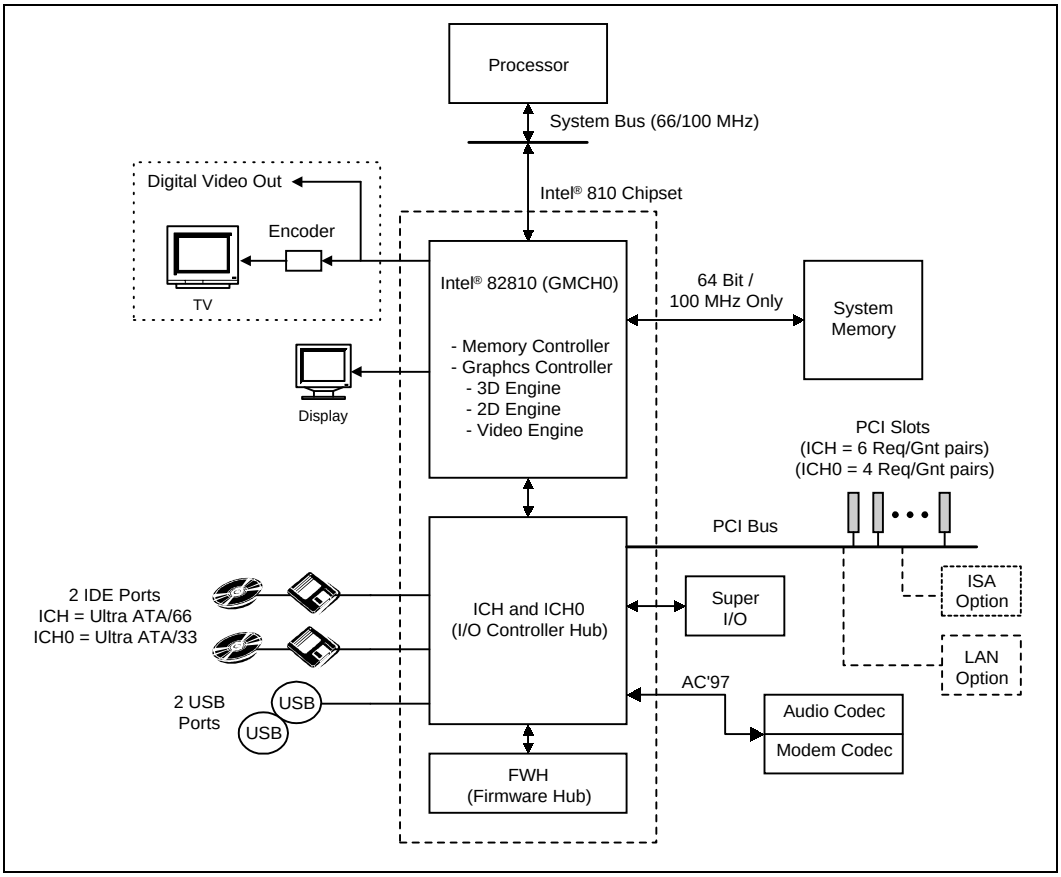
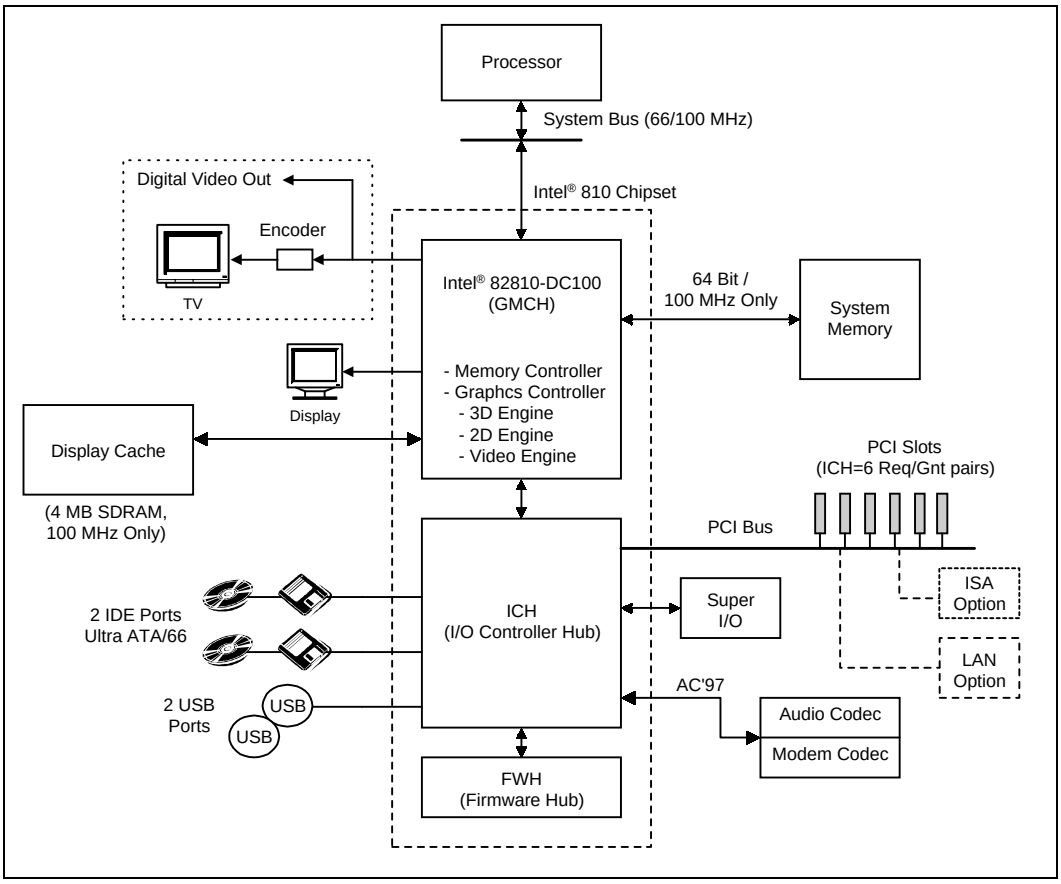


Figure 1-2. Intel® 810 Chipset with Display Cache Configuration



1.3 Platform Initiatives

1.3.1 Hub Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC'97 and Ultra ATA/66, coupled with the existing USB, I/O requirements could impact PCI bus performance. The Intel® 810 chipset's *hub interface architecture* ensures that the I/O subsystem (both PCI and the integrated I/O features (IDE, AC'97, USB, etc.)), receives adequate bandwidth. By placing the I/O bridge on the hub interface (instead of PCI), the hub architecture ensures that both the I/O functions integrated into the ICH and the PCI peripherals obtain the bandwidth necessary for peak performance.

1.3.2 Manageability

The Intel® 810 chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

processor Present Indicator

The ICH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH will reboot the system.

Function Disable

The ICH provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect

The ICH provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The ICH can be programmed to generate an SMI# or TCO event due to an active INTRUDER# signal.

Alert-On-LAN* (82801AA ICH only)

The ICH supports Alert-On-LAN*. In response to a TCO event (intruder detect, thermal event, processor not booting) the ICH sends a hardcoded message over the SMBus. A LAN controller supporting the Alert-On-LAN* protocol can decode this SMBus message and send a message over the network to alert the network manager.

1.3.3 AC’97

The *Audio Codec ’97* (AC’97) Specification defines a digital link that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and an MC. The AC’97 Specification defines the interface between the system logic and the audio or modem codec known as the *AC’97 Digital Link*.

The ability to add cost-effective audio and modem solutions as the platform migrates away from ISA is important. The AC’97 audio and modem components are software configurable, reducing configuration errors. The Intel® 810 chipset’s AC’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC’97 digital link. Using the Intel® 810 chipset’s integrated AC’97 digital link reduces cost and eases migration from ISA.

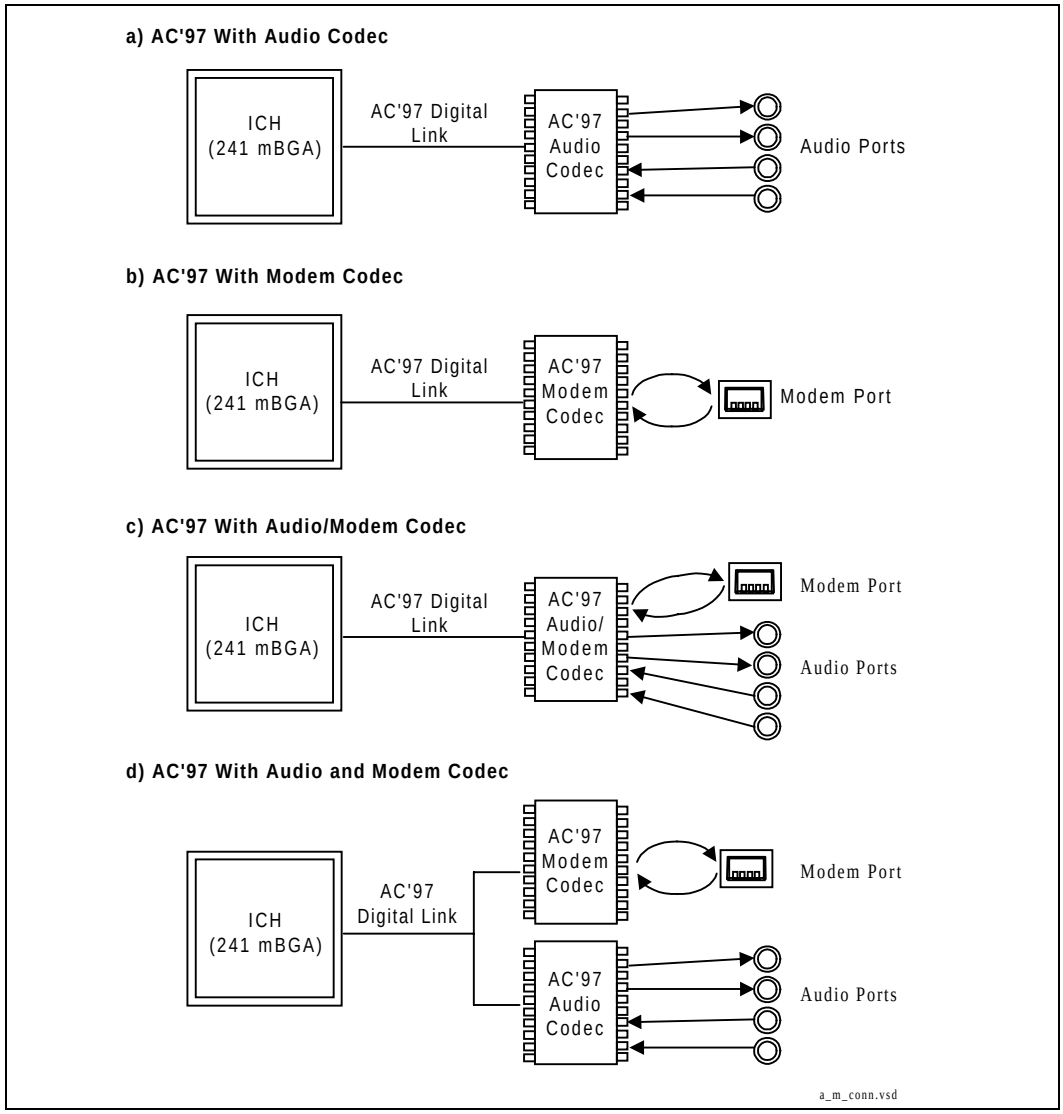
The ICH is an AC’97 compliant controller that supports up to two codecs with independent PCI functions for audio and modem. The ICH communicates with the codec(s) via a digital serial link called the AC-link. All digital audio/modem streams and command/status information is communicated over the AC-link. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

By using an audio codec, the AC’97 digital link allows for cost-effective, high-quality, integrated audio on the Intel® 810 chipset platform. In addition, an AC’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC’97. The

Intel® 810 chipset's integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec (Figure 1-3 a) or a modem with a modem codec (Figure 1-3 b). For systems requiring both audio and a modem, there are two solutions. The audio codec and the modem codec can be integrated into an AMC (Figure 1-3 c), or separate audio and modem codecs can be connected to the ICH (Figure 1-3 d).

The modem implementation for different countries should be considered as telephone systems vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. Intel is developing an AC'97 digital link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

Figure 1-3. AC'97 with Audio and Modem Codec Connections



1.3.4 Low Pin Count (LPC) Interface

In the Intel® 810 chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of devices offered and features supported.

In addition, depending on system requirements, a device bay controller and USB hub could be integrated into the LPC Super I/O component. For systems requiring ISA support, an ISA-IRQ to serial-IRQ converter is required. Potentially, this converter could be integrated into the Super I/O.

1.3.5 *Security – the Intel® Random Number Generator*

The Intel® 810 chipset features the first of Intel's platform security features, the Intel Random Number Generator (RNG). The Intel RNG is a component of the 82802 Firmware Hub (FWH), and it supplies applications and security middleware products with true non-deterministic random numbers (through the Intel® Security Driver).

Better random numbers lead to better security. Most cryptographic functions, especially functions that provide authentication or encryption services, require random numbers for purposes such as key generation. One attack on those cryptographic functions is to predict the random numbers being used to generate those keys; current methods that use system and user input to seed a pseudo random number generator have shown to be susceptible to those attacks. The Intel® RNG uses thermal noise across a resistor to generate true non-deterministic, unpredictable random numbers.

2

Layout and Routing Guidelines

Layout and Routing Guidelines 2

This chapter describes motherboard layout and routing guidelines for Intel® 810 chipset systems. This chapter does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

Note: **If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design.** Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from these guidelines Should be simulated.

2.1 General Recommendations

The trace impedance typically noted (i.e., 60 ohm ±15%) is the “nominal” trace impedance for a 5 mil wide trace (i.e., the impedance of the trace when not subjected to the fields created by changing current in neighboring traces). When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

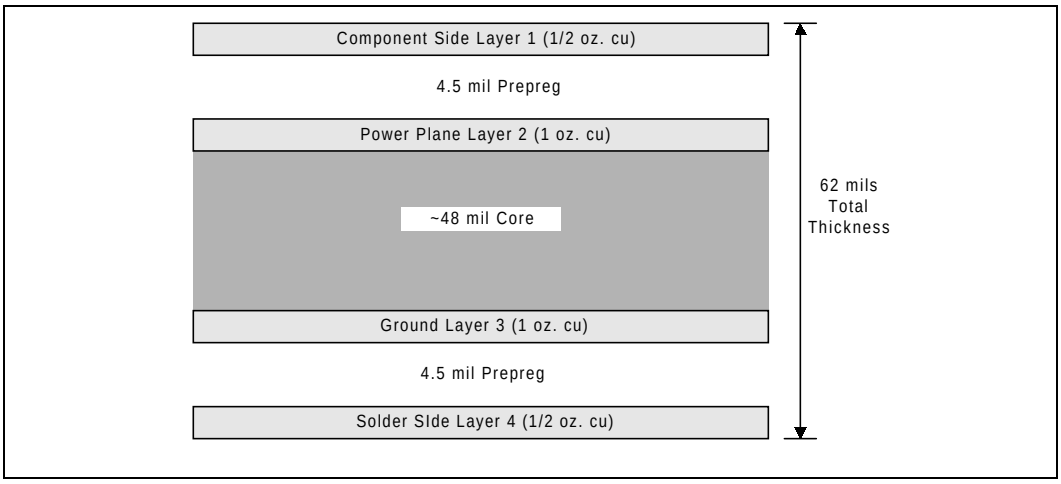
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using the *stack-up* (refer to Figure 2-1). If this stack-up is not used, simulations should be completed.

2.2 Nominal Board Stackup

The Intel® 810 chipset platform requires a board stackup yielding a target impedance of 60 ohm ±15% with a 5 mil nominal trace width. Figure 2-1 presents an example stackup to achieve this. It is a
4-layer fabrication construction using 53% resin, FR4 material.

Figure 2-1. Nominal Board Stackup



2.3 Component Quadrant Layouts

Figure 2-2. GMCH Quadrant Layout (topview)

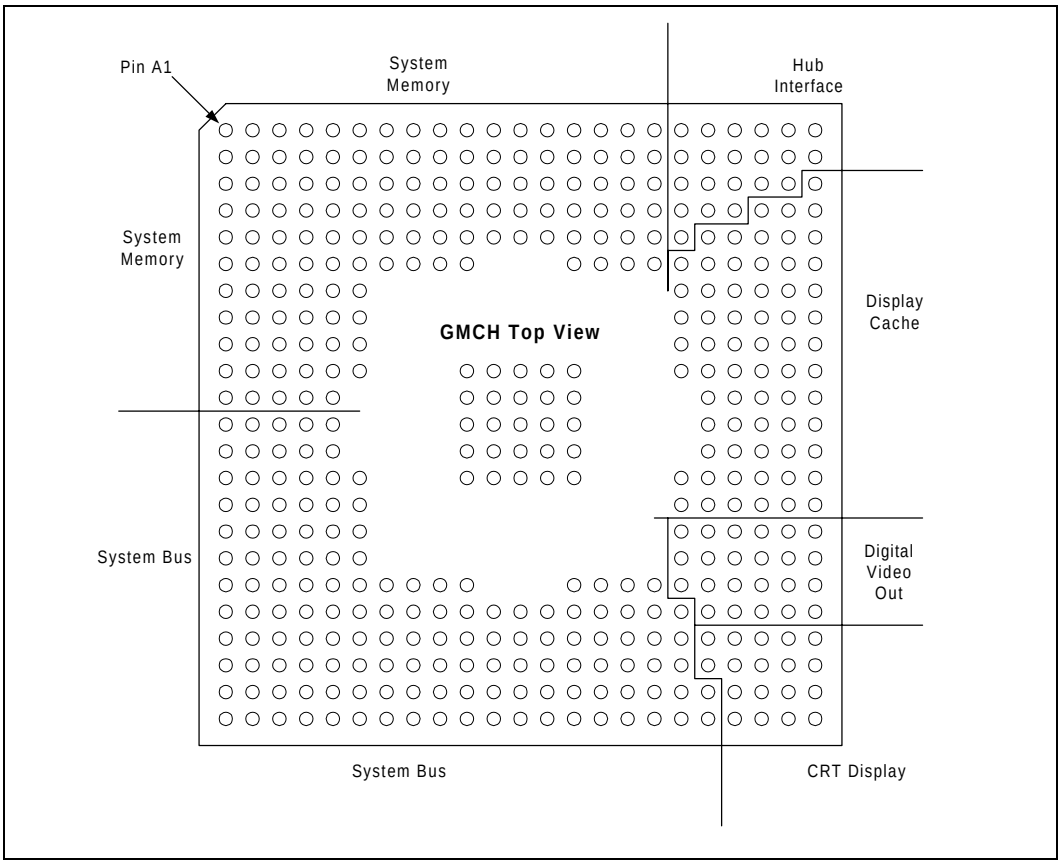
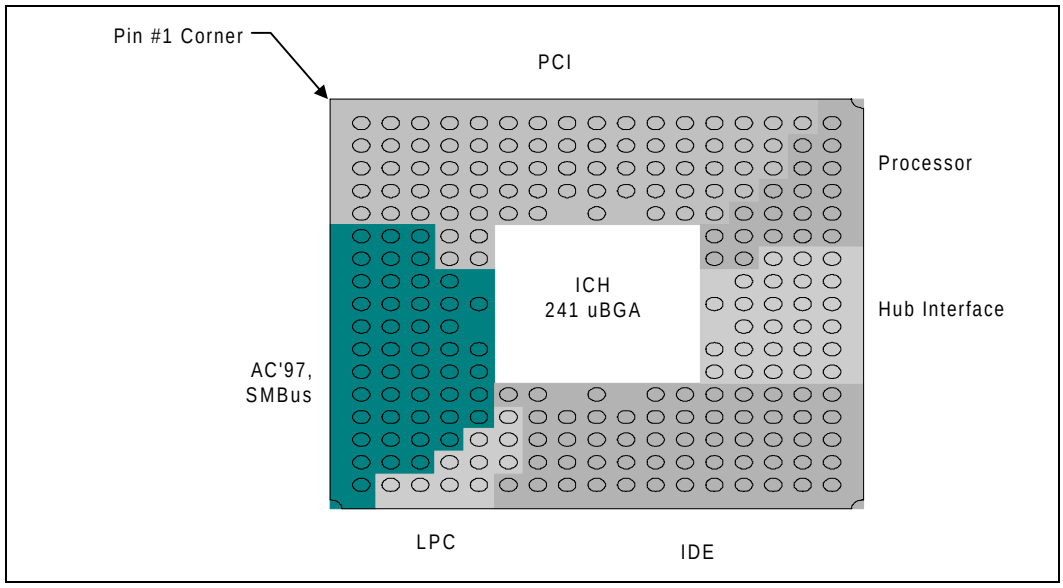


Figure 2-3. ICH 241-uBGA Quadrant Layout (topview)

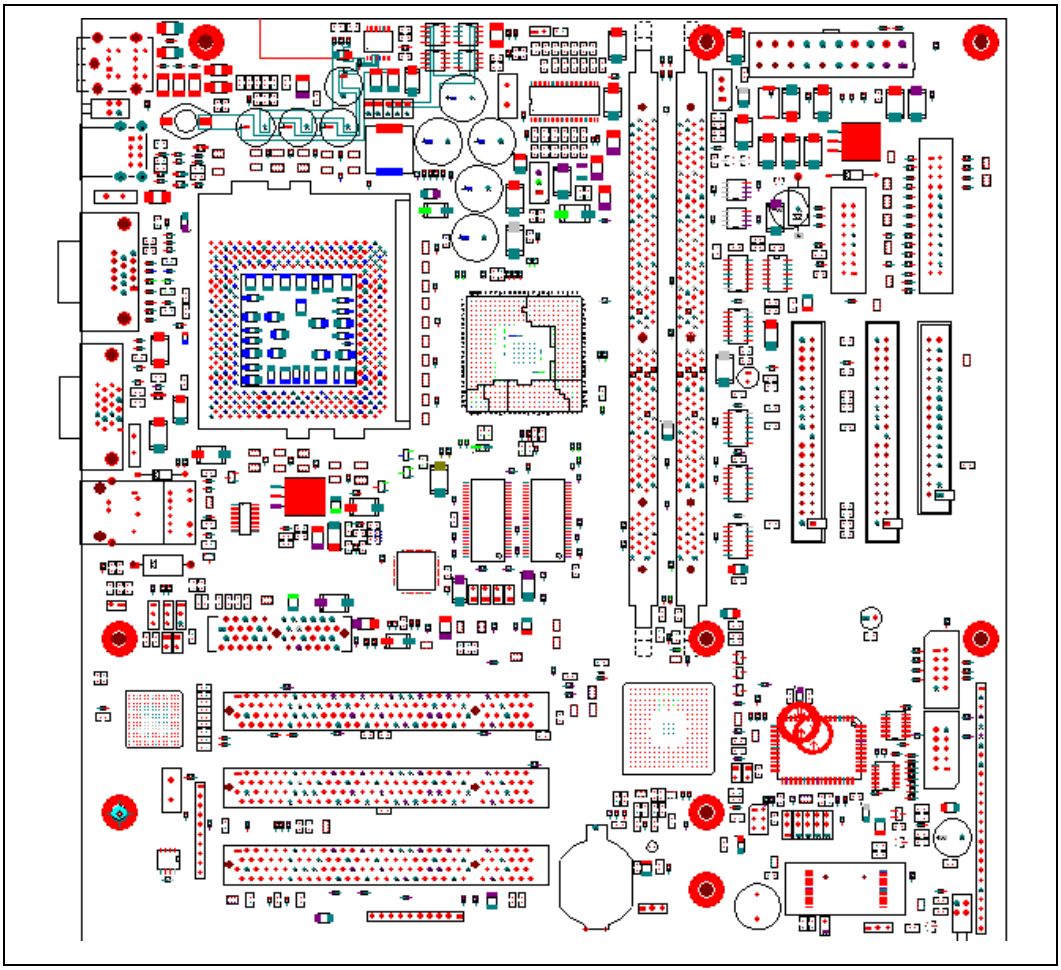


2.4 Intel® 810 Chipset Component Placement

The assumptions for component placement are:

- uATX Form Factor
- 4-Layer Motherboard
- Single Sided Assembly

Figure 2-4. uATX Placement Example



2.5 System Bus Routing

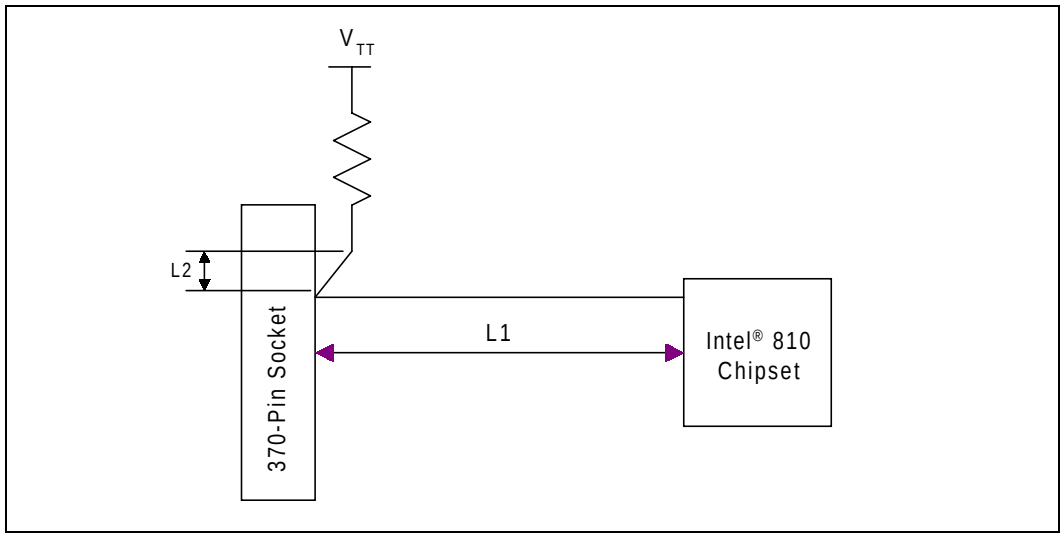
This section describes the design for the AGTL+ system bus for the Intel® Celeron™ processor and the Intel® 810 chipset. For more information on the AGTL+ bus, see Section 1.1.2, "References" on page 1-3.

2.5.1 Single Ended Termination (SET) Network Topology and Conditions

Termination resistors at only the PPGA can reduce system cost, at the expense of increased ringing and reduced solution space. However, the topology has some limitations which are discussed below.

In the SET topology, the termination should be placed close to the processor either on the motherboard or on the processor substrate. There is no termination present at the chipset end of the network. Due to the lack of termination, SET will exhibit much more ringback than the dual terminated topology. Extra care will be required in SET simulations to make sure that the ringback specs are met under the worst case signal quality conditions.

Figure 2-5. Topology for Single Processor Designs with Single End Termination (SET)



2.5.2 SET Trace Length Requirements

The required trace lengths for operation at 66/100 MHz with the SET topology are based on the Intel® Celeron™ processor PPGA timing analysis results, and are listed below. These trace lengths also meet the system bus timing requirements.

Table 2-1. SET Baseboard Trace Length Requirements

Trace	Minimum Length	Maximum Length
L1	1.9”	5.0”
L2	0.5”	2.0”

This section explains the recommended topology and design guidelines found for the AGTL+ bus between the Intel® Celeron™ processor and the Intel® 810 chipset. The maximum and minimum trace lengths were determined from sweep simulation results compared with the system timing and signal quality performance requirements of the chips.

The recommended topology for the AGTL+ bus is a single-ended termination topology. There is a resistor near the processor acting as the pull-up for the bus. In this case, it is recommended that the MB trace length be L1.

The actual AGTL+ bus trace width is a standard 5 mil, with minimum edge-to-edge trace spacing set at 12 mils. This helps minimize possible crosstalk effects. Also, the V_{TT} voltage should be 1.5V ±3% for static condition, but the worst case tolerance is ±9%.

2.5.3 Motherboard Layout Rules

AGTL+ Signals

- AGTL+ signals should be routed with lengths between L1 of trace from the processor pin to the chipset.
- The AGTL+ signals trace length between the processor pin and the resistor pack should be within L2.
- Traces are to be routed with a minimum of 12 mil edge-edge spacing, and the ratio of this spacing to the dielectric thickness of the layer should be at least 2.
- The trace width is recommended to be 5 mils and not greater than 6 mils.
- The minimum spacing can be decreased to 5 mils for escaping the PPGA and the BGA areas, for a length of less than 0.25”. Any coupling that might occur in the layout where the spacing is reduced due to board real estate problems should be limited to a length of less than 0.25”.
- It is strongly recommended that AGTL+ signals should be routed on the signal layer next to the ground layer (referenced to ground).

Non-AGTL+ Signals

Route these signals on any layer or any combination of layers. These signals are asynchronous, so there are no layout guidelines to be specified for these signals.

Table 2-2. Routing Guidelines for Non-AGTL+ Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length	Notes
FERR#	5 mils	10 mils	1” to 6”	
IERR#	5 mils	10 mils	1” to 6”	
PRDY#	5 mils	10 mils	1” to 6”	
TDO	5 mils	10 mils	1” to 6”	
THERMTRIP#	5 mils	10 mils	1” to 6”	
LINT[0]	5 mils	10 mils	1” to 6”	
LINT[1]	5 mils	10 mils	1” to 6”	
PWRGOOD	5 mils	10 mils	1” to 6”	
TDI	5 mils	10 mils	1” to 6”	
TMS	5 mils	10 mils	1” to 6”	
TRST#	5 mils	10 mils	1” to 6”	
SLP#	5 mils	10 mils	1” to 6”	
PICD[0]	5 mils	10 mils	1” to 6”	
PICD[1]	5 mils	10 mils	1” to 6”	
SMI	5 mils	10 mils	1” to 6”	
PICCLK	5 mils	10 mils	1” to 6”	
NMI	5 mils	10 mils	1” to 6”	
PREQ#	5 mils	10 mils	1” to 6”	
BSEL	5 mils	10 mils	1” to 6”	
THRMDP	5 mils	20 mils	No restrictions	Note 1
THRMDN	5 mils	20 mils	No restrictions	Note 1
GTLREF[0:7]	25 mils minimum	15 mils	No restrictions	Note 2

NOTES:

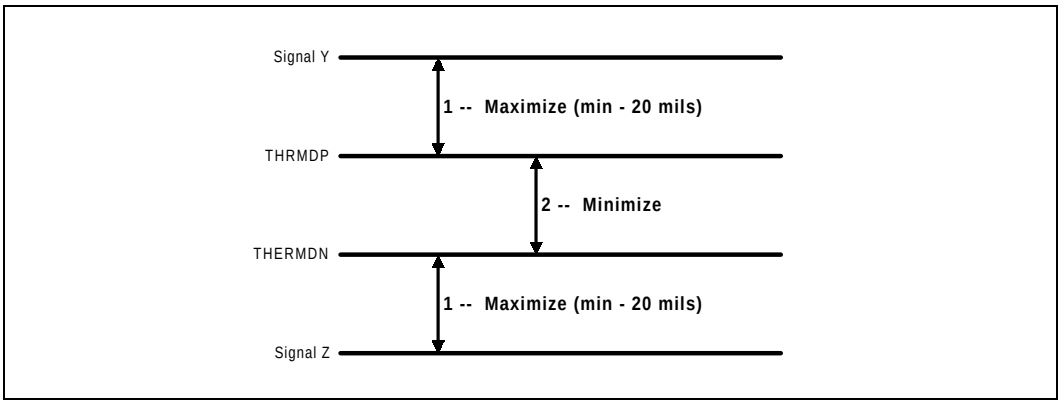
1. These traces (THRMDP and THRMDN) route the Intel® Celeron™ processor’s thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance.Refer to Figure 2-6.

Rule	
Length Equalization	route these traces parallel ±0.5”
Layer	route both on the same layer

2. GTLREF: This is the reference voltage for the AGTL+ system bus.

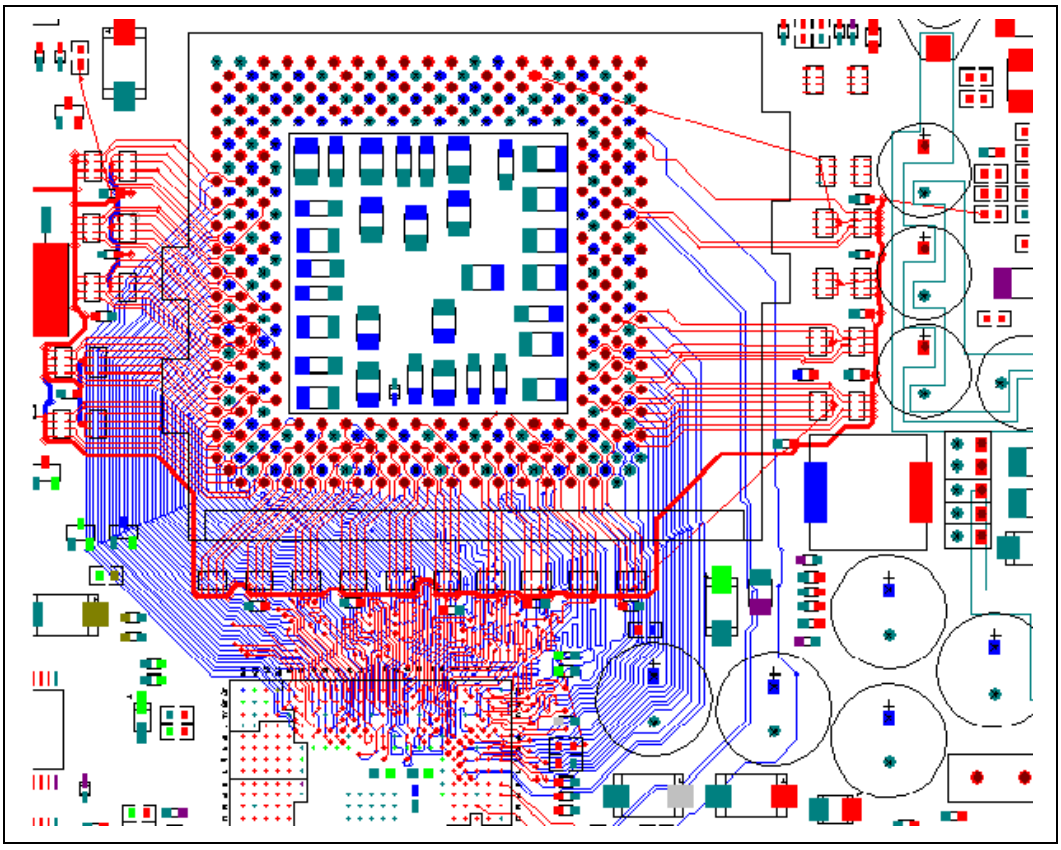
Trace Width	25mils minimum
Trace spacing	N/A
Spacing to other traces	15 mils
Topology	Loop or Plane

Figure 2-6. Routing for THRMDP and THRMDN



2.5.4 System Bus to GMCH Routing Example

Figure 2-7. System Bus to GMCH Routing Example



2.5.5 Minimizing Crosstalk

The following general rules will minimize the impact of crosstalk in the high speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 12 mils between trace edges wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between the sections when the spacing restrictions relaxes.
- Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL+ is a low signal swing technology, it is important to isolate AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 5V PCI.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
- Route AGTL+ address, data and control signals in separate groups to minimize crosstalk between groups. Keep at least 25 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the cross sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the tradeoff for this smaller cross sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.
- For the clock trace, provide a guard ground or spacing around of at least about 25 mils to the edge of the adjacent trace.

2.6 System Memory Layout Guidelines

2.6.1 System Memory Solution Space

Figure 2-8. System Memory Topologies

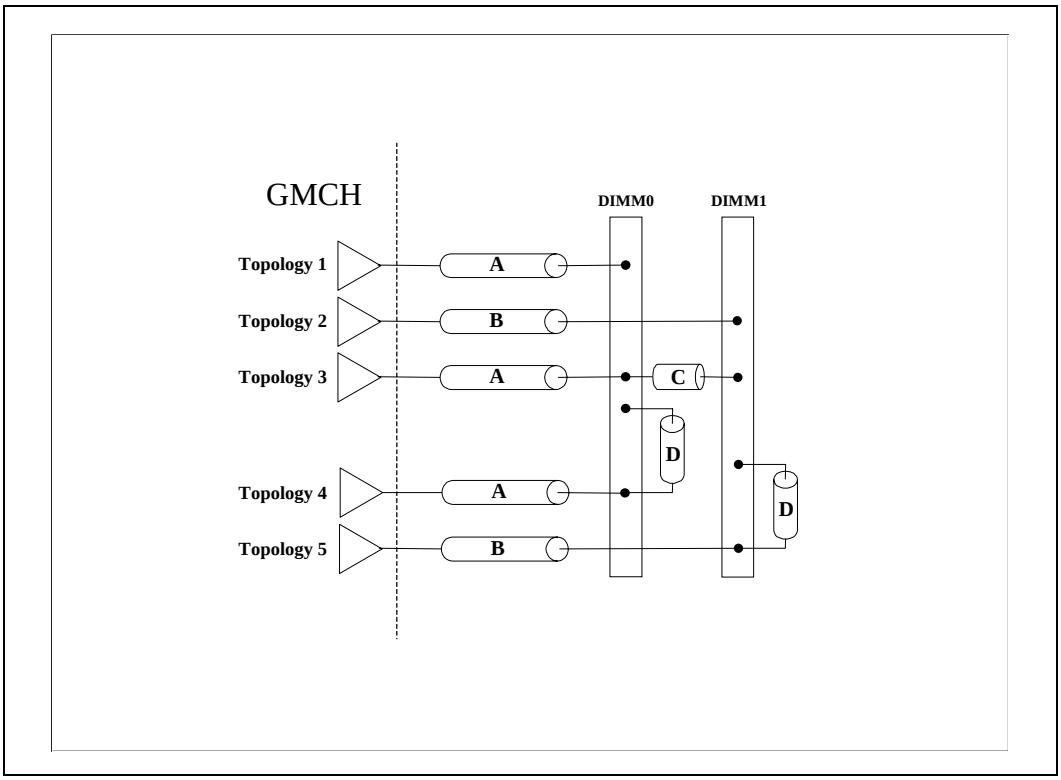


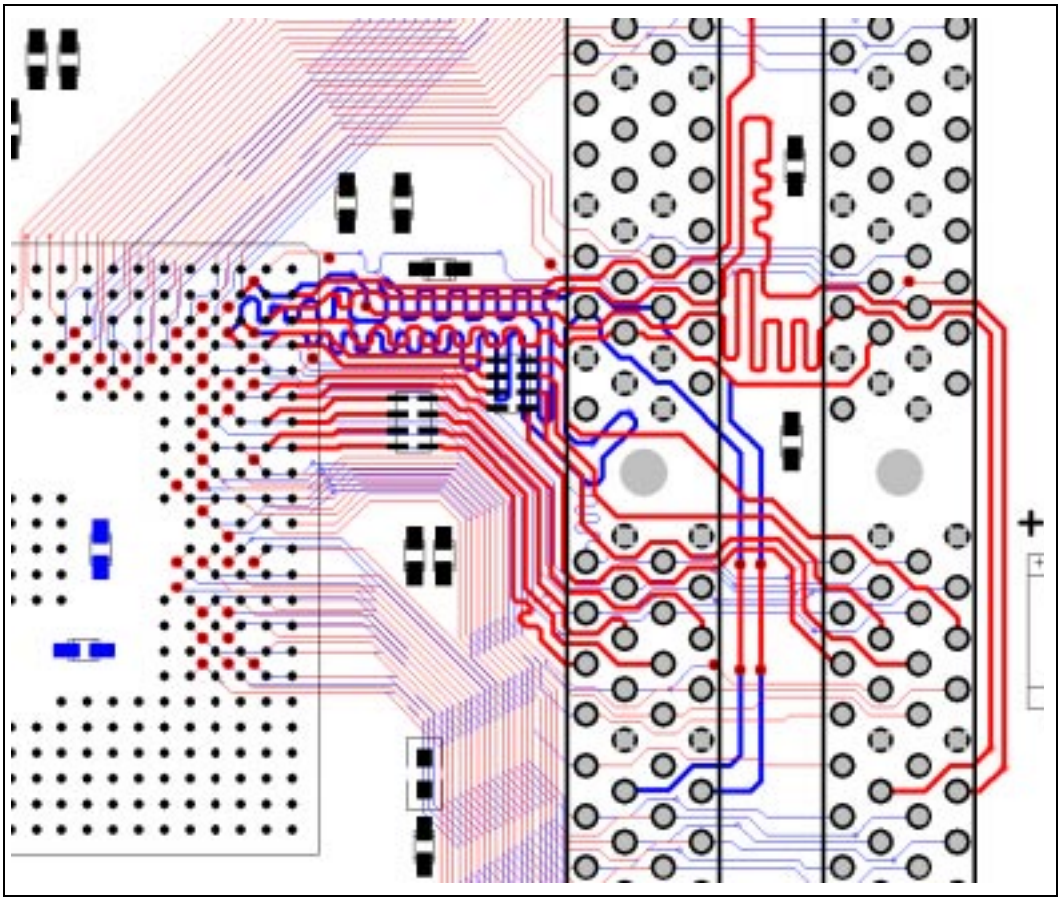
Table 2-3. System Memory Routing

Signal		Top.	Trace (mils)		Trace Lengths (inches)													
					A	B		C		D		E		F		G	
			Width	Space	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCS[3:2]#	Opt.1	5	10	8								3	5			1.5	2
	Opt.2	5	10	8								2.2	5			1.5	1.8
	Opt.3	5	10	8								1.6	5			1.15	1.5
SCS[1:0]#	Opt.1	4	10	8						3	5					1.5	2
	Opt.2	4	10	8						2.2	5					1.5	1.8
	Opt.3	4	10	8						1.6	5					1.15	1.5
SMAA[7:4]		1	10	8	0.5	0.5	2										
SMAB[7:4]#		2	10	8	0.5			0.5	2								
SCKE[1:0]		3	10	8						1	2.5			0.4	1		
SMD[63:0], SDQM[7:0]		3	5	7						1	3			0.4	1		
SCAS#, SRAS#, SWE#		3	5	7						1	3.5			0.4	1		
SBS[1:0], SMAA[11:8, 3:0]		3	5	7						1	2.5			0.4	1		

NOTE: It is recommended to add 10 ohm series resistors to the MAA[7:4] and the MAB[7:4] lines as close as possible to GMCH for signal integrity.

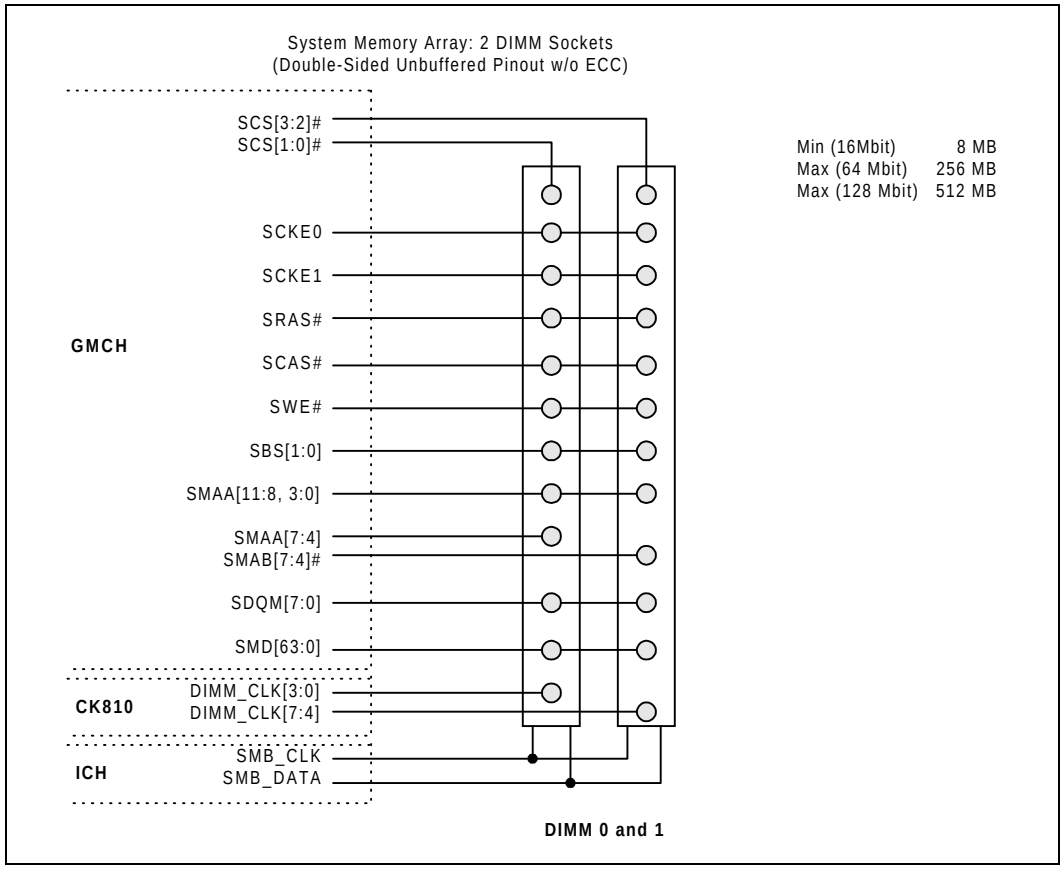
2.6.2 System Memory Routing Example

Figure 2-9. System Memory Routing Example



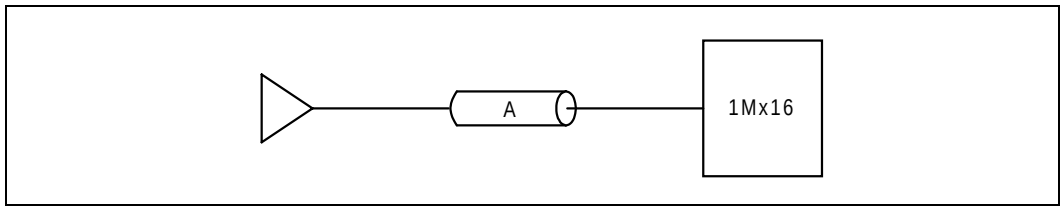
2.6.3 System Memory Connectivity

Figure 2-10. System Memory Connectivity



2.7 Display Cache Interface

Figure 2-11. Display Cache (Topology 1)



2.7.1 Display Cache Solution Space

Table 2-4. Display Cache Routing (Topology 1)

Signal	Topology	Trace (mils)		A (inches)	
		Width	Spacing	Min	Max
LMD[31:0], LDQM[3:0]	1	5	7	1	5

NOTE: Trace Length (inches)

Figure 2-12. Display Cache (Topology 2)

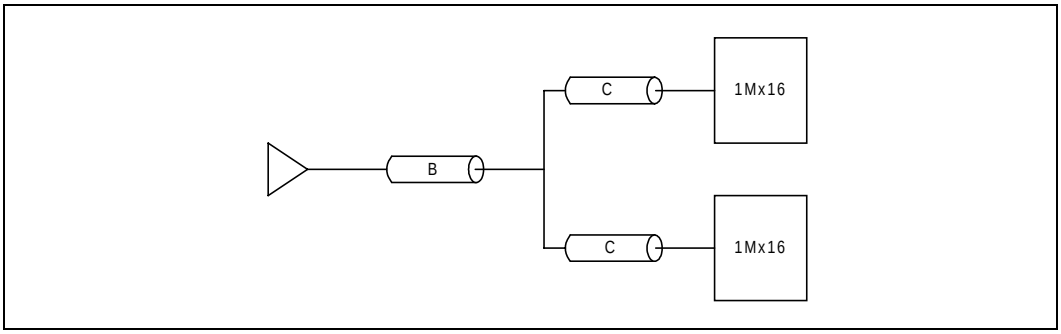


Table 2-5. Display Cache Routing (Topology 2)

Signal	Topology	Trace (units=mils)		B (inches)		C (inches)	
		Width	Spacing	Min	Max	Min	Max
LMA[11:0], LWE#, LCS#, LRAS#, LCAS#	2	5	7	1	3.75	0.75	1.25

Figure 2-13. Display Cache (Topology 3)

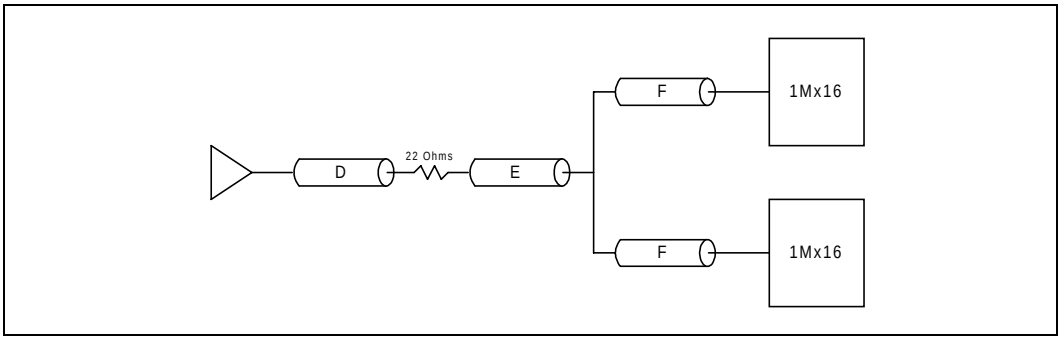


Table 2-6. Display Cache Routing (Topology 3)

Signal	Topology	Trace (units=mils)		D (inches)	E (inches)		F (inches)	
		Width	Spacing	Length	Min	Max	Min	Max
TCLK	3	5	7	0.5	1.5	2.5	0.75	1.25

Figure 2-14. Display Cache (Topology 4)

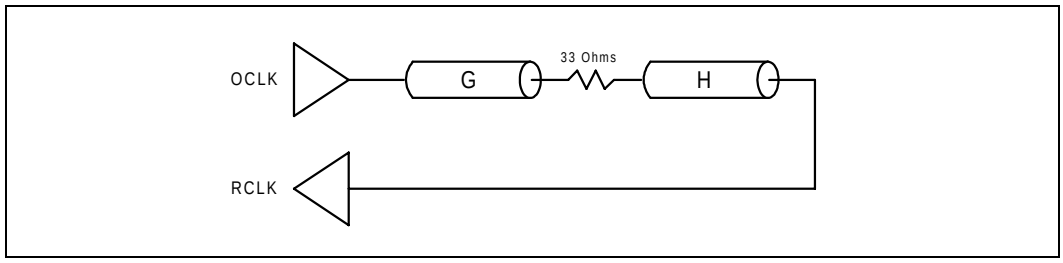


Table 2-7. Display Cache Routing (Topology 4)

Signal	Topology	Trace (units=mils)		G (inches)	H (inches)	
		Width	Spacing	Length	Min	Max
OCLK	4	5	6	0.5	3.25	3.75

2.8 Hub Interface

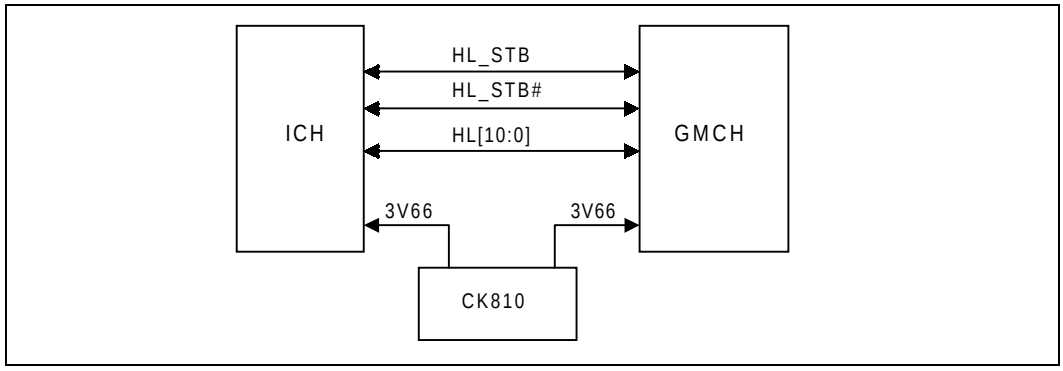
The GMCH ball assignment and ICH ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals are routed directly from the GMCH to the ICH on the top signal layer (refer to Figure 2-15). The hub interface has two signal groups:

- Data Signals: HL[10:0]
- Strobe Signals: HL_STB, HL_STB# (differential strobe pair).

There are no pull-ups or pull-downs required on the hub interface. HL11 on the 82801AA ICH (reserved on the 82801AB ICH0) can be brought out to a test point for NAND Tree testing is recommended.

Each signal should be routed such that the signal meets the guidelines documented for its signal group.

Figure 2-15. Hub Interface Signal Routing Example



2.8.1 Data Signals

Hub interface data signals should be routed with a trace width of *5* mils and a trace spacing of *20* mils. These signals can be routed with a trace width of *5* mils and a trace spacing of *15* mils for navigation around components or mounting holes. To break-out of the GMCH and the ICH, the hub interface data signals can be routed with a trace width of *5* mils and a trace spacing of *5* mils. The signals should be separated to a trace width of *5* mils and a trace spacing of 20 mils within 0.3" of the GMCH/ICH components.

The maximum trace length for the hub interface data signals is 7". These signals should each be matched within ±0.1" of the HL_STB and HL_STB# signals.

2.8.2 Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 7" and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes with ±0.1".

2.8.3 HREF Generation/Distribution

HREF is the hub interface reference voltage. It is 0.5 * 1.8V = 0.9V ±2%. It can be generated locally, or a single HREF divider can be used (as shown in Figure 2-16 and Figure 2-17). Each divider consists of a DC element and an AC element. The resistors in the DC element should be equal in value and rated at 1% tolerance. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The resistors in the AC element of the resistor divider should be no greater than 80 ohm and the capacitors should be 500 pF. Additionally, the reference voltage should be bypassed to ground at each component with a 0.1 uF capacitor.

Figure 2-16. Single Hub Interface Reference Divider Circuit

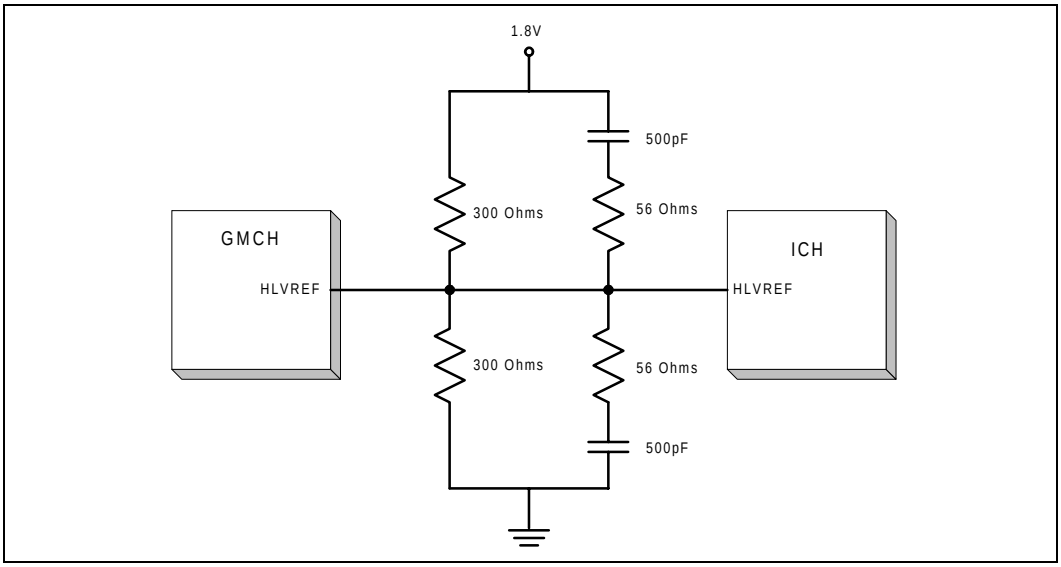
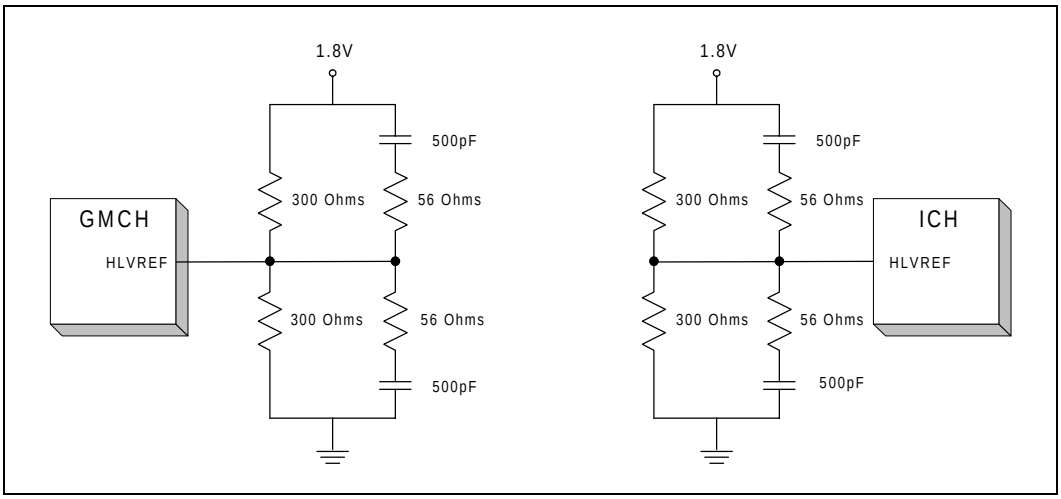


Figure 2-17. Locally Generated Hub Interface Reference Dividers



2.8.4 Compensation

There are two options for the ICH hub interface compensation (HLCOMP). HLCOMP is used by the ICH to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet for details on compensation. It can be used as either Impedance Compensation (ZCOMP) or Resistive Compensation (RCOMP). The guidelines are below:

- **RCOMP:** Tie the HLCOMP pin to a 40 ohm 1% or 2% pull-up resistor (to 1.8V) via a 10 mil wide, 0.5” trace (targeted for a nominal trace impedance of 40 ohm).
- **ZCOMP:** The HLCOMP pin should be tied to a 10 mil trace that is AT LEAST 18” long. This trace should be unterminated and care should be taken when routing the signal to avoid crosstalk (15-20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

The GMCH also has a hub interface compensation pin. This signal (HLCOMP) can be routed using either the RCOMP method or ZCOMP method described for the ICH.

2.9 Ultra ATA/33 and Ultra ATA/66

2.9.1 IDE Routing Guidelines

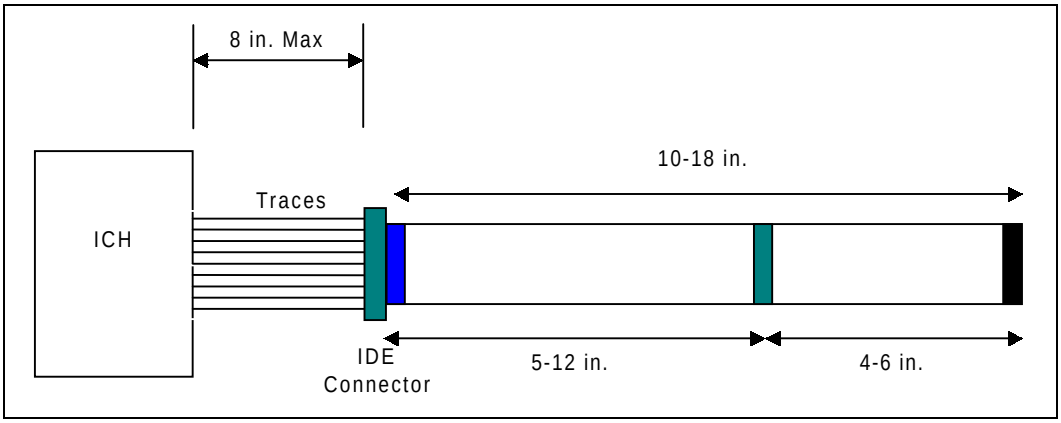
This section contains guidelines for connecting and routing the ICH IDE interface. The ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH0 and the ICH has integrated the series terminating resistors that have been typically required on the IDE data and control signals running to the two ATA connectors.

The IDE interface can be routed with 5 mil traces on 5 mil spaces and should be less than 8 inches long (from ICH to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 1” shorter than the longest IDE signal (on the channel).

Cabling

- **Length of Cable:** Each IDE cable should be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **UltraATA/66:** Ultra ATA/66 requires the use of an 80 conductor cable (for 82801AA ICH only).
- **ICH Placement:** The ICH should be placed within 8” of the ATA connector.
- **PC99 Requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft* PC99. The CSEL signal needs to be pulled down at the host side by using a 470 ohm pull-down resistor for each ATA connector.

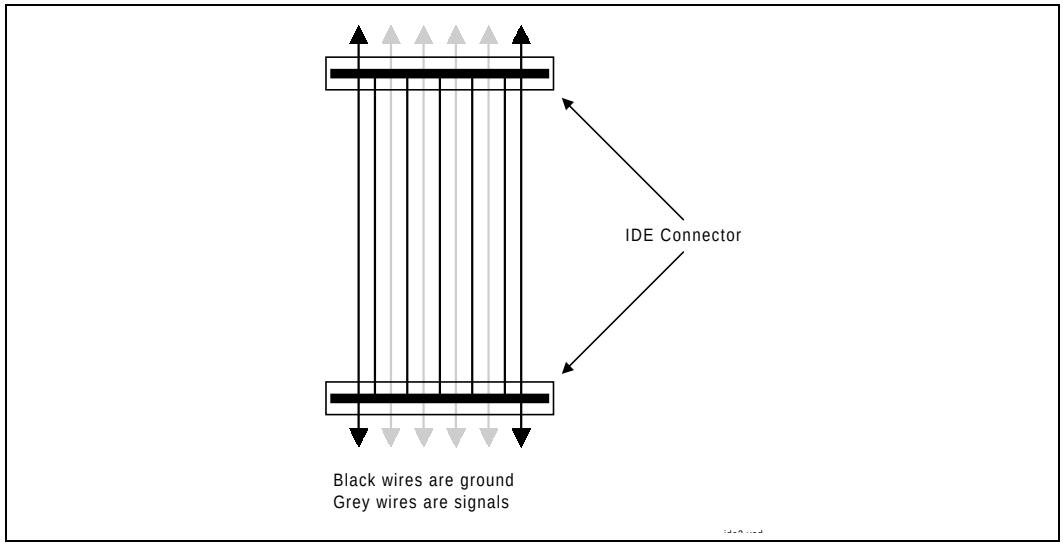
Figure 2-18. IDE Min/Max Routing and Cable Lengths



A new IDE cable is required for Ultra ATA/66 (82801AA ICH only). This cable is an 80 conductor cable; however, the 40 pin connectors do not change. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the

cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

Figure 2-19. Ultra ATA/66 Cable



Motherboard

- **ICH Placement:** The ICH should be placed within 8” of the ATA connector(s). There are no minimum length requirements for this spacing.
- **Capacitance:** The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
- **Series Termination:** There is no need for series termination resistors on the data and control signals since there is series termination integrated into these signal lines on the ICH.
  - A 1K ohm pullup to 5V is required on PIORDY and SIORDY.
  - A 470 ohm pulldown is required on pin 28 of each connector.
  - A 5.6K ohm pulldown is required on PDREQ and SDREQ.
  - Support Cable Select (CSEL) is a PC99 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
  - Primary IDE connector uses IRQ14 and the secondary IDE connector uses IRQ15.
  - IRQ14 and IRQ15 each need an 8.2K ohm pull-up resistor to VCC.
  - Due to the elimination of the ISA bus from the ICH, PCI_RST# should be connected to pin 1 of the IDE connectors as the IDE reset signal. Due to high loading, the PCI_RST# signal should be buffered.
  - There is no internal pull up or down on PDD7 or SDD7 of the ICH. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10K ohm pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up (as required by the ATA-4 specification).
  - If no IDE is implemented with the ICH, the input signals (xDREQ and xIORDY) can be grounded and the output signals left as no connects.

Figure 2-20. Resistor Schematic for Primary IDE Connectors

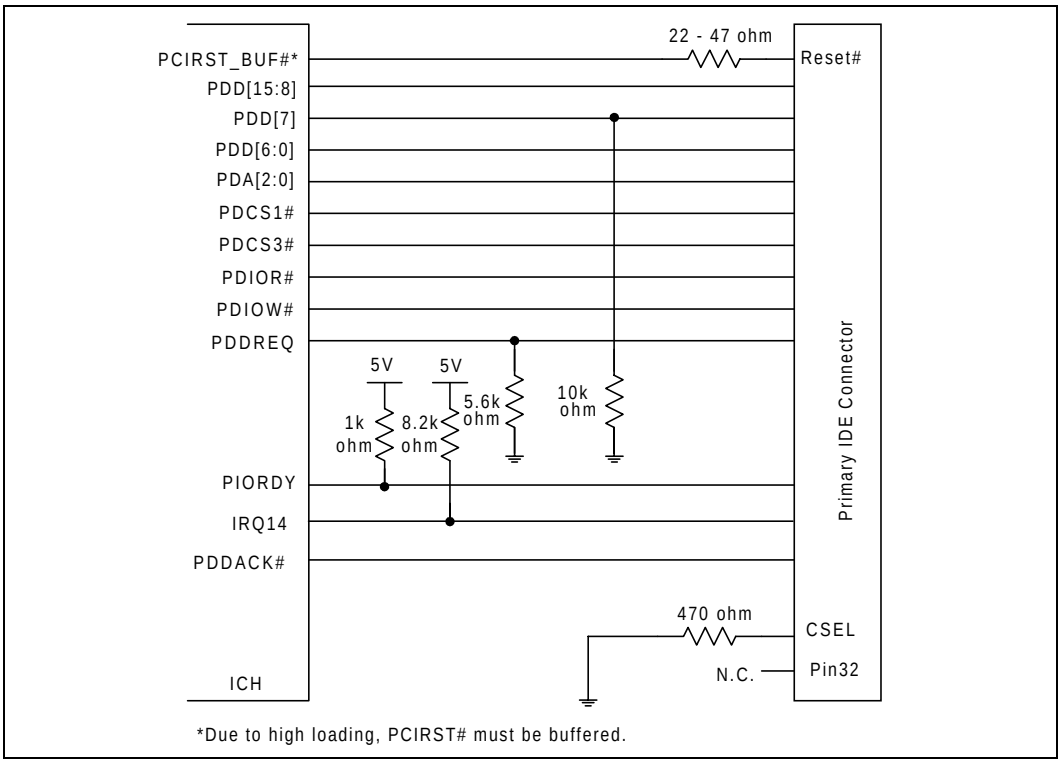
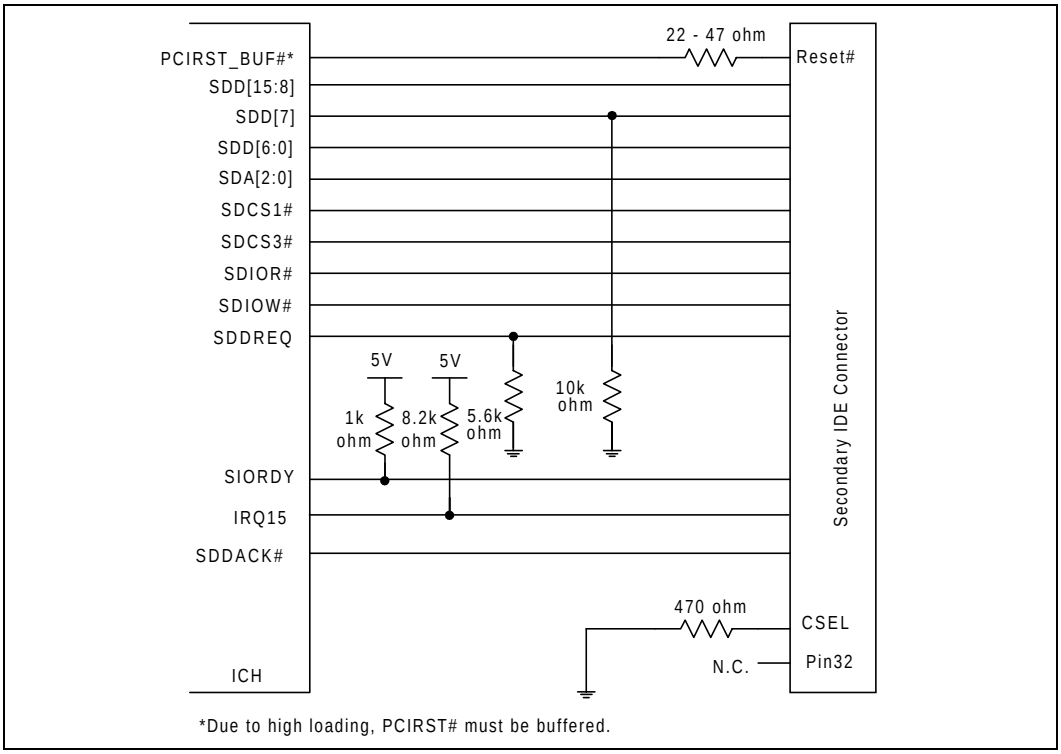


Figure 2-21. Resistor Schematic for Secondary IDE Connectors



2.9.2 Ultra ATA/66 Detection (82801AA ICH only)

The 82801AA ICH supports Ultra ATA/66 devices (82801AB ICH0 does not support Ultra ATA/66). The ATA/66 cable is an 80-conductor cable; however the 40 pin connectors used on motherboards for 40-conductor cables do not change as a result of this new cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together at the connectors on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

To determine if ATA/66 mode can be enabled, the Intel® 810 chipset using the ICH requires the system BIOS to attempt to determine the cable type used in the system. The BIOS does this in one of two ways:

- Host Side Detection
- Device Side Detection

If the BIOS detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the ICH and the IDE device. Otherwise, the BIOS can only enable modes that do not require an 80-conductor cable (example: Ultra ATA/33 Mode).

After determining the Ultra DMA mode to be used, the BIOS will configure the Intel® 810 chipset hardware and software to match the selected mode.

2.9.2.1 Ultra ATA/66 Motherboard Guidelines

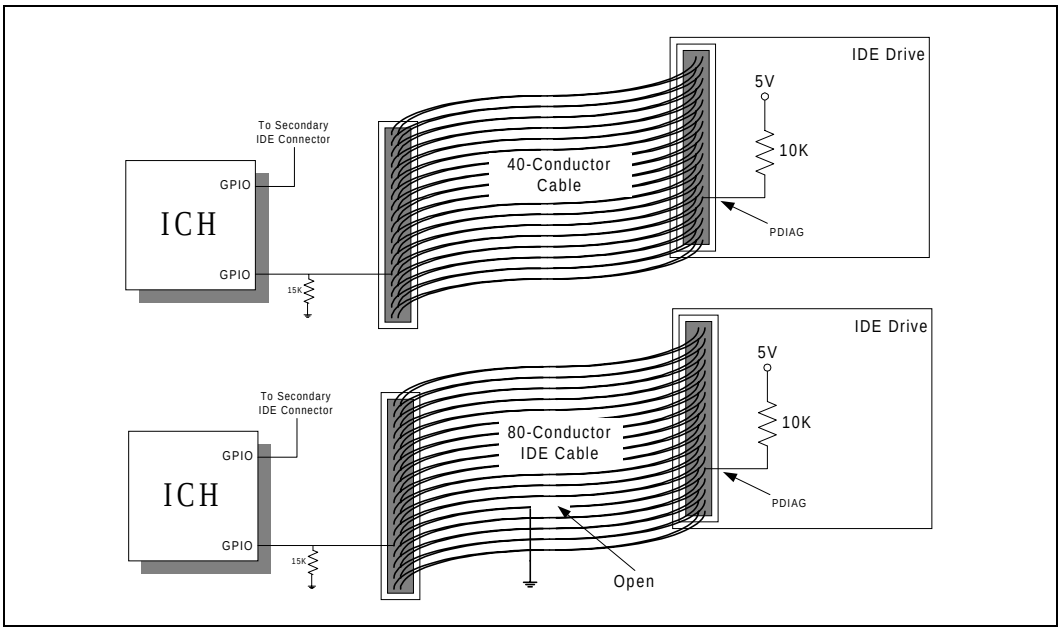
The Intel® 810 chipset (using the 82801AA ICH) can use two methods to detect the cable type. Each mode requires a different motherboard layout.

Host-Side Detection—BIOS Detects Cable Type Using GPIOs

Host side detection requires the use of two GPI pins (1 per IDE controller). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 2-22. All Ultra ATA/66 devices have a 10K ohm pull-up resistor to 5 volts. Most of the GPIO pins on the ICH and all GPIs on FWH are not 5 volt tolerant. This requires a resistor divider so that 5 volts will not be driven to the ICH or FWH pins. The proper value of the series resistor is 15K ohm (as shown on Figure 2-22). This creates a 10K ohm/15K ohm resistor divider and will produce approximately 3 volts for a logic high.

This mechanism allows the host, after diagnostics, to sample PDIAG#/CBLID#. If PDIAG#/CBLIB# is high then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG#/CBLID# is low then there is an 80-conductor cable in the system.

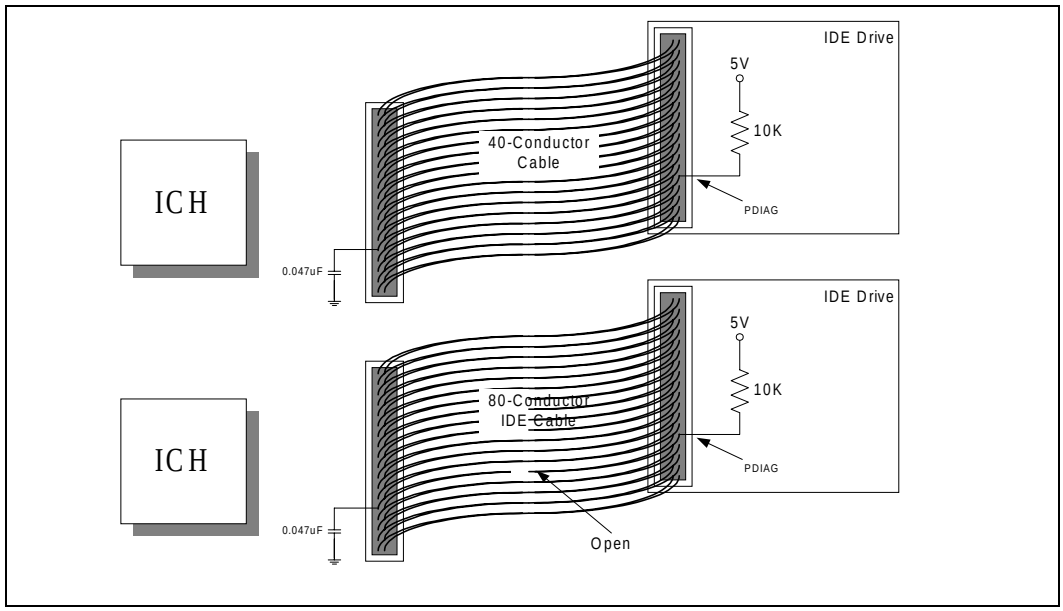
Figure 2-22. Host-Side IDE Cable Detection



Device-Side Detection—BIOS Queries IDE Drive for Cable Type

Device side detection requires only a 0.047 uF capacitor on the motherboard as shown in Figure 2-23. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10K ohm resistor). The drive will sample the PDIAG# signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through and therefore the capacitor has no effect. In a 40-conductor cable, PDIAG#/CBLID# is connected though to the drive. Therefore, the signal rises more slowly. The drive can detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

Figure 2-23. Host-Side IDE Cable Detection

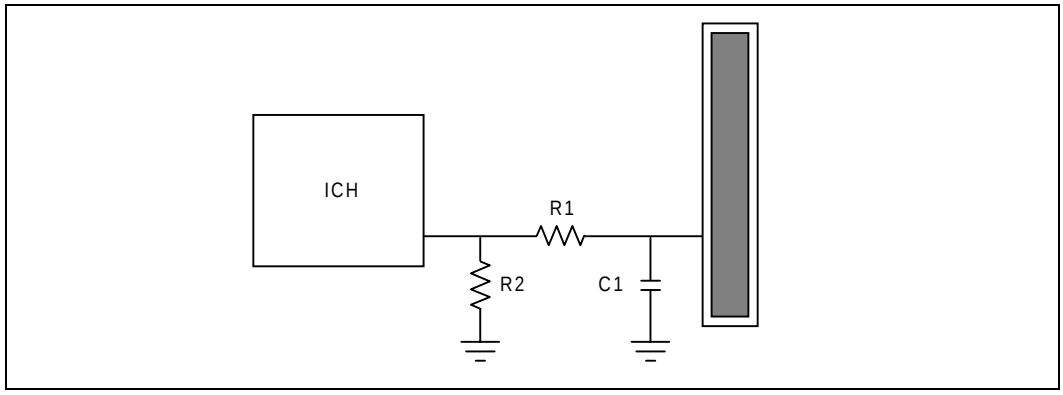


Layout for Both Host-Side and Drive-Side Cable Detection

It is possible to layout for both Host-Side and Drive-Side cable detection and decide the method to be used during assembly. Figure 2-24 shows the layout that allows for both host-side and drive-side detection.

- For Host-Side Detection
  - — R1 is a 0 ohm resistor
  - — R2 is a 15K ohm resistor
  - — C1 is not stuffed
- For Drive-Side Detection
  - — R1 is not stuffed
  - — R2 is not stuffed
  - — C1 is a 0.047 uF capacitor

Figure 2-24. Host-Side IDE Cable Detection



2.10 AC'97

The ICH implements an AC'97 2.1 compliant digital controller. Any codec attached to the ICH AC-link should be AC'97 2.1 compliant as well. Contact your preferred codec vendor for information on AC'97 2.1 compliant products. The AC'97 2.1 specification is on the Intel website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The ICH supports the following combinations of codecs:

Table 2-8. AC'97 Configuration Combinations

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in Table 2-8, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

2.10.1 Audio/Modem Riser Card (AMR)

Intel is developing a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM plug-in card options. The AMR specification is available on the Intel developer website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The AMR specification provides a mechanism for AC'97 codecs to be on a riser card. This is important for modem codecs as it helps ease international certification of the modem.

2.10.2 AC'97 Routing

To ensure maximum performance from the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device specific recommendations.

Following are the basic recommendations:

- Special consideration must be given for the ground return paths for the analog signals. If isolated ground planes are used, pin B2 on the AMR connector should be used as an isolated ground pin and should be connected to an isolated ground plane to reduce noise in the analog circuits. The AMR designer and motherboard designer should jointly address any EMI issues when implementing isolated grounds.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in the other.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05" wide.
- Keep digital signal traces, especially the clock, as far way from analog input and voltage reference pins as possible.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (¼" to ½ " wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05" wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground (i.e., there should not be any signals crossing the split/gap between the ground planes). Doing so will cause a ground loop. This will greatly increase EMI emissions and degrade analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path where voltage coefficient, temperature coefficient or noise are not a factor.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.
- Figure 2-25 and Figure 2-26 show the motherboard trace lengths for an ATX form factor with a codec on the motherboard and an AMR connector. Two routing methods are provided for the AC'97 interface: the tee topology and the daisy-chain topology. The AC'97 link signals can be routed using 5 mil traces with 5 mil space between the traces. NLX routing recommendations will be provided in a future revision of this document.

Figure 2-25. Tee Topology AC'97 Trace Length Requirements for ATX

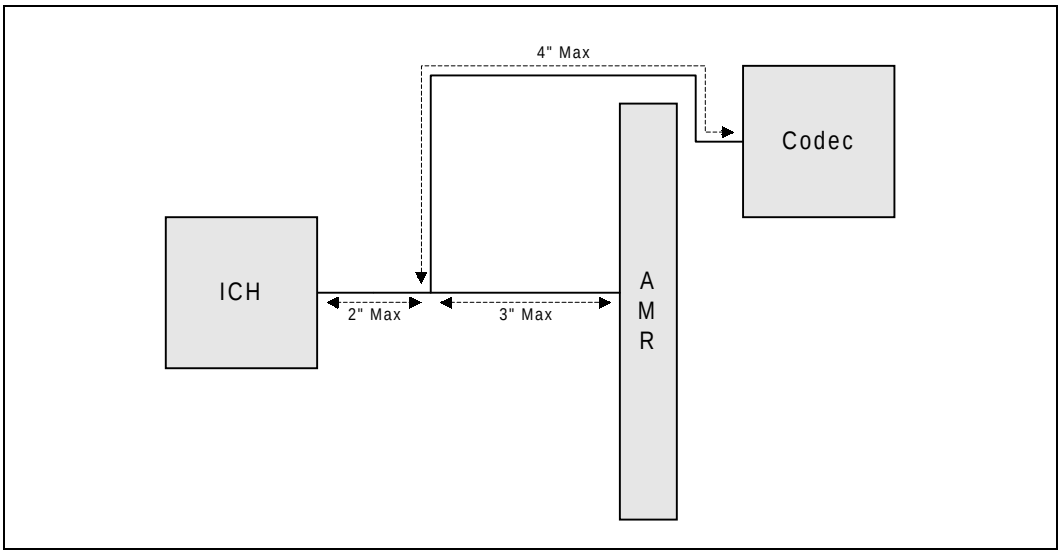
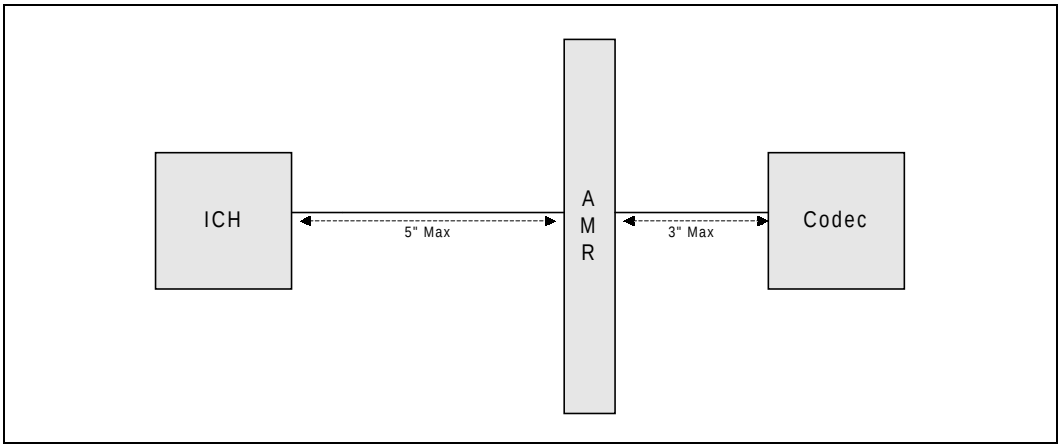


Figure 2-26. Daisy-Chain Topology AC'97 Trace Length Requirements for ATX



Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH), and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH supports wake on ring from S1-S4 via the AC’97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

If no codec is attached to the link, internal pulldowns will prevent the inputs from floating; therefore, external resistors are not required.

2.10.3 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. These recommendations do not represent the only implementation or a complete checklist, but provides recommendations based on the ICH platform.

- Codec Implementation
  - The motherboard can implement any valid combination of codecs on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on the AMR module; however, nothing precludes a modem codec on the motherboard.
  - Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH platform.
  - If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground.
  - The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
  - Components such as FET switches, buffers, or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing this will potentially interfere with timing margins and signal integrity.
  - If the motherboard requires that an AMR module override a primary codec down, a means of preventing contention on the AC-link must be provided for the onboard codec.
  - The ICH supports Wake On Ring from S1-S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pulldowns prevent the inputs from floating; therefore, external resistors are not required. The ICH does not wake from the S5 state via the AC'97 link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10K ohm) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH's internal pull-down resistors are enabled, and thus there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that has the potential of not being connected to a codec*. For example, if a dedicated audio codec is on the motherboard, and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. If, however, the SDATAIN signal has no codec connected, or is connected to an AMR slot, or is connected to an onboard codec that can be hardware disabled, then the signal should have an external pull-down resistor to ground.
  - In a lightly loaded system (e.g., single codec down), AC'97 signal integrity analysis should be evaluated to confirm that the signal quality on the link is acceptable by the codec used in the design. A series resistor at the driver and/or a capacitor at the codec can be implemented to compensate for any signal integrity issues. The values used are design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 5.

- AMR Slot Special Connections
  - AUDIO_MUTE#: No connect on the motherboard.
  - AUDIO_PWRDN: No connect on the motherboard. Codecs on the AMR card should implement a powerdown pin, per the AC'97 2.1 specification, to control the amplifier.
  - MONO_PHONE: Connect top onboard audio codec if supported.
  - MONO_OUT/PC_BEEP: Connect to SPKR output from the ICH, or MONO_OUT from onboard codec.
  - PRIMARY_DN#: See discussion above.
  - +5VDUAL/+5VSB: Connect to VCC5 core on the motherboard, unless adequate power supply is available. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
  - S/P-DIF_IN: Connect to ground on the motherboard.
  - AC_SDATAIN[3:2]: No connect on the motherboard. The ICH supports a maximum of two codecs, which should be attached to SDATAIN[1:0].
  - AC97_MSTRCLK: Connect to ground on the motherboard.
- The ICH provides internal weak pulldowns. Therefore, the motherboard does not need to provide discrete pulldown resistors.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

2.11 USB

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15K ohm pulldown resistors on both P+/P- data lines.
- 15 ohm series resistors should be placed as close as possible to the ICH (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pF caps must be placed as close to the ICH as possible, and on the ICH side of the series resistors on the USB data lines (P0±, P1±). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15K ohm ±5% pulldown resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±), and are for signal termination required by the USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0±, P1±- signals should be 45 ohms (to ground) for each USB signal P+ or P-. This may be achieved with 9 mil wide traces on the motherboard based on the stackup recommended in Figure 2-1. The impedance is 90 ohms between the differential signal pairs P+ and P- to match the 90 ohm USB twisted pair cable impedance. Note that the twisted pair characteristic impedance of 90 ohms is the series impedance of both wires, resulting in an individual wire presenting a 45 ohm impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as 'critical signals' (i.e., hand routing preferred). The P+/P- signal pair should be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. The P+/P- signal traces should also be the same length. This minimizes the effect of common mode current on EMI.

Figure 2-27 illustrates the recommended USB schematic.

Figure 2-27. USB Data Signals

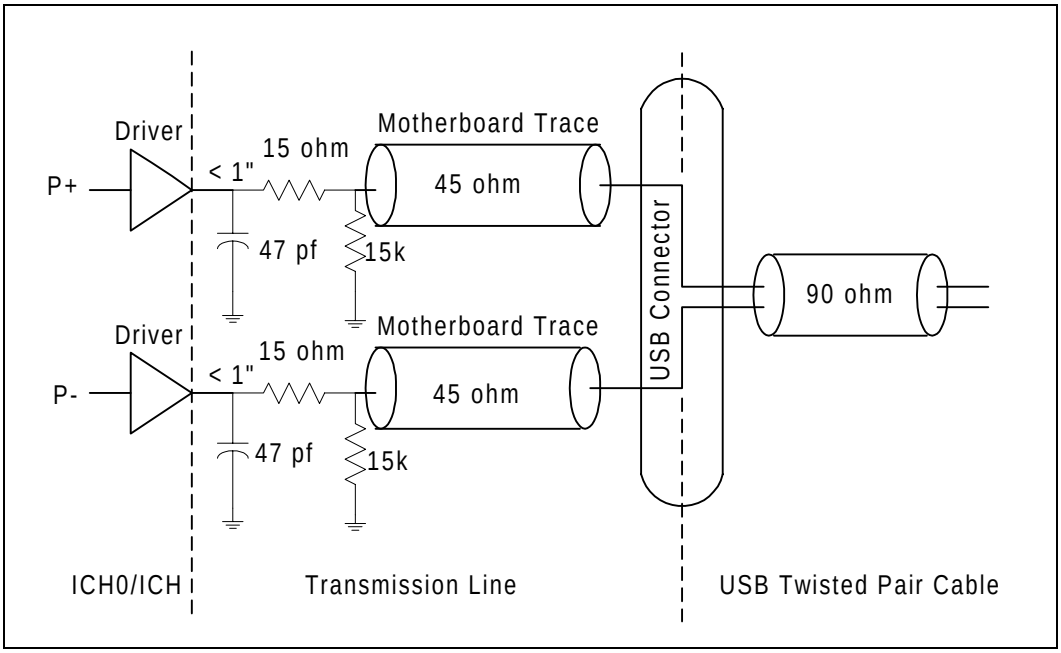


Table 2-9. Recommended USB Trace Characteristics

Impedance 'Z0' = 45.4 ohm
Line Delay = 160.2 ps
Capacitance = 3.5 pF
Inductance = 7.3 nH
Res @ 20° C = 53.9m ohm

2.12 IOAPIC (I/O Advanced Programmable Interrupt Controller)

Systems that do not use the ICH I/O APIC should follow these recommendations:

On the ICH:

- Tie PICCLK directly to ground
- Tie PICD0, PICD1 directly to ground

On the processor:

- PICCLK must be connected from the clock generator to the PICCLK pin on the processor
- Tie PICD0 to VCC_{CMOS} through a 150 ohm resistor
- Tie PICD1 to VCC_{CMOS} through a 150 ohm resistor

Note: If not using IOAPIC, turn off APIC clocks to ICH through I^2C.

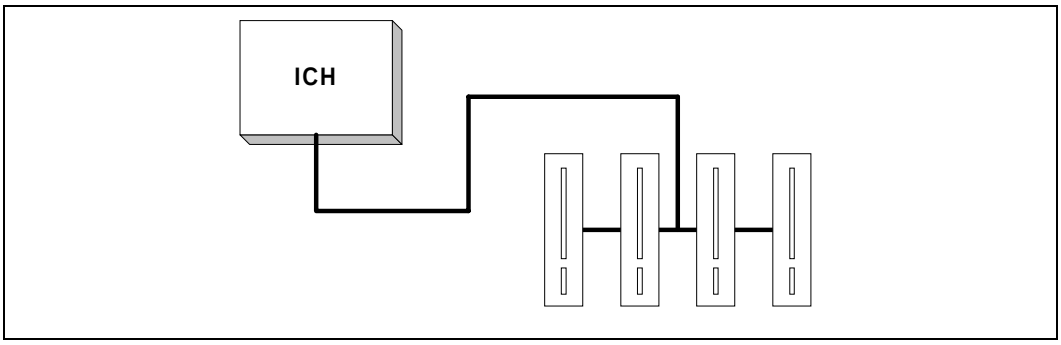
2.13 PCI

The ICH provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification Revision 2.2.*

The 82801AB ICH0 supports 4 PCI Bus masters (excluding ICH0), by providing 4 REQ#/GNT# pairs. The 82801AA ICH supports 6 PCI Bus masters (excluding ICH), by providing 6 REQ#/GNT# pairs. In addition, the 82801AA ICH supports 2 PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair. The 82801AB ICH0 does not multiplex any PCI REQ#/GNT# pairs.

For both the 82801AA ICH and 82801AB ICH0, based on simulations done by Intel, it is recommended that four is the maximum number of PCI slots that should be connected to either the 82801AA ICH or the 82801AB ICH0. This limit is due to timing and loading considerations established during simulations. If a system designer wants to have 5 PCI slots connected to the 82801AA ICH, then it is recommended that they do simulations to verify proper design.

Figure 2-28. PCI Bus Layout Example for 4 PCI Connectors



2.14 RTC

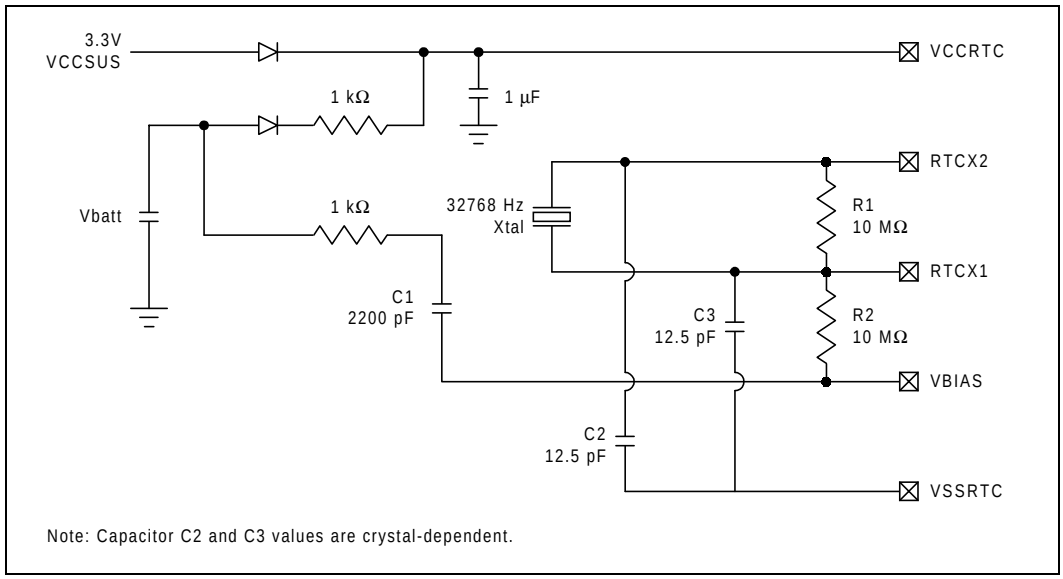
The ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. This internal RTC module provides two key functions: a) keeping date and time, b) storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH. **This circuit is not the same as the circuit used for the PIIX4.**

2.14.1 RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 pins. Figure 2-29 represents the external circuitry that comprises the oscillator of the ICH RTC.

Figure 2-29. External Circuitry for the ICH RTC



NOTES:
1. The exact capacitor value should be based on the crystal vendor's recommendations.
2. VccRTC: Power for RTC Well.
3. RTCX2: Crystal Input 2 – Connected to the 32.768 KHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.768 KHz crystal.
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
6. Vss: Ground.

2.14.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 should be set to 2200 pF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values (C2 and C3):

$$Cload = (C2*C3)/(C2+C3) + Cparasitic$$

C3 can be chosen such that C3 > C2; then, C2 can be trimmed to obtain the 32.768 KHz.

2.14.3 RTC Layout Considerations

- Keep the XTAL lead lengths as short as possible; around 1 inch is sufficient.
- Minimize the capacitance between RTCX1and RTCX2 in the routing.
- Put a ground plane under the XTAL components.
- Do not route any switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean; use a filter (e.g., an RC lowpass) or a ferrite inductor.
- Keep high speed switching signals (e.g., PCI signals) away from VCCRTC, RTCX1, RTCX2 and VBIAS.

2.14.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system.

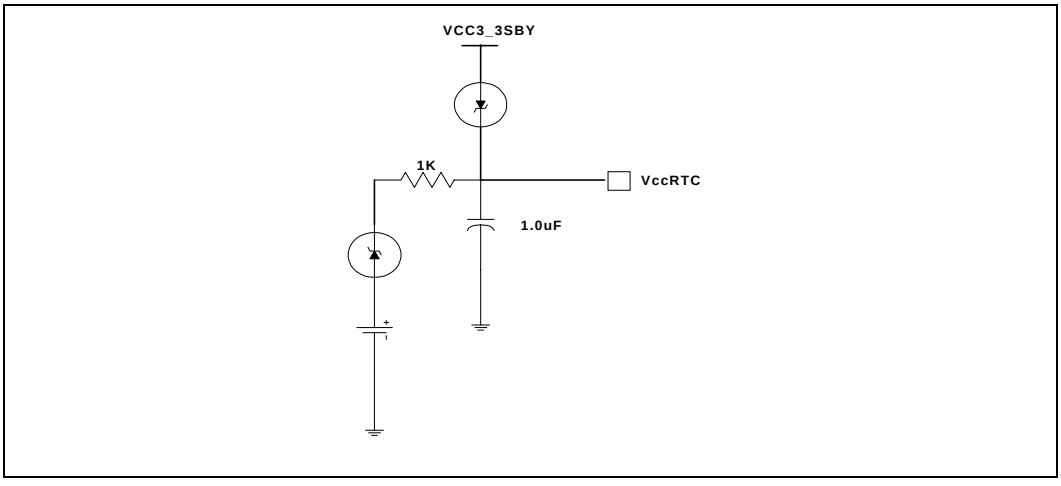
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mA per hour (assumed usable) and the average current required is 3 uA, the battery life will be at least:

170,000 uAhr / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse-biased when the system power is not available. Figure 2-30 is an example of a diode circuitry that can be used.

Figure 2-30. A Diode Circuit to Connect RTC External Battery

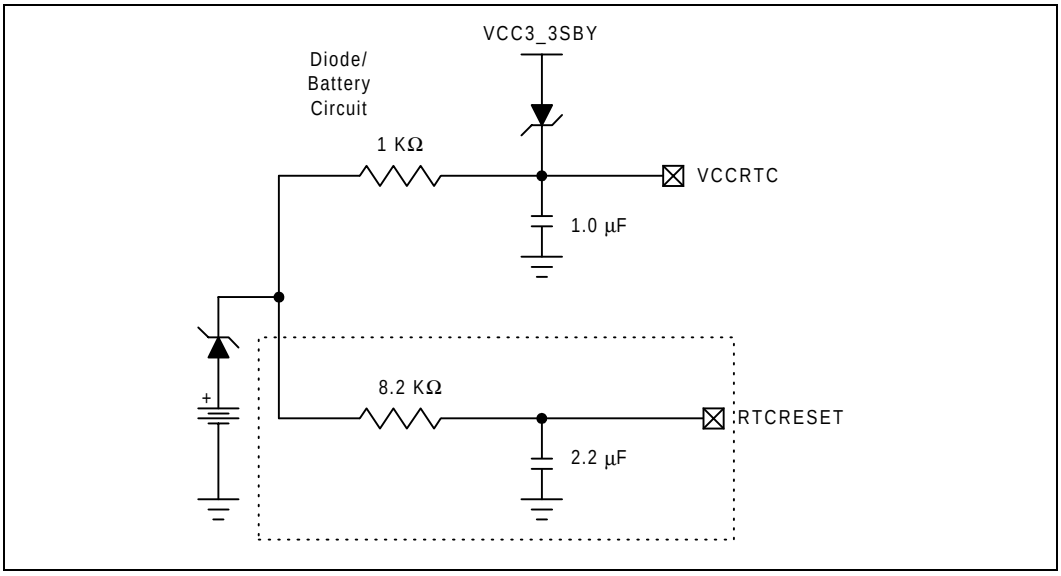


A standby power supply should be used to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

2.14.5 RTC External RTCRESET Circuit

The ICH RTC requires some additional external circuitry. The RTCRESET (RTC Well Test) signal is used to reset the RTC Well. The external capacitor (2.2 uF) and the external resistor (8.2K ohm) between RTCRESET and the RTC battery (Vbat) were selected to create a RC time delay, such that RTCRESET goes high some time after the battery voltage is valid. The RC time delay should be in the range of 10–20 ms. When RTCRESET is asserted bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result, when the system boots, BIOS knows that the RTC battery has been removed.

Figure 2-31. RTCRESET External Circuit for the ICH RTC



This RTCRESET circuit is combined with the diode circuit (Figure 2-30) which allows the RTC well to be powered by the battery when the system power is not available. Figure 2-31 is an example of this circuitry that is used, in conjunction with the external diode circuit.

2.14.6 VBIAS DC Voltage and Noise Measurements

- Steady state VBIAS will be a DC voltage of about 0.38V ±.06V.
- VBIAS will be “kicked” when the battery is inserted to about 0.7–1.0V; it will come back to its DC value within a few ms.
- Noise on VBIAS must be kept to a minimum (200mV or less).
- VBIAS is very sensitive and can not be directly probed; it can be probed through a 0.01 uF capacitor.
- Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely.
- To minimize noise of VBIAS it is necessary to implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet.

2.15 Processor PLL Filter Recommendation

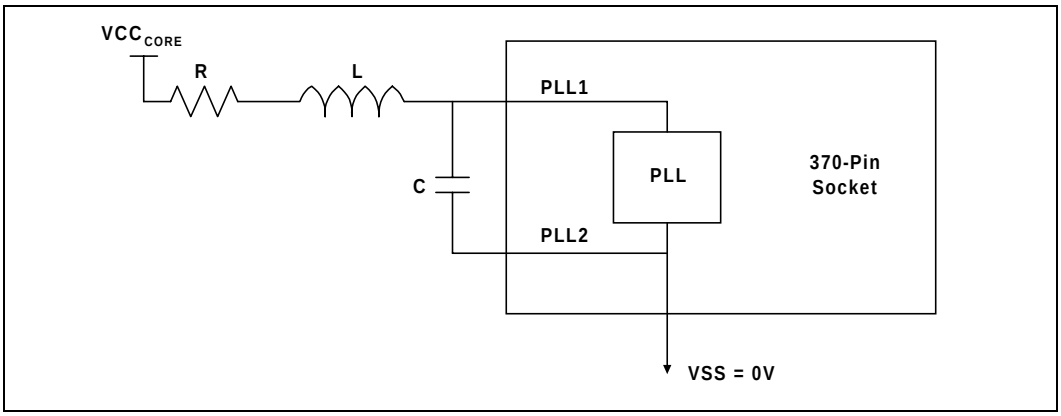
2.15.1 Processor PLL Filter Recommendation

All Intel® Celeron™ processors have internal PLL clock generators that are analog and require quiet power supplies to minimize jitter.

2.15.2 Topology

The general desired topology is shown in Figure 2-32. Not shown are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

Figure 2-32. Filter Topology



2.15.3 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. In general, the low-pass description forms an adequate description for the filter.

The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

< 0.2 dB gain in pass band

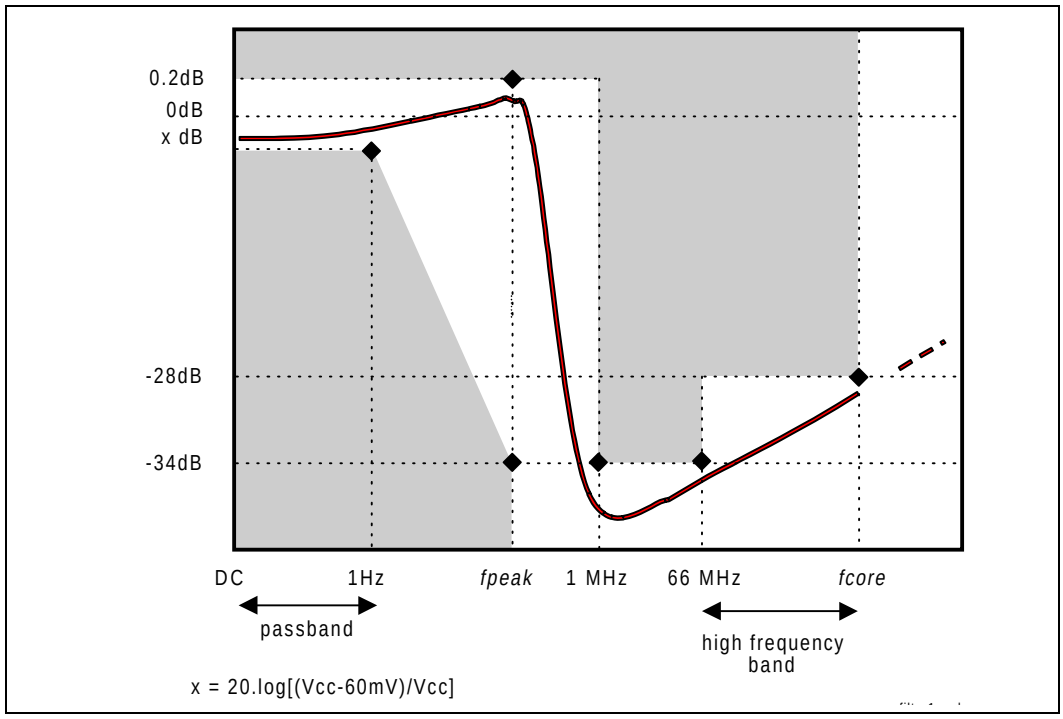
< 0.5 dB attenuation in pass band (see DC drop in next set of requirements)

> 34 dB attenuation from 1 MHz to 66 MHz

> 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 2-33.

Figure 2-33. Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak,* if it exists, it should be less than 0.05 MHz.

Other requirements:

- Filter should support DC current > 30 mA.
- Shielded type inductor to minimize magnetic pickup.
- DC voltage drop from VCC to PLL1 should be < 60mV, which in practice implies series R < 2 ohm; also means pass band (from DC to 1Hz) attenuation < 0.5dB for VCC = 1.1V, and < 0.35dB for VCC = 1.5V.

2.15.4 Recommendation for Intel Platforms

The following tables are examples of components that meet Intel's recommendations, when configured in the topology presented in Figure 2-32.

Table 2-10. Inductor

Part Number	Value	Tol	SRF	Rated I	DCR
TDK MLF2012A4R7KT	4.7 uH	10%	35 MHz	30 mA	0.56 ohm (1W max)
Murata LQG21N4R7K00T1	4.7 uH	10%	47 MHz	30 mA	0.7 ohm (±50%)
Murata LQG21C4R7N00	4.7 uH	30%	35 MHz	30 mA	0.3 ohm max

Table 2-11. Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 uF	20%	2.5 nH	0.225 ohm
AVX TPSD336M020S0200	33 uF	20%	TBD	0.2 ohm

Table 2-12. Resistor

Value	Tolerance	Power	Note
1 ohm	10%	1/16 W	Resistor may be implemented with trace resistance, in which discrete R is not needed

To satisfy damping requirements, total series resistance in the filter (from $V_{CC_{CORE}}$ to the top plate of the capacitor) must be at least 0.35 ohm. This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has a minimum DCR of 0.25 ohm, then a routing resistance of at least 0.10 ohm is required. Be careful not to exceed the maximum resistance rule (2 ohm). For example, if using discrete R1, the maximum DCR of the L should be less than 2.0 - 1.1 = 0.9 ohm, which precludes using some inductors.

Other routing requirements:

- C should be close to PLL1 and PLL2 pins, < 0.1 ohm per route. These routes do not count towards the minimum damping R requirement.
- PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- L should be close to C; any routing resistance should be inserted between $V_{CC_{CORE}}$ and L.
- Any discrete R should be inserted between $V_{CC_{CORE}}$ and L.

Figure 2-34. Using Discrete R

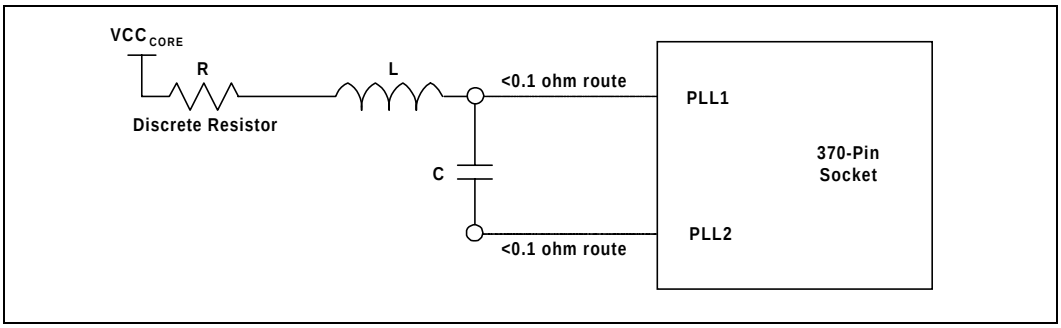
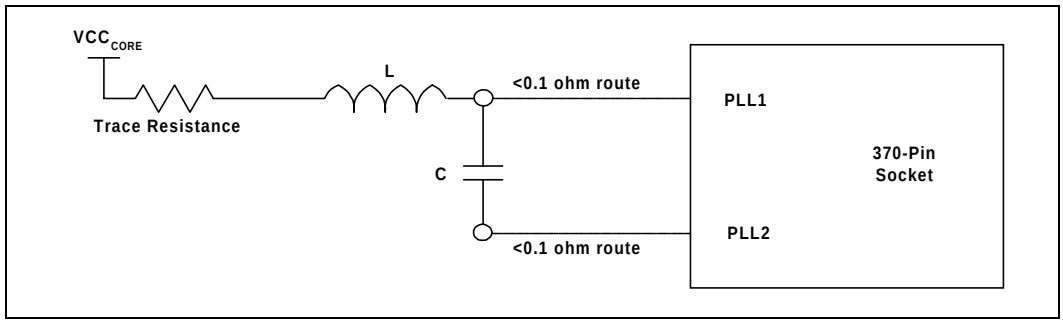


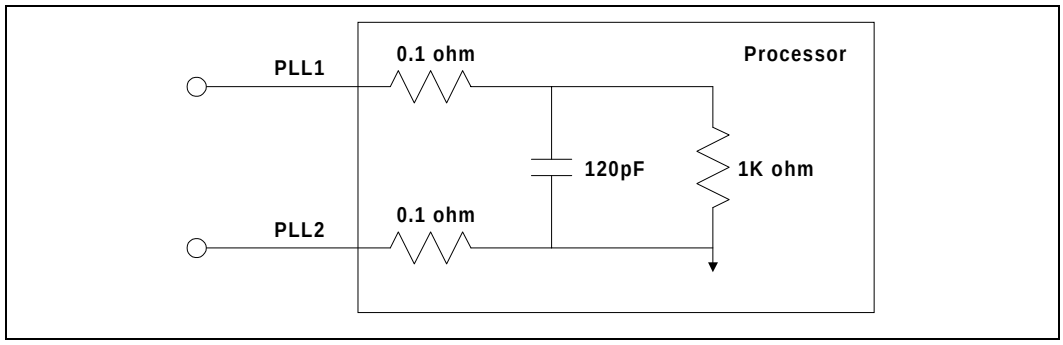
Figure 2-35. No Discrete R



2.15.5 Custom Solutions

As long as filter performance as specified in Figure 2-33 and other requirements outlined in Section 2.15.3, “Filter Specification” on page 2-34 are satisfied, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in Figure 2-36.

Figure 2-36. Core Reference Model



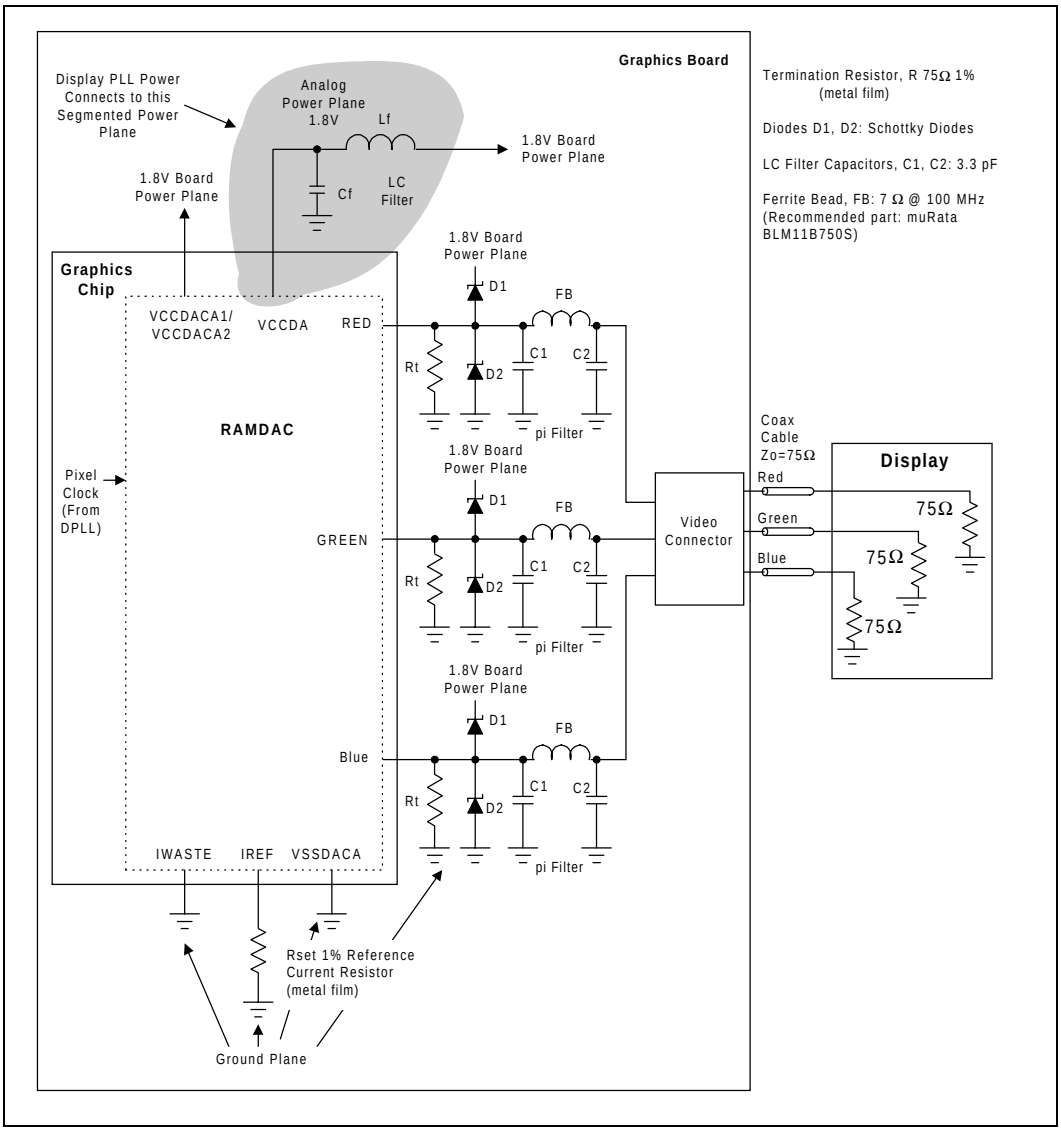
NOTES:
1. 0.1 ohm resistors represent package routing[1].
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1K ohm resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Please sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum VCC_{CORE} level.

1. For other modules (interposer, DMM, etc), adjust routing resistor if desired, but use minimum numbers.

2.16 RAMDAC/Display Interface

Figure 2-37 shows the interface of the RAMDAC analog current outputs with the display. Each DAC output is doubly-terminated with a 75 ohm resistance; one 75 ohm resistance from the DAC output to the board ground and the other termination resistance exists within the display. The equivalent dc resistance at the output of each DAC output is 37.5 ohm. The output current of each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also an LC pi-filter which is used to reduce high-frequency glitches and noise, and reduce EMI. To maximize the performance, the filter impedance, cable impedance and load impedance should be the same. The LC pi-filter consists of two 3.3 pF capacitors and a ferrite bead with a 75 ohm impedance at 100 MHz. The LC pi-filter is designed to filter glitches produced by the RAMDAC while maintaining adequate edge rates to support high-end display resolutions.

Figure 2-37. Schematic of RAMDAC Video Interface



NOTE: Diodes D_1, D_2 are clamping diodes and may not be necessary to populate.

In addition to the termination resistance and LC pi-filter, there are protection diodes connected to the RAMDAC outputs to help prevent latch-up. The protection diodes must be connected to the same power supply rails as the RAMDAC. An LC filter is recommended to connect the segmented analog 1.8V power plane of the RAMDAC to the 1.8V board power plane. The LC filter is recommended to be designed for a cut-off frequency of 100 KHz.

2.16.1 Reference Resistor (Rset) Calculation

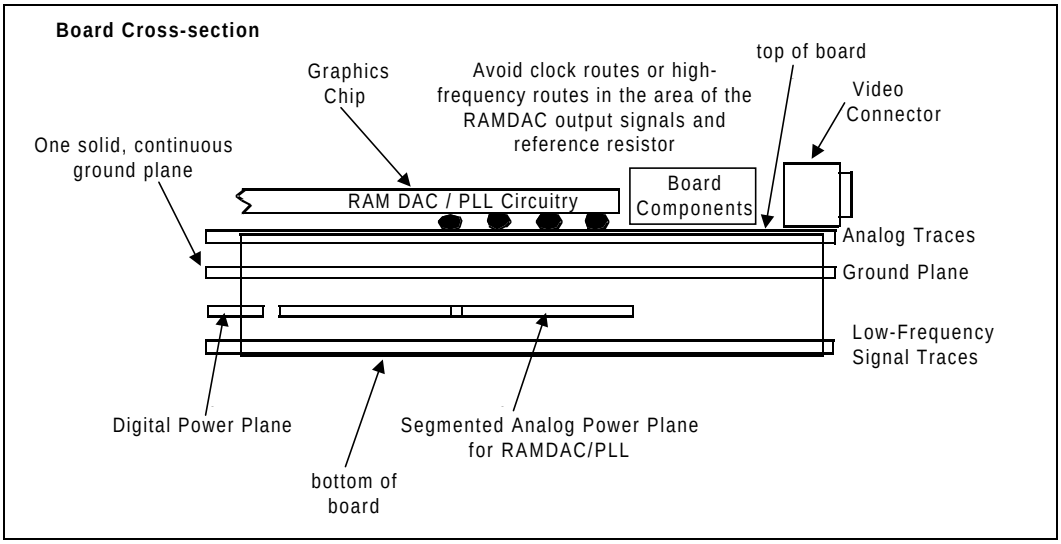
The full-swing video output is designed to be 0.7V according to the VESA video standard. With an equivalent dc resistance of 37.5 ohm (two 75 ohm in parallel - one 75 ohm termination on the board and one 75 ohm termination within the display), the full-scale output current of a RAMDAC channel is 0.7/37.5 ohm = 18.67 mA. Since the RAMDAC is an 8-bit current-steering DAC, this full-scale current is equivalent 255I, where I is a unit current. Therefore, the unit current or LSB current of the DAC signals equals 73.2 µA. The reference circuitry generates a voltage across this R_{set} resistor equal to a bandgap voltage divided-by-three (409 mV). The RAMDAC reference current generation circuitry is designed to generate a 32I reference current using the reference voltage and the R_{set} value. To generate a 32I reference current for the RAMDAC, the reference current setting resistor, R_{set}, is calculated from the following equation:

$$R_{set} = V_{REF}/32I = 0.409V/32*73.2\mu A = 174\ \Omega$$

2.16.2 RAMDAC Board Design Guidelines

Figure 2-38 shows a general cross-section of a typical four-layer board. The recommended RAMDAC routing for a four layer board is such that the red, green and blue video outputs be routed on the top (bottom) layer over (under) a solid ground plane to maximize noise rejection characteristics of the video outputs. It is essential to avoid toggling signals from being routed next to the video output signals to the VGA connector. A 20 mil spacing between any video route and any other routes is recommended.

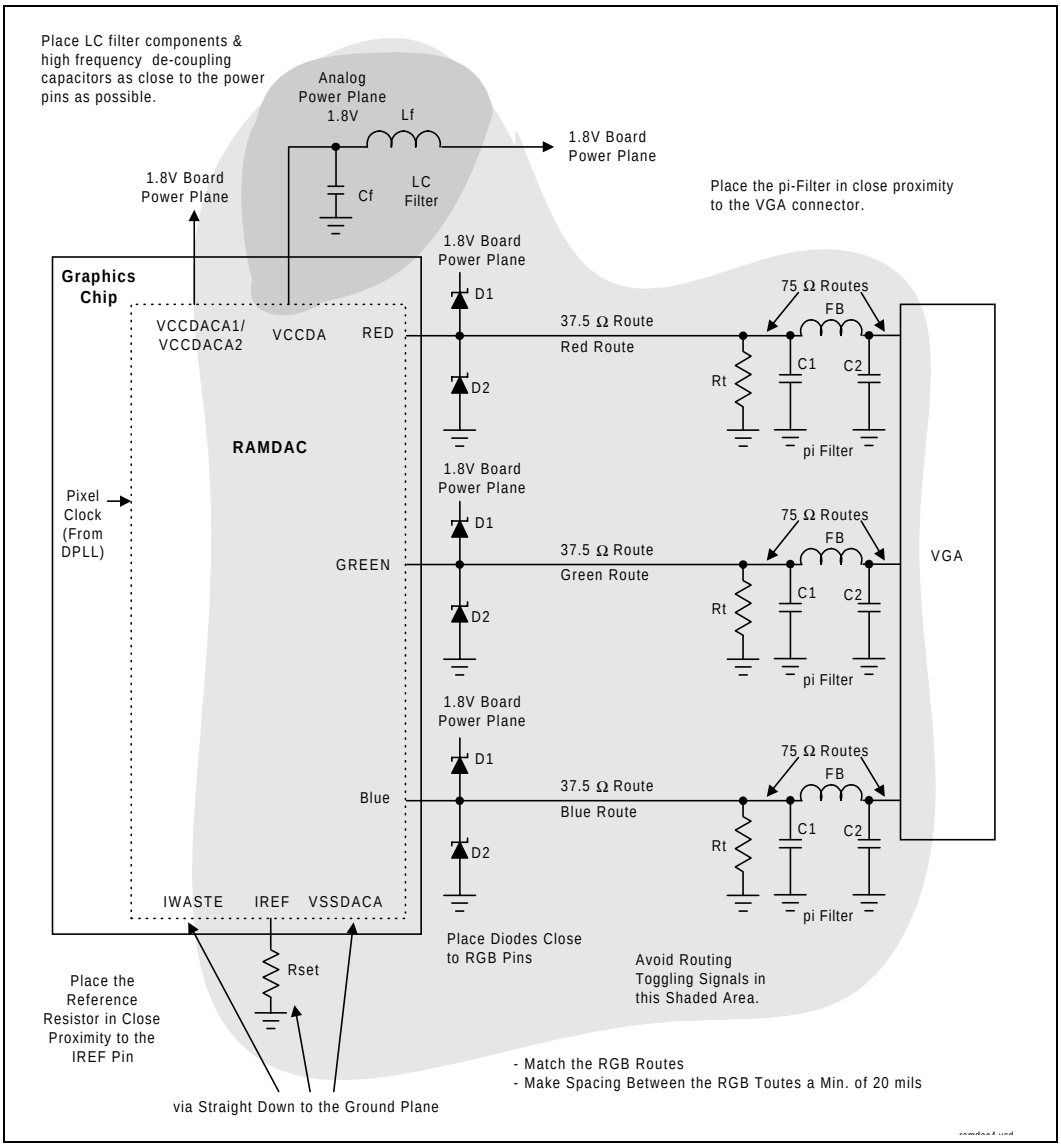
Figure 2-38. Cross-section View of a Four-Layer Board



Matching of the video routes (red, green, and blue) from the RAMDAC to the VGA connector is also essential. The routing for these signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends and jogs).

Figure 2-39 shows recommended RAMDAC component placement and routing. The termination resistance can be placed anywhere along the video route from the RAMDAC output to the VGA connector as long as the impedance of the traces are designed as indicated in Figure 2-39. The pi-filters are recommended to be placed in close proximity to the VGA connector to maximize EMI filtering effectiveness. The LC filter components for the RAMDAC/PLL power plane, de-coupling capacitors, latch-up protection diodes, and the reference resistor are recommended to be placed in close proximity to the respective pins.

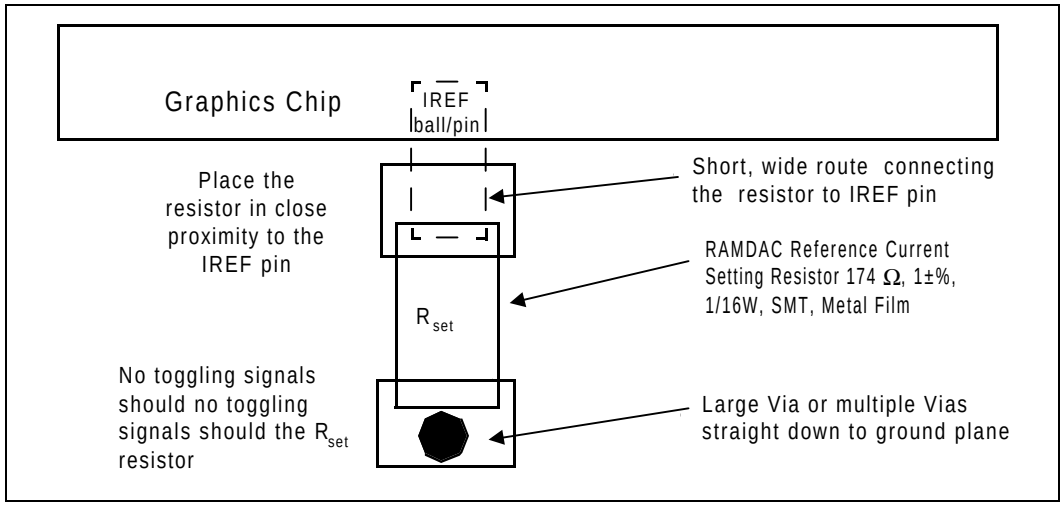
Figure 2-39. RAMDAC Component and Routing Guidelines



NOTE: Diodes D_1, D_2 are clamping diodes and may not be necessary to populate.

Figure 2-40 shows the recommended reference resistor placement and connections.

Figure 2-40. Recommended RAMDAC Reference Resistor Placement and Connections



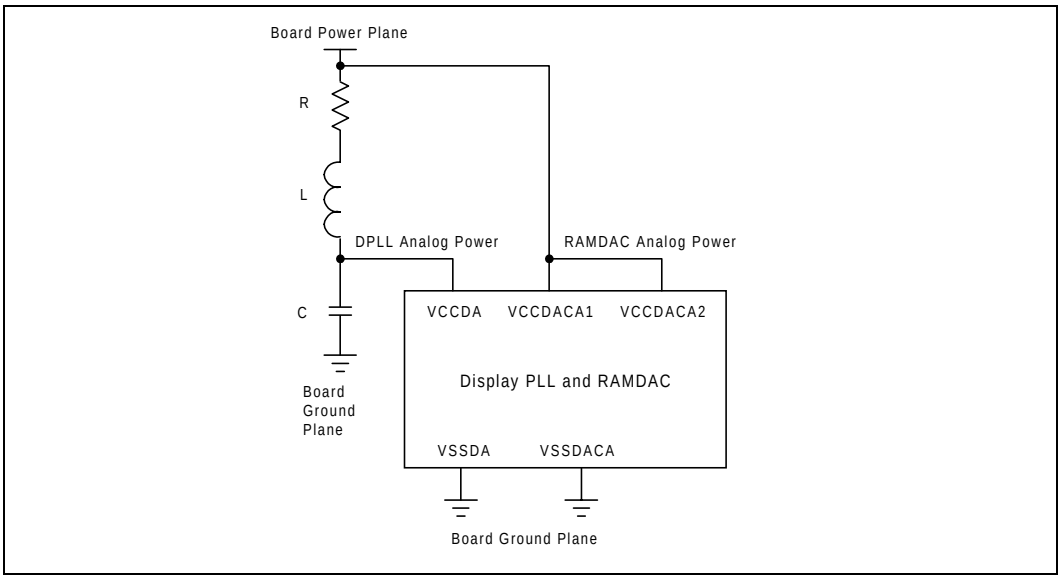
2.17 DPLL Filter Design Guidelines

The Intel® 810 chipset contains sensitive phase-locked loop circuitry, the DPLL, that can cause excessive dot clock jitter. Excessive jitter on the dot clock may result in a “jittery” image. An LC filter network connected to the DPLL analog power supply is recommended to reduce dot clock jitter.

The DPLL bandwidth varies with the resolution of the display and can be as low as 100 KHz. In addition, the DPLL jitter transfer function can exhibit jitter peaking effects in the range from 100 KHz to a few megahertz. A low-pass LC filter is recommended for the display PLL analog power supply designed to attenuate power supply noise with frequency content from 100 KHz and above so that jitter amplification is minimized.

Figure 2-41 is a block diagram showing the recommended topology of the filter connection (parasitics not shown). The display PLL analog power rail (VCCDA) is connected to the board power plane through an LC filter. The RAMDAC analog power rail (VCCDACA1 and VCCDACA2) are connected directly to the 1.8V board power plane.

Figure 2-41. Recommended LC Filter Connection



The resistance from the inductor to the board 1.8V power plane represents the total resistance from the board power plane to the filter capacitor. This resistance, which can be a physical resistor, routing/via resistance, parasitic resistance of the inductor or combinations of these, acts as a damping resistance for the filter and effects the response of the filter.

The LC filter topology shown in Figure 2-41 is the preferred choice since the RAMDAC minimum voltage level requirement does not place constraints on the LC filter for the DPLL. The maximum current flowing into the DPLL analog power is approximately 30 mA, much less than that of the RAMDAC, and therefore, a filter inductor with a higher dc resistance can be tolerated. With the topology in Figure 2-41, the filter inductor dc current rating must be at least 30 mA and the maximum IR drop from the board power plane to the VCCDA ball should be 100 mV or less (corresponds to a series resistance equal to or less than 3.3 ohm. This larger dc resistance tolerance improves the damping and the filter response.

2.17.1 Filter Specification

The low-pass filter specification with the input being the board power plane and the output measured across the filter capacitor is defined as follows for the filter topology shown in Figure 2-41.

- pass band gain < 0.2 dB
- dc IR drop from board power plane to the DPLL VCCDA ball < 100 mV (and a maximum dc resistance < 3.3 ohm)
- filter should support a dc current > 30 mA
- minimum attenuation from 100 kHz to 10 MHz = 10 dB (desired attenuation > 20 dB)
- a magnetically shielded inductor is recommended

The resistance from the board power plane to the filter capacitor node should be designed to meet the filter specifications outlined above. This resistance acts as a damping resistance for the filter and affects the filter characteristics. This resistance includes the routing resistance from the board power plane connection to the filter inductor, the filter inductor parasitic resistance, the routing

from the filter inductor to the filter capacitor, and resistance of the associated vias. Part of this resistance can be a physical resistor. A physical resistor may not be needed depending on the resistance of the inductor and the routing/via resistance.

The filter capacitance should be chosen with as low of an ESR (equivalent series resistance) and ESL (equivalent series inductance) as possible to achieve the best filter performance. The parasitics of the filter capacitor can alter the characteristics of the filter significantly and even cause the filter to be ineffective at the frequencies of interest. The LC filter must be simulated with all the parasitics of the inductor, capacitor, and associated routing parasitics along with tolerances.

2.17.2 Recommended Routing/Component Placement

- The filter capacitance should be placed as close to the VCCDA ball as possible so that the routing resistance from the filter capacitor lead to the package VCCDA ball is < 0.1 ohm.
- The VSSDA ball should via straight down to the board ground plane.
- The filter inductor should be placed in close proximity to the filter capacitor and any routing resistance should be inserted between the board power plane connection and the filter inductor.
- If a discrete resistor is used for the LC filter, the resistor should be placed between the board power plane connection and the filter inductor.

2.17.3 Example LC Filter Components

Table 2-13 and Table 2-14 shows example LC components and resistance for the LC filter topology shown in Figure 2-41.

Table 2-13. DPLL LC Filter Component Example

Component	Manufacturer	Part No.	Description
Capacitor	KEMET	T495D336MD16AS	33 µF ±20%, 16VDC, ESR=0.225 ohm @ 100 kHz, ESL=2.5 nH
Inductor	muRATA	LQG11A68NJ00	68 nH ±5%, 300 mA, Max dc resistance = 0.8 ohm, size=0603
Resistance	—	—	< 3.3 ohm

The resistance of the filter is defined as the total resistance from the board power plane to the filter inductor. If a discrete resistor is used as part of this resistance, the tolerance and temperature coefficient should be accounted for so that the maximum dc resistance in this path from the board power plane connection to the DPLL VCCDA ball is less than 3.3 ohm to meet the IR drop requirement.

Table 2-14. Additional DPLL LC Filter Component Example

Component	Manufacturer	Part No.	Description
Capacitor	KEMET	T495D336MD16AS	33 µF ±20%, 16VDC, ESR=0.225 ohm @ 100 kHz, ESL=2.5 nH
Inductor	muRATA	LQG21NR10K10	100 nH ±10%, 250 mA, Max dc resistance = 0.26 ohm, size=0805, magnetically shielded

As an example, Figure 2-42 is a Bode plot showing the frequency response using the capacitor and inductor values shown in Table 2-14. The capacitor and inductor values were held constant while the resistance was swept for four different combinations of resistance (the resistance of the discrete/trace resistor and the resistance of the inductor), each resulting in a different series resistance. In addition, different values for the resistance of the inductor were assumed based on its max and typical DC resistance. This is summarized in Table 2-15. This yielded the four different frequency response curves shown in Figure 2-42.

Figure 2-42. Frequency Response (see Table 2-15)

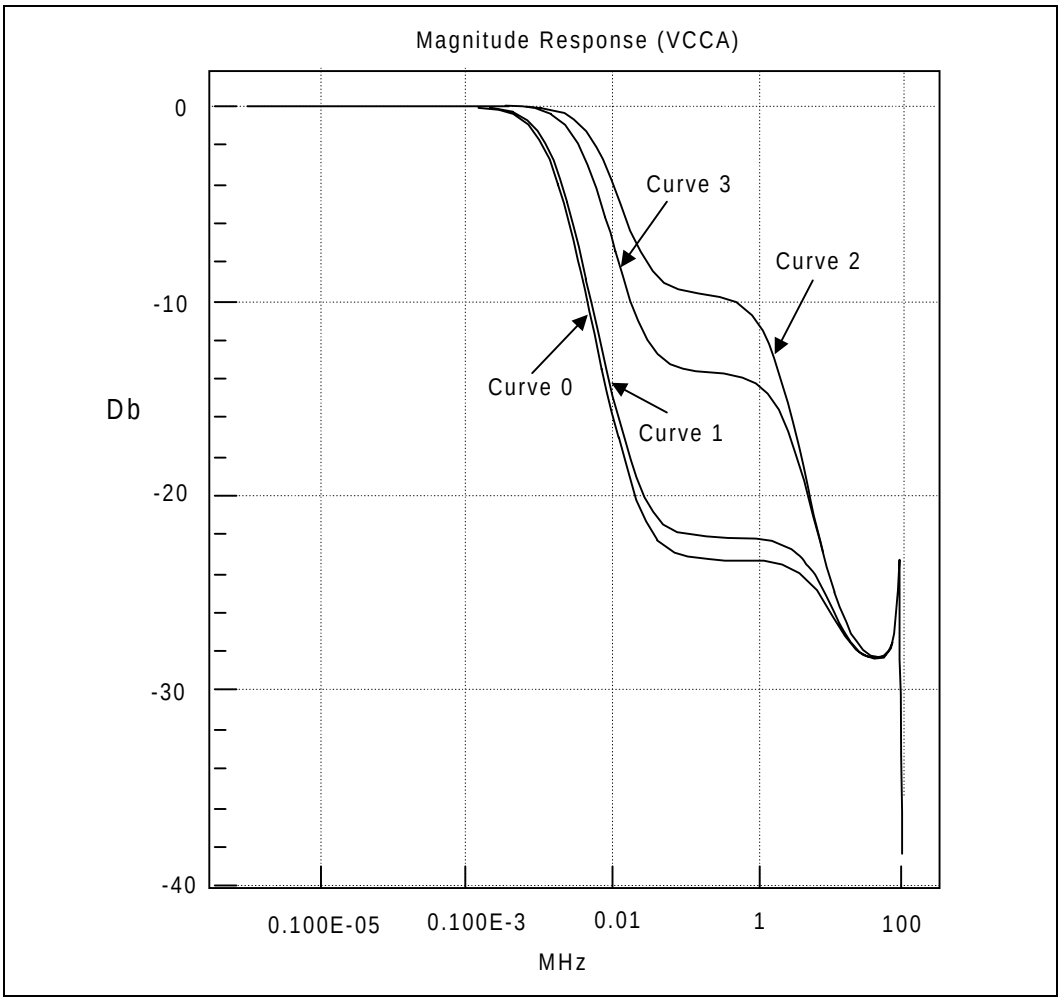


Table 2-15. Resistance Values for Frequency Response Curves (see Figure 2-42)

Curve	$R_{TRACE} + R_{DISCRETE}$	R_{IND}
0	2.2 ohm	0.8 ohm
1	2.2 ohm	0.4 ohm
2	0 ohm	0.4 ohm
3	0 ohm	0.8 ohm

As series resistance ($R_{TRACE} + R_{DISCRETE} + R_{IND}$) increases, the filter response (i.e., attenuation in PLL bandwidth) improves. There is a limit of 3.3 ohm total series resistance of the filter to limit DC voltage drop.

3

Clocking

Clocking 3

3.1 Clock Generation

There is only one clock generator component required in an Intel® 810 chipset system. The CK810 is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clocks are 2.5V. As a result, the CK810 device requires both 3.3V and 2.5V. These power supplies should be as clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines.

The clocking chip comes in a single 56-pin SSOP package. This provides the clock frequencies listed in Table 3-1.

Table 3-1. Intel® 810 Chipset Clocks

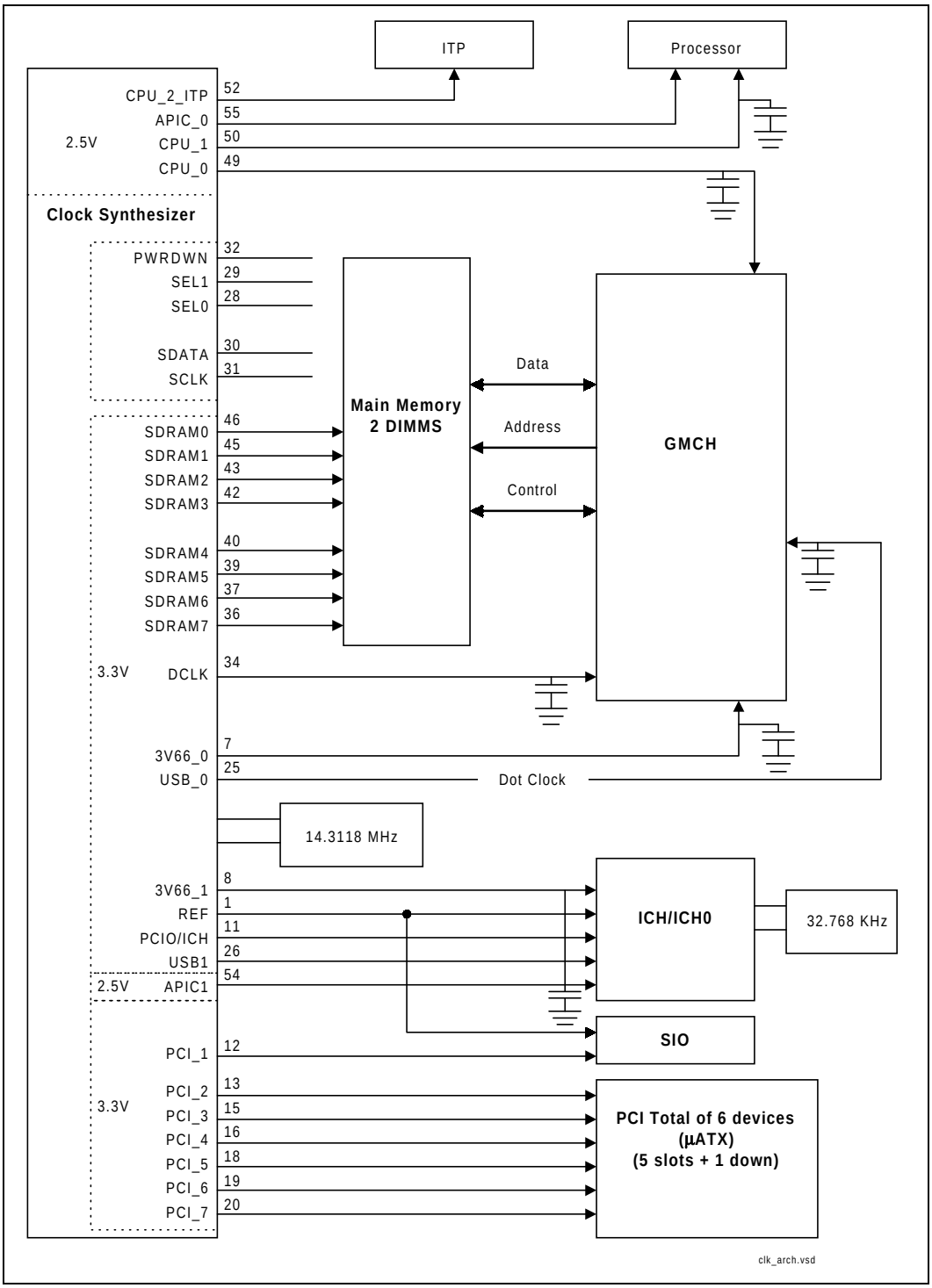
Number	Clock	Frequency
3	CPU Clocks	66/100 MHz
9	SDRAM Clocks	100 MHz
8	PCI Clocks	33 MHz
2	APIC Clocks	16.67/33 MHz
2	48 MHz Clocks	48 MHz
2	3V66 MHz Clocks	66 MHz
1	REF Clock	14.31818 MHz

Features (56 Pin SSOP Package)

- 3 copies of processor Clock 66 MHz/100 MHz (2.5V) [CPU, GCH, ITP]
- 9 copies of 100 MHz (all the time) SDRAM Clock (3.3V) [SDRAM[0:7], DClk]
- 8 copies of PCI Clock (33 MHz) (3.3V)
- 2 copies of APIC Clock @16.67 MHz or 33 MHz, synchronous to CPU Clock (2.5V)
- 2 copy of 48 MHz Clock (3.3V) [Non SSC]
- 2 copies of 3V66 MHz Clock (3.3V)
- 1 copy of REF Clock @14.31818 MHz (3.3V) also used as input strap to determine APIC frequency
- 66 MHz or 100 MHz CPU operation (selectable at power up only)
- Ref. 14.31818 MHz Xtal Oscillator Input
- Power Down Pin
- Spread Spectrum Support
- I^2C Support for turning off unused clocks

3.2 Clock Architecture

Figure 3-1. Intel® 810 Chipset Clock Architecture



3.3 Clock Routing Guidelines

Table 3-2 shows the group skew and jitter limits.

Table 3-2. Group Skew and Jitter Limits at the Pins of the Clock Chip

Signal Group	Pin-Pin Skew	Cycle-Cycle Jitter	Nominal Vdd	Skew, jitter measure point
CPU	175 pS	250 pS	2.5V	1.25V
SDRAM	250 pS	250 pS	3.3V	1.50V
APIC	250 pS	500 pS	2.5V	1.25V
48 MHz	250 pS	500 pS	3.3V	1.50V
3V66	175 pS	500 pS	3.3V	1.50V
PCI	500 pS	500 pS	3.3V	1.50V
REF	N/A	1000 pS	3.3V	1.50V

Table 3-3 shows the Signal Group and Resistor Tolerance.

Table 3-3. Signal Group and Resistor

Signal Group	Resistor
CPU	33 ohm ± 5%
SDRAM/DCLK	22 ohm ± 5%
3V66	22 ohm ± 5%
PCI	33 ohm ± 5%
TCLK	22 ohm ± 5%
OCLK/RCLK	33 ohm ± 5%
48 MHz	33 ohm ± 5%
APIC	33 ohm ± 5%
REF	10 ohm ± 5%

Table 3-4 shows the layout dimensions for the clock routing.

Note: All the clock signals must be routed on the same layer which reference to a ground plane.

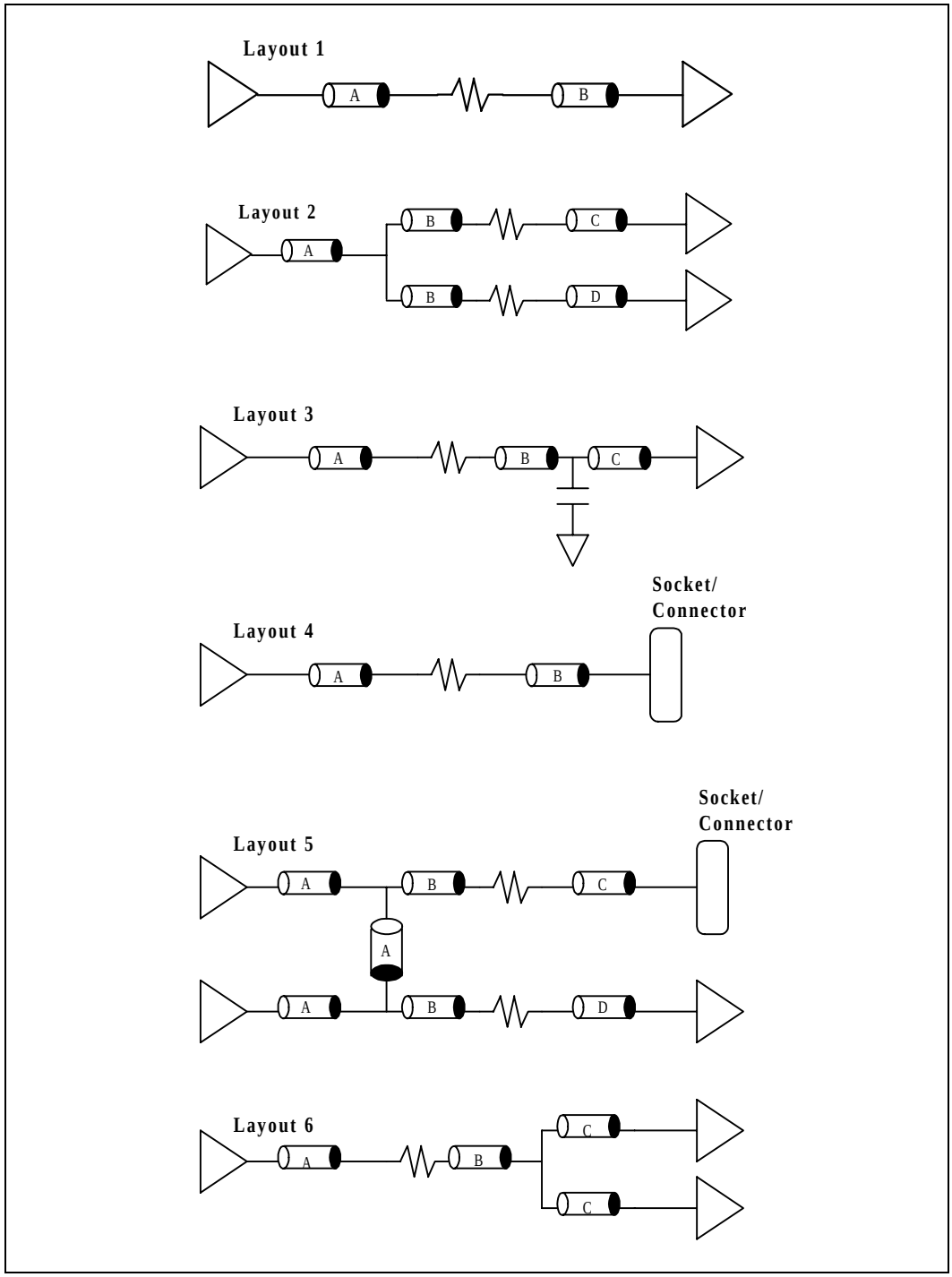
Table 3-4. Layout Dimensions

Group	Receiver	Resistor	Cap	Topology	A	B	C	D
SDRAM	DIMM	22 ohm	N/A	Layout 1	0.5”	X	N/A	N/A
CPU	Segment C => PPGA Segment D => GMCH	33 ohm	N/A	Layout 5	0.1”	0.5”	X+4.1	X+5.55”
DCLK	GMCH	22 ohm	22 pf	Layout 3	0.5”	X+2.4”	0.5”	N/A
3V66	GMCH	22 ohm	18 pF	Layout 3	0.5”	X+0.8”	0.5”	N/A
3V66	ICH	22 ohm	18 pF	Layout 3	0.5”	X+0.8”	0.5”	N/A
PCI	PCI device	33 ohm	N/A	Layout 1	0.5”	X+3.85” to X+10.1”	N/A	N/A
PCI	PCI socket	33 ohm	N/A	Layout 4	0.5”	X+0.4” to X+6.85”	N/A	N/A
PCI	ICH	33 ohm	N/A	Layout 1	0.5”	X+4.0”	N/A	N/A
TCLK	SDRAM	22 ohm	N/A	Layout 6	0.5”	1.5” to 2.5”	0.75” to 1.25”	N/A
OCLK/RCLK	GMCH	33 ohm	N/A	Layout 1	0.5”	3.25” to 3.75”	N/A	N/A
APIC	PPGA	33 ohm	N/A	Layout 4	0.5”	Y	N/A	N/A
APIC	ICH	33 ohm	N/A	Layout 1	0.5”	Y+2.4”	N/A	N/A

NOTE: X and Y trace lengths are arbitrary. Simulations were performed with each X=2", 4", and 6.”

Figure 3-2 shows the different topologies used for the clock routing guidelines.

Figure 3-2. Different Topologies for the Clock Routing Guidelines

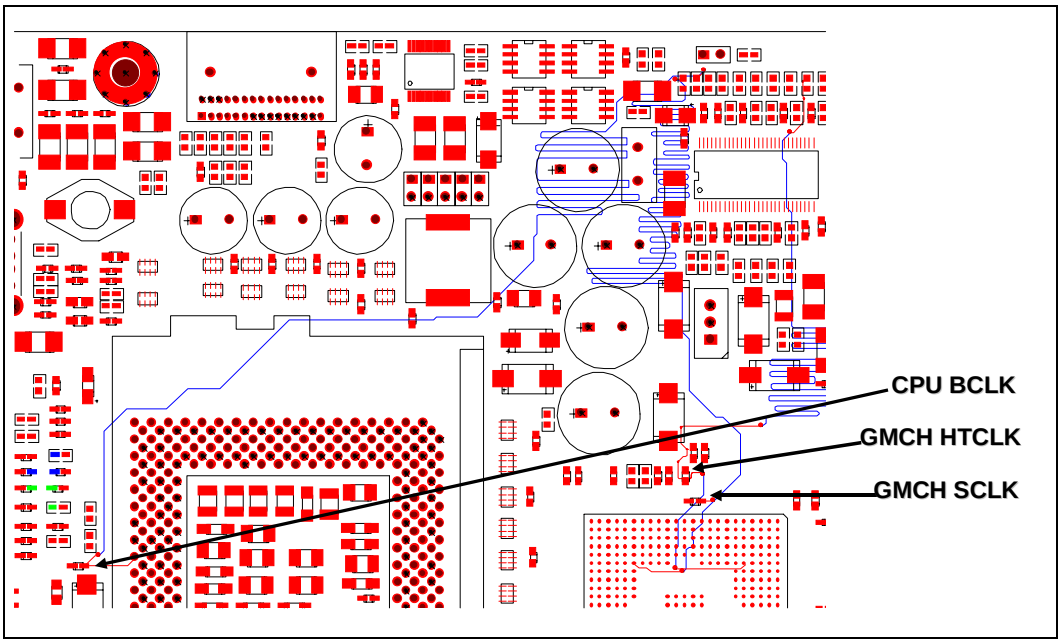


3.4 Capacitor Sites

Intel recommends 0603 package capacitor sites placed as close as possible to the clock input receivers for AC tuning for the following signal groups:

- GMCH
- Processor
- SDRAM/DCLK
- 3V66
- 3V66 to the ICH0/ICH

Figure 3-3. Example of Capacitor Placement Near Clock Input Receiver



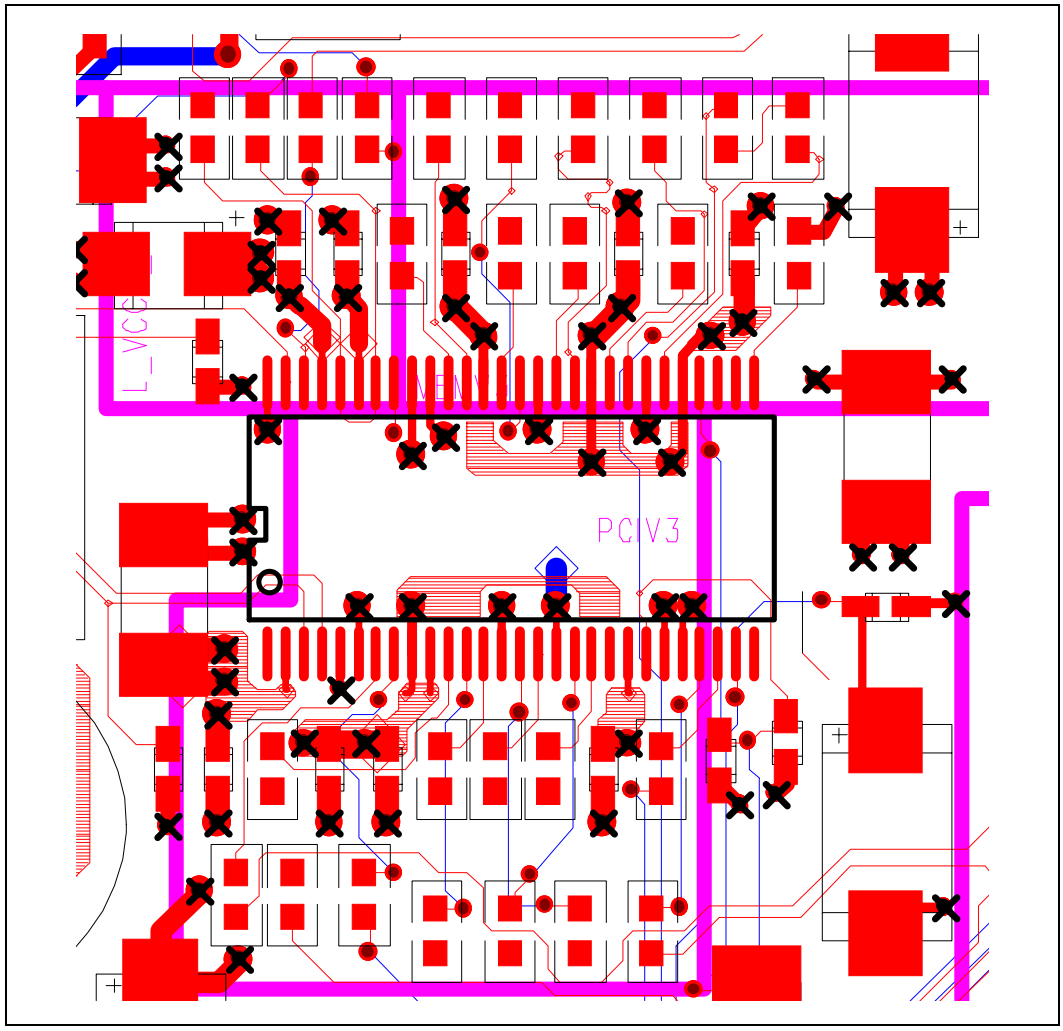
3.5 Clock Power Decoupling Guidelines

Several general layout guidelines should be followed when laying out the power planes for the CK810 clock generator.

- Isolate power planes to the each of the clock groups.
- Place local decoupling as close to power pins as possible and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14 mil finished hole with a 24–26 mil path. An example power via is an 18 mil finished hole with a 33–38 mil path. For large decoupling or power planes with large current transients it is recommended to use a larger power via.

An example of clock power layout is presented in Figure 3-4.

Figure 3-4. Example of Clock Power Plane Splits and Decoupling



3.6 Clock Skew Requirements

To ensure correct system functionality, certain clocks must maintain a skew relationship to other clocks as summarized in Section 3.6.1.

3.6.1 IntraGroup Skew Limits

Clocks within each group must maintain appropriate skew relationship to each other. These requirements are summarized in Table 3-5.

Table 3-5. Clock Skew Requirements

Group Pair	Skew Limit	Measurement Point of Receiver
CPU BCLK to GMCH HTCLK	350 pS window	Pin on top of PPGA PKG GMCH Ball
GMCH SCLK to DIMM Clocks	±630 pS Referenced to GMCH SCLK	GMCH Ball DRAM Component Pin on Module
GMCH HubCLK to ICH HubCLK	575 pS window	GMCH Ball ICH Ball

4

System Design Considerations

System Design Considerations 4

4.1 Power Delivery

Power delivery terminology definitions are indicated in Section 1.1, “About This Design Guide” on page 1-1.

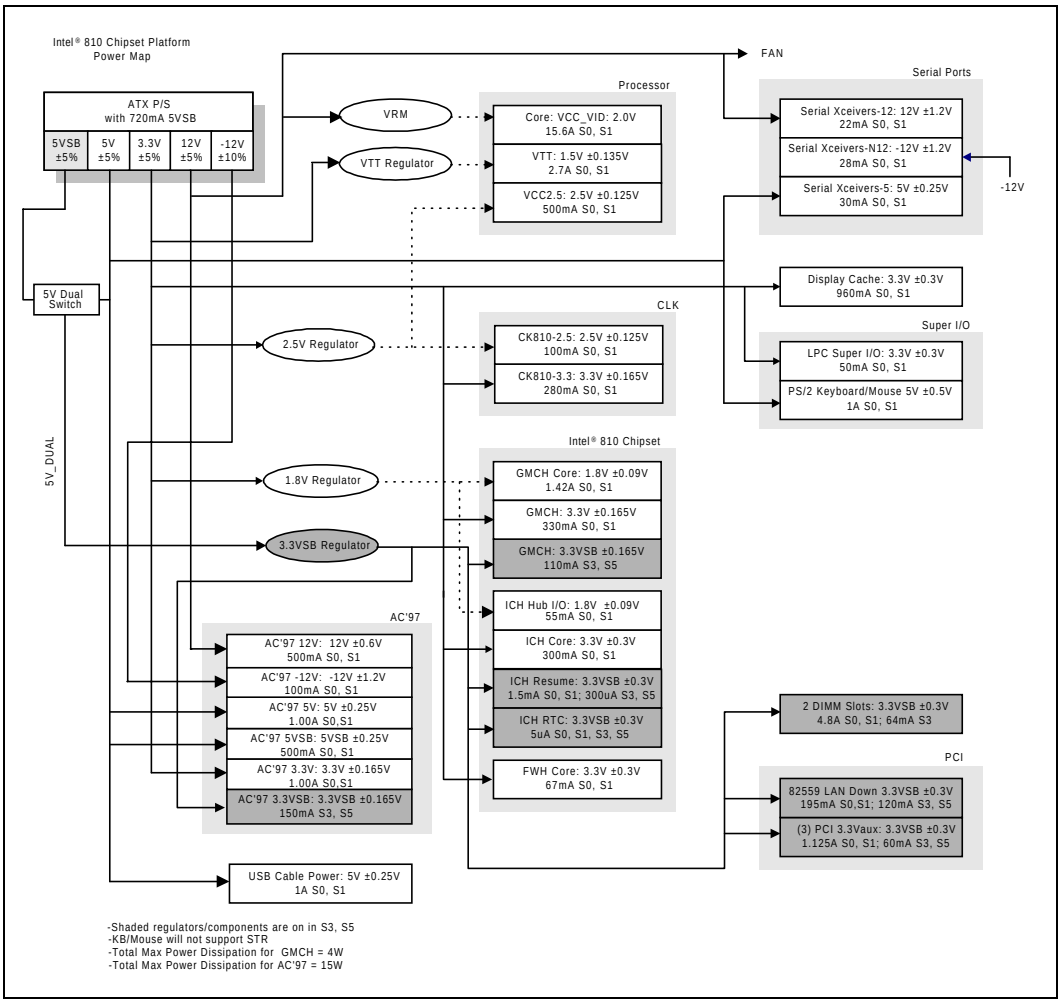
4.1.1 Intel® 810 Chipset CRB Power Delivery

Figure 4-1 shows the power delivery architecture for the Intel® 810 Customer Reference Board (CRB). This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the *suspend-to-RAM* (STR) state.

During STR, only the necessary devices are powered. These devices include: main memory, the ICH resume well, PCI wake devices (via 3.3Vaux), the Intel® 82559 LAN down chip, AC’97 and optionally USB (USB can only be powered if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in *suspend* and in *full-power*. The power requirements should be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions given in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical, when deviating from these examples to consider the effect of the change.

Figure 4-1. Intel® 810 Chipset Power Delivery Architecture



NOTE: The above current values represent the maximum sustained current draw.

Table 4-1. Intel® 810 Chipset Power Map

Voltage	Description	Voltage Lo (V)	Voltage Nom (V)	Voltage Hi (V)	Current Max (mA)	Power Max[1] (mW)	Current Max (SB) (mA)	Power Max[2] (SB) (mW)
1.5 V	Processor V_{TT}	1.365	1.5	1.635	2700	4414.5	N/A	N/A
1.8 V	ICH Hub interface I/O	1.710	1.8	1.890	55	103.95	N/A	N/A
	GMCH Core	1.710	1.8	1.890	1420	2683.8	N/A	N/A
2.0 V	processor VCC_{CORE}		2.0		15600	31200	N/A	N/A
2.5 V	CLK-2.5	2.375	2.5	2.625	100	262.5	N/A	N/A
	processor 2.5V	2.375	2.5	2.625	500	1312.5	N/A	N/A
3.3 V	CLK-3.3	3.135	3.3	3.465	280	970.2	N/A	N/A
	ICH Core	3.000	3.3	3.600	300	1080	N/A	N/A
	Display Cache	3.000	3.3	3.600	960	3456	N/A	N/A
	FWH Core	3.000	3.3	3.600	67	241.2	N/A	N/A
	AC'97 3.3V	3.135	3.3	3.465	1000	3465	N/A	N/A
	GMCH	3.135	3.3	3.465	330	1143.45	N/A	N/A
	Super I/O	3.000	3.3	3.600	50	180	N/A	N/A
3.3 VSB	ICH Resume	3.000	3.3	3.600	0.3	1.08	1.5	5.4
	ICH RTC	3.000	3.3	3.600	0.005	0.018	0.006	0.0216
	GMCH	3.135	3.3	3.465	N/A	N/A	110	103.95
	PCI (3 slots)	3.000	3.3	3.600	1125	4050	60	216
	82559 LAN Down	3.000	3.3	3.600	195	702	120	432
	AC'97 3.3 VSB	3.135	3.3	3.465	1000	3465	150	519.75
	2 DIMM Slots	3.000	3.3	3.600	4800	17280	64	230.4
5 V	Serial Xceivers-5	4.500	5.0	5.500	30	165	N/A	N/A
	Keyboard/Mouse	4.500	5.0	5.500	1000	5500	N/A	N/A
	AC'97 5V	4.750	5.0	5.250	1000	5250	N/A	N/A
	USB	4.750	5.0	5.250	1000	5250	N/A	N/A
	AC'97 5 VSB	4.750	5.0	5.250	500	2625	N/A	N/A
12 V	AC'97 12V	11.400	12.0	12.600	500	6300	N/A	N/A
	Serial Xceivers 12V	10.800	12.0	13.200	22	290.4	N/A	N/A
-12 V	AC'97 -12V	10.800	12.0	13.200	100	1320	N/A	N/A
	Serial Xceivers -12V	10.800	12.0	13.200	28	369.6	N/A	N/A
TOTAL						**101.1 W**	**505.5 mA**	**1.79 W**

NOTES:
1. Power Max is calculated using the values from Voltage Hi and Current Max columns (V Hi x I Max).
2. Power Max (SB) is calculated using the values from Voltage Hi and Current Max (SB) columns (V Hi x I Max (SB)).

In addition to the power planes provided by the ATX power supply, an *instantly available* Intel® 810 chipset system (using *Suspend-to-RAM)* requires 6 power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the Intel® 810 chipset Customer Reference Board will have a *5V Dual Switch*.

5V Dual Switch

This switch powers the *5V Dual plane* from the 5V core ATX supply during *full-power* operation. During *Suspend-to-RAM,* the *5V Dual plane* will be powered from the 5V Standby power supply.

Note: The voltage on the 5V Dual plane **is not 5.0V!** There is a resistive drop through the *5V Dual Switch* that should be considered. Therefore, NO COMPONENTS should be connected directly to the 5V Dual plane. On the Customer Reference Board, the only device connected directly to the 5V Dual plane is the 3.3V voltage regulator (to regulate to lower voltages).

Table 4-2. Intel® 810 Chipset Voltage Regulator Specifications

Voltage	Max Current
1.5 V	2.7 A
1.8 V	1.5 A
2.5 V	0.6 A
3.3 V	7.2 A
VCC_{CORE}	15.6 A

VCC_{CORE}

This power plane is used to power the processor. Refer to the latest revisions of the following documents:

- *VRM 8.2 DC-DC Converter* Design Guidelines
- *PPGA 370 Power Delivery* Guidelines

Note: This regulator is required in ALL designs.

V_{TT}

This power plane is used to power the AGTL+ termination resistors. Refer to the latest revisions of:

- *Intel® Celeron™ Processor* Datasheet

Note: This regulator is required in ALL designs.

1.8V

The 1.8V plane powers the GMCH core, the ICH Hub interface I/O, and digital video out. This voltage is obtained from using a 1.8V voltage regulator that regulates the voltage from the 3.3V power supply voltage (or the 5V power supply voltage).

Note: This regulator is required in ALL designs.

2.5V

The 2.5V plane powers the 2.5V rail of the clock synthesizer and the CMOS pullups to the processor. The total maximum current requirement is approximately 100 mA. This voltage is obtained from using a 2.5V voltage regulator that regulates the voltage from the 3.3V power supply voltage (or the 5V power supply voltage).

Note: This regulator is required in ALL designs.

3.3VSB

The 3.3VSB plane powers the suspend well of the ICH, the ICH Real Time Clock, the AC'97 AMR connector, the 2 DIMM slots, and the PCI 3.3Vaux suspend power pins.

The 3.3Vaux requirement state that during suspend, the system must deliver 375 mA to each *wake-enabled* card and 20 mA to each *non wake-enabled* card. During *full-power* operation, the system must be able to supply 375 mA to *EACH* card. Therefore, the total current requirement for the PCI 3.3Vaux suspend power pins is:

- *Full-power Operation:* 375 mA*number of PCI slots
- *Suspend Operation:* 375+20*(number of PCI slots – 1)

The total maximum current requirement for the 3.3VSB power plane (as well as the 3.3V regulator) is 7.12 A.

Note: This regulator is required in ALL designs.

4.1.2 LED Indicator for S0-S5 States

Although not required by the ACPI Specification, Intel recommends that an on-board LED be implemented that informs the user that the system is in a full-on or a sleep state (as opposed to a mechanical off state). In general, depending on the particular implementation, it may not be safe to add/remove hardware to the system while the system is in an S5 state. Since the S5 state may closely resemble the mechanical off state, (i.e., display blank, fans off, no noise, etc.) this LED indicator, when lit, lets the user know that it is NOT safe to add/remove hardware to the system. Implementation of this LED indicator may help prevent hardware damage to the system when a user is changing hardware. This may be implemented by connecting an LED to one of the auxiliary power supplies.

4.2 Decoupling Guidelines

4.2.1 Vcc_{CORE} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep an interconnect resistance from the regulator (or VRM pins) to the Socket pins of less than 0.3m ohm. This can be accomplished by keeping a maximum distance of 1.0 inches between the regulator output and Socket Vcc pins. The recommended Vcc_{CORE} interconnect is a 2.0 inch wide (the width of the VRM 8.2 connector) by 1.0 inch long (maximum distance between the 370-pin socket and the VRM connector) plane segment with a standard 1-ounce plating. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, is provided on the voltage regulation module (VRM) defined in the *VRM 8.2 DC-DC Converter Design Guidelines*. The Vcc_{CORE} supply should be capable of delivering a recommended minimum dI_{CCCORE}/dt while maintaining the required tolerances.

Adequate decoupling capacitance should be placed near the power pins of the Intel® Celeron™ processor PPGA. In order to obtain optimal performance Intel recommends using 10 or more 4.7 uF 1206-style capacitors and 19 or more 1.0 uF 0805-style capacitors when using a conventional Voltage Regulator Module. Inductance should be reduced by connecting capacitors directly to the Vcc_{CORE} and Vss planes with minimal trace length between the component pads and vias to the plane. Be sure to include the effects of board inductance within the simulation. Also, when choosing the capacitors to use, keep in mind the operating temperatures that will be seen and the rated tolerance.

Bulk capacitance with a low Effective Series Resistance (ESR) should also be placed near the Intel® Celeron™ processor PPGA to handle changes in average current between the low-power and normal operating states. About 9000 uF of capacitance with an ESR of 5m ohm makes a good starting point for simulations, although more capacitance may be needed to bring the ESR down to this level due to the current technology in the industry. Voltage Regulator Modules already contain this bulk capacitance. Be sure to determine what is available on the market before choosing parameters for the models. Also, include power supply response time and cable inductance in a full simulation.

The Intel® Celeron™ processor PPGA does not contain high frequency decoupling capacitance on the processor package. High frequency decoupling and bulk decoupling should be provided for by the system motherboard for proper AGTL+ bus operation.

Although the system bus receives power external to the processor, this power supply will also require the same diligent decoupling methodologies as the processor. Note that the existence of external power entering through the I/O buffers causes Vss current to be higher than the Vcc_{CORE} current. For more information the following documents are recommended:

- *Pentium® II Processor AGTL+ Guidelines*
- *Pentium® II Processor Power Distribution Guideline*
- *Pentium® II Processor Developer's Manual*

4.2.2 Phase Lock Loop (PLL) Decoupling

Isolated analog decoupling is required for the internal PLL. This should be a 22 µF ±20% capacitor and a 22 µH ±30% inductor. The capacitor should be across the PLL1 and PLL2 pins of the processor. The inductor should be connected from PLL1 to Vcc_{CORE}.

4.2.3 GMCH Decoupling Guidelines

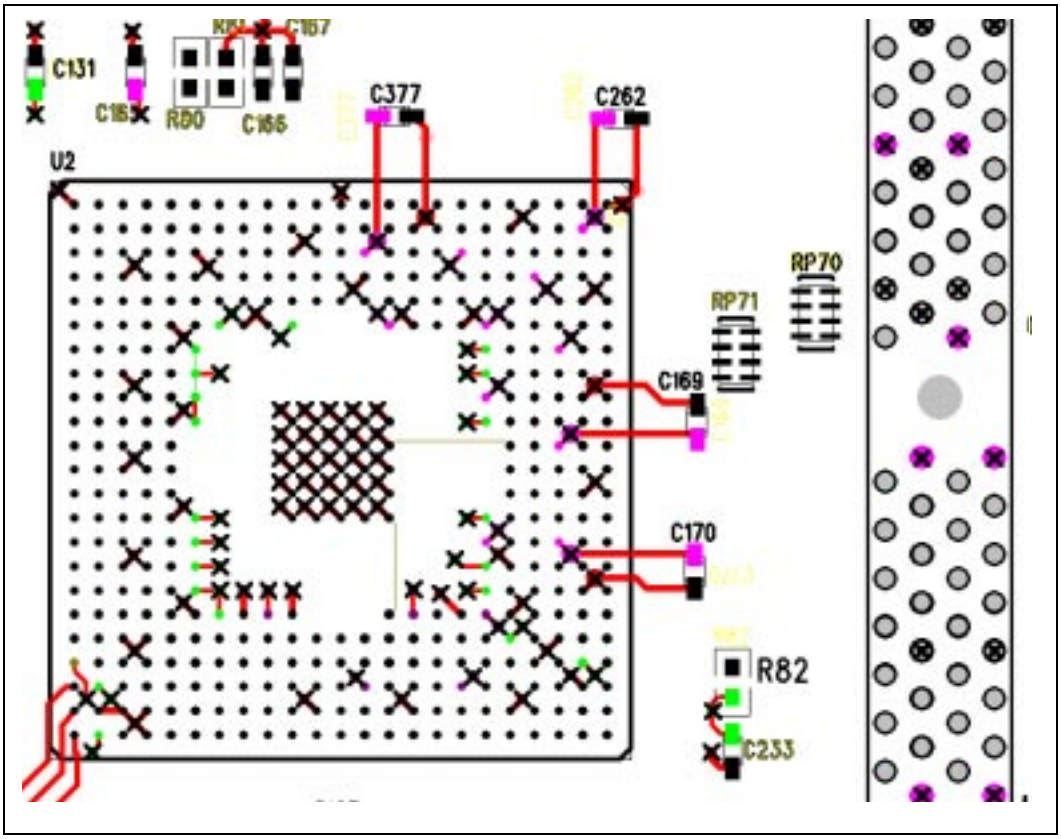
GMCH Vsus 3.3V (3.3V Standby) Power Plane Decoupling

- 3.3V Droop Spec.
  - — Worse case droop on 3.3V plane must not go below 2.5 V.
  - — *Droop below the minimum Vcc of 3.135 V must not occur for a period greater than 2ns.*
- Place four 0.01 µF decoupling capacitors as close as possible to GMCH.
  - — Trace from cap pad to via < 500 mils (Ideal = 300 mils).
  - — Trace width at least 15 mils.
- Use power vias (multiple if possible).
  - — Power via example: 18 mil drill, 33–38 mil width.
- Place capacitors orientation such that flight time will be minimized.
  - — Vias between GMCH ball and cap pad (see Figure 4-2).

Power Plane Layout

- Make the power planes as square as possible with no sharp corners.
- Avoid crossing traces over multiple power planes.

Figure 4-2. GMCH Power Plane Decoupling



4.3 Power Delivery Guidelines

These are general power delivery guidelines for the 370-pin socket. This power delivery guideline is set up to cover the maximum decoupling guidelines covering both the Intel® Celeron™ processor and future processors.

Note: These guidelines are developed only for the Basic PC products, and should NOT be confused with their cartridge (performance) counterparts.

4.3.1 Decoupling Requirement

VCC_{CORE} Decoupling Design

PPGA (on motherboard) processor

VCC_{CORE} = 2.0V, Icc_{CORE} = 0.8A ~ 14A

- Ten or more 4.7 uF in 1206 package (ceramic X5R or better)
  - — All capacitors will be placed within the socket hole and mounted directly on the primary side of the motherboard. The capacitors are arranged so to minimize the overall inductance between Vcc/Vss power pins.
- Nineteen or more 1.0 uF in 0805 package
  - — All capacitors will be placed within the socket hole and mounted directly on the primary side of the motherboard. The capacitors are arranged so to minimize the overall inductance between Vcc/Vss power pins.

These capacitors are shown on the interior section of Figure 4-3.

V_{TT} Decoupling Design

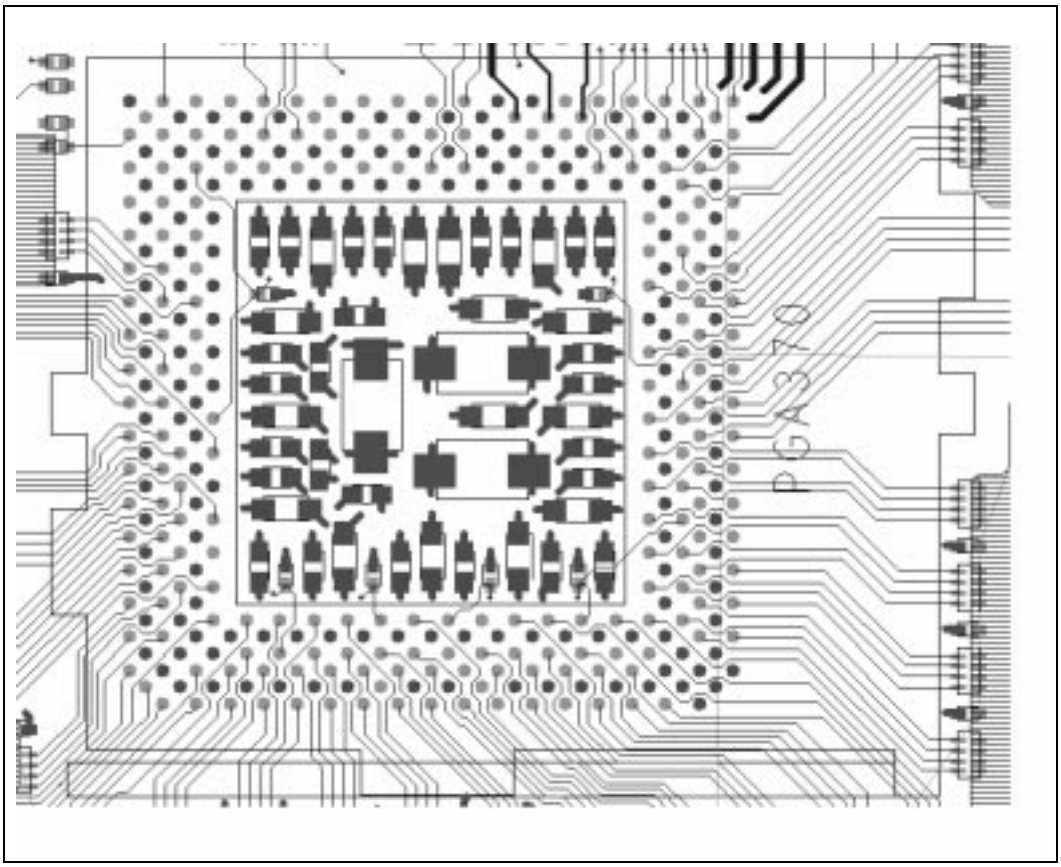
For I_{TT} = 3.5 (max),

Fourteen capacitors 0.1uF in 0603 package placed within 200 mils of R-packs, one capacitor for every two R-packs. These capacitors are shown on the outer exterior of Figure 4-3.

V_{REF} Decoupling Design

Four 0.1 uF capacitors in 0603 package placed near the V_{REF} pins (within 500 mils). These capacitors are shown on the interior section of Figure 4-3.

Figure 4-3. 370-Pin Socket



NOTE: Although there appears to be more capacitors allocated than the requirement listed, this figure is simply a layout study, and shows more than the minimum amount of capacitors needed. This figure should be used more as a visual aid than an actual representation of the decoupling guidelines.

Figure 4-3 shows the area on the motherboard allocated for the processor. The high frequency decoupling capacitors are allocated in the center of Figure 4-3, containing 1206 and 0805 packages. The configuration of their layout is such that the trace length from the capacitors to the Vcc/Vss pins are minimized as possible to reduce the trace length inductance. The 1206 packages are located by realizing that they are slightly larger in size than the 0805 packages.

4.3.2 Power Plane Layout Guideline

GND Plane and VCC_{CORE} Power Plane

Located directly underneath the processor plane as shown in Figure 4-3. No split planes.

V_{TT} Power Supply

Cut plane on the top layer surrounding the socket.

V_{REF} Power Supply

Flat cut trace (25 mils) surrounding the interior of the socket.

4.4 Thermal Design Power

Thermal Design power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP of the GMCH component is 4.0 W.

4.5 Power Sequencing

This section shows the timings between various signals during different power state transitions.

Figure 4-4. G3-S0 Transistion

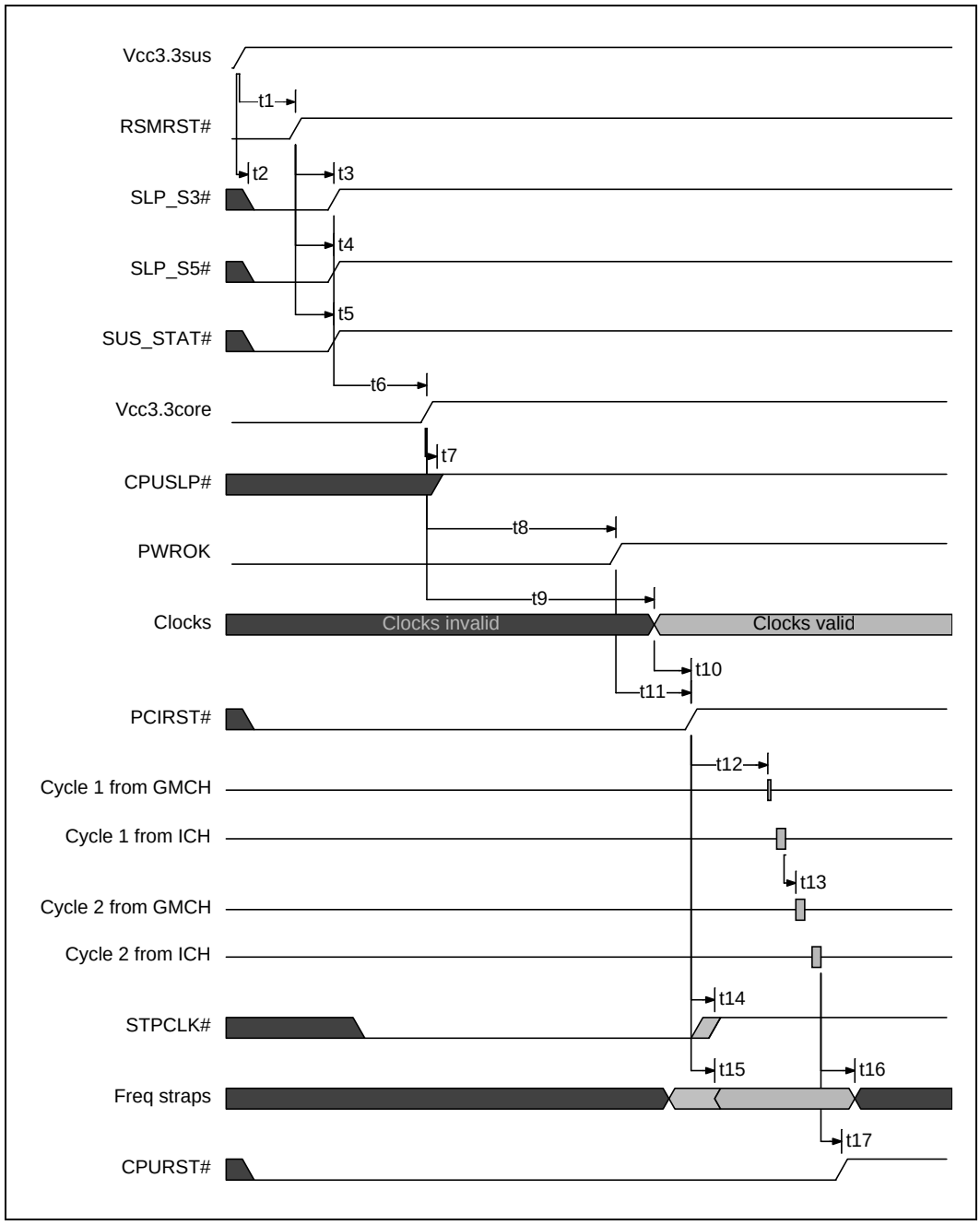


Figure 4-5. S0-S3-S0 Transition

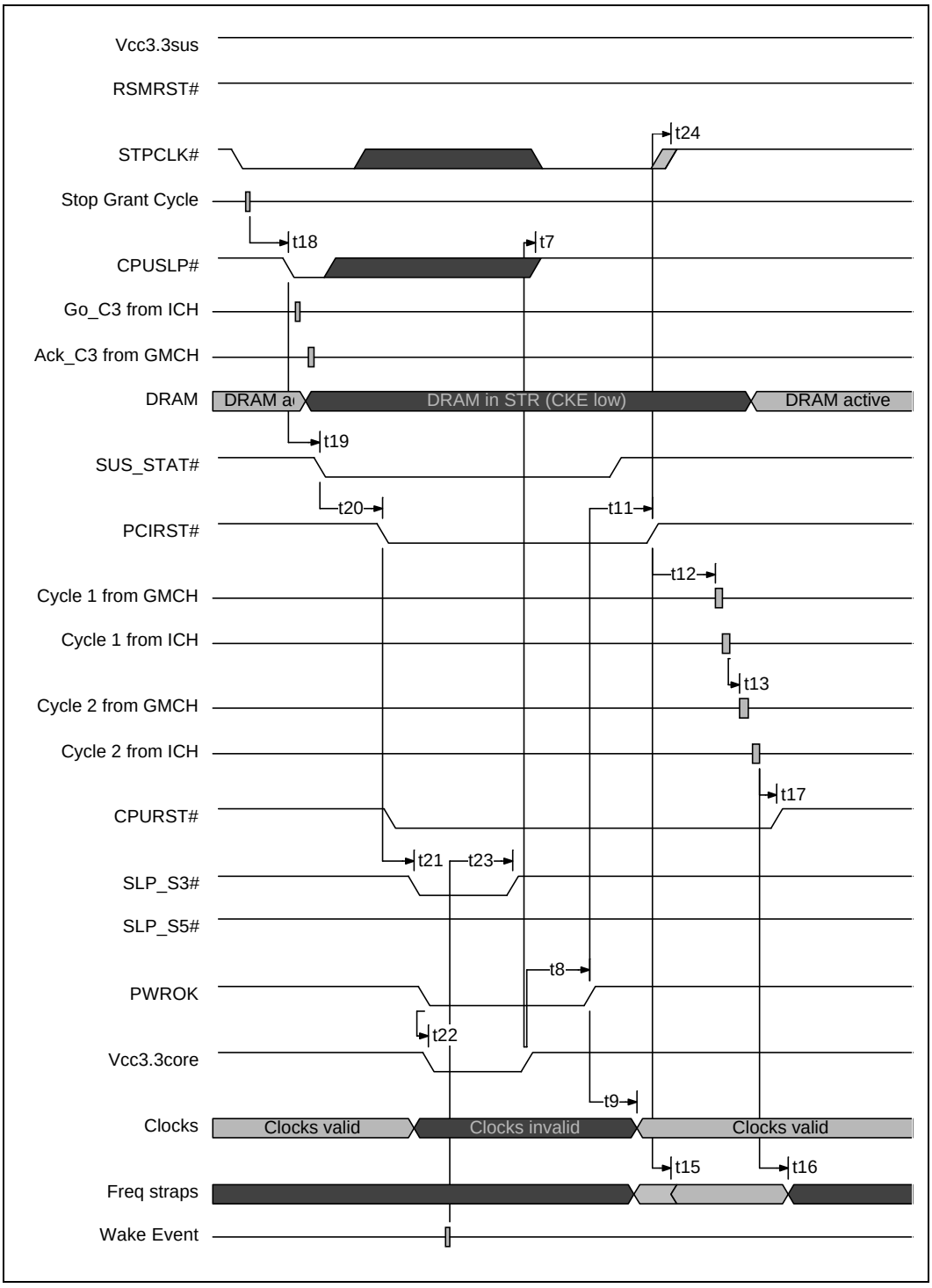


Figure 4-6. S0-S5-S0 Transition

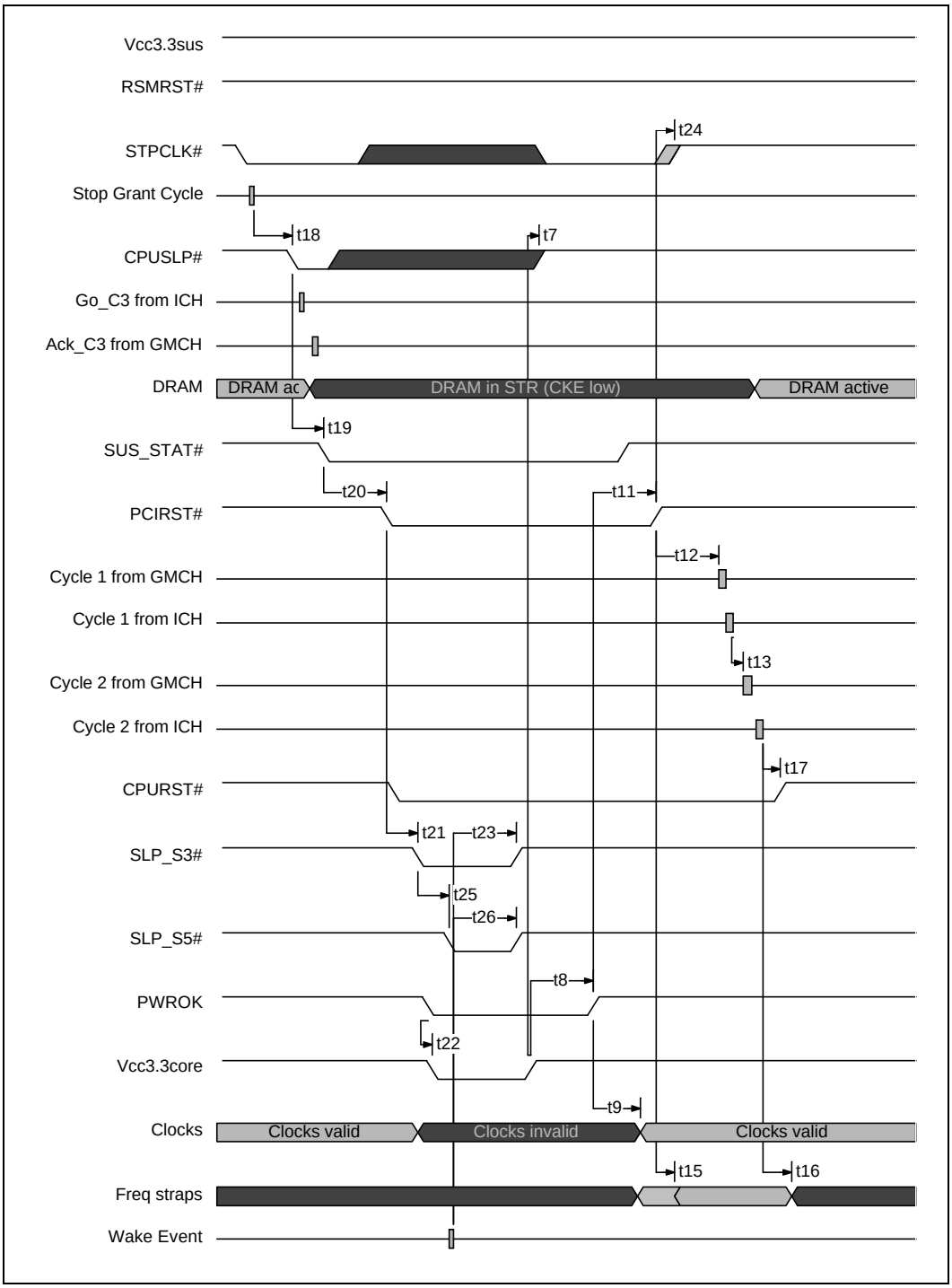


Table 4-3. Power Sequencing Timing Definitions

Symbol	Parameter	Min.	Max.	Units
t1	VccSUS Good to RSMRST# inactive	1	25	ms
t2	VccSUS Good to SLP_S3#, SLP_S5#, and PCIRST# active		50	ns
t3	RSMRST# inactive to SLP_S3# inactive	1	4	RTC clocks
t4	RSMRST# inactive to SLP_S5# inactive	1	4	RTC clocks
t5	RSMRST# inactive to SUS_STAT# inactive	1	4	RTC clocks
t6	SLP_S3#, SLP_S5#, SUS_STAT# inactive to Vcc3.3core good	*	*	
t7	Vcc3.3core good to CPUSLP# inactive		50	ns
t8	Vcc3.3core good to PWROK active	*	*	
t9	Vcc3.3core good to clocks valid	*	*	
t10	Clocks valid to PCIRST# inactive	500		us
t11	PWROK active to PCIRST# inactive	.9	1.1	ms
t12	PCIRST# inactive to Cycle 1 from GMCH		1	ms
t13	Cycle 1 from ICH to Cycle 2 from GMCH		60	ns
t14	PCIRST# inactive to STPCLK de-assertion	1	4	PCI clocks
t15	PCIRST# to frequency straps valid	-4	4	PCI clocks
t16	Cycle 2 from ICH to frequency straps invalid		180	ns
t17	Cycle 2 from ICH to CPURST# inactive		110	ns
t18	Stop Grant Cycle to CPUSLP# active		8	PCI clocks
t19	CPUSLP# active to SUS_STAT# active		1	RTC clock
t20	SUS_STAT# active to PCIRST# active	2	3	RTC clocks
t21	PCIRST# active to SLP_S3# active	1	2	RTC clocks
t22	PWROK inactive to Vcc3.3core not good	20		ns
t23	Wake event to SLP_S3# inactive	2	3	RTC clocks
t24	PCIRST# inactive to STPCLK# inactive	1	4	PCI clocks
t25	SLP_S3# active to SLP_S5# active	1	2	RTC clocks
t26	SLP_S5# inactive to SLP_S3# inactive	2	3	RTC clocks

NOTE: * This value is board dependent.

5

Design Checklist

Design Checklist 5

5.1 Design Review Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an Intel® 810 chipset. This is not a complete list and does guarantee that a design will function properly. Beyond the items contained in the following text, refer to the most recent version of the Design Guide for more detailed instructions on designing a motherboard.

5.1.1 Design Checklist Summary

The following tables provide design considerations for the various portions of a design. Each table describes one of those portions, and is titled accordingly. Contact your Intel Field Representative for questions or issues regarding interpretation of the information contained in these tables.

Table 5-1. AGTL+ Connectivity Checklist

CPU Pin	I/O	Comments
A[31:3]#	I/O	Terminate to V_{TT} / Connect to GMCH.
ADS#	I/O	Terminate to V_{TT} / Connect to GMCH.
BNR#	I/O	Terminate to V_{TT} / Connect to GMCH.
BP[3:2]#	I/O	Optional for Debug: Terminate to V_{TT} / Leave as No Connect.
BPM[1:0]	I/O	Optional for Debug: Terminate to V_{TT} / Leave as No Connect.
BPRI#	I	Terminate to V_{TT} / Connect to GMCH.
BR[0]#	I/O	Tie to Vss via 10–1K ohm resistor.
D[63:0]#	I/O	Terminate to V_{TT} / Connect to GMCH.
DBSY#	I/O	Terminate to V_{TT} / Connect to GMCH.
DEFER#	I	Terminate to V_{TT} / Connect to GMCH.
DRDY#	I/O	Terminate to V_{TT} / Connect to GMCH.
HIT#	I/O	Terminate to V_{TT} / Connect to GMCH.
HITM#	I/O	Terminate to V_{TT} / Connect to GMCH.
LOCK#	I/O	Terminate to V_{TT} / Connect to GMCH.
REQ[4:0]#	I/O	Terminate to V_{TT} / Connect to GMCH.
RESET#	I	Terminate to V_{TT} / 240 ohm series resistor to ITP / Connect to GMCH.
RS[2:0]#	I	Terminate to V_{TT} / Connect to GMCH.
TRDY#	I	Terminate to V_{TT} / Connect to GMCH.
RTTCTRL (S35)	I	Tie to Vss via a 110 ohm ±1% 1/16W resistor.
SLEWCTRL (E27)	I	Tie to Vss via a 110 ohm ±1% 1/16W resistor.

NOTE: All inputs should be properly terminated to an appropriate logic level.

Table 5-2. CMOS Connectivity Checklist

CPU Pin	I/O	Comments
A20M#	I	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
BSEL	O	220 ohm pull-up to 2.5V / connect to SEL0 on clock generator / 10K ohm series resistor to Display Cache MD29.
FERR#	O	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
FLUSH#	I	150 ohm 5% pull-up to VCC_{CMOS}, if unused; otherwise, refer to interface specification to meet VIH/VIL levels and undershoot/overshoot spec for the processor.
IERR#	O	150 ohm 5% pull-up to VCC_{CMOS}, if required by external logic.
IGNNE#	I	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
INIT#	I	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH / Connect to FWH.
LINT[1:0]	I	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
PICD[1:0]	I/O	150 ohm pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
PWRGOOD	I	220–450 ohm pull-up to 2.5V / Connect to PWRGOOD logic.
SLP#	I	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
SMI#	I	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
STPCLK#	I	150 ohm 5% pull-up to VCC_{CMOS} / Connect to ICH0/ICH.
THERMTRIP#	O	150 ohm 5% pull-up to VCC_{CMOS}, if required by external logic.
$VCORE_{DET}$ (E21)	I	220 ohm pull-up to 2.5V or VCC3 / connect via 10K ohm series resistor to Display Cache LMD27.

NOTE: All inputs should be properly terminated to an appropriate logic level.

Table 5-3. ITP Checklist

CPU Pin	I/O	Comments
TCK	I	150–450 ohm pullup to Vcc_{CMOS} / 47 ohm series resistor to processor.
TDI	I	150–450 ohm pullup to Vcc_{CMOS} / Connect to ITP.
TDO	O	150–450 ohm pullup to Vcc_{CMOS} / Connect to ITP.
TMS	I	150–450 ohm pullup to Vcc_{CMOS} / 47 ohm series resistor to processor.
TRST#	I	680 ohm pulldown / Connect to ITP.
PRDY#	O	Optional for Debug: Terminate to V_{TT} / 240 ohm series resistor to ITP.
PREQ#	I	150–450 ohm pullup to Vcc_{CMOS} / Connect to ITP.

NOTE: All inputs should be properly terminated to an appropriate logic level.

Table 5-4. Miscellaneous Checklist

CPU Pin	Comments
BCLK	Connect to clock generator / Gang with GMCH HCLK, 33 ohm or 45 ohm series terminator should match the series terminator on the GMCH HCLK.
CPUPRES#	If not used, tie to Vss; otherwise, pullup and connect to external logic.
EDGCTRL	Pullup to Vcc_{CORE} with 51 ohm ±5% resistor.
PICCLK	Connect to clock generator / 33 ohm series termination.
PLL1, PLL2	Capacitor across PLL1 and PLL2, with series inductor to Vcc_{CORE}. See Processor PLL decoupling guidelines for value and component requirements.
THERMDP, THERMDN	No Connect if not used; otherwise, connect to thermal sensor using vendor guidelines.
VCC_1.5	Connect to 1.5V supply.
VCC_2.5	Connect to 2.5V supply.
Vcc_{CMOS}	Use for system CMOS pullup voltage Decoupling Guidelines: 1 ea. (min) 0.1 uF in 0603 package.
Vcc_{CORE}	Connect to regulator output Decoupling Guidelines: 10 ea. (min) 4.7 uF in 1206 package / 19 ea. (min) 1.0 uF in 0805 package.
VID[3:0]	8.2K ohm (approximate) pullup resistor to 5V unless regulator implements internally.
VID[4]	Connect regulator controller pin to ground (not on processor).
V_{REF}[7:0]	Connect to V_{REF} voltage divider made up of 75 ohm and 150 ohm 1% resistors connected to V_{TT}. Decoupling Guidelines: 4 ea. (min) 0.1 uF in 0603 package.
V_{TT}	Decoupling guidelines: 14 ea. (min) 0.1 uF in 0603 package.

Table 5-5. ICH Checklist (Sheet 1 of 2)

Checklist Line Items	Comments
PME#, PWRBTN#, LAD[3:0]#/FWH[3:0]#	No external pullup resistors on those signals with integrated pullups.
SPKR	Optional strapping: Internal pullup resistor is enabled at reset for strapping; after reset, the internal pullup resistor is disabled. Otherwise, connect to motherboard speaker logic.
AC_SDOUT	Optional strapping: Internal pulldown resistor is enabled at reset for strapping. after reset, the internal pulldown resistor is disabled. Otherwise, connect to AC'97 logic.
AC_BITCLK	Internal pulldown resistor is enabled only when the AC link shut-off bit in the ICH is set. Otherwise, connect to AC'97 logic.
AC_SDIN[1:0]	Internal pulldown resistors are enabled only when the AC link shut-off bit in the ICH is set. Use 10K ohm (approximate) pulldown resistors on both signals if using AMR. For onboard AC'97 devices, use a 10K ohm (approximate) pulldown resistor on the signal that is not used. Otherwise, connect to AC'97 logic.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	No external series termination resistors on those signals with integrated series resistors.
PCIRST#	The PCIRST# signal should be buffered to the IDE connectors.
No floating inputs (including bi-directional signals):	Unused core well inputs should be tied to a valid logic level (either pulled up to 3.3V or pulled down to ground). Unused resume well inputs must be either pulled up to 3.3VSB or pulled down to ground. Ensure ALL unconnected signals are OUTPUTS ONLY!
PDD[15:0], SDD[15:0]	PDD7 and SDD7 need a 10K ohm (approximate) pulldown resistor. No other pullups/pulldowns are required. Refer to ATA ATAPI-4 specification.
PIORDY, SDIORDY	Use approximately 1K ohm pullup resistor to 5V.
PDDREQ, SDDREQ	Use approximately 5.6K ohm pulldown resistor to ground.
IRQ14, IRQ15	Need 8.2K ohm (approximate) pullup resistor to 5V.
HL11	No pullup resistor required. A test point or no-stuff resistor is needed to be able to drive the ICH into NAND tree mode for testing purposes.
VccRTC	No Clear CMOS Jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe-mode strapping for Clear CMOS.
SMBus: SMBCLK SMBDATA	The SMBus signals can be pulled up to VCC3.3 standby. Isolate any devices that are not on the same power plane as the SMBus pullups in any states where VCC3.3 standby is on and VCC3.3 is off. The value of the SMBus pullups should reflect the number of loads on the bus. For most implementations with 4–5 loads, 4.7K ohm resistors are recommended. OEMs should conduct simulation to determine exact resistor value.

Table 5-5. ICH Checklist (Sheet 2 of 2)

Checklist Line Items	Comments
APICD[0:1], APICCLK	If the APIC is used: 150 ohm (approximate) pullups on APICD[0:1] and connect APICCLK to the clock generator. If the APIC is not used: The APICCLK can either be tied to GND or connected to the clock generator, but not left floating.
ICH RTC Oscillator Circuitry:	Refer to the circuit (resistor values and capacitor values, etc.) shown in the Design Guide.
GPI[8:13]	Ensure all wake events are routed through these inputs. These are the only GPIs that can be used as ACPI compliant wake events because they are the only GPI signals in the resume well that have associated status bits in the GPE1_STS register.
HL_COMP	There are 2 options for HL_COMP: **Option 1**–RCOMP Method: Tie the COMP pin to a 40 ohm 1% or 2% (or 39 ohm 1%) pullup resistor to 1.8V via a 10 mil wide, very short (~0.5 inch) trace (targeted for a nominal trace impedance of 40 ohm). **Option 2**–ZCOMP Method: The COMP pin must be tied to a 10 mil trace that is AT LEAST 18 inches long. This trace must be un-terminated and care should be taken when routing the signal to avoid crosstalk (15–20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.
5V_REF	Refer to the most recent version of the Design Guide for implementation of the voltage sequencing circuit.
SERIRQ	Need 8.2K ohm (approximate) pullup resistor to 3.3V.
SLP_S3#, SLP_S5#	No pullups required. These signals are always driven by the ICH.
CLK66	Needs 18pF tuning capacitor as close as possible to ICH.
PCI_GNT# signals	No external pullups are required on PCI_GNT# signals. However, if external pullups are implemented, they must be pulled up to 3.3V.

Table 5-6. ICH Checklist

Checklist Line Items	Comments
GPIO27/ALERTCLK GPIO28/ALERTDATA	Add a 10K ohm pullup resistor to 3VSB (3 volt standby) on both of these signals.

Table 5-7. GMCH Checklist

Checklist Line Items	Comments
VCCDA	VCCDA needs to be connected to an isolated power plane.
HCLK, SCLK	22 pF cap to ground as close as possible to GMCH.
GTLREFA, GTLREFB	Refer to the latest design guide for the correct GTLREF generation circuit.
HUBREF	Refer to the latest design guide for the correct HUBREF generation circuit. Also, place a 0.1 uF cap as close as possible to GMCH to ground.
IWASTE	Tie to ground.
IREF	Place a resistor as close as possible to GMCH and via straight to VSS plane. A 174 ohm 1% resistor is recommended.
LTVCA, LTVDA	10K ohm (approximate) pullup resistor to 3.3V if digital video out is not implemented.
TCLK	Series resistor 22 ohm ± 2%.
OCLK/RCLK	Series resistor 33 ohm ± 2%.
LMD[27:31] Reset strapping options:	Strapping options: For a "1", use a 10K ohm (approximate) pullup resistor to 3.3V; a "0" is default (due to internal pulldown resistors). LMD31: 0 - Normal operation 1 - XOR TREE for testing purposes LMD30: 0 - Normal operation 1 - Tri-state mode for testing purposes (will tri-state all signals) LMD29: 0 - System bus frequency = 66 MHz 1 - System bus frequency = 100 MHz LMD28: The value on LMD28 sampled at the rising edge of CPURST# reflects if the IOQD (In-Order Queue Depth) is set to 1 or 4. 0 - IOQD = 4 1 - IOQD = 1 LMD27: Connect to $V_{CORE_{DET}}$ on the processor (pin E21) through a 10K ohm series resistor.
HCOMP	**Option 1**–RCOMP Method: Tie the HCOMP pin to a 40 ohm 1% or 2% (or 39 ohm 1%) pull-up resistor to 1.8V via a 10 mil wide, very short (~0.5") trace. **Option 2**–ZCOMP Method: The HCOMP pin must be tied to a 10 mil trace that is AT LEAST 18" long. This trace must be un-terminated and care should be taken when routing the signal to avoid crosstalk (15–20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

Table 5-8. System Memory Checklist

Checklist Line Items	Comments
Pin 147	Connect to Ground (since Intel® 810 chipset does not support registered DIMMs).
WP (Pin 81 on the DIMMs)	Add a 4.7K ohm pullup resistor to 3.3V. This is a recommendation to write-protect the DIMM's EEPROM.
MAA[7:4], MAB[7:4]	Add 10 ohm series resistors to the MAA[7:4], MAB[7:4] as close as possible to GMCH for signal integrity.

Table 5-9. Display Cache Checklist

Checklist Line Items	Comments
CKE	4.7K ohm pull-up resistor to VCC3.

Table 5-10. LPC Super I/O Checklist

Checklist Line Items	Comments
LPC_PME#	Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH.
LPC_SMI#	This signal can be connected to any ICH GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion.
LFRAME#	This signal is actively driven by ICH and does not require a pullup resistor.
LAD[0:3]	No additional pull-up resistors required. These signals have integrated pullups in the ICH.
LDREQ[0]#	This signal is actively driven by the Super I/O and does not require a pullup resistor.

Table 5-11. IDE Checklist

Checklist Line Items	Comments
CBLID#/PDIAG# (cable detect):	Refer to the latest design guide for the correct circuit. NOTE: All ATA66 drives will have the capability to detect cables.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	No external series termination resistors required on those signals with integrated series resistors.
IDE Reset	This signal requires a 22–47 ohm series termination resistor and should be connected to buffered PCIRST#.
PDD[15:0], SDD[15:0]	PDD7 and SDD7 need a 10K ohm (approximate) pull-down resistor to ground. Refer to ATA ATAPI-4 specification.
PIORDY, SDIORDY	Need 1K ohm (approximate) pull-up resistor to 5V.
IRQ14, IRQ15	Need 8.2K ohm to 10K ohm pull-up resistor to 5V.
PDDREQ, SDDREQ	Need 5.6K ohm (approximate) pull-down resistor to ground.
CSEL	Need 470 ohm (approximate) pull-down resistor to ground.
IDEACTP#, IDEACTS#	Can use a 10K ohm (approximate) pull-up resistor to 5V for HD LED implementation.
IOCS16#	Leave as No Connect.

Table 5-12. Clock Generator Checklist

Checklist Line Items	Comments
VDD3 Pins	Each of the following groups of pins (all belonging to VDD3) need to be on their own isolated 3.3V power plane: Group 1: VCC3 pins 2, 9, 10 and 21 Group 2: VCC3 pin 27 Group 3: VCC3 pins 33, 38 and 44 (also SEL1)
CPU	Series resistor 33 ohm ± 5%.
SDRAM/DCLK	Series resistor 22 ohm ± 5%.
3V66	Series resistor 22 ohm ± 5%.
PCI	Series resistor 33 ohm ± 5%.
48MHz	Series resistor 33 ohm ± 5%.
APIC	Series resistor 33 ohm ± 5%.
REF	Series resistor 10 ohm ± 5%.

Table 5-13. FWH Checklist

Checklist Line Items	Comments
No floating inputs.	Unused FGPI pins need to be tied to a valid logic level.
INIT#	FWH INIT# must be connected to processor INIT#.
RST#	FWH RST# must be connected to PCIRST#.
ID[3:0]	For a system with only one FWH device, tie ID[3:0] to ground.

Table 5-14. PCI Bus Checklist

Checklist Line Items	Comments
ACK64# REQ64#	(5V PCI environment) 2.7K ohm (approximate) pull-up resistors to VCC5. (3V PCI environment) 8.2K ohm (approximate) pull-up resistors to VCC3_3. Each REQ64# and ACK64# requires its own pull-up.
IDSEL lines to PCI connectors	100 ohm series resistor.
SBO# SDONE	5.6K ohm pull-up resistor to VCC3_3 or VCC5.
3Vaux	Optional to 3VSB, but required if PCI devices supporting wakeup events.

Table 5-15. USB / Keyboard / Mouse Checklist

Checklist Line Items	Comments
D-/D+ data lines	To provide nominal target trace impedance of 45 ohm, should be 9 mils wide based on the recommended stackup presented in Section 2.2, “Nominal Board Stackup” on page 2-1.
D-/D+ data lines	Use 15 ohm series resistors.
VCC USB (Cable power)	Power off 5 volt standby, if wake on USB is to be implemented, If there is adequate standby power. It should be powered off of 5 volt core instead of 5 volt standby if adequate standby power is not available.
Voltage Drop Considerations	The resistive component of the fuses, ferrite beads and traces must be considered when choosing components and Power/GND trace width. This must be done such that the resistance between the Vcc5 power supply and the host USB Port is minimized. Minimizing this resistance will minimize voltage drop seen along that path during operating conditions.
Fuse	A minimum of 1A fuse should be used. A larger fuse may be necessary to minimize the voltage drop.
Voltage Droop Considerations	Sufficient bypass capacitance should be located near the host USB receptacles to minimize the voltage droop that occurs upon the hot attach of a new device. See the most recent version of the USB specification for more information.

Table 5-16. AC’97 Checklist (Sheet 1 of 2)

Checklist Line Items	Comments
AC_SDIN[1:0]	AC_SDIN[0] is recommended to be used for an onboard audio codec. Only one primary codec can be present on the link. A maximum of two active codecs are supported in an ICH platform. The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10K ohm) pull-down resistor (See Section 2.10, “AC’97” on page 2-24 for more information).
PRI_DN#	If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground. The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
AC-link	Components such as FET switches, buffers, or logic gates, should not be implemented on the AC-link signals, except AC_RST#, without doing thorough simulation and analysis. Doing so will potentially interfere with timing margins and signal integrity A means of preventing contention on the AC-link must be provided for an onboard codec if the motherboard requires that an AMR module with a primary codec take precedence over an onboard primary codec.
AUDIO_MUTE#:	No connect on the motherboard.
AUDIO_PWRDN	Codecs on the AMR card should implement the EAPD powerdown pin, per the AC’97 2.1 specification, to control the amplifier.
MONO_PHONE	Connect to onboard audio codec if supported.
MONO_OUT/ PC_BEEP	Connect to SPKR output from ICH or MONO_OUT from onboard codec.
PRIMARY_DN#	See discussion above.

Table 5-16. AC'97 Checklist (Sheet 2 of 2)

Checklist Line Items	Comments
+5VDUAL/+5VSB	If an adequate power supply is available, this pin should be connected to +5Vdual or +5Vsby. In the event that these planes cannot support the required power, it can be connected to VCC5 core on the motherboard. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
S/P-DIF_IN	Connect to ground on the motherboard.
AC_SDIN[3:2]	No connect on the motherboard. The ICH supports a maximum of two codecs, which should be attached to SDIN[1:0].
AC97_MSTRCLK	Connect to ground on the motherboard.
PC_BEEP	Should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

Table 5-17. Power Delivery Checklist

Checklist Line Items	Comments
All voltage regulator components meet maximum current requirements	Consider all loads on a regulator, including other regulators.
All regulator components meet thermal requirements	Ensure the voltage regulator components and dissipate the required amount of heat.
If devices are powered directly from a dual rail (i.e., not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET.	"Dual" voltage rails may not be at the expected voltage.
Dropout Voltage	The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage.
Voltage tolerance requirements are met	See individual component specification for each voltage tolerance.
Total power consumption in S3 must be less than the rated standby supply current.	Adequate power must be supplied by power supply.

5.2 Pullup and Pulldown Resistor Values

Pullup and pulldown values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pullup voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pullup voltage tolerance, the pullup/pulldown resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum/maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications and other considerations.

A simplistic DC calculation for a pullup value is:

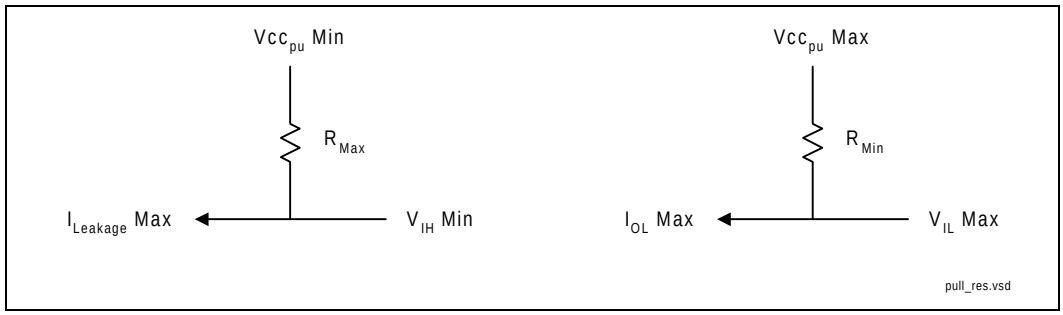
$$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{LEAKAGE}\ MAX$$

$$R_{MIN} = (Vcc_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$$

Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} is also determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including input capacitance of the devices to be driven, output capacitance of the driver, and line capacitance. This calculation yields the largest pullup resistor allowable to meet the rise time t.

$$R_{MAX} = -t / (C * \ln(1-(V_{IH}\ MIN / Vcc_{PU}\ MIN)))$$

Figure 5-1. Pullup Resistor Example



5.3 RTC

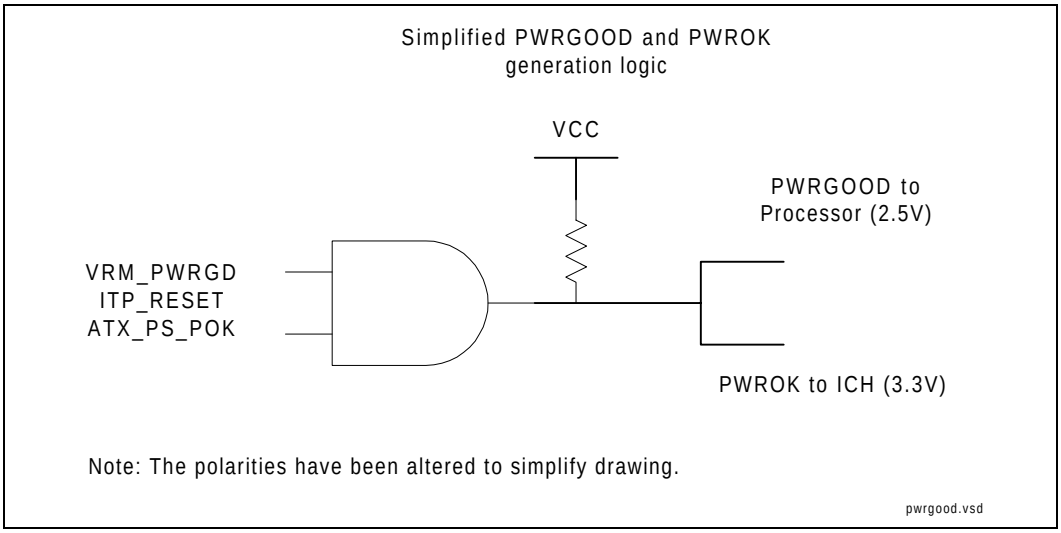
Guidelines to minimize ESD events that may cause loss of CMOS contents:

- Provide a 1 uF 805 X5R dielectric, monolithic, ceramic capacitor on the VCCRTC pin. This capacitor connection should not be stubbed off the trace run and should be as close as possible to the ICH. If a stub is required, it should be kept to a few mm maximum length. The ground connection should be made through a via to the plane with no trace between the capacitor pad and the via.
- Place the battery, 1K ohm series current limit resistor, and the common-cathode isolation diode very close to the ICH. If this is not possible, place the common-cathode diode and the 1K ohm resistor as close to the 1 µF cap as possible. Do not place these components between the cap and the ICH. The battery can be placed remotely from the ICH.
- On boards that have chassis-intrusion utilizing inverters powered by the VCCRTC pin, place the inverters as close to the common-cathode diode as possible. If this is not possible, keep the trace run near the center of the board.
- Keep the ICH VCCRTC trace away from the board edge. If this trace must run from opposite ends of the board, keep the trace run towards the board center, away from the board edge where contact could be made by those handling the board.

5.4 Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH integrates 16 msec debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity, and not be connected directly to logic on the board.
- PS_POK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, making sure that the input to the ICH is at a 3V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- It is recommended that 3.3V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 msec.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to CPU is driven with an open collector buffer pulled up to 2.5V using a 330 ohm resistor.
- The circuitry checks for both processor VRM powered up, and the PS_POK signal from the ATX power supply connector before asserting PWRGOOD and PWROK to the processor and ICH.

Figure 5-2. PWRGOOD & PWROK Logic



- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.

- SLP_S3# from the ICH must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

5.4.1 Power Button Implementation

The items below should be considered when implementing a power management model for a desktop system. The power states are as follows:

S1–Stop Grant – (CPU context not lost)

S3–STR (Suspend To RAM)

S4–STD (Suspend To Disk)

S5–Soft-off

- Wake: Pressing the power button wakes the computer from S1–S5.
- Sleep: Pressing the power button signals software/firmware in the following manner:
  - — If SCI is enabled, the power button will generate an SCI to the OS.
    - The OS will implement the power button policy to allow orderly shutdowns.
    - Do not override this with additional hardware.
  - — If SCI is not enabled:
    - Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
    - Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
    - Always install an SMI handler for the power button that operates until ACPI is enabled.
  - — Emergency Override: Pressing the power button for 4 seconds goes directly to S5.
    - This is only to be used in EMERGENCIES when system is not responding.
    - This will cause the user data to be lost in most cases.
    - Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off; this violates ACPI.
- To be compliant with the latest PC9x specification, machines must appear off to the user when in the S1–S4 sleeping states. This includes:
  - — All lights except a power state light must be off.
  - — The system must be inaudible: silent or stopped fan; drives are off.

Note: Contact Microsoft* for the latest information concerning PC9x and Microsoft* Logo programs.

6

Flexible Motherboard Guidelines

Flexible Motherboard Guidelines 6

6.1 Flexible Processor Guidelines

6.1.1 Flexible System Design DC Guidelines

The processor DC guidelines for flexible system designed in this section are defined at the processor pin.

Table 6-1 lists the guidelines for future 1.5V processors and Table 6-2 lists the guidelines for future 2.0V processors. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 6-1. Flexible Processor Voltage and Current Guidelines for 1.5V Processors

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Vcc_{CORE}	V_{CC} for processor core		1.5		V	1, 3
Baseboard Tolerance, Static	processor core voltage static tolerance at processor pins	–0.070		0.070	V	2, 3
Baseboard Tolerance, Transient	processor core voltage transient tolerance level at processor pins	–0.110		0.110	V	2, 3
I_{CCCORE}	I_{CC} for processor core			12.6	A	1, 4, 5, 7
I_{SGnt}	I_{CC} Stop-Grant for processor core			0.8	A	6
dI_{CCCORE}/dt	Power supply current slew rate			240	A/µS	8, 9

NOTES:
1. Vcc_{CORE} and Icc_{CORE} supply the processor core.
2. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
3. These are the tolerance requirements, across a 20 MHz bandwidth at the processor pin at the bottom side of the system platform. Vcc_{CORE} must return to within the static voltage specification within 100 us after a transient event; see the VRM 8.4 DC-DC Converter Specification for further details.
4. Max ICC measurements are measured at Vcc max. voltage, under maximum signal loading conditions.
5. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of Vcc_{CORE} (Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

   $$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE}\ \text{Tolerance, Transient})$$

6. The current specified is also for AutoHALT state.
7. Maximum values are specified by design/characterization at maximum Vcc_{CORE}.
8. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
9. dICC/dt specifications are specified at the processor pins.

Table 6-2. Flexible Processor Voltage and Current Guidelines for 2.0 V Processors [1]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Vcc_{CORE}	V_{CC} for processor core		2.00		V	1, 3
Baseboard Tolerance, Static	processor core voltage static tolerance at processor pins	–0.089		0.100	V	2, 3
Baseboard Tolerance, Transient	processor core voltage transient tolerance level at processor pins	–0.144		0.144	V	2, 3
I_{CCCORE}	I_{CC} for processor core			15.6	A	1, 4, 5, 7
I_{SGnt}	I_{CC} Stop-Grant for processor core			0.8	A	6
dI_{CCCORE}/dt	Power supply current slew rate			240	A/µS	8, 9

NOTES:

1. Vcc_{CORE} and Icc_{CORE} supply the processor core.
2. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
3. These are the tolerance requirements, across a 20 MHz bandwidth at the top of the PPGA package. Vcc_{CORE} must return to within the static voltage specification within 100 us after a transient event; see the VRM 8.4 DC-DC Converter Specification for further details.
4. Max ICC measurements are measured at Vcc max. voltage, under maximum signal loading conditions.
5. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e. typical) voltage level of Vcc_{CORE} (Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

   $$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times Vcc_{CORE\_TYP} / (Vcc_{CORE\_TYP} + Vcc_{CORE}\ \text{Tolerance, Transient})$$

6. The current specified is also for AutoHALT state.
7. Maximum values are specified by design/characterization at maximum Vcc_{CORE}.
8. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
9. dICC/dt specifications are specified at the processor pins.

6.1.2 System Bus AC Guidelines

Table 6-3 and Table 6-4 contain 66 MHz and 100 MHz system bus AC Guidelines defined at the processor pins.

Table 6-3 contains the BCLK guidelines and Table 6-4 contains the AGTL+ system bus guidelines. Processor System Bus AC Specifications for the AGTL+ Signal Group at the processor pins for 100 MHz are equivalent to 66 MHz. The 66 MHz specification is documented in the processor datasheet.

Table 6-3. Flexible Motherboard Processor System Bus AC Guidelines (Clock) at the Processor Pins [1,2,3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency			66.67 100.00	MHz MHz		All processor core frequencies
T1: BCLK Period	15.0 10.0			ns ns	6-1 6-1	4, 5, 9 4, 6, 9
T2: BCLK Period Stability			±300 ±250	ps ps	6-1 6-1	5, 7, 8, 9 6, 7, 8, 9
T3: BCLK High Time	4.94 2.5			ns	6-1	@>2.0V [5] @>2.0V [6]
T4: BCLK Low Time	4.94 2.4			ns	6-1	@<0.5V [5] @<0.5V [6]
T5: BCLK Rise Time	0.34 0.38		1.5 1.36	ns ns	6-1 6-1	(0.5V–2.0V) [5, 11] (0.5V–2.0V) [6, 11]
T6: BCLK Fall Time	0.34 0.38		1.5 1.36	ns ns	6-1 6-1	(2.0V–0.5V) [5, 11] (2.0V–0.5V) [6, 11]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25V at the processor core pins.
4. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
5. This specification applies to the processor when operating with a system bus frequency of 66 MHz.
6. This specification applies to the processor when operating with a system bus frequency of 100 MHz.
7. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
8. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 KHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
9. The average period over a 1uS period of time must be greater than the minimum specified period.

Figure 6-1. BCLK Waveform

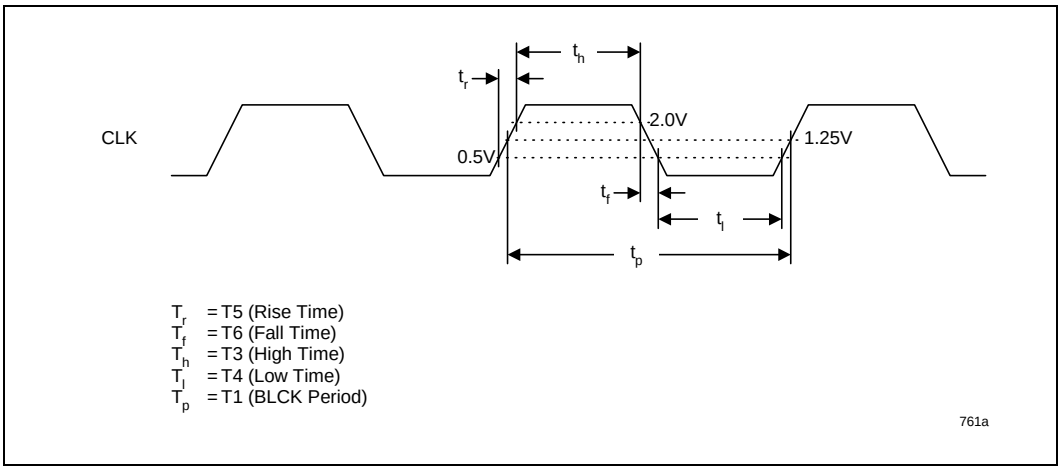


Table 6-4. Processor System Bus AC Guidelines (AGTL+ Signal Group) at the Processor Pins [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.30	4.43	ns	6-2	5
T8: AGTL+ Input Setup Time	1.75		ns	6-3	5, 6, 7, 8
T9: AGTL+ Input Hold Time	0.85		ns	6-3	9
T10: RESET# Pulse Width	1.00		ms	6-4	7, 10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00V at the processor pins.
4. This specification applies to the processor operating with a 66 MHz or 100 MHz system bus.
5. Valid delay timings for these signals are specified into 25 ohm to 1.5V and with V_{REF} at 1.0V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40V swing.
9. Specification is for a maximum 1.0V swing.
10. After Vcc_{CORE} and BCLK become stable.

Figure 6-2. Processor System Bus Valid Delay Timings

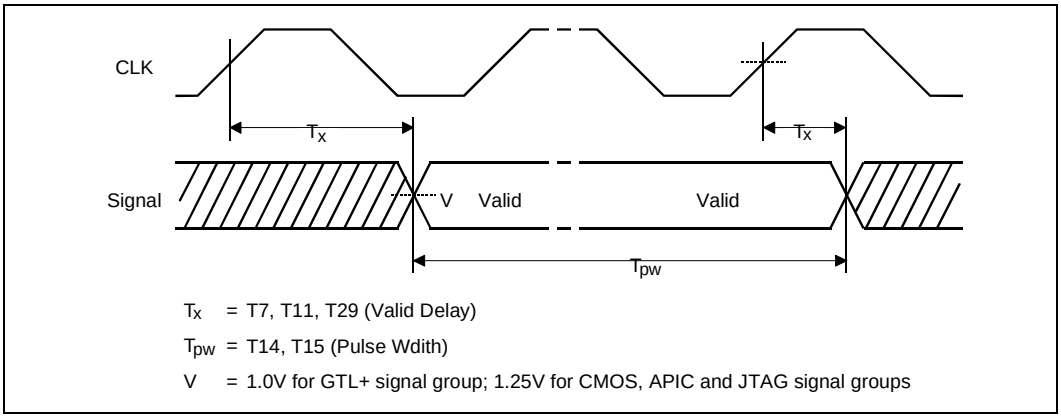


Figure 6-3. Processor System Bus Setup and Hold Timings

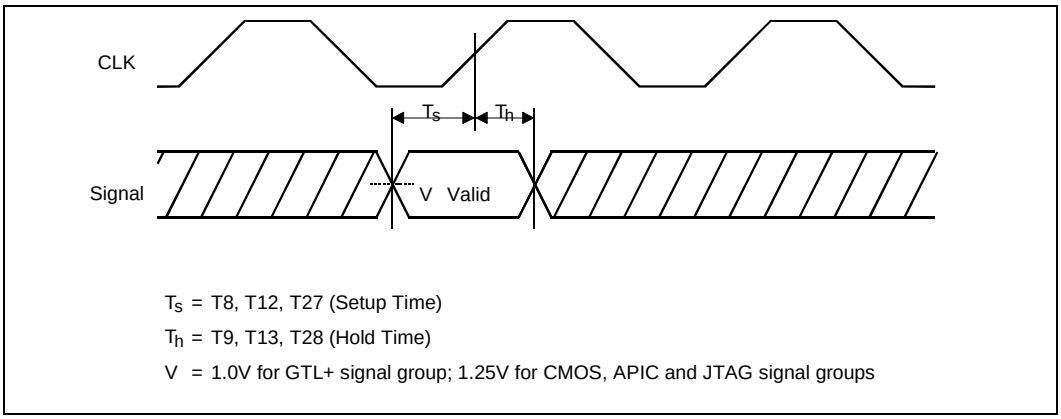
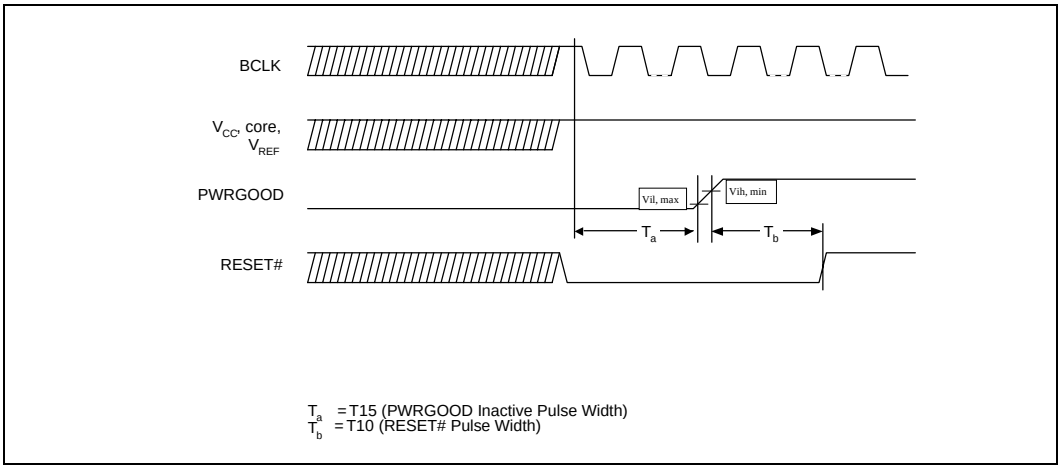


Figure 6-4. Power-On Reset and Configuration Timings



6.1.3 Thermal Guidelines

Table 6-5 provides the recommended thermal design power dissipation for use in designing a flexible system board. The processor's heatslug is the attach location for all thermal solutions. The maximum and minimum case temperatures are specified in Table 6-5. A thermal solution should be designed to ensure the temperature of the case never exceeds these specifications.

Table 6-5. Intel® Celeron™ Processor PPGA Flexible Thermal Design Power [1, 2]

Processor Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)
30.0[2]	0	70

NOTES:
1. These values are specified at nominal Vcc_{CORE} for the processor core.
2. These values are preliminary.

6.2 Flexible Chipset Guidelines

6.2.1 82801AB (ICH0)/82801AA (ICH) Scalability

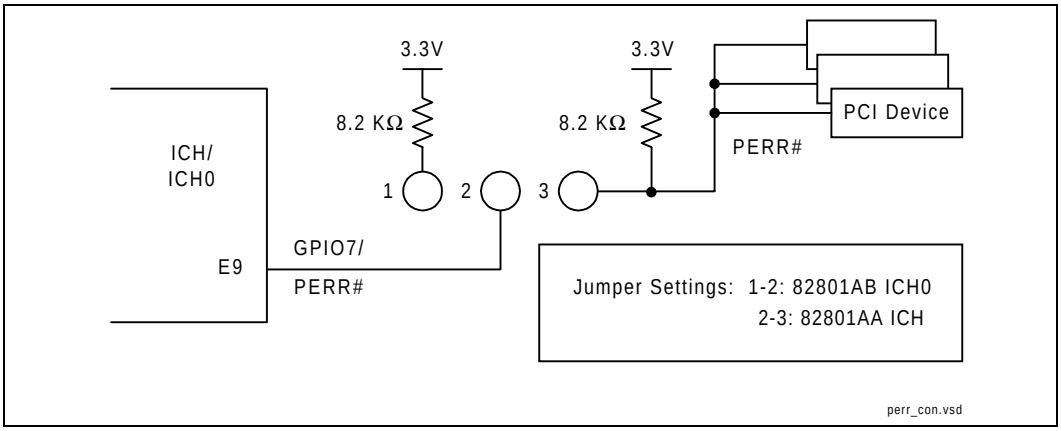
While the 82801AB (ICH0) and 82801AA (ICH) are pin compatible, there are some signal implementation differences. The signals that have different implementation and need considerations in 82801AB (ICH0) and 82801AA (ICH) are PERR#, REQ[4:5]#/GNT[4:5]#, SUSCLK, ALERTCLK and ALERTDATA. The following sections consider possible ways to connect those signals for a scaleable motherboard to support both 82801AB (ICH0) and 82801AA (ICH).

6.2.1.1 PCI PERR# (Ball Position E9)

For the 82801AA (ICH), PERR# is multiplexed with GPI7. For the 82801AB (ICH0), PERR# is not available.

Case 1: If the system designer decides to support PERR# on a scaleable motherboard, the connection of PERR# in this case is illustrated in Figure 6-5. Note that jumper implementation is needed to select the system configuration.

Figure 6-5. PERR# Connection



Case 2: If the system designer chooses not to support PERR# on a scaleable motherboard, GPIO7/PERR# is available as a GPIO and can be used as needed. In this case, the jumper shown in Figure 6-5 may not be needed. If the GPIO is not used, there should be a pull-up resistor on it. Also, PERR# on PCI devices should be connected together and pulled up to Vcc.

6.2.1.2 PCI REQ[4]#/GNT[4]# Pair (Ball Position B11/A11)

For the 82801AA (ICH), PCI REQ[4]#/GNT[4]# are the 5th PCI REQ/GNT pair.

For the 82801AB (ICH0), the PCI REQ[4]#/GNT[4]# pair is not available. Even when REQ[4]# is driven active (low), the 82801AB (ICH0) will not treat it as being active; GNT[4]# signal is always high during S0 and S1 states, and not driven during S3-S5 states. Therefore, if the system designer chooses to use the PCI REQ[4]#/GNT[4]# pair for a PCI device on a scaleable motherboard, the REQ/GNT pair can be connected to the PCI device like any other PCI REQ/GNT pair. However, this PCI device will be disabled when the 82801AB (ICH0) is used instead of the 82801AA (ICH).

6.2.1.3 PCI REQ[5]#/GNT[5]# Pair (Ball Position P4/R5)

For the 82801AA (ICH), PCI REQ[5]#/GNT[5]# are the 6th PCI REQ/GNT pair. REQ[5]# is multiplexed with GPIO1 and PC/PCI REQ[B]#; GNT[5]# is multiplexed with GPIO17 and PC/PCI GNT[B]#.

For the 82801AB (ICH0), the PCI REQ[5]#/GNT[5]# pair is not implemented.

If the system designer chooses to use the PCI REQ[5]#/GNT[5]# pair for a PCI device on a scaleable motherboard, the REQ/GNT pair can be connected to the PCI device like any other PCI REQ/GNT pairs. However, this PCI device will be disabled when the 82801AB (ICH0) is used instead of the 82801AA (ICH).

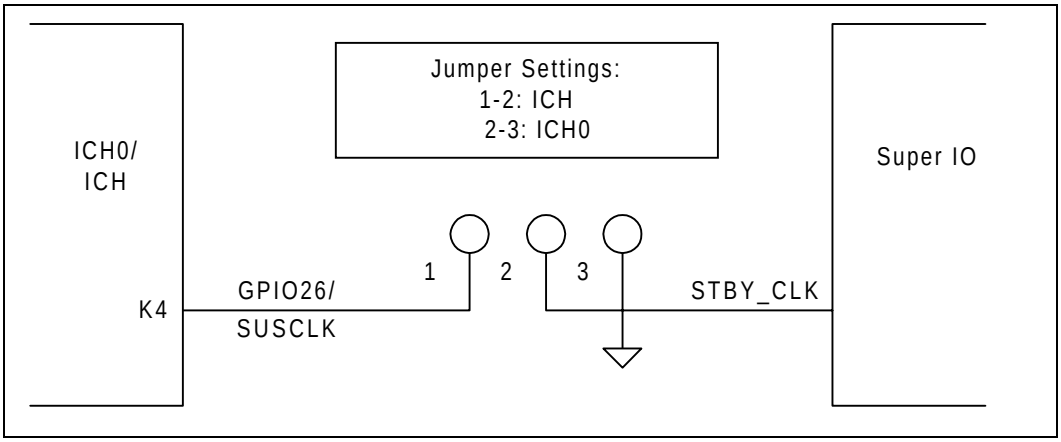
6.2.1.4 SUSCLK (Ball Position K4)

For the 92901AA (ICH), SUSCLK is multiplexed with GPIO26. For the 92901AB (ICH0), SUSCLK is not implemented.

Case 1: If the system designer decides to support wake from S3 on mouse or keyboard on a scaleable motherboard, a possible connection of SUSCLK is illustrated in Figure 6-6. A jumper is needed in this case to select the system configuration.

Note that the illustration is based on an SMC LPC SIO that has a standby clock for wake up events and the standby clock needs to be pulled to ground, if not used. Other vendors' SIO may have different implementation or requirements on the clock scheme for supporting wake from S3 on mouse or keyboard. In other words, the connection for SUSCLK on a scaleable motherboard is SIO dependent.

Figure 6-6. SUSCLK Connection



Case 2: If the system designer chooses not to support wake from S3 on mouse or keyboard on a scaleable motherboard, GPIO26/SUSCLK is available as a GPIO, and can be used as needed. If the GPIO is not used, it can be left as a no connect. The STBY_CLK in the SIO part needs to be treated per the SIO specification when not used.

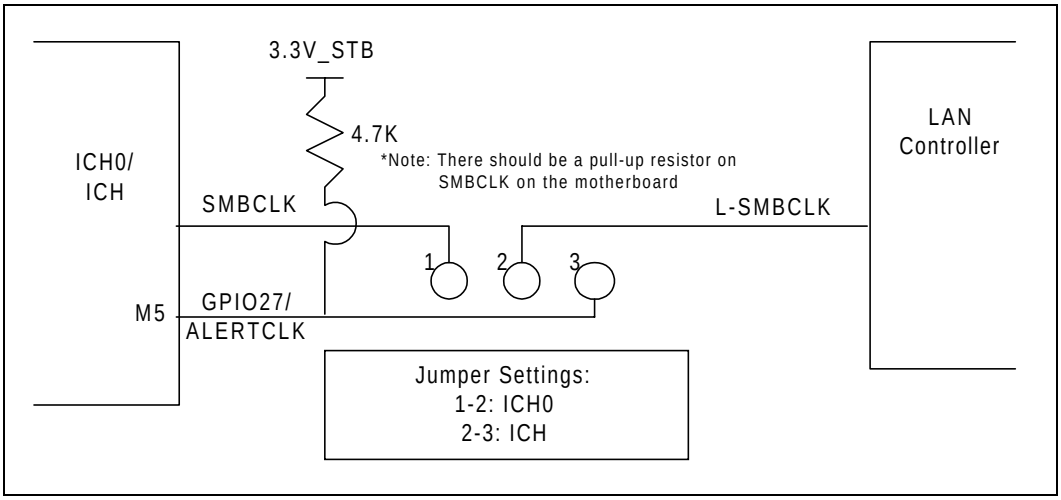
6.2.1.5 ALERTCLK/ALERTDATA (Ball Position M5/L5)

The 82801AA (ICH) supports Alert-On-Lan (AOL) through ALERTCLK and ALERTDATA, which are multiplexed with GPIO27 and GPIO28.

The 82801AB (ICH0) does not implement ALERTCLK/ALERTDATA.

If the system designer decides to support AOL on a scaleable motherboard, the suggested connection is shown in Figure 6-7. Note that the figure illustrates the connection of GPIO27/ ALERTCLK (and SMBCLK). The same connection will be used for GPIO28/ALERTDATA (and SMBDATA).

Figure 6-7. GPIO27/ALERTCLK Connection



6.2.1.6 ATA33/ATA66 Scalability

The 82801AA (ICH) supports Ultra ATA/66, while the 82801AB (ICH0) supports Ultra ATA/33 only. Although Ultra ATA/33 and ATA/66 devices use the same type of connector, the ATA/66 drives do require new cables and method for the system BIOS to detect the new cables. Refer to Section 2.9.2, “Ultra ATA/66 Detection (82801AA ICH only)” on page 2-21 for IDE cable detection methods.

7

Third Party

Third-Party Vendor Information 7

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the Intel® 810 Chipset. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

Table 7-1. Super I/O

Vendors	Contact	Phone
SMC	Dave Jenoff	(909) 244-4937
National	Robert Reneau	(408) 721-2981
ITE	Don Gardenhire	(512)388-7880
Winbond	James Chen	(02) 27190505 - Taipei office

Table 7-2. Clock Generation

Vendors	Contact	Phone
Cypress	John Wunner	206-821-9202 x325
ICS	Raju Shah	408-925-9493
IC Works	Jeff Keip	408-922-0202, x1185
IMI	Elie Ayache	408-263-6300, x235
PERICOM	Ken Buntaran	408-435-1000

Table 7-3. Memory Vendors

http://developer.intel.com/design/motherbd/se/se_mem.htm

Table 7-4. Voltage Regulator Vendors

Vendors	Contact	Phone
Linear Tech Corp.	Stuewart Washino	408-432-6326
Celestica	Dariusz Basarab	416-448-5841
Corsair Microsystems	John Beekley	888-222-4346
Delta Electronics	Colin Weng	886-2-6988, x233(Taiwan)
N. America: Delta Products Corp.	Maurice Lee	510-770-0660, x111

Table 7-5. Flat Panel

Vendors	Contact	Phone
Silicon Images Inc	John Nelson	408-873-3111

Table 7-6. AC'97

Vendors	Contact	Phone
Analog Devices	Dave Babicz	781-461-3237
AKM	George Hill	408-436-8580
Cirrus Logic (Crystal)	David Crowell	512-912-3587
Creative Technologies Ltd./ Ensoniq Corp.	Steve Erickson	408-428-6600 x6945
Diamond Multimedia Systems	Theresa Leonard	360-604-1478
ESS Technology	Bill Windsor	510-492-1708
Euphonics, Inc.	David Taylor	408-554-7201
IC Ensemble Inc.	Steve Allen	408-969-0888 x106
Motorola	Pat Casey	508-261-4649
PCTel, Inc.	Steve Manuel	410-965-2172
Conexant (formerly Rockwell)	Tom Eichenberg	949-221-4164
SigmaTel	Spence Jackson Arron Lyman	512-343-6636 512-343-6636 x11
Staccato Systems	Bob Starr	650-853-7035
Tritech Microelectronics, Inc.	Rod Maier	408-941-1360
Yamaha	Jose Villafuerte (US) Kazunari Fukaya (Japan)	408-467-2300 (0539) 62-6081

A

PCI Devices/Functions/ Registers/Interrupts

PCI Devices/Functions/Registers/ Interrupts A

Table A-1. PCI Devices and Functions

Device	Function	Function Description
82801AB (ICH0)		
Device 30	Function 0	Intel® 82801AB PCI Bridge
Device 31	Function 0	Intel® 82801AB LPC Bridge
Device 31	Function 1	Intel® 82801AB Bus Master IDE Controller
Device 31	Function 2	Intel® 82801AB USB Universal Host Controller
Device 31	Function 3	Intel® 82801AB SMBus Controller
Device 31	Function 4	Reserved
Device 31	Function 5	Intel® 82801AB AC'97 Audio Controller
Device 31	Function 6	Intel® 82801AB AC'97 Modem Controller
Device 31	Function 7	Reserved
82801AA (ICH)		
Device 30	Function 0	Intel® 82801AA PCI Bridge
Device 31	Function 0	Intel® 82801AA LPC Bridge
Device 31	Function 1	Intel® 82801AA Bus Master IDE Controller
Device 31	Function 2	Intel® 82801AA USB Universal Host Controller
Device 31	Function 3	Intel® 82801AA SMBus Controller
Device 31	Function 4	Reserved
Device 31	Function 5	Intel® 82801AA AC'97 Audio Controller
Device 31	Function 6	Intel® 82801AA AC'97 Modem Controller
Device 31	Function 7	Reserved
82810 GMCH		
Device 0	Function 0	Intel® 82810 System and Memory Controller
Device 1	Function 0	Intel® 82810 Internal Graphics Device
82810-DC100 GMCH		
Device 0	Function 0	Intel® 82810 System and Memory Controller
Device 1	Function 0	Intel® 82810 Internal Graphics Device

Table A-2. PCI Devices and Registers

Function Description	Vendor ID Register	Device ID Register	Revision ID Register	Class Code Register	Sub-Class Register	Program Interface Register
82801AB (ICH0)						
PCI Bridge	8086h	0x2428	Note 1	06h	04h	00h
LPC Bridge	8086h	0x2420	Note 1	06h	01h	00h
Bus Master IDE Controller	8086h	0x2421	Note 1	01h	01h	80h
USB Universal Host Controller	8086h	0x2422	Note 1	0Ch	03h	00h
SMBus Controller	8086h	0x2423	Note 1	0Ch	05h	00h
AC'97 Audio Controller	8086h	0x2425	Note 1	04h	01h	00h
AC'97 Modem Controller	8086h	0x2426	Note 1	04h	01h	00h
82801AA (ICH)						
PCI Bridge	8086h	0x2418	Note 1	06h	04h	00h
LPC Bridge	8086h	0x2410	Note 1	06h	01h	00h
Bus Master IDE Controller	8086h	0x2411	Note 1	01h	01h	80h
USB Universal Host Controller	8086h	0x2412	Note 1	0Ch	03h	00h
SMBus Controller	8086h	0x2413	Note 1	0Ch	05h	00h
AC'97 Audio Controller	8086h	0x2415	Note 1	04h	01h	00h
AC'97 Modem Controller	8086h	0x2416	Note 1	04h	01h	00h
82810 GMCH						
System and Memory Controller	8086h	0x7120	Note 1	06h	00h	00h
Internal Graphics Device	8086h	0x7121	Note 1	03h	00h	00h
82810-DC100						
System and Memory Controller	8086h	0x7122	Note 1	06h	00h	00h
Internal Graphics Device	8086h	0x7123	Note 1	03h	00h	00h

NOTES:
1. See Specification Update document for the particular product.

Table A-3. PCI Devices and Interrupts

Function Description	APIC Interrupt	ISA/PCI IRQ
82801AB (ICH0)		
Intel® 82801AB PCI Bridge	N/A	N/A
Intel® 82801AB LPC Bridge	N/A	N/A
Intel® 82801AB Bus Master IDE Controller	Interrupt 14	IRQ14
Intel® 82801AB USB Universal Host Controller	Interrupt 18	PIRQC#
Intel® 82801AB SMBus Controller	Interrupt 17	PIRQB#
Reserved	N/A	N/A
Intel® 82801AB AC'97 Audio Controller	Interrupt 17	PIRQB#
Intel® 82801AB AC'97 Modem Controller	Interrupt 17	PIRQB#
Reserved	N/A	N/A
82801AA (ICH)		
Intel® 82801AA PCI Bridge	N/A	N/A
Intel® 82801AA LPC Bridge	N/A	N/A
Intel® 82801AA Bus Master IDE Controller	Interrupt 14	IRQ14
Intel® 82801AA USB Universal Host Controller	Interrupt 18	PIRQC#
Intel® 82801AA SMBus Controller	Interrupt 17	PIRQB#
Reserved	N/A	N/A
Intel® 82801AA AC'97 Audio Controller	Interrupt 17	PIRQB#
Intel® 82801AA AC'97 Modem Controller	Interrupt 17	PIRQB#
Reserved	N/A	N/A
82810 GMCH0		
Intel® 82810 System and Memory Controller	N/A	N/A
Intel® 82810 Internal Graphics Device	Interrupt 16	PIRQA#
82810-DC100 (GMCH)		
Intel® 82810-DC100 System and Memory Controller	N/A	N/A
Intel® 82810-DC100 Internal Graphics Device	Interrupt 16	PIRQA#

B

Bill-Of-Materials (BOM)

Bill-of-Materials (BOM) B

Table B-4. Bill-of-Materials

QTY	REFERENCE DESIGNATION	DESCRIPTION	PACKAGE	MFG.	MFG'S PART NUMBER
1	N/A	BATTERY	BAT	PANASONIC	CR2032
2	C75,C174	Cap.,47 uf,16vdc,Tant.	SM7343	Kemet	T491D476K016AS
151	C166,C216,C294,C211,C259, C361,C355,C353,C36,C287, C361,C355,C353,C36,C287, C246,C335,C342,C12,C1, C266,C213,C268,C324,C378, C267,C284,C337,C336,C33, C34,C129,C11,C32,C133, C144,C150,C65,C206,C39, C38,C52,C47,C61,C63, C22,C147,C261,C184,C19, C165,C241,C302,C297,C229, C279,C209,C204,C207,C9, C157,C218,C220,C219,C381, C169,C262,C295,C296,C307, C319,C10,C345,C171,C303, C263,C350,C341,C343,C234, C278,C288,C244,C243,C130, C232,C247,C239,C382,C223, C249,C252,C251,C215,C175, C181,C254,C248,C245,C260, C163,C77,C253,C170,C73, C265,C323,C317,C367,C321, C23,C363,C365,C362,C50, C205,C221,C42,C6,C334, C180,C257,C212,C377, C227,C67,C82,C83, C86,C87,C66,C72,C360, C333,C81,C80,C352,C298, C283,C291,C354,C285,C339, C160,C250,C78,C340,C318, C172,C376,C320,C240,C256, C127,C338,C322	Cap., 0.1 uf, 16vdc, X7R	SM0603	Kemet	C0603C104K4RAC
9	C168,C238,C331,C269,C293, C236,C114,C161,C379	Cap.,22 pf,50vdc,C0G	SM0603	Kemet	C0603C220K5GAC
12	C158,C48,C55,C71, C162,C188,C74,C85,C70, C69,C62,C84	Cap.,22 uf,16vdc,Tant.	SM7343	Kemet	T491D226K016AS
27	C217,C17,C199,C198,C191, C195,C20,C308,C332,C304, C41,C203,C380,C383,C228, C131,C164,C242,C237,C214, C233,C305,C289, C169, C170, C262, C377	Cap., 0.01 uf, 16vdc, X7R	SM0603	Kemet	C0603C103K4RAC
4	C366,C346,C51,C49	Cap.,12 pf, 50vdc, C0G, ±5%	SM0603	Kemet	C0603C120J5GAC
34	C349,C290,C264,C370,C121, C142,C118,C113,C120,C156, C154,C107,C145,C149,C138, C137,C132,C135,C148,C134, C143,C141,C108,C151,C57, C43,C21,C301,C344,C351, C274,C224,C374,C183	Cap.,1.0uf,50vdc,X7R	SM1210	Kemet	C1210C105K5RAC
15	C373,C258,C14,C15,C5, C2,C3,C4,C210,C356, C371,C177,C176,C300,C299	Cap.,470pf,16vdc,X7R	SM0603	Kemet	C0603C471K4RAC
12	C358,C348,C357,C359,C179, C178,C79,C182,C16,C13, C8,C98	Cap.,47pf,50vdc,C0G	SM0603	Kemet	C0603C470K5GAC
2	C202,C201	Cap., 68 uf,16vdc,Tant.	SM7343	Kemet	T491D686K016AS

Table B-4. Bill-of-Materials

QTY	REFERENCE DESIGNATION	DESCRIPTION	PACKAGE	MFG.	MFG'S PART NUMBER
8	C124,C167,C37,C53,C46, C64,C60,C40	Cap.,0.001 uf,16vdc,X7R	SM0603	Kemet	C0603C102K4RAC
17	C91,C197,C196,C194,C193, C192, C190,C189,C97,C96,C94,C92, C90,C88,C89,C93,C95	Cap.,180 pf,16vdc,X7R	SM0603	Kemet	C0603C181K4RAC
24	C325,C326,C327,C328,C329, C330,C369,C368,C275,C276, C277,C272,C271,C231,C280, C310,C311,C309,C315,C313, C314,C316,C312,C226	Cap.,100 pf,50vdc,C0G	SM0603	Kemet	C0603C101K5GAC
10	C109,C111,C106,C105,C104, C103,C122,C119,C102,C100	Cap.,3.3 pf,50vdc,C0G	SM0603	Kemet	C0603C339K5GAC
5	C76,C270,C225,C159,C59	Cap., 100 uf, 16vdc, Tant.,0.1ESR	SM7343	Kemet	T495D107K010AS 4823
1	C45	Cap.,0.01 uf,16vdc,X7R	SM0603	Kemet	C0603C103K4RAC
10	C185,C27,C292,C281,C44,C282,C230,C200,C273,C286	Cap., 10 uf, 16vdc, Tant.	SM6032	Kemet	T491C106K016AS
12	C136,C117,C110,C115,C153, C146,C126,C139,C155,C140, C125,C152	Cap.,4.7 uf,X5R	SM1206	muRata	GRM42-6X5R475K
3	C56,C68,C255	Cap.,4.7 uf,16vdc,Tant.	SM3528	Kemet	T491B475K016AS
1	C187,C186	Cap.,0.047 uf,16vdc,X7R	SM0603	Kemet	C0603C473K4RAC
1	C347	Cap., 2200 pf,16vdc,X7R	SM0603	Kemet	C0603C222K4RAC
1	C35	Cap.,220 pf,16vdc,X7R	SM0603	Kemet	C0603C221K4RAC
6	C29,C7,C26,C30,C173,C375	Cap.,1200 uf,10vdc,Tant., Low ESR	T.H. (radial)	Sanyo	10MV1200GX
5	C54,C128,C28,C58,C31	Cap.,2700 uf,10vdc,Tant., Low ESR	T.H. (radial)	Sanyo	10MV2700GX
1	C18	Cap.,150 pf,50vdc,C0G	SM0603	Kemet	C0603C151K5GAC
4	C116,C101,C112,C208	Cap.,10 pf,50vdc,C0G	SM0603	Kemet	C0603C100K5GAC
2	C25,C24	Cap.,1.0 uf,50vdc,X7R	SM1812	Kemet	C1812C105K5RAC
5	C364,C99,C306,C235,C372	Cap.,2.2 uf,16vdc,Tant.	SM3216	Kemet	T491A225K016AS
1	CR2	Diode,Schottky,3A	DO-201AD	Fairchild	1N5822
5	CR10,CR9,CR8,CR6,CR5	Diode,dual,schottky,S config.	SOT-23	Philips	BAT54S
2	CR1,CR4	Diode,Highspeed	SOD-27(DO-35)	Philips	1N4148
3	CR14,CR13,CR11	Diode, schottky	SOT-23	Philips	BAT17
1	CR15	Diode,dual,schottky, C config.	SOT-23	Philips	BAT54C
1	CR7	Diode,1N5821	DO-201AD	Fairchild	1N5821
1	CR12	LED,RED,Diffused	T.H.	Liteon	LTL-4266N
1	CR3	LED,Bi-Color,Red/Grn, Non-tinted,Diffused	T.H.	Liteon	LTL-14CHJ
1	F3	Fuse,Polyswitch,2.5A	T.H.	Raychem	RUSB250
1	F2	Fuse,Polyswitch,1.25A@ $20^{o}C$	SMD	Raychem	SMD125-2
1	F1	Fuse,Polyswitch,2.5A @ $20^{o}C$	T.H.	Raychem	RUSB250
2	J11,J13	Conn.,DIMM,168 pin, SDRAM,3.3vdc	168_DIMM	Molex	71736-0008

Table B-4. Bill-of-Materials

QTY	REFERENCE DESIGNATION	DESCRIPTION	PACKAGE	MFG.	MFG'S PART NUMBER
1	J5	Conn.,hdr2x13,shroulded, vertical,PP	T.H.	AMP	103308-6
1	J6	Conn.,DB15,shielded,VGA, R/A	T.H.	AMP	787066-3
1	J8	Conn.,0.050" mini D ribbon (MDR),R/A	T.H.	AMP	2-178238-2
1	J3	Conn., USB, R/A, Dual stack	T.H.	AMP	787617-1
1	J7	Conn.,hdr2x8,shroulded, Game Port	T.H.	MOLEX	2516-6002UG
1	J20	Conn.,hdr1x26,Front panel	T.H.	Berg	68001-226
3	J16,J17,J22	Conn., PCI	T.H.	AMP	145154-4
1	J2	Conn.,R/A,30pin,ITP	T.H.	AMP	104069-5
1	J23	Conn.,hdr2x3,Debug Hdr	T.H.	AMP	87227-3
2	J19,J21	Conn.,hdr2x5,Shrouded, COM1&COM2	T.H.	AMP	111657-1
1	J1	Conn., Min. Cir. DIN, Dual stack	T.H.	AMP	84376
2	J12,J15	Conn., Hdr 2x20, Shrouded,IDE	T.H.	AMP	111945-8
1	J14	Conn., Hdr 2x17, Shrouded,Floppy	34-PIN	AMP	111944-7
1	J9	Conn., RJ45 w/LED, + magnetics	T.H.	Amphenol	RJMG-5312-11-01
4	J24,J26,J25,J27	Conn., Hdr 1x3	T.H.	Berg	68001-203
1	J18	Conn., AMR	T.H.	AMP	650090-7
16	JP6,JP14,JP15,JP21,JP7, JP1,JP17, JP18, JP16,JP13, J P11,JP3,JP2,JP5,JP4,JP12	Conn., Header, 1x2	T.H.	Berg	68001-202
6	JP8,JP9,JP10,JP22,JP20, JP19	Conn., Hdr 1x3	T.H.	Berg	68001-203
1	L14	Power Choke Coil,0.8 uH,20 A, 2.24m ohms	SMD	Panasonic	ETQP6F0R8L
1	L22	Inductor,4.7 uH,30 mA, 0.7 ohm,shielded	SM0805	MuRata	LQG21N4R7K10
16	L26,L27,L12,L25,L4,L7,L6,L3, L2, L1, L13,L17, L18, L15, L16, L5	Ferrite Bead,300 mA,R=0.3,Z=125	SM1812	ACT	BCB-1812
1	L24	Inductor,68 nH, 300 mA, R=0.8	SM0603	muRata	LQG11A68NJ00
3	L21,L20,L19	Ferrite Bead,200 mA,R=0.15,Z=70	SM0603	muRata	BLM11B750S
1	L8	Inductor,1uH,9A,0.009 ohm	SMD	Coilcraft	DO3316P-102
4	L9,L23,L10,L11	Ferrite Bead, 200mA, R=0.60, Z=120	SM0805	ACT	KCB-0805
1	Q11	Trans.,2N3904	SOT-23	Motorola	MMBT3904LT1
1	Q10	Trans.,TMOS FET	SOT-23	Motorola	2N7002LT1
4	Q1,Q3,Q2,Q4	MOSFET,N-Channel,30v	SO-8	Temic	Si4410DY
1	Q7	Trans.,2N3904	SOT-23	Motorola	MMBT3904LT1
2	Q9,Q8	MOSFET,N-Channel,30v	SO-8	Temic	Si4410DY

Table B-4. Bill-of-Materials

QTY	REFERENCE DESIGNATION	DESCRIPTION	PACKAGE	MFG.	MFG'S PART NUMBER
21	R60,R159,R152,R79,R115, R114,R222,R223,R213,R183, R186,R215,R200,R123,R62, R124,R180,R89,R178,R126, R172	Res.,4.7K ohm	SM0603	KOA	RM73B1JT472J
9	R102,R109,R106,R110,R107, R80,R69,R67,R66	Res.,75 ohm,1%	SM0603	KOA	RK73H1JT75R0F
5	R104,R7,R81,R73,R6	Res.,150 ohm,1%	SM0603	KOA	RK73H1JT1500F
1	R154	Res.,62K ohm	SM0603	KOA	RM73B1JT623J
1	R156	Res.,549 ohm,1%	SM0603	KOA	RK73H1JT5490F
3	R155,R163,R162	Res.,619 ohm,1%	SM0603	KOA	RK73H1JT6190F
4	R157,R158,R160,R161	Res.,49.9 ohm,1%	SM0603	KOA	RK73H1JT49R9F
17	R77,R34,R25,R32,R35R43, R26,R50,R51,R44,R45,R52, R53,R46,R129,R139,R140	Res.,33 ohm	SM0603	KOA	RK73B1JT330J
15	R8,R216,R206,R173,R133, R100,R143,R65,R74,R202, R116,R122,R113,R118,R121	Res.,1K ohm	SM0603	KOA	RM73B1JT102J
4	R3,R4,R88,R179	Res.,47 ohm	SM0603	KOA	RM73B1JT470J
35	R2,R218,R78,R90,R91,R185, R119,R195,R194,R151,R120, R64,R71,R150,R117,R181, R83,R225,R105,R103,R146, R148,R149,R31,R128,R193, R192,R96,R95,R92,R84, R210,R198,R13,R15	Res.,0 ohm	SM0603	KOA	RM73Z1JT
15	R17,R209,R187,R23,R231, R138,R93,R136,R137,R87, R230,R166,R170,R85,R203	Res.,10K ohm	SM0603	KOA	RM73B1JT103J
5	R21,R1,R56,R57,R99	Res.,243 ohm,1%	SM0603	KOA	RK73H1JT2430F
1	R5	Res.,680ohm	SM0603	KOA	RM73B1JT681J
1	R76	Res.,51 ohm	SM0603	KOA	RM73B1JT510J
2	R48,R184	Res.,10 ohm	SM0603	KOA	RM73B1JT100J
7	R41,R141,R16,R219,R175, R174, R86	Res.,8.2K ohm	SM0603	KOA	RM73B1JT822J
2	R82,R182	Res.,40.2 ohm,1%	SM0603	KOA	RK73H1JT40R2F
1	R125	Res.,174 ohm,1%	SM0603	KOA	RK73H1JT1780F
1	R165	Res.,402 ohm,1%	SM0603	Dale	CRCW06034020FT
2	R220,R197	Res.,10M ohm	SM0603	KOA	RM73B1JT106J
4	R168,R191,R167,R153	Res.,100 ohm	SM0603	KOA	RM73B1JT101J
1	R217	Res.,100K ohm	SM0603	KOA	RM73B1JT104J
1	R212	Res.,82 ohm	SM0603	KOA	RM73B1JT820J
5	R190,R189,R135,R134,R18	Res.,5.6K ohm	SM0603	KOA	RM73B1JT562J
3	R58,R59,R75	Res.,2.2K ohm	SM0603	KOA	RM73B1JT222J
3	R207,R208,R20	Res.,2.7K ohm	SM0603	KOA	RM73B1JT272J
3	R101,R228,R132	Res.,470 ohm	SM0603	KOA	RM73B1JT471J
4	R204,R205,R214,R211	Res.,15 ohm,1%	SM0603	KOA	RK73H1JT15R0F
6	R14,R12,R63,R11,R221,R94	Res.,15K ohm	SM0603	KOA	RM73B1JT153J
1	R72	Res.,470K ohm	SM0603	KOA	RM73B1JT474J
1	R201	Res.,560K ohm	SM0603	KOA	RM73B1JT564J

Table B-4. Bill-of-Materials

QTY	REFERENCE DESIGNATION	DESCRIPTION	PACKAGE	MFG.	MFG'S PART NUMBER
2	R224,R235	Res.,2.2K ohm	SM0603	KOA	RM73B1JT222J
1	R164	Res.,3K ohm	SM0603	KOA	RM73B1JT302J
3	R55,R130,R131	Res.,301ohm,1%	SM0603	KOA	RK73H1JT3010F
1	R54	Res.,130 ohm,1%	SM0603	KOA	RK73H1JT1300F
1	R19	Res.,20 ohm	SM0603	KOA	RM73B1JT200J
4	R33,R9,R232,R171	Res.,220 ohm	SM0603	KOA	RM73B1JT221J
3	R226,R199,R196	Res.,1M ohm	SM0603	KOA	RM73B1JT105J
1	R142	Res.,22K ohm	SM0603	KOA	RM73B1JT223J
14	R36,R37,R38,R39,R40,R47, R42,R49,R27,R28,R29,R30, R24,R127	Res.,22.1 ohm,12%	SM0603	KOA	RK73H1J22R1FT
2	R234,R233	Res.,68 ohm	SM0603	KOA	RM73B1JT680J
10	R10,R112,R111,R108,R144, R145,R188,R97,R98,R169	Res.,330 ohm ±5%	SM0603	KOA	RM73B1JT331J
1	R61	Res.,4.7K ohm	SM0603	KOA	RM73B1JT472J
2	R227,R229	Res.,47K ohm	SM0603	KOA	RM73B1JT473J
1	R147	Res.,330Kohm	SM0603	KOA	RM73B1JT334J
1	R22	Res.,5.1ohm	SM0603	KOA	RM73B1JT5R1J
2	R68, R70	Res.,110 ohm, 1%	SM0603	KOA	RK73H1JT1100F
29	RP6,RP5,RP10,RP9,RP21, RP41, RP43,RP26, RP25,RP35, RP24, RP23, RP38,RP42, RP40, RP39, RP37, RP32, RP36, RP33, RP7, RP11, RP12, RP20, RP8, RP22, RP18, RP19,RP3	Res. Pack, 56ohm	4_603	KOA	CN1J4TE560J
2	RP30,RP31	Res. Pack, 1K ohm	4_603	KOA	CN1J4TE102J
2	RP48,RP46	Res. Pack,10K ohm	4_603	KOA	CN1J4TE103J
4	RP1,RP62,RP61,RP60	Res. Pack,4.7K ohm	4_603	KOA	CN1J4TE472J
3	RP16,RP15,RP27	Res. Pack,33 ohm	4_603	KOA	CN1J4TE330J
6	RP28,RP17,RP13,RP14, RP29, RP34	Res. Pack,2.2K ohm	4_603	KOA	CN1J4TE222J
2	RP47,RP58	Res. Pack,5.6K ohm	4_603	KOA	CN1J4TE562J
7	RP57,RP55,RP63,RP56, RP52, RP53,RP54	Res. Pack, 8.2K ohm	4_603	KOA	CN1J4TE822J
8	RP69,RP68,RP66,RP65, RP67, RP44,RP64,RP4	Res. Pack, 0 ohm	4_603	KOA	CNZ1J4T
1	RP2	Res. Pack,330 ohm	4_603	KOA	CN1J4TE331J
2	RP50,RP49	Res. Pack, 150 ohm	4_603	KOA	CN1J4TE151J
2	RP59,RP45	Res.Pack,SIP,2.7K ohm	SIP10	Vishay	CSC10A01272G
1	RP51	Res. Pack,2.7K ohm	4_603	KOA	CN1J4TE272J
2	RP70,RP71	Res. Pack,10 ohm, 5%	4_603	KOA	CN1J4TE100J
1	SP1	SPEAKER	T.H.	RDI	DMT-1206
2	SW2,SW1	SWITCH, SPST, PB	T.H.	Grayhill	32-01
1	U12	I.C.,Hex Schmitt-trigger inverter	14SOIC	TI	SN74LVC14AD
2	U17,U16	I.C., RS232 Rec./Drv.	SSOP20	TI	GD75232-DB
2	U8,U9	I.C.,1X16SDRAM	50P_TSOP	Samsung	KM416S1020C

Table B-4. Bill-of-Materials

QTY	REFERENCE DESIGNATION	DESCRIPTION	PACKAGE	MFG.	MFG'S PART NUMBER
2	U5,U11	I.C.,Hex Buf./Drv. w/open-drain outputs	14SOIC	TI	SN74LVC07AD
1	J4	Conn., ATX	T.H.	Molex	39-29-9202
1	U15	I.C., SMSC LPC47B272	QFP100	SMSC	LPC47B272
1	U3	I.C.,Hex Inverter w/open-drain outputs	14SOIC	TI	SN74LVC06AD
2	Q5,Q6	I.C.,P-Channel FET	SSOT-3	Fairchild	NDS356AP
1	U1	I.C., ICS CK-Whitney	56PIN_SSOP	ICS	ICS9250AF-10
1	U2	I.C.,Intel 82810-DC100 (GMCH)	421BGA	Intel	Intel Supplied
1	U14	I.C.,Intel 82801AB (ICH0)	241BGA	Intel	Intel Supplied
1	U7	I.C., Flat-Panel Transmitter	64PIN_TQFP	SII	Intel Supplied
1	U13	I.C., Intel 82559	PBGA196	Intel	Intel Supplied
1	U10	I.C.,Quad. 2-input Positive-AND Gates	14SOIC	TI	SN74LVC08AD
1	U6	I.C.,High Speed CMOS 10bit Bus Switch	QSOP24	Quality Semi.	QS3384Q
1	U18	I.C., 1024-Bit Serial EEPROM	SO-8	Fairchild	NM93C46LZM8
1	U4	I.C.,Quad. 2-input Positive-NAND Schmitt	14SOIC	TI	SN74LS132D
2	VR2,VR3	I.C.,Adj. Pos. Regulator	TO-220	Linear Tech.	LT1587CT
1	VR4	I.C.,Fixed 3.3v Pos. Regulator	DD PAK	Linear Tech.	LT1117CM-3.3
1	VR1	I.C., Switching Regulator Controller	SSOP_20P	Linear Tech.	LTC1753CG
1	VR5	I.C.,GTL+ Regulator	DD PAK	Linear Tech.	LT1587CM-1.5
1	X2	Socket,370pin PGA	T.H.	AMP	916783-2
1	X1	Socket,14pin DIP,Osc. 48MHz	T.H.		
1	X4	Socket, 40pin TSOP, Intel 82802 (FWH)	T.H.	Meritec	980020-40-01
1	Y1	XTAL, 14.318Mhz	T.H.	Saronix	49S143-32
1	Y3	XTAL, 32.768khz_ICH	T.H.	Mtron	MMCC-2 32.768
1	Y2	XTAL, 25MHz, Parallel, Fund	T.H.	Saronix	49S250-16
1	X3	BATTERY Socket	T.H.	AMP	120591-1
1	N/A	I.C., Intel 82802AB, FWH	TSOP40	Intel	Intel Supplied
1	N/A	I.C.,Osc,48MHz,3.3V	T.H.	Saronix	DTH080A3 - 48.0000
2	R177,R176	Res.,56.2ohm,1%	SM0603	KOA	RK73H1JT56R2F
2	C123,C222	Cap.,33uf,16vdc,Tant.	SM7343	Kemet	T495D336M016AS

C

Customer Reference Board (CRB) Schematics

Customer Reference Board (CRB) Schematics C

This appendix provides a set of schematics for Intel's Customer Reference Board (CRB). The CRB feature list is shown below (for flexible motherboard design considerations see Section 6).

Intel® 810 Chipset Customer Reference Board Feature Set

- Intel® 810 Chipset
  - — Graphics and Memory Controller Hub (GMCH)
  - — I/O Controller Hub (ICH0)
  - — Firmware Hub (FWH)
- Support for the Intel® Celeron™ Processor PPGA 66/100 MHz System Bus Frequency
- Debug Port
- Synchronous SDRAM Memory Interface
  - — 100 MHz SDRAM Support
  - — 2 DIMM Sockets
- 4 MB Display Cache
- 3 PCI Add-in Slots
  - — 3 REQ#/GNT# pairs
- An Intel 82559 LAN Integrated into the Motherboard
- 2 IDE Connectors with Ultra ATA/33 Support
- 2 USB Connectors
- ATX Power Connector
- LPC SIO
  - — Floppy Disk Controller
  - — 1 Parallel Port, 1 Serial Port
  - — PS/2 Keyboard Controller
  - — PS/2 Mouse Controller
  - — Game/Midi Port
- AC'97 Bus Connector and Audio Codec
- WfM 1.1 Compliant
- Integrated System Management
- Integrated Power Management
  - — ACPI Rev. 1.0 Compliant
  - — APM Rev. 1.2 Compliant
- Intel® Celeron™ Processor PPGA On-board VRM
- 4-Layer Design

D

Reference Information

Intel® 810 Chipset: Thermal Design Considerations

Application Note AP-670

June 1999

Order Number: 292228-001

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Revision History

Revision	Description	Date
-001	Initial Release	June 1999

1.0 Introduction

This document is provides an understanding of the thermal characteristics of the Intel® 810 chipset and discusses guidelines for meeting the thermal requirements imposed on platforms. Some previous generations of Intel® Celeron™ processor PCIsets did not require a significant platform design effort to meet the component case temperature specifications. As the market transitions to higher-speeds and higher bandwidths with enhanced features, devices will generate more heat. Consequently, this introduces new thermal challenges for system designers. Depending on the type of system and the chassis characteristics, new designs may be required to provide better cooling solutions for these devices.

Elements of Thermal Design

In a system environment, the temperature of a component is a function of both the system and component thermal characteristics. The system level thermal constraints consist of the local ambient temperature at the component, the airflow over the component and surrounding board as well as the physical constraints at, above, and surrounding the component which may limit the size of a thermal enhancement (heat sink). The component's case temperature depends on the component power dissipation, size, packaging materials (effective thermal conductivity), the type of interconnection to the substrate and motherboard, the presence of a thermal cooling solution, the thermal conductivity and the power density of the substrate, nearby components, and motherboard.

All of these parameters are pushed by the continued trend of technology to increase performance levels (higher operating speeds, MHz) and power density (more transistors). As operating frequencies increase and packaging size decreases, the power density increases and the thermal cooling solution space and airflow become more constrained. The result is an increased emphasis on system design to ensure that thermal design requirements are met for each component in the system.

Importance of Thermal Management

The objective of thermal management is to ensure that the temperature of all components in a system is maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

1.1 Intel® 810 Chipset Packaging Terminology

BGA	Ball Grid Array. A package type defined by a resin-fiber substrate on to which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
Junction	Refers to a P-N junction on the silicon itself. In his document it is used as a temperature reference point.
MBGA	Mini Ball Grid Array. Defined as an Intel® BGA with 1.27mm ball pitch.
Lands	The pads on the PCB to which the BGA Balls are soldered.
Mold-Cap	The black encapsulating molding compound. The top of this is where maximum case temperatures are taken and where heat sinks are attached.
PCB	Printed Circuit Board.
TDP	Thermal Design Power. This is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.
Thermal Balls	Typically, this refers to an array of balls in the center of the larger array of balls which serve to channel heat into the PCB as well as ground connections.

1.2 References

- *Intel® 810 Chipset Design Guide* (Order Number: 290657)
- *Intel® 810 Chipset: Intel® 82810 and 82810-DC100 Graphics and Memory Controller Hub (GMCH)* Datasheet (Order Number: 290656)
- *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet (Order Number: 290655)
- *Intel® Celeron ™ Processor Thermal Design Guidelines* Application Note (Order Number: 243331)
- *Design For EMI* Application Note AP-589 (Order Number: 243334)
- Integrated Circuit Thermal Measurement Method-Electrical Test Method (EIA/JESD51-1)
- Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air) (EIAJESD51-2)

2.0 Thermal Specifications

Thermal Design Power (TDP) for the Intel® 810 chipset can be found either in the *Intel® 810 Chipset Design Guide* or *Design Guide Updates*. Refer to these documents to verify the thermal and power specifications for the Intel® 810 chipset. In general, systems should be designed to dissipate the highest possible thermal power.

To ensure proper operation and reliability of the Intel® 810 chipset, the thermal solution must maintain the case temperature at or below the values specified in Table 1 and Table 2. Considering the power dissipation levels and typical system ambient environments of 45°C to 55°C, if the case temperature exceeds the maximum case temperature listed in Table 1, system or component level thermal enhancements will be required to dissipate the heat generated.

To dissipate the highest possible thermal power good system airflow is critical. Airflow is determined by the size and number of fans, vents and ducts along with their placement in relation to the components and the airflow channels within the system. In addition, acoustic noise constraints may limit the size and/or types of fans, vents and ducts that can be used in a particular design.

To develop a reliable, cost-effective thermal solution, all of the above variables must be considered. Thermal characterization and simulation should be carried out at the entire system level accounting for the thermal requirements of each component.

Table 1. Intel® 810 Chipset Preliminary Thermal Absolute Maximum Rating

Parameter	Maximum	Notes
$T_{case\text{-}nhs}$	114 °C	1
$T_{case\text{-}hs}$	97 °C	2

NOTES:
1. $T_{case\text{-}nhs}$ is defined as the maximum case temperature without any thermal enhancement to the package.
2. $T_{case\text{-}hs}$ is defined as the maximum case temperature with the default thermal solution attached (see Section A).

Table 2. ICH Preliminary Thermal Absolute Maximum Rating

Parameter	Maximum	Notes
$T_{case\text{-}nhs}$	100°C	1

NOTES:
1. $T_{case\text{-}nhs}$ is defined as the maximum case temperature without any thermal enhancement to the package.

2.1 Case Temperature

The case temperature is a function of the local ambient temperature and the internal temperature of the component under evaluation. As a local ambient temperature is not specified for the components in an Intel® 810 chipset, the only restriction is that the maximum case temperature (Tcase) is not exceeded. Section 5.1 discusses proper guidelines for measuring the case temperature. Note that increasing the heat flow through the case (moldcap) increases the difference in temperature between the junction and case, reducing the maximum allowable case temperature. For the default thermal solution, see the adjusted values listed in Table 1.

2.2 Power

In previous generations of chipsets where Quad Flat Pack (QFP) packages may have been the primary package type, the majority of power dissipation has been through the plastic case of the package into the surrounding air. With the advent of Ball Grid Array (BGA) packaging for chipsets, the majority of the thermal power dissipated by the chipset typically flows into the motherboard to which it is mounted (when thermal or center balls are present). The remaining thermal power is dissipated into the ambient environment by the package itself. The MBGA packages used in the Intel® 810 chipset continues this trend.

The amount of thermal power dissipated, either into the board or by the package, varies depending on how well the motherboard conducts heat away from the package and whether the package uses thermal enhancements. While package thermal enhancements typically serve to improve heat flow through the case via a heat sink, how well the motherboard conducts heat away from the package is strictly a function of motherboard design:

The following are recommendations to ensure good thermal conductivity between the thermal balls and the inner planes of the motherboard:

- Good mechanical connection
- One via per ground ball be used (min).
- Minimum width of the trace connecting motherboard ground pads to their respective vias be 10 mil.
- Plated Via Size for ground balls be 14 to 16mil in diameter on a 24 mil to 27 mil pad. A larger via is more efficient in channeling heat.
- Do not use Thermal Relief Patterns to connect the via to the inner power and ground planes.

The following are recommendations to ensure that the motherboard inner planes effectively conduct heat away from the area beneath the package:

- Good ground paths to areas of the board away from the BGA will distribute heat more efficiently.
- The size of the motherboard, number of copper layers and the thickness of those layers. In some cases, the use of “2-ounce copper” on the ground plane has been successful in improving the thermal conduction by reducing case temperatures.

All points should be taken into account by system and board designers when developing new systems.

3.0 Designing for Thermal Performance

This section discusses general design consideration for all chassis. Specific design considerations for uATX, ATX and NLX chassis may be found at the following URLs:

http://www.teleport.com/~nlx/

http://www.teleport.com/~atx/

http://www.teleport.com/~microatx/

3.1 System Cooling

The first step in defining an acceptable cooling solution is to estimate the total airflow required to cool the entire system (not just the processor). Using the ideas from the 1st Law of Thermodynamics (Conservation of Energy) for a steady state steady flow process, the relationship between volumetric airflow, heat load (measured DC power), and the temperature rise of the system can be studied. To reach this simplified model, it is assumed that the change in kinetic and potential energy of the airflow is zero and no work is performed by the system.

For a zero airflow restriction inside the computer, the relationships are as follows:

$$V = f(\text{Power} / \text{Temperature rise})$$

Where **V** is the volumetric airflow, **Power** is the actual power dissipated by the power supply (DC power), and **Temperature rise** is the temperature rise of the system.

Note: For NO change in system temperature, as DC power increase, airflow must increase

Thus, more volumetric airflow is needed to keep the temperature rise of the system at a minimum. Note that these are under ideal conditions. In reality, there is between 30% to 50% restriction of airflow. For a well-designed chassis, an airflow increase of approximately 25% is typical to account for the system impedance. If possible, use the measured DC power of the system for the Power variable. The AC power can be used as an approximation; however, the inefficiency of the power supply makes this measurement larger than the actual power dissipated.

3.2 System Fans

Fans implement the forced convection approach to cooling. Stated simply, the greater the air velocity over the surface of a component, the greater the heat transfer from that component. Fans can be used to blow air into (pressurize) or out of (evacuate) the chassis depending on which direction they are installed.

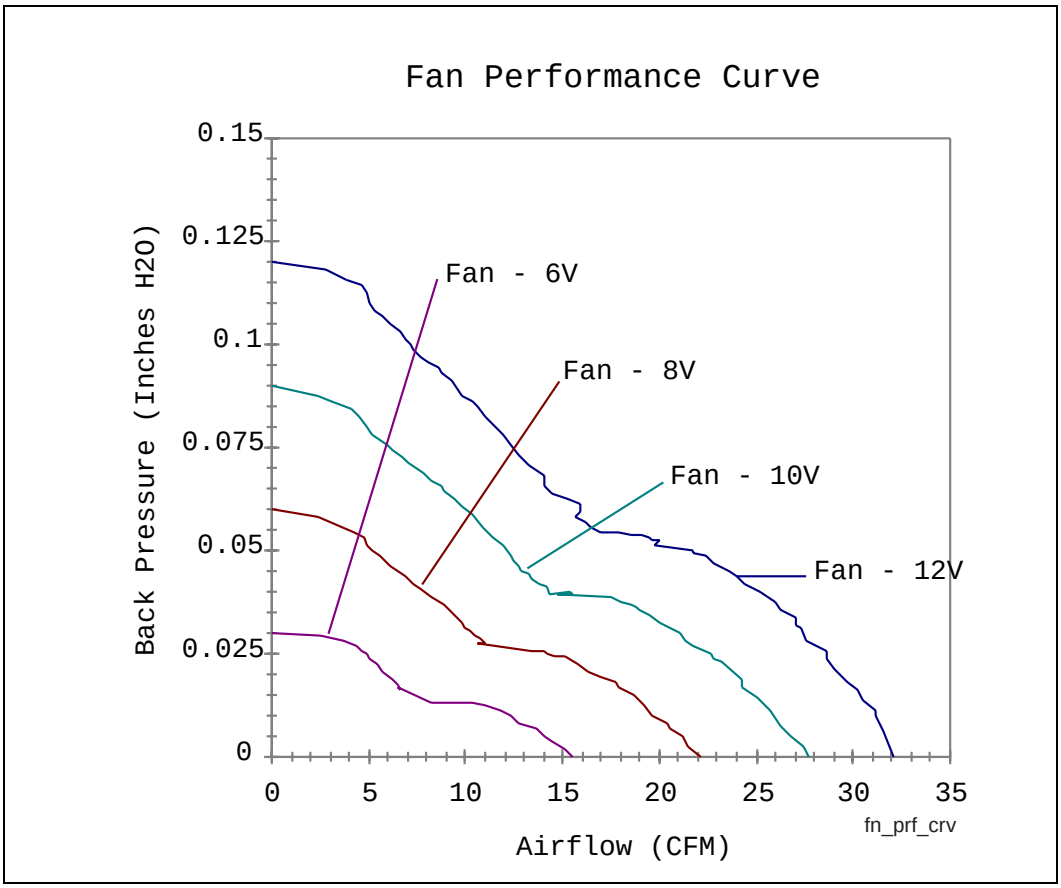
- **Pressurizing** the chassis with a fan delivers cool, room-temperature ambient air onto any location where it is needed to enhance heat transfer.
- **Evacuating** induces a negative pressure (relative to room ambient) inside the chassis, which draws air in through the vents. This inflow of air from the vents is pulled through the chassis across hot components and is exhausted out the fan. Fans may differ in their characteristics, and, therefore, a prudent choice of fans can optimize both airflow and acoustics.

3.2.1 Fan Types

Although there are several types of fans to consider for system cooling, this chapter focuses on two types; Tube Axial and Radial.

Tube axial is the most commonly used type throughout the computer industry. Axial fans typically cost less and generally push more air at a given back pressure. Radial fans, however, are much less susceptible to variations in back pressure and often have restricted openings which can focus needed cooling air directly at hot components. When power dissipation is highly concentrated, a blower may be a reasonable option. Figure 1 shows a typical axial fan characteristic curve and the effect of running the fan at different speeds (or voltage levels).

Figure 1. Typical Fan Characteristic Curve (for Various Voltages)



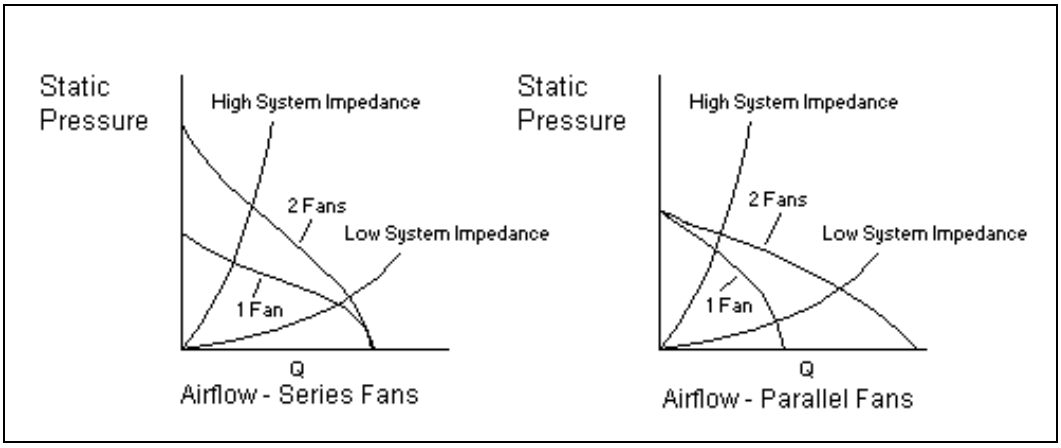
3.2.2 Parallel and Series Fan Combinations

Multiple fans can be utilized in two combinations, parallel and series.

- Two identical fans in parallel double the airflow, total airflow equals the airflow of fan 1 + airflow of fan 2 at zero back pressure, An example of a parallel fan combination is a system fan and a power supply fan both either pressurizing or evacuating a chassis.
- Two identical fans in series doubles the system's ability to overcome back pressure; total pressure is equal to the pressure of fan 1 + the pressure of fan 2 at zero airflow, An example of a series fan combination is a system fan blowing air into the chassis and a power supply fan exhausting air from the chassis.

Generally, due to venting, leakage and design compromises, when multiple fans are employed, a combination series/parallel configuration is often implemented. The effect of employing series/parallel fan configurations is shown in Figure 2.

Figure 2. Performance Curves for Series and Parallel Fan Combinations



Employing multiple (identical) fans in a system provides some marginal increase in airflow. The exact amount depends on many factors including fan speed and configuration, as well as chassis airflow impedance. If the fans are not identical, the figures will change slightly, but the trends will be the similar. **The general rule is: If the chassis has high impedance, place the fans in series. If the chassis has low impedance, place the fans in parallel.**

3.2.3 Fan Relationships

Fan variables such as airflow, pressure, R.P.M., and power can be generalized for a tube axial two fan combination of constant diameter.

- Airflow increases linearly with speed
- Pressure increases with the square of the speed
- Power increases with the cube of the speed

Understand that increasing the fan speed to increase airflow results in a much larger increase in pressure. If increased airflow is desired, consider increasing the fan diameter from 80 mm to 92 mm instead of increasing the speed. Cost must be considered because generally 92 mm fans are more expensive than 80 mm fans; however, a 92 mm fan operating at the same flow rate as an 80 mm fan is approximately 6 dBA quieter.

3.2.4 Fan Speed Control

Fan speed control circuit ideas have been around for some time but were generally avoided because of adding unnecessary cost and system complexity. Computers are now incorporating hotter processors and peripherals requiring greater airflow while, at the same time, customers are requesting quieter systems. These competing design constraints have led to a resurgence of fan speed control options. Fan speed control allows a system to vary its airflow as changes in load and/or temperature occur. Fan noise increases with fan speed and is a major contributor to total system noise. For systems that incorporate fan speed control, proper speed regulation is important since it is desirable to achieve low acoustic levels without overheating components. The fan speed control circuit should be designed such that it monitors temperature at a component (or several components) and adjusts fan speed as necessary to maintain the required thermal margin. Three distinct design options should be considered.

- **Discrete Digital Switches.** If airflow requirements can be confined to a discrete number of fan speeds, this option is the cheapest and easiest to implement.
- **Analog Linear Control between Two Guard Bands.** For fans used in most systems, speed control can usually be accomplished by varying the voltage level at the fan's power terminals (many power supplies/fans come equipped with this feature). An operating voltage range example for an 80 mm, 30 CFM, 0.14 amp fan might be 8 V to 12 V DC, corresponding to 1650 rpm and 2500 rpm, respectively.
- **Pulse Width Modulation Schemes.** This is a digital variation on the second option. Consider this option if the fan needs to be varied from some minimum speed (presumably set for the system sleep state) to some maximum speed (needed for a fully loaded active state).

Summary

Independent of which fan speed control method is chosen, the following issues should also be noted:

- The location where temperature is monitored is important (sensing critical component case temperatures is recommended).
- A driver circuit for the fan must be included.
- Some fans need a minimum starting voltage (see fan specification).
- Fan noise increases with fan speed (operating voltage). Minimum fan noise occurs at maximum fan power efficiency (see fan specification).
- If the fan is not speed controlled, at what speed (voltage level) is it operating? In this case since it is not possible to vary fan speed, choose the lowest rated fan speed that will cool the system under worst-case loading/temperature conditions.

If fan speed control is implemented, the thermal design should account for various load and temperature combinations. Component temperatures should be verified to ensure the thermal design meets specification under these load and temperature combinations.

4.0 System Airflow

4.1 Chassis and Bezel Venting

Proper venting is a key element in any good thermal design. A balanced vent configuration is a critical factor in this design. Implementing an insufficient amount of venting does not allow enough air into the system for adequate cooling. Implementing too much venting can decrease the air velocity across system components, resulting in less heat transfer through forced convection. To increase airflow through the system, all system accessory components (cables, wires, sheet metal, etc.) should present the lowest possible air impedance. To eliminate possible electromagnetic compliance issues, both the maximum vertical and maximum horizontal dimensions of ventilation apertures, I/O ports, and open areas along chassis seams must be less than 1/20th of a wavelength of the highest harmonic frequency of interest.

Key Considerations

- **Power Supply.** The air flow from the power supply fan is less of an importance when the front system fan delivers the majority of the airflow.
- **Front bezel venting.** The bezel vent area should be as large as possible because it serves as the main air inlet for the system. It also provides the main airflow source for the core logic components. **Ensure the plastic bezel vent pattern allows air to enter freely so it does not overly restrict airflow into the system.**
- **Riser card.** Some venting at the front and back of any riser cards is necessary to allow for the evacuation of the chassis and airflow over the add-in cards.
- **Side chassis venting.** This is desirable if there are any cards with components which require cooling nearby.
- **Rear chassis venting.** This adds to the airflow capability of the chassis.
- **Peripheral bay venting.** Cools peripherals. Minimal venting, if any, should produce adequate results. Implementing too much venting may cause lower airflow in other areas of the chassis.

4.2 Airflow Impedance

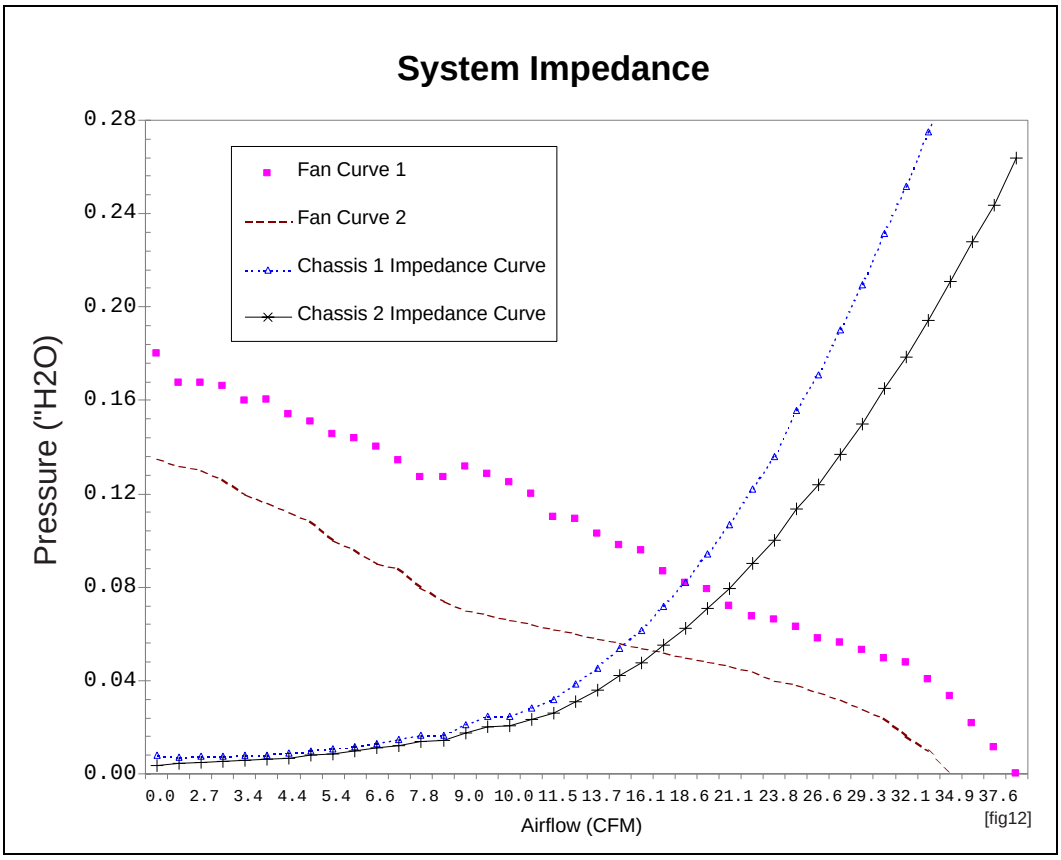
Air flowing through a computer chassis encounters frictional resistance, known as airflow impedance. This impedance creates a pressure drop in the chassis. The pressure drop will vary with the square of the velocity. Plotting pressure loss versus volumetric flow rate, which results in the system characteristic curve, can show the relationship. The point about this behavior is that if one data point on the curve is known, the system's overall performance can be predicted. When the system characteristic curve is superimposed on the fan performance curve, the operating point of the system is specified explicitly. The concept is demonstrated in Figure 3 where different power supplies are compared with different chassis.

The following lists additional guidelines to consider when assessing system airflow issues:

- To avoid pressure and volume fluctuations, the operating point should be chosen just right of the intersection between the fan curve and the chassis impedance curve.
- Choose a fan with a steep characteristic curve to maintain constant volumetric flow even with variable system impedance.
- Avoid obstructions near the inlet and exhaust of the fans as these tend to decrease airflow and increase system noise. Objects near the inlet can contribute to system noise.

- Use fan speed control whenever possible. This yields adequate thermal margin and provides a significant acoustic advantage.
- Power supply cables and drive signal cables should be kept short and properly folded.

Figure 3. System Characteristic Curve



4.3 Power Supply Airflow Characteristics

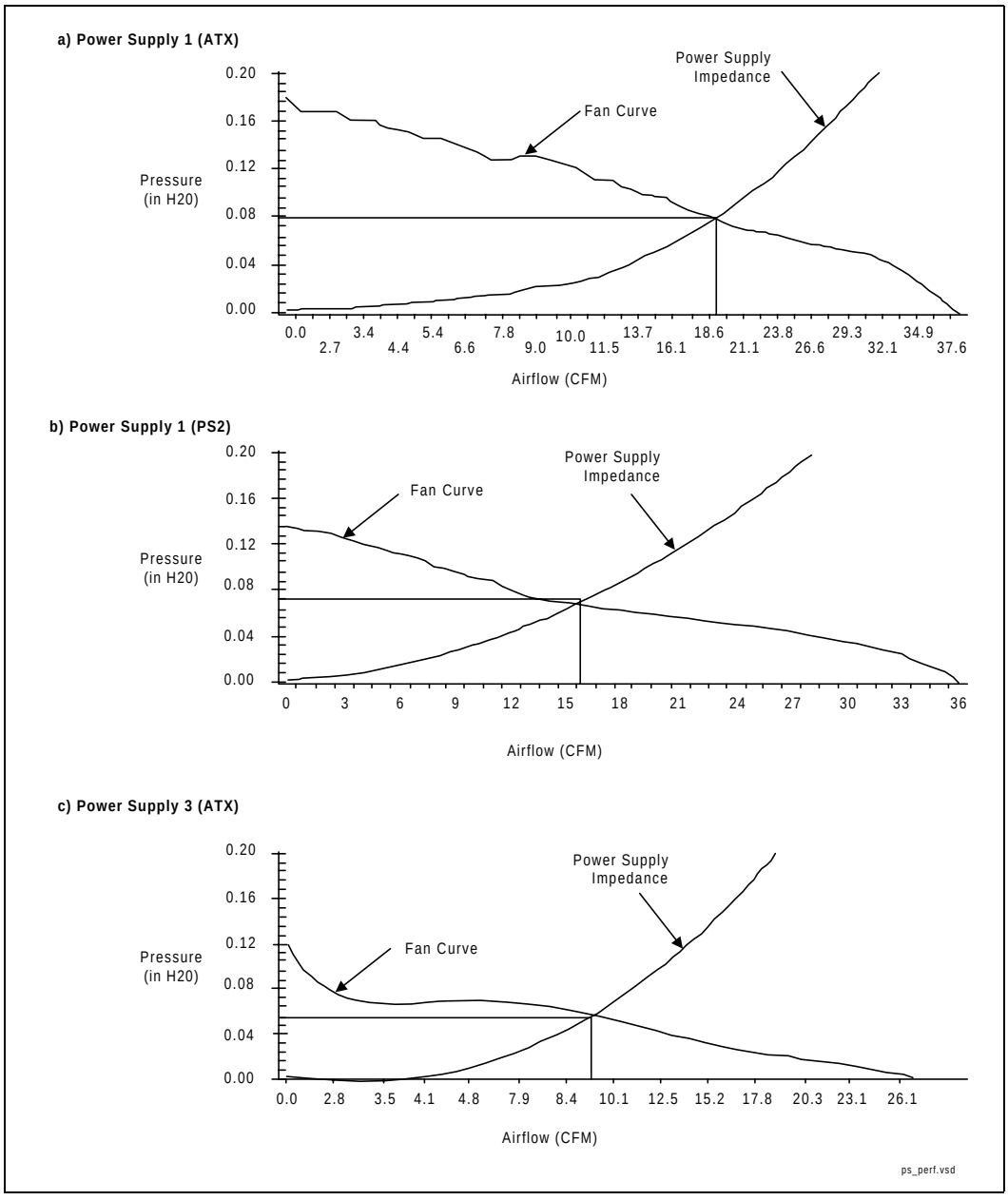
The power supply is the most influential component in the cooling system design. The chassis venting scheme may be well designed; however, if the correct power supply is not selected, the system will not cool the processor, chipset, memory, and/or the peripherals. The power supply and any system fans must provide enough airflow to cool the system heat load as outlined by the Equation in Section 2.1.

Key considerations when selecting/designing a power supply:

- Evacuate the chassis (rather than pressurize it) with the power supply fan. The advantage of evacuating the chassis is that cool room ambient air can be delivered (via vents) to any location where it is needed to enhance heat transfer. Evaluation has shown evacuating produces greater cooling than pressurizing using the same fan with proper implementation.
- All vents should have a minimum free area ratio of 60%. Consult the EMI design guidelines to ensure vent designs comply with all applicable regulations.
- Implement a wire fan grille rather than the common stamped sheet metal designs because the airflow impedance is reduced.
- When designing a power supply, minimize the component height to keep their profile low and streamlined. This reduces the overall airflow impedance while still maintaining effective power supply cooling.
- Keep power supply cables short to reduce their airflow obstruction.
- Select a power supply with the highest airflow possible. A well-designed power supply has low airflow impedance, allowing a smaller, quieter fan for cooling. The poorly designed supply requires a larger, louder fan to maintain the same airflow due to its greater airflow impedance.

Figure 4 depicts the power supply impedance curve and the associated fan curve of three different power supplies. The point where the fan curve intersects the power supply impedance curve defines the operating point. Power supplies 1 and 2 (ATX and PS2 style, respectively) flow approximately twice as much as power supply 3 (ATX style). Note power supply 3 has a smaller fan and higher airflow impedance resulting in the lower airflow.

Figure 4. Power Supply Performance Comparison



4.4 Ducting

Ducts can be designed to isolate components from the effects of system heating and to maximize the thermal budget. Air provided by a fan or blower can be channeled directly over the components to be cooled or split into multiple paths to cool multiple components.

Ducting Placement

When ducting is to be used, it should direct the airflow evenly from the fan across the entire target area and surrounding motherboard. The ducting should be accomplished, if possible, with smooth, gradual turns as this will enhance the airflow characteristics. Sharp turns in ducting should be avoided. Sharp turns increase friction and drag and will greatly reduce the volume of air reaching the target.

While there are many ducting options, an excellent source of ducting alternatives can be found at the following URL:

http://developer.intel.com/ial/sdt/fanduct.htm

4.5 Intel® 810 Chipset GMCH Thermal Attributes

4.5.1 Physical Package Information

The GMCH (Intel 82810 and 82810-DC100) is packaged in a 31 mm, 4-layer MBGA. As a reference, the mechanical drawings are shown in Figure 5 and Figure 6.

Figure 5. GMCH Package Dimensions (421 BGA)–Top and Side View

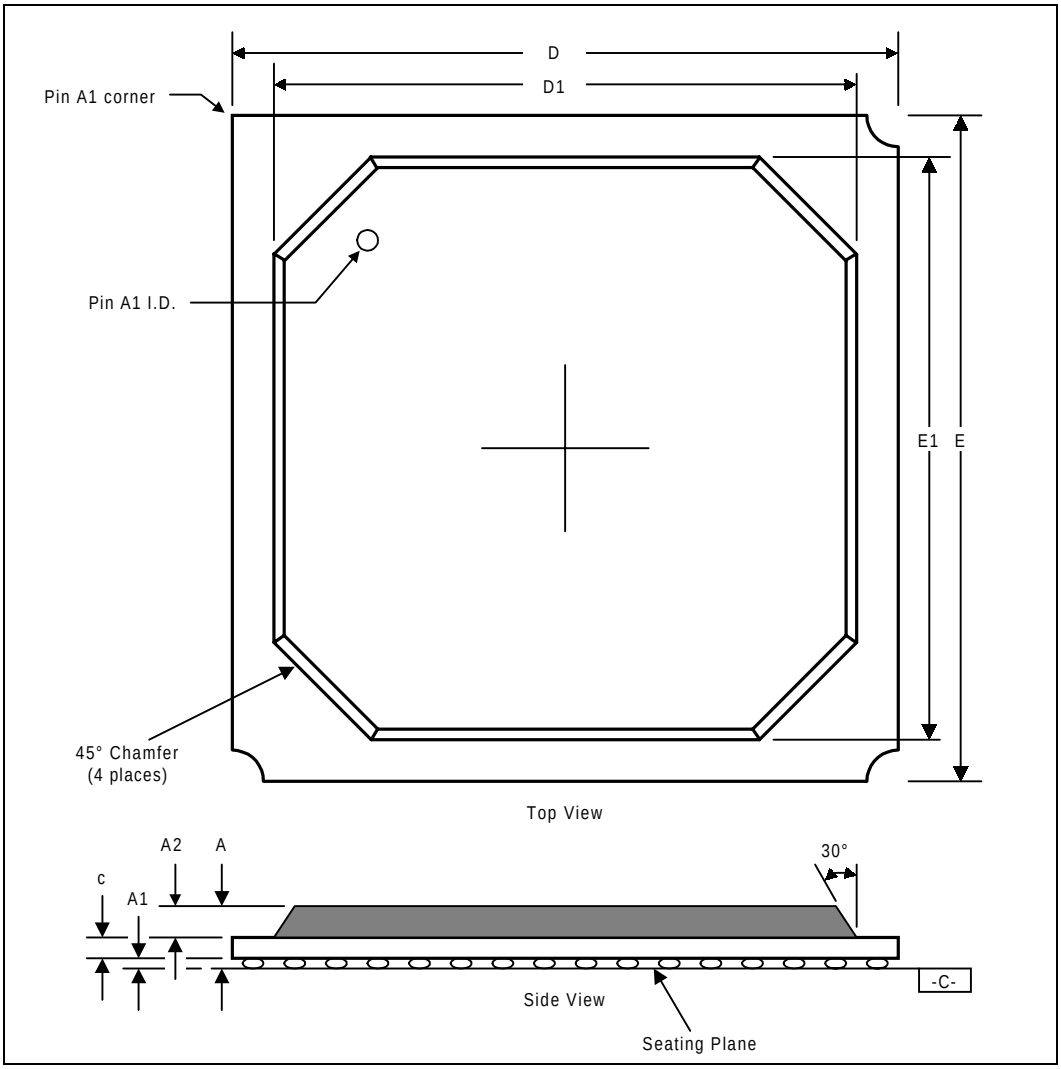


Figure 6. GMCH Package Dimensions (421 BGA)–Bottom View

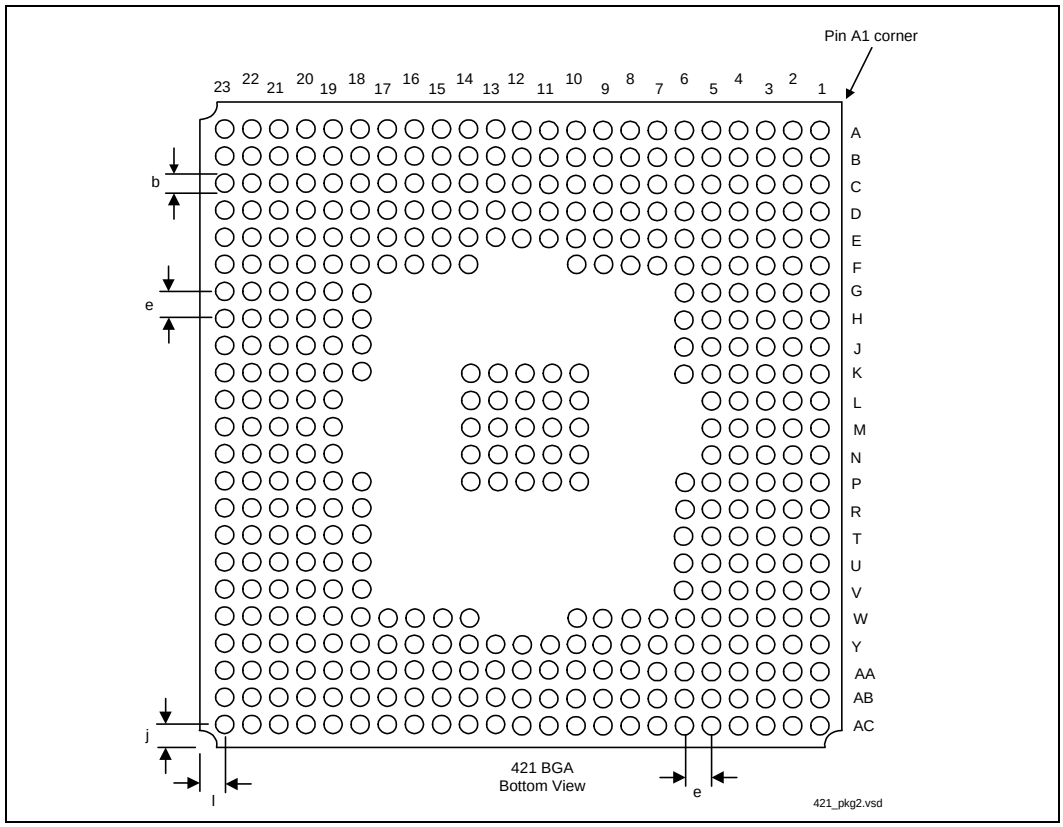


Table 3. GMCH Package Dimensions (421 BGA)

Symbol	Min	Nominal	Max	Units	Note
A	2.17	2.38	2.59	mm	
A1	0.50	0.60	0.70	mm	
A2	1.12	1.17	1.22	mm	
D	30.80	31.00	31.20	mm	
D1	25.80	26.00	26.20	mm	
E	30.90	31.00	31.10	mm	
E1	25.80	26.00	26.20	mm	
e	1.27 (solder ball pitch)			mm	
l	1.53 REF.			mm	
J	1.53 REF.			mm	
M	23 x 23 Matrix			mm	
b^2	0.60	0.75	0.90	mm	
c	0.55	0.61	0.67	mm	

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5-1982
2. Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-)
3. Primary Datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.

4.5.2 GMCH Package Thermal Characteristics

As an aid in determining the optimum airflow and heat sink combination for GMCH, Table 4 and Table 5 have been provided. The tables show Tcase as a function of airflow and ambient at the Thermal Design Power. These tables can be used to evaluate the system solution.

Table 4. No Heat Sink Attached (Tcase Specification = 114 °C)

Ambient (°C)	Heat Sink Tcase at TDP (°C)						
60	126	122	118	115	112	110	107
55	121	117	113	110	107	105	102
50	116	112	108	105	102	100	97
45	111	107	103	100	97	95	92
40	106	102	98	95	92	90	87
35	101	97	93	90	87	85	82
LFM	0	50	100	150	200	250	300

NOTES:
1. The values indicated in unshaded cells are combinations that will exceed the allowable case temperature for GMCH with default thermal solution. The values in shaded cells do not.
2. Heat Sink case assumes the default thermal solution, see Section A.3.
3. Tcase max with no heat sink is 114 °C, Tcase max with a heat sink is 97 °C.
4. Data collected is from Flotherm* simulations based on a motherboard environment, see Section C.
5. Zero LFM environment assumes natural convection.

Table 5. Heat Sink Attached (Tcase Specification = 97 °C)

Ambient (°C)	Heat Sink Tcase at TDP (°C)						
60	106	102	98	93	89	86	84
55	101	97	93	88	84	81	79
50	96	92	88	83	79	76	74
45	91	87	83	78	74	71	69
40	86	82	78	73	69	66	64
35	81	77	73	68	64	61	59
LFM	0	50	100	150	200	250	300

NOTES:
1. The values indicated in unshaded cells are combinations that will exceed the allowable case temperature for GMCH with default thermal solution. The values in shaded cells do not.
2. Heat Sink case assumes the default thermal solution, see Section A.3.
3. Tcase max with no heat sink is 114 °C, Tcase max with a heat sink is 97 °C.
4. Data collected is from Flotherm* simulations based on a motherboard environment, see Section C.
5. Zero LFM environment assumes natural convection.

5.0 Measurements for Thermal Specifications

To appropriately determine the thermal properties of the system, measurements must be made. Guidelines have been established for the proper techniques to be used when measuring the Intel® 810 chipset case temperatures. Section 5.1 provides guidelines on how to accurately measure the case temperature of the Intel® 810 chipset. Section 5.2 contains information on running an application program that emulates anticipated maximum thermal design power. The flowchart in Figure 9, as well as Appendix A offer useful guidelines for performance and evaluation.

5.1 Case Temperature Measurements

To ensure functionality and reliability, the Intel® 810 chipset is specified for proper operation when Tcase (case temperature) is maintained at or below the maximum case temperatures listed in Table 1. The surface temperature of the case in the geometric center of the mold cap is measured. Special care is required when measuring the Tcase temperature to ensure an accurate temperature measurement.

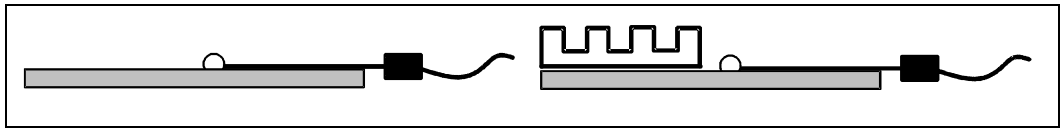
Thermocouples are often used to measure Tcase. Before any temperature measurements are made, the thermocouples must be calibrated.

When measuring the temperature of a surface which is at a different temperature from the surrounding local ambient air, errors could be introduced in the measurements. The measurement errors could be due to having a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation, convection, by conduction through thermocouple leads, or by contact between the thermocouple cement and the heat-sink base for those solutions which implement a heat-sink. To minimize these measurement errors the following approach is recommended:

Attaching the Thermocouple

- Use 36 gauge or smaller diameter K type thermocouples.
- Ensure that the thermocouple has been properly calibrated.
- Attach the thermocouple bead or junction to the top surface of the package (case) in the center of the mold-cap using high thermal conductivity cements. An alternative for tape attach users is to use the tape itself to mount the thermocouple. **It is critical that the thermocouple lead be butted tightly against the entire moldcap.**
- The thermocouple should be attached at a 0° angle if there is no interference with the thermocouple attach location or leads (refer to Figure 7). This is the preferred method and is recommended for use with both unenhanced packages as well as packages employing Thermal Enhancements.

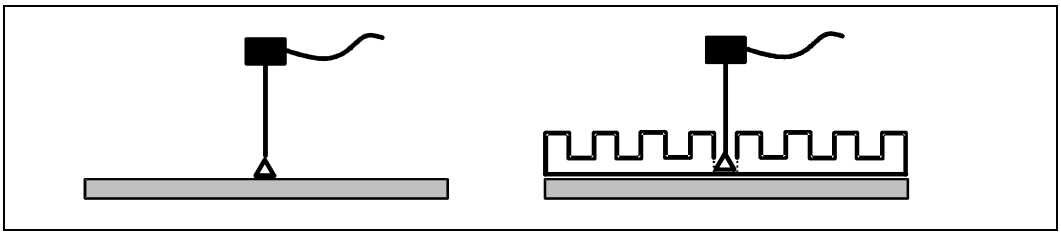
Figure 7. Technique for Measuring Tcase with 0° Angle Attachment



- If the thermocouple cannot be attached as previously shown, the thermocouple may be attached at a 90° angle. (refer to Figure 8).
- The hole size through the heat sink base to route the thermocouple wires out should be smaller than 0.150” in diameter.

- Make sure there is no contact between the thermocouple cement and heat sink base. This contact will affect the thermocouple reading.

Figure 8. Technique for Measuring Tcase with 90° Angle Attachment

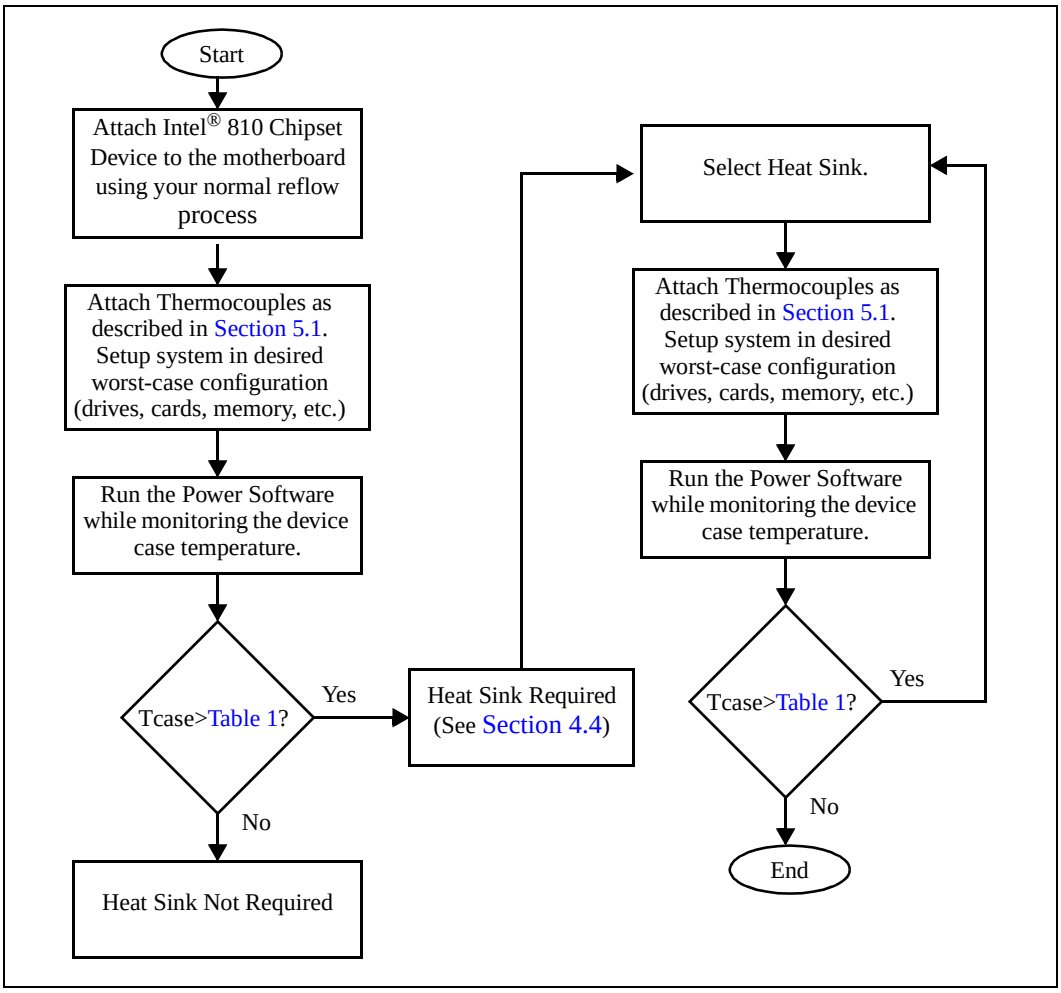


5.2 Power Simulation Program

The Power Simulation Software is a utility designed to test the thermal design power for an Intel® 810 chipset when used in conjunction with a Intel® Celeron™ processor. The combination of the Intel® Celeron™ processor and the higher bandwidth capability of the Intel® 810 chipset enables new levels of system performance. To ensure the thermal performance of the Intel® 810 chipset under “worst-case realistic application” conditions, Intel has developed a software utility that emulates this anticipated power dissipation.

The Power Simulation Software has been developed solely for testing Thermal Design Power and customer thermal solutions (Figure 9). Real future applications may exceed the Thermal Design Power limit for transient time periods.

Figure 9. Thermal Enhancement Decision Flowchart



6.0 Conclusion

As the complexity of today's systems continues to increase, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Heat can be dissipated using improved system cooling, selective use of ducting and/or passive heat sinks.

The simplest and most cost effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents and ducts. When additional cooling is required, thermal enhancements may be implemented in conjunction with enhanced system cooling. The size of the fan or heat sink can be varied to balance size and space constraints with acoustic noise.

This document has presented the conditions and requirements to properly design a cooling solution for systems implementing the Intel® 810 chipset. Properly designed solutions provide adequate cooling to maintain the chipset case temperatures at or below those listed in Table 1 and. This is accomplished by providing a low local ambient temperature and creating a minimal thermal resistance to that local ambient temperature. By maintaining the Intel® 810 chipset case temperature at or below those recommended in this document, a system will function properly and reliably.

Appendix A Thermal Enhancements

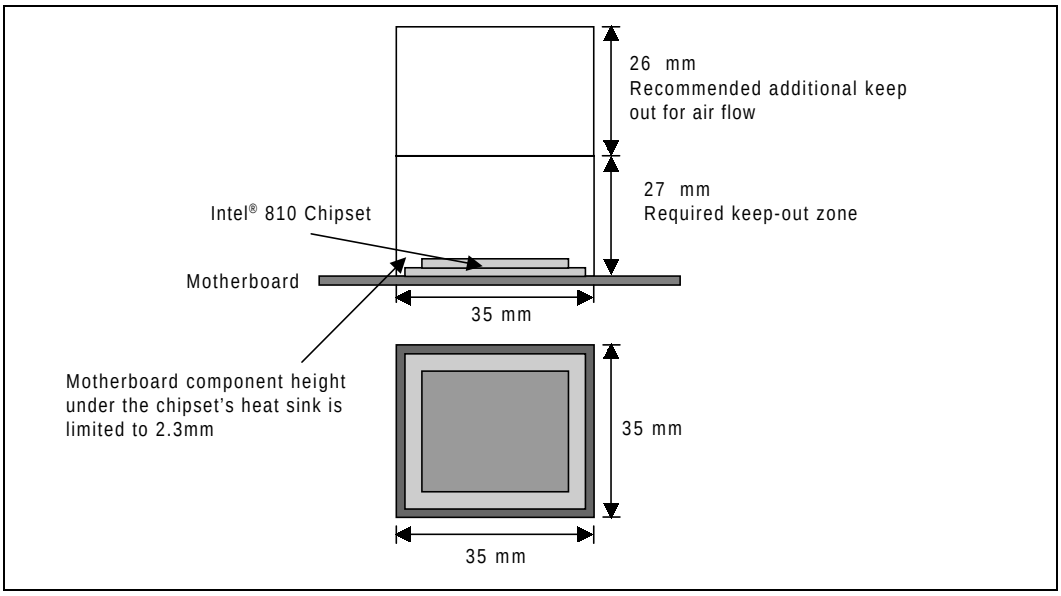
If sufficient airflow cannot be supplied to the component and motherboard, one method used to improve thermal performance is to increase the surface area of the component by attaching a metallic heat sink to the mold cap. To maximize the heat transfer, maximizing the surface area of the heat sink itself can reduce the thermal resistance from the heat sink to the air.

Note: Increasing the heat flow through the case increases the difference in temperature between the junction and case, reducing the maximum allowable case temperature.

A.1 Clearances

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width and depth constraints typically placed on the Intel® 810 chipset components are shown in Figure 10.

Figure 0-1. Extruded Heat Sink Drawing for GMCH With Socketed Processors



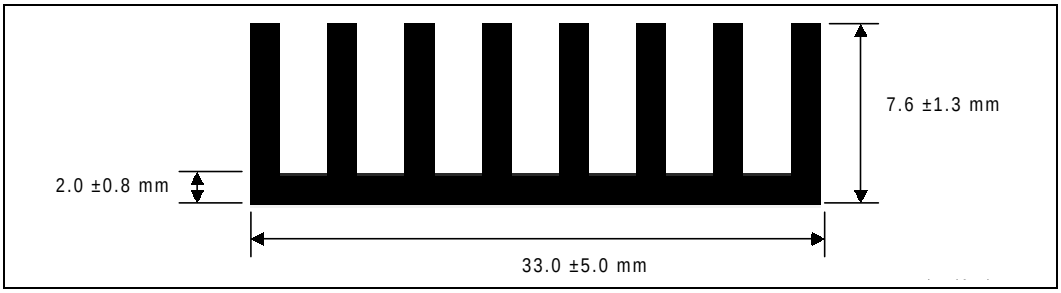
A.2 Default Thermal Solutions

For users having no control over the end-user's thermal environment or for users wanting to bypass the thermal modeling and evaluation process, Intel has developed a default thermal solution for the GMCH (discussed in the following section). The Default Thermal Solutions are designed to replicate the component thermal performance as shown in Figure 3 and Figure 4. **If, after implementing the Default Thermal Solution, the case temperature continues to exceed the appropriate value listed in Table 1, additional cooling will be required. This can typically be accomplished by improving airflow to the component or to the motherboard surrounding the component.**

A.3 Extruded Heat Sinks

An extruded heat sink is the default thermal solutions for the Intel® 810 chipset if T_{case} is exceeded and airflow improvements are not implemented. The drawing for this heat sink is shown in Figure 11. Recommended sources for the extruded heat sink are discussed in Appendix B. The weight of any of the extruded heat sinks should not exceed 25 gm.

Figure 10. Extruded Heat Sink Drawing for the GMCH



A.3.1 Attaching the Extruded Heat Sink

The extruded heat sink may be attached using clips and thermal interface (tape, grease, phase-change, etc.), epoxy or tape adhesives.

Clips

A well designed clip in conjunction with a thermal interface material (tape, grease, etc.) solution may offer the best combination of mechanical stability and reworkability. Use of a clip requires significant advance planning as mounting holes are required in the PCB. The mounting holes should be non-plated, but each must have a grounded annular ring on the solder side of the board surrounding the hole. For a typical low-cost clip, this annular ring should have an inner diameter of 150 mils and an outer diameter of 300 mils. It is recommended that this ring contain at least 8 ground connections. The solder mask opening for these holes should have a radius of 300 mils.

As clip designs are generally unique to a specific system and board layout, no procedural comments are provided.

Epoxy

Some users may prefer to implement epoxy attaches for their thermal solution. For these users, products known to be compatible with the mold cap material are listed in Appendix B. Epoxy users should plan their process carefully as once attached, the heat sink may be difficult or impossible to remove without damaging the component

For the epoxies described in Appendix B, the manufacturer's recommended attach procedure is as follows:

1. Ensure that the surface of the component and heat sink are free from contamination. Use a clean, lint-free wipe, proper safety precautions and isopropyl alcohol to ensure cleanliness.
2. Use the applicator provided by the epoxy manufacturer to apply the epoxy-activator to the mold-cap.
3. After the activator-solvent evaporates, the active ingredients will appear "wet" and will remain active for a maximum of two hours after application**. Contamination of the surface during this time prior to bonding must be avoided.**

4. Apply the adhesive to the heat sink. The amount of adhesive applied to the heat sink should be limited to the amount necessary to fill the bond and provide a small fillet.
5. Join and secure the assembly centering the heat sink on the component using a maximum pressure of 30 psi. Wait for the adhesive to set (approximately 5 minutes) before any further handling. Full cure occurs in 4–24 hours. **When applying pressure during attach, care should be taken to ensure that the motherboard is kept flat, bending or flexing the motherboard during application of the thermal solution may damage the solder joints of the Intel® 810 chipset. Excessive bending/flexing will create open joints.**

Note: The successful application of this product depends on accurate dispensing on to the parts being bonded. The manufacturer (Appendix B) offers equipment engineers to assist customers in selecting and implementing the appropriate dispensing equipment for various applications.

To remove the heat sink after the epoxy has set, the manufacturer recommends applying heat (70°C – 93°C) to the assembly. When in this temperature range, the heat sink can safely be removed from the component without damaging it.

Tape

For users who prefer to attach via tape, refer to Appendix B for the suggested manufacturer and part number. To maximize the bond line contact area and improve adhesion we recommend using two pieces of tape, one attached to the heat sink and one attached to the moldcap as shown in Figure 12, Figure 13, and Figure 14. The recommended attach procedure is at the end of this section.

Figure 11.Tape Layers (exploded diagram)

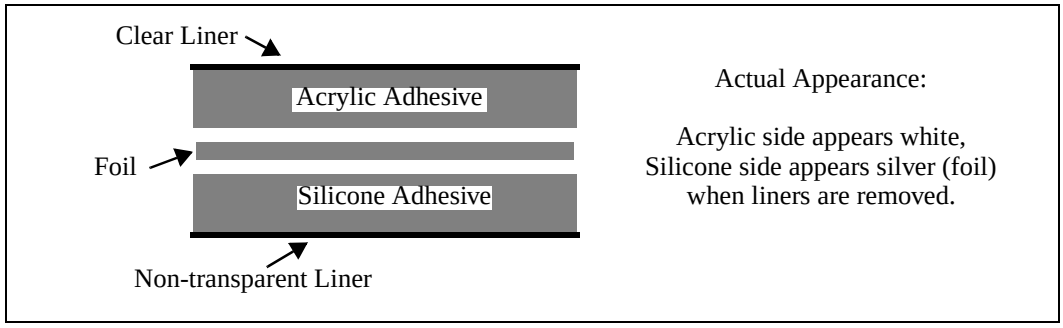


Figure 12.Attaching the Tape to the Package and Heat Sink

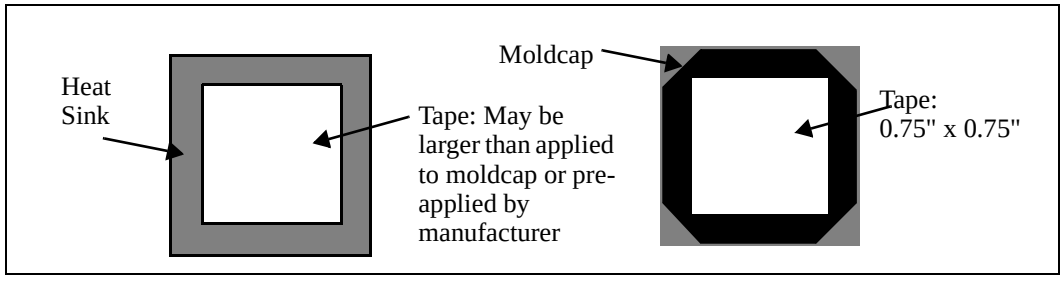
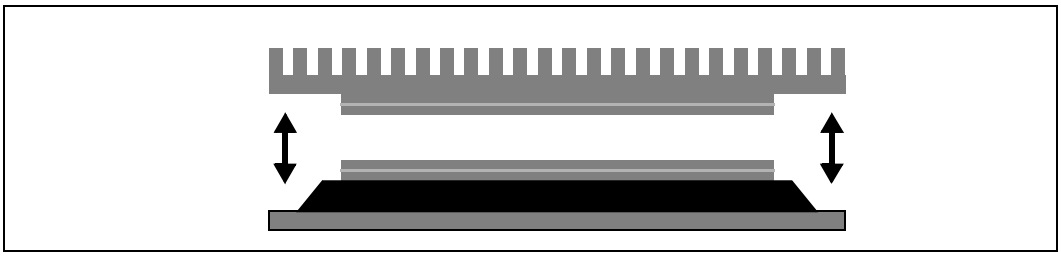


Figure 13.Completing the Attach Process



Note: Silicone adhesive always joins to either the heat sink or the mold cap, the acrylic adhesive sides must join to each other (Figure 12).

Note: As every motherboard, system and heat sink combination may introduce variance in attach strength, it is generally recommended that the user carefully evaluate the reliability of tape attaches prior to using in high volume.

For the Tape described in Appendix B the recommended two-piece attach procedure is as follows:

1. Ensure that the surface of the component and heat sink are free from contamination. Use a clean, lint-free wipe, proper safety precautions and Isopropyl Alcohol to ensure cleanliness.
2. Cut tape to size. Suggestions for the appropriate size can be seen in Figure 13.
3. Heat sink side: Remove the non-transparent liner. You will see foil underneath (Figure 12). Apply the tape to the center of the heat sink and smooth over the entire surface using moderate pressure. **There should be no air bubbles under the tape.**
4. Component side: Remove the non-transparent liner. You will see foil underneath (Figure 12). Apply the tape to the center of the mold cap and smooth over the entire surface using moderate pressure. **There should be no air bubbles under the tape.**
5. Both sides: Remove the clear liners from each side, center the heat sink over the component and apply using any one of the manufacturer's recommended temperature/pressure options shown in Table 6. **When applying pressure during attach, care should be taken to ensure that the motherboard is kept flat, bending or flexing the motherboard during application of the thermal solution may damage the solder joints of the Intel® 810 chipset. Excessive bending/flexing will create open joints.**

Table 6. Tape Attach Application Temperature/Pressure Options (Not To Be Exceeded)

Pressure	Temperature	Time
10 psi (0.069 mPa)	22°C	15 seconds
30 psi (0.207 mPa)	22°C	5 seconds
10 psi (0.069 mPa)	50-65°C	5 seconds
30 psi (0.207 mPa)	50-65°C	3 seconds

Note: Approximately 70% of the ultimate adhesion bond strength is achieved with initial application, 80%–90% of the ultimate adhesion bond is achieved within 15 minutes and ultimate adhesion strength is achieved within 36 hours.

Reliability

As every motherboard, system, heat sink and attach-process combination may introduce variance in attach strength, it is generally recommended that the user carefully evaluate the reliability of the completed assembly prior to use in high volume. Some test recommendations can be seen in Table 7.

Table 7. Reliability Validation

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	50G, board level 11 msec, 3 shocks/direction	Visual Check
Random Vibration	7.3 G, board level 45 minutes/axis, 50 to 2000 Hz	Visual Check
Temperature Life	85°C, 2000 hours total, checkpoints occur at 168, 500, 1000 and 2000 hours	Visual Check
Thermal Cycling	-5°C to +70°C 500 Cycles	Visual Check
Humidity	85% relative humidity 55°C, 1000 hours	Visual Check

NOTES:
1. The above tests should be performed on a sample size of at least 12 assemblies from 3 lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

A.4 Thermal Interface Management for Heat-Sink Solutions

For solutions where a heat sink is preferred, to optimize the heat sink design for the Intel® 810 chipset, it is important to understand the impact of factors related to the interface between the mold-cap and the heat sink base. Specifically, the bond line thickness, interface material area and interface material thermal conductivity should be managed to realize the most effective heat-sink solution.

A.4.2 Bond Line Management

The gap between the mold-cap and the heat sink base will impact heat-sink solution performance. The larger the gap between the two surfaces, the greater the thermal resistance. The thickness of the gap is determined by the flatness of both the heat sink base and the mold-cap, plus the thickness of the thermal interface material (e.g., PSA, thermal grease, epoxy) used between these two surfaces.

The Intel® 810 chipset mold cap planarity is specified as 0.006 inches maximum.

A.4.3 Interface Material Performance

Two factors impact the performance of the interface material between the thermal plate and the heat sink base:

- Thermal resistance of the material
- Wetting/filling characteristics of the material

Thermal resistance describes the ability and ease of the thermal interface material to transfer heat from one surface to another. The higher the thermal resistance, the less efficient an interface is at transferring heat. The thermal resistance of the interface material has a significant impact on the thermal performance of the overall thermal solution. A high thermal resistance requires a larger temperature drop across the interface; thus, the thermal solution needs to be more efficient.

The wetting/filling characteristics of the thermal interface material is its ability to fill the gap between the case and the heat-sink. Since air is an extremely poor thermal conductor, the more completely the interface material fills the gaps, the lower the temperature drop across the interface.

Appendix B Heatsink and Attach Suppliers

Table 8. Extruded Heat Sink Sales Locations

Supplier	Part Number	Comment
Thermalloy*	22372B	http://www.thermalloy.com/catalog/htm/eprof13b.htm#19044
Aavid*	634553 B 01299	http://www.aavid.com/html/atp.html

Table 9. Attach Sales Locations

Supplier	Part Number	Comment
Epoxy*	383 or 384	http://www.loctite.com Select the country of your choice and Select “Products for the Electronics Industry”.
Chomerics Tape	T-410	For Tape, please go to: http://www.chomerics.com/locate

Appendix C System Based Thermal Assumptions

As mentioned in earlier sections, the majority of the thermal power dissipated by the chipset typically flows into the motherboard to which it is mounted (when thermal or center balls are present). The size of the board is a key factor in determining the amount of heat which the package may dissipate. In the course of comparing JESD/JEDEC derived data to data derived from system-level testing, the effect of the larger board used for a typical motherboard was profound. To reconcile the differences and provide more realistic data to the customer, Intel has adopted a system-based thermal simulation and test methodology. Figure 15 and Figure 16 depict the system based model for the Intel® 810 chipset.

The assumptions in the system-based model shown in Figure 15 and Figure 16 are:

- 4L 1oz. Board (6X6”) Thermal Dissipation Area
- Processor does not dissipate any heat to MB
- Airflow is parallel to the MB
- Airflow and ambient are measured at 1” above the MB and 1” upstream from the GMCH center
- Processor HS modeled for airflow restriction only.

Figure 14. Airflow/Ambient Reference Point—Front View

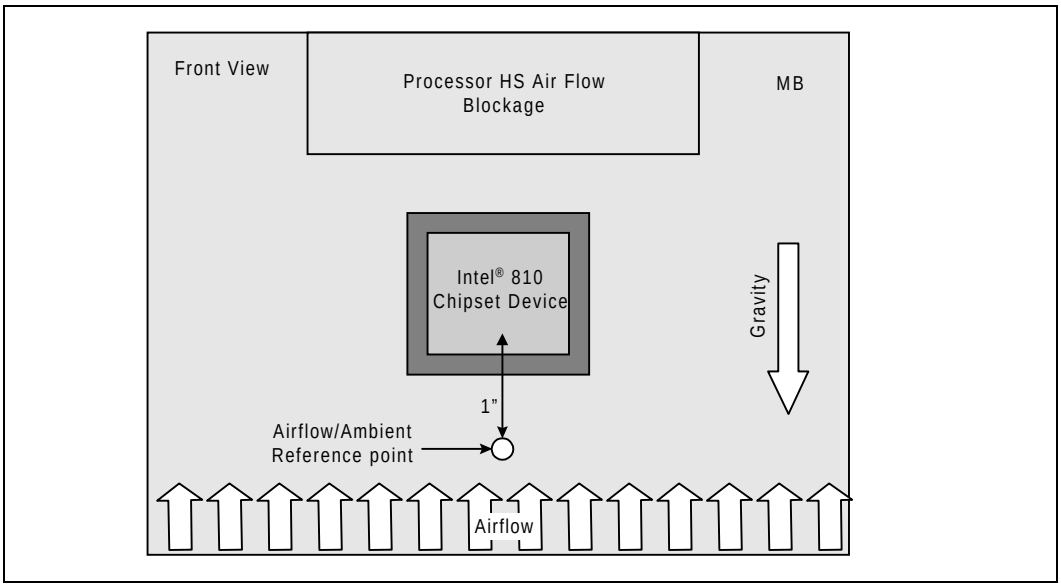
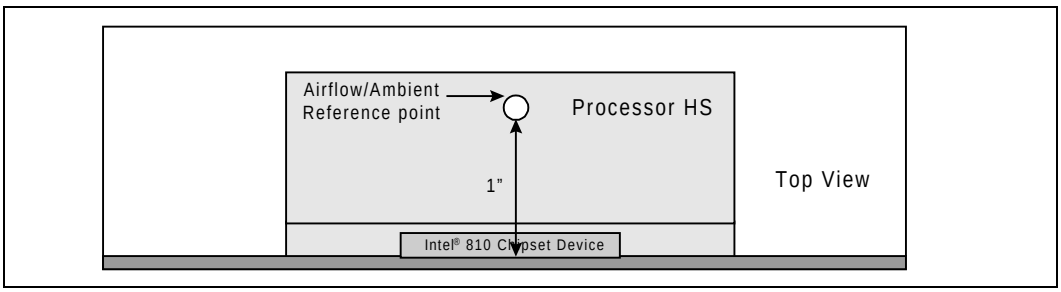


Figure 15. Airflow/Ambient Reference Point—Top View



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