# Intel® 440GX AGPset

## Design Guide Update

***May 1999***

Order Number: 290660-001

# Contents

# Revision History

| Rev. | Draft/Changes | Date |
|---|---|---|
| 001 | Initial Release | May 1999 |

# Preface

This document is an update to the specifications contained in the Intel® 440GX AGPset Design Guide Rev 1.0, March 1999, order number 290651-001.

References may also be made to the following documents: the Intel® 440GX AGPset: 82443BX Host Bridge Controller data sheet, order number 290638-001, and the 82371AB (PIIX4) data sheet section of the Platform Components databook, order number 296467-009.

It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. This design guide is primarily targeted at the PC market segment and was first published in 1999. Those using this design guide should check for device availability before designing in any of the components included in this document

## Nomenclature

**General Design Considerations** includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 82440GX AGPset.

**Schematic, Layout and Routing Updates** include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

**Documentation Changes** include suggested changes to the current published design guide not including the above.

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel® 440GX AGPset stepping. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### Codes Used in Summary Table

| | |
|---|---|
| Doc: | Document change or update that will be implemented. |
| Shaded: | This item is either new or modified from the previous version of the document. |

| NO. | Plans | GENERAL DESIGN CONSIDERATIONS |
|---|---|---|
| 1 | Doc | Implementing a RESET BUTTON for 440GX Based Systems |
| 2 | Doc | PCIRST# Load Sensitivity on PIIX4/PIIX4E |
| 3 | Doc | SPD EEPROM Write Protection. |
| 4 | Doc | Execute the WBINVD Instruction to Save Cache State to Memory Before Initiating an S2 or S3 Sleep State. |
| 5 | Doc | SLP# Connectivity in Multi-processor Systems. |

| NO. | Plans | SCHEMATIC, LAYOUT AND ROUTING UPDATES |
|---|---|---|
| 1 | Doc | Guidelines to minimize ESD events that may cause loss of CMOS contents is added. |
| 2 | Doc | Correct Strapping for SMC FDC37C932FR Ultra IO device VBAT pin. |

| NO. | Plans | DOCUMENTATION CHANGES |
|---|---|---|
| | | There are currently no known documentation changes. |

# General Design Considerations

## 1. Implementing a RESET BUTTON for Desktop Based Systems

The following should be considered when implementing a RESET BUTTON for 440GX based systems:

The system reset button has typically been connected indirectly to the PWROK input of the PIIX4/PIIX4E. This technique will not reset the suspend well logic, which includes the SMBus Host and Slave controllers. To reset the hardware in the suspend well, the reset button should be connected to the RSMRST# input of the PIIX4/PIIX4E. Assertion of RSMRST#, via a reset button, will result in a complete system reset. RSMRST# assertion will cause SUS[A-C]# to assert which results in the deassertion of PWROK if SUS[A-C]# controls the power supply PS-ON control signal. The deassertion of PWROK will cause the PIIX4/PIIX4E to assert PCIRST#, RSTDRV, and CPURST.

## 2. PCIRST# Load Sensitivity on PIIX4/PIIX4E

A specific board sensitivity has been identified by PCD that may result in a low going glitch on a deasserted PCIRST# signal when it is lightly loaded. This glitch may occur as a result of VCC droop caused by simultaneous switching of most/all AD[31:0] signals from 0 to 1. This glitch can in some designs be low enough (below 1.7V) to interfere with proper operation of the Host PCI Bridge Controller component.

This sensitivity manifests itself on designs where PCIRST# is lightly loaded with less than approximately 50pF, or is not driving the entire PCI bus. Design features that could aggravate the problem are; an in-line active component on the PCIRST# signal, such as an AND gate or, lack of a series termination resistor on the PCIRST# signal at the PIIX4 or PIIX4E.

There are several improvements that can be implemented individually or in any combination. First, a series termination resistor between 22 and 33 ohms placed close to the PIIX4/PIIX4E will help reduce the glitch. Second, an external capacitor of approximately 47pF will help reduce the glitch. Third, if the design currently uses an in-line active gate/buffer on PCIRST# to drive the PCI bus, consider removal of this gate/buffer entirely. The PIIX4/PIIX4E is designed to drive the entire PCI bus.

## 3. SPD EEPROM Write Protection

The PC SDRAM Unbuffered DIMM Specification, Rev 1.0, dated Feb 1998, shows pin 81 of the DIMM module is the WP (write protect) pin for the SPD EEPROM. The block diagrams show there is a 47K pull-down resistor tied to the WP pin. This allows the DIMM manufacturers to write SPD data to the EEPROM.

An OEM may wish to use the SPD EEPROM to write information into the DIMMs at production for system level checkout to identify the DIMM installed as being shipped with the system. For this reason, the OEM may wish to include some logic to control the level on pin 81 of the DIMM modules so that after the DIMM is tagged, they can be write protected again. If this pin is pulled high on the motherboard, the DIMM SPD EEPROM is write protected.

Pin 81 of the DIMM sockets on the 82440GX reference schematics are shown as “NC”, no connects. If an OEM wishes to write protect the SDRAM SPD EEPROMS, then these pins should be pulled high.

## 4. Execute the WBINVD Instruction to Save Cache State to Memory Before Initiating an S2 or S3 Sleep State

If a system design requires that the hardware platform be capable of flushing the processor caches, then FLUSH# must be asserted a minimum of one BSCLCK before STPCLK#. Power management software should perform a WBINVD on each processor for the S2 and S3 sleep states. Flushing the cache on each processor is not necessary for the S1 sleep state.

## 5. SLP# Connectivity in Multi-processor Systems

For multi-processor systems using the PIIX4/PIIX4E, the SLP# signal may be asserted to one of the processors before it is in a processor sleep state 3, and therefore not yet acknowledged. This could result in a wakeup problem.

Specifically, For PIIX4/PIIX4E based platforms, STPCLK# from the PIIX4E is connected to all processors, and SLP# from the PIIX4E is connected to all processors. The following sequence occurs:

1) OS writes to PMCNTRL register

2) PIIX4E asserts STPCLK#, then waits for Stop Grant

3) The processor acknowledges with a Stop Grant Acknowledge

4) PIIX4E asserts SLP# after receiving Stop Grant Acknowledge

While this sequence works for uni-processor systems, processors are put into Processor Sleep State 3, not State 5, during ACPI S1 state. This means that the SLP# signal *must not be connected* to any processor in multi-processor systems.

Note that disabling the SLEEP_EN bit in the PIIX4E Processor Control register is not an accecptable workaround for this issue since this bit only controls SLP# assertion in C3 state, not in S1 state.

# Schematic, Layout and Routing Updates

## 1. Guidelines to Minimize ESD Events That May Cause Loss of CMOS Contents

Recommendations for New Board Designs:

1) Provide a 1uF X5R dielectric, monolithic, ceramic capacitor between the VCCRTC pin of the PIIX4/PIIX4E and the ground plane. This capacitor's positive connection should not be stubbed off the trace run and must be as close as possible to the PIIX4/PIIX4E. The capacitor must be no further than 0.5 inch from the PIIX4/PIIX4E. If a stub is required, it should be kept to a few mm maximum length. The ground connection should be made through a via to the ground plane, with no or minimal trace between the capacitor pad and the via.

2) Place the battery, 1K Ohm series current limit resistor, and the common-cathode isolation diode very close to the PIIX4/PIIX4E. If this is not possible, place the common-cathode diode and the 1K Ohm resistor as close to the 1uF capacitor as possible. Do not place these components between the capacitor and the PIIX4. The battery can be placed remotely from the PIIX4/PIIX4E.

3) On boards that have chassis-intrusion utilizing external logic powered by the VCCRTC pin, place the inverters as close to the common-cathode diode as possible. If this is not possible, keep the trace run near the center of the board.

4) Keep the PIIX4/PIIX4E VCCRTC trace away from the board edge. If this trace must run from opposite ends of the board, keep the trace run towards the board center, away from the board edge where people and equipment that handle the board could make contact.

Recommendations for Existing Board Designs:

1) The effectiveness of adding a 1uF capacitor, as identified above, needs to be determined by examining the routing and placement. For example, placing the capacitor far from the PIIX4 reduces its effectiveness.

## 2. Correct Strapping for SMC FDC37C932FR Ultra IO Device VBAT Pin

When the PIIX4/PIIX4E internal RTC is used, the SMC Ultra IO device, FDC37C932FR, VBAT pin must be connected to ground through between a 1K and 0 ohm  pull-down resistor.

# Documentation Changes

There are currently no known documentation changes.

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