Intel® 820 Chipset Design Guide Addendum

For the Intel® Pentium® III Processor for the PGA370 Socket

Addendum to the Intel® 820 Chipset Design Guide

April, 2000

Order Number: 298178 - 002

Contents

Figures

Tables

Revision History

Rev.	Description	Date
-001	• Initial Release	February, 2000
-002	• Some uni-processor pins changed to ground • Updated trace lengths for Non-AGTL+ Signals • Updated keep-out area requirements for certain processors	April, 2000

Preface

This document is an update to the guidelines contained in the Intel® 820 Chipset Platform Design Guide Revision 1.0 (Order Number: 290631-00x).

1. Introduction:

The Intel® Pentium® III processor in the FC-PGA package is the next member of the P6 family, in the Intel® IA-32 processor line. The processor uses the same core and offers the same performance as the Intel® Pentium® III processor S.E.C.C. 2 processor, but utilizes a new package technology called flip-chip pin grid array, or FC-PGA. This package utilizes the same 370-pin zero insertion force socket (PGA370) used by the Intel® Celeron$_{TM}$ processor. Thermal solutions are attached directly to the back of the processor core package without the use of a thermal plate or heat spreader.

1.1. Intel® Pentium® III Processor for the PGA370 Socket – Layout Guidelines

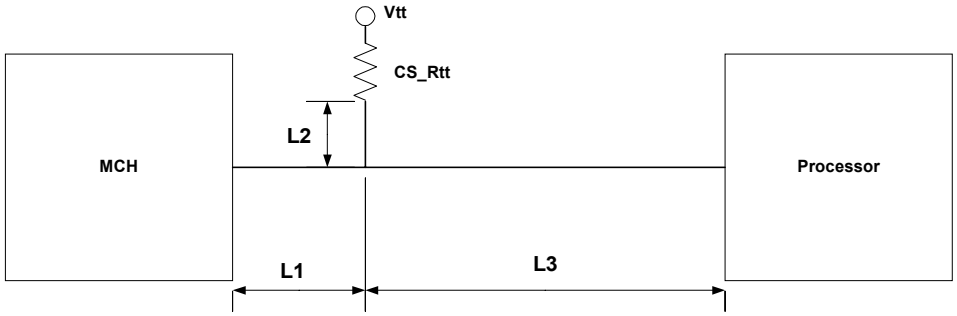
The Intel® Pentium® III processor for the PGA370 socket is the next generation Intel® Pentium® III processor. The differences between the PGA370 and SECC2 design implementations are detailed in this addendum. The PGA370 design requires additional termination at the chipset for the AGTL+ signals. In addition, the platform power delivery requirements are different for the PGA370 design compared to the SECC2 design. AGTL+ layout considerations detailed in the Intel® 820 Chipset Design Guide still apply to FC-PGA designs (including ground referencing the AGTL+ signals).

1.1.1. 100/133MHz System Bus (Uni-Processor Configuration)

The following layout guidelines support platform designs with the Intel® Pentium® III processor for the PGA370 socket and the Intel® 820 chipset.

The recommended solution covers system bus speeds of 100 MHz and 133 MHz. The solution proposed in this section requires the motherboard design to terminate the AGTL+ system bus at the chipset. The additional termination at the chipset improves signal integrity by reducing reflections from the MCH.

First, determine the approximate location of the processor and the chipset on the motherboard. An example topology is shown in the Figure 1. Table 1 provides segment descriptions and length recommendations for the topology shown. The end of a segment length is defined at the pin of a device or component. Refer to section 1.1.20 for clock routing guidelines. Figure 2 and Figure 3 show an example of routing the chipset termination.



Intel® Pentium® III processor:	CPU_Rtt = 62 Ω +/- 15% on processor die
CS_Rtt:	Chipset Termination to Vtt = 62 Ω +/- 2%
L1:	Chipset Stub - Length to termination stub
L2:	Termination Length
L3:	Motherboard Trace Length
L(1,2,3):	Zo = 60 Ω+/- 15%

Figure 1: Intel® Pentium® III processor FCPGA (Uni-Processor Configuration)

Segment	Description	Min Length (inches)	Max Length (inches)
L1	Chipset Stub Length	0.50	0.85
L2	Chipset Termination Length	0.00	0.50
L3	Motherboard Trace Length	2.50	4.50

Table 1: Segment Descriptions and Lengths for Figure 1

The resistor packs are on the component side of the motherboard. They are shown in Figure 2 to indicate their relative location to the MCH. The AGTL+ signals are routed on the bottom layer for this example.

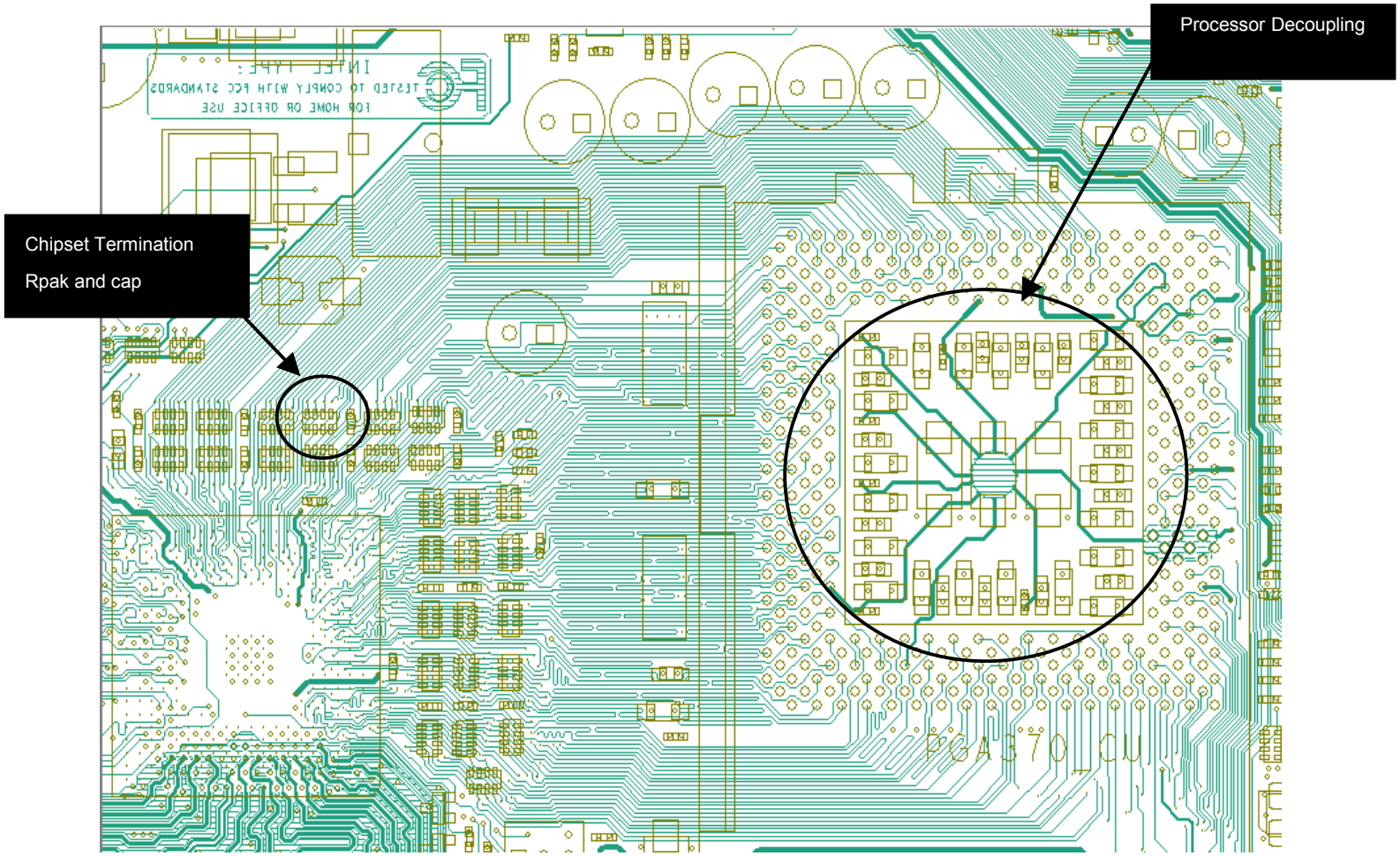


Figure 2: Chipset Termination Example (Bottom Side)

The blue line indicates the cut in the power layer. Ground referencing is required for the AGTL+ signals.

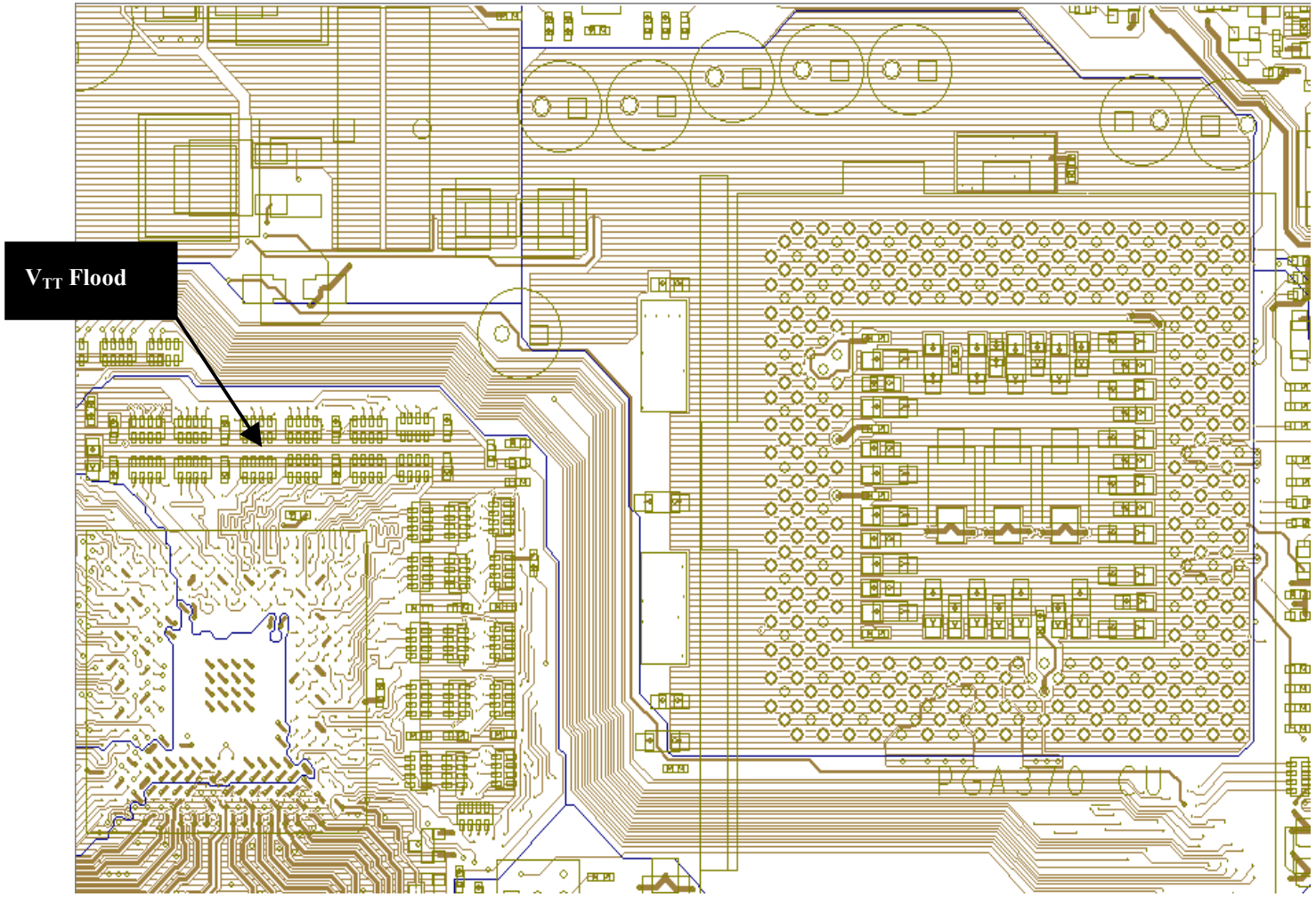


Figure 3: Chipset Termination Example (Component Side)

1.1.2. 100/133MHz System Bus (Dual-Processor Configuration)

The following layout guidelines support platform designs with the Intel® Pentium® III processor for the PGA370 socket and the Intel® 820 chipset. The recommended solution covers system bus speeds of 100 MHz and 133 MHz

First, determine the approximate location of the processors and the chipset on the motherboard. Table 2 provides segment descriptions and length recommendations for the topology shown in Figure 4. The end of a segment length is defined at the pin of a device or component. Refer to section 1.1.20 for clock routing guidelines

CPU stub lengths of the same net (CPUlen in Figure 4) must be length matched within 25mils (+/- 12.5 mils).

The AGTL+ signals should be routed as 5 mil traces on 15 mil spacing with a manufacturing tolerance of 60 Ω +/- 10%.

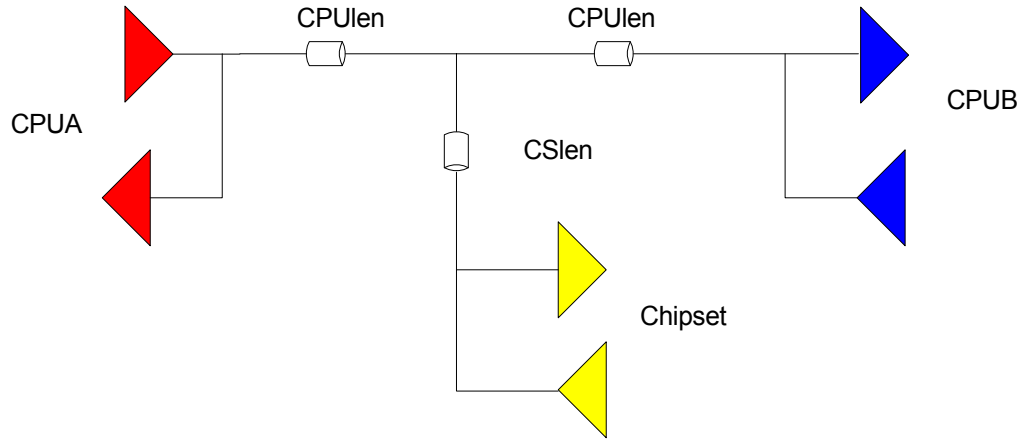


Figure 4: Intel® Pentium® III Processor FCPGA (Dual-Processor Configuration)

Parameter	Minimum	Maximum
CPUlen	2.5 inches	3.5 inches
CSlen	2.25 inches	2.5inches

Table 2: Segment Descriptions and Lengths for Figure 4

1.1.3. Intel® 820 Chipset (PGA370) Processor Checklist

This checklist supports Intel® Pentium® III processors utilizing the FC-PGA package.

AGTL+	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
A[35:3]#	Connect to MCH (A[31:3]#) and terminate to Vtt with 62 ohms (+/- 2%). Leave A[35:32]# as N/C (not supported by chipset)	Connect A[31:3]# to second processor. Termination is not required. Leave A[35:32]# as N/C.
ADS#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
AERR#	Leave as N/C (not supported by chipset)	Leave as N/C
AP[1:0]#	Leave as N/C (not supported by chipset)	Leave as N/C
BERR#	Leave as N/C (not supported by chipset)	Leave as N/C
BINIT#	Leave as N/C (not supported by chipset)	Leave as N/C
BNR#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
BP[3:2]#	Leave as N/C	Leave as N/C
BPM[1:0]	Leave as N/C	Leave as N/C
BPRI#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
BR0#	Pull-down to GND with 10Ω resistor	For arbitration ID, tie BR0# of CPU0 to BR1# of CPU1 and tie BR1# of CPU0 to BR0# of CPU1. Refer to the Intel® 820 Chipset Design Guide for additional information (Order Number 290631-00x).
BR1#	Leave as N/C	
D[63:0]#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
DBSY#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
DEFER#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
DEP[7:0]#	Leave as N/C	Leave as N/C
DRDY#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
HIT#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
HITM#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
LOCK#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
REQ[4:0]#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.

AGTL+	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
RESET#	86 ohm pullup to Vtt tied to 22 ohm series resistor to a 10 pF cap to ground, connect to MCH and connect to ITP (RESET#) with 240Ω series resistor. MCH requires an 86 ohm pullup to Vtt. Refer to Figure 12.	Connect CPU0 to Vtt or Vcmos with 56ohm +/-5% Connect CPU1 to Vtt or Vcmos with 56 ohm +/-5% tied to a 10 pF cap to ground, Refer to Figure 13.
RESET2#	Driven by same signal as RESET# (see Figure 12 for recommended topology)	For DP configurations, connect pin X4 (RESET2#) to ground on CPU0 and CPU1.
RP#	Leave as N/C (not supported by chipset)	Leave as N/C
RS[2:0]#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.
RSP#	Leave as N/C (not supported by chipset)	Leave as N/C
TRDY#	Connect to MCH and terminate to Vtt with 62 ohms (+/- 2%)	Connect to MCH and both processors, termination is not required.

Note: The CMOS and TAP checklists below are specific to platforms using the Intel® 820 Chipset and the PGA370 Intel® Pentium® III processor. V_{TT} and VCC_{CMOS} are the same voltage on an Intel® 820 chipset based platform.

CMOS	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
A20M#	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH	Connect to 2nd processor
FERR#	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH	Connect to 2nd processor
FLUSH#	150Ω pull-up to VCC_{CMOS} or V_{TT}. (Not supported by the chipset)	Connect to 2nd processor
IERR#	Leave as N/C (not supported by chipset)	Connect to 2nd processor
IGNNE#	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH	Connect to 2nd processor
INIT#	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH and FWH	Connect to 2nd processor
LINT0/INTR	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH	Connect to 2nd processor
LINT1/NMI	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH	Connect to 2nd processor
PICD[1:0]	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH	Two 300-330Ω pull ups to VCC_{CMOS} or V_{TT} located at each end of the trace. Connect to CPU0 and CPU1.
PREQ#	Connect to ITP (PREQ0#) with 200-330Ω pull-up to VCC_{CMOS} or V_{TT}	Connect to ITP (PREQ1) with 200-330Ω pull-up to VCC_{CMOS} or V_{TT}
PWRGOOD	Connect to ICH (CPUPWRGD) with 150-330Ω pull-up to $VCC_{2.5}$	Connect to 2nd processor
SLP#	150Ω pull-up to VCC_{CMOS} or V_{TT}. Connect to ICH	Connect to 2nd processor

CMOS	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
SMI#	Connect the CPU to the 56Ω series resistor to 330Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT} and 100pF to ground. Connect to ICH through 33Ω resistor. Refer to Figure 6.	Daisy chain to CPU0 with matching stub lengths. Refer to Figure 7.
STPCLK#	150Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT}. Connect to ICH	Connect to 2nd processor
THERMTRIP#	Connect to power-off logic or ASIC with 150Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT}, or leave as N/C	Connect to 2nd processor

TAP	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
PRDY#	Connect to ITP (PRDY0#) with 240Ω series resistor and 150Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT} (series resistor needs to be placed next to the debug port with the termination resistor on the processor side)	Connect to ITP (PRDY1#) with 240Ω series resistor and 150Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT} (series resistor needs to be placed next to the debug port with the termination resistor on the processor side)
TCK	Connect to ITP (TCK) with 47Ω series resistor and 1kΩ pull-up to $V_{CC_{CMOS}}$ or V_{TT}	Each processor should receive a separately buffered copy of TCK from the ITP. See Figure 5 for the recommended Bessel filter.
TDO	Connect to ITP (TDO) with 150Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT}	Connect to ITP (TDI) with 200Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT}.
TDI	Connect to ITP (TDI) with 200-330Ω pull-up to $V_{CC_{CMOS}}$ or V_{TT}	TDI of CPU0 is connected to the ITP (TDI). TDI of CPU1 is connected to TDO of CPU0. Pull-up both sets of TDI/TDO nets as described.
TMS	Connect to ITP (TMS) with 47Ω series resistor and 1kΩ pull-up to $V_{CC_{CMOS}}$ or V_{TT}	Each processor should receive a separately buffered copy of TMS from the ITP. See figre 5 for the recommended Bessel filter.
TRST#	Connect to ITP (TRST#) with ~680Ω pull-down to GND	Connect to 2nd processor

CLOCK	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
BCLK	Connect to CK133 with 22-33Ω series resistor (based on clock driver characteristics) To reduce pin-to-pin skew, tie all host clock outputs together at the clock driver then route to the MCH and processors	Use separate BCLK from TAP and CPU0, or use ganged clock. Terminate as described. To reduce pin-to-pin skew, tie all host clock outputs together at the clock driver then route to the MCH and processors.
PICCLK	Connect to CK133 with 22-33Ω series resistor (based on driver characteristics)	Use separate PICCLK from CPU0. Terminate as described.

POWER /OTHER	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
BSEL0	Connect to ICH (VRMPWRGD) with 220Ω pull-up to 3.3V	Connect to 2nd processor
BSEL1	Connect to CK133 (133/100#) with 220Ω pull-up to 3.3V and connect to MCH (HL10) with 8.2kΩ series resistor	Connect to 2nd processor
CLKREF	Connect to 1.25V through a resistor divider using two 1% tolerant resistors (see Figure 11)	Connect the same as CPU0
CPUPRES#	Connect to PWRGOOD logic (to prevent system from powering up if no processor is present), GND, or leave as N/C If used, 1k–10kΩ pull-up to any voltage	Connect the same as CPU0
EDGCTRL	Leave as N/C	Leave as N/C
PLL1, PLL2	Connect to LC low pass filter (see Figure 15)	Connect the same as CPU0
RTTCTRL	Pull-down to GND with 62Ω ± 1% resistor	Pull-down to GND with 62Ω ± 1% resistor
SLEWCTRL	Pull-down to GND with 110Ω ± 1% resistor	Pull-down to GND with 110Ω ± 1% resistor
$V_{CC1.5}$	Connect to 1.5V regulator	Connect the same as CPU0
$V_{CC2.5}$	Leave as N/C	Leave as N/C
V_{CCCMOS}	Used as pull-up voltage source for CMOS signals between processor and chipset and for TAP signals between processor and ITP. Must have some decoupling (HF/LF) present. Decouple with a minimum of one 0.1µF capacitor	Connect the same as CPU0
V_{CCCORE}	Connect to VRM 8.4 voltage regulator and provide low and high frequency decoupling (see section 1.1.19)	Connect the same as CPU0
$V_{CORE_{DET}}$	Connect to PWRGOOD logic (to prevent system from powering up if an Intel® Celeron™ processor is installed), GND, or leave as N/C	Connect the same as CPU0
V_{REF}	Connect to 1.0V through a resistor divider (75Ω ± 1% and 150Ω ± 1% resistors) to V_{TT} Decouple with a minimum of four 0.1µF capacitors placed within 500mils of V_{REF} pins.	Connect the same as CPU0
VID[3:0]	Connect to core voltage regulator (may require 10kΩ pull-up if regulator does not have internal pull-ups) Optional override (jumpers, ASIC, etc) could be used for debug purposes May also connect to system monitoring device	Connect the same as CPU0

POWER /OTHER	CPU PIN CONNECTION – CPU0 (Uni-Processor Configuration)	CPU PIN CONNECTION – CPU1 (Dual-Processor Configuration)
V_{TT}	Connect to 1.5V regulator and provide high and low frequency decoupling. Connect all 15 V_{TT} pins on Intel® 820 chipset based designs. . In addition, tie RESERVED Pin G37 to V_{TT} for platforms using the Pentium III processor based on the cA2 stepping. Refer to the Pentium III processor specification update for stepping details.	Connect to 1.5V regulator and provide high and low frequency decoupling. Connect all 15 V_{TT} pins on Intel® 820 chipset based designs. In addition, tie RESERVED Pin G37 to V_{TT} for platforms using the Pentium III processor based on the cA2 stepping. Refer to the Pentium III processor specification update for stepping details. Reserved Vtt pins: AA33, AA35, AN21, E23, S33, U35, U37, X2
RESERVED	The following pins must be left as no-connects: AK30, F10, L33, N33, N35, N37, Q33, Q35, Q37, R2, W35, X2, and Y1 Note: In DP configurations, pin X2 is BR1# and needs to be connected to CPU1. Note: pins AJ3, AL1, and AN3 should now be connected to ground	The following pins must be left as no-connects: AK30, F10, L33, N33, N35, N37, Q33, Q35, Q37, R2, W35, and Y1

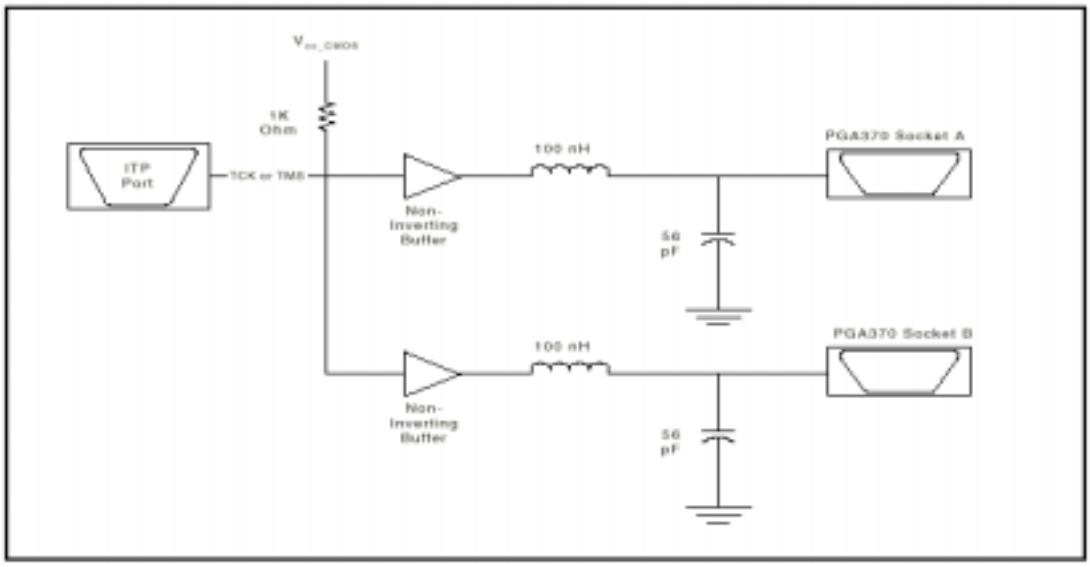


Figure 5: TCK/TMS Implementation Example for DP Designs

1.1.4. Motherboard Layout Rules for AGTL+ Signals

AGTL+ layout considerations detailed in the Intel® 820 Chipset Design Guide and the Intel® 820 Chipset Platform Design Guide Update 1.xx apply to PGA370 designs.

Special Considerations:

1) Ground Reference

It is strongly recommended that AGTL+ signals be routed on the signal layer next to the ground layer (referenced to ground). It is Important to provide effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane.

2) Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase Overshoot/Undershoot due to significantly increased inductance. If signals must cross a split in a reference plane, add a decoupling capacitor to stitch the planes together to remove the discontinuity in the return path.

3) CPU Connector Breakout

It is strongly recommended that AGTL+ signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the connector on the same layer. If routing is tight, breakout from the connector on the opposite routing layer over a ground reference and cross over to a main signal layer near the CPU connector.

Note: Following the above layout rules and the guidelines in the Intel® 820 Chipset Platform Design Guide are critical for AGTL+ signal integrity, particularly for the 0.18micron process technology

Failure to satisfy the special considerations listed above may cause severe SSO effects, including failures due to signal quality and timing violations.

1.1.5. Motherboard Layout Rules for Non-AGTL+ (CMOS) Signals

Non-AGTL+ (CMOS) Signals

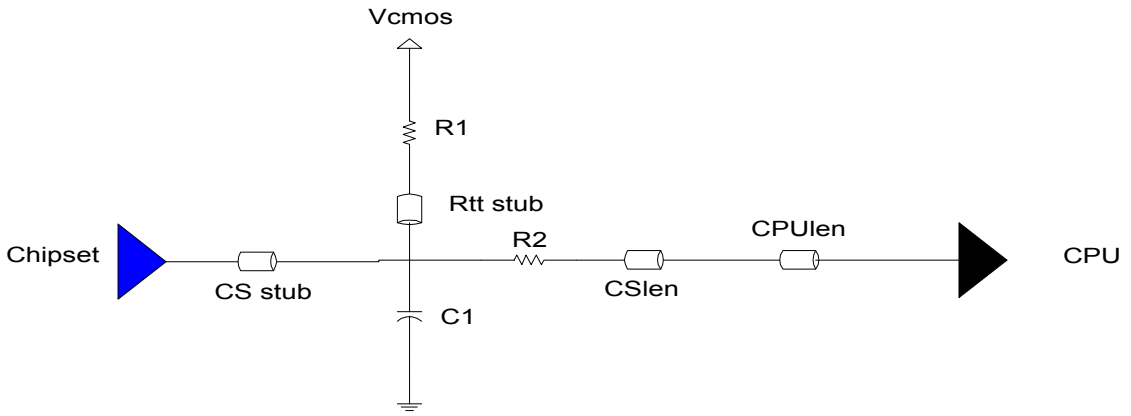
Route these signals on any layer or any combination of layers.

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 9”
FERR#	5 mils	10 mils	1” to 9”
FLUSH#	5 mils	10 mils	1” to 9”
IERR#	5 mils	10 mils	1” to 9”
IGNNE#	5 mils	10 mils	1” to 9”
INIT#	5 mils	10 mils	1” to 9”
LINT[0] (INTR)	5 mils	10 mils	1” to 9”
LINT[1] (NMI)	5 mils	10 mils	1” to 9”
PICD[1:0]	5 mils	10 mils	1” to 9”
PREQ#	5 mils	10 mils	1” to 9”
PWRGOOD	5 mils	10 mils	1” to 9”
SLP#	5 mils	10 mils	1” to 9”
STPCLK	5 mils	10 mils	1” to 9”
THERMTRIP#	5 mils	10 mils	1” to 9”

Table 3: Routing Guidelines for Non-AGTL+ Signals

1.1.6. SMI# Layout Guidelines (Uni-Processor)

Designs should follow the additional guidelines in Figure 6 to reduce or eliminate the probability of a spurious SMI# assertion.



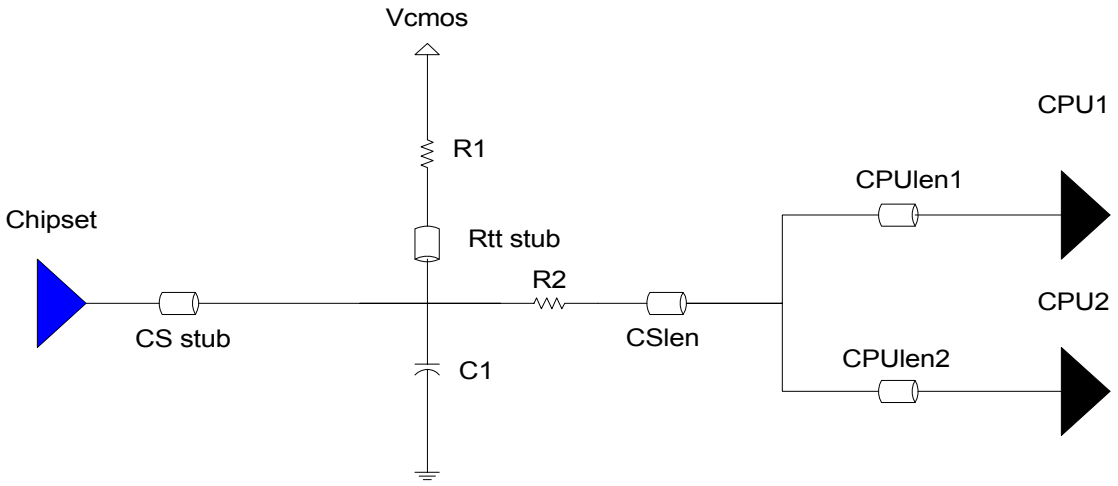
Parameter	Minimum	Maximum
CS stub	0.25"	1.5"
Rtt stub	0"	1.5"
CSlen	0.25"	10"
CPUlen1	0.25"	10"
CPUlen2	0.25"	10"

Parameter	Value	Tolerance
R1	330 Ω	+/- 5%
R2	33 Ω	+/- 5%
C1	100 pF	+/- 5%

Figure 6: SMI# Routing Guidelines (Uni-Processor)

1.1.7. SMI# Layout Guidelines (Dual-Processor)

Dual processor designs should follow the additional guidelines in Figure 7 to reduce or eliminate the probability of a spurious SMI# assertion.



Parameter	Minimum	Maximum
CS stub	0.25"	1.5"
Rtt stub	0"	1.5"
CSlen	0.25"	10"
CPUlen1	0.25"	10"
CPUlen2	0.25"	10"

Parameter	Value	Tolerance
R1	330 Ω	+/- 5%
R2	33 Ω	+/- 5%
C1	100 pF	+/- 5%
Trace Spacing	5:15 mils	
Trace Impedance	60 Ω	+/- 10%

Figure 7: SMI# Routing Guidelines (Dual Processor)

1.1.8. Processor Thermal Diode (THRMDP and THRMDN)

These traces (THRMDP and THRMDN) route the processor's thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance. Refer to Figure 8:

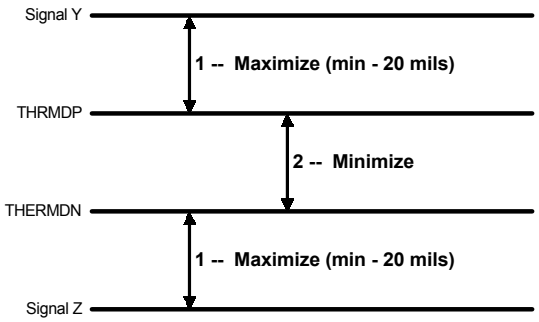


Figure 8: Routing for THRMDP and THRMDN

Rule	
Length Equalization	route these traces parallel +/- 0.5"
Layer	route both on the same layer

1.1.9. Additional Host Bus Guidelines

Additional host bus layout guidelines detailed in the Intel® 820 Chipset Platform Design Guide 1.0 and the Intel® 820 Chipset Platform Design Guide Update 1.xx apply to PGA370 designs.

Special Considerations:

1) BREQ Pins

UP systems should pull BREQ0 to ground through a 10 ohm resistor. DP systems should implement the circuitry on pages 2-53 and 2-54 of the Intel® 820 Chipset Design Guide for arbitration ID strapping.

1.1.10. Decoupling Guidelines for Intel® 820 Chipset/PGA370 Designs

These are preliminary decoupling guidelines for PGA370 designs and are estimated to meet VRM 8.4 V1.5 motherboard guidelines. Do not share vias on decoupling capacitors, and provide more than one via per decoupling capacitor.

1. Vcc_CORE Decoupling Design

- Ten or more 4.7uF capacitors in 1206 packages. Ceramic X7R capacitors are recommended.

  All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between Vcc_CORE/Vss power pins. Examples are as shown in Figure 9 below and Figure 2 on page 7.

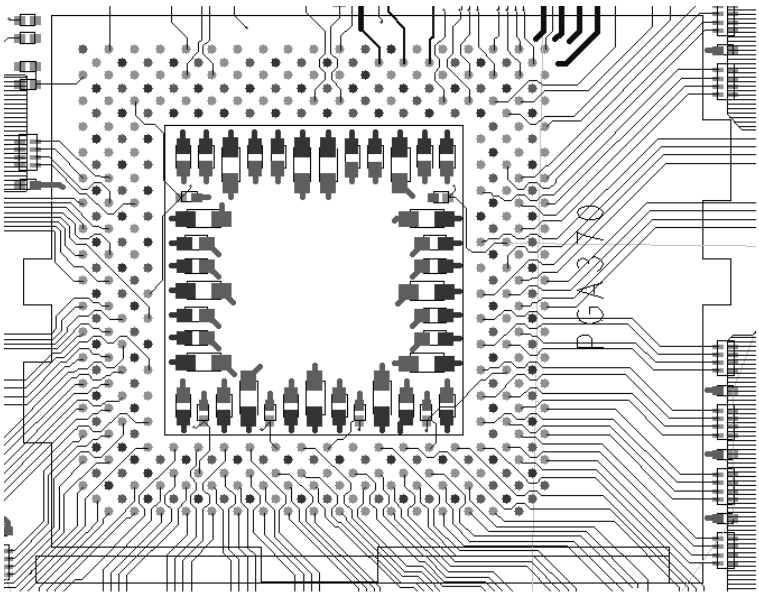


Figure 9: Capacitor Placement on the Motherboard

2. V_{TT} Decoupling Design

For Itt = 3.0A (max).

- Nineteen - 0.1uF capacitors in 0603 packages placed within 200 mils of AGTL+ termination R-pack's, minimum of one capacitor for every two R-packs. These capacitors are shown on the exterior of the MCH in Figure 2. Ceramic X7R capacitors are recommended.

3. Vref Decoupling Design

- Four - 0.1uF capacitors in 0603 packages placed near Vref pins (within 500 mils). Ceramic X7R capacitors are recommended.

1.1.11. VREF Implementation

The Vref input pins supply the AGTL+ reference voltage, which is 2/3 of V_{TT}. Vref should be generated with one voltage divider between the MCH and the processor for all Vref pins. It is recommended that Vref be decoupled with a minimum of six 0.1uF capacitors. Four of the 0.1uF should be placed within 500 mils of the processor input pins (minimum of one capacitor per processor Vref pin). Refer to Figure 10.

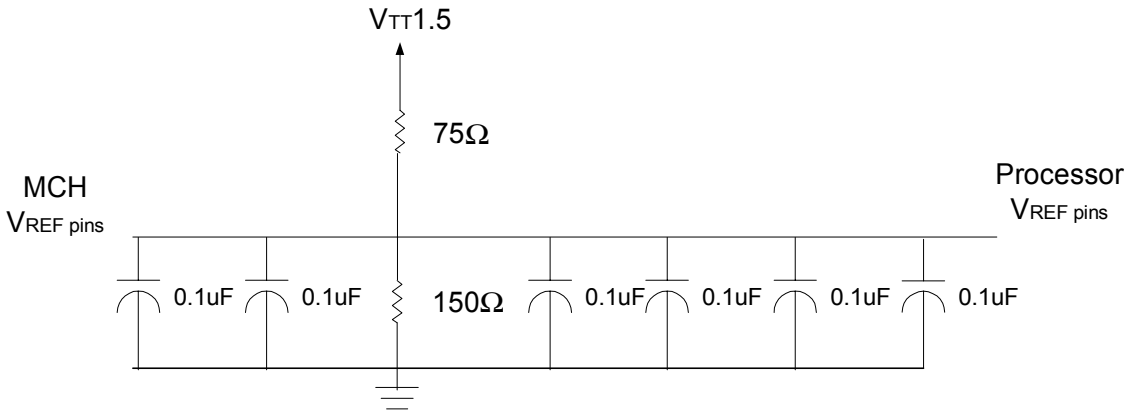


Figure 10: Vref Decoupling

1.1.12. CLKREF Circuit Implementation

The CLKREF input, utilized by the Intel® Pentium® III processor for the PGA370 socket, requires a 1.25V source. It can be generated from a voltage divider on the Vcc2.5 or Vcc3.3 sources utilizing 1% tolerance resistors. A .47uF or larger decoupling capacitor is required on this input. See Figure 11: and Table 4 for example CLKREF circuits. Do not use V_{TT} as the source for this reference!

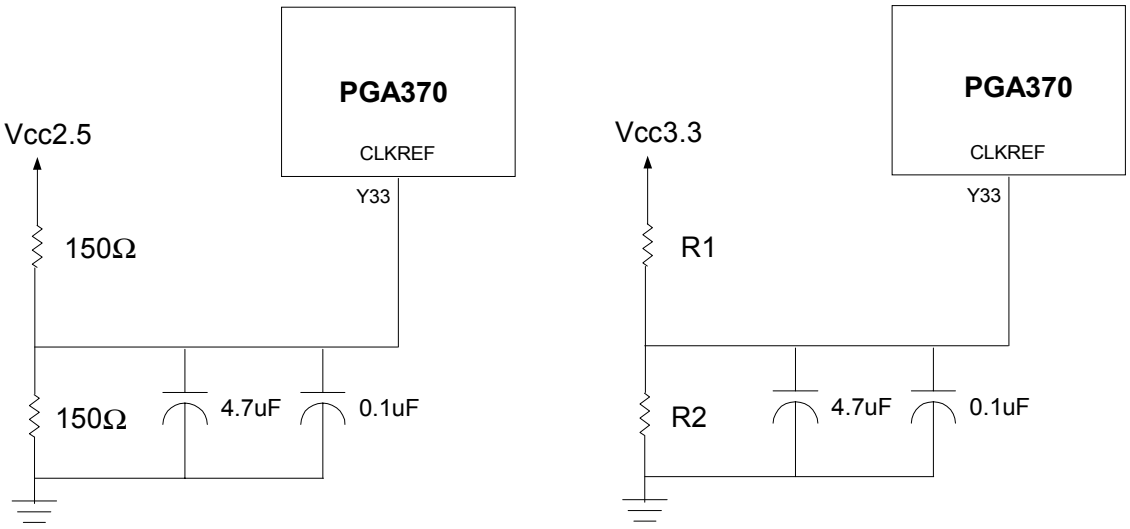


Figure 11: Examples for CLKREF Divider Circuit

R1 (Ω)	R2 (Ω)	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

Table 4: Resistor Values for CLKREF Divider (3.3V Source)

[All of the combinations in Table 4 are valid]

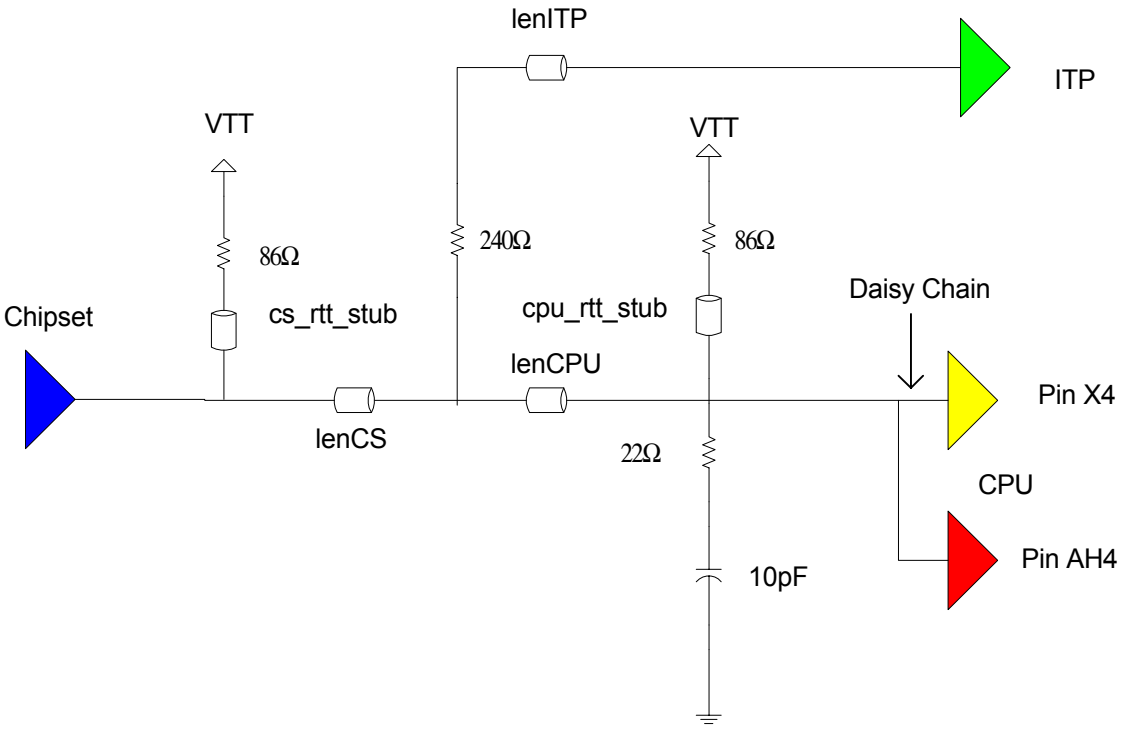
1.1.13. On-die Rtt Considerations

The Intel® Pentium® III processor for the PGA370 has variable on-die termination resistors that terminate the AGTL+ bus at the processor. The value of the resistor can be varied via the RTTCTRL pin found on the PGA370 socket. The value of the pull-down on the RTTCTRL pin will set the value of the on-die Rtt. For Intel® 820 chipset designs, the recommended RTTCTRL pulldown resistor is 62 ohms +/- 1%. Please refer to the Intel® Pentium® III Processor for the PGA370 Socket at 500E MHz and 550EMHz datasheet for additional information on the RTTCTRL pin functionality.

1.1.14. Connecting RESET# and RESET2# on a PGA370 Design (Uni-processor)

Uniprocessor PGA370 designs must route the AGTL+ reset signal from the chipset to two pins on the processor as well as to the debug port connector. This reset signal is connected to pins AH4 (RESET#) and X4 (RESET2#) at the PGA370 socket. Finally, the AGTL+ reset signal must always be terminated to V_{TT} on the motherboard. See Figure 12 below.

Designs which do not support the debug port will not utilize the 240 ohm series resistor or the connection of RESET# to the debug port connector. Note: The V_{TT} pull-up values are 86Ω per Figure 12.

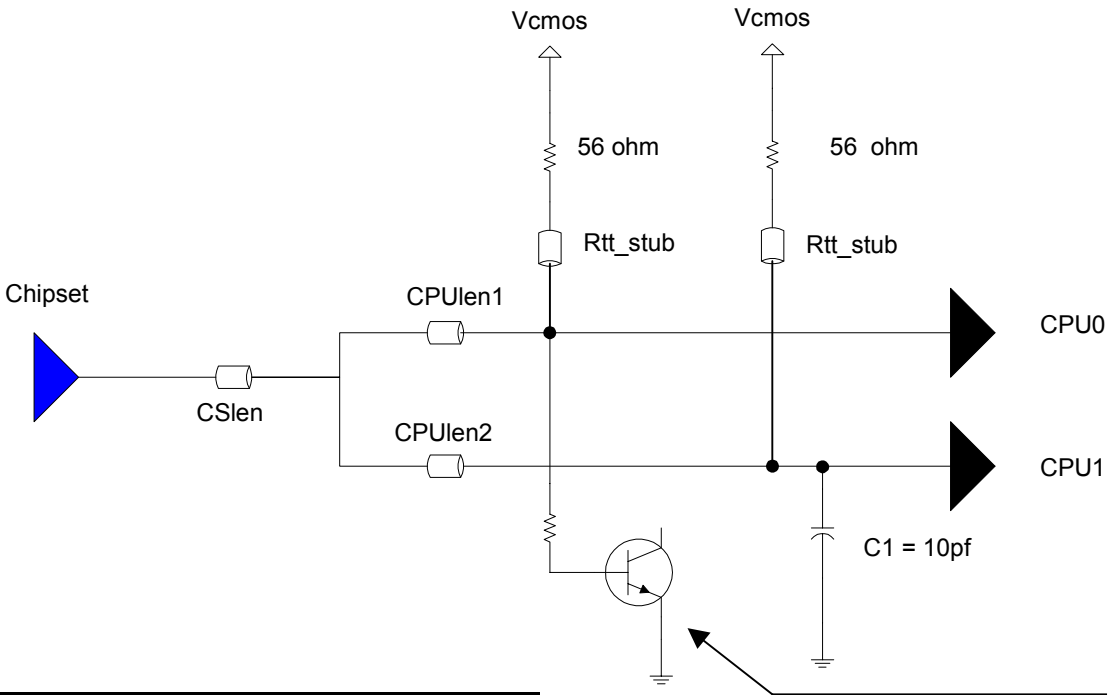


Parameter	Minimum (in)	Maximum (in)
lenCS	0.5	1.5
lenITP	1	3
lenCPU	0.5	1.5
cs_rtt_stub	0.5	1.5
cpu_rtt_stub	0.5	1.5

Figure 12: AGTL+ Reset Schematic for PGA370 Designs

1.1.15. Connecting RESET# and RESET2# on a PGA370 Design (Dual Processor)

Reset2# (pin X4) should be connected to ground for Dual Processor designs. Reset# (pin AH4) should be connected per Figure 13 to prevent ringback.



Parameter	Minimum (in)	Maximum (in)
CPUlen	2.5	3.5
CSlen	2.25	2.5
Rtt_stub	0	0.25

Figure 13: AGTL+ Reset for DP Intel® 820 Chipset Based Designs

- R1 = 56 +/- 5% ohms
- C1 = 10pF +/- 5%
- 60 Ohm +/- 10% motherboard manufacturing impedance
- Place C1 as close to the trace as possible
- 5:15 trace width to spacing ratio
- **CPU stub lengths of the same net must be matched within 0.25”**

1.1.16. Debug Port Requirements

Due to the lower voltage technology employed with the FC-PGA processor, changes are required to support the debug port. Previously, the test access port (TAP) signals used 2.5V logic. This is the case with the Intel® Celeron™ processor in the PPGA package. FC-PGA processors utilize 1.5V logic levels on the TAP. As a result, a new debug port connector is to be used on *flexible* PGA370 designs. The new 1.5V connector is the mirror image of the older 2.5V connector. Either connector will fit into the same printed circuit board layout. The pin numbers change, as can be seen in Figure 14. Along with the new connector, an In-Target Probe (ITP) that is capable of communicating with the TAP at 1.5V logic levels is required.

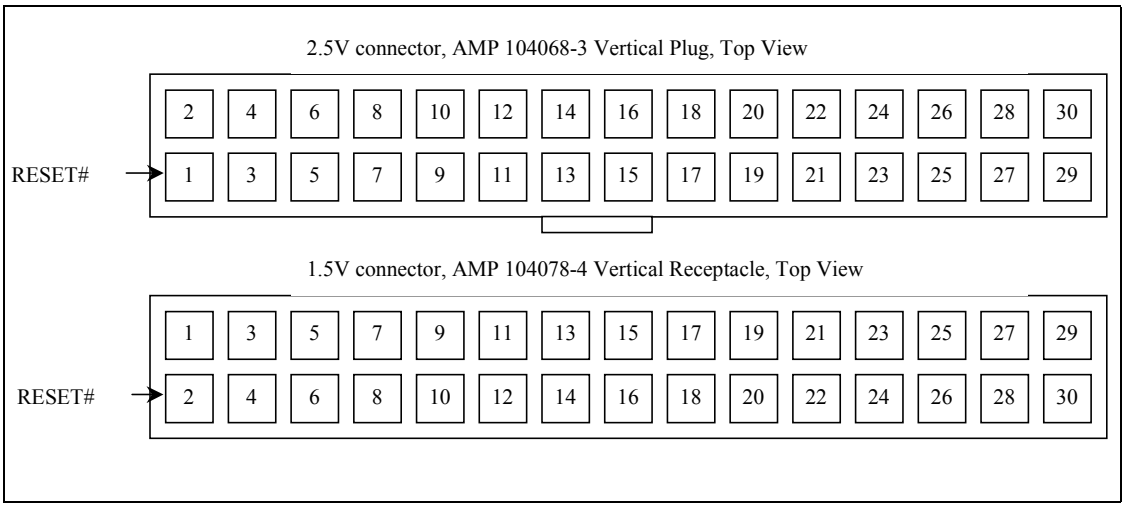


Figure 14: TAP Connector Comparison

See the specific processor datasheet for more information regarding the debug port.

1.1.17. Processor PLL Filter Recommendations

Intel® PGA370 processors have internal phase lock loop (PLL) clock generators which are analog in nature and require quiet power supplies to minimize jitter.

Topology

The general desired topology is shown in Figure 15. Not shown are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

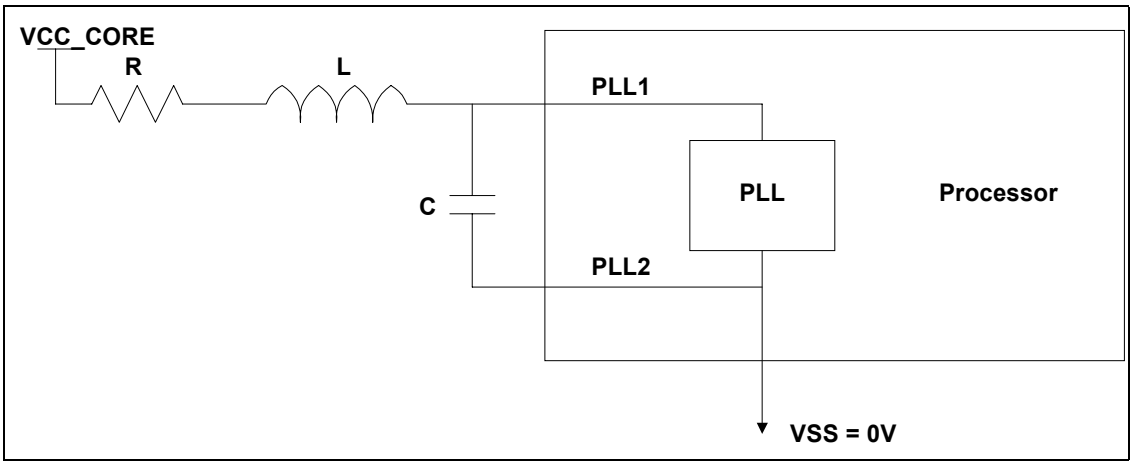


Figure 15: PLL Filter Topology

Recommendation for Intel® Platforms

The following tables are examples of components that meet Intel's recommendations, when configured in topology

Part Number	Value	Tol	SRF	Rated I	DCR (Typical)
TDK MLF2012A4R7KT	4.7uH	10%	35MHz	30mA	0.56Ω (1 Ω max)
Murata LQG21N4R7K00T1	4.7uH	10%	47MHz	30mA	0.7 Ω (+/-50%)
Murata LQG21C4R7N00	4.7uH	30%	35MHz	30mA	0.3 Ω max

Table 5: Componenet Recommendations – Inductor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33uF	20%	2.5nH	0.225 Ω
AVX TPSD336M020S0200	33uF	20%	TBD	0.2 Ω

Table 6: Component Recommendations - Capacitor

Value	Tolerance	Power	Note
1 Ω	10%	1/16W	Resistor may be implemented with trace resistance, in which discrete R is not needed

Table 7: Componenet Recommendations - Resistor

To satisfy damping requirements, total series resistance in the filter (from VCC_CORE to the top plate of the capacitor) must be at least 0.35Ω. This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has minimum DCR of 0.25Ω, then a routing resistance of at least 0.10Ω is required. Be careful not to exceed the maximum resistance rule (2Ω). For example, if using discrete R1 (1Ω ± 1%), the maximum DCR of the L (trace plus inductor) should be less than 2.0 - 1.1 = 0.9Ω, which precludes using some inductors and will set a max trace length.

Routing requirements:

- The capacitor (C) should be close (< .500") to the PLL1 and PLL2 pins, < 0.1Ω per route.[1]
- The PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- The inductor (L) should be close to C; any routing resistance should be inserted between VCC_CORE and L.
- Any discrete resistor (R) should be inserted between VCC_CORE and L.

Other requirements:

- Use shielded type inductor to minimize magnetic pickup
- Filter should support DC current > 30mA

[1] These routes do not count towards the minimum damping R requirement.

- DC voltage drop from VCC to PLL1 should be < 60mV, which in practice implies series R < 2Ω; also means pass band (from DC to 1Hz) attenuation < 0.5dB for VCC = 1.1V, and < 0.35dB for VCC = 1.5V.

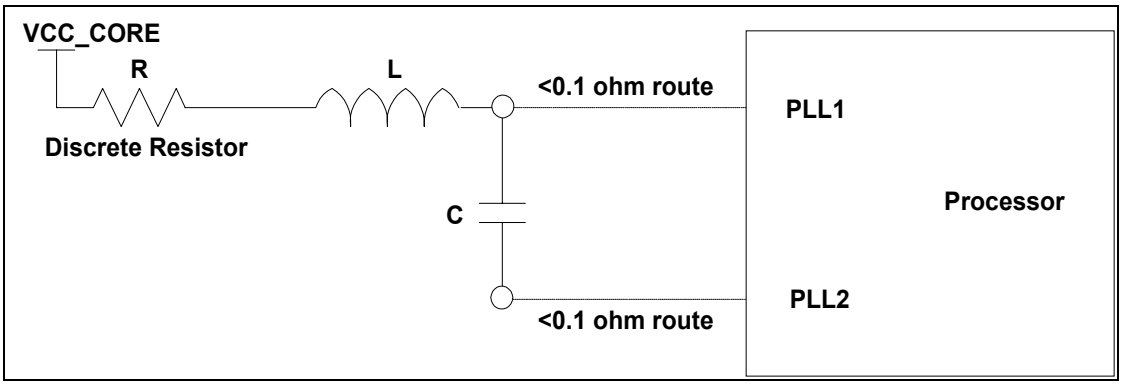


Figure 16: Example PLL Filter Using a Discrete Resistor

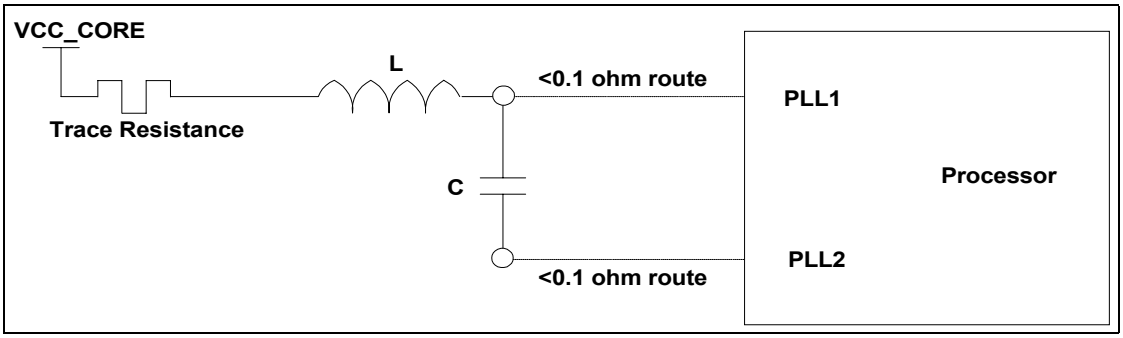


Figure 17: Example PLL Filter Using a Buried Resistor

1.1.18. Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation.

The low-pass specification, with input at VCC_CORE and output measured across the capacitor, is as follows:

- < 0.2dB gain in pass band
- < 0.5dB attenuation in pass band (see DC drop in next set of requirements)
- > 34dB attenuation from 1MHz to 66MHz
- > 28dB attenuation from 66MHz to core frequency

The filter specification is graphically shown in Figure 18.

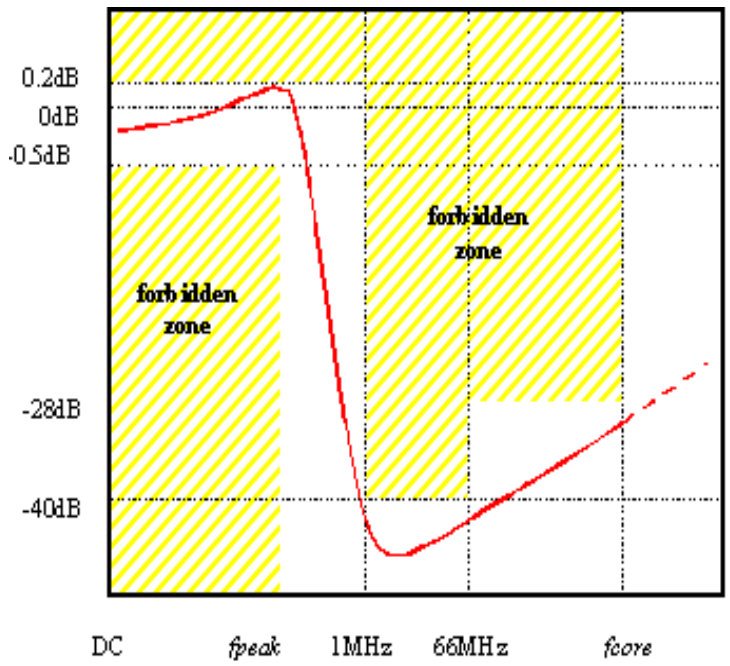


Figure 18: Filter Specification

Note: for Figure 18:

- Diagram not to scale.
- No specification for frequencies beyond *fcore*.
- *fpeak* should be less than 0.05MHz.

1.1.19. Power Delivery Guidelines for PGA370 Designs

Intel® Pentium® III processor with FC-PGA designs utilize Dual Ended Termination (DET) which increases the current requirements of the V_{TT} regulator. Additional power concerns must be addressed in designing an Intel® 820 chipset based platform with FC-PGA processors. Refer to the Intel® Pentium® III processor datasheet for the latest information.

V_{CCCORE} (V_{CC_VID})

This should be connected to the VRM 8.4 voltage regulator with sufficient decoupling outlined in section 1.1.10. Current requirements will vary by configuration and frequency – refer to the Intel® Pentium® III processor datasheet for information pertaining to specific processors.

Additional considerations:

Follow VRM8.4 rev 1.6 or later for implementation details for the latest Intel® Pentium® III processor Icc requirements. Please consult with your voltage regulator vendor for limitations on their components. Please consult the Intel® Pentium® III datasheet for the latest Icc requirements.

V_{TT} and $V_{CC1.5}$

This should be connected to the 1.5V regulator with sufficient current capacity for dual ended termination and 1.5V power delivery to the processor. Previous requirements for V_{TT} on Intel® 820 Chipset designs were for single ended termination. V_{TT} should be connected to the same 1.5V regulator used for $V_{CC1.5}$.

Additional considerations:

It is required that V_{TT} and $V_{CC1.5}$ be held to 1.5V +/- 3% while the processor system bus is static. +/-3% is the required design target; +/-9% will come from the transient noise added. Total I_{TT} current requirements for both the chipset and the processor are approximately 5.4 Amps.

Distribute V_{TT} with a wide trace. A 0.050" minimum trace is recommended to minimize DC losses.

$V_{CC2.5}$

The Intel® Pentium® III processor for the PGA370 socket does not use this signal. Leaving the pin unconnected is recommended.

1.1.20. Clock Routing Guidelines for PGA370 Designs

1.1.20.1. Uni-Processor Configurations

Clock signals should be routed on .005" traces with a minimum of .015" between adjacent signals. A minimum of 0.020" spacing is recommended. The series resistor should be located as close to the clock driver as possible. The 10pF - 603 capacitor should be added as close to the resistor as possible. The clock trace length to the processor should be 3.54 inches shorter than the clock trace to the MCH. Refer to Figure 19.

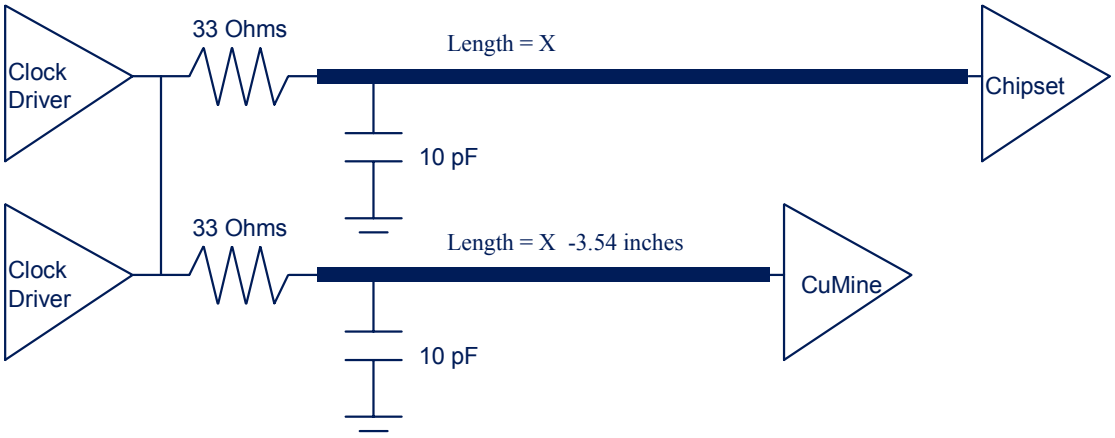


Figure 19: Intel® 820 Chipset / FCPGA Clock Routing Guidelines (Uni-Processor Configuration)

1.1.20.2. Dual-Processor Configurations

Clock signals should be routed on .005" traces with a minimum of .015" between adjacent signals. A minimum of 0.020" spacing is recommended. The series resistor should be located as close to the clock driver as possible. The 10pF - 603 capacitor should be added as close to the resistor as possible. The clock trace length to each processor should be 2.40 inches shorter than the clock trace to the MCH. Refer to Figure 20.

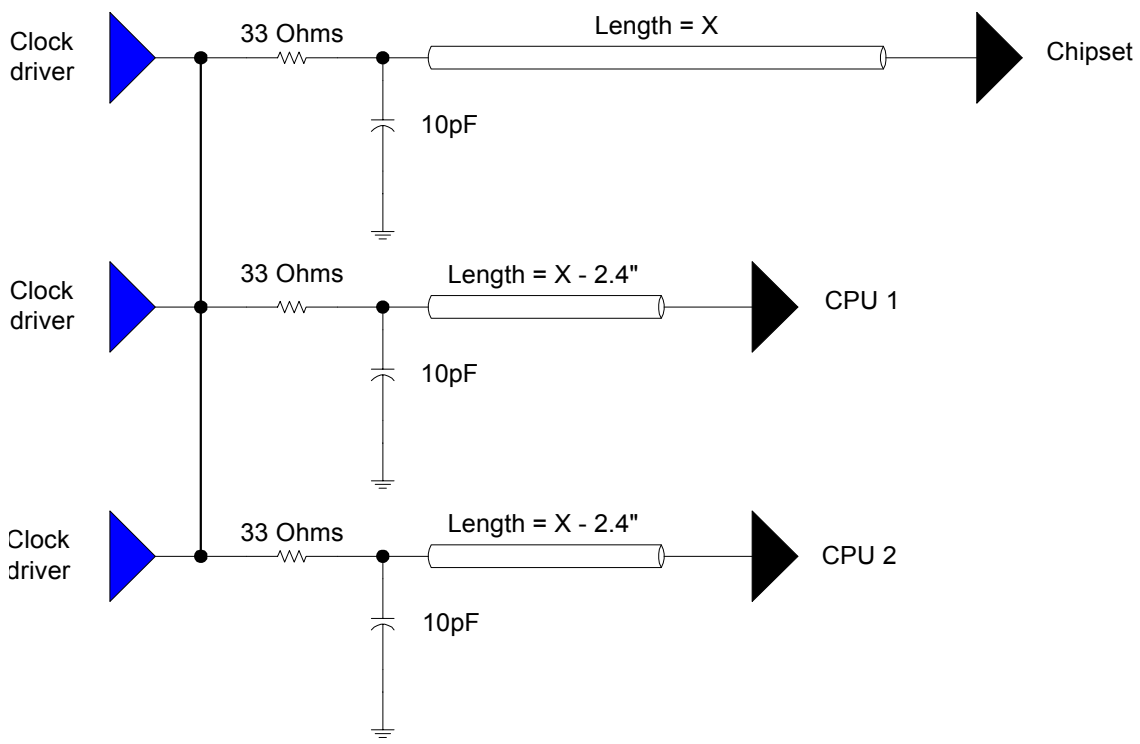


Figure 20: Intel® 820 Chipset / FCPGA Clock Routing Guidelines (Dual Processor Configuration)

1.1.21. PGA370 Thermal Considerations

Refer to the Intel® Pentium® III processor datasheet for the latest thermal considerations for PGA370 designs The Intel® Pentium® III processor datasheet can be found at: http://developer.intel.com/design/PentiumIII/datashts/

The current keep-out requirements are detailed below. Figure 21 shows the system component keep-out volume above the socket connector required for the reference design thermal solution for high frequency FCPGA processors. This keep-out envelope provides adequate room for the heat sink, fan and attach hardware under static conditions as well as room for installation of these components on the socket.

Figure 22 shows component keep-outs on the motherboard required to prevent interference with the reference design thermal solution. Note portions of the heat sink and attach hardware hang over the motherboard.

Adhering to these keep-out areas will ensure compatibility with Intel boxed processor products and Intel enabled third party vendor thermal solutions for FCPGA processors. While the keep-out requirements should provide adequate space for the reference design thermal solution, systems integrators should check their vendor to ensure their specific thermal solutions fit within their specific system designs. Please ensure that the thermal solutions under analysis comprehend the specific thermal design requirements for higher frequency Pentium® III processors.

While thermal solutions for lower frequency FCPGA processors may not require the full keep-out area, larger thermal solutions will be required for higher frequency processors and failure to adhere to the guidelines will result in mechanical interference.

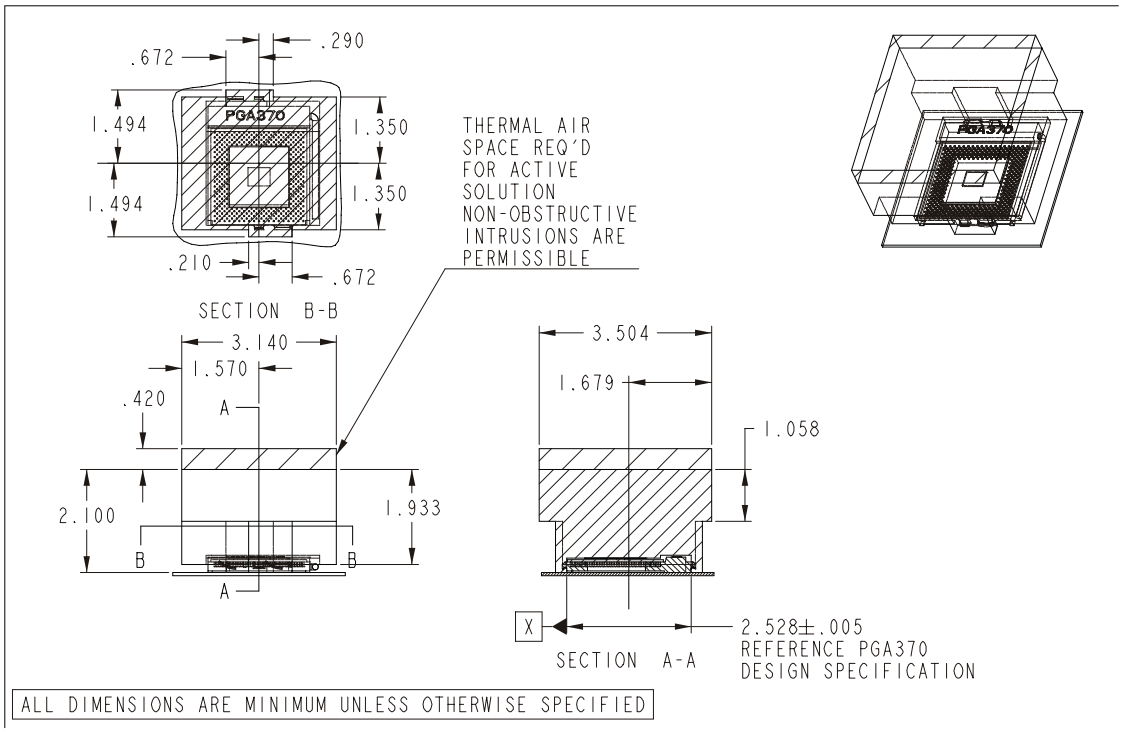


Figure 21: Heat Sink Volumetric Keep Out Regions

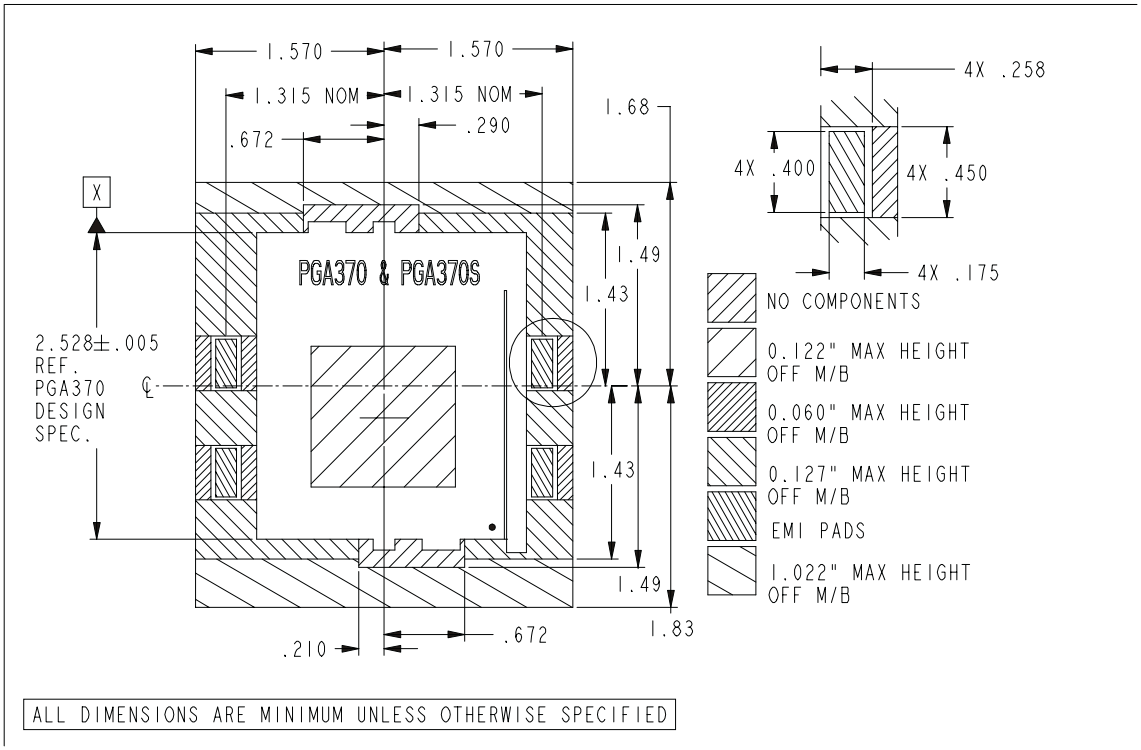


Figure 22: Motherboard Component Keep Out Regions

1.1.22. PGA370 EMI Considerations

Intel recommends that customers implement EMI Heatsink ground pads on any platform under development that will support Intel® Pentium® III processors. This recommendation provides the ability to utilize Heatsink Grounding should it become necessary to pass EMI emission regulations. Completed designs that do not implement the EMI Ground Pads should consider implementing them in a future board spin as a contingency plan for supporting high frequency processors. Depending upon the platform emission characteristics, platform/processor compatibility, platform lifetime, etc., Heatsink Grounding may not be required and, therefore, OEMs should make the decision to implement the ground pads based upon their specific platform design characteristics and needs. Please refer to the *Intel® Pentium® III Processor Based Platforms and Heatsink Grounding* application note for additional information.

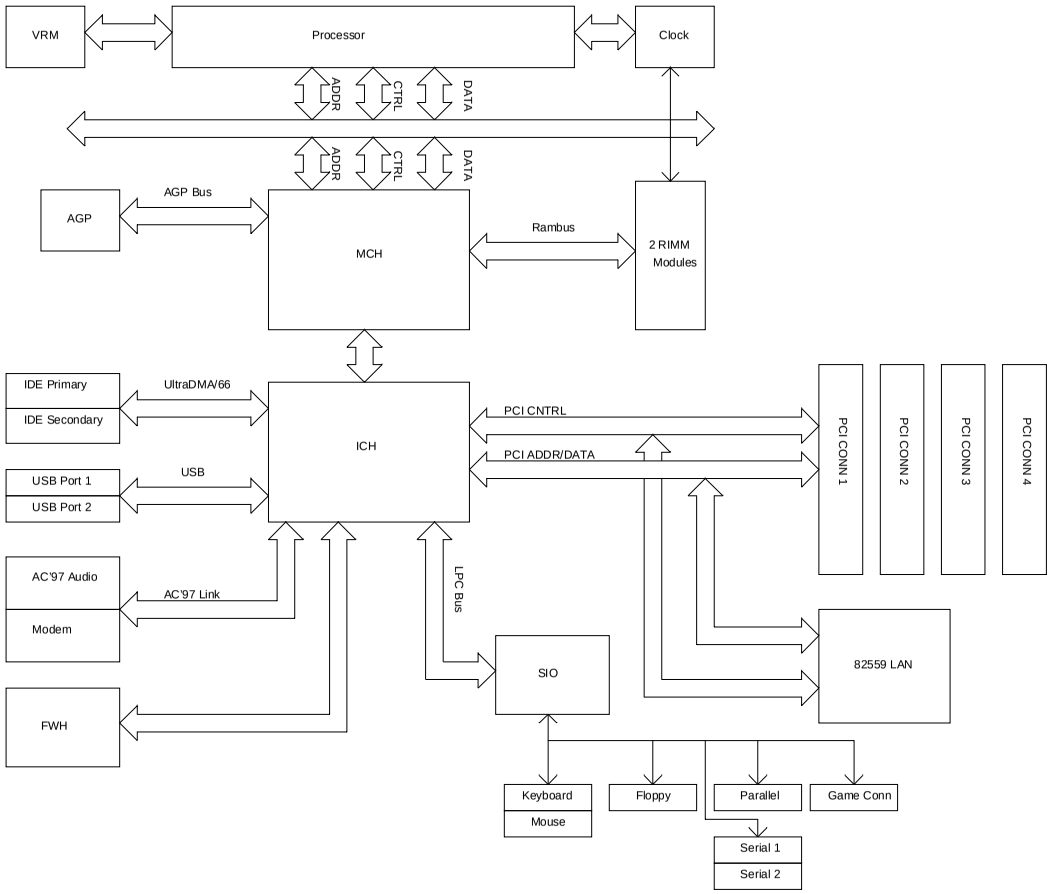
2. RIMM – Uni-Processor FCPGA Reference Schematics

INTEL(R) 820 CHIPSET
UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS
REV B (FCPGA PROCESSOR)

Note that these schematics are preliminary and are subject to change.

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD		REV: 1.0
intel® PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 4-6-2000 9:23	SHEET: 1 OF 37

Block Diagram



Device Table

REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U20	74LVC06A	A, B, C	31
U14	74LVC07A	A, B, C	18, 29
U19	74LVC07A	A, C, D	18, 22
U3	74LVC08A	A, B	15, 31
U15	74LVC14a	A, B, C, D	31
U18	74LS132	B, C	29, 31
U13	82820 (ICH)		8, 9
U10	82820 (MCH)		6, 7
U5	82559		16
U8	93C46A		16
U2	AD1881		13
U11	CK133		5
U12	DRCG		5
U16	FWH		10
U4, U6	GD75232		25
U1	LM4880		14
U17	LPC47B27X		12
U9	ADM1021		3
U7	TPS2042		23

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD BLOCK DIAGRAM		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 4-6-2000 9:21	SHEET: 2 OF 37

SKT?

370-PIN SOCKET

PART 1

HD#[63:0] 6,34

HD#0	W1	HD#0
HD#1	T4	HD#1
HD#2	N1	HD#2
HD#3	M6	HD#3
HD#4	U1	HD#4
HD#5	S3	HD#5
HD#6	T6	HD#6
HD#7	J1	HD#7
HD#8	S1	HD#8
HD#9	P6	HD#9
HD#10	Q3	HD#10
HD#11	M4	HD#11
HD#12	Q1	HD#12
HD#13	L1	HD#13
HD#14	N3	HD#14
HD#15	U3	HD#15
HD#16	H4	HD#16
HD#17	R4	HD#17
HD#18	P4	HD#18
HD#19	H6	HD#19
HD#20	L3	HD#20
HD#21	G1	HD#21
HD#22	F8	HD#22
HD#23	G3	HD#23
HD#24	K6	HD#24
HD#25	E3	HD#25
HD#26	E1	HD#26
HD#27	F12	HD#27
HD#28	A5	HD#28
HD#29	A3	HD#29
HD#30	J3	HD#30
HD#31	C5	HD#31
HD#32	F6	HD#32
HD#33	C1	HD#33
HD#34	C7	HD#34
HD#35	B2	HD#35
HD#36	C9	HD#36
HD#37	A9	HD#37
HD#38	D8	HD#38
HD#39	D10	HD#39
HD#40	C15	HD#40
HD#41	D14	HD#41
HD#42	D12	HD#42
HD#43	A7	HD#43
HD#44	A11	HD#44
HD#45	C11	HD#45
HD#46	A21	HD#46
HD#47	A15	HD#47
HD#48	A17	HD#48
HD#49	C13	HD#49
HD#50	C25	HD#50
HD#51	A13	HD#51
HD#52	D16	HD#52
HD#53	A23	HD#53
HD#54	C21	HD#54
HD#55	C19	HD#55
HD#56	C27	HD#56
HD#57	A19	HD#57
HD#58	C23	HD#58
HD#59	C17	HD#59
HD#60	A25	HD#60
HD#61	A27	HD#61
HD#62	E25	HD#62
HD#63	F16	HD#63

VCCVID;B26,C3,AK2,AF2,AB2,T2,P2,K2,F4,E5,AM4,AE5,AA5,W5,S5,N5,J5,F2,D6,B6
VCCVID;AM8,AJ9,E9,B10,AM12,AJ13,E13,B14,AM16,AJ5,AJ17,E17,B18,AM20,AJ21,D20,F22
VCCVID;AM24,AJ25,D24,F26,AM28,AJ29,D28,AK34,F30,B30,AM32,AH32,Z32,V32,R32
VCCVID;M32,H32,AF34,AB34,X34,T34,P34,K34,F34,B34,AH36,B22,V36,R36,H36,D36,D32
VCCVID;AD32,AH24,F14,K32,AA37,Y35

VTT1_5;AH20,AK16,AL21,AN11,AN15,G35,AL13

GND;AM34,AH2,AD2,Z2,V2,M2,D18,H2,D2,AL3,AK4,AG5,AC5,Y5,U5,Q5,L5,G5,D4,B4
GND;AM6,AJ7,E7,B8,AM10,AJ11,E11,B12,AM14,AJ15,E15,B16,AM18,AJ19,E19,F20,B20
GND;AM22,AJ23,D22,F24,B24,AM26,AJ27,D26,F28,B28,AM30,D30,AF32,AB32,X32,T32
GND;P32,F32,B32,AH34,AD34,Z34,V34,R34,M34,H34,D34,AK36,AF36,X36,T36,P36,K36
GND;F36,A37,AC33,Y37,AJ3,AL1,AN3

HA#[31:3] 6,34

HA#3	AK8	HA#3
HA#4	AH12	HA#4
HA#5	AH8	HA#5
HA#6	AN9	HA#6
HA#7	AL15	HA#7
HA#8	AH10	HA#8
HA#9	AL9	HA#9
HA#10	AH6	HA#10
HA#11	AK10	HA#11
HA#12	AN5	HA#12
HA#13	AL7	HA#13
HA#14	AK14	HA#14
HA#15	AL5	HA#15
HA#16	AN7	HA#16
HA#17	AE1	HA#17
HA#18	Z6	HA#18
HA#19	AG3	HA#19
HA#20	AC3	HA#20
HA#21	AJ1	HA#21
HA#22	AE3	HA#22
HA#23	AB6	HA#23
HA#24	AB4	HA#24
HA#25	AF6	HA#25
HA#26	Y3	HA#26
HA#27	AA1	HA#27
HA#28	AK6	HA#28
HA#29	Z4	HA#29
HA#30	AA3	HA#30
HA#31	AD4	HA#31
HA#32	X6	
HA#33	AC1	
HA#34	W3	
HA#35	AF4	

VID[3:0] 28

VID0	AL35	VID0
VID1	AM36	VID1
VID2	AL37	VID2
VID3	AJ37	VID3

RS#0	AH26	RS#0	6,34
RS#1	AH22	RS#1	6,34
RS#2	AK28	RS#2	6,34

REQ#0	AK18	HREQ#0	6,34
REQ#1	AH16	HREQ#1	6,34
REQ#2	AH18	HREQ#2	6,34
REQ#3	AL19	HREQ#3	6,34
REQ#4	AL17	HREQ#4	6,34

DEP0#	C33
DEP1#	C31
DEP2#	A33
DEP3#	A31
DEP4#	E31
DEP5#	C29
DEP6#	E29
DEP7#	A29

RESVTT0	U37
RESVTT1	U35
RESVTT2	S37
RESVTT3	S33
RESVTT4	E23
RESVTT5	AN21
RESVTT6	AA35
RESVTT7	AA33

VTT1_5

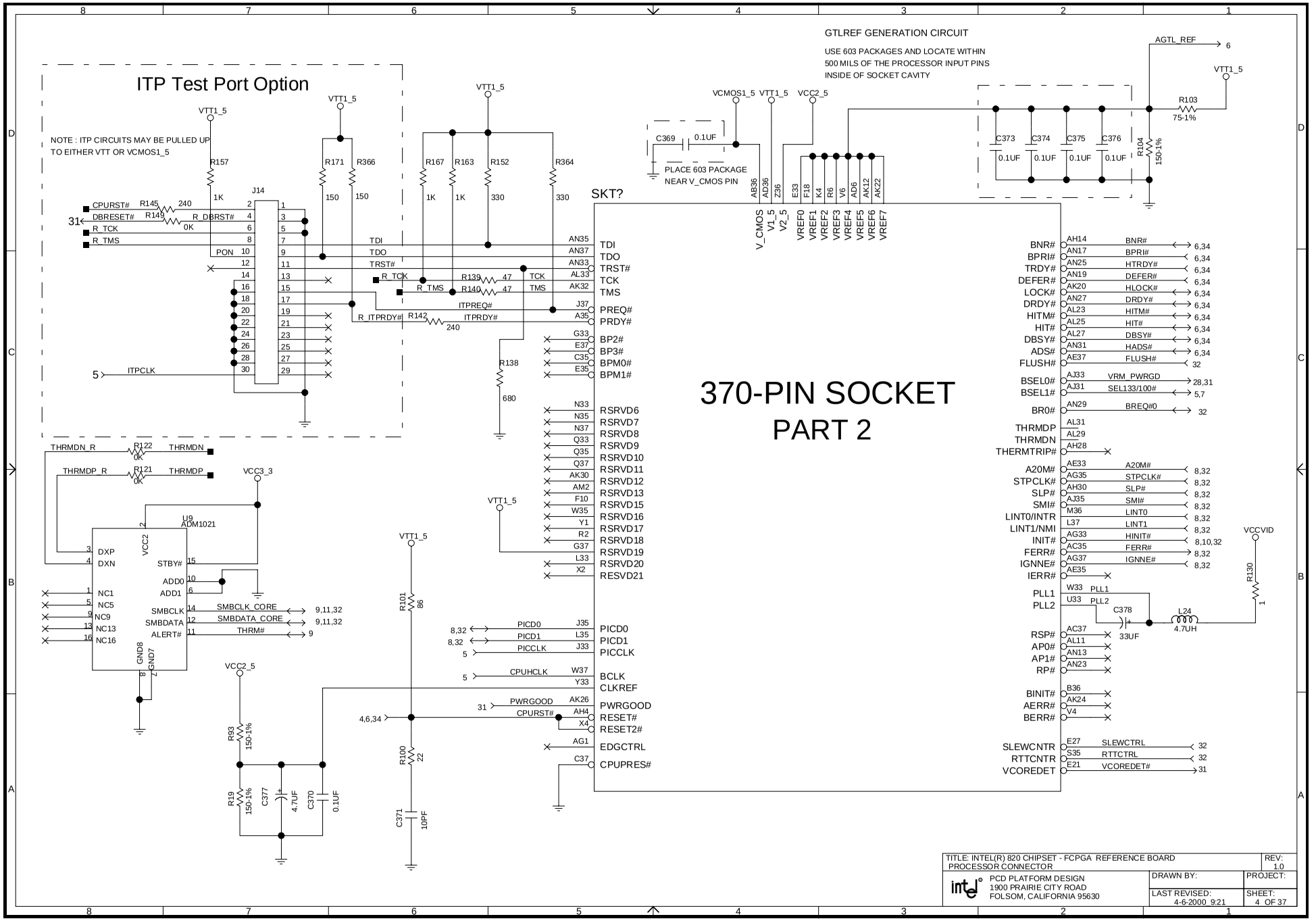
VCC12

Fan Header

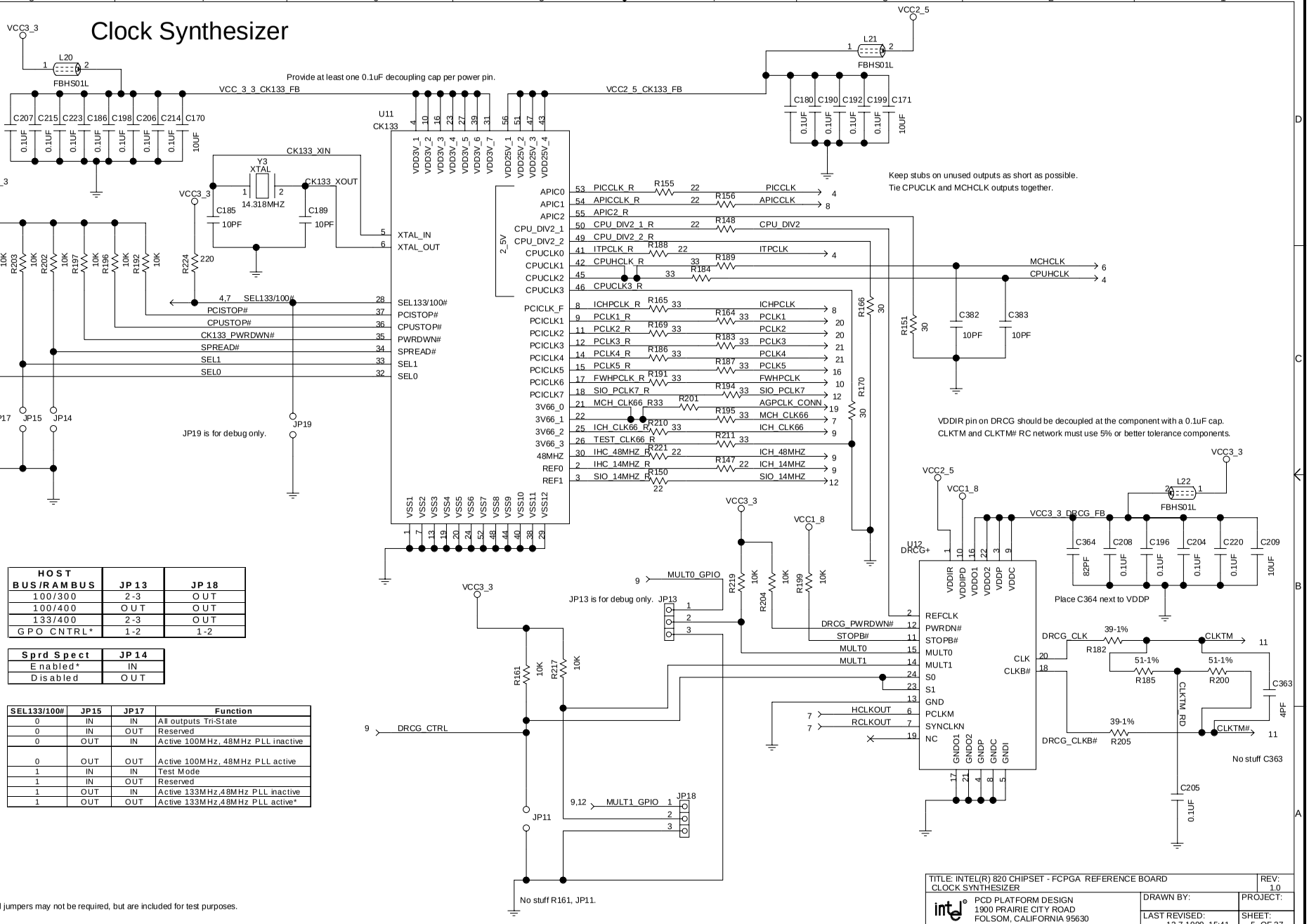
C80 0.1UF

JP16 1 2 3

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD PROCESSOR CONNECTOR		REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 4-6-2000 9:21	SHEET: 3 OF 37


ITP Test Port Option
NOTE : ITP CIRCUITS MAY BE PULLED UP TO EITHER VTT OR VCMOS1_5
GTLREF GENERATION CIRCUIT
USE 603 PACKAGES AND LOCATE WITHIN 500 MILS OF THE PROCESSOR INPUT PINS INSIDE OF SOCKET CAVITY
PLACE 603 PACKAGE NEAR V_CMOS PIN
SKT?
370-PIN SOCKET
PART 2
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD PROCESSOR CONNECTOR
REV: 1.0
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 4-6-2000 9:21
SHEET: 4 OF 37

Clock Synthesizer

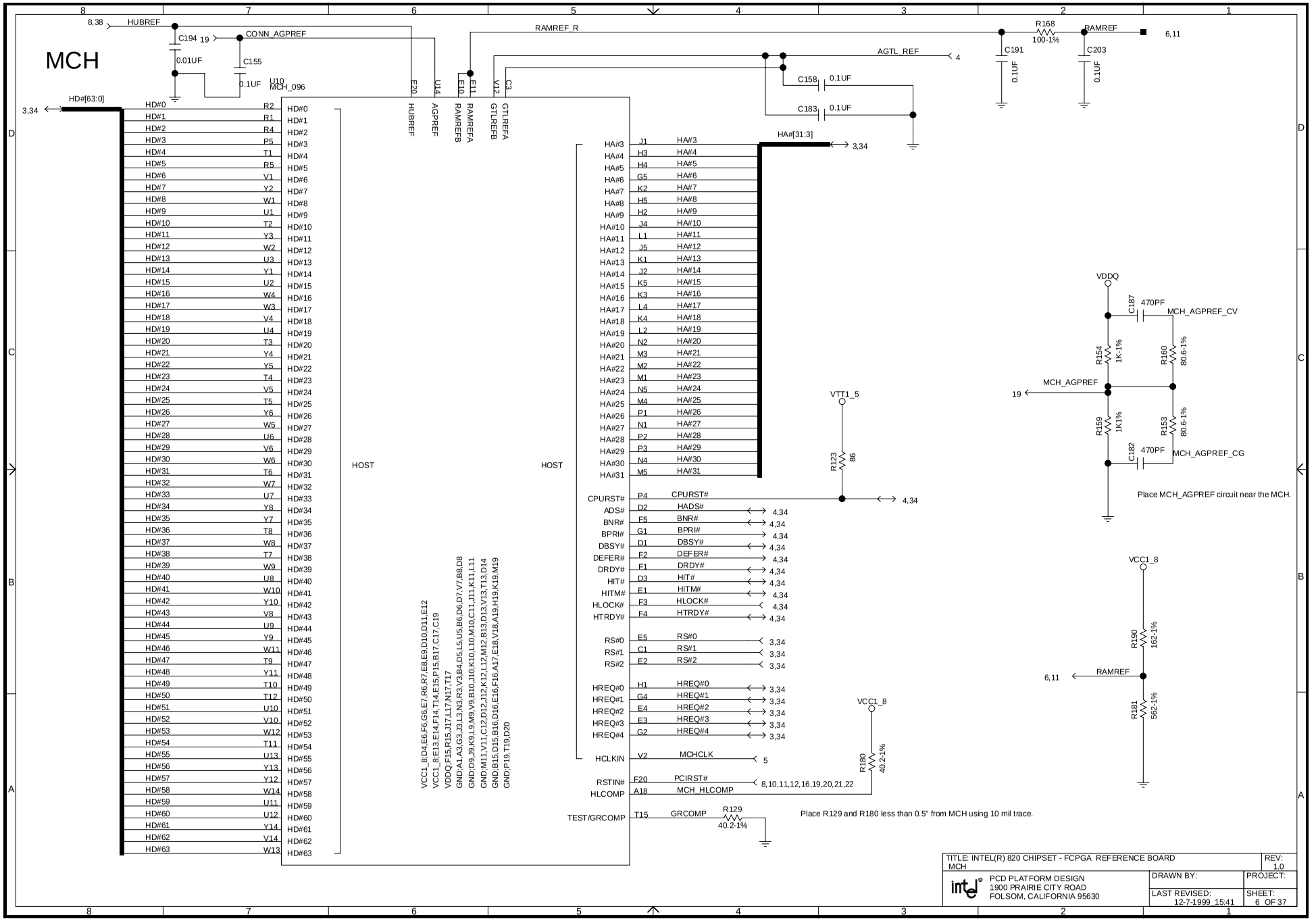


HOST BUS/RAMBUS	JP13	JP18
100/300	2-3	OUT
100/400	OUT	OUT
133/400	2-3	OUT
GPO CNTRL*	1-2	1-2

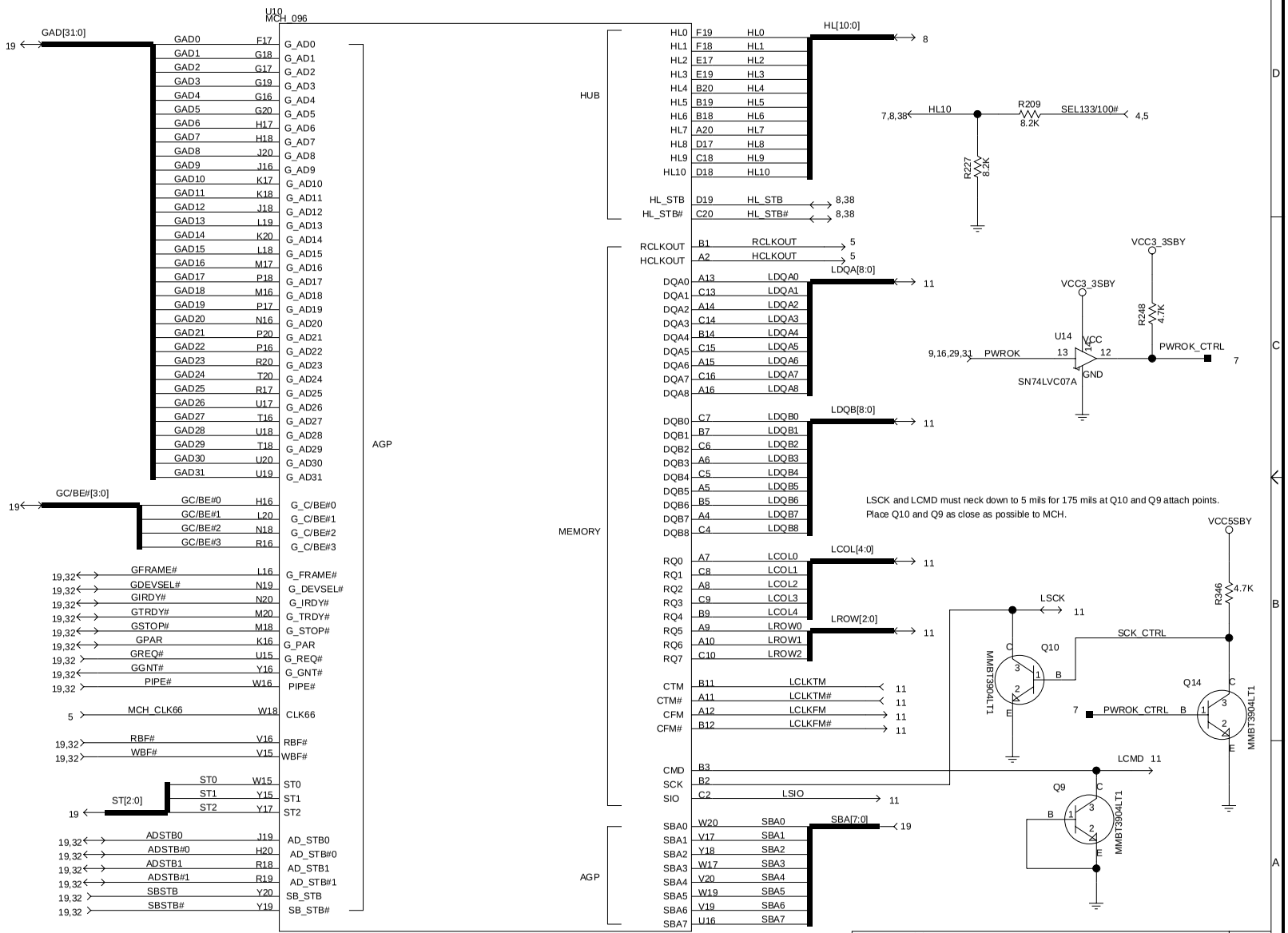
Sprd Spect	JP14
Enabled*	IN
Disabled	OUT

SEL133/100#	JP15	JP17	Function
0	IN	IN	All outputs Tri-State
0	IN	OUT	Reserved
0	OUT	IN	Active 100MHz, 48MHz PLL inactive
0	OUT	OUT	Active 100MHz, 48MHz PLL active
1	IN	IN	Test Mode
1	IN	OUT	Reserved
1	OUT	IN	Active 133MHz,48MHz PLL inactive
1	OUT	OUT	Active 133MHz,48MHz PLL active*

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD CLOCK SYNTHESIZER		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 12-7-1999 15:41	SHEET: 5 OF 37

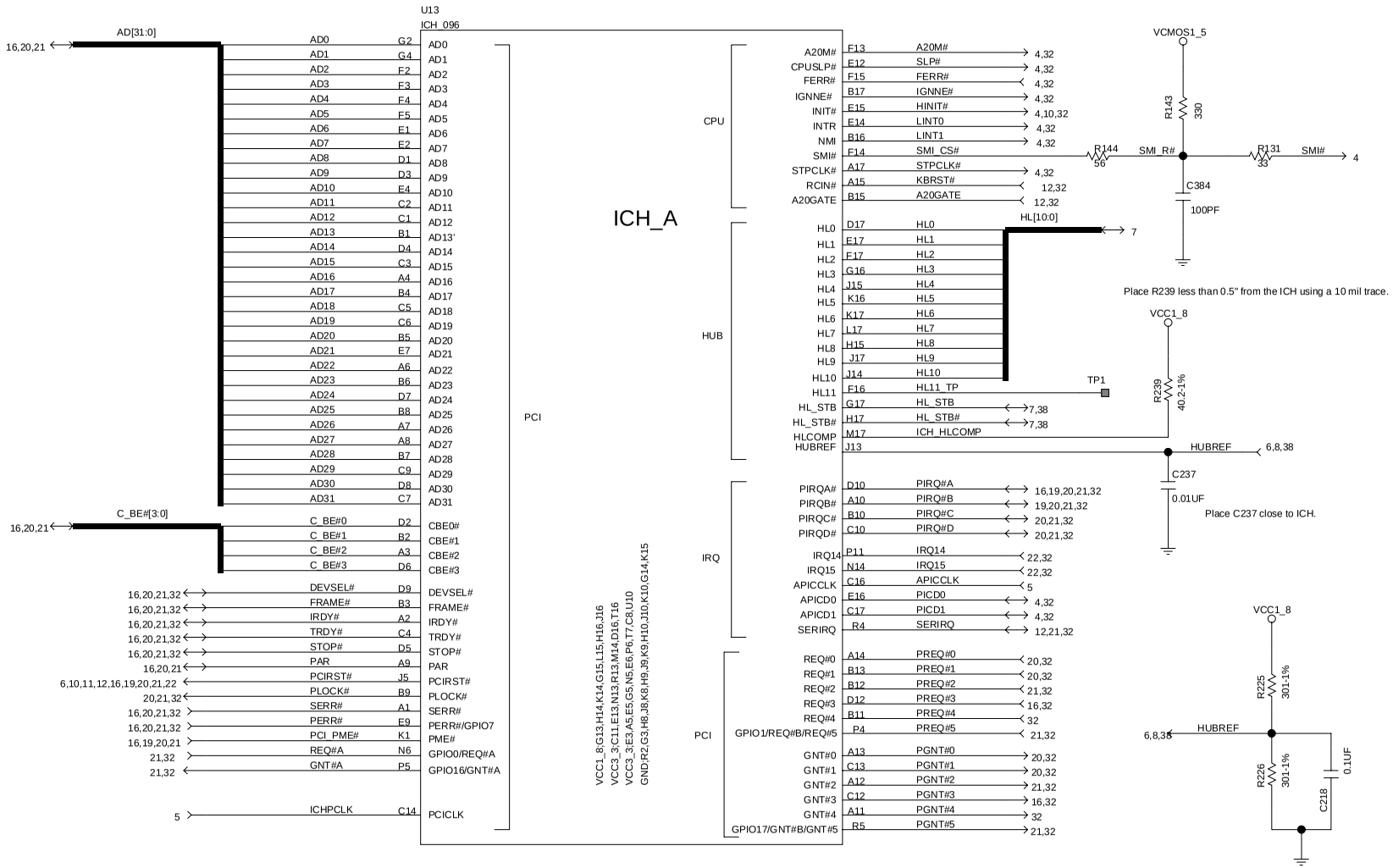

MCH
8,38 HUBREF
C194 0.01UF
19 CONN_AGPREF
C155 0.1UF
U10 MCH_096
RAMREF_R
R168 100-1%
RAMREF 6,11
C191 0.1UF
C203 0.1UF
AGTL_REF 4
C158 0.1UF
C183 0.1UF
HD#[63:0]
3,34
HA#[31:3] 3,34
HUBREF E20
AGPREF U14
RAMREFB E10
RAMREFA F11
GTLREFB V12
GTLREFA C3
HOST
HOST
VTT1_5
R123 66
CPURST# 4,34
ADS# 4,34
BNR# 4,34
BPRI# 4,34
DBSY# 4,34
DEFER# 4,34
DRDY# 4,34
HIT# 4,34
HITM# 4,34
HLOCK# 4,34
HTRDY# 4,34
RS#0 3,34
RS#1 3,34
RS#2 3,34
HREQ#0 3,34
HREQ#1 3,34
HREQ#2 3,34
HREQ#3 3,34
HREQ#4 3,34
HCLKIN MCHCLK 5
RSTIN# PCIRST# 8,10,11,12,16,19,20,21,22
HLCOMP MCH_HLCOMP
TEST/GRCOMP GRCOMP R129 40.2-1%
VCC1_8
R180 40.2-1%
Place R129 and R180 less than 0.5" from MCH using 10 mil trace.
VDDQ
C187 470PF MCH_AGPREF_CV
R154 1K-1%
R160 80.6-1%
MCH_AGPREF 19
R159 1K1%
R153 80.6-1%
C182 470PF MCH_AGPREF_CG
Place MCH_AGPREF circuit near the MCH.
VCC1_8
R190 162-1%
6,11 RAMREF
R181 562-1%
VCC1_8;D4,E6,F6,G6,E7,R6,R7,E8,E9,D10,D11,E12
VCC1_8;E13,E14,F14,T14,E15,P15,B17,C17,C19
VDDQ;F15,R15,J17,L17,N17,T17
GND;A1,A3,G3,J3,L3,N3,R3,V3,B4,D5,L5,U5,B6,D6,D7,V7,B8,D8
GND;D9,J9,K9,L9,M9,V9,B10,J10,K10,L10,M10,C11,J11,K11,L11
GND;M11,V11,C12,D12,J12,K12,L12,M12,B13,D13,V13,T13,D14
GND;B15,D15,B16,D16,E16,F16,A17,E18,V18,A19,H19,K19,M19
GND;P19,T19,D20
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD
MCH
REV: 1.0
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 12-7-1999 15:41
SHEET: 6 OF 37

MCH

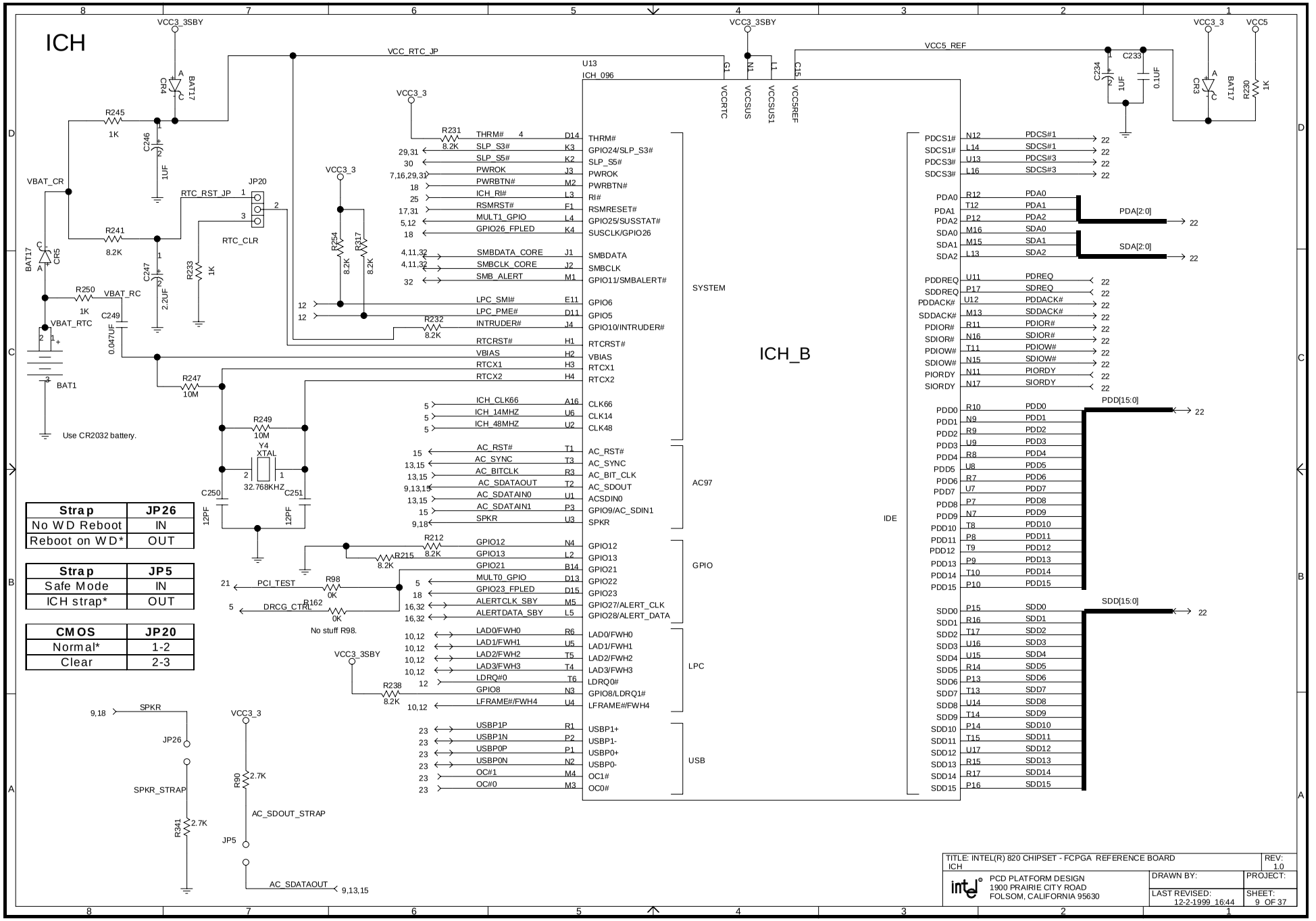


TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD MCH	REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
LAST REVISED: 11-23-1999 9:22	SHEET: 7 OF 37

ICH



TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD ICH		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 12-7-1999 15:41	SHEET: 8 OF 37



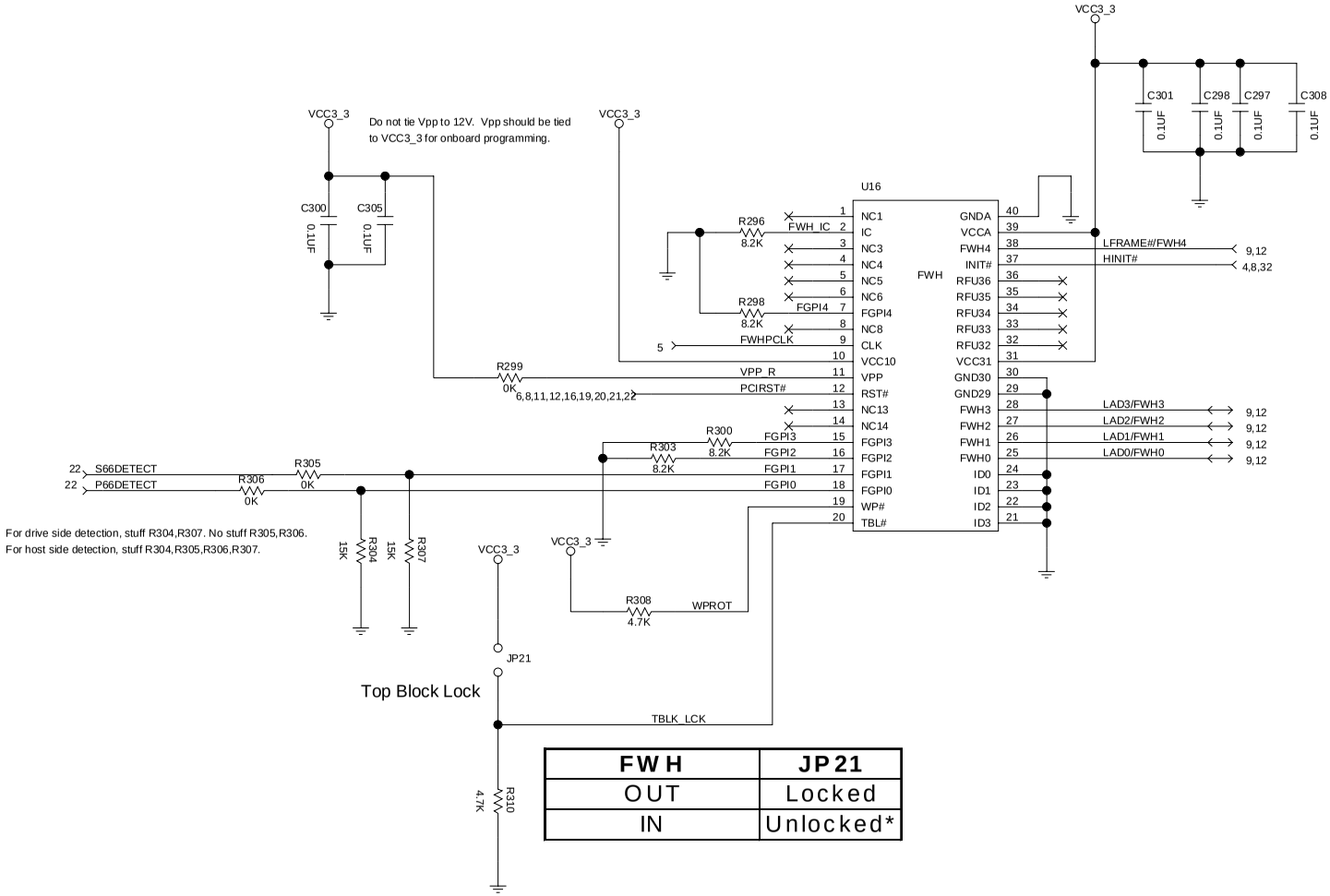
Strap	JP26
No WD Reboot	IN
Reboot on WD*	OUT

Strap	JP5
Safe Mode	IN
ICH strap*	OUT

CMOS	JP20
Normal*	1-2
Clear	2-3

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD ICH			REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:		PROJECT:
	LAST REVISED: 12-2-1999 16:44		SHEET: 9 OF 37

FWH

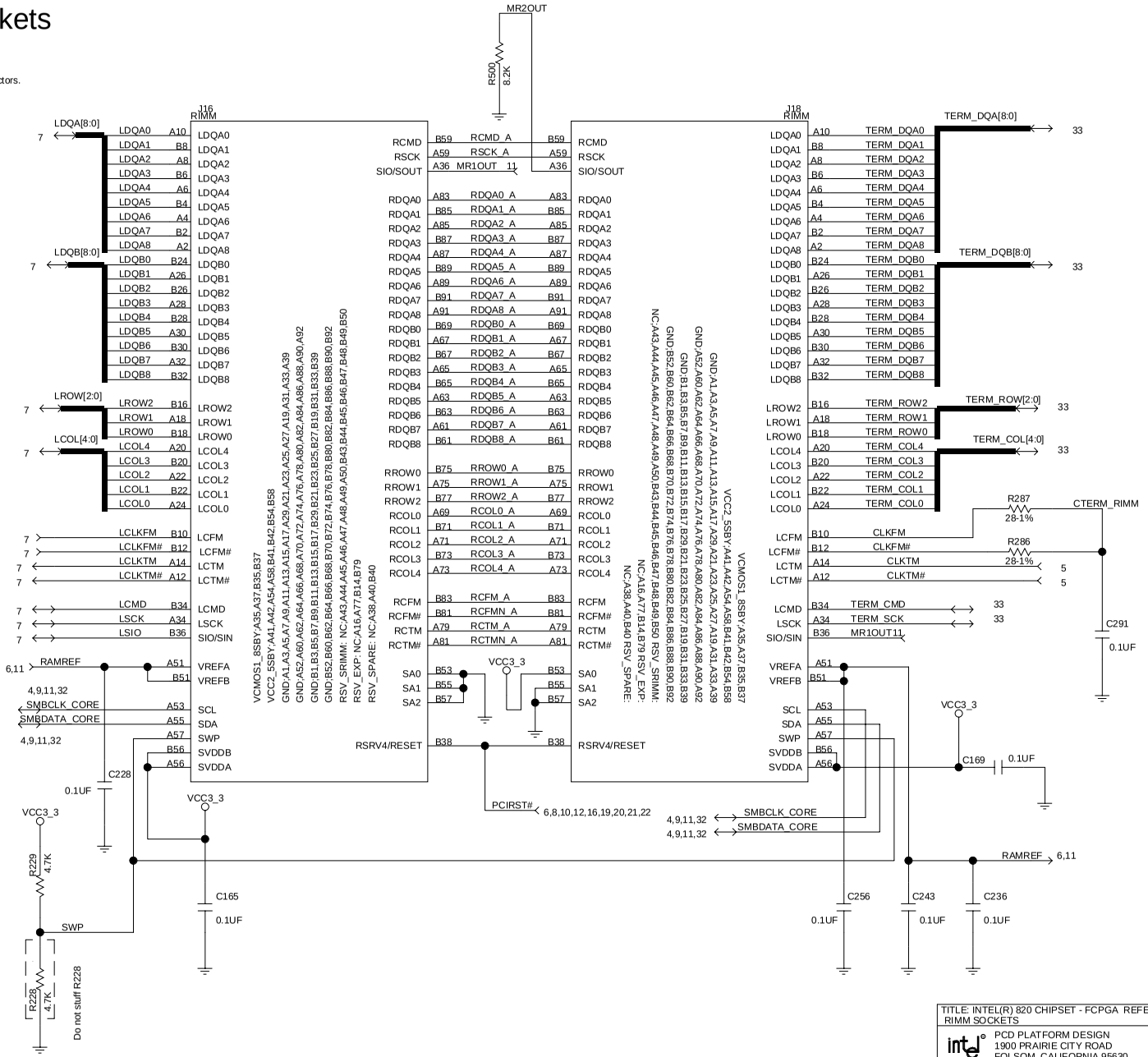


FWH	JP21
OUT	Locked
IN	Unlocked*

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD FWH		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:56	SHEET: 10 OF 37

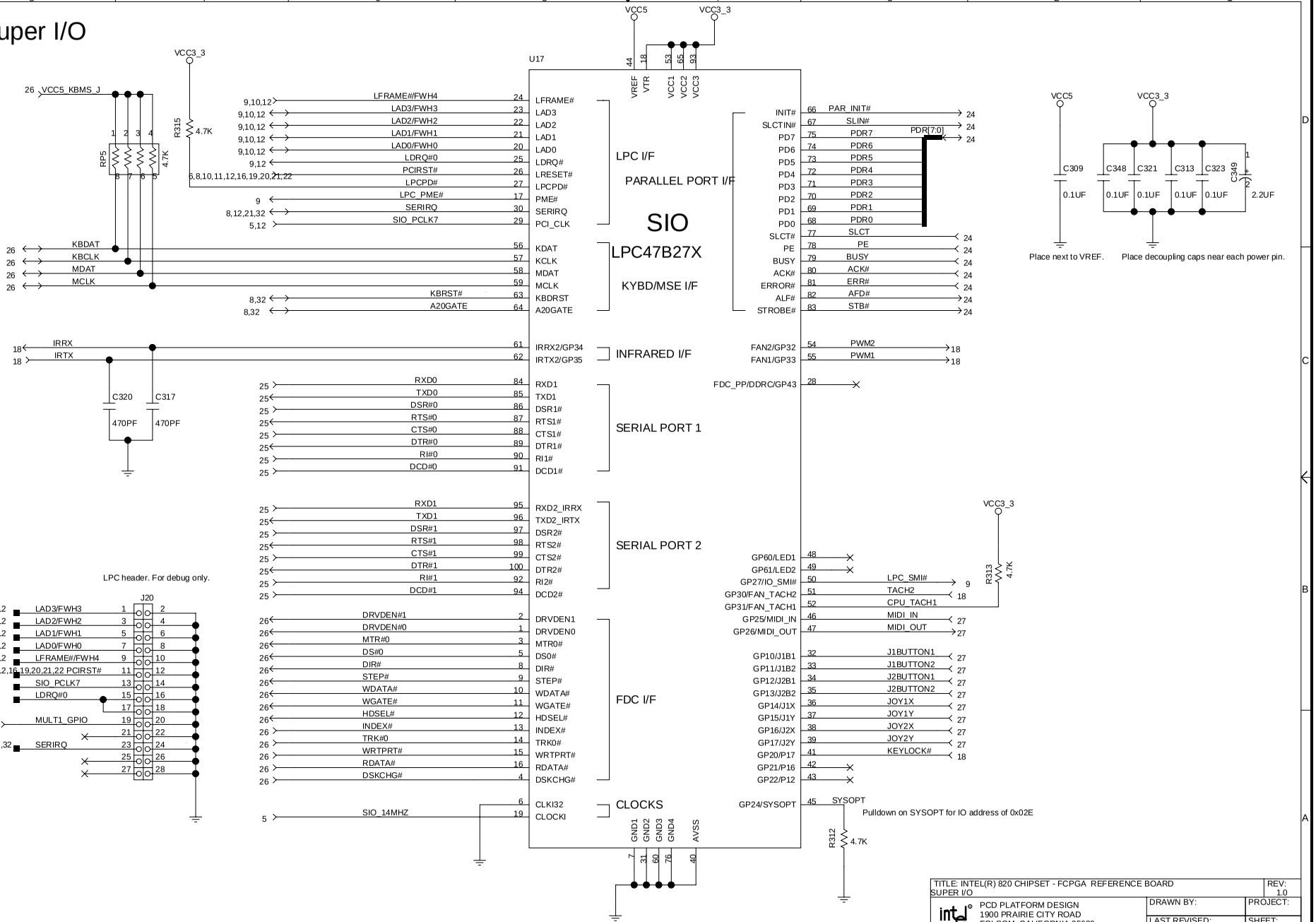
2 RIMM Sockets

As shown, RIMMs are 184-pin connectors.



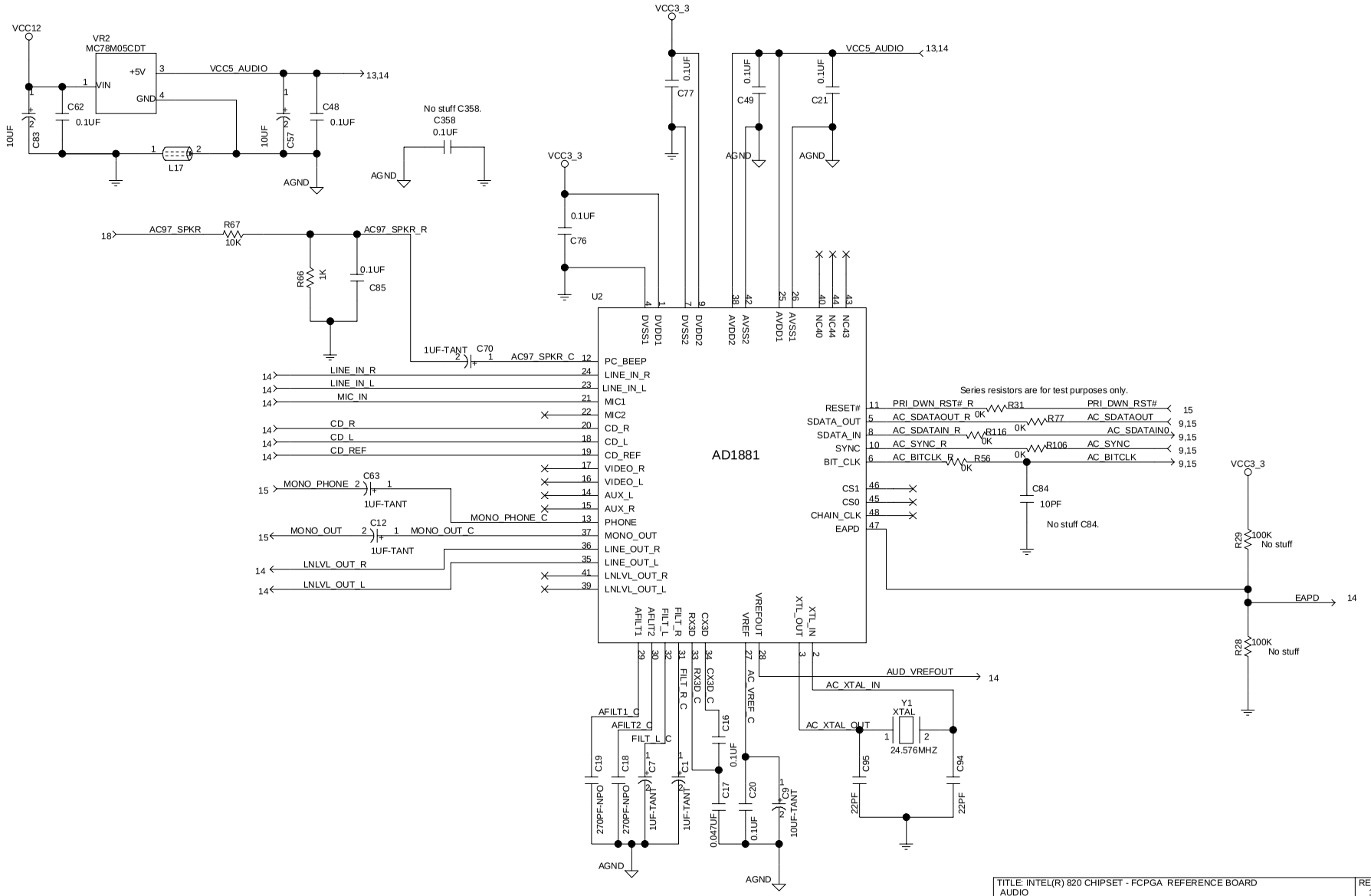
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD RIMM SOCKETS	REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
LAST REVISED: 11-23-1999 11:14	SHEET: 11 OF 37

Super I/O



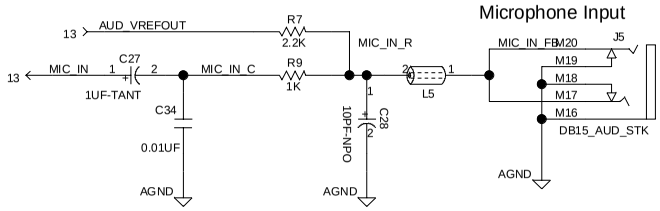
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD SUPER I/O	REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
LAST REVISED: 11-10-1999 8:56	SHEET: 12 OF 37

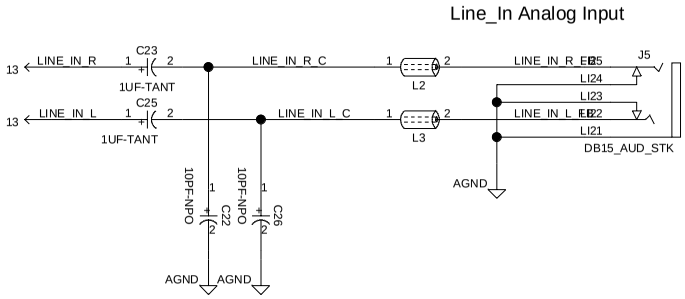
AC’97 Audio

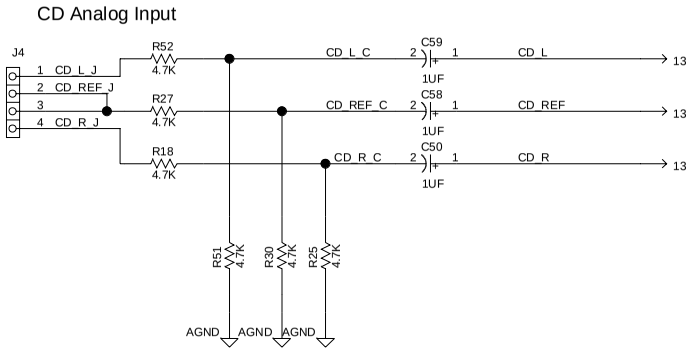


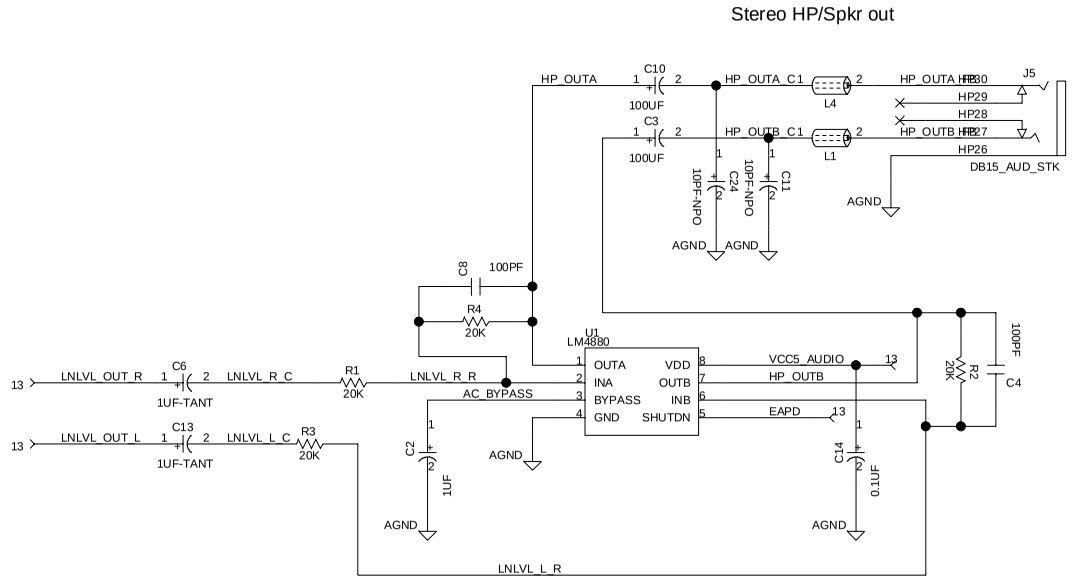
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD AUDIO		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:56	SHEET: 13 OF 37

AC'97 Audio



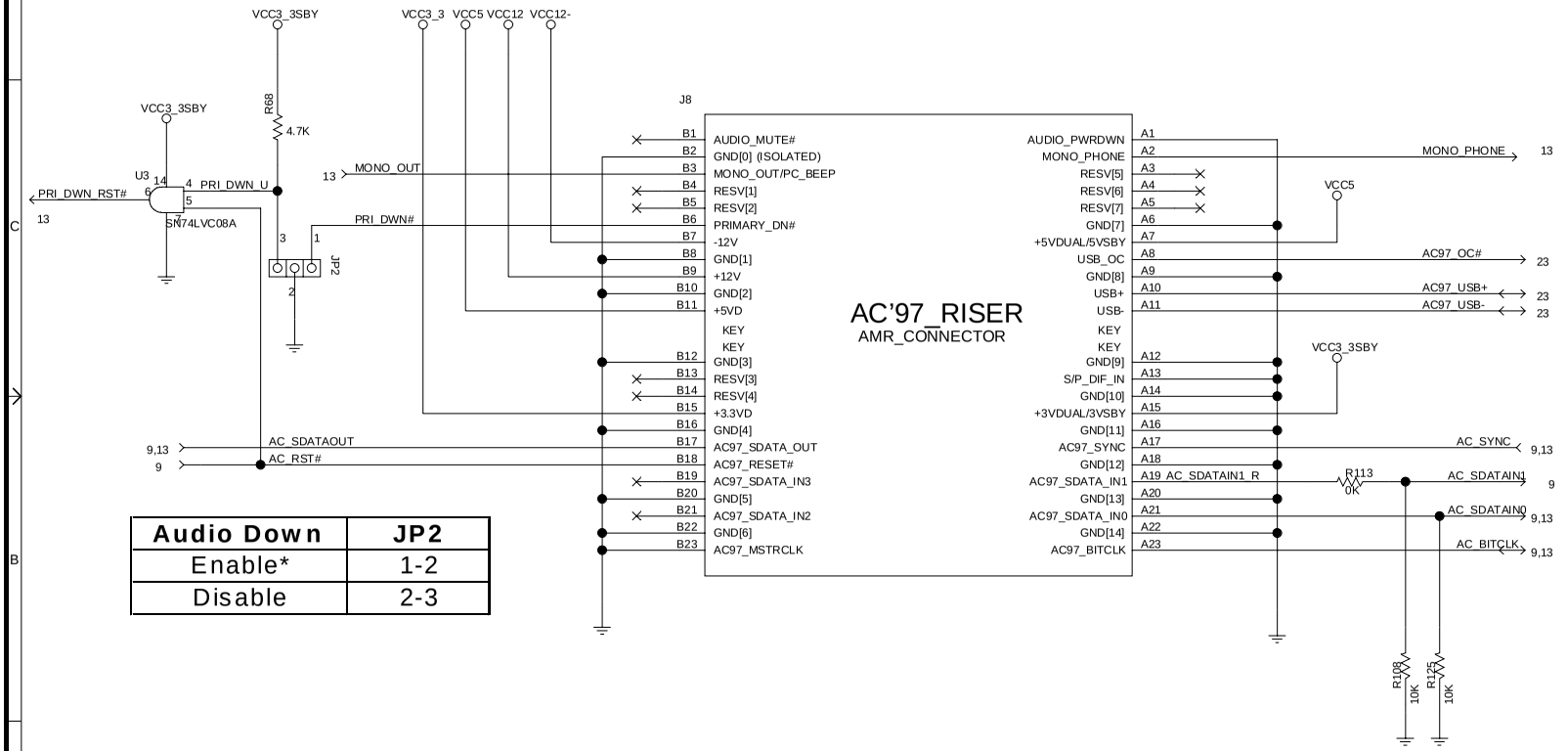






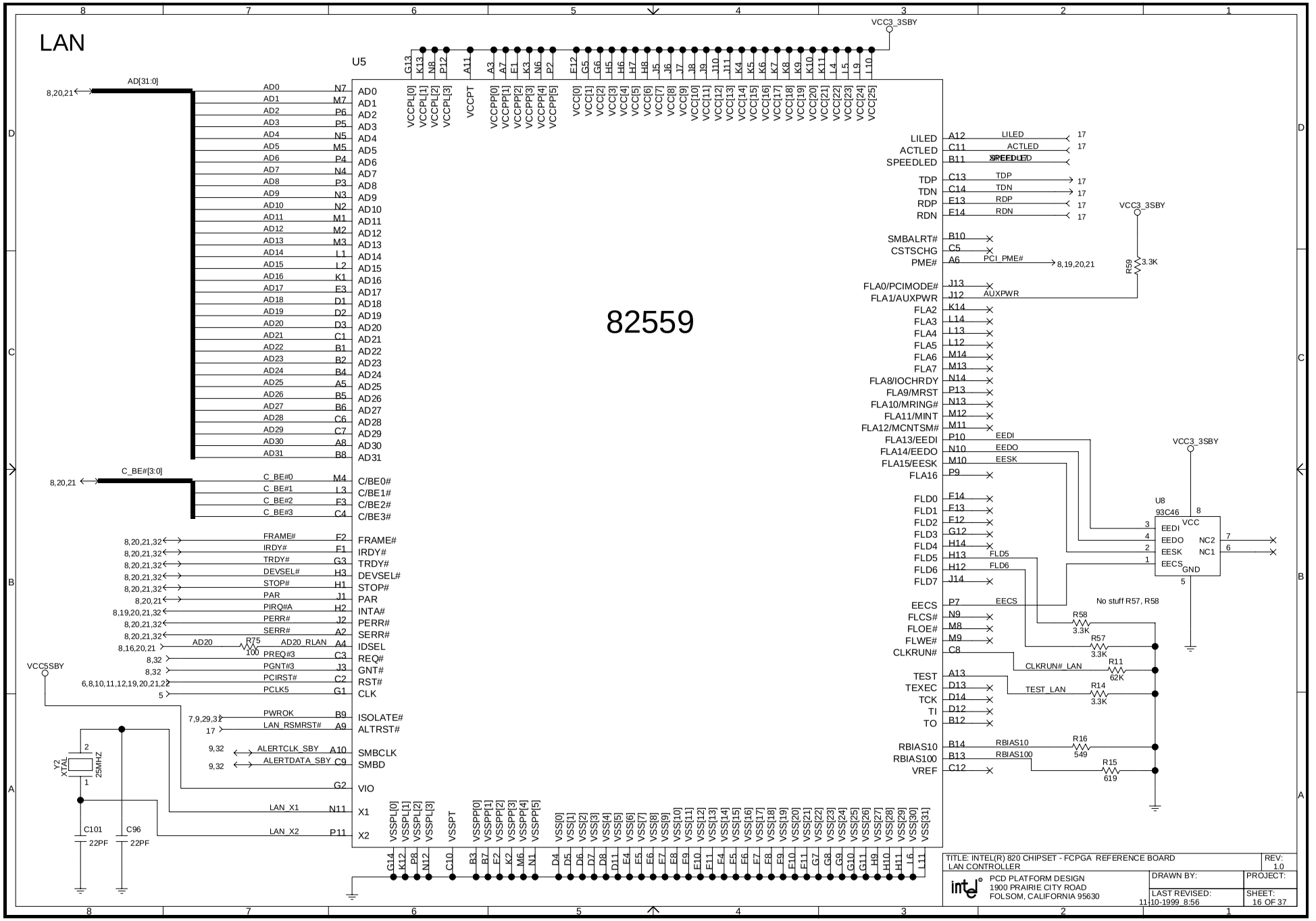
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD AUDIO		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:56	SHEET: 14 OF 37

AC'97 Audio/Modem Riser

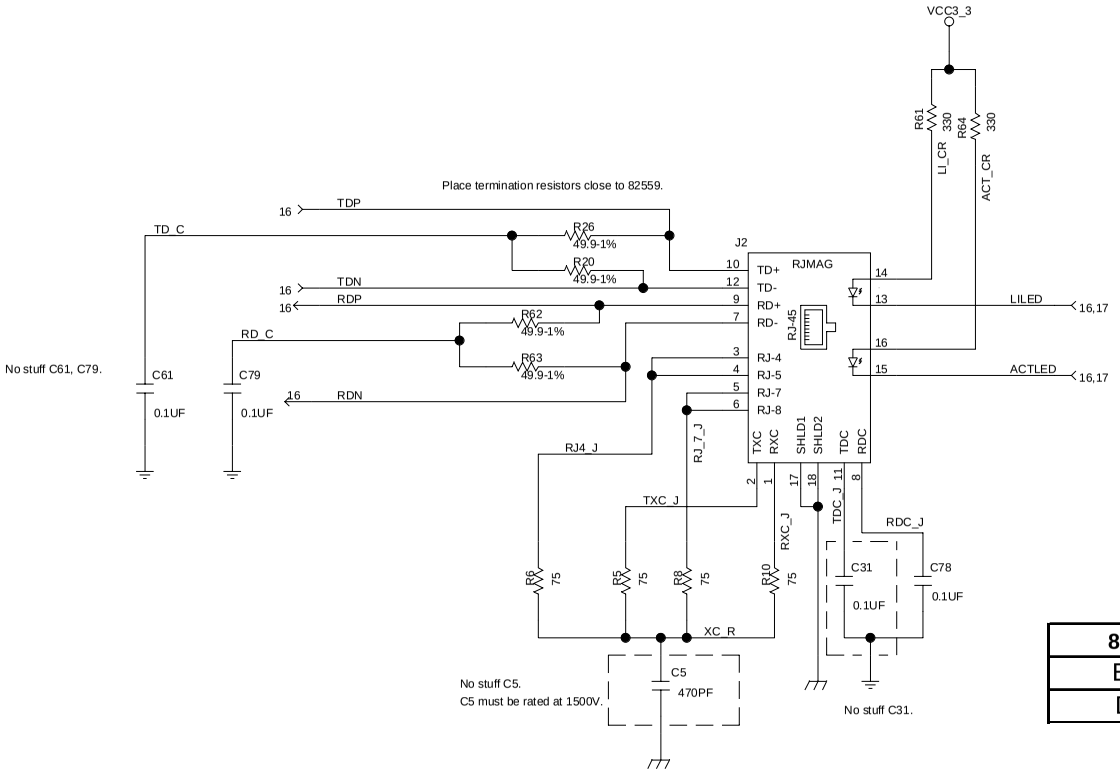


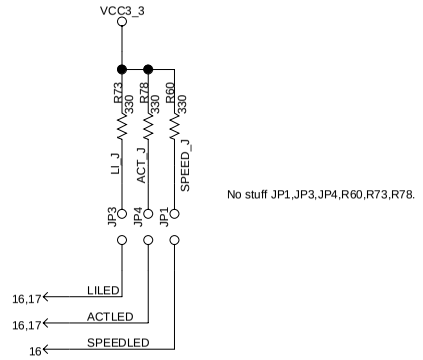
Audio Down	JP2
Enable*	1-2
Disable	2-3

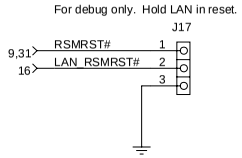
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD AUDIO/MODEM RISER		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED:	SHEET: 15 OF 37


LAN
U5
82559
VCC3_3SBY
AD[31:0]
8,20,21
C_BE#[3:0]
8,20,21
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
PIRQ#A
PERR#
SERR#
AD20
R75
100
AD20_RLAN
PREQ#3
PGNT#3
PCIRST#
PCLK5
VCC5SBY
PWROK
LAN_RSMRST#
ALERTCLK_SBY
ALERTDATA_SBY
Y2
XTAL
25MHZ
LAN_X1
LAN_X2
C101
22PF
C96
22PF
LILED
ACTLED
SPEEDLED
TDP
TDN
RDP
RDN
SMBALRT#
CSTSCHG
PME#
PCI_PME#
8,19,20,21
R59
3.3K
FLA0/PCIMODE#
FLA1/AUXPWR
AUXPWR
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16
EEDI
EEDO
EESK
U8
93C46
VCC
EEDI
EEDO
EESK
EECS
NC2
NC1
GND
FLD5
FLD6
FLD7
EECS
FLCS#
FLOE#
FLWE#
CLKRUN#
No stuff R57, R58
R58
3.3K
R57
3.3K
CLKRUN#_LAN
R11
62K
TEST
TEXEC
TCK
TI
TO
TEST_LAN
R14
3.3K
RBIAS10
RBIAS100
VREF
R16
549
R15
619
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD
LAN CONTROLLER
REV: 1.0
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED:
11-10-1999 8:56
SHEET:
16 OF 37

LAN



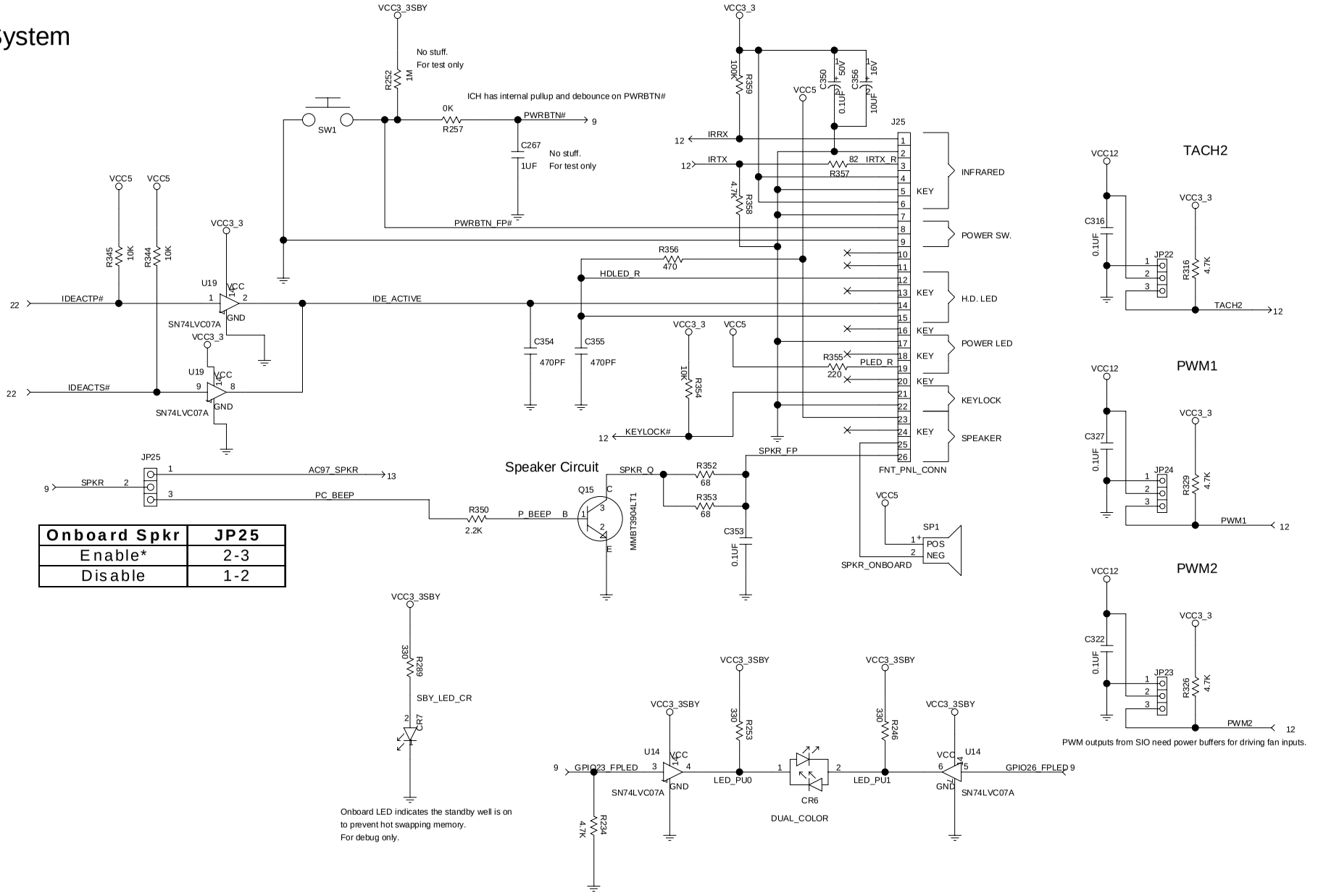




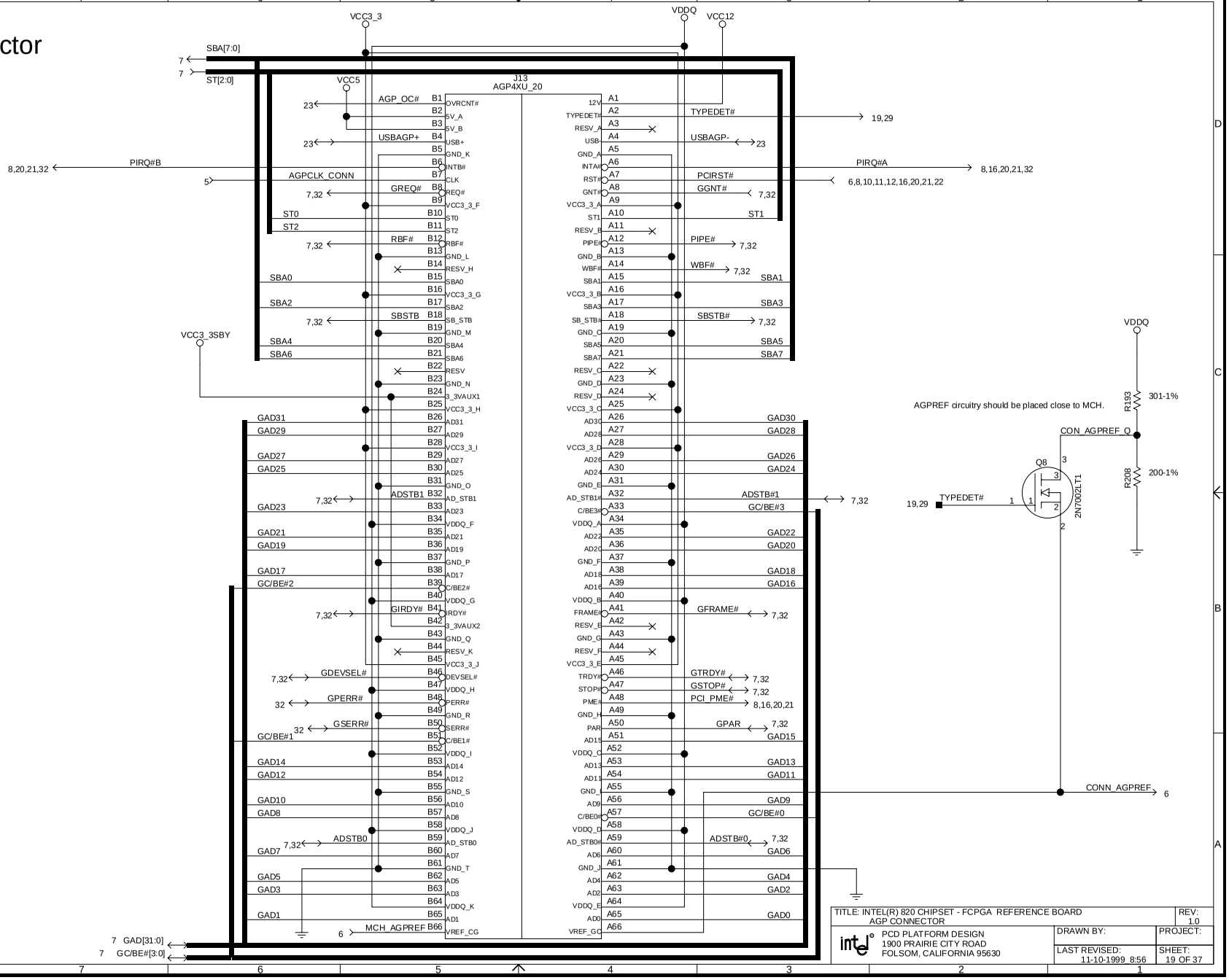
82559 LAN	J17
Enable*	1-2
Disable	2-3

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD LAN		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:56	SHEET: 17 OF 37

System

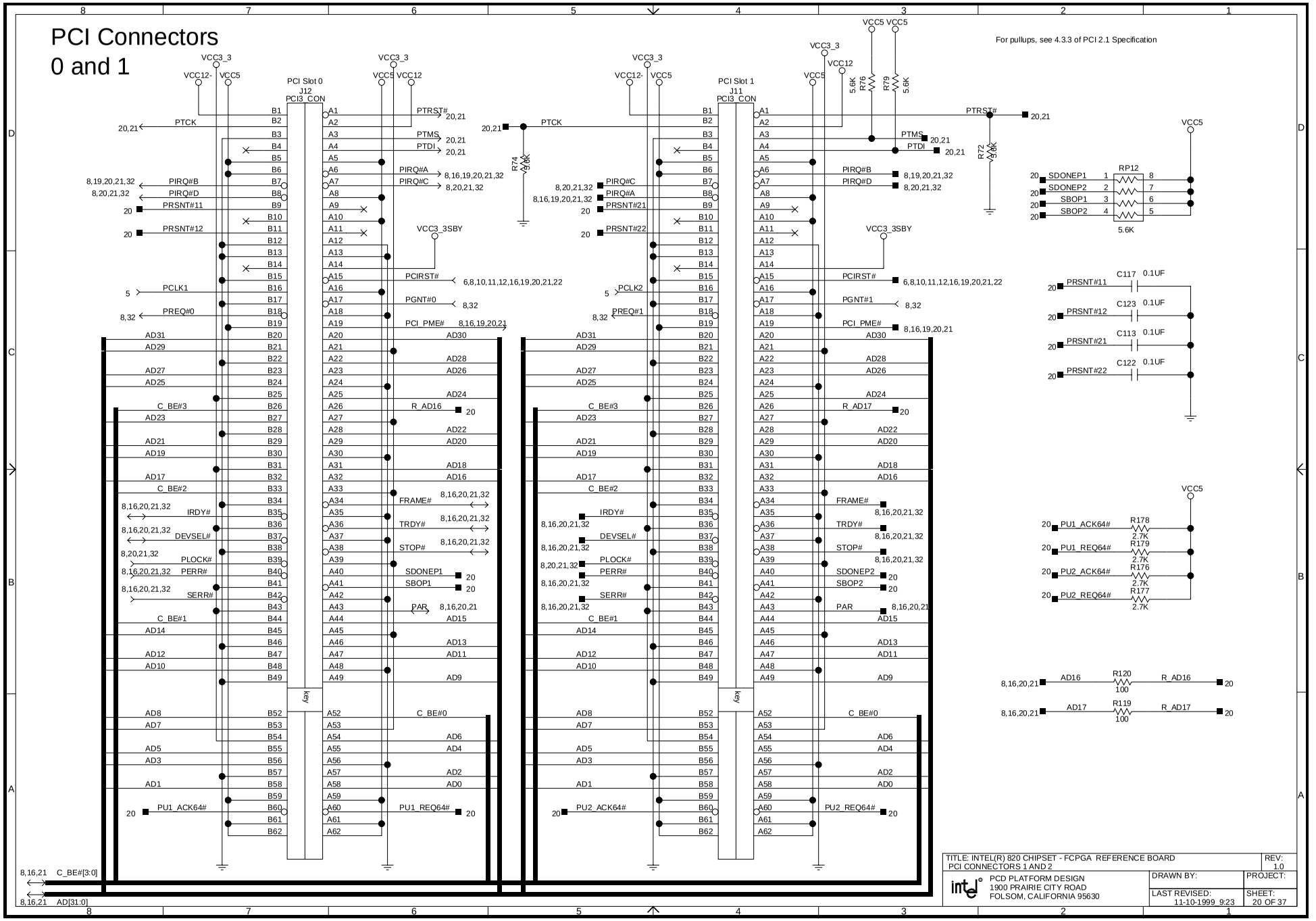

VCC3_3SBY
No stuff.
For test only
R252
1M
ICH has internal pullup and debounce on PWRBTN#
0K
R257
PWRBTN#
9
SW1
C267
1UF
No stuff.
For test only
PWRBTN_FP#
VCC3_3
R359
100K
VCC5
C350
0.1UF
50V
C356
10UF
16V
J25
IRRX
12
IRTX
12
82
IRTX_R
R357
R358
4.7K
INFRARED
KEY
POWER SW.
R356
470
HDLED_R
H.D. LED
KEY
POWER LED
PLED_R
R355
220
KEY
KEYLOCK
KEY
SPEAKER
FNT_PNL_CONN
VCC5
VCC5
R345
10K
R344
10K
VCC3_3
U19
VCC
GND
SN74LVC07A
IDEACTP#
22
IDE_ACTIVE
C354
470PF
C355
470PF
IDEACTS#
22
SN74LVC07A
VCC3_3
VCC5
R354
10K
KEYLOCK#
12
SPKR_FP
JP25
SPKR
9
AC97_SPKR
13
PC_BEEP
Speaker Circuit
SPKR_Q
R352
68
R353
68
R350
2.2K
P_BEEP
B
Q15
MMBT3904LT1
C353
0.1UF
VCC5
SP1
POS
NEG
SPKR_ONBOARD
Onboard Spkr
JP25
Enable*
2-3
Disable
1-2
VCC3_3SBY
R289
330
SBY_LED_CR
CR7
Onboard LED indicates the standby well is on
to prevent hot swapping memory.
For debug only.
VCC3_3SBY
R253
330
LED_PU0
VCC3_3SBY
R246
330
LED_PU1
VCC3_3SBY
U14
VCC
GND
SN74LVC07A
GPIO23_FPLED
9
R234
4.7K
CR6
DUAL_COLOR
GPIO26_FPLED
9
TACH2
VCC12
C316
0.1UF
VCC3_3
JP22
R316
4.7K
TACH2
12
PWM1
VCC12
C327
0.1UF
VCC3_3
JP24
R329
4.7K
PWM1
12
PWM2
VCC12
C322
0.1UF
VCC3_3
JP23
R326
4.7K
PWM2
12
PWM outputs from SIO need power buffers for driving fan inputs.
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD
SYSTEM
REV: 1.0
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-10-1999 8:56
SHEET: 18 OF 37

AGP Connector



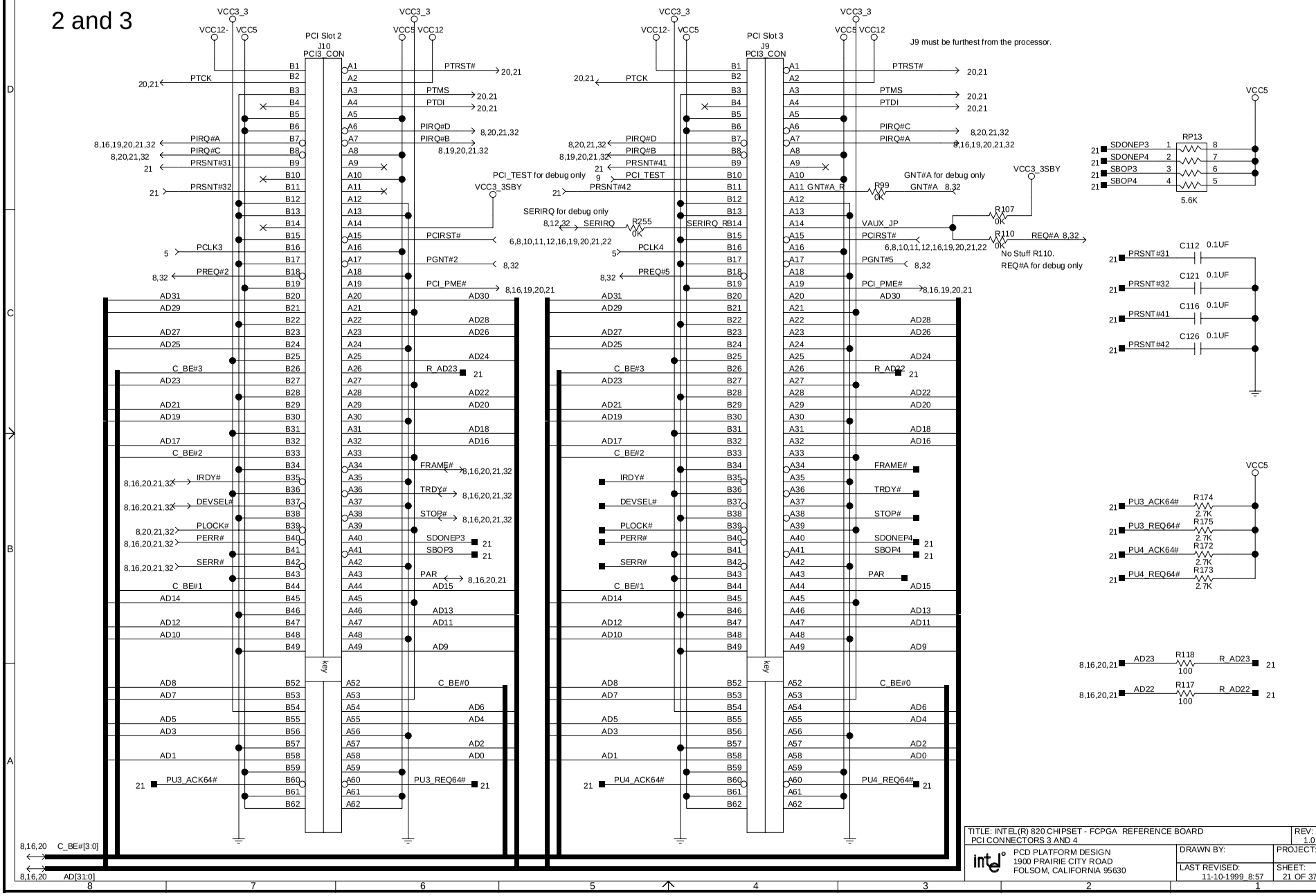
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD AGP CONNECTOR		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:56	SHEET: 19 OF 37

PCI Connectors 0 and 1



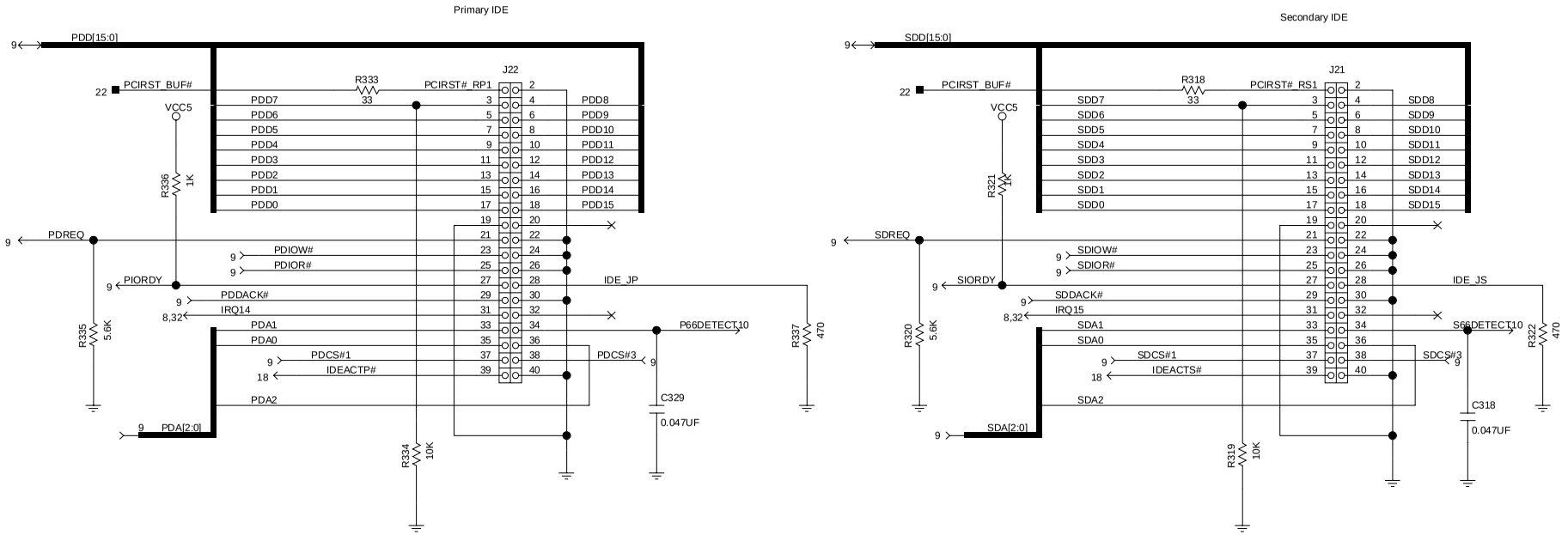
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD PCI CONNECTORS 1 AND 2	REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
LAST REVISED: 11-10-1999 9:23	SHEET: 20 OF 37

PCI Connectors
2 and 3



TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD PCI CONNECTORS 3 AND 4	REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
	LAST REVISED: 11-10-1999 8:57 / SHEET: 21 OF 37

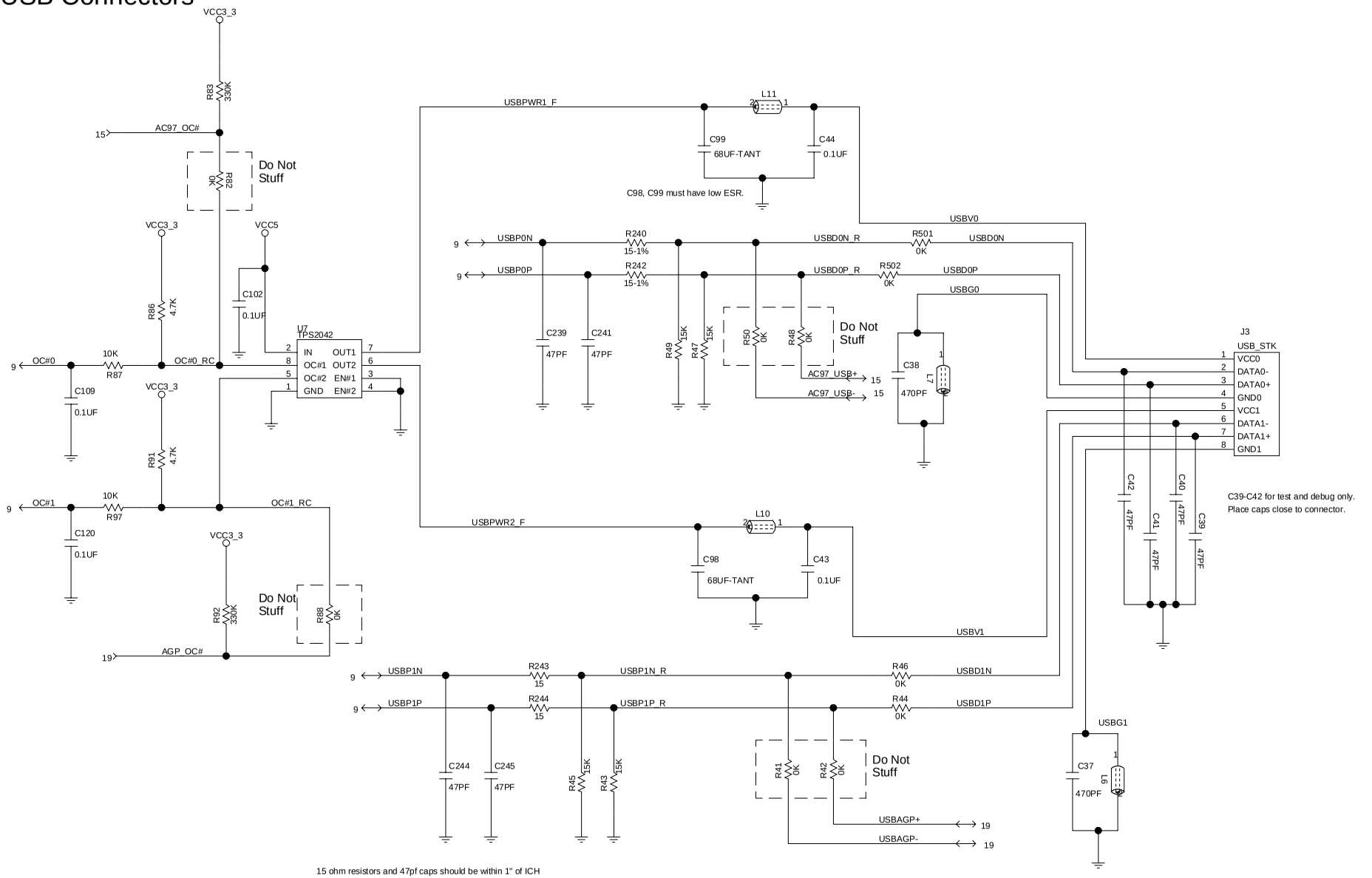
IDE Connectors



For drive side detection, stuff C329,C318.
For host side detection, no stuff C329,C318.
P66DETECT and S66DETECT can be connected to a GPI for BIOS cable detection.

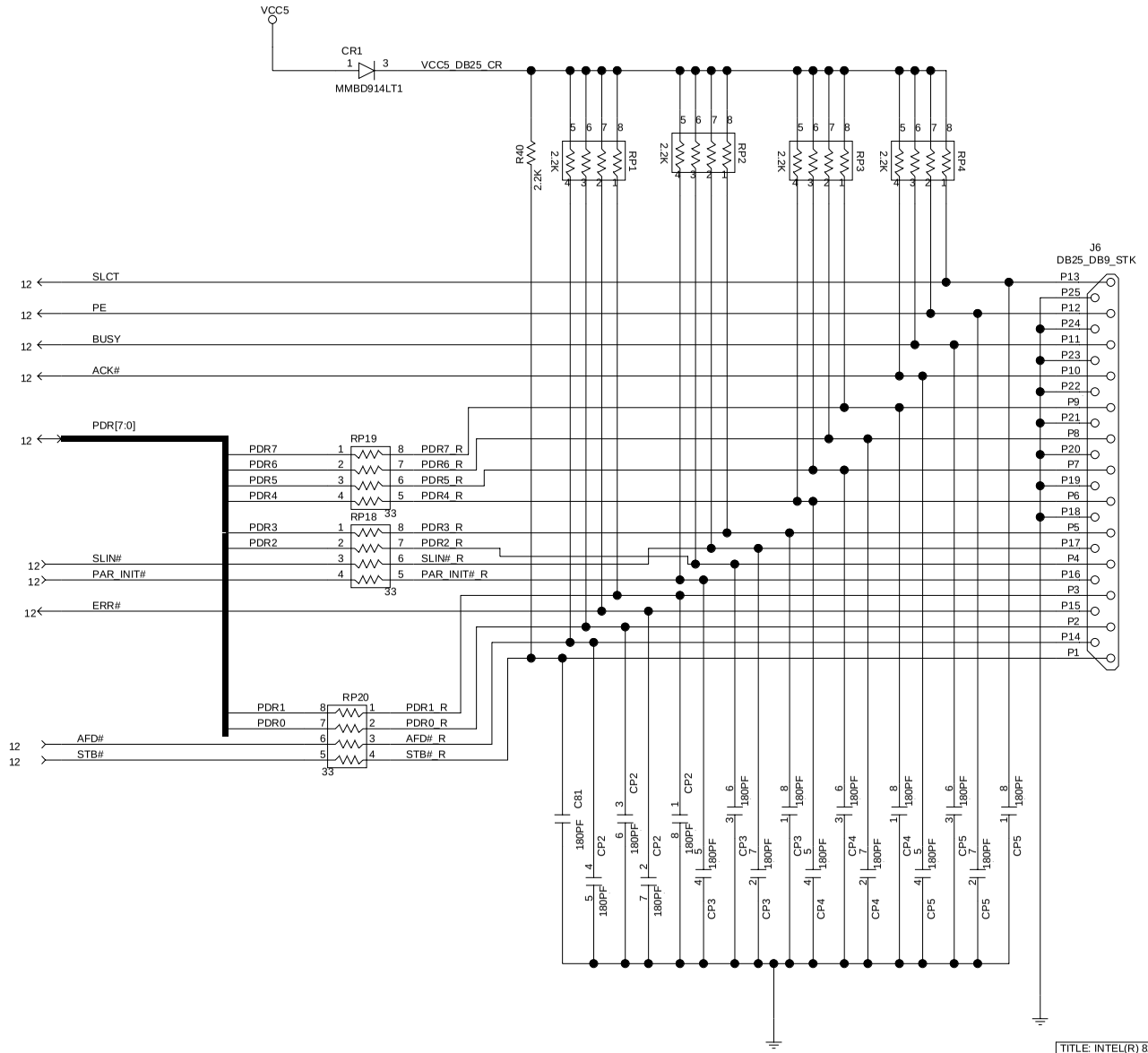
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD IDE CONNECTORS		REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:57	SHEET: 22 OF 37

USB Connectors



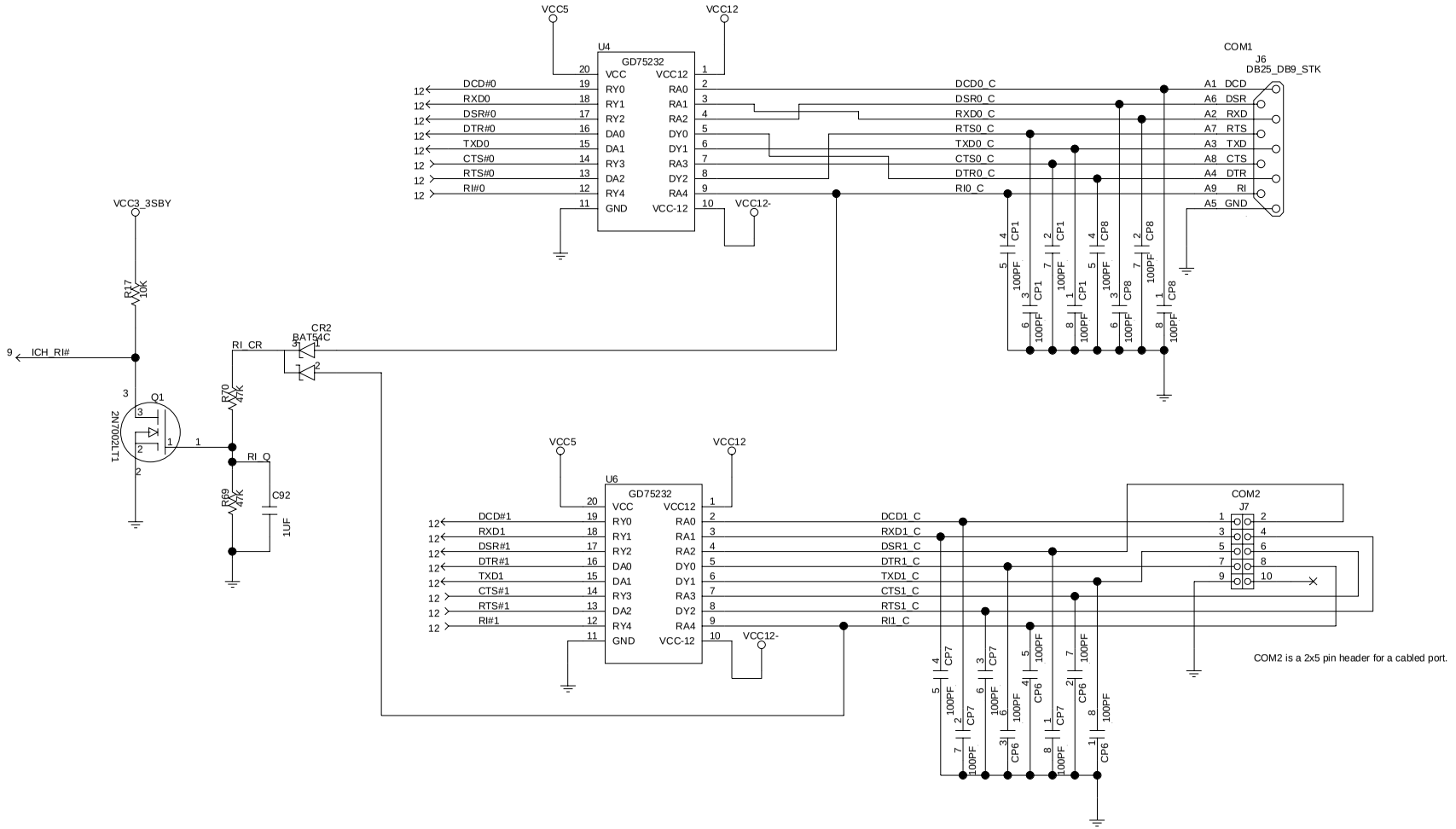
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD USB CONNECTORS		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:57	SHEET: 23 OF 37

Parallel Port



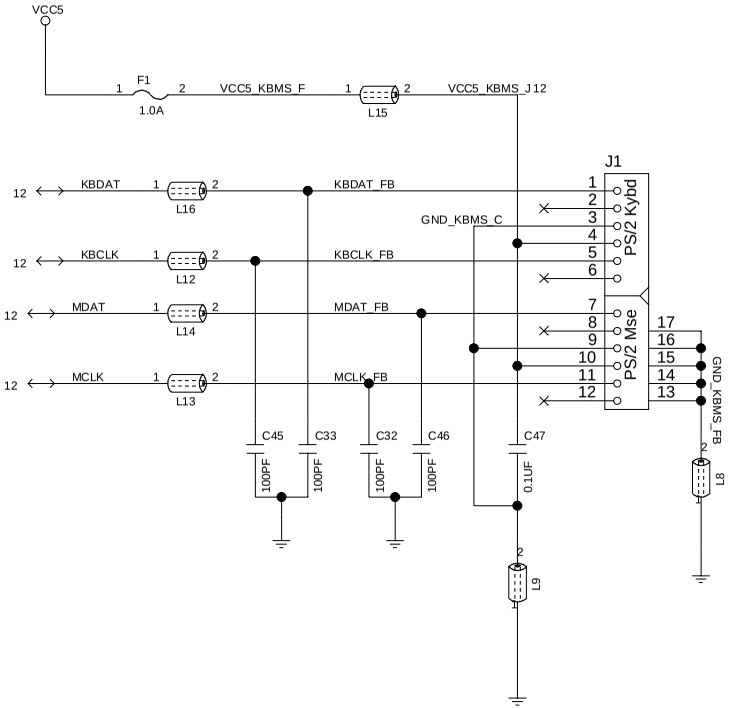
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD PARALLEL PORT		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:57	SHEET: 24 OF 37

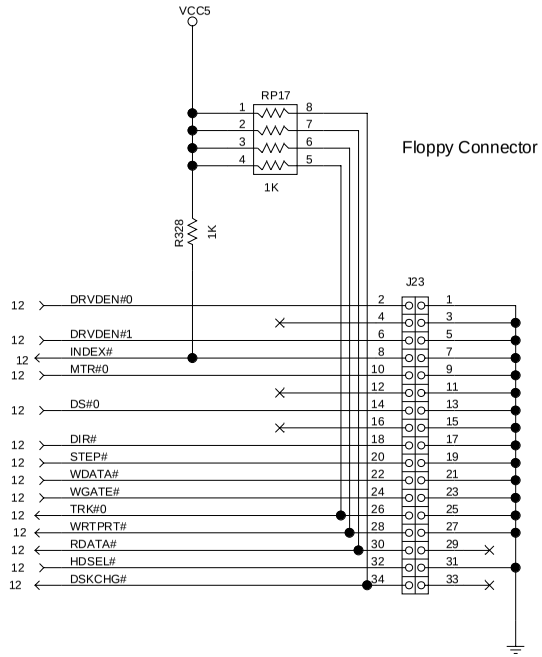
Serial Ports



TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD SERIAL PORTS		REV: 1.0
intel® PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:57	SHEET: 25 OF 37

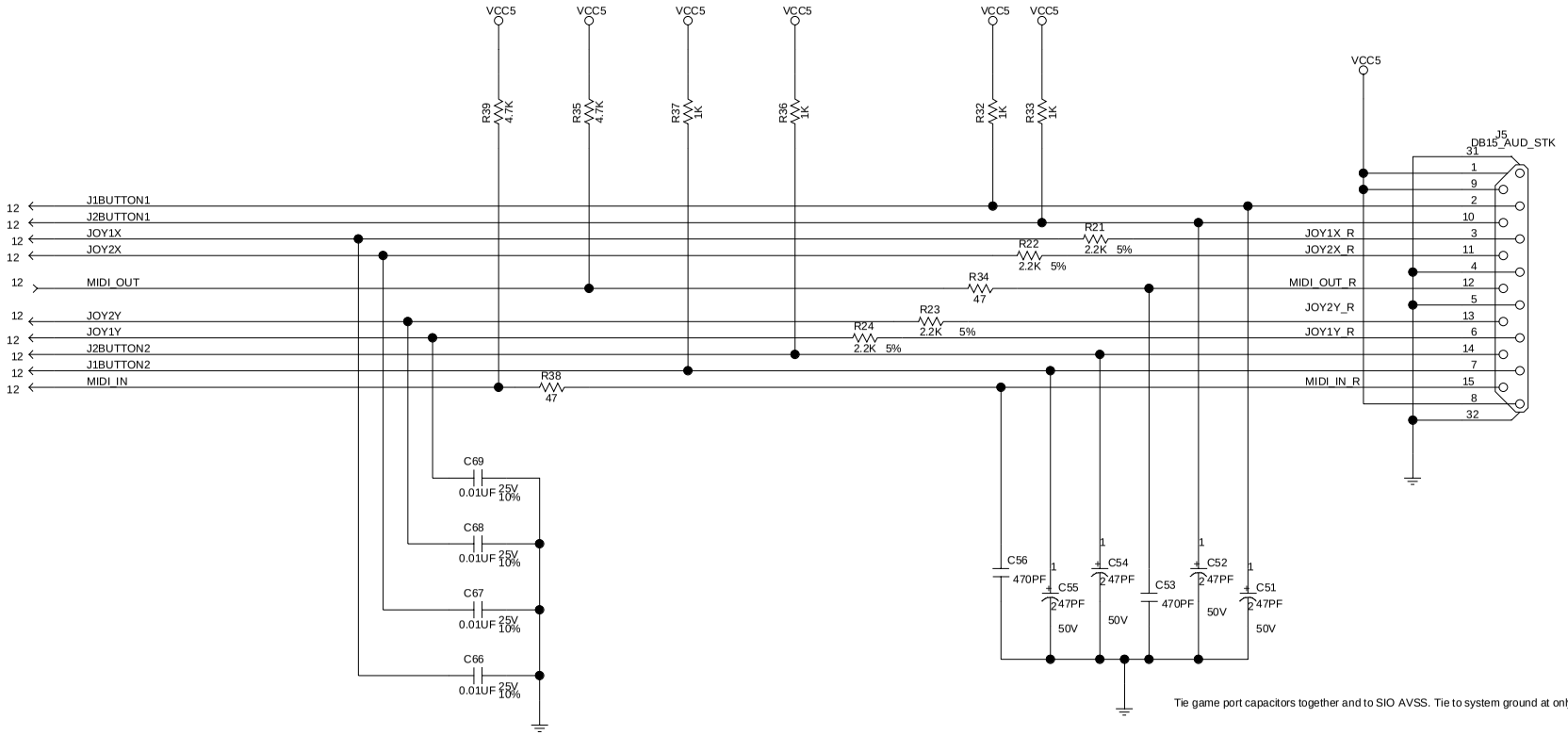
Keyboard/Mouse/Floppy





TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD KEYBOARD/MOUSE/FLOPPY		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:57	SHEET: 26 OF 37

Game Port

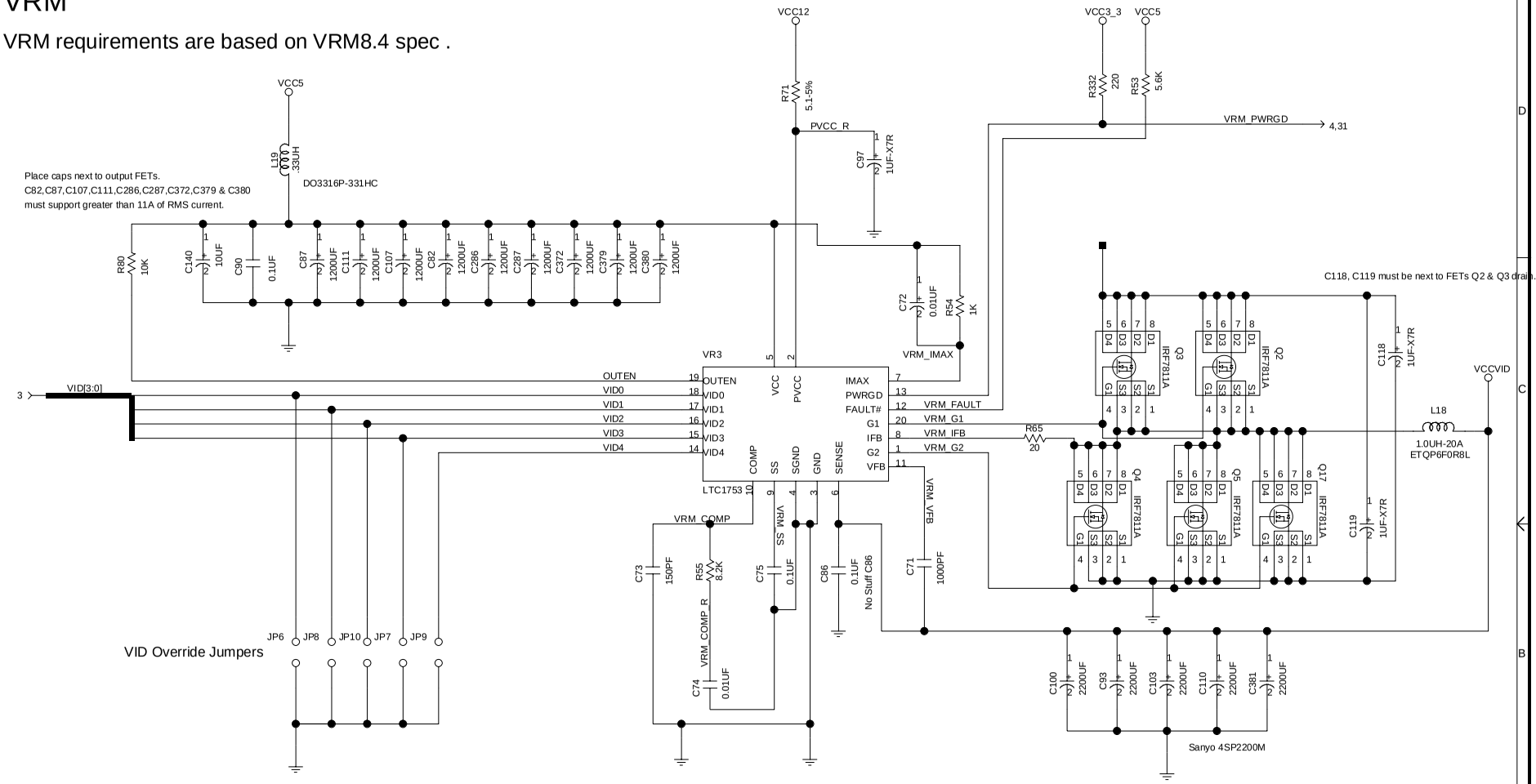


Tie game port capacitors together and to SIO AVSS. Tie to system ground at only a single point.

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD GAME PORT		REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED:	SHEET: 27 OF 37

VRM

VRM requirements are based on VRM8.4 spec .

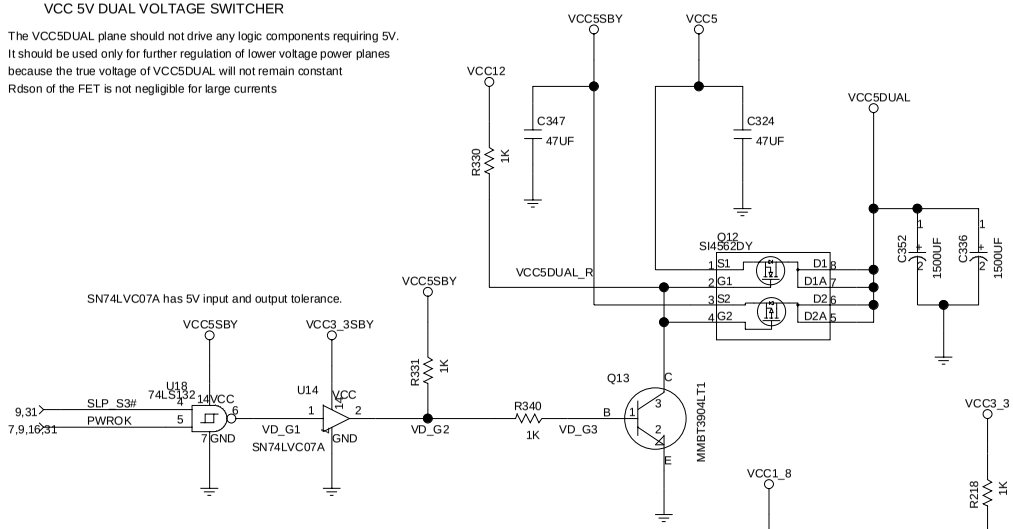


TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD VRM 8.4		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 12-8-1999 16:15	SHEET: 28 OF 37

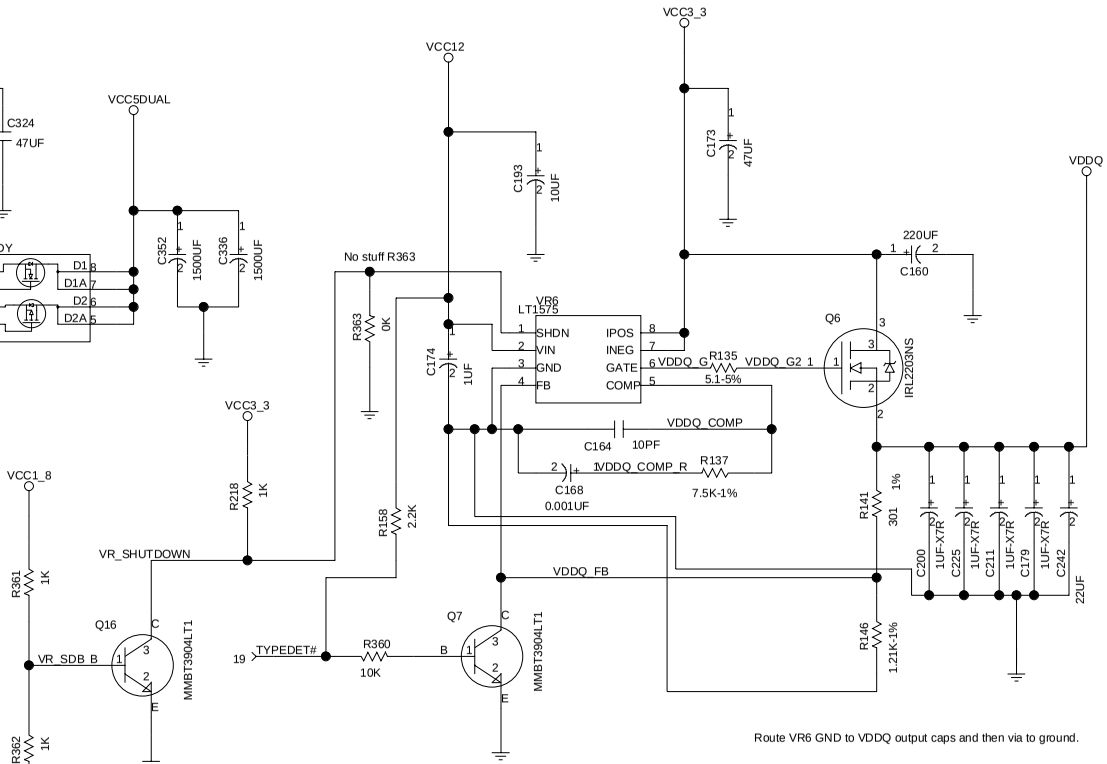
Voltage Regulators

VCC 5V DUAL VOLTAGE SWITCHER

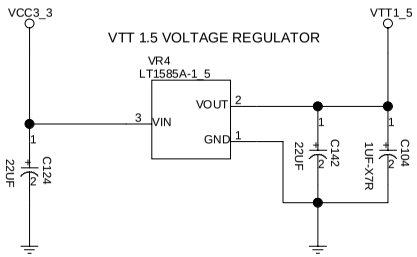
The VCC5DUAL plane should not drive any logic components requiring 5V.
It should be used only for further regulation of lower voltage power planes
because the true voltage of VCC5DUAL will not remain constant
Rdson of the FET is not negligible for large currents



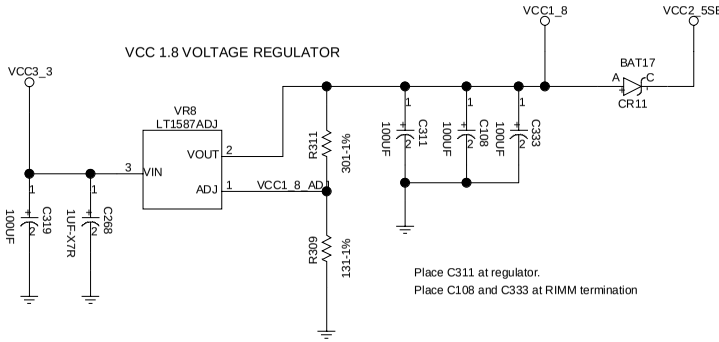
AGP VDDQ VOLTAGE REGULATOR



VTT 1.5 VOLTAGE REGULATOR

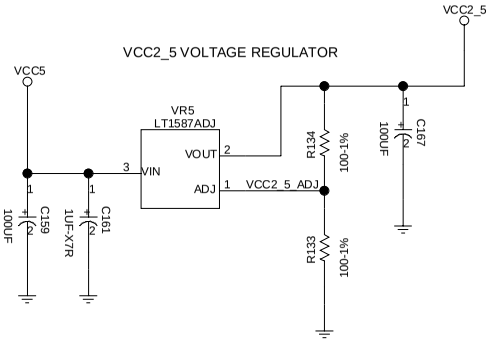


VCC 1.8 VOLTAGE REGULATOR

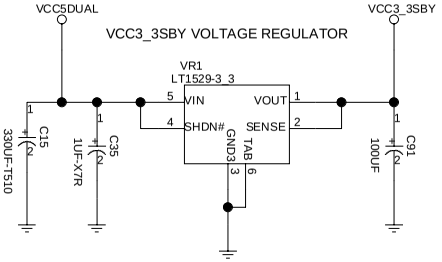


Place C311 at regulator.
Place C108 and C333 at RIMM termination

VCC2_5 VOLTAGE REGULATOR

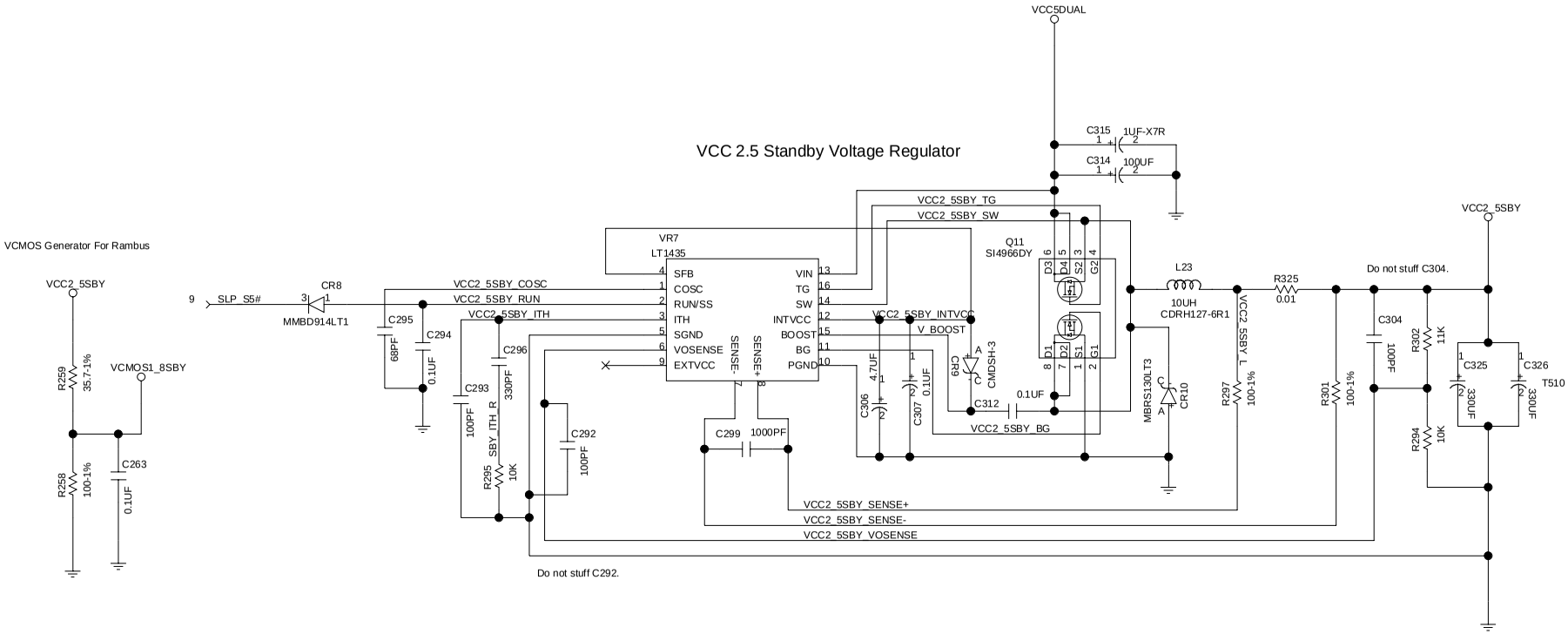


VCC3_3SBY VOLTAGE REGULATOR



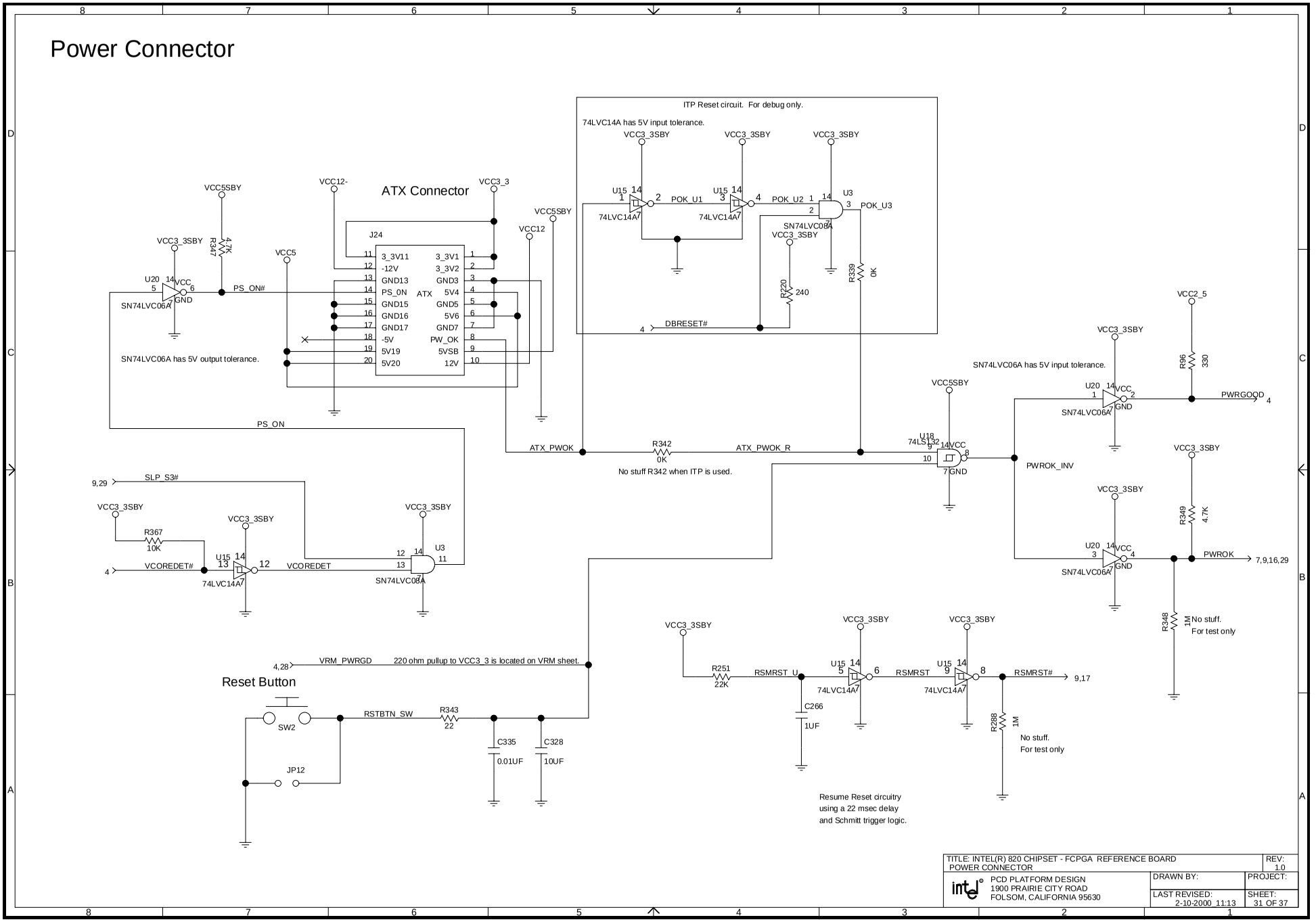
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD VOLTAGE REGULATORS		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:57	SHEET: 29 OF 37

Voltage Regulators



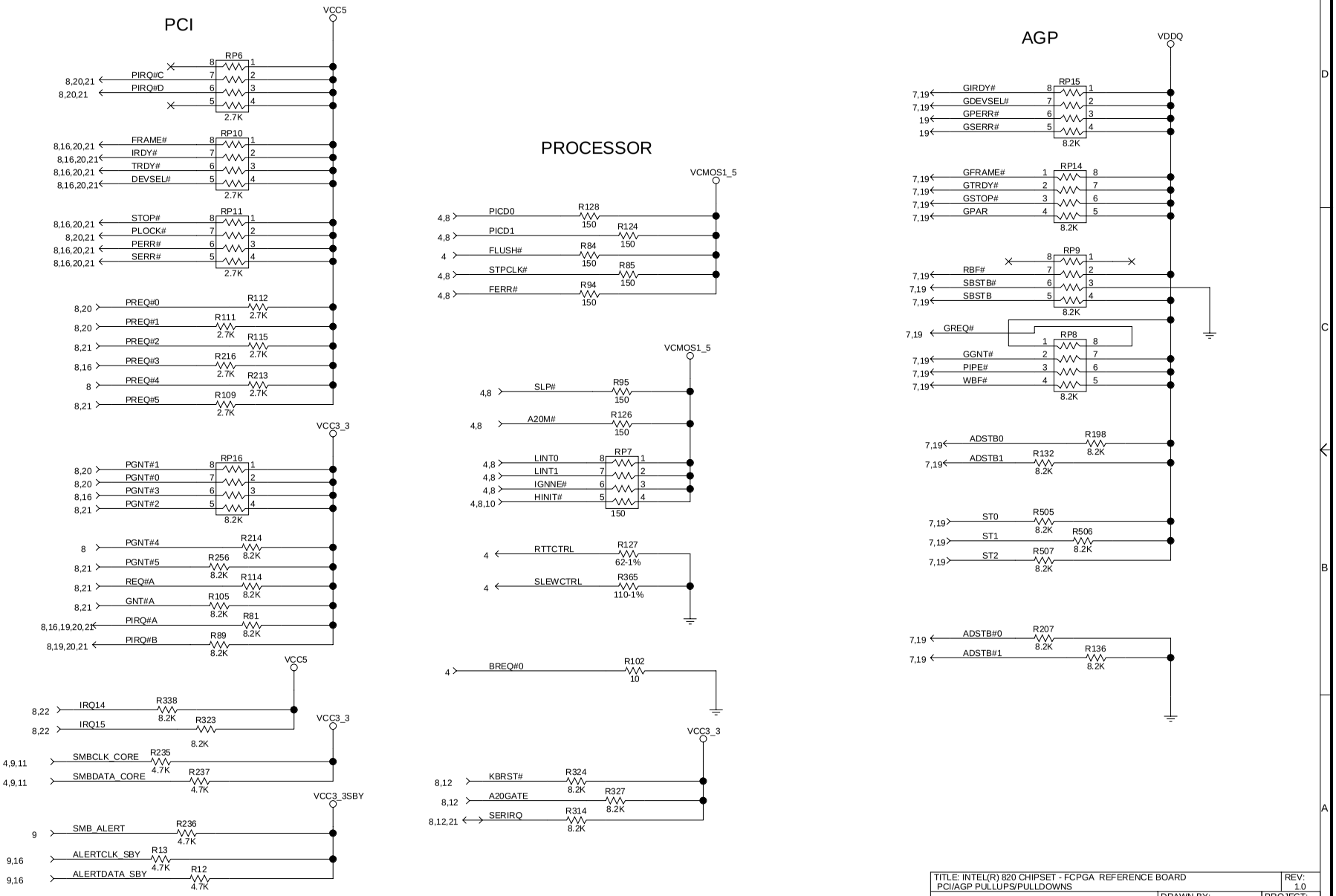
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD VOLTAGE REGULATORS		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-10-1999 8:57	SHEET: 30 OF 37

Power Connector



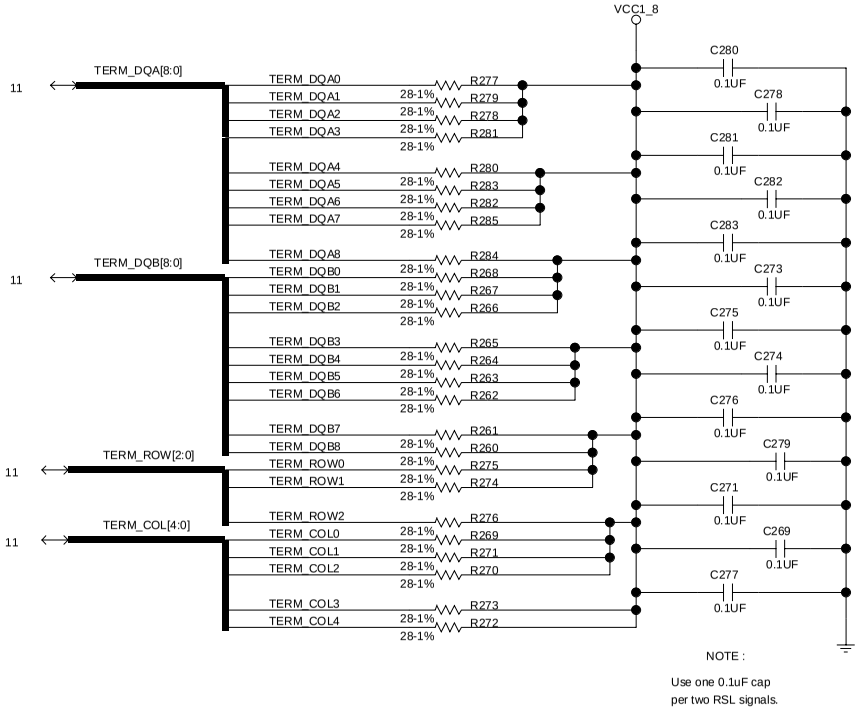
TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD POWER CONNECTOR		REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 2-10-2000 11:13	SHEET: 31 OF 37

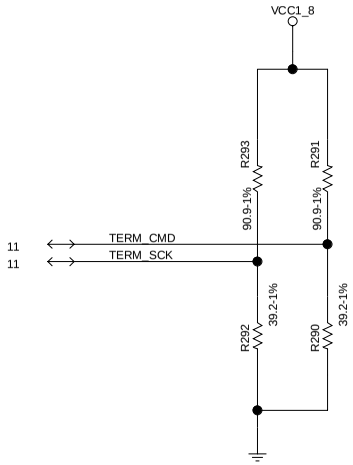
PCI/AGP Pullups/Pulldowns



TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD PCI/AGP PULLUPS/PULLDOWNS		REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 12-7-1999 15:29	SHEET: 32 OF 37

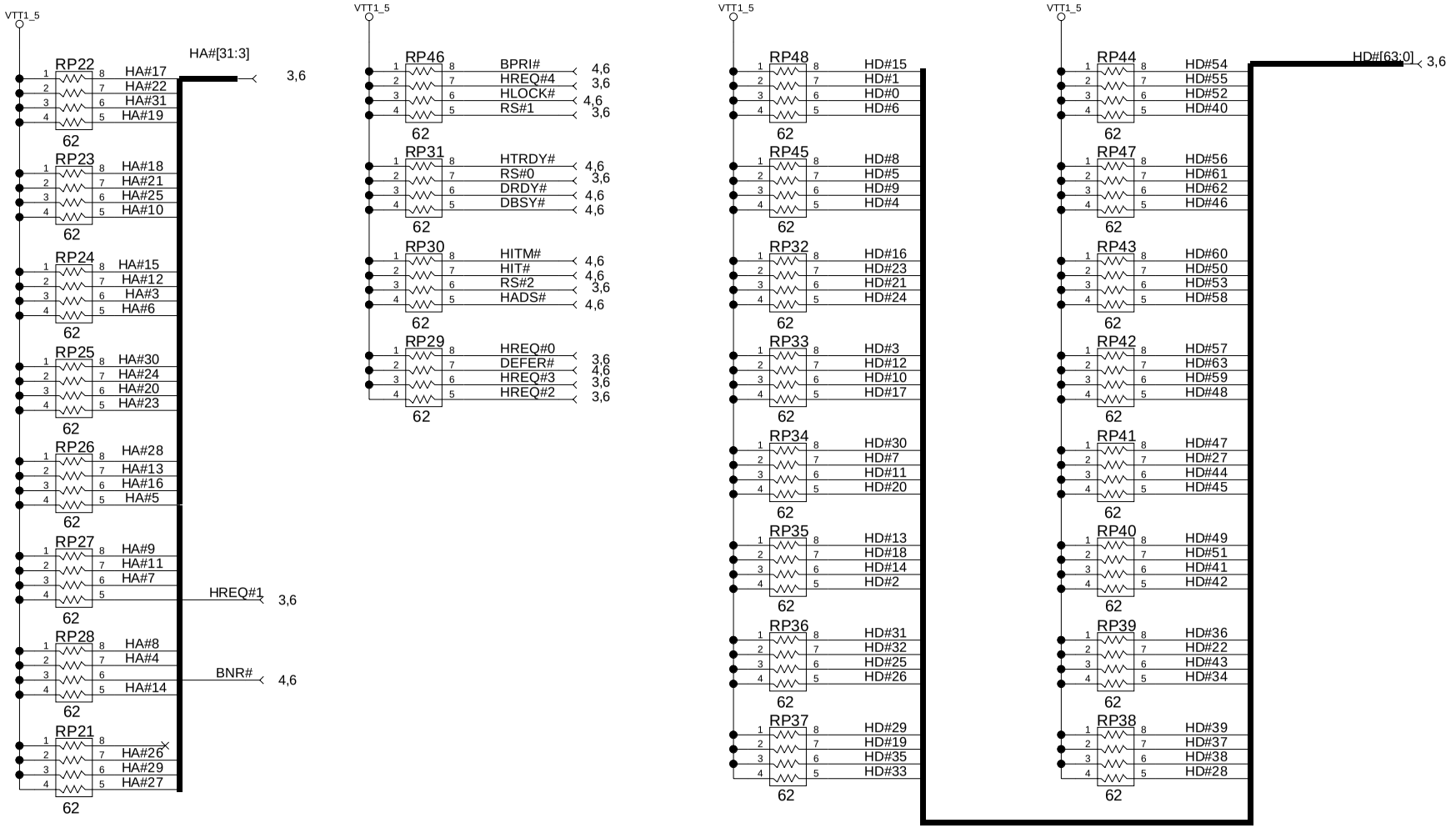
Rambus Termination





TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD RAMBUS TERMINATION		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-23-1999 11:04	SHEET: 33 OF 37

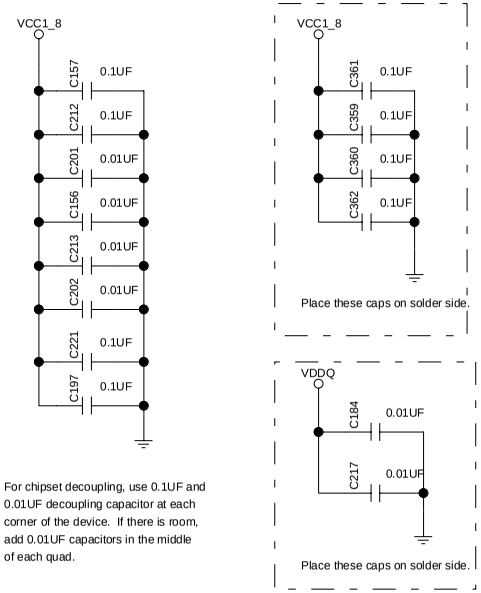
AGTL+ Termination



TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD AGTL+ TERMINATION		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 12-8-1999 8:18	SHEET: 34 OF 37

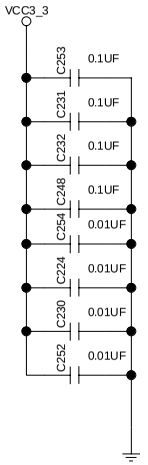
Decoupling

MCH Decoupling

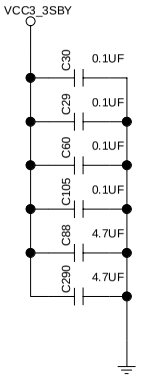


For chipset decoupling, use 0.1UF and 0.01UF decoupling capacitor at each corner of the device. If there is room, add 0.01UF capacitors in the middle of each quad.

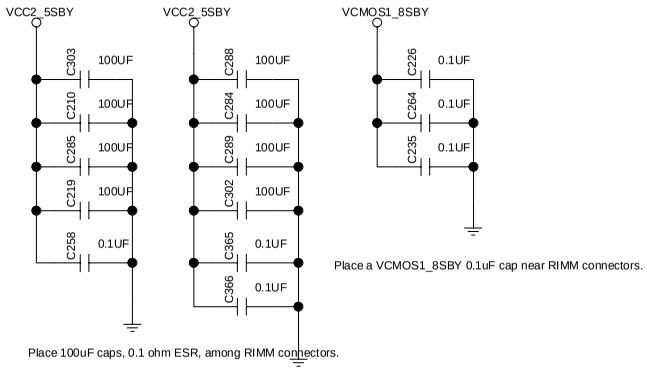
ICH Decoupling



82559 Decoupling.



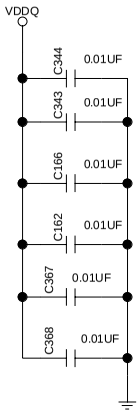
RIMM Decoupling



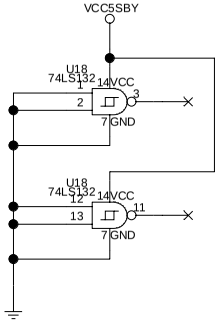
Place 100uF caps, 0.1 ohm ESR, among RIMM connectors.

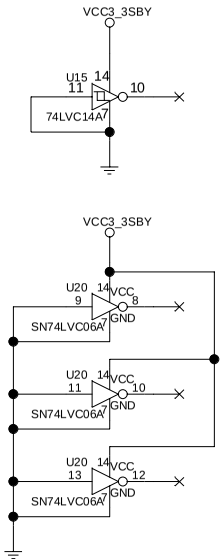
Place a VCMOS1_8SBY 0.1uF cap near RIMM connectors.

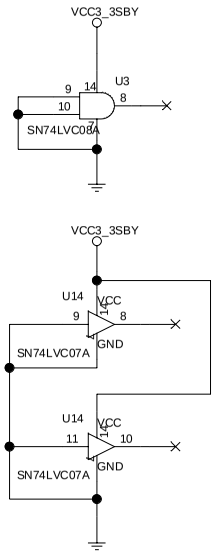
Un-used Gates

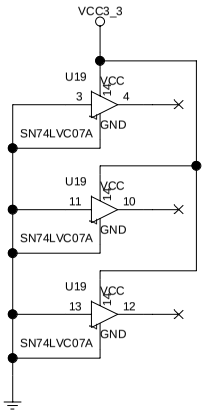


Place VDDQ capacitors within 70 mils of outer balls of MCH.



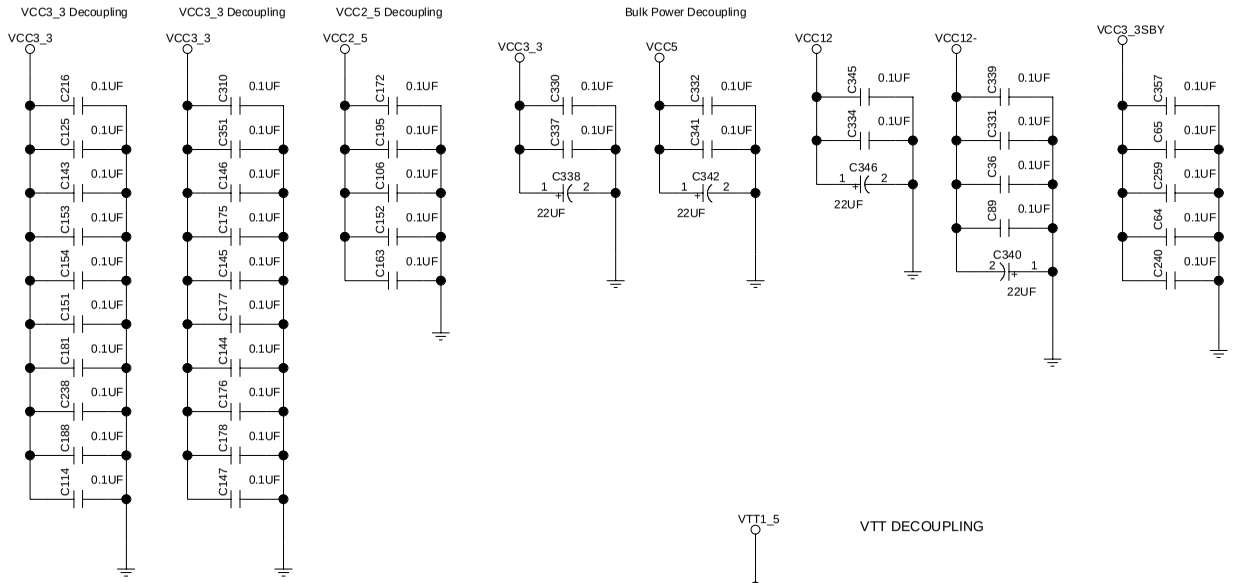


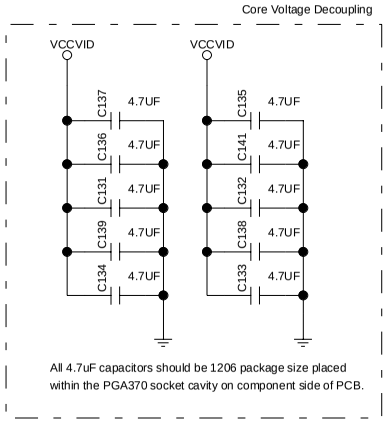


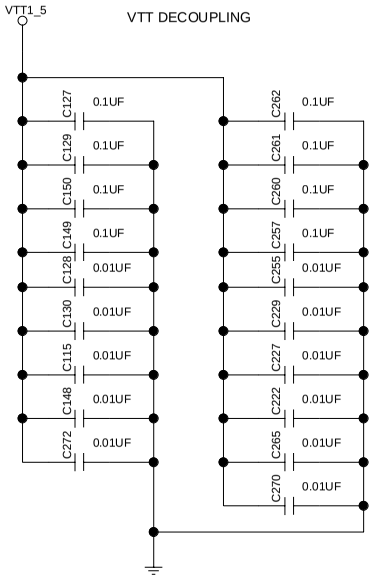


TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD DECOUPLING		REV: 1.0
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-23-1999 11:14	SHEET: 35 OF 37

Decoupling







TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD BULK DECOUPLING		REV: 1.0
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-23-1999 11:14	SHEET: 36 OF 37

Revision History

REVISION 1.0

Pgs 3, 4 Modified 82820 2-RIMM Rev C schematics by replacing SC242 with 370 FC-PGA socket.
Changed to low voltage ITP connector.

Pg 34 Added 62 ohm pullup resistor packs for AGTL+ termination.

TITLE: INTEL(R) 820 CHIPSET - FCPGA REFERENCE BOARD REVISION HISTORY			REV: 1.0
intel® PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630		DRAWN BY:	PROJECT:
		LAST REVISED: 11-10-1999 8:55	SHEET: 37 OF 37