Intel® 815 Chipset Platform

Design Guide

June 2000

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Revision History

Rev.	Description	Date
1.0	Initial Release	June 2000

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1. Introduction

This design guide organizes Intel's design recommendations for Intel® 815 chipset systems. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document also addresses system such design issues as thermal requirements for Intel® 815 chipset systems.

Design recommendations, board schematics, debug recommendations, and a system checklist are covered. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues.

The Intel schematics in this document can be used as references for board designers. While the included schematics cover specific designs, the core schematics remain the same for most Intel® 815 chipset platforms. The debug recommendations should be consulted when debugging an Intel® 815 chipset system. However, these debug recommendations should be understood before completing board design, to ensure the correct implementation of the debug port, in addition to other debug features.

1.1. Reference Documents

- *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) Datasheet* (document number: 290688) (http://developer.intel.com/design/chipsets/designex/298233.htm)
- *Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet* (document number: 290658)
- *Intel® 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub Datasheet* (document number: 290655)
- *Pentium® II Processor AGTL+ Guidelines* (document number: 243330)
- *Pentium® II Processor Power Distribution Guidelines* (document number: 243332)
- *Pentium® II Processor Developer's Manual* (document number: 243341)
- *Pentium® III Processor Specification Update* (latest revision from website)
- *AP 907 Pentium® III Processor Power Distribution Guidelines* (document number: 245085)
- *AP-585 Pentium® II Processor AGTL+ Guidelines* (document number: 243330)
- *AP-587 Pentium® II Processor Power Distribution Guidelines* (document number: 243332)
- *CK97 Clock Synthesizer Design Guidelines* (document number: 243867)
- *PCI Local Bus Specification*, Revision 2.2
- *Universal Serial Bus Specification*, Revision 1.0
- *VRM 8.4 DC-DC Converter Design Guidelines* (when available)

1.2. System Overview

The Intel® 815 chipset contains a Graphics Memory Controller Hub (GMCH) component for desktop platforms. It provides the processor interface, DRAM interface, hub interface, and an AGP interface or internal graphics. It is optimized for the Intel® Pentium®III and Intel® Celeron™ processors and the ICH. This product provides flexibility and scalability in graphics and memory subsystem performance. Competitive internal graphics can be scaled via an AGP card interface, and PC100 SDRAM system memory can be scaled to PC133 system memory.

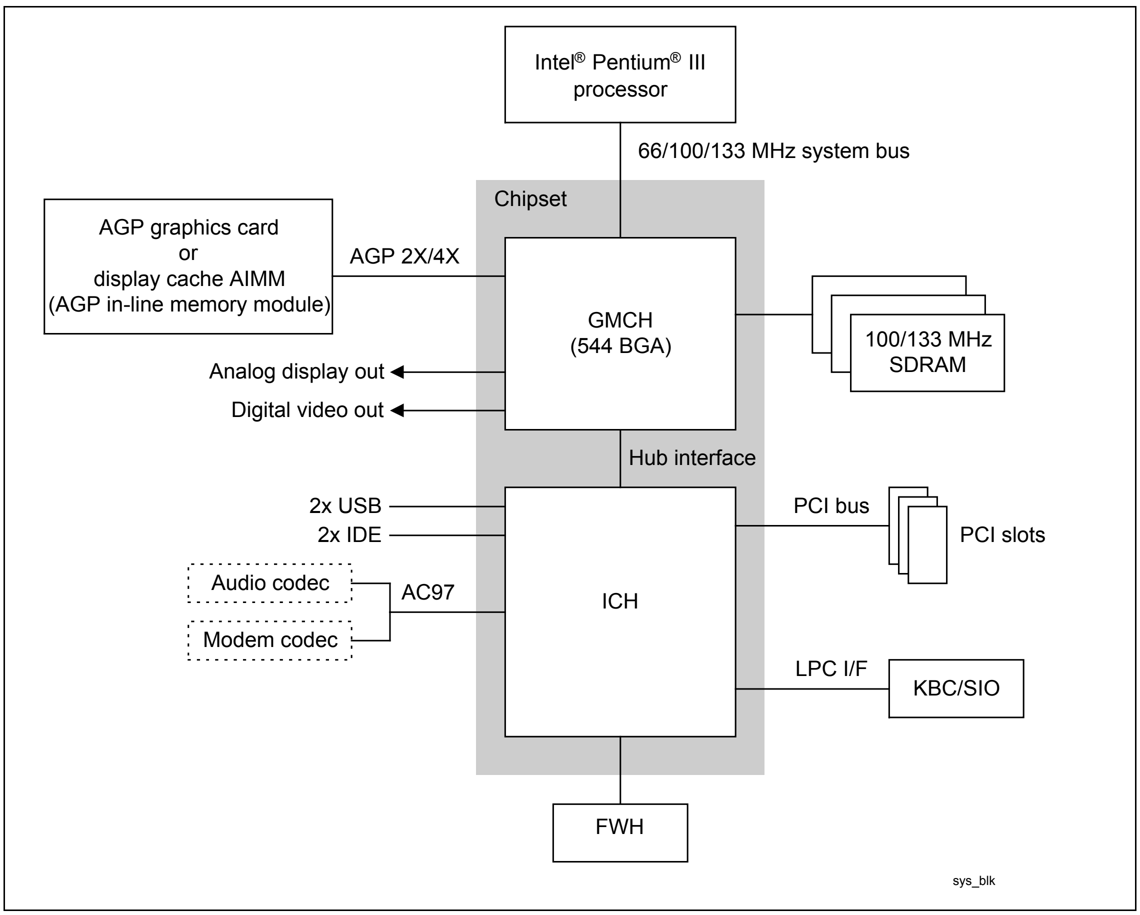
The Accelerated Hub Architecture interface (the chipset component interconnect) is designed into the chipset to provide an efficient, high-bandwidth communication channel between the 82815 GMCH and the I/O hub controller. The chipset architecture also enables a security and manageability infrastructure through the Firmware Hub component.

An ACPI-compliant Intel® 815 chipset platform can support the *Full-on (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4),* and *Soft-off (S5)* power management states. Through the use of an appropriate LAN device, the chipset also supports *Wake-on-LAN** for remote administration and troubleshooting. The chipset architecture removes the requirement of the ISA expansion bus that traditionally was integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software-configurable* AC'97 audio and modem coder/decoders (codecs), instead of the traditional ISA devices.

1.2.1. System Features

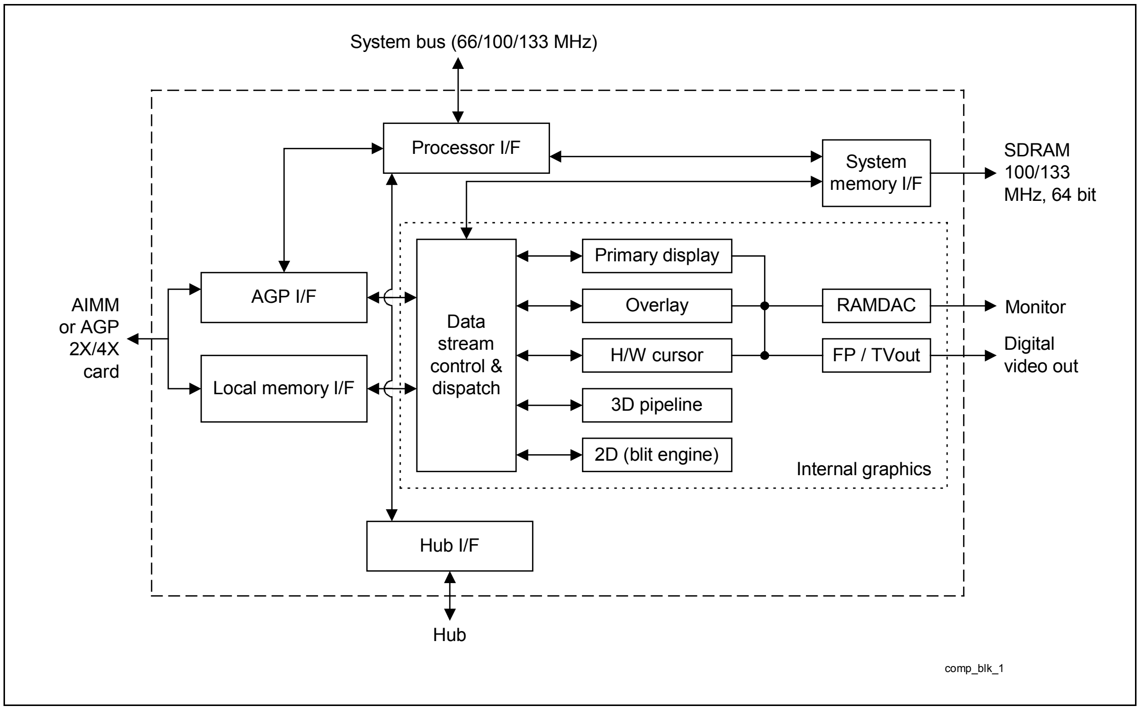
The Intel® 815 chipset contains two *core* components: the 82815 Graphics and Memory Controller Hub (GMCH) and the 82801AA I/O Controller Hub (ICH). The GMCH integrates a 66/100/133-MHz, P6 family system bus controller, integrated 2D/3D graphics accelerator or AGP(2X/4X) discrete graphics card, 100/133-MHz SDRAM controller, and a high-speed accelerated hub architecture interface for communication with the ICH. The ICH integrates an Ultra ATA/66 (ICH) controller, USB host controller, LPC interface controller, FWH interface controller, PCI interface controller, AC'97 digital controller, and a hub interface for communication with the GMCH.

Figure 1. System Block Diagram



1.2.2. Component Features

Figure 2. Component Block Diagram



1.2.2.1. 82815 GMCH

1.2.2.1.1. Processor/System Bus Support

- Optimized for the Intel® Pentium® III processor at 133-MHz system bus frequency
- Support for Intel® Celeron™ processors (FC-PGA) 533A and >566 MHz (66-MHz system bus) and Intel Pentium III processors (FC-PGA) (100-MHz / 133-MHz system bus)
- Supports 32-bit AGTL+ bus addressing. (No support for 36-bit address extension.)
- Supports uniprocessor systems.
- AGTL+ bus driver technology (gated AGTL+ receivers for reduced power)

1.2.2.1.2. Integrated DRAM Controller

- 32 MB to 256 MB using 64-Mb technology; 512 MB using 128-Mb technology
- Supports up to 3 double-sided DIMMS (6 rows).
- 100-MHz, 133-MHz SDRAM interface
- 64-bit data interface
- Standard SDRAM (synchronous) DRAM support (x-1-1-1 access)
- Supports only 3.3-V DIMM DRAM configurations.
- No registered DIMM support
- Support for symmetrical and asymmetrical DRAM addressing
- Support for ×8, ×16 DRAM device widths
- Refresh mechanism: CAS-before-RAS only
- Support for DIMM serial PD (presence detect) scheme via SMBus interface
- STR power management support via self-refresh mode using CKE

1.2.2.1.3. Accelerated Graphics Port (AGP) Interface

- Supports a single AGP (2X/4X) device (either via a connector or on the motherboard).
- Synchronously coupled to the host with 1:1 (66-MHz), 2:3 (100-MHz) and 1:2 (133-MHz) clock ratio

AGP Support

- Supports AGP 2.0, including 4X AGP data transfers, but not the 2X/4X Fast Write protocol.
- AGP universal connector support via dual-mode buffers to allow AGP 2.0 3.3-V or 1.5-V signaling
- 32-deep AGP request queue
- AGP address translation mechanism with integrated fully associative 20-entry TLB
- High-priority access support
- Delayed transaction support for AGP reads that can not be serviced immediately
- AGP semantic traffic to the DRAM is not snooped on the system bus and therefore is not coherent with the processor caches.

1.2.2.1.4. Integrated Graphics Controller

- Full 2D/3D/DirectX acceleration
- Texture-mapped 3D with point-sampled, bilinear, trilinear, and anisotropic filtering
- Hardware setup with support for strips and fans
- Hardware motion compensation assist for software MPEG/DVD decode
- Digital Video Out interface adds support for digital displays and TV-Out.
- PC9X compliant
- Integrated 230-MHz DAC

1.2.2.1.5. Integrated Local Graphics Memory Controller (Display Cache)

- 0 MB to 4 MB (via AIMM) using zero, one or two parts
- 32-bit data interface
- 133-MHz memory clock
- Supports ONLY 3.3-V SDRAMs

1.2.2.1.6. Packaging/Power

- 544 BGA with local memory port
- 1.85-V (±3% within margins of 1.795 V to 1.9 V) core and mixed 3.3-V, 1.5-V and AGTL+ I/O

1.2.2.2. I/O Controller Hub (ICH)

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system, as follows:

- Upstream accelerated hub architecture interface for access to the GMCH
- PCI 2.2 interface (6 PCI Req/Grant pairs)
- Bus master IDE controller; supports Ultra ATA/66
- USB controller
- I/O APIC
- SMBus controller
- FWH interface
- LPC interface
- AC'97 2.1 interface
- Integrated system management controller
- Alert on LAN*
- IRQ controller

1.2.2.2.1. Packaging/Power

- 241 mBGA
- 3.3-V core and 1.8-V and 3.3-V standby

1.2.2.3. Firmware Hub (FWH)

The hardware features of this device include:

- Integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 GPIs

1.2.2.3.1. Packaging/Power

- 40L TSOP and 32L PLCC
- 3.3-V core and 3.3 V / 12 V for fast programming

1.2.3. Platform Initiatives

1.2.3.1. Intel® PC 133

The Intel PC 133 initiative provides the memory bandwidth necessary to obtain high performance from the Intel Pentium III processor and AGP graphics controllers. The Intel 815 chipset SDRAM interface supports 100-MHz and 133-MHz operation. The latter delivers 1.066 GB/s of theoretical memory bandwidth, compared with the 800-MB/s theoretical memory bandwidth of 100-MHz SDRAM systems.

1.2.3.2. Accelerated Hub Architecture Interface

As the I/O speed has increased, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC'97 and Ultra ATA/66, coupled with the existing USB, I/O requirements could affect PCI bus performance. The Intel 815 chipset's *accelerated hub architecture* ensures that the I/O subsystem, both PCI and integrated I/O features (e.g., IDE, AC'97, USB), receives adequate bandwidth. By placing the I/O bridge on the accelerated hub architecture interface, instead of PCI, I/O functions integrated into the ICH and the PCI peripherals are ensured the bandwidth necessary for peak performance.

1.2.3.3. Internet Streaming SIMD Extensions

The Intel Pentium III processor provides 70 new SIMD (single-instruction, multiple-data) instructions. The new extensions are floating-point SIMD extensions. Intel MMX™ technology provides integer SIMD instructions. The Internet Streaming SIMD extensions complement the Intel MMX technology SIMD instructions and provide a performance boost to floating-point-intensive 3D applications.

1.2.3.4. AGP 2.0

The AGP 2.0 interface allows graphics controllers to access main memory at more than 1GB/s, which is twice the bandwidth of previous AGP platforms. AGP 2.0 provides the infrastructure necessary for *photorealistic 3D.* In conjunction with the Internet Streaming SIMD Extensions, AGP 2.0 delivers the next level of 3D graphics performance.

1.2.3.5. Manageability

The Intel 815 chipset platform integrates several functions designed to manage the system and lower the system's total cost of ownership (TCO). These system management functions are designed to report errors, diagnose the system, and recover from system lockups, without the aid of an external microcontroller.

TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

Processor Present Indicator

The ICH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH will reboot the system.

Function Disable

The ICH provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB, and SMBus. Once disabled, these functions no longer decode I/O, memory or PCI configuration space. Also, no interrupts or power management events are generated by the disabled functions.

Intruder Detect

The ICH provides an input signal, INTRUDER#, that can be attached to a switch that is activated when the system case is opened. The ICH can be programmed to generate an SMI# or TCO event as the result of an active INTRUDER# signal.

Alert on LAN*

The ICH supports Alert on LAN. In response to a TCO event (intruder detect, thermal event, processor boot failure), the ICH sends a hard-coded message over the SMBus. A LAN controller supporting the Alert on LAN protocol can decode this SMBus message and send a message over the network to alert the network manager.

1.2.3.6. AC’97

The *Audio Codec ’97* (AC’97) specification defines a digital link that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC) or both an AC and an MC. The AC’97 specification defines the interface between the system logic and the audio or modem codec, known as the *AC’97 Digital Link*.

As the platform migrates away from ISA, the ability to add cost-effective audio and modem solutions is important. The AC’97 audio and modem components are software configurable, which reduces configuration errors. The chipset’s AC’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC’97 digital link. Using the Intel 815 chipset’s integrated AC’97 digital link reduces the cost and facilitates the migration from ISA.

The ICH is an AC’97-compliant controller that supports up to two codecs, with independent PCI functions for audio and modem. The ICH communicates with the codec(s) via a digital serial link called the AC-link. All digital audio/modem streams and command/status information are communicated over the AC-link. Microphone input and left and right audio channels are supported for a high-quality, two-speaker audio solution. Wake-on-ring-from-suspend also is supported with an appropriate modem codec.

By using an audio codec, the AC’97 digital link allows for cost-effective, high-quality, integrated audio on the platform. In addition, an AC’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC’97. The chipset’s integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec or a modem with a modem codec. For systems requiring both audio and a modem, there are two solutions: The audio codec and the modem codec can be integrated into an AMC, or separate audio and modem codecs can be connected to the ICH.

The modem implementation for different countries should be considered, because telephone systems vary. When a split design is used, the audio codec can be on board, and the modem codec can be placed on a riser. Intel is developing a second-generation AC’97 digital link connector called the Communications and Networking Riser (CNR). With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel, where the external ports can be located.

1.2.3.7. Low-Pin-Count (LPC) Interface

In the Intel 815 chipset platform, the Super I/O (SIO) component has migrated to the Low-Pin-Count (LPC) interface. Migration to the LPC interface allows for lower-cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended, because the AC’97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of the devices offered and the features supported.

In addition, depending on system requirements, specific system I/O requirements may be integrated into the LPC Super I/O. For example, a USB hub can be integrated to connect to the ICH USB output and extend it to multiple USB connectors. Other SIO integration targets include a device bay controller or ISA-IRQ - to - serial-IRQ converter that supports a PCI-to-ISA bridge. Contact your Super I/O vendor to ensure the availability of the desired LPC Super I/O features.

1.2.3.8. Security – The Intel® Random Number Generator

The Intel 815 chipset based system contains the first of Intel's platform security features, the Intel® Random Number Generator (RNG). The RNG is a component of the Intel® 82802 Firmware Hub (FWH), and it supplies applications and security middleware products with true nondeterministic random numbers, through the Intel® Security Driver.

Better random numbers lead to better security. Most cryptographic functions, especially functions that provide authentication or encryption services, require random numbers for purposes such as key generation. One attack on those cryptographic functions is to predict the random numbers being used to generate those keys. Current methods that use system and user input to seed a pseudorandom number generator have proved vulnerable to those attacks. The RNG uses thermal noise across a resistor to generate true nondeterministic, unpredictable random numbers.

Applications often access cryptographic functions through security middleware products such as Microsoft's CAPI*, RSA's BSAFE* and the OpenGroup's CDSA*. Intel is working to ensure that middleware products and applications are enabled to take advantage of this capability. By implementing the BIOS requirements and testing and loading the Intel Security Driver, you can ensure that the Intel RNG is enabled on your platform design.

The ICH BIOS specification contains complete details of the BIOS requirements for enabling the RNG. In summary, the system BIOS must contain a System Device Node for the FWH device for plug-and-play operating systems to use the Random Number Generator through the Security Driver. The devnode is required for the operating system to find the FWH at enumeration time, and the specific devnode number associates the FWH with the Security Driver.

- The BIOS must report a single device node for the FWH.
- Intel˘specific EISA ID (devnode number must be INT0800)
- Device type: System peripherals/other
- Device attrib: Nonconfigurable and cannot be disabled
- ANSI ID string: "Intel FWH"
- Memory range descriptor: Describing feature space
- For PnP operating systems, BIOS ranges are allocated through E820h and ACPI structures, as in current BIOSes.
- For non-PnP operating systems, FWH ranges should be reserved through the Int 15h E820h function.

A complete Intel 815 chipset system must have the Security Driver loaded, for applications to take advantage of the Random Number Generator. The Security Driver implements an interface that middleware and some applications call to access the RNG. The Security Driver can be obtained from the PCG chipset driver download website at http://developer.intel.com/design/chipsets/drivers/SWDev/.

2. General Design Considerations

This chapter documents motherboard layout and routing guidelines for Intel® 815 chipset systems. This chapter does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations be completed for each design. Even when the guidelines are followed, it is recommended that critical signals be simulated to ensure proper signal integrity and flight time. Any deviation from these guidelines should be simulated.

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the "nominal" trace impedance for a 5-mil-wide trace. That is, it is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace, based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce the settling time.

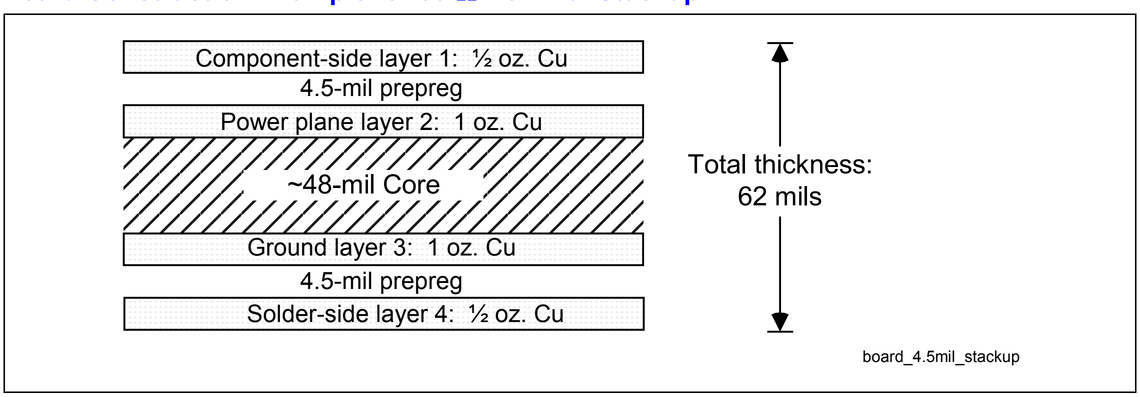
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using a PCB *stack-up* similar to that illustrated in the following figure.

2.1. Nominal Board Stackup

The Intel 815 chipset platform requires a board stack-up yielding a target impedance of 60 Ω ± 15%, with a 5-mil nominal trace width. The following figure shows an example stack-up that achieves this. It is a 4-layer printed circuit board (PCB) construction using 53%-resin, FR4 material.

Figure 3. Board Construction Example for 60-Ω Nominal Stackup



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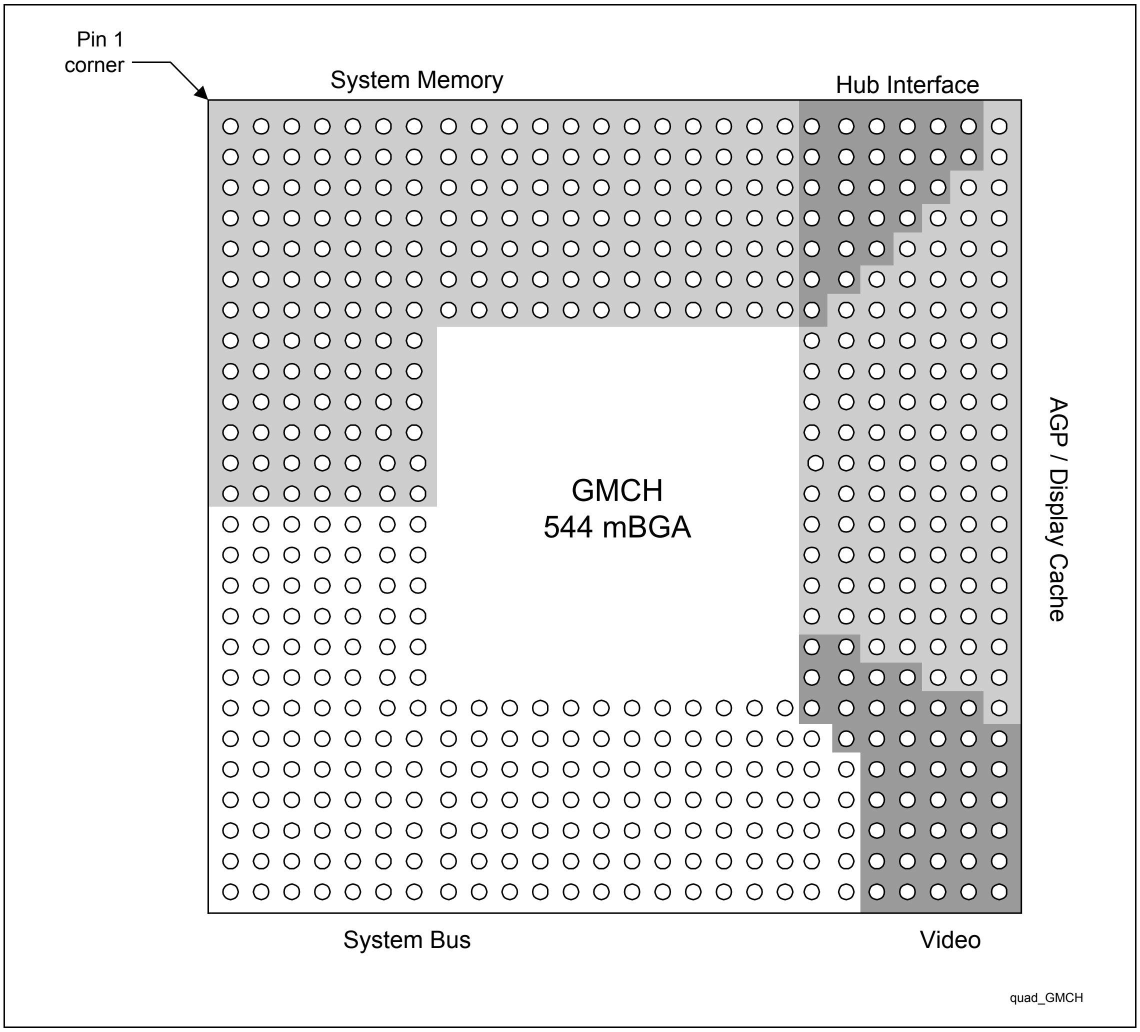
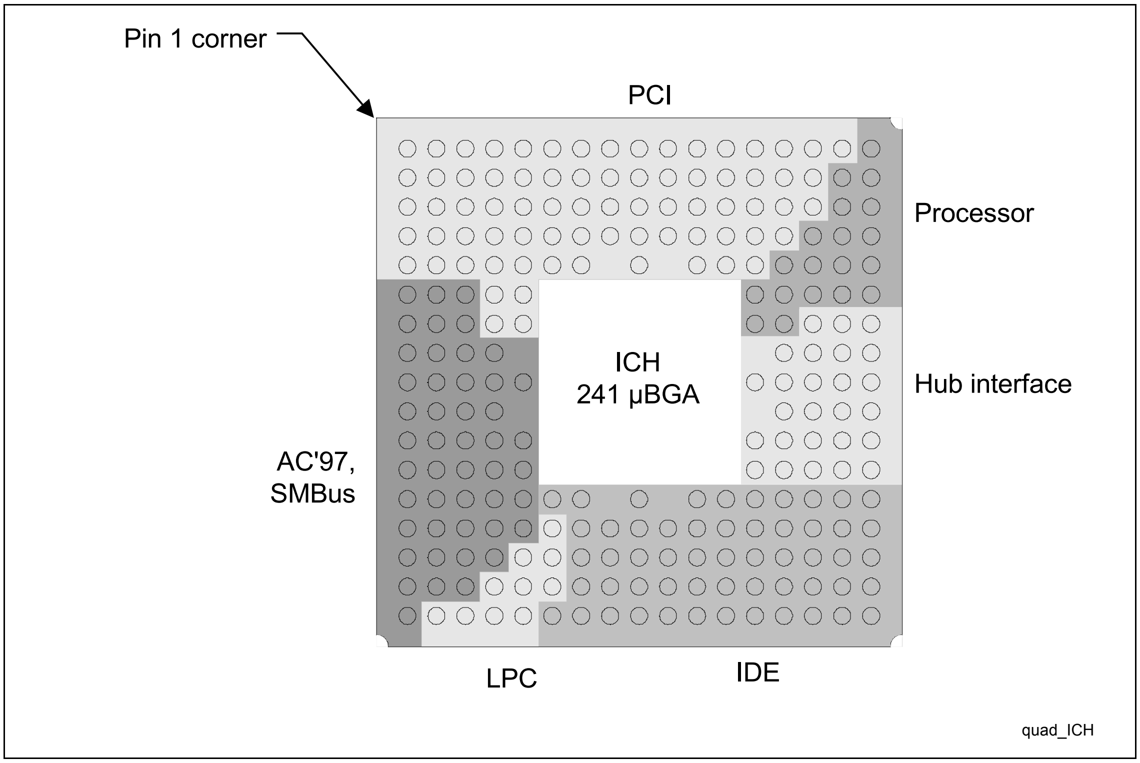
3. Component Quadrant Layouts

Figure 4. Intel® 815 Chipset GMCH 544 mBGA Quadrant Layout (Top View)



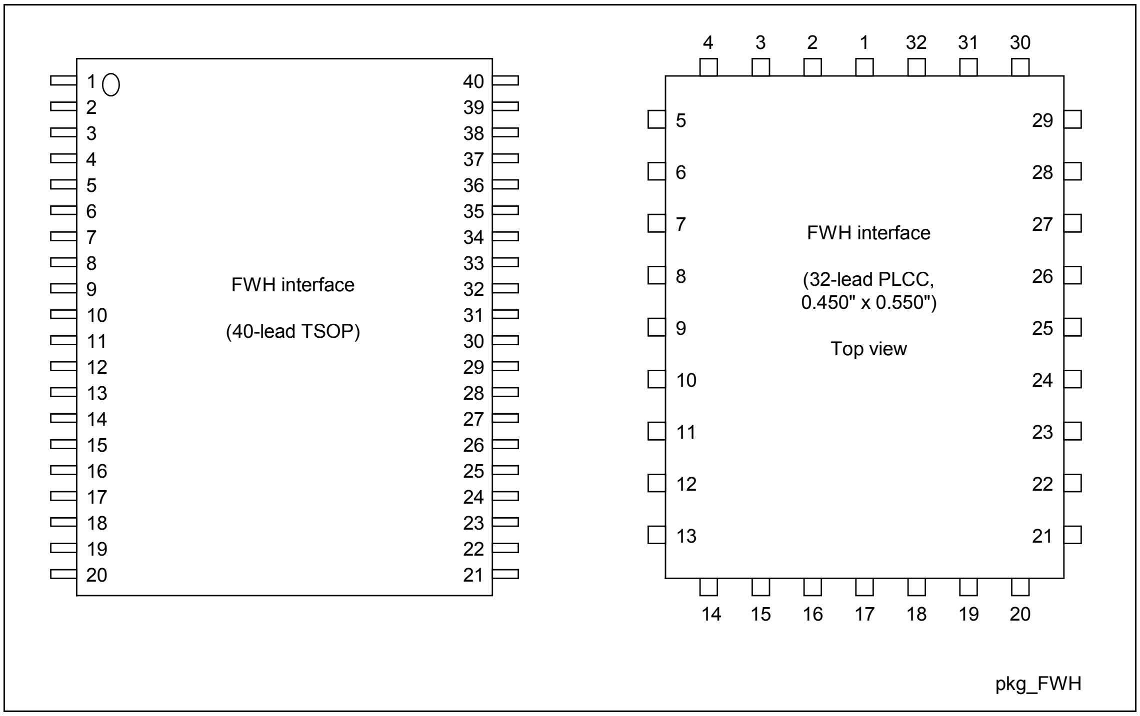
This diagram illustrates the relative signal quadrant locations on the Intel 815 chipset GMCH ballout. It does not represent the actual ballout. Refer to the *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) Datasheet* for the actual ballout.

Figure 5. ICH 241 mBGA Quadrant Layout (Top View)



This diagram illustrates the relative signal quadrant locations on the ICH ballout. It does not represent the actual ballout. Refer to the *Intel® 82801AA (ICH1) and 82801AB (ICH0) I/O Controller Hub Datasheet* for the actual ballout.

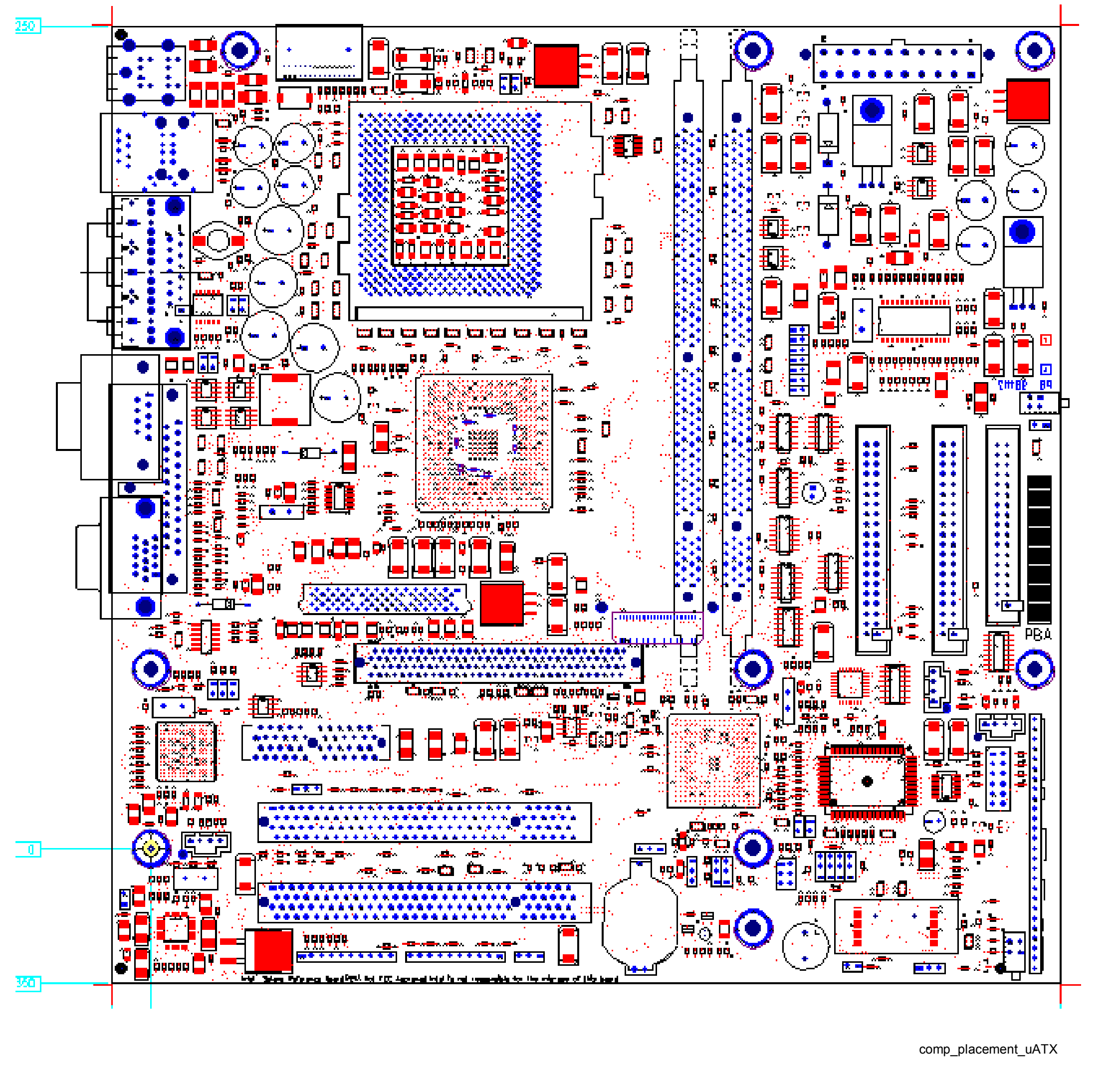
Figure 6. Firmware Hub (FWH) Packages



3.1. Intel® 815 Chipset Component Placement

The component placement shown in the following figure assumes a 4-layer, Micro-ATX motherboard with top-side-only component population (single-sided assembly).

Figure 7. Micro-ATX Placement Example



4. System Bus Design Guidelines

The next generation of the Intel® Pentium® III processor delivers higher performance by integrating the level 2 cache into the processor and running it at the core speed. In addition, the Intel® Pentium® III processor will run at a higher core and system bus speed than previous-generation IA-32 processors. The Intel® Pentium® III processor maintains hardware and software compatibility with the current Intel® Pentium® III processors. A new package technology enables the Intel® Pentium® III processor in a PGA370 socket. This is referred to as the Intel® Pentium® III Flip Chip-Pin Grid Array (FC-PGA) processor.

This section explains the design considerations for flexible platforms capable of using the Intel® 815 chipset with the full range of Intel® Celeron™ processor > 566 MHz and Intel® Pentium® III processors that use the PGA370 socket.

4.1.1. Terminology

In this document, the following terminology applies:

- *Flexible PGA370* refers to new-generation Intel® 815 chipsets that use a new, "flexible" PGA370 socket. In general, these designs support 66/100/133-MHz system bus operation, *VRM 8.4 DC-DC Converter Guidelines*, and Intel Celeron™ processor (PPGA) > 566 MHz and FC-PGA Intel® Pentium® III processors in single-microprocessor-based designs.
- The system bus speed supported by the design is based on the capabilities of the used processor, chipset, and clock driver.
- *All* references to Intel® Celeron™ processors are to the Intel® Celeron™ processor 533A and >566 MHz processors.

4.2. System Bus Routing Guidelines

The following layout guide supports designs using Intel® Pentium® III processors (FC-PGA) and Intel® Celeron™ processors, with the Intel® 815 chipset. The solution covers system bus speeds of 66 MHz for the Intel® Celeron™ processor and 100/133 MHz for FC-PGA Intel® Pentium® III processors. The solution proposed for this segment requires the motherboard design to terminate the system bus AGTL+ signals with 56-Ω±5% Rtt resistors. Intel® Pentium® III processors must also be configured to 110-Ω internal Rtt resistors.

4.2.1. Initial Timing Analysis

The following table lists the AGTL+ component timings of the processors and 82815 GMCH defined at the pins. **These timings are for reference only. Obtain each processor's specifications from its electrical, mechanical, and thermal specification.**

Table 1. FCPGA Processor and Intel® 815 Chipset GMCH AGTL+ Parameters *for Example* Calculations

IC Parameters	FC-PGA Processor at 133-MHz System Bus	Intel® 815 Chipset GMCH	Notes
Clock to Output maximum (T_{CO_MAX})	3.25 ns (for 66/100/133-MHz system bus speeds)	4.1	2
Clock to Output minimum (T_{CO_MIN})	0.40 ns (for 66/100/133-MHz system bus)	1.05	2
Setup time (T_{SU_MIN})	1.20 ns for BREQ lines 0.95 for all other AGTL+ Lines @ 133 MHz 1.20 ns for all other AGTL+ Lines @ 66/100 MHz	2.65	2,3
Hold time (T_{HOLD})	1.0 ns (For 66/100/133-MHz system bus speeds)	0.10	

NOTES:
1. All times in nanoseconds.
2. *Numbers in table are for reference only*. These timing parameters are subject to change. Check the appropriate component documentation for the valid timing parameter values.
3. T_{SU_MIN} = 2.65 ns assumes that the 82815 GMCH sees a minimum edge rate equal to 0.3 V/ns.

The following table lists example AGTL+ initial maximum flight times and Table 3 lists example minimum flight time calculations for a 133-MHz, uniprocessor system using the FC-PGA processor/ Intel 815 chipset system bus. Note that assumed values were used for clock skew and clock jitter. **Clock skew and clock jitter values depend on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.**

The data in the following two tables were derived assuming the following:

- CLK_{SKEW} = 0.20 ns
  (Note: Assumes that the clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together (i.e., "ganging") at the clock driver output pins, and that the PCB clock routing skew is 150 ps. The system timing budget must assume 0.175 ns of clock driver skew, if outputs are not tied together and a clock driver that conforms to the *CK815 Clock Synthesizer/Driver Specification* is used.)
- CLK_{JITTER} = 0.250 ns

See the respective processor's electrical, mechanical, and thermal specification, appropriate Intel 815 chipset documentation, and the *CK815 Clock Synthesizer/Driver Specification* for details on the clock skew and jitter specifications. Exact details regarding the host clock routing topology are provided with the platform design guideline.

Table 2. Example T_{FLT_MAX} Calculations for 133-MHz Bus

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}
Processor	GMCH	7.50	3.25	2.65	0.20	0.25	0.40	1.1
GMCH	Processor	7.50	4.1	1.20	0.20	0.25	0.40	1.35

NOTES:
1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.

Table 3. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	THOLD	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor	GMCH	0.10	0.20	0.40	0.10
GMCH	Processor	1.00	0.20	1.05	0.15

NOTES:
1. All times in nanoseconds.

The flight times in Table 2 include the margin, to account for the following phenomena that Intel observed when multiple bits switched simultaneously. These multi-bit effects can adversely affect the flight time and signal quality and sometimes are not accounted for in the simulation. Accordingly, the maximum flight times depend on the baseboard design, and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in
- Rising or falling edge rate degradation at the receiver, caused by inductance in the current return path, which requires extrapolation that causes additional delay
- Cross-talk on the PCB and inside the package can cause signal variation.

There are additional effects that **may not necessarily** be covered by the multi-bit adjustment factor and should be budgeted as appropriate for the baseboard design. Examples include:

- The effective board propagation constant (S_{EFF}), which is a function of:
  — Dielectric constant (ε_r) of the PCB material
  — Type of trace connecting the components (stripline or microstrip)
  — Length of trace and component load on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time, **but is not necessarily equal to** the flight time.

4.3. General Topology and Layout Guidelines

The following topology and layout guidelines are preliminary and subject to change. The guidelines are derived from empirical testing with the Intel® 810E chipset as well as correlative simulations with very preliminary Intel 815 chipset package models. Refer to the *Intel® Celeron™ Processor* Datasheet and the *Intel® Pentium® III Processor for the PGA370 Socket* Datasheet for detailed information on processor signal groups and pin definitions, as referenced later.

In the Single-Ended Termination(SET) topology for the 370-pin socket (PGA370), the termination should be placed close to the processor on the motherboard. No termination is present at the chipset end of the network. For this reason, SET will exhibit much more ringback than the dual-terminated topology. Extra care is required in SET simulations to ensure that the ringback specs are satisfied under the worst-case signal quality conditions. Intel® 815 chipset designs require all AGTL+ signals to be terminated with a 56-Ω termination on the motherboard. To satisfy the processor signal integrity requirements, **it is highly recommended that all system bus signal segments be referenced to the ground plane for the entire route**.

Figure 8. Topology for 370-Pin Socket Designs with Single-Ended Termination (SET)

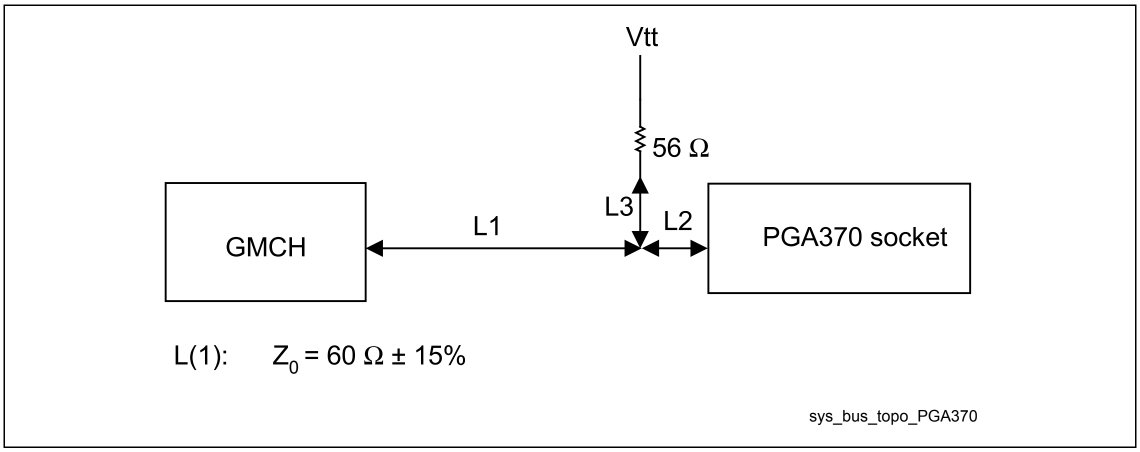


Table 4. Segment Descriptions and Lengths for the Previous Figure

Segment	Description	Min. Length (in.)	Max. Length (in.)
L1+L2	GMCH to Rtt Stub	1.90	4.50
L2	PGA370 Pin to Rtt stub	0.0	0.20
L3	Rtt Stub length	0.50	2.50

NOTES:
1. All AGTL+ bus signals should be referenced to the ground plane for the entire route.

- AGTL+ signals should be routed with trace lengths within the range specified for L1+L2 from the processor pin to the chipset.
- Use an intragroup AGTL+ spacing to line width to dielectric thickness ratio of at least 2:1:1 for microstrip geometry. If ε_r = 4.5, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10-mil spacing, 5-mil traces, and a 5-mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
- The recommended trace width is 5 mils, but not wider than 6 mils.

The following table contains the trace width:space ratios assumed for this topology. Three cross-talk cases are considered in this guideline: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intragroup AGTL+ cross-talk involves interference between AGTL+ signals within the same group. Intergroup AGTL+ cross-talk involves interference by AGTL+ signals in a particular group with AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ cross-talk is the mutual interference of CMOS and AGTL+ signals.

Table 5. Trace Width : Space Guidelines

Cross-talk Type	Trace Width : Space Ratios
Intragroup AGTL+ signals (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ signals (different group AGTL+)	5:15 or 6:18
AGTL+ to System Memory signals	5:30 or 6:36
AGTL+ to any other signal	5:20 or 6:24

NOTES:
1. Edge to edge spacing
2. Units are in mils.

4.3.1.1. Motherboard Layout Rules for AGTL+ Signals to Improve Signal Integrity

Ground Reference

It is strongly recommended that AGTL+ signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide an effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane.

Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance.

Processor Connector Breakout

It is strongly recommended that AGTL+ signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the connector on the same layer. If routing is tight, break out from the connector on the opposite routing layer over a ground reference and cross over to the main signal layer near the processor connector.

Note: For AGTL+ signal integrity, it is imperative to comply with these layout rules, particularly for the 0.18-micron process technology.

Minimizing Cross-talk

The following general rules will minimize the effect of cross-talk in the high-speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges, wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces must be close and parallel to each other, minimize the distance between them, and maximize the distance between the sections when the spacing restrictions are relaxed.
- Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL+ is a low-signal-swing technology, it is important to isolate AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 5-V PCI.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the cross-talk.
- Route AGTL+ address, data and control signals in separate groups to minimize cross-talk between groups. Keep at least 25 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the cross-talk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross-sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the trade-off for this smaller cross-sectional area is a higher trace resistivity that can reduce the falling-edge noise margin because of the I*R loss along the trace.

Spacing to System Memory Signals

- AGTL+ signals must be well isolated from the system memory signals to minimize the impact of cross-talk.
- AGTL+ signal trace edges must be at least 30 mils from any system memory trace edge within 100 mils of the ball of the 82815 GMCH. This spacing requirement supercedes any spacing requirement for AGTL+ to other signals documented elsewhere in the design guide.

4.3.1.2. Motherboard Layout Rules for Non-AGTL+ (CMOS) Signals

Table 6. Routing Guidelines for Non-AGTL+ Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1" to 9"
FERR#	5 mils	10 mils	1" to 9"
FLUSH#	5 mils	10 mils	1" to 9"
IERR#	5 mils	10 mils	1" to 9"
IGNNE#	5 mils	10 mils	1" to 9"
INIT#	5 mils	10 mils	1" to 9"
LINT[0] (INTR)	5 mils	10 mils	1" to 9"
LINT[1] (NMI)	5 mils	10 mils	1" to 9"
PICD[1:0]	5 mils	10 mils	1" to 9"
PREQ#	5 mils	10 mils	1" to 9"
PWRGOOD	5 mils	10 mils	1" to 9"
SLP#	5 mils	10 mils	1" to 9"
SMI#	5 mils	10 mils	1" to 9"
STPCLK	5 mils	10 mils	1" to 9"
THERMTRIP#	5 mils	10 mils	1" to 9"

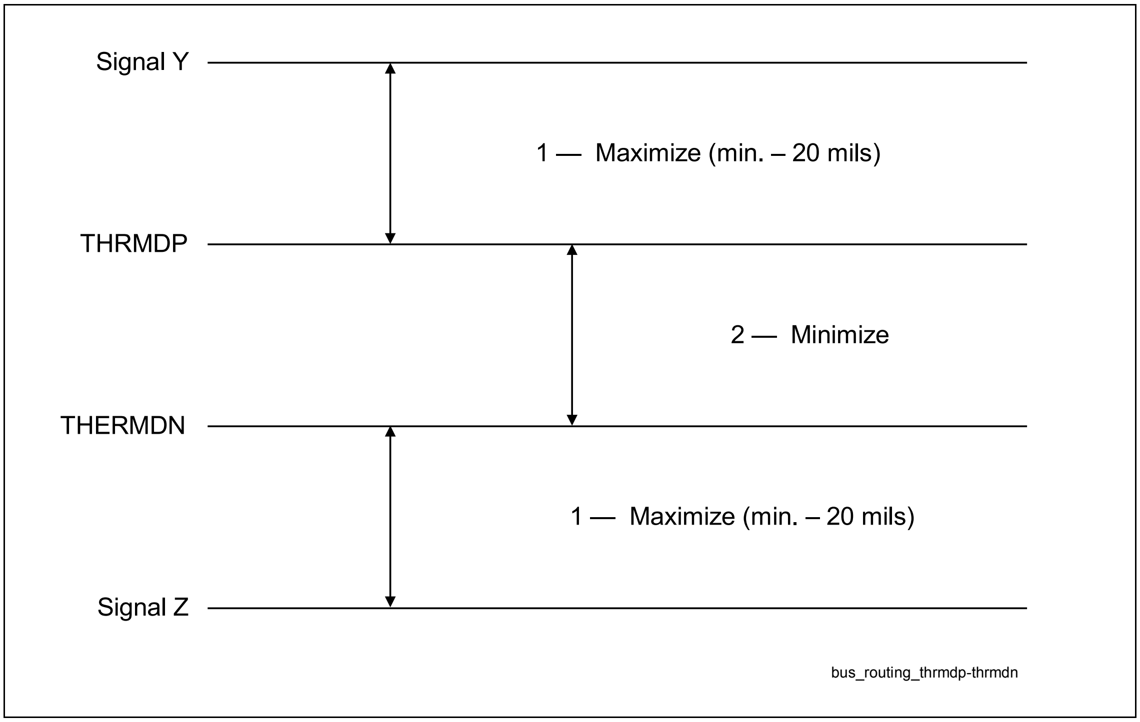
NOTES:

1. Route these signals on any layer or combination of layers.

4.3.1.3. THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor's thermal diode connections. The thermal diode operates at very low currents and may be susceptible to cross-talk. The traces should be routed close together to reduce loop area and inductance.

Figure 9. Routing for THRMDP and THRMDN



NOTES:
1. Route these traces parallel and equalize lengths within ±0.5”.
2. Route THRMDP and THRMDN on the same layer.

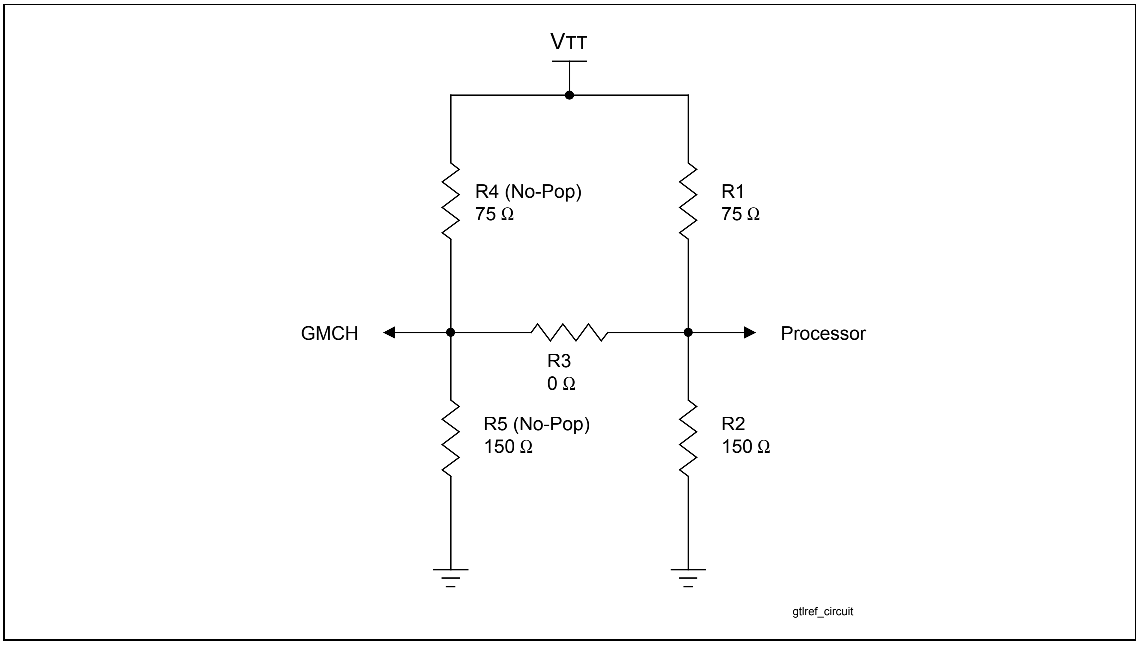
4.3.1.4. Additional Routing and Placement Considerations

- Distribute Vtt with a wide trace. A 0.050” minimum trace is recommended to minimize DC losses. Route the Vtt trace to all components on the host bus. Be sure to include decoupling capacitors.
- The Vtt voltage should be 1.5 V ± 3% for static conditions and 1.5 V ± 9% for the worst-case transient condition.
- Place resistor divider pairs for VREF generation at the GMCH component. VREF also is delivered to the processor.

4.3.2. GTLREF Topology and Layout for Debug

It is strongly recommended that resistor sites be added to the layout to split the GTLREF sources to the processor and the chipset. This allows the designer to independently modify the reference voltage to each component for debug purposes. The recommended GTLREF circuit topology is shown in the following figure.

Figure 10. GTLREF Circuit Topology



- Normal shared GTLREF (one source, routed to both the GMCH and processor)
  - Populate R1, R2, and R3 with values shown
  - Do NOT Populate R4 and R5
- Independent GTLREF for Platform Debug (independent sources for each the GMCH and processor)
  - Populate R1, R2, R4, and R5 with values shown
  - Do NOT Populate R3

GTLREF Layout and Routing Guidelines

- Place all resistor sites for GTLREF generation close to the GMCH.
- Route GTLREF with as wide a trace as possible.
- Use 1-0.1 uF decoupling capacitor for every 2 GTLREF pins at the processor (4 capacitors total). Place as close as possible (within 500mils) to the Socket 370 GTLREF pins.
- Use 1-0.1 uF decoupling capacitor for each of the 2 GTLREF pins at the GMCH (2 capacitors total). Place as close as possible to the GMCH GTLREF balls.

4.4. Electrical Differences for Flexible PGA370 Designs

The change in design from the *legacy PGA370* to the *flexible PGA370* involves several electrical changes, as follows:

- Changes to the PGA370 socket pin definitions. The FC-PGA Intel® Pentium® III processor utilizes a superset of the Intel® Celeron™ processor (PPGA) pin definition.
- Addition of VTT (AGTL+ termination voltage) delivery to the PGA370 socket
- BSEL[1:0] implementation differences. BSEL1 has been added to select either a 100-MHz or 133-MHz system bus frequency setting from the clock synthesizer.
- Additional PLL reference voltage (1.25 V) on new CLKREF pin
- More stringent undershoot/overshoot requirements for CMOS and AGTL+ signals
- Addition of on-die Rtt (AGTL+ termination resistors) for the FC-PGA processor. The requirement for on-motherboard Rtt implementation remains when supporting the Intel Celeron™ processor (PPGA). When only FC-PGA processors are supported, the reset signal (RESET#) still requires termination to VTT on the motherboard.

4.5. PGA370 Socket Definition Details

The following tables compare *legacy PGA370* pin names and functions with new *flexible PGA370* pin names and functions. Designers must pay close attention to the notes section following this table, for compatibility concerns regarding these pin changes.

Table 7. Platform Pin Definition Comparison for Single-Microprocessor Designs

Pin #	Legacy PGA370 Pin Name	Flexible PGA370 Pin Name	Function	Type	Notes
A29	Reserved	DEP7#	Data bus ECC data	AGTL+, I/O	2
A31	Reserved	DEP3#	Data bus ECC data	AGTL+, I/O	2
A33	Reserved	DEP2#	Data bus ECC data	AGTL+, I/O	2
AA33	Reserved	VTT	AGTL+ termination voltage	Power/other	4
AA35	Reserved	VTT	AGTL+ termination voltage	Power/other	4
AC1	Reserved	A33#	Additional AGTL+ address	AGTL+, I/O	2
AC37	Reserved	RSP#	Response parity	AGTL+, I	2
AF4	Reserved	A35#	Additional AGTL+ address	AGTL+, I/O	2
AH20	Reserved	VTT	AGTL+ termination voltage	Power	
AH4	Reserved	RESET#	Processor reset (used by the FC-PGA Intel® Pentium® III processor)	AGTL+, I	3
AJ31	GND	BSEL1	System bus frequency select	CMOS, I/O	1
AK16	Reserved	VTT	AGTL+ termination voltage	Power	
AK24	Reserved	AERR#	Address parity error	AGTL+, I/O	2
AL11	Reserved	AP0#	Address parity	AGTL+, I/O	2

Pin #	Legacy PGA370 Pin Name	Flexible PGA370 Pin Name	Function	Type	Notes
AL13	Reserved	VTT	AGTL+ termination voltage	Power	
AL21	Reserved	VTT	AGTL+ termination voltage	Power	
AM2	GND	Reserved	Reserved	Reserved	1
AN11	Reserved	VTT	AGTL+ termination voltage	Power	
AN13	Reserved	AP1#	Address parity	AGTL+, I/O	2
AN15	Reserved	VTT	AGTL+ termination voltage	Power	
AN21	Reserved	VTT	AGTL+ termination voltage	Power/other	4
AN23	Reserved	RP#	Request parity	AGTL+, I/O	
B36	Reserved	BINIT#	Bus initialization	AGTL+, I/O	2
C29	Reserved	DEP5#	Data bus ECC data	AGTL+, I/O	2
C31	Reserved	DEP1#	Data bus ECC data	AGTL+, I/O	2
C33	Reserved	DEP0#	Data bus ECC data	AGTL+, I/O	2
E23	Reserved	VTT	AGTL+ termination voltage	Power/other	4
E29	Reserved	DEP6#	Data bus ECC data	AGTL+, I/O	2
E31	Reserved	DEP4#	Data bus ECC data	AGTL+, I/O	2
G35	Reserved	VTT	AGTL+ termination voltage	Power/other	
G37	Reserved	See Note 5			
S33	Reserved	VTT	AGTL+ termination voltage	Power/other	4
S37	Reserved	VTT	AGTL+ termination voltage	Power/other	4
U35	Reserved	VTT	AGTL+ termination voltage	Power/other	4
U37	Reserved	VTT	AGTL+ termination voltage	Power/other	4
V4	Reserved	BERR#	Bus error	AGTL+, I/O	2
W3	Reserved	A34#	Additional AGTL+ address	AGTL+, I/O	2
X4	RESET#	RESET2#	Processor reset (used by Intel® Celeron™ processor (PPGA))	AGTL+, I	3
X6	Reserved	A32#	Additional AGTL+ address	AGTL+, I/O	2
Y33	GND	CLKREF	1.25-V PLL reference	Power	1

NOTES:

1. These signals are defined as ground (Vss) in legacy designs utilizing the PGA370 socket. For new *flexible PGA370* designs, use the new signal definitions. These new signal definitions are backwards-compatible with the Intel® Celeron™ processor (PPGA).
2. While these signals are not used in Intel® 815 chipset designs, they are available for chipsets that support these functions. Only the FC-PGA Intel® Pentium® III processor offers these capabilities in the PGA370 platform.
3. The AGTL+ reset signal, RESET#, is delivered to pin X4 on *legacy PGA370* designs. On *flexible PGA370* designs, it is delivered to X4 **and** AH4 pins. See **Error! Reference source not found.** for more details.
4. RESET2# is not required for platforms that do not support the Intel Celeron™ processor . Pin X4 should then be connected to ground.
5. These pins must be connected to the 1.5-volt Vtt plane.
6. This pin must be connected to Vtt for platforms using the Intel Pentium III processor based on the cA2 stepping. Refer to the Intel Pentium III processor specification update for stepping details.

Table 8. Processor Pin Definition Comparison

Pin #	Intel® Celeron™ Processor (PPGA) Pin Name	Intel® Celeron™ Processor FC-PGA Pin Name	FC-PGA Intel Pentium® III Processor Pin Name	Function
A29	Reserved	Reserved	DEP7#	Data bus ECC data
A31	Reserved	Reserved	DEP3#	Data bus ECC data
A33	Reserved	Reserved	DEP2#	Data bus ECC data
AA33	Reserved	Reserved	VTT	AGTL+ termination voltage
AA35	Reserved	Reserved	VTT	AGTL+ termination voltage
AC1	Reserved	Reserved	A33#	Additional AGTL+ address
AC37	Reserved	Reserved	RSP#	Response parity
AF4	Reserved	Reserved	A35#	Additional AGTL+ address
AH20	Reserved	Reserved	VTT	AGTL+ termination voltage
AH4	Reserved	Reserved	RESET#	Processor reset (used by the FC-PGA Intel Pentium III processor)
AJ31	GND	BSEL1	BSEL1	System bus frequency select
AK16	Reserved	Reserved	VTT	AGTL+ termination voltage
AK24	Reserved	Reserved	AERR#	Address parity error
AL11	Reserved	Reserved	AP0#	Address parity
AL13	Reserved	Reserved	VTT	AGTL+ termination voltage
AL21	Reserved	Reserved	VTT	AGTL+ termination voltage
AM2	GND	Reserved	Reserved	Reserved
AN11	Reserved	Reserved	VTT	AGTL+ termination voltage
AN13	Reserved	Reserved	AP1#	Address parity
AN15	Reserved	Reserved	VTT	AGTL+ termination voltage
AN21	Reserved	Reserved	VTT	AGTL+ termination voltage
AN23	Reserved	Reserved	RP#	Request parity
B36	Reserved	Reserved	BINIT#	Bus initialization
C29	Reserved	Reserved	DEP5#	Data bus ECC data
C31	Reserved	Reserved	DEP1#	Data bus ECC data
C33	Reserved	Reserved	DEP0#	Data bus ECC data
E23	Reserved	Reserved	VTT	AGTL+ termination voltage
E29	Reserved	Reserved	DEP6#	Data bus ECC data
E31	Reserved	Reserved	DEP4#	Data bus ECC data
G35	Reserved	Reserved	VTT	AGTL+ termination voltage
S33	Reserved	Reserved	VTT	AGTL+ termination voltage

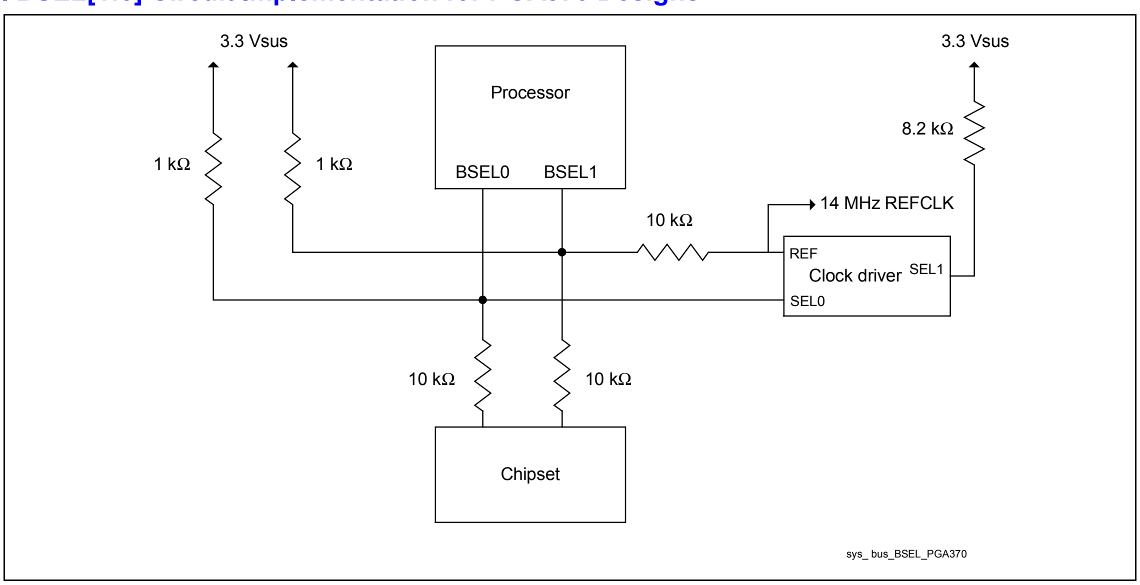
Pin #	Intel® Celeron™ Processor (PPGA) Pin Name	Intel® Celeron™ Processor FC-PGA Pin Name	FC-PGA Intel Pentium® III Processor Pin Name	Function
S37	Reserved	Reserved	VTT	AGTL+ termination voltage
U35	Reserved	Reserved	VTT	AGTL+ termination voltage
U37	Reserved	Reserved	VTT	AGTL+ termination voltage
V4	Reserved	Reserved	BERR#	Bus error
W3	Reserved	Reserved	A34#	Additional AGTL+ address
X4	RESET#	RESET#	RESET2#	Processor reset (used by Intel® Celeron™ processors)
X6	Reserved	Reserved	A32#	Additional AGTL+ address
Y33	GND	Reserved	CLKREF	1.25-V PLL reference

4.6. BSEL[1:0] Implementation Differences

The FC-PGA Intel Pentium III processor utilizes the BSEL1 pin to select either the 100-MHz or 133-MHz system bus frequency setting from the clock synthesizer. While the BSEL0 signal is still connected to the PGA370 socket, the FC-PGA Intel Pentium III processor does not utilize it. Only the Intel Celeron™ processor (PPGA) utilizes the BSEL0 signal. The FC-PGA Intel Pentium III processors are 3.3-V tolerant for these signals, as are the clock and chipset. However, the Intel Celeron™ processor (PPGA) utilizes 2.5-V logic levels on the BSEL signals. Therefore, *flexible PGA370* designs will utilize 2.5-V logic levels on the BSEL[1:0] signals to support widest range of processors.

CK815 has been designed to support selections of 66 MHz, 100 MHz, and 133 MHz. The REF input pin has been redefined to be a frequency selection strap (BSEL1) during power-on, after which it becomes a 14-MHz reference clock output. The following figure details the new BSEL[1:0] circuit design for *flexible PGA370* designs. Note that BSEL[1:0] are now pulled up using 1-kΩ resistors. Also refer to the following figure for more details.

Figure 11. BSEL[1:0] Circuit Implementation for PGA370 Designs



4.7. CLKREF Circuit Implementation

The CLKREF input utilized by the FC-PGA Intel Pentium III processor requires a 1.25-V source. It can be generated from a voltage divider on the Vcc2.5 or Vcc3.3 sources, utilizing 1% tolerance resistors. A 4.7-µF decoupling capacitor should be included on this input. See the following figure and table for example CLKREF circuits. **Do not use Vtt as the source for this reference!**

Figure 12. Examples for CLKREF Divider Circuit

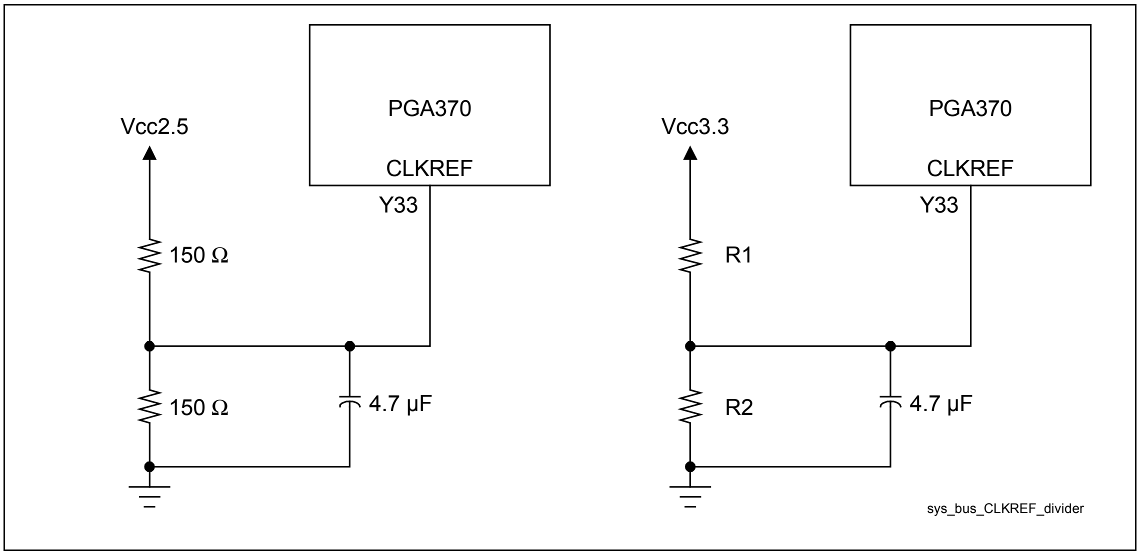


Table 9. Resistor Values for CLKREF Divider (3.3-V Source)

R1 (Ω)	R2 (Ω)	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

4.8. Undershoot/Overshoot Requirements

Undershoot and overshoot specifications become more critical as the process technology for microprocessors shrinks due to thinner gate oxide. Violating these undershoot and overshoot limits will degrade the life expectancy of the processor.

The FC-PGA Intel Pentium III processor has more restrictive overshoot and undershoot requirements for system bus signals than did previous processors. These requirements stipulate that a signal at the output of the driver buffer and at the input of the receiver buffer must not exceed the maximum absolute overshoot voltage limit (2.18 V) and the minimum absolute undershoot voltage limit (-0.58 V). Exceeding these limits will damage the FC-PGA processor. There also is a time-dependent, nonlinear overshoot and undershoot requirement that depends on the amplitude and duration of the overshoot/undershoot. See the appropriate FC-PGA Intel Pentium III processor's electrical, mechanical and thermal specification for more details on the FC-PGA Intel processor overshoot/undershoot specifications. A new undershoot/overshoot checking tool will be made available to assist in understanding whether simulation results or actual oscilloscope measurements satisfy signal integrity requirements in the datasheet.

4.9. Processor Reset Requirements

Flexible PGA370 designs must route the AGTL+ reset signal from the chipset to two pins on the processor as well as to the debug port connector. This reset signal is connected to pins AH4 (RESET#) and X4 (RESET2#) at the PGA370 socket. Finally**, the AGTL+ reset signal must always be terminated to VTT on the motherboard**.

Designs that do not support the debug port will not utilize the 240-Ω series resistor or the connection of RESET# to the debug port connector. RESET2# is not required for platforms that do not support the Intel Celeron™ processor. Pin X4 should then be connected to ground.

The routing rules for the AGTL+ reset signal are shown in the following figure.

Figure 13. RESET#/RESET2# Routing Guidelines

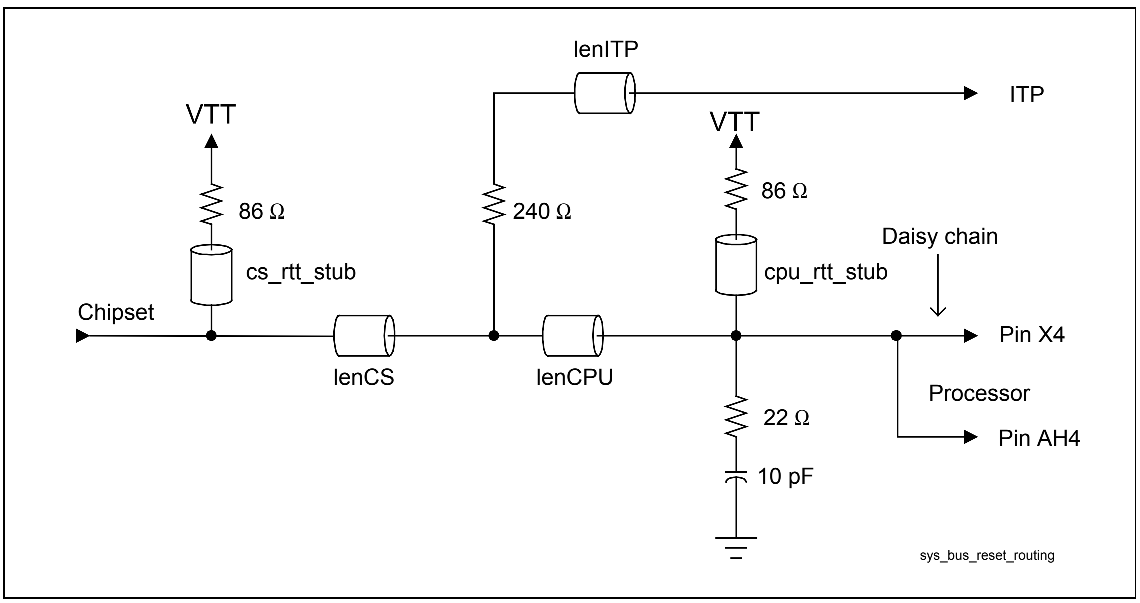


Table 10. RESET#/RESET2# Routing Guidelines (see Figure 13)

Parameter	Minimum (in)	Maximum (in)
lenCS	0.5	1.5
lenITP	1	3
lenCPU	0.5	1.5
cs_rtt_stub	0.5	1.5
cpu_rtt_stub	0.5	1.5

4.10. Determining the Intalled Processor via Hardware Mechanisms

The following figure provides the logic decoding to determine which processor is installed in a PGA370 design.

Table 11. Determining the Installed Processor via Hardware Mechanisms

VID	VCORE_DET	CPUPRES#	Notes
1001	0	0	FC-PGA Intel® Pentium® III processor installed.
1011	0	0	Intel® celeron™ FC-PGA processor installed.
0001	1	0	Intel® Celeron™ processor (PPGA) installed.
1111	X	1	No processor installed.

4.11. Processor PLL Filter Recommendations

Intel PGA370 processors have internal phase lock loop (PLL) clock generators, which are analog and require a quiet power supply to minimize jitter.

4.11.1. Topology

The general desired topology is shown in Figure 15. Not shown are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

4.11.2. Filter Specification

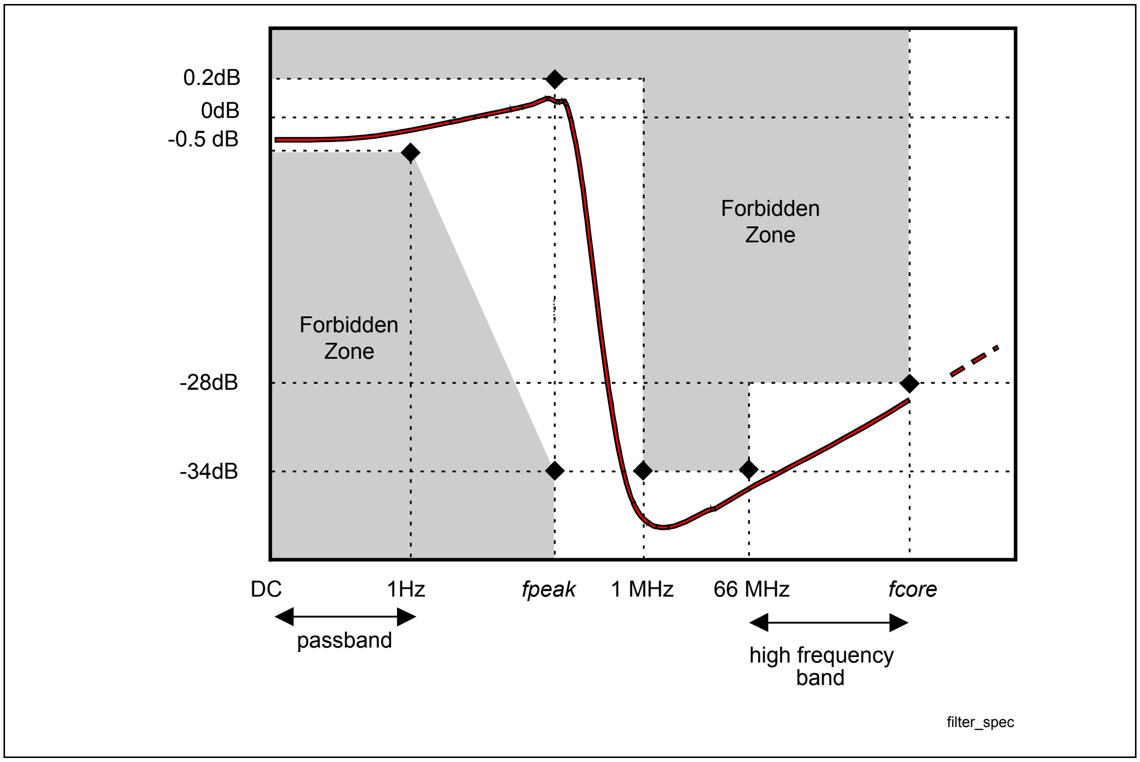
The filter's function is to protect the PLL from external noise through low-pass attenuation.

The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

- <0.2-dB gain in pass band
- <0.5-dB attenuation in pass band (see DC drop in next set of requirements)
- >34-dB attenuation from 1 MHz to 66 MHz
- >28-dB attenuation from 66 MHz to core frequency

The filter specification is graphed in the following figure.

Figure 14. Filter Specification



NOTES:

1. Diagram not to scale
2. No specification for frequencies beyond *fcore*
3. *fpeak* should be less than 0.05 MHz.

Other requirements:

- Use shielded-type inductor to minimize magnetic pickup.
- Filter should support DC current > 30 mA.
- DC voltage drop from VCC to PLL1 should be < 60 mV, which in practice implies series R < 2 Ω. It also means pass band (from DC to 1 Hz) attenuation < 0.5 dB for VCC = 1.1 V, and < 0.35dB for VCC = 1.5 V.

4.11.3. Recommendation for Intel® Platforms

The following tables list examples of components that comply with Intel's recommendations, when configured in the topology discussed in Figure 15.

Table 12. Component Recommendations – Inductor

Part Number	Value	Tol.	SRF	Rated I	DCR (Typical)
TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max.)
Murata LQG21N4R7K00T1	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (±50%)
Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3 Ω max.

Table 13. Component Recommendations - Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%	2.5 nH	0.2 Ω

Table 14. Component Recommendations - Resistor

Value	Tolerance	Power	Note
1 Ω	10%	1/16 W	Resistor may be implemented with trace resistance, in which discrete R is not needed.

To satisfy damping requirements, total series resistance in the filter (from VCC_{CORE} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor may be in the form of a discrete component or routing, or both. For example, if the picked inductor has a minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, when using discrete R1 (1 Ω ± 1%), the maximum DCR of the L (trace plus inductor) should be less than 2.0 – 1.1 = 0.9 Ω, which precludes the use of some inductors and will set the max. trace length.

Other routing requirements:

- The capacitor (C) should be close to the PLL1 and PLL2 pins, <0.1 Ω per route[1].
- The PLL2 route should be parallel and next to the PLL1 route (minimize loop area).
- The inductor (L) should be close to C. Any routing resistance should be inserted between VCC_{CORE} and L.
- Any discrete resistor (R) should be inserted between VCC_{CORE} and L.

[1] These routes do not count towards the minimum damping R requirement.

Figure 15. Example PLL Filter Using a Discrete Resistor

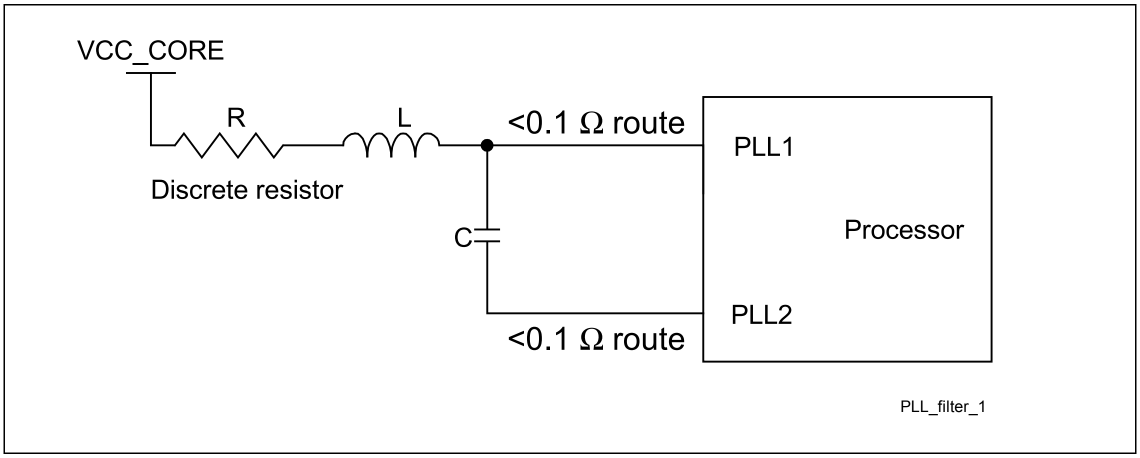
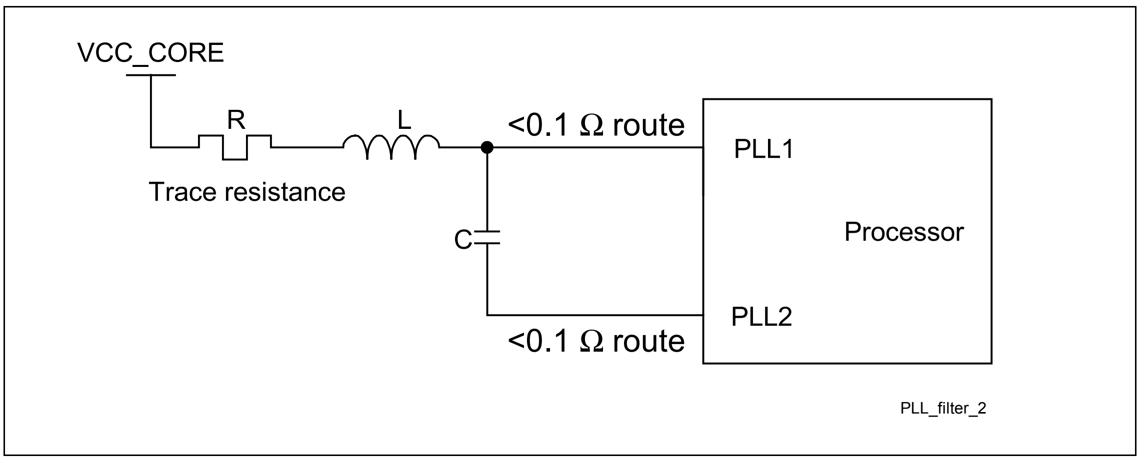


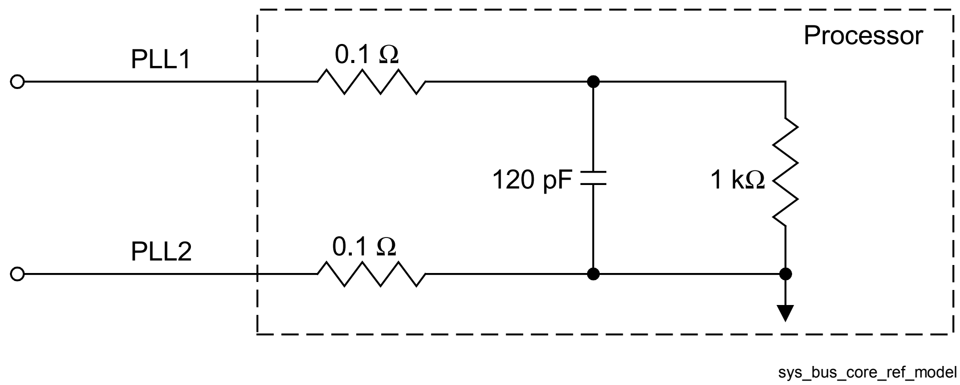
Figure 16. Example PLL Filter Using a Buried Resistor



4.11.4. Custom Solutions

As long as the filter performance and requirements specified and outlined in Section 4.11.2 are satisfied, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in the following figure.

Figure 17. Core Reference Model



NOTES:
1. 0.1-Ω resistors represent package routing. (For other modules (e.g., interposer, DMM), adjust the routing resistor if desired, but use minimum numbers.)
2. 120-pF capacitor represents internal decoupling capacitor.
3. 1-kΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Sweep across component/parasitic tolerances.

To observe the IR drop, use a DC current of 30 mA and the minimum Vcc_{CORE} level.

4.12. Voltage Regulation Guidelines

In a *flexible PGA370* design, the voltage regulation module (VRM) or on-board voltage regulator (VR) must be compliant with Intel *VRM 8.4 DC-DC Converter Design Guidelines*, revision 1.6 or higher. This is necessary to support the power supply requirements of the FC-PGA Intel Pentium III processor at speeds greater than 650 MHz.

4.13. Decoupling Guidelines for Flexible PGA370 Designs

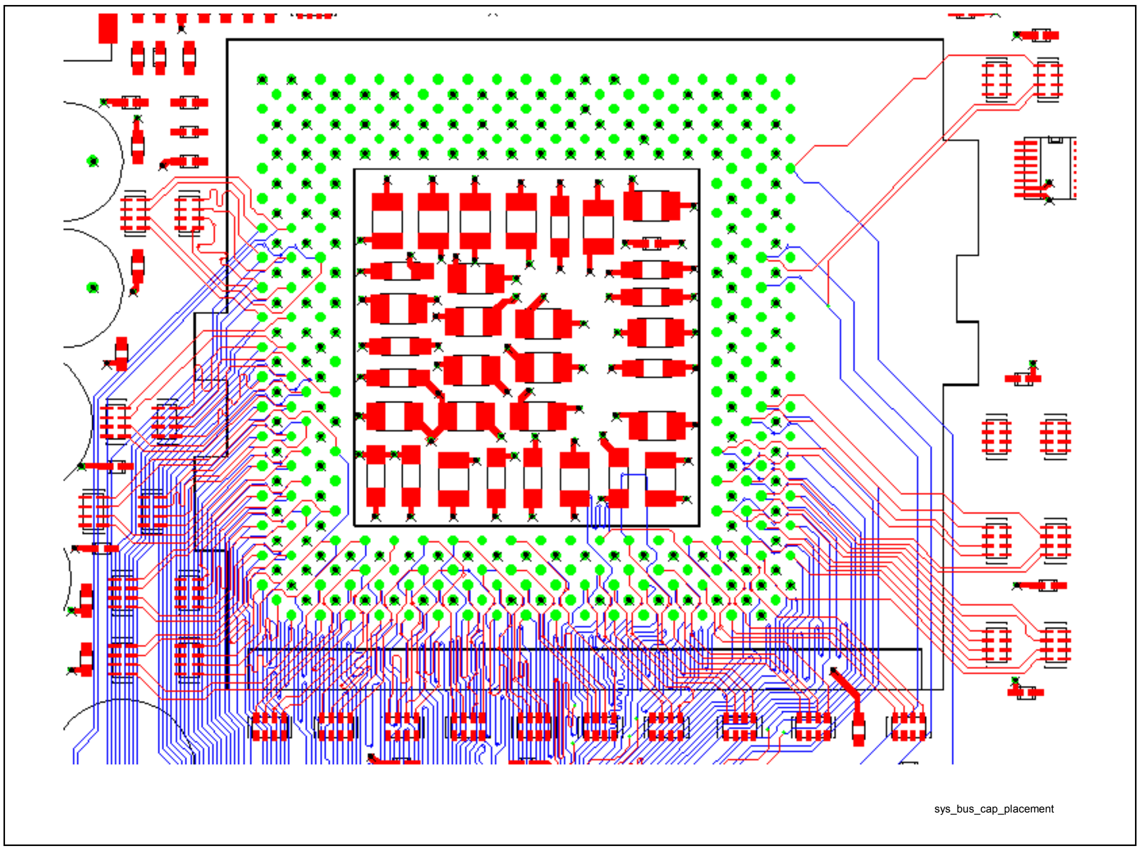
These are preliminary decoupling guidelines for *flexible PGA370* designs and are estimated to meet the specifications of *VRM 8.4 DC-DC Converter Design Guidelines*, ver. 1.6.

4.13.1. Vcc_{CORE} Decoupling Design

Ten or more 4.7-µF capacitors in 1206 packages.

All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between Vcc_{CORE} / Vss power pins, as shown in the following figure.

Figure 18. Capacitor Placement on the Motherboard



4.13.2. Vtt Decoupling Design

For Itt = 3.0A (max.)

Nineteen 0.1-µF capacitors in 0603 packages placed within 200 mils of AGTL+ termination R-packs, with one capacitor for every two R-packs. These capacitors are shown at the exterior in the previous figure.

4.13.3. VREF Decoupling Design

Four 0.1-µF capacitors in a 0603 package placed near the VREF pins (within 500 mils).

4.14. Thermal/EMI Considerations

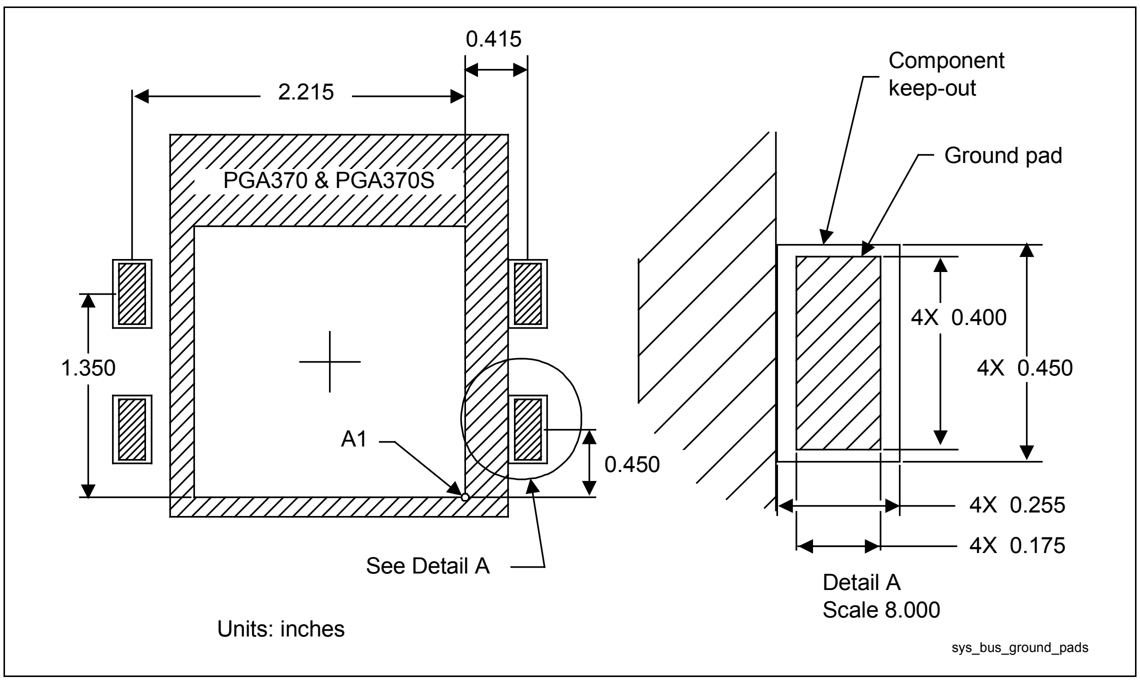
Heat sink requirements will be different for FC-PGA processors than for previous processors using PPGA packaging. The current flexible motherboard guideline for the FC-PGA Intel Pentium III processor calls for 30.4 W.

- Increase power density for the FC-PGA Intel® Pentium® III processor (FMB = 41.9 W/cm^2).
- Different thermal design verification for FC-PGA compared with PPGA-packaged processors. The FC-PGA Intel Pentium III processor is specified using Tj versus Tcase (used with Intel Celeron™ processors).
- New heatsink for FC-PGA package that is not backwards-compatible with PPGA processors.
- New heatsink clips for FC-PGA processor heatsinks.
- Option to add motherboard features to ground the processor heatsink for opportunity to reduce electromagnetic interference (EMI).

4.14.1. Optional Grounded Heatsink Implementation for EMI Reduction

The following figure shows the concept for providing an AC ground return path to the processor heat sink. Experiments at Intel demonstrate improved EMI emissions with prototypes of this solution. Further details will be provided in the next revision of this design guide.

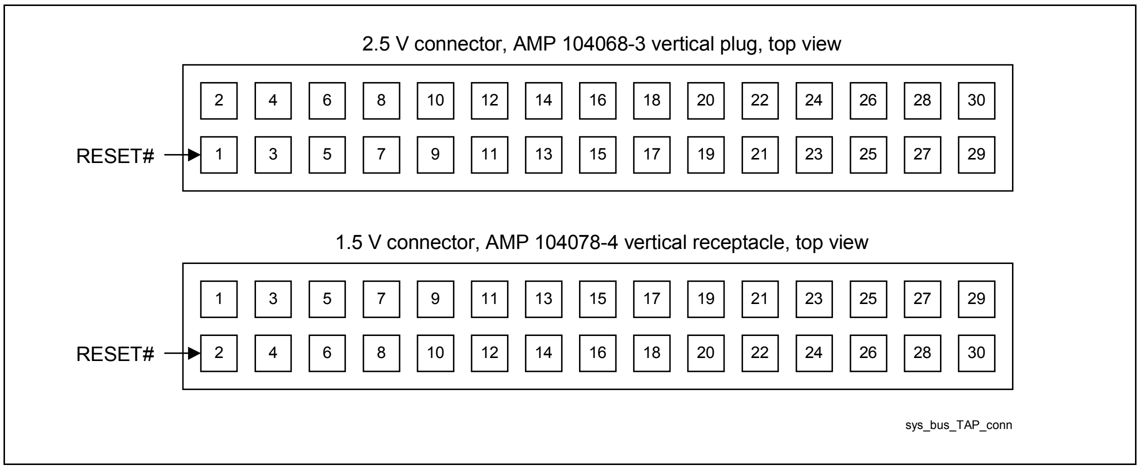
Figure 19. Location of Grounding Pads



4.15. Debug Port Changes

Due to the lower-voltage technology employed in the FC-PGA processor, changes are required to support the debug port. Previously, the test access port (TAP) signals used 2.5-V logic. This is the case with the Intel Celeron™ processor in the PPGA package. FC-PGA processors utilize 1.5-V logic levels on the TAP. As a result, a new debug port connector is to be used on *flexible PGA370* designs. The new 1.5-V connector is the mirror image of the older 2.5-V connector. Either connector will fit into the same printed circuit board layout. Just the pin numbers would change, as can be seen in the following drawing. Along with the new connector, an In-Target Probe (ITP) capable of communicating with the TAP at 1.5-V logic levels is required.

Figure 20. TAP Connector Comparison



Caution: FC-PGA processors require an in-target probe (ITP) compatible with 1.5-V signal levels on the TAP. Previous ITPs are designed to work with higher voltages and may damage the processor if they are connected to an FC-PGA processor.

See the processor datasheet for more information regarding the debug port.

4.16. FCPGA Heatsink keepout Zone

Figure 4.1 shows the system component keep-out volume above the socket connector required for the reference design thermal solution for high frequency FC-PGA processors. This keep-out envelope provides adequate room for the heat sink, fan and attach hardware under static conditions as well as room for installation of these components on the socket.

Figure 4.2 shows component keep-outs on the motherboard required to prevent interference with the reference design thermal solution. Note portions of the heat sink and attach hardware hang over the motherboard.

Adhering to these keep-out areas will ensure compatibility with Intel boxed processor products and Intel enabled third party vendor thermal solutions for FC-PGA processors. While the keep-out requirements should provide adequate space for the reference design thermal solution, systems integrators should check their vendor to ensure their specific thermal solutions fit within their specific system designs. Please ensure that the thermal solutions under analysis comprehend the specific thermal design requirements for higher frequency Pentium III processors.

While thermal solutions for lower frequency FC-PGA processors may not require the full keep-out area, larger thermal solutions will be required for higher frequency processors and failure to adhere to the guidelines will result in mechanical interference.

Figure 21. Heat Sink Volumetric Keep Out Regions

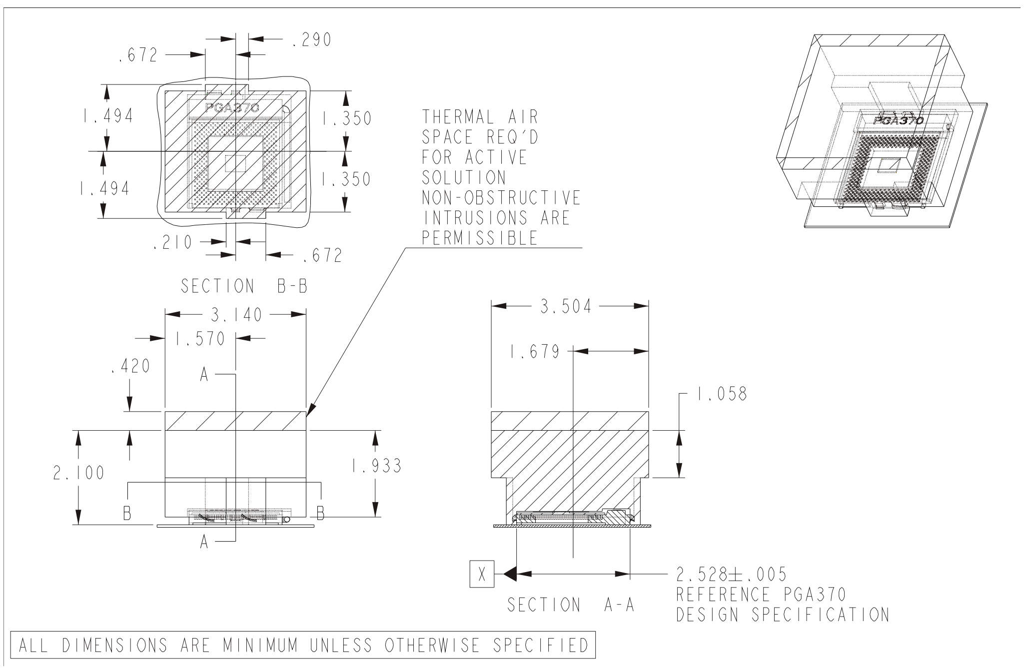
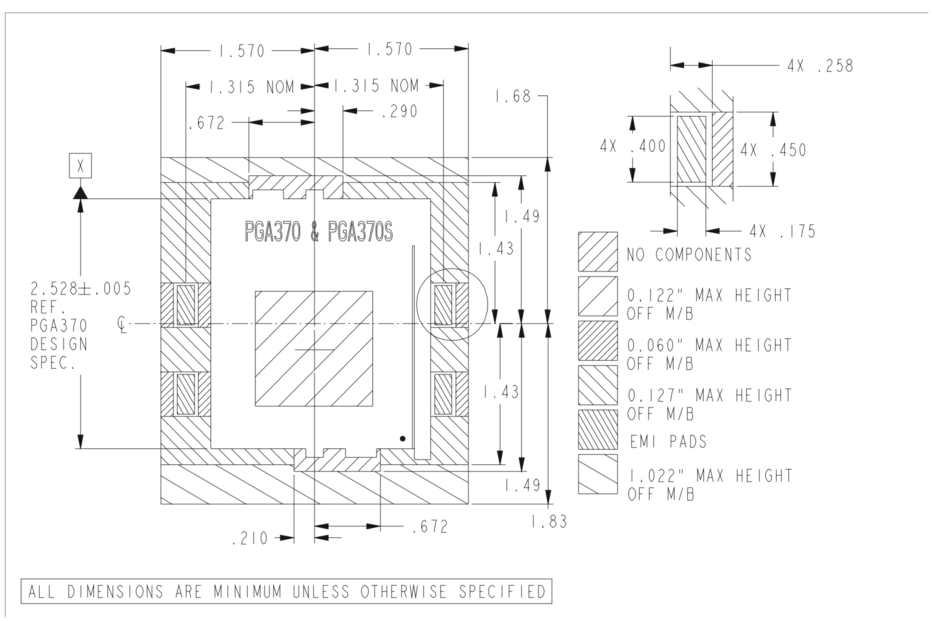


Figure 22. Motherboard Component Keep Out Regions



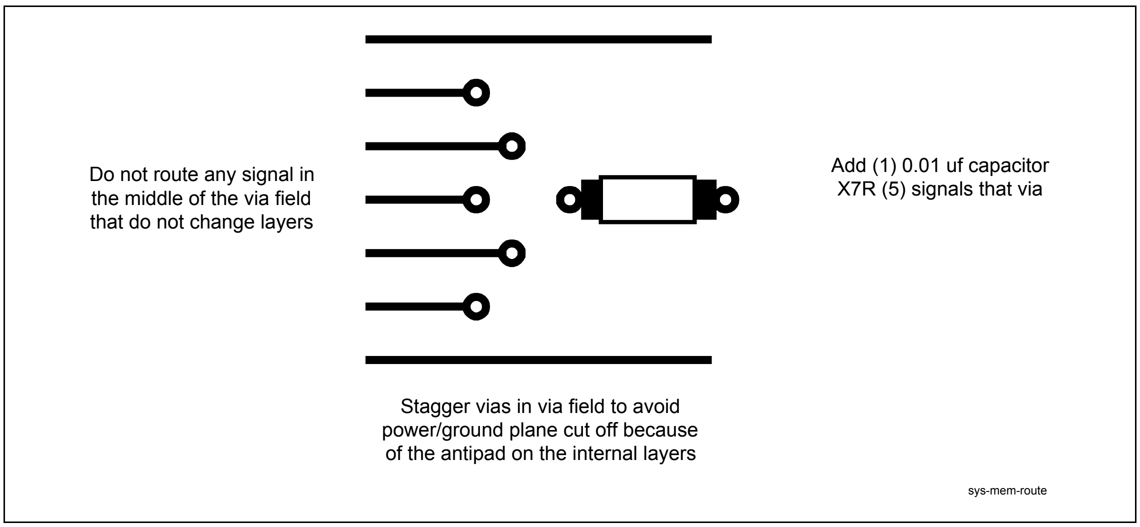
5. System Memory Design Guidelines

5.1. System Memory Routing Guidelines

Ground plane reference all system memory signals. To provide a good current return path and limit noise on the system memory signals, the signals should be ground referenced from the GMCH to the DIMM connectors and from DIMM connector to DIMM connector. If ground referencing is not possible, system memory signals should be, at a minimum, referenced to a single plane. If single plane referencing is not possible, stitching capacitors should be added no more than 200 mils from the signal via field. System memory signals may via to the backside of the PCB under the GMCH without a stitching capacitor as long as the trace on the topside of the PCB is less than 200 mils. Note that it is recommended that a parallel plate capacitor between VCC3.3SUS and GND be added to account for the current return path discontinuity (See decoupling section 15). Use (1) .01 uF X7R capacitor per every (5) system memory signals that switch plane references. No more than two vias are allowed on any system memory signal.

If a group of system memory signals needs to change layers, a via field should be created and a decoupling capacitor should be added at the end of the via field. Do not route signals in the middle of a via field; this will cause noise to be generated on the current return path of these signals and can lead to issues on these signals. See figure below. The traces shown are on layer 1 only. The figure shows signals that are changing layer and two signals that are not changing layer. Note the two signals around the via field create a keep out zone where no signals that do not change layer should be routed.

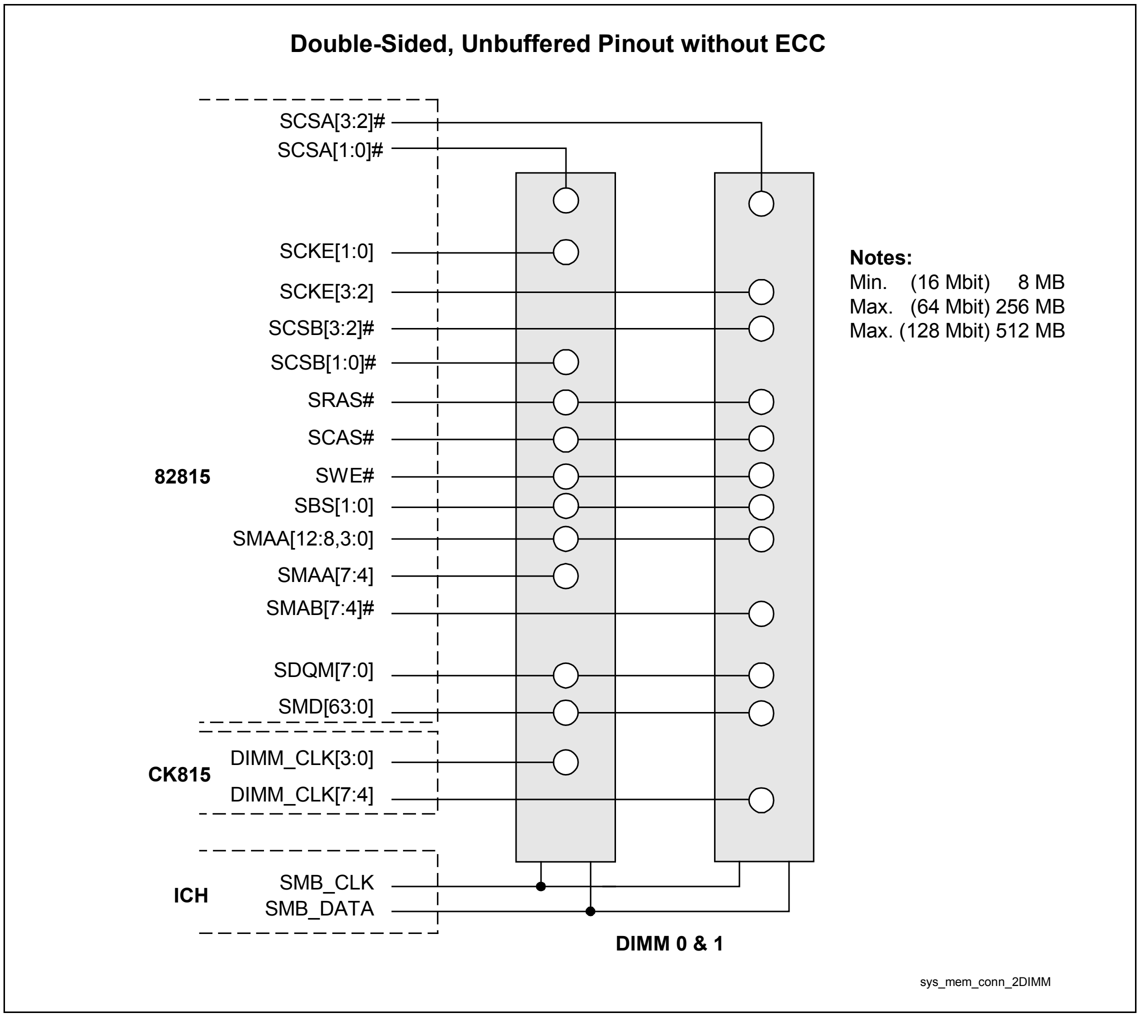
Figure 23. System Memory Routing Guidelines



5.2. System Memory 2-DIMM Design Guidelines

5.2.1. System Memory 2-DIMM Connectivity

Figure 24. System Memory Connectivity (2 DIMM)



5.2.2. System Memory 2-DIMM Layout Guidelines

Figure 25. System Memory 2-DIMM Routing Topologies

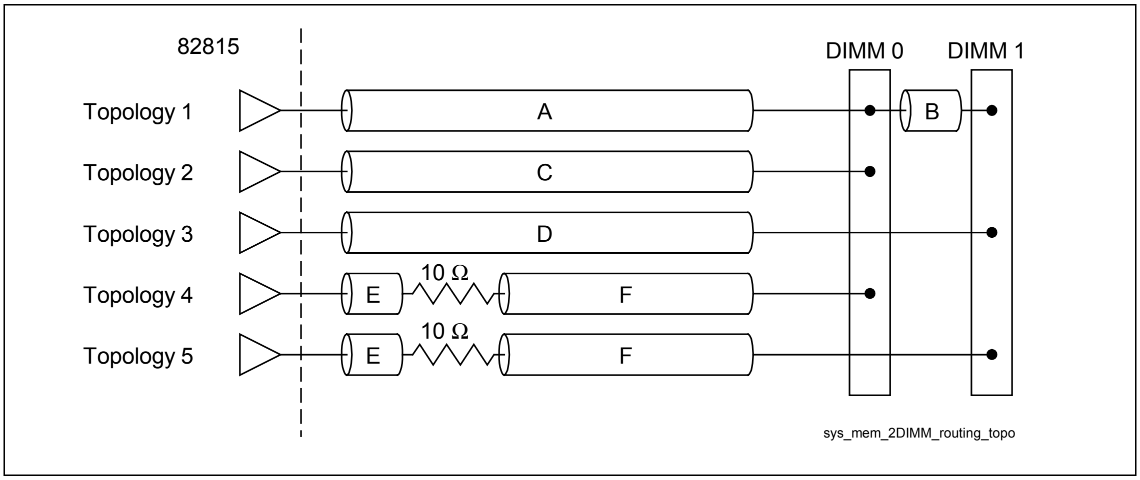
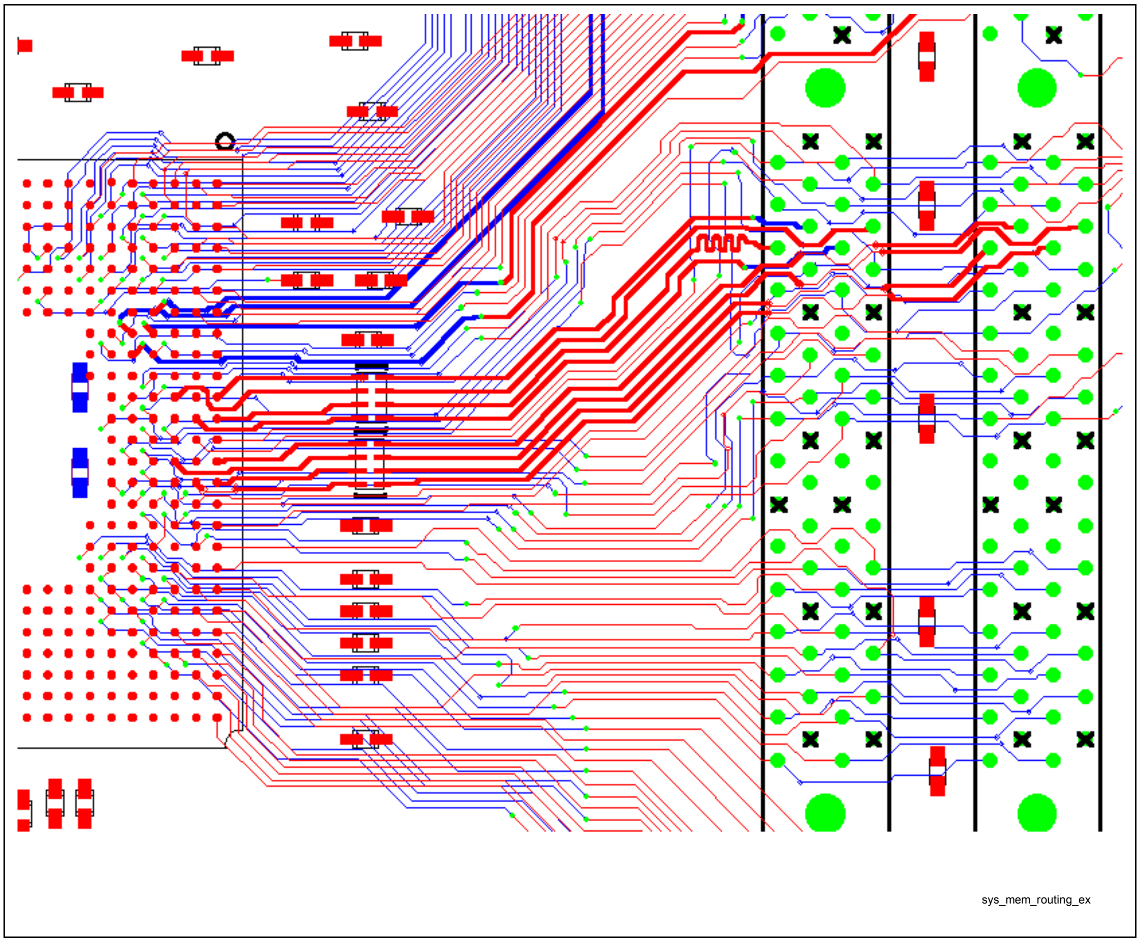


Table 15. System Memory 2-DIMM Solution Space

				Trace Lengths (inches)											
Signal	Top	Trace (mils)		A		B		C		D		E		F	
		Width	Spacing	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SCS[3:2]#	3	5	10							1	4.5				
SCS[1:0]#	2	5	10					1	4.5						
SMAA[7:4]	4	10	10									0.4	0.5	2	4
SMAB[7:4]#	5	10	10									0.4	0.5	2	4
SCKE[3:2]	3	10	10							3	4				
SCKE[1:0]	2	10	10					3	4						
SMD[63:0]	1	5	10	1.75	4	0.4	0.5								
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5								
SCAS#, SRAS#, SWE#	1	5	10	1	4.0	0.4	0.5								
SBS[1:0], SMAA[12:8,3:0]	1	5	10	1	4.0	0.4	0.5								

Figure 26. System Memory Routing Example



Routing in the previous figure is for example purposes only. It does not necessarily represent complete and correct routing for this interface.

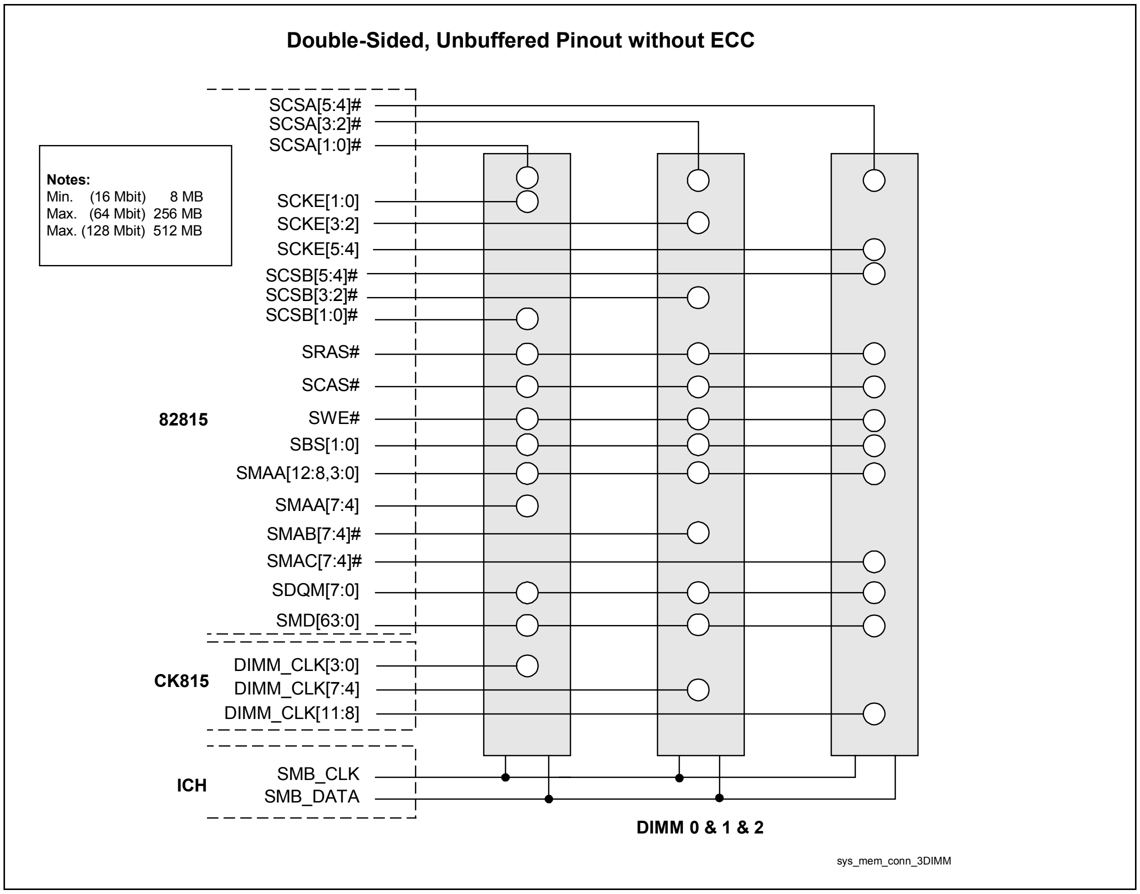
5.2.2.1. System Memory Bus Isolation

In addition to meeting the spacing requirements outlined in Table 15, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

5.3. System Memory 3-DIMM Design Guidelines

5.3.1. System Memory 3-DIMM Connectivity

Figure 27. System Memory Connectivity (3 DIMM)



5.3.2. System Memory 3-DIMM Layout Guidelines

Figure 28. System Memory 3-DIMM Routing Topologies

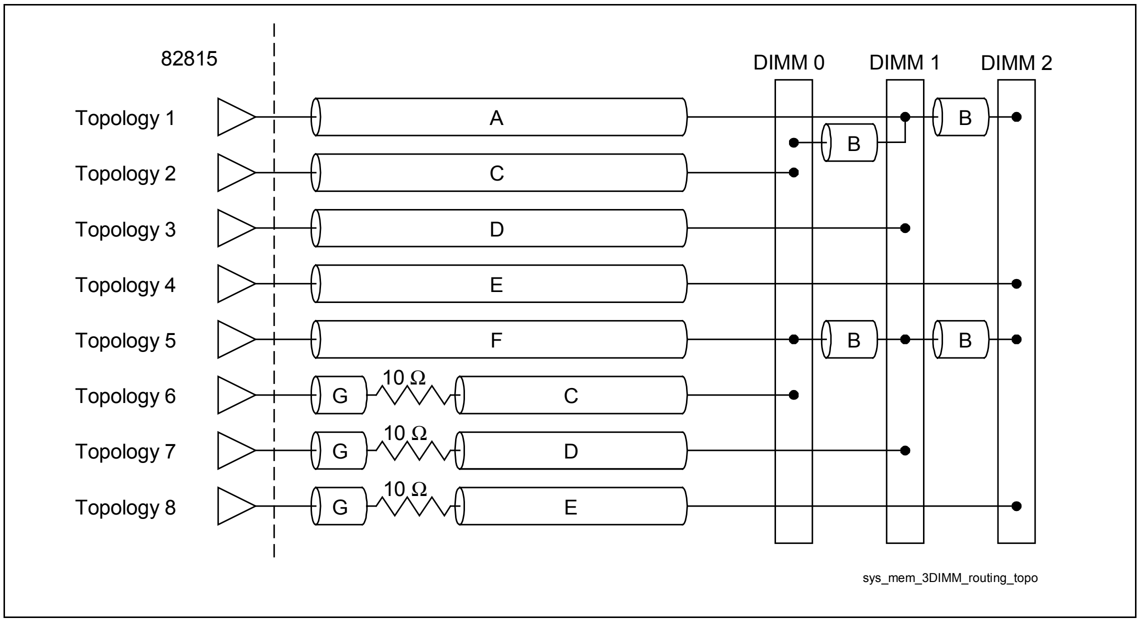


Table 16. System Memory 3-DIMM Solution Space

				Trace Lengths (inches)													
		Trace (mils)		A		B		C		D		E		F		G	
Signal	Top	Width	Spacing	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SCS[5:4]#	4	5	10									1	4.5				
SCS[3:2]#	3	5	10							1	4.5						
SCS[1:0]#	2	5	10					1	4.5								
SMAA[7:4]	6	10	10					2	4							0.4	0.5
SMAB[7:4]#	7	10	10							2	4					0.4	0.5
SMAC[7:4}	8	10	10									2	4			0.4	0.5
SCKE[5:4]	4	10	10									3	4				
SCKE[3:2]	3	10	10							3	4						
SCKE[1:0]	2	10	10					3	4								
SMD[63:0]	1	5	10	1.75	4	0.4	0.5										
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5										
SCAS#, SRAS#, SWE#	5	5	10			0.4	0.5							1	4		
SBS[1:0], SMAA[12:8,3:0]	5	5	10			0.4	0.5							1	4		

5.3.2.1. System Memory Bus Isolation

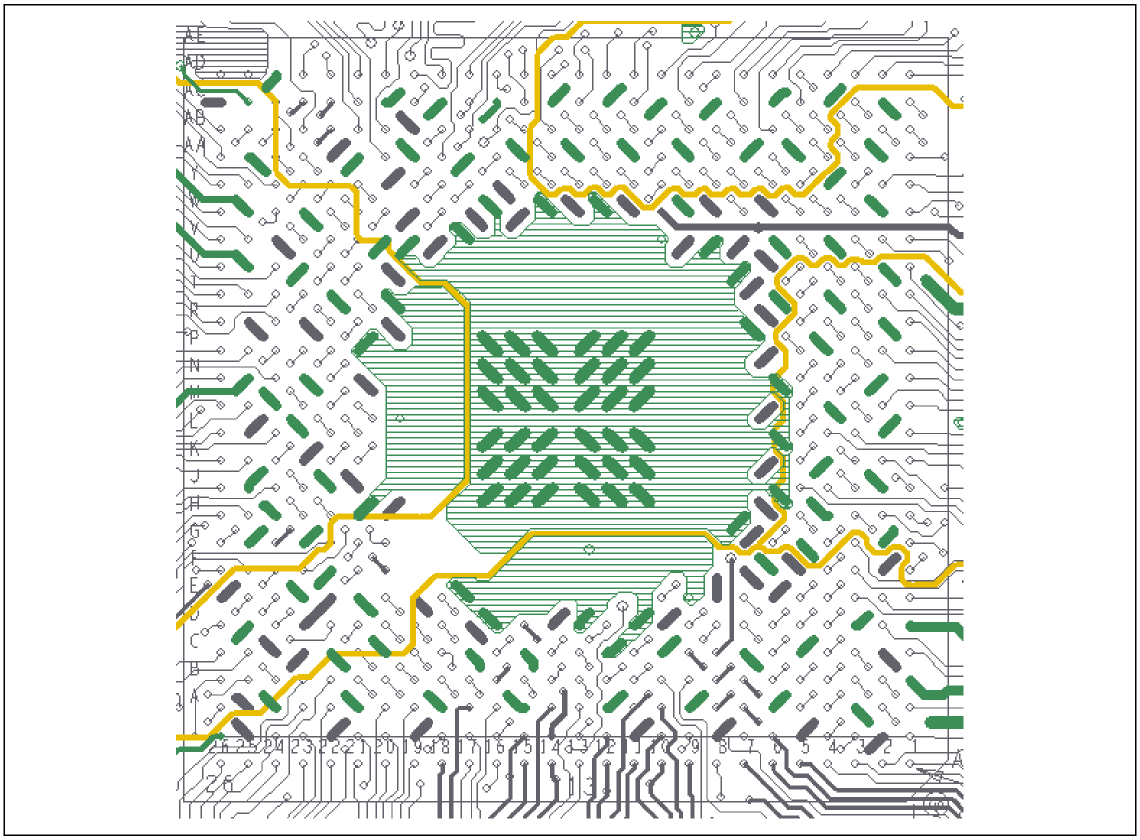
In addition to meeting the spacing requirements outlined in Table 16, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

5.4. System Memory Decoupling Guidelines

A minimum of eight 0.1-µF low-ESL ceramic capacitors (e.g., 0603 body type, X7R dielectric) are required and must be as close as possible to the GMCH. They should be placed within at most 70 mils to the edge of the GMCH package edge for VSUS_3.3 decoupling, and they should be evenly distributed around the system memory interface signal field including the side of the GMCH where the system memory interface meets the host interface. There are power and GND balls throughout the system memory ball field of the GMCH that need good local decoupling. Make sure to use at least 14 mil drilled vias and wide traces from the pads of the capacitor to the power or ground plane to create a low inductance path. If possible multiple vias per capacitor pad are recommended to further reduce inductance. In order to add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (500 mils maximum).

To further de-couple the GMCH and provide a solid current return path for the system memory interface signals it is recommended that a parallel plate capacitor be added under the GMCH. Add a topside or bottom side copper flood under center of the GMCH to create a parallel plate capacitor between VCC3.3 and GND, See following figure. The dashed lines indicate power plane splits on layer 2 or layer 3 depending on stack-up. The filled region in the middle of the GMCH indicates a ground plate (on layer 1 if the power plane is on layer 2 or on layer 4 if the power layer is on layer 3).

Figure 29. Intel® 815 Chipset Decoupling Example

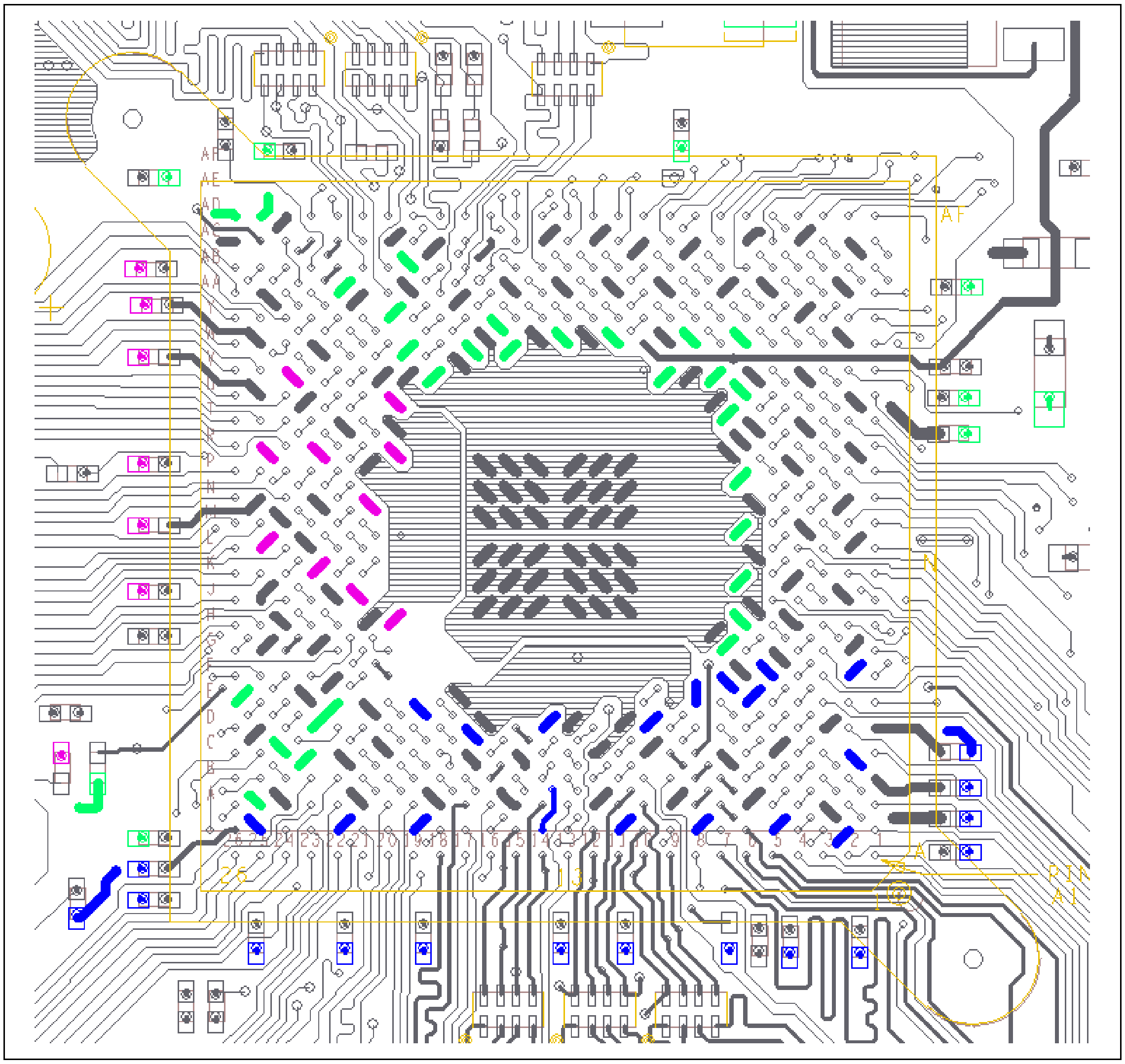


Yellow lines show layer two plane splits. Note that the layer 1 shapes do NOT cross the plane splits. The southern shape is a Vss fill over VddSDRAM. The western shape is a Vss fill over VddAGP. The larger northeastern shape is a Vss fill over VddCORE.

Additional decoupling capacitors should be added between the DIMM connectors to provide a current return path for the reference plane discontinuity created by the DIMM connectors themselves. (1) .01uf X7R capacitor should be added per every (10) SDRAM signals. Capacitors should be placed between the DIMM connectors and evenly spread out across the SDRAM interface.

For debug purposes, four or more 0603 capacitor sites should be placed on the backside of the board, evenly distributed under the Intel 815 chipset's system memory interface signal field.

Figure 30. Intel® 815 Chipset Decoupling Example



5.5. Compensation

A system memory compensation resistor (SRCOMP) is used by the GMCH to adjust the buffer characteristics to specific board and operating environment characteristics. Refer to the *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) Datasheet* for details on compensation. Tie the SRCOMP pin of the GMCH to 40-Ω 1% or 2% pull-up resistor to 3.3 Vsus (3.3-volt standby) via a 10-mil-wide, 0.5" trace (targeted for a nominal impedance of 40 Ω).

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6. AGP/Display Cache Design Guidelines

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms) refer to the latest *AGP Interface Specification, Revision 2.0*, which can be obtained from http://www.agpforum.org. This design guide (*Intel® 815 Chipset Platform Design Guide*) focuses only on specific Intel 815 chipset platform recommendations.

6.1. AGP Interface

A single AGP connector is supported by the GMCH's AGP interface. LOCK# and SERR#/PERR# are not supported. See the display cache discussion for a display cache/AGP muxing description and a description of the AGP In-Line Memory Module (AIMM).

The AGP buffers operate in one of two selectable modes to support the AGP universal connector:

- 3.3-V drive, not 5-V safe. This mode is compliant with the AGP 1.0 66-MHz spec.
- 1.5-V drive, not 3.3-V safe. This mode is compliant with the AGP 2.0 spec.

AGP 4X must operate at 1.5 V. AGP 2X can operate at 3.3 V or 1.5 V. The AGP interface supports up to 4X AGP signaling, though 4X fast writes are not supported. AGP semantic cycles to DRAM are not snooped on the host bus.

The GMCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. The GMCH contains a 32-deep AGP request queue. High priority accesses are supported. All AGP semantic accesses hitting the graphics aperture pass through an address translation mechanism with a fully-associative 20-entry TLB.

Accesses between AGP and the hub interface are limited to hub interface-originated memory writes to AGP. Cacheable accesses from the IOQ queue flow through one path, while aperture accesses follow another path. Cacheable AGP (SBA,PIPE#, and FRAME#) reads to DRAM all snoop the cacheable global write buffer (GWB) for system data coherency. Aperture AGP (SBA, PIPE#) reads to DRAM snoop the aperture queue (GCMCRWQ). Aperture AGP (FRAME#) reads and writes to DRAM proceed through a FIFO and there is no RAW capability, so no snoop is required.

The AGP interface is clocked from the 66-MHz clock (3V66). The AGP-to-host/memory interface is synchronous with a clock ratio of 1:1 (66 MHz : 66 MHz), 2:3 (66 MHz : 100 MHz) and 1:2 (66 MHz : 133 MHz).

6.1.1. AGP In-Line Memory Module (AIMM)

The GMCH multiplexes the AGP signal interface with the integrated graphics' display cache interface. As a result, for a flexible motherboard that supports both integrated graphics and add-in AGP video cards, a display cache (for integrated graphics) must be populated on a card in the universal AGP slot. The card is called an AGP In-Line Memory Module (AIMM) card. Intel provides the specification for this card in a separate document called the *AGP In-Line Memory Module Specification.*

AGP guidelines are presented in this section for motherboards that support the population of an AIMM card in their AGP slot, as well as for those that do not. Where there are distinct guidelines dependent on whether or not a motherboard will support an AIMM card, the section detailing routing guidelines will be broken in to subsections, as follows:

- Follow the subsection entitled "Flexible Motherboard Guidelines," if the motherboard supports an AIMM card populated in the AGP slot.
- Follow the subsection entitled "AGP Only Motherboard Guidelines," if the motherboard will NOT support an AIMM card populated in the AGP slot.

6.1.2. AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that AGP cards and AGP In Line Memory Module (AIMM) cards may come unseated during system shipping and handling without proper retention. To avoid disengaged AGP cards and AIMM modules, Intel recommends that AGP based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket that is used to properly locate the card with respect to the chassis and to assist with card retention. The AGP RM is available in two different handle orientations: left-handed (see Figure 31) and right-handed. Most system boards accommodate the left-handed AGP RM. The manufacturing capacity of the left-handed RM currently exceeds the right-handed capacity, and as a result Intel recommends that customers design their systems to insure they can use the left-handed version of the AGP RM (see Figure 32). The right-handed AGP RM is identical to the left-handed AGP RM, except for the position of the actuation handle. This handle is located on the same end as the primary design, but extends from the opposite side (mirrored about the center axis running parallel to the length of the part). Figure 32 contains keep out information for the left hand AGP retention mechanism. Use this information to make sure that your motherboard design leaves adequate space to install the retention mechanism.

The AGP interconnect design requires that the AGP card must be retained to the extent that the card not back out more than 0.99 mm (0.039 in) within the AGP connector. To accomplish this it is recommended that new cards implement an additional notch feature in the mechanical keying tab to allow an anchor point on the AGP card for interfacing with an AGP RM. The retention mechanism's round peg engages with the AGP or AIMM card's retention tab and prevents the card from disengaging during dynamic loading. The additional notch feature in the mechanical keying tab is required for 1.5-volt AGP cards and is recommended for the new 3.3-volt AGP cards.

Figure 31. AGP Left-Handed Retention Mechanism

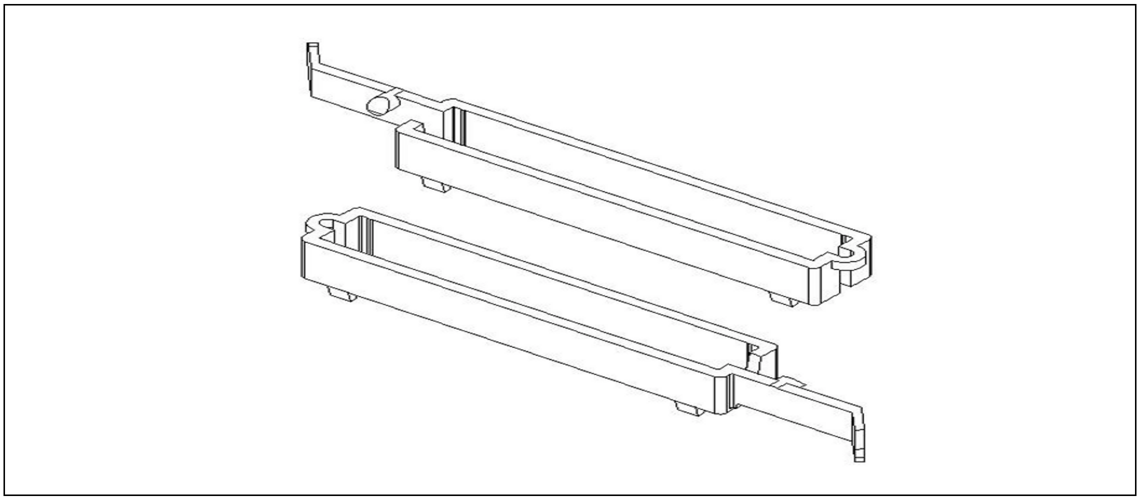
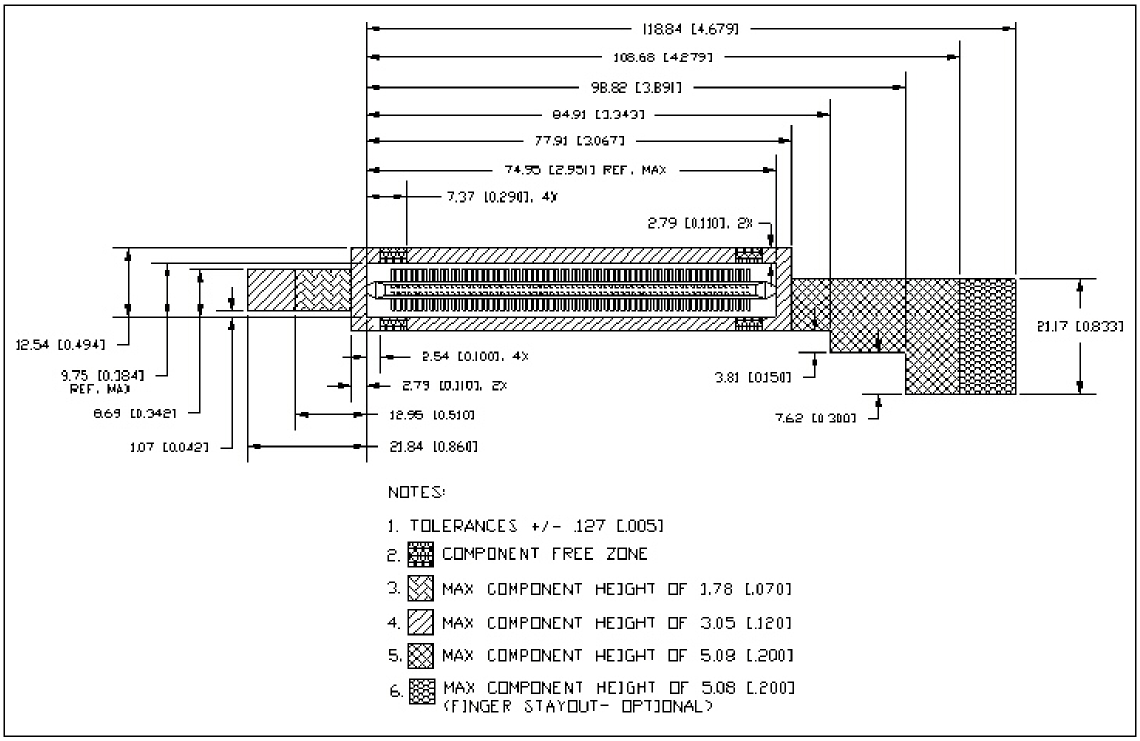


Figure 32. AGP Left-Handed Retention Mechanism Keep Out Information



Engineering Change Request number 48 (ECR #48) of the AGP specification details the AGP RM, which is recommended for all AGP cards. These are approved changes to the Accelerated Graphics Port (AGP) Interface Specification, Revision 2.0. Intel intends to incorporate the AGP RM changes into later revisions of the AGP Interface Specification. In addition, Intel has defined a reference design of a mechanical device to utilize the features defined in ECR #48.

ECR #48 can be viewed off the Intel Web site at:

http://developer.intel.com/technology/agp/ecr.htm

More information regarding this component (AGP RM) is available from the following vendors.

Resin Color	Supplier Part Number	"Left Handed" Orientation (Preferred)	"Right Handed" Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

6.2. AGP 2.0

The AGP Interface Specification, rev. 2.0, enhances the functionality of the original AGP Interface Specification (rev. 1.0) by allowing 4X data transfers (i.e., 4 data samples per clock) and 1.5-volt operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66-MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66-MHz) clock or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66-MHz clock cycle, therefore the data cycle time is 7.5 ns. To allow for these high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on AGP (1.5 V) requires even more noise immunity. For example, during 1.5-V operation, V_{ilmax} is 570 mv. Without proper isolation, cross-talk could create signal integrity issues.

6.2.1. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: *1X timing domain signals*, *2X/4X timing domain signals*, and *miscellaneous signals*. Each group has different routing requirements. In addition, within the *2X/4X timing domain signals*, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. However, trace length matching requirements only need to be met within each set of 2X/4X timing domain signals.

The signal groups are documented in the following table.

Table 17. AGP 2.0 Signal Groups

Group	Signal
1X timing domain	• CLK (3.3 V), RBF#, WBF#, ST[2:0], PIPE#, REQ#, GNT#, PAR, FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#
2X / 4X timing domain	• **Set #1**: AD[15:0], C/BE[1:0]#, AD_STB0, AD_STB0#1[1] • **Set #2**: AD[31:16], C/BE[3:2]#, AD_STB1, AD_STB1#[1] • **Set #3**: SBA[7:0], SB_STB, SB_STB#1
Miscellaneous, async	• USB+, USB-, OVRCNT#, PME#, TYPDET#, PERR#, SERR#, INTA#, INTB#

NOTES:

1. These signals are used in 4X AGP mode ONLY.

Table 18. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section, the term *data* refers to AD[31:0], C/BE[3:0]#, and SBA[7:0]. The term *strobe* refers to AD_STB[1:0], AD_STB#[1:0], SB_STB, and SB_STB#. When the term *data* is used, it refers to one of the three sets of data signals, as in Table 17. When the term *strobe* is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (*1X timing domain signals*, *2X/4X timing domain signals*, and *miscellaneous signals)* will be addressed separately.

6.3. AGP Routing Guidelines

6.3.1. 1X Timing Domain Routing Guidelines

6.3.1.1. Flexible Motherboard Guidelines

- The AGP 1X timing domain signals (refer to Table 17) have a maximum trace length of 4" for motherboards that support an AGP In-Line Memory Module (AIMM) card. This maximum applies to ALL signals listed as 1X timing domain signals in Table 17.
- AGP 1X signals multiplexed with display cached signals (listed in the following table) should be routed with a 1:3 trace width-to-spacing ratio. All other AGP 1X timing domain signals can be routed with 5-mil minimum trace separation.
- There are no trace length matching requirements for 1X timing domain signals.

Table 19. Multiplexed AGP1X Signals on Flexible Motherboards

AGP 1X Signal Names	
RBF#	FRAME#
ST[2:0]	IRDY#
PIPE#	TRDY#
REQ#	STOP#
GNT#	DEVSEL#
PAR	

6.3.1.2. AGP-Only Motherboard Guidelines

- The AGP 1X timing domain signals (refer to Table 17) have a maximum trace length of 7.5" for motherboards that will **NOT** support an AGP In-Line Memory Module (AIMM) card. This maximum applies to ALL signals listed as 1X timing domain signals in Table 17.
- All AGP 1X timing domain signals can be routed with 5-mil minimum trace separation.
- There are no trace length matching requirements for 1X timing domain signals.

6.3.2. 2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to ALL signals listed in Table 17 as 2X/4X timing domain signals. These signals should be routed using 5-mil (60-Ω) traces.

The maximum line length and length mismatch requirements depend on the routing rules used on the motherboard. These routing rules were created to provide design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6") and long AGP interfaces (e.g., > 6" and < 7.25") are documented separately. The maximum length allowed for the AGP interface (on AGP-only motherboards) is 7.25".

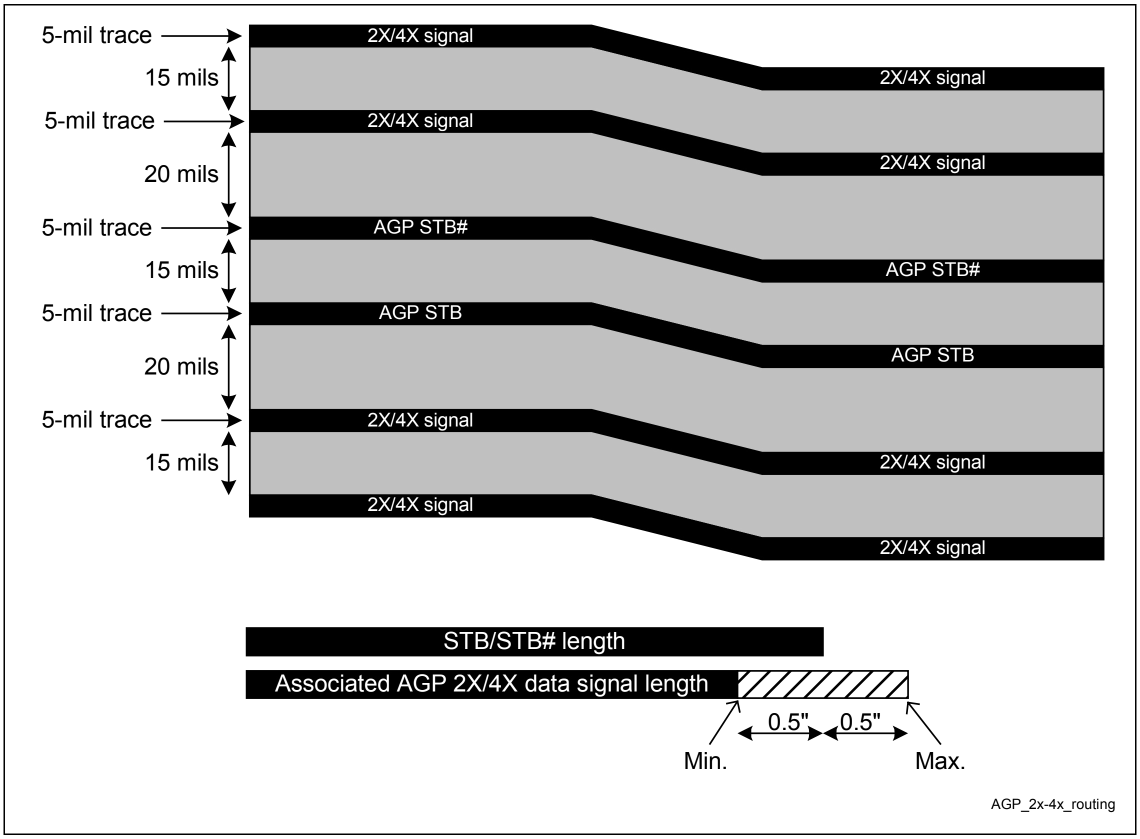
6.3.2.1. Flexible Motherboard Guidelines

- For motherboards that support either an AGP card or an AIMM card in the AGP slot, the maximum length of AGP 2X/4X timing domain signals is 4”.
- 1:3 trace width-to-spacing is required for AGP 2X/4X signal traces.
- AGP 2X/4X signals must be matched their associated strobe (as outlined in Table 17), within ±0.5”.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) is 3.7” long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) could be 3.2” to 4” long (since there is a 4” max. length). Another strobe set (e.g., SB_STB and SB_STB#) could be 3.1” long, so that the associated data signals (e.g., SBA[7:0]) could be 2.6” to 3.6” long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Since each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed using 5-mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals—and all other signals—by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1.” (That is, a strobe and its complement must be the same length within 0.1.”).

Figure 33. AGP 2X/4X Routing Example for Interfaces < 6” and AIMM/AGP Solutions



6.3.2.2. AGP-Only Motherboard Guidelines

For motherboards that will not support an AIMM card populated in the AGP slot, the maximum AGP 2X/4X signal trace length is 7.25”. However, there are different guidelines for AGP interfaces shorter than 6” (e.g., all AGP 2X/4X signals are less than 6” long) and those longer than 6” but shorter than the maximum of 7.25”.

6.3.2.2.1. AGP Interfaces Shorter Than 6”

These guidelines are for designs that require less than 6” between the AGP connector and the GMCH:

- 1:3 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 17), within ±0.5”.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) is 5.3” long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) could be 4.8” to 5.8” long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2” long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 3.7” to 4.7” long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5-mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals—and all other signals—by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1.” (That is, a strobe and its complement must be the same length, within 0.1.”) Refer to the previous figure for an illustration of these requirements.

6.3.2.2.2. AGP Interfaces Longer Than 6”

Because longer lines have more cross-talk, they require more space between traces to reduce the skew. These guidelines are for designs that require more than 6” (but less than the maximum of 7.25”) between the AGP connector and the GMCH, as follows:

- 1:4 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 17), within ±0.125”.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) is 6.5” long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) could be 6.475” to 6.625” long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2” long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 6.075” to 6.325” long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5-mil traces with at least 20 mils of space (1:4) between them. This pair should be separated from the rest of the AGP signals—and all other signals—by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1”. (That is, a strobe and its complement must be the same length, within 0.1”.)

6.3.3. AGP Routing Guideline Considerations and Summary

This section applies to all AGP signals in any motherboard support configuration (e.g., “flexible” or “AGP only”), as follows:

- The 2X/4X timing domain signals can be routed with 5-mil spacing, when breaking out of the GMCH. The routing must widen to the documented requirements, within 0.3” of the GMCH package.
- When matching the trace length for the AGP 4X interface, all traces should be matched from the ball of the GMCH to the pin on the AGP connector. It is not necessary to compensate for the lengths of the AGP signals on the GMCH package.
- Reduce line length mismatch to ensure added margin. Trace length mismatch for all signals within a signal group should be as close to zero as possible, to provide timing margin.
- To reduce trace-to-trace coupling (cross-talk), separate the traces as much as possible.
- All signals in a signal group should be routed on the same layer.
- The trace length and trace spacing requirements ***must*** not be violated by any signal.

Table 20. AGP 2.0 Routing Summary

Signal	Max. Length	Trace Spacing (5-mil Traces)	Length Mismatch	Relative to	Notes
1X Timing Domain	7.5” 4	5 mils	No requirement	N/A	None
2X/4X Timing Domain Set#1	7.25” [4]	20 mils	±0.125”	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	7.25” [4]	20 mils	±0.125”	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	7.25”[4]	20 mils	±0.125”	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length
2X/4X Timing Domain Set#1	6” [3]	15 mils[1]	±0.5”	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6”[3]	15 mils[1]	±0.5”	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6”[3]	15 mils[1]	±0.5”	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils.
2. These guidelines apply to board stack-ups with 15% impedance tolerance.
3. 4” is the maximum length for a flexible motherboards.
4. Solution valid for AGP-only motherboards.

6.3.4. AGP Clock Routing

The maximum total AGP clock skew, between the GMCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but at all points on the clock edge that fall within the switching range. The 1-ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew. (The motherboard designer determines how the 0.9 ns is allocated between the board and the synthesizer.)

For the Intel 815 chipset platform's AGP clock routing guidelines, refer to Section 6.3.

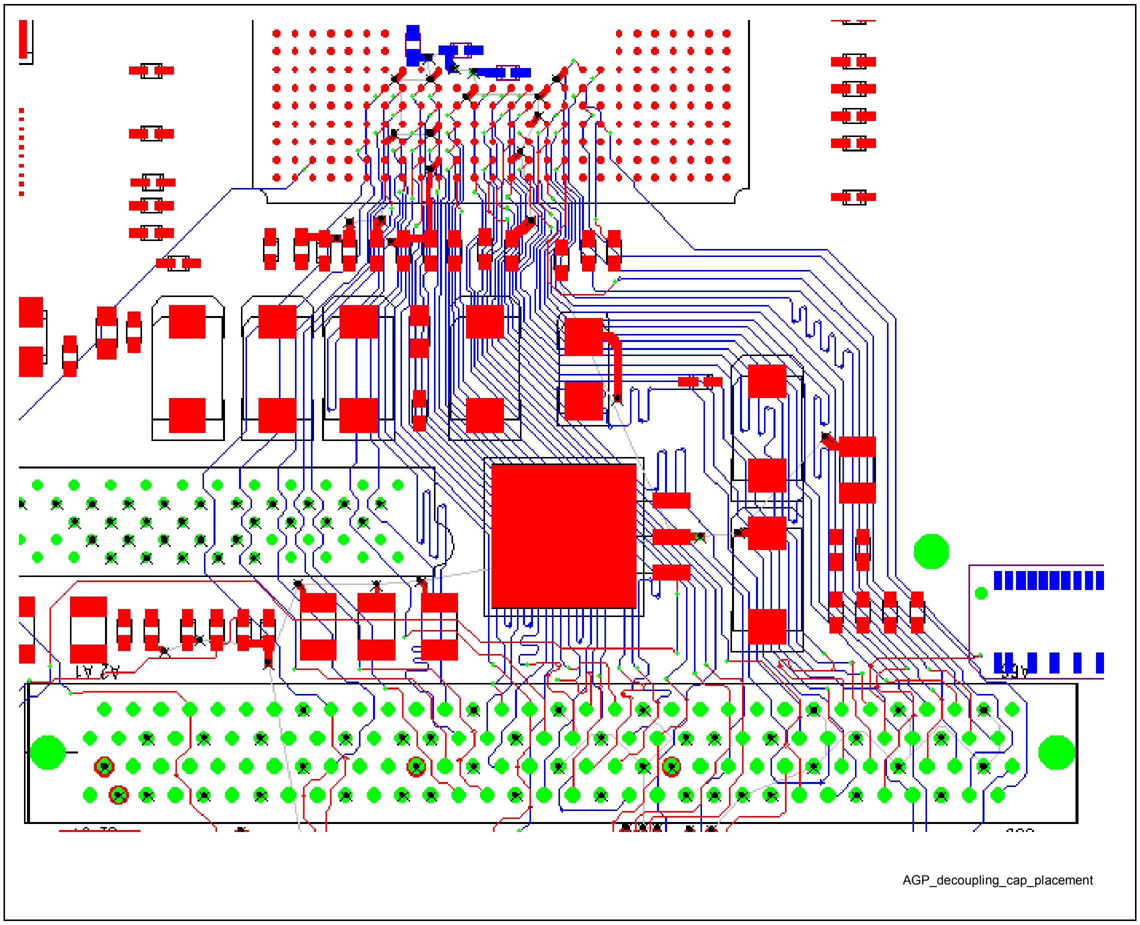
6.3.5. AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the GMCH. The following guidelines are not intended to replace thorough system validation on Intel 815 chipset-based products.

- A minimum of six 0.01-µF capacitors are required and must be as close as possible to the GMCH. These should be placed within 70 mils of the outer row of balls on the GMCH for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- It is recommended that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- To add the decoupling capacitors within 70 mils of the GMCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1" max.).
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. *On a typical four layer PCB design, the signals transition from one side of the board to the other.* One extra 0.01-µF capacitor is required per 10 vias. The capacitor should be placed as close as possible to the center of the via field.

The designer should ensure that the AGP connector is well decoupled, as described in the Rev. 1.0 AGP Design Guide, Section 1.5.3.3.

Figure 34. AGP Decoupling Capacitor Placement Example



The previous figure is for example purposes only. It does not necessarily represent complete and correct routing for this interface.

6.3.6. AGP Routing Ground Reference

It is strongly recommended that at least the following critical signals be referenced to ground from the GMCH to an AGP connector (or to an AGP video controller, if implemented as a “down” solution on an AGP-only motherboard), using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the minimum signal set listed previously, it is strongly recommended that half of all AGP signals be referenced to ground, depending on the board layout. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all Intel 815 chipset designs.

6.4. AGP 2.0 Power Delivery Guidelines

6.4.1. VDDQ Generation and TYPEDET#

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. This voltage is *always* 3.3 V. VDDQ is the interface voltage. In AGP 1.0 implementations, VDDQ was also 3.3 V. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ, as both are tied to the 3.3-V power plane on the motherboard.

AGP 2.0 requires that these power planes be separate. In conjunction with the 4X data rate, the AGP 2.0 interface specification provides for low-voltage (1.5-V) operation. The AGP 2.0 specification implements a TYPEDET# (type detect) signal on the AGP connector, that determines the operating voltage of the AGP 2.0 interface (VDDQ). The motherboard must provide either 1.5 V or 3.3 V to the add-in card, depending on the state of the TYPEDET# signal. (Refer to the following table.) 1.5-V low-voltage operation applies *ONLY* to the AGP interface (VDDQ). VCC is always 3.3 V.

Note: The motherboard provides 3.3 V to the Vcc pins of the AGP connector. If the graphics controller needs a lower voltage, then the add-in card must regulate the 3.3-V Vcc voltage to the controller's requirements. The graphics controller may ONLY power AGP I/O buffers with the VDDQ power pins.

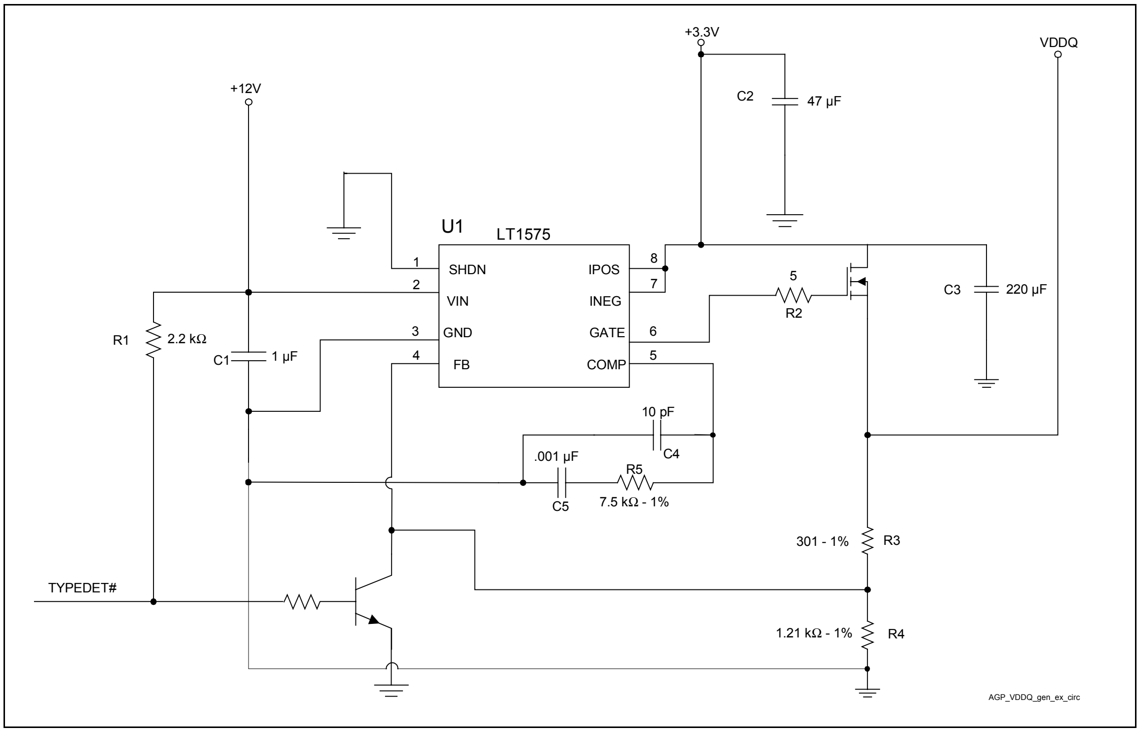
The TYPEDET# signal indicates whether the AGP 2.0 interface operates at 1.5 V or 3.3 V. If TYPEDET# is floating (no connect) on an AGP add-in card, the interface is 3.3 V. If TYPEDET# is shorted to ground, the interface is 1.5 V.

Table 21. TYPDET#/VDDQ Relationship

TYPEDET# (on add-in card)	VDDQ (supplied by MB)
GND	1.5 V
N/C	3.3 V

As a result of this requirement, the motherboard must provide a *flexible* voltage regulator or key the slot to preclude add-in cards with voltage requirements incompatible with the motherboard. This regulator must supply the appropriate voltage to the VDDQ pins on the AGP connector. For specific design recommendations, refer to the schematics in Section 0. VDDQ generation and AGP VREF generation must be considered together. Before developing VDDQ generation circuitry, refer to Section 6.4.1 and the AGP 2.0 interface specification.

Figure 35. AGP VDDQ Generation Example Circuit



The previous figure demonstrates *one* way to design the VDDQ voltage regulator. This regulator is a linear regulator with an external, low-Rds_{on} FET. The source of the FET is connected to 3.3 V. This regulator will convert 3.3 V to 1.5 V or pass 3.3 V, depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3 V (not 5 V) to control thermals (i.e., 5 V regulated down to 1.5 V with a linear regulator will dissipate approximately 7 W at 2 A). Because it must draw power from 3.3 V and, in some situations, must simply pass that 3.3 V to VDDQ (when a 3.3-V add-in card is placed in the system), the regulator MUST use a low-Rds_{on} FET.

AGP 1.0 ECR #44 modified $VDDQ3.3_{min}$ to 3.1 V. Using an ATX power supply, the 3.3 V_{min} is 3.168. Therefore, 68 mV of drop is allowed across the FET at 2 A. This corresponds to a FET with an Rds_{on} of 34 mΩ.

How does the regulator switch? The feedback resistor divider is set to 1.5 V. When a 1.5-V card is placed in the system, the transistor is off and the regulator regulates to 1.5 V. When a 3.3-V card is placed in the system, the transistor is on, and the feedback will be pulled to ground. When this happens, the regulator will drive the gate of the FET to nearly 12 V. This will turn the FET on and pass 3.3 V – 2 A * Rds_{on} to VDDQ.

6.4.2. VREF Generation for AGP 2.0 (2X and 4X)

VREF generation for AGP 2.0 will be different, depending on the AGP card type used. 3.3-V AGP cards will generate VREF locally. That is, they will have a resistor divider on the card that will divide VDDQ down to VREF (refer to the following figure). To account for potential differences between VDDQ and GND at the GMCH and graphics controller, 1.5-V cards use source-generated VREF. That is, the VREF signal is generated at the graphics controller and sent to the GMCH, and another VREF is generated at the GMCH and sent to the graphics controller (refer to the following figure).

Both the graphics controller and the GMCH are required to generate VREF and distribute it through the connector (1.5-V add-in cards only). The following two pins are defined on the AGP 2.0 universal connector to allow this VREF passing:

- VrefGC : VREF from the graphics controller to the chipset
- VrefCG : VREF from the chipset to the graphics controller

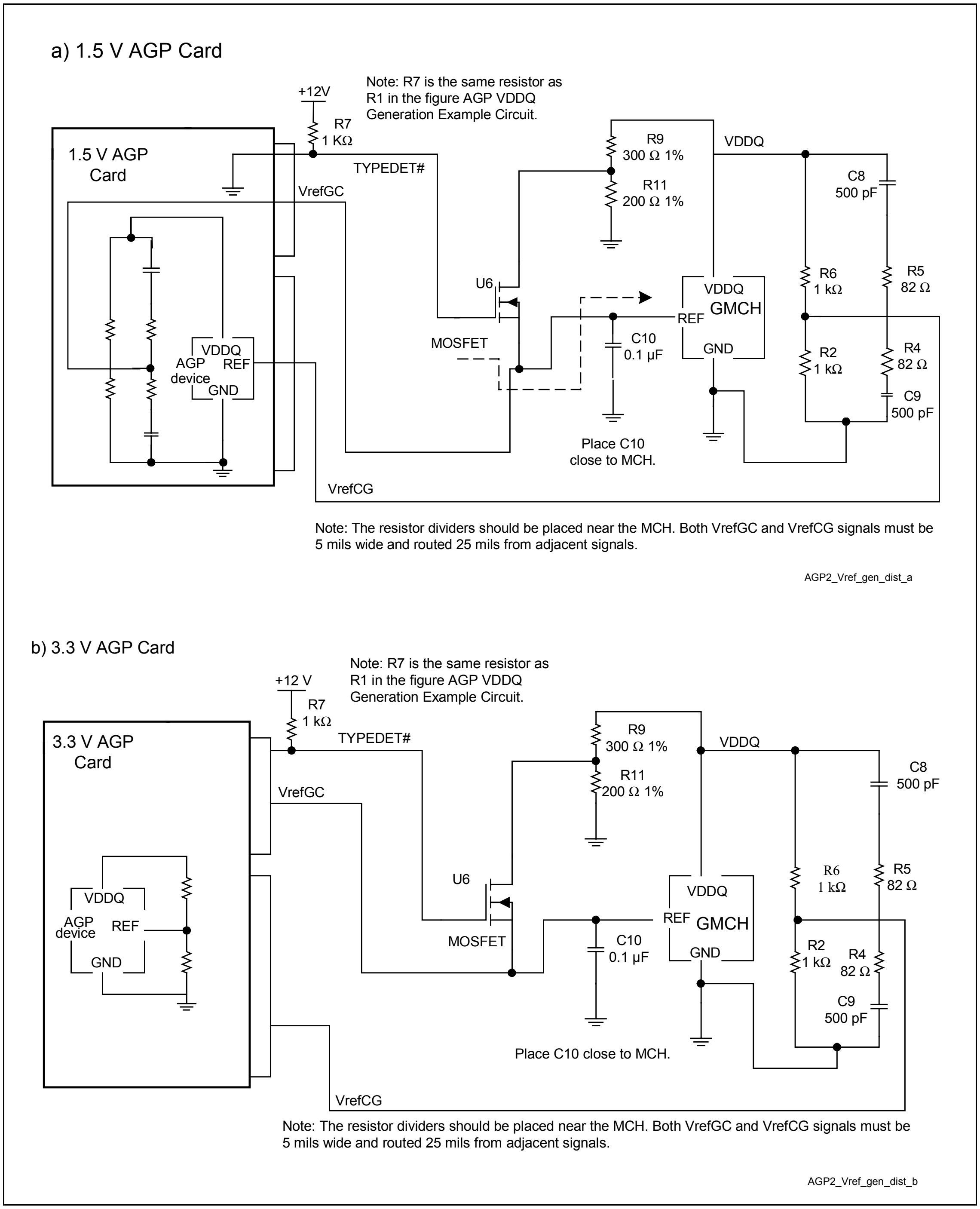
To preserve the common mode relationship between the VREF and data signals, the routing of the two VREF signals must be matched in length to the strobe lines, within 0.5” on the motherboard and within 0.25” on the add-in card.

The voltage divider networks consists of AC and DC elements, as shown in the following figure.

The VREF divider network should be placed as close as practical to the AGP interface, to get the benefit of the common-mode power supply effects. However, the trace spacing around the VREF signals must be a minimum of 25 mils to reduce cross-talk and maintain signal integrity.

During 3.3-V AGP 2.0 operation, VREF must be 0.4 VDDQ. However, during 1.5-V AGP 2.0 operation, VREF must be 0.5 VDDQ. This requires a flexible voltage divider for VREF. There are various methods of accomplishing this. An example of one is shown in the following figure.

Figure 36. AGP 2.0 VREF Generation and Distribution



The flexible VREF divider shown in the previous figure uses an FET switch to switch between the locally generated VREF (for 3.3-V add-in cards) and the source-generated VREF (for 1.5-V add-in cards).

Usage of the source-generated VREF at the receiver is optional and is a product implementation issue beyond the scope of this document.

6.5. Additional AGP Design Guidelines

6.5.1. Compensation

The GMCH AGP interface supports resistive buffer compensation (RCOMP). Tie the GRCOMP pin to a 40-Ω, 2% (or 39-Ω, 1%) pull-down resistor (to ground) via a 10-mil-wide, very short (<0.5") trace.

6.5.2. AGP Pull-ups

AGP control signals require resistors that pull up to VDDQ on the motherboard, to ensure that they contain stable values when no agent is actively driving the bus. The following signals require pull-up resistors:

1X Timing Domain Signals:

- FRAME#
- TRDY#
- IRDY#
- DEVSEL#
- STOP#
- SERR#
- PERR#
- RBF#
- PIPE#
- REQ#
- WBF#
- GNT#
- ST[2:0]

It is critical that these signals be pulled up to VDDQ, not 3.3 V.

The trace stub to the pull-up resistor on 1X timing domain signals should be kept at less than 0.5", to avoid signal reflections from the stub.

The strobe signals require pull-ups/pull-downs on the motherboard to ensure that they contain stable values when no agent is driving the bus.

Note: **INTA# and INTB# should be pulled to 3.3 V, not VDDQ.**

2X/4X Timing Domain Signals:

- AD_STB[1:0] (pull up to VDDQ)
- SB_STB (pull up to VDDQ)
- AD_STB[1:0]# (pull down to ground)
- SB_STB# (pull down to ground)

The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept to less than 0.1", to avoid signal reflections from the stub.

The pull-up/pull-down resistor value requirements are Rmin = 4 kΩ and Rmax = 16 kΩ. The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

6.5.2.1. AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3-V tolerant during 1.5-V operation:

- PME#
- INTA#
- INTB#
- GPERR#
- GSERR#
- CLK
- RST

The following signals on the AGP interface are 5-V tolerant (refer to the USB specification):

- USB+
- USB-
- OVRCNT#

The following special AGP signal is either GROUNDED or NOT CONNECTED on an AGP card.

- TYPEDET#

All other signals on the AGP interface are in the VDDQ group. They are not 3.3-V tolerant during 1.5-V AGP operation!

6.6. Motherboard / Add-in Card Interoperability

There are three AGP connectors: *3.3-V AGP connector, 1.5-V AGP connector*, and *Universal AGP connector*. To maximize add-in flexibility, it is highly advisable to implement the universal connector in an Intel 815 chipset-based system. All add-in cards are *either* 3.3-V or 1.5-V cards. 4X transfers at 3.3 V are not allowed due to timings.

Table 22. Connector/Add-in Card Interoperability

	1.5-V Connector	3.3-V Connector	Universal Connector
1.5-V Card	✔	NO	✔
3.3-V Card	NO	✔	✔

Table 23. Voltage/Data Rate Interoperability

	1X	2X	4X
1.5-V VDDQ	✔	✔	✔
3.3-V VDDQ	✔	✔	NO

6.7. AGP / Display Cache Shared Interface

As described previously, the AGP and display cache interfaces of Intel 815 chipset are multiplexed or shared. In other words, the same component pins (balls) are used for both interfaces, although obviously only one interface can be supported at any given time. As a result, almost all display cache interface signals are mapped onto the new AGP interface. The Intel 815 chipset can be configured in either AGP mode or Graphics mode. In the AGP mode, the interface supports a full AGP 4X interface. In the Graphics mode, the interface becomes a display cache interface similar to the Intel 810E chipset. Note, however, that in the Graphics mode, the display cache is optional. No SDRAM devices have to be connected to the interface. The only dedicated display cache signals are OCLK and RCLK, which need not connect directly to the SDRAM devices. These are not mapped onto existing AGP signals.

6.7.1. AIMM Card Considerations

To support the fullest flexibility, a display cache exists on an add-in card (AGP In-Line Memory Module, or AIMM) that complies with the AGP connector form factor. If the motherboard designer follows the flexible routing guidelines for the AGP interface, which were detailed in previous sections, the customer can choose to populate the AGP slot in an Intel 815 chipset system with either an AGP Graphics card with an AIMM card to enable the highest-possible internal graphics performance, or with nothing to obtain the lowest-cost internal graphics solution. Some AIMM/Intel 815 chipset interfacing implications are as follows. For a complete description of the AIMM card design, refer to the *AGP Inline Memory Module Specification*, which is available from Intel.

- A strap is required to determine which frequency to select for display cache operation. This is the L_FSEL pin of the GMCH. The AIMM card will pull this signal up or down, as appropriate to communicate to the Intel 815 chipset the appropriate operating frequency. The Intel 815 chipset will sample this pin on the deasserting edge of reset.
- Since current SDRAM technology is always 3.3 V rather than the 1.5-V option also supported by AGP, the AIMM card should set the TYPEDET# signal correctly so as to indicate that it requires a 3.3-V power supply. Furthermore, the AIMM card should have only the 3.3-V key and not the 1.5-V key, thereby preventing it from being inserted into a 1.5-V-only connector.
- The pad buffers on the chip will be the normal AGP buffers and will work for both interfaces.
- In internal graphics mode, the AGPREF signal, which is required for the AGP mode, should remain functional as a reference voltage for sampling 3.3-V LMD inputs. The voltage level on AGPREF should remain exactly the same as in the AGP mode (as opposed to VCC/2, which was used for previous products).

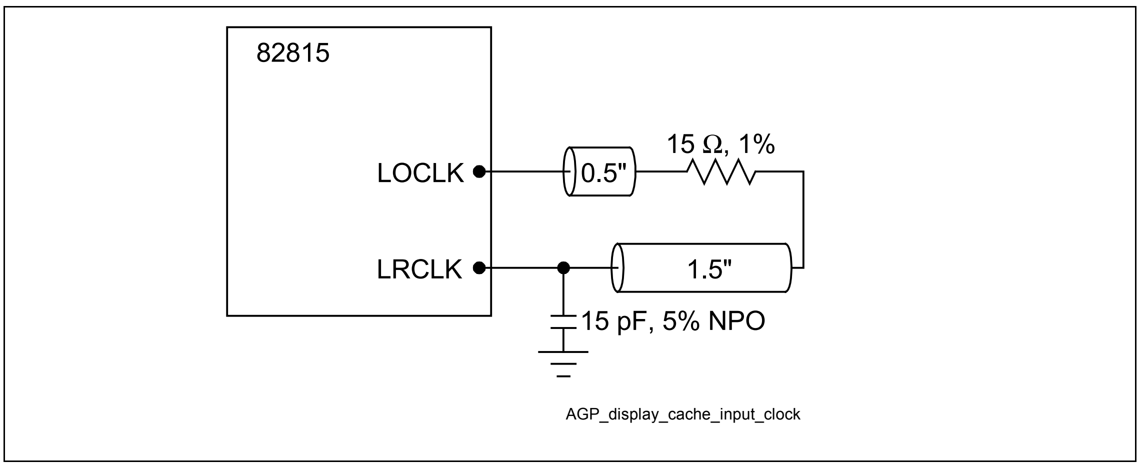
6.7.1.1. AGP and AIMM Mechanical Considerations

The AIMM card will be designed with a notch on the PCB to go around the AGP universal retention mechanism. To guarantee that the AIMM card will meet all shock and vibration requirements of the system, the AGP universal retention mechanism will be required on all AGP sockets that will support an AIMM card.

6.7.2. Display Cache Clocking

The display cache is clocked source synchronously from a clock generated by the GMCH. The display cache clocking scheme uses three clock signals: LTCLK clocks the SDRAM devices and is muxed with an AGP signal and should be routed according to the flexible AGP guidelines. LOCLK and LRCLK clock the input buffers of the Intel 815 chipset. LOCLK is an output of the GMCH and is a buffered copy of LTCLK. LOCLK should be connected to LRCLK at the GMCH with a length of PCB trace, to create the appropriate clock skew relationship between the Intel 815 chipset clock input (LRCLK) and the SDRAM capacitor clock input(s). The guidelines are illustrated in the following figure.

Figure 37. Intel® 815 Chipset Display Cache Input Clocking



The capacitor should be placed as close as possible to the GMCH LRCLK pin. To minimize skew variation, we recommend a 1% series termination resistor, and a 5% NPO capacitor (to stabilize the value across temperatures). In addition to the 15-Ω, 1% resistor and 15-pF, 5% NPO capacitor, the following combination also can be used: 10-Ω 1% resistor and 22-pF, 5% NPO.

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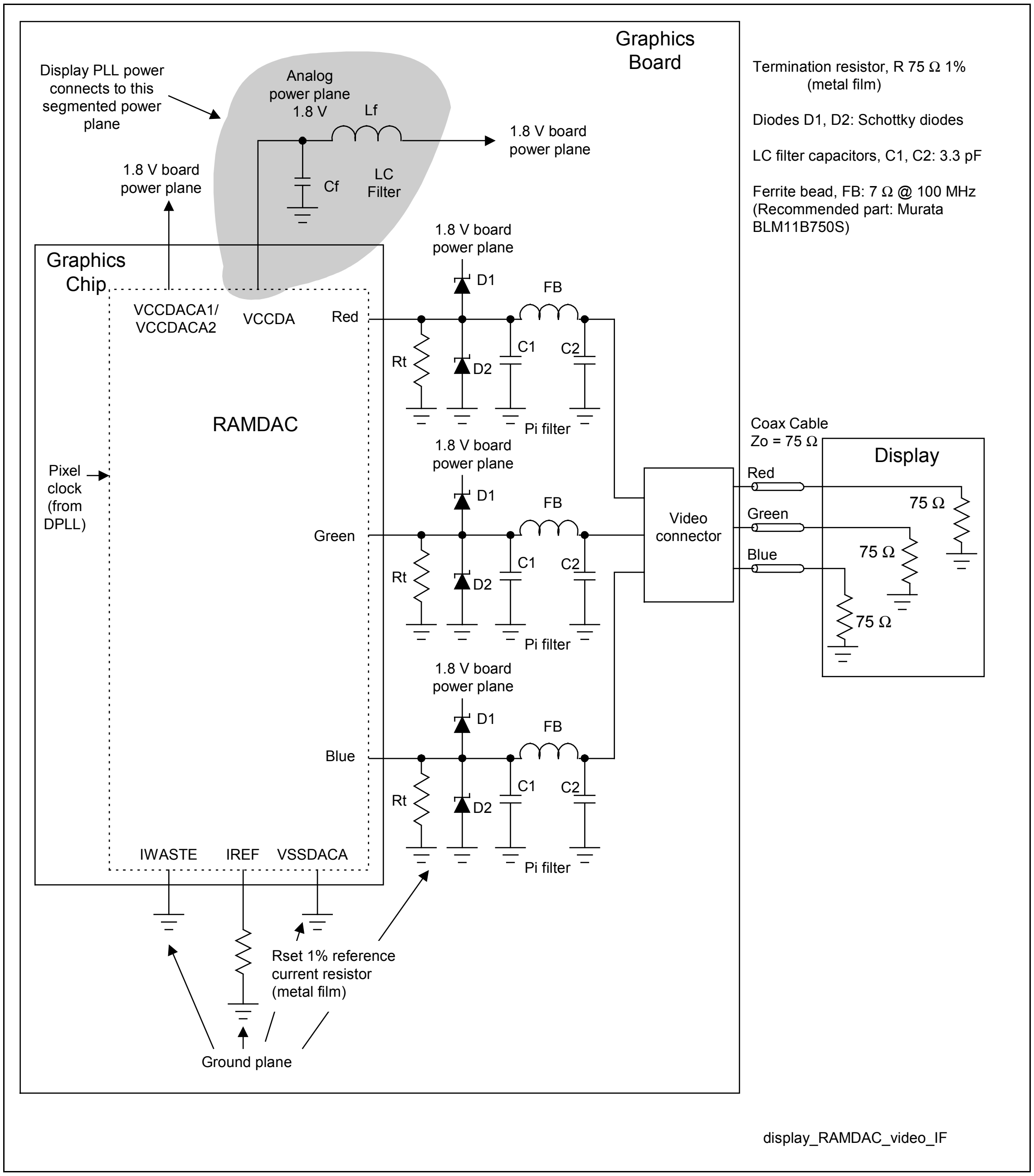
7. Integrated Graphics Display Output

7.1. Analog RGB/CRT

7.1.1. RAMDAC/Display Interface

The following figure shows the interface of the RAMDAC analog current outputs with the display. Each DAC output is doubly terminated with a 75-Ω resistance: One 75-Ω resistance is from the DAC output to the board ground, and the other termination resistance exists within the display. The equivalent DC resistance at the output of each DAC output is 37.5 Ω. The current output from each DAC flows into this equivalent resistive load to produce a video voltage, without the need for external buffering. There is also an LC pi-filter that is used to reduce high-frequency glitches and noise and to reduce EMI. To maximize the performance, the filter impedance, cable impedance, and load impedance should be the same. The LC pi-filter consists of two 3.3-pF capacitors and a ferrite bead with a 75-Ω impedance at 100 MHz. The LC pi-filter is designed to filter glitches produced by the RAMDAC, while maintaining adequate edge rates to support high-end display resolutions.

Figure 38. Schematic of RAMDAC Video Interface



Note: Diodes D_1, D_2 are clamping diodes with low leakage and low capacitive loading. An example is: California Micro Devices PAC DN006 (6 channel ESD protection array).

In addition to the termination resistance and LC pi-filter, there are protection diodes connected to the RAMDAC outputs to help prevent latch-up. The protection diodes must be connected to the same power supply rails as the RAMDAC. An LC filter is recommended to connect the segmented analog 1.8-V power plane of the RAMDAC to the 1.8-V board power plane. The LC filter should be designed for a cut-off frequency of 100 kHz.

7.1.2. Reference Resistor (Rset) Calculation

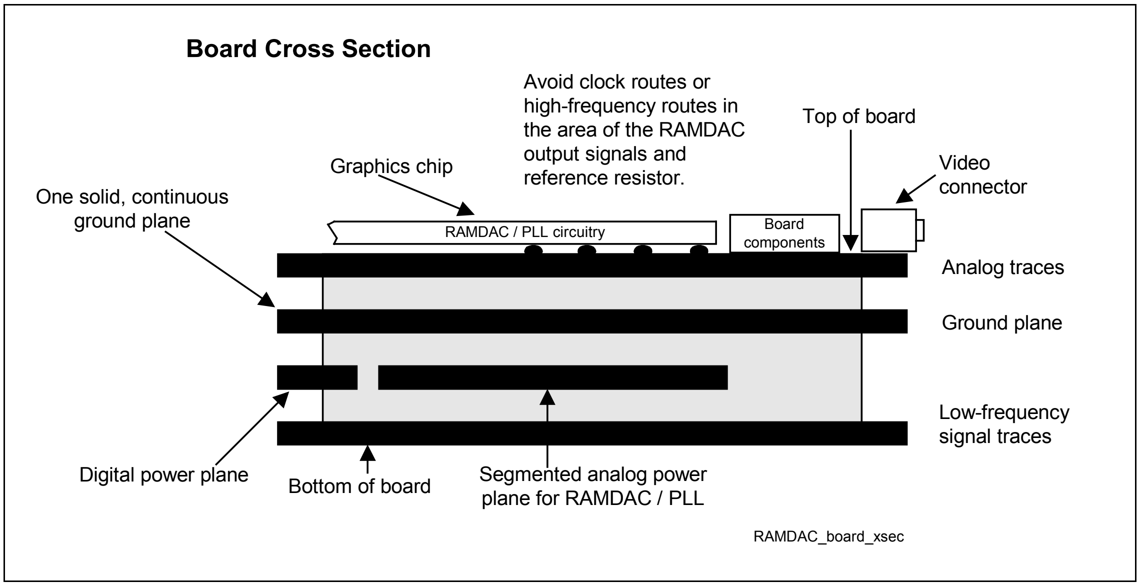
The full-swing video output is designed to be 0.7 V, according to the VESA video standard. With an equivalent DC resistance of 37.5 Ω (two 75-Ω in parallel; one 75-Ω termination on the board and one 75-Ω termination within the display), the full-scale output current of a RAMDAC channel is 0.7/37.5 Ω = 18.67 mA. Since the RAMDAC is an 8-bit current-steering DAC, this full-scale current is equivalent to 255 I, where I is a unit current. Therefore, the unit current or LSB current of the DAC signals equals 73.2 µA. The reference circuitry generates a voltage across this R_{set} resistor equal to the bandgap voltage divided by three (407.6 mV). The RAMDAC reference current generation circuitry is designed to generate a 32-I reference current using the reference voltage and the R_{set} value. To generate a 32-I reference current for the RAMDAC, the reference current setting resistor, R_{set}, is calculated using the following equation:

$$R_{set} = V_{REF} / 32\ I = 0.4076\ V / 32*73.2\ \mu A = 174\ \Omega$$

7.1.3. RAMDAC Board Design Guidelines

The following figure shows a general cross-section of a typical four-layer board. The recommended RAMDAC routing for a four-layer board is such that the red, green, and blue video outputs are routed on the top (bottom) layer over (under) a solid ground plane, to maximize the noise rejection characteristics of the video outputs. It is essential to prevent toggling signals from being routed next to the video output signals to the VGA connector. A 20-mil spacing between any video route and any other routes is recommended.

Figure 39. Cross-Sectional View of a Four-Layer Board

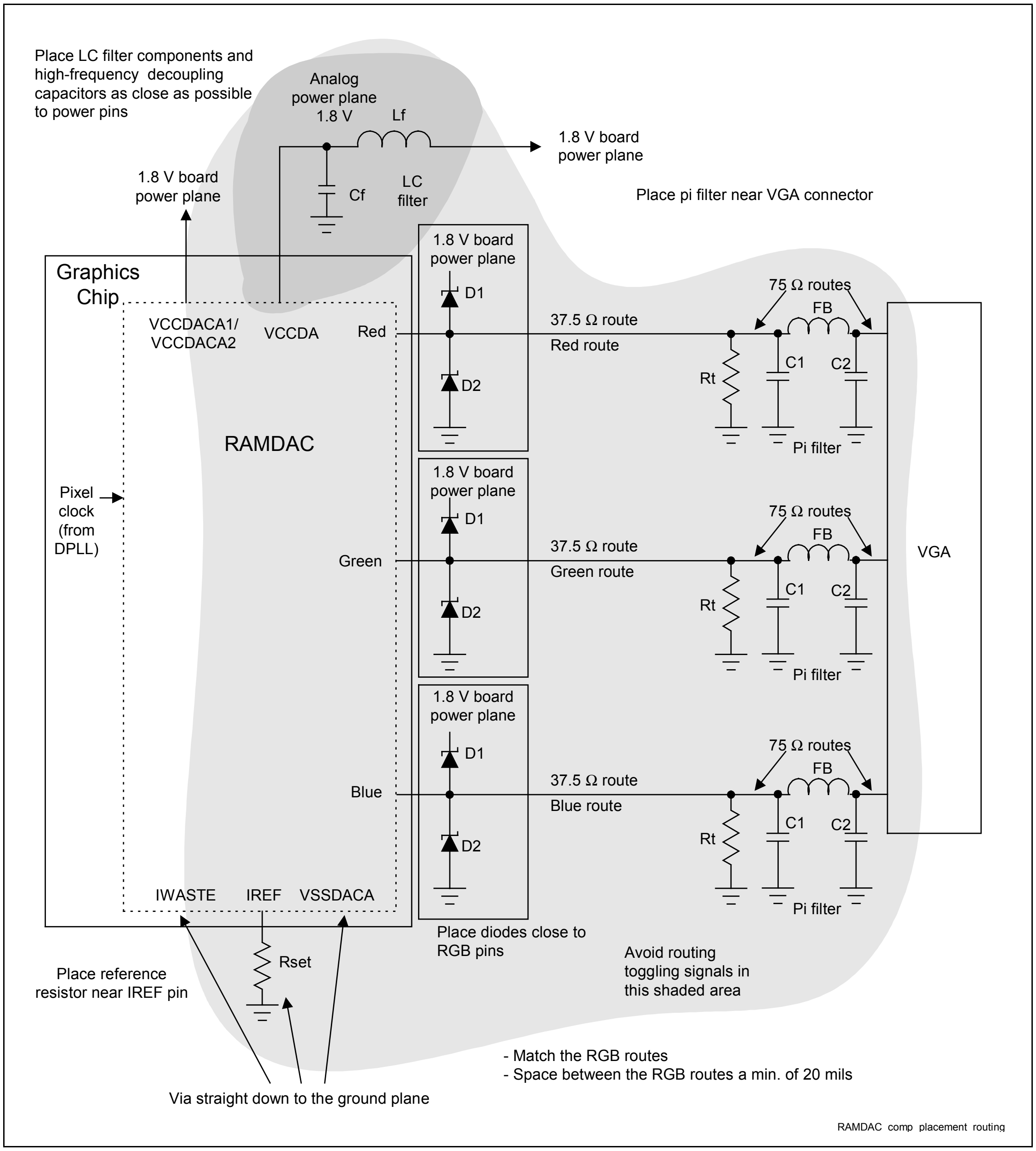


Matching the video routes (red, green, blue) from the RAMDAC to the VGA connector also is essential. The routing for these signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends and jogs).

The following figure shows the recommended RAMDAC component placement and routing. The termination resistance can be placed anywhere along the video route from the RAMDAC output to the

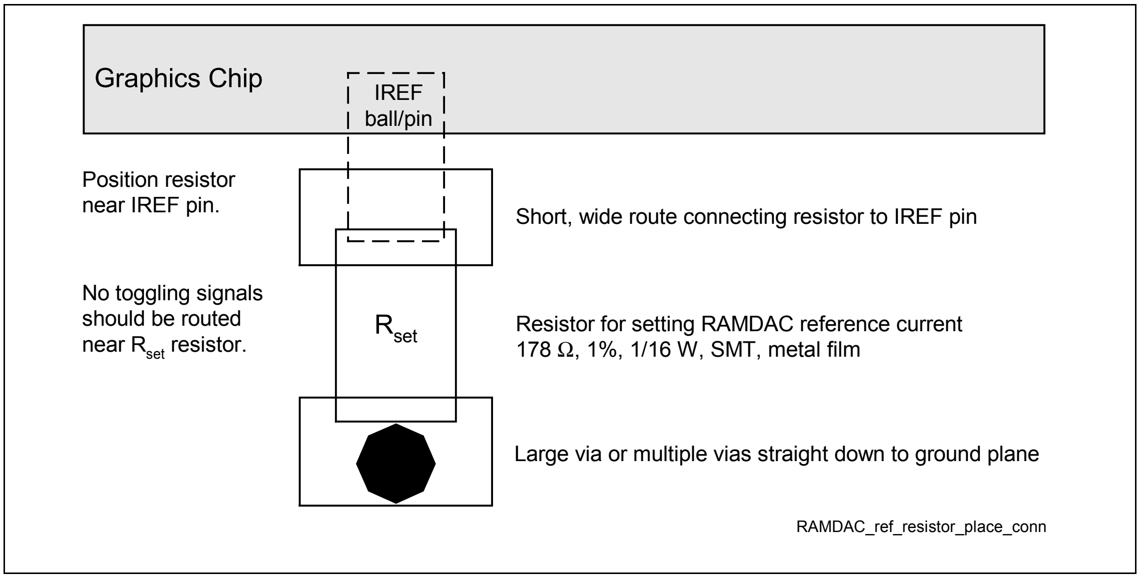
VGA connector, as long as the impedance of the traces is designed as indicated in the following figure. It is recommended that the pi-filters be placed in close proximity to the VGA connector, to maximize EMI filtering effectiveness. It is recommended that the LC filter components for the RAMDAC/PLL power plane, decoupling capacitors, latch-up protection diodes, and reference resistor be placed in close proximity to the respective pins. Figure 41 shows the recommended reference resistor placement and ground connections.

Figure 40. Recommended RAMDAC Component Placement & Routing



Note: Diodes D_1, D_2 are clamping diodes with low leakage and low capacitive loading. An example is: California Micro Devices PAC DN006 (6 channel ESD protection array).

Figure 41. Recommended RAMDAC Reference Resistor Placement and Connections



7.1.4. HSYNC/VSYNC Output Guidelines

The Hsync and Vsync output of the 82815 GMCH may exhibit up to 1.26V P-P noise when driven high under high traffic system memory conditions. To minimize this, the following is required.

Add External Buffers to Hsync and Vsync. Examples include: Series 10 Ohm resistor with a 74LVC08

7.2. Digital Video Out

The Intel® Digital Video Out (DVO) port is a scaleable, low-interface port that ranges from 1.1 V to 1.8 V. This Intel DVO port interfaces with a discrete TV encoder to enable platform support for TV-Out, with a discrete TMDS transmitter to enable platform support for DVI-compliant digital displays, or with an integrated TV encoder and TMDS transmitter.

The GMCH DVO port controls the video front-end devices via an I2C interface, by using the LTVDA and LTVCK pins. I^2C is a two-wire communications bus/protocol. The protocol and bus are used to collect EDID (Extended Display Identification) from a digital display panel and to detect and configure registers in the TV encoder or TMDS transmitter chips.

7.2.1. DVO Interface Routing Guidelines

Route data signals (LTVDATA[11:0]) with a trace width of *5* mils and a trace spacing of *20* mils. These signals can be routed with a trace width of *5* and a trace spacing of *15* for navigation around components or mounting holes. To break out of the GMCH, the DVO data signals can be routed with a trace width of *5* and a trace spacing of *5*. The signals should be separated to a trace width of *5* and a trace spacing of *20* within 0.3” of the GMCH component. The maximum trace length for the DVO data signals is 7”. These signals should each be matched within ±0.1” of the LTVCLKOUT[1] and LTVCLKOUT[0] signals.

Route the LTVCLKOUT[1:0] signals 5 mils wide and 20 mils apart. This signal pair should be a minimum of 20 mils from any adjacent signals. The maximum length for LTVCLKOUT[1:0] is 7”, and the two signals should be the same length.

7.2.2. DVO I^2C Interface Considerations

LTVDA and LTVCK should be connected to the TMDS transmitter, TV encoder or integrated TMDS transmitter/TV encoder device, as required by the specifications for those devices. LTVDA and LTVCK should also be connected to the DVI connector, as specified by the DVI specification. 4.7-kΩ pull-ups (or pull-ups with the appropriate value derived from simulation) are required on each of LTVDA and LTVCK.

7.2.3. Leaving the Intel® 815 Chipset DVO Port Unconnected

If the motherboard does not implement any of the possible video devices with the Intel 815 chipset’s DVO port, the following are recommended on the motherboard:

- Pull-up LTVDA and LTVCK with 4.7-kΩ resistors at the GMCH. This will prevent the Intel 815 chipset DVO controller from confusing noise on these lines for false I^2C cycles.
- Route LTVDATA[11:0] and LTVCLKOUT[1:0] out of the BGA to test points for use by automated test equipment (if required). These signals are part of one of the GMCH XOR chains.

8. Hub Interface

The 82815 GMCH ball assignment and 82801AA ICH ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals be routed directly from the GMCH to the ICH on the top signal layer. Refer to the following figure.

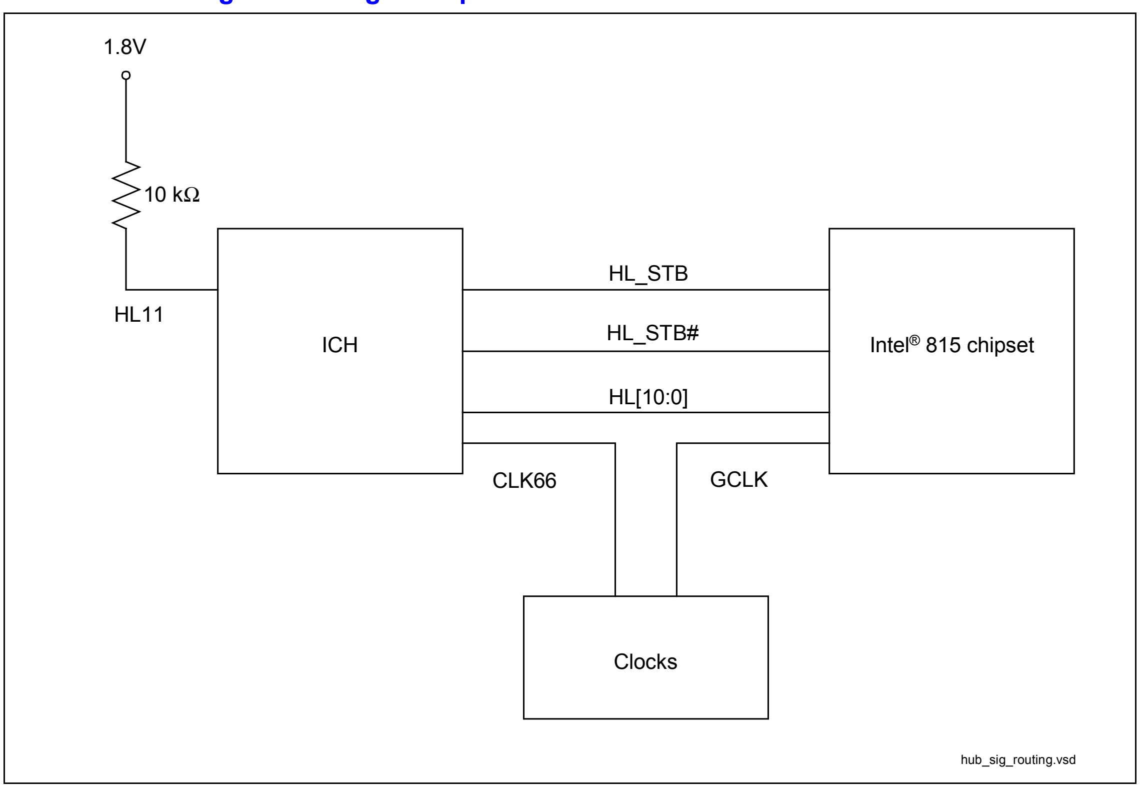
The hub interface is broken into two signal groups: data signals and strobe signals.

- Data Signals:
  - HL[10:0]
- Strobe Signals:
  - HL_STB
  - HL_STB#

Note: HL_STB/HL_STB# is a differential strobe pair.

No pull-ups or pull-downs are required on the hub interface. HL[11] on the ICH should be brought out to a test point for NAND Tree testing. Each signal should be routed such that it meets the guidelines documented for the signal group to which it belongs.

Figure 42. Hub Interface Signal Routing Example



8.1.1. Data Signals

Hub interface data signals should be routed with a trace width of *5* and a trace spacing of *20*. These signals can be routed with a trace width of *5* and a trace spacing of *15* for navigation around components or mounting holes. To break out of the GMCH and the ICH, the hub interface data signals can be routed with a trace width of *5* and a trace spacing of *5*. The signals should be separated to a trace width of *5* and a trace spacing of *20* within 0.3” of the GMCH/ICH components.

The maximum trace length for the hub Interface data signals is 7”. These signals should each be matched within ±0.1” of the HL_STB and HL_STB# signals.

8.1.2. Strobe Signals

Due to their differential nature, the hub Interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signal. The maximum length for the strobe signals is 7”, and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes, within ±0.1”.

8.1.3. HREF Generation/Distribution

HREF is the hub interface reference voltage. It is 0.5 * 1.8 V = 0.9 V ± 2%. It can be generated using a single HREF divider or locally generated dividers (as shown in the following two figures). The resistors should be equal in value and rated at 1% tolerance (to maintain 2% tolerance on 0.9 V). The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from a minimum of 100 Ω to a maximum of 1 kΩ (300 Ω shown in example).

The single HREF divider should not be located more than 4" away from either the GMCH or ICH. If the single HREF divider is located more than 4" away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01-µF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor must be close to the component HREF pin.

Figure 43. Single-Hub-Interface Reference Divider Circuit

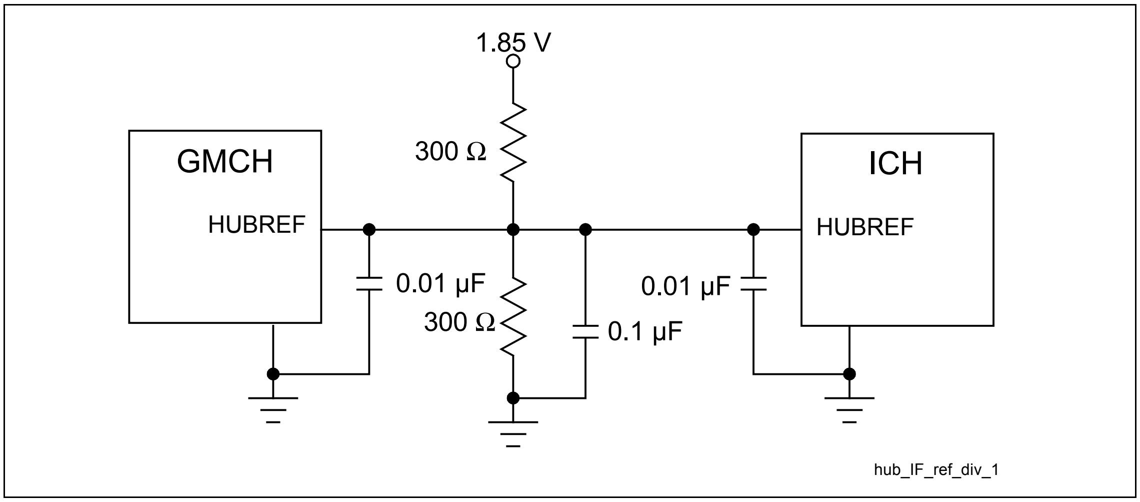
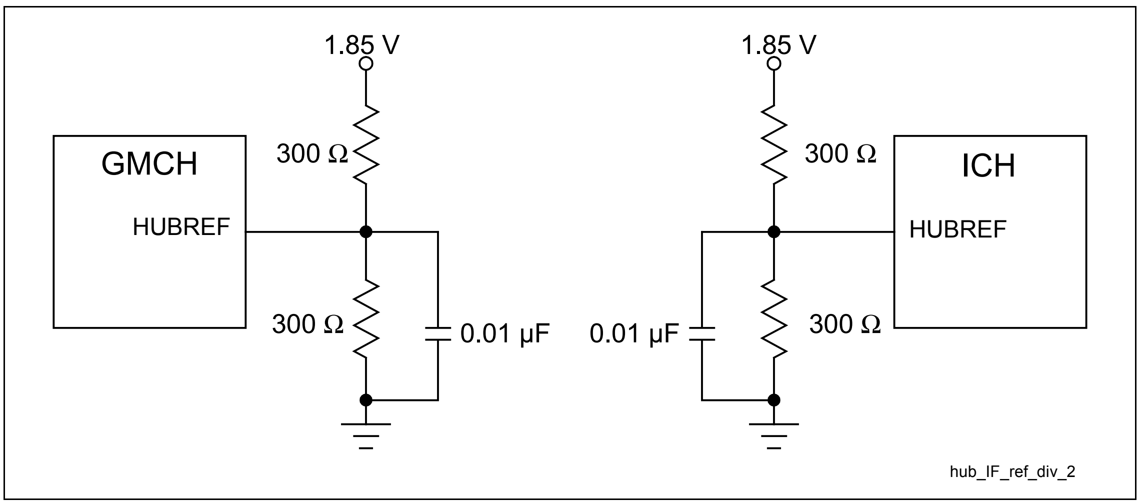


Figure 44. Locally Generated Hub Interface Reference Dividers



8.1.4. Compensation

Independent Hub interface compensation resistors are used by the 82815 GMCH and ICH to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) Datasheet* and the *Intel® 82801AA (ICH) and 82801AB (ICH0) I/O Controller Hub Datasheet* for details on compensation. Resistive compensation (RCOMP) guidelines are as follows:

- **RCOMP:** Tie the HLCOMP pin of each component to a 40-Ω 1% or 2% pull-up resistor (to 1.8 V) via a 10-mil-wide, 0.5" trace (targeted at a nominal trace impedance of 40 Ω). The GMCH and ICH each require their own RCOMP resistor.

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9. I/O Subsystem

9.1. Ultra ATA/66

9.1.1. IDE Routing Guidelines

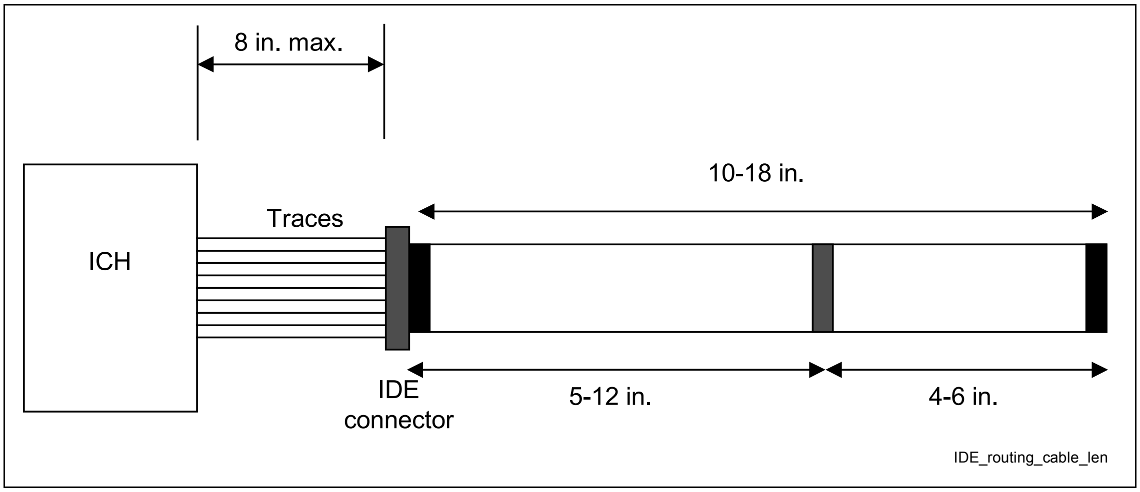
This section contains guidelines for connecting and routing the ICH IDE interface. The ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement and signal termination for both IDE channels. The ICH integrates the series terminating resistors typically required on the IDE data and control signals running to the two ATA connectors.

The IDE interface can be routed with 5-mil traces on 5-mil spaces, and it should be less than 8” long (from ICH to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 1”shorter than the longest IDE signal (on the channel).

Cabling

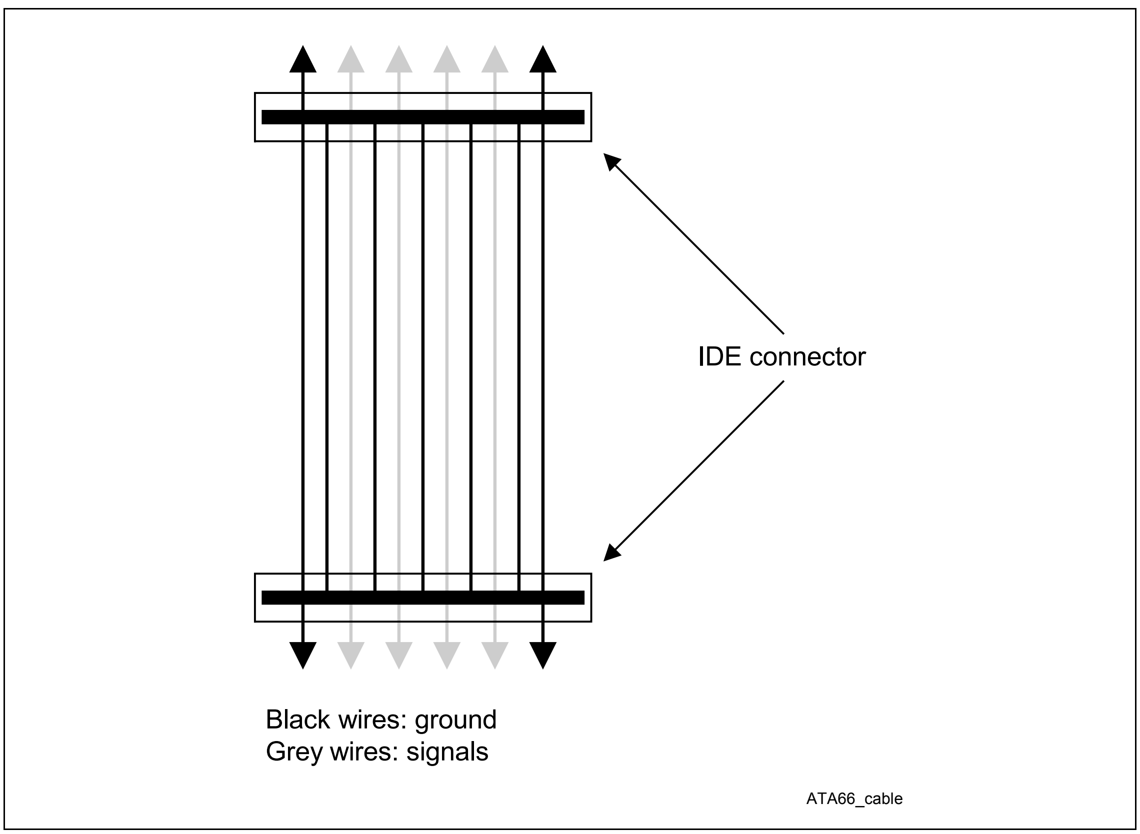
- **Length of Cable:** Each IDE cable should be ≤18”.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6” between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the connector next closest to the end of the cable (6” away from the end of the cable).
- **Grounding:** Provide a direct low-impedance chassis path between the motherboard ground and hard disk drives.
- **Ultra ATA/66:** Ultra ATA/66 requires the use of an 80-conductor cable.
- **ICH Placement:** The ICH should be placed within 8” of the ATA connector.
- **PC99 Requirement:** Support of Cable Select for master-slave configuration is a system design requirement for Microsoft PC99. The CSEL signal needs to be pulled down at the host side by means of a 470-Ω pull-down resistor for each ATA connector.

Figure 45. IDE Min./Max. Routing and Cable Lengths



The new IDE cable required for Ultra ATA/66 is an 80-conductor cable. However, the 40-pin connectors do not change. The wires in the cable alternate as follows: ground, signal, ground, signal,…. All ground wires are tied together on the cable (and they are tied to ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*, which can be obtained from the Small Form Factor Committee.

Figure 46. Ultra ATA/66 Cable



Motherboard

- **ICH Placement:** The ICH should be placed within 8” of the ATA connector(s). There are no minimum length requirements for this spacing.
- **Capacitance:** The capacitance of each pin of the IDE connector on the host should be less than 25 pF when the cables are disconnected from the host.
- **Series Termination:** There is no need for series termination resistors on the data and control signals, since series termination is integrated into these signal lines on the ICH.
- A 1-kΩ pull-up to 5 V is required on PIORDY and SIORDY.
- A 470-Ω pull-down is required on pin 28 of each connector.
- A 5.6-kΩ pull-down is required on PDREQ and SDREQ.
- Support Cable Select (CSEL) is a PC99 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
- The primary IDE connector uses IRQ14, and the secondary IDE connector uses IRQ15.
- IRQ14 and IRQ15 each require an 8.2-kΩ pull-up resistor to VCC.
- Due to the elimination of the ISA bus from the ICH, PCI_RST# should be connected to pin 1 of the IDE connectors as the IDE reset signal. Because of high loading, the PCI_RST# signal should be buffered.
- There is no internal pull up or down on PDD7 or SDD7 of the ICH. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10-kΩ pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up (as required by the ATA-4 specification).
- If no IDE is implemented with the ICH, the input signals (xDREQ and xIORDY) can be grounded and the output signals can be left as no connects.

Figure 47. Resistor Schematic for Primary IDE Connectors

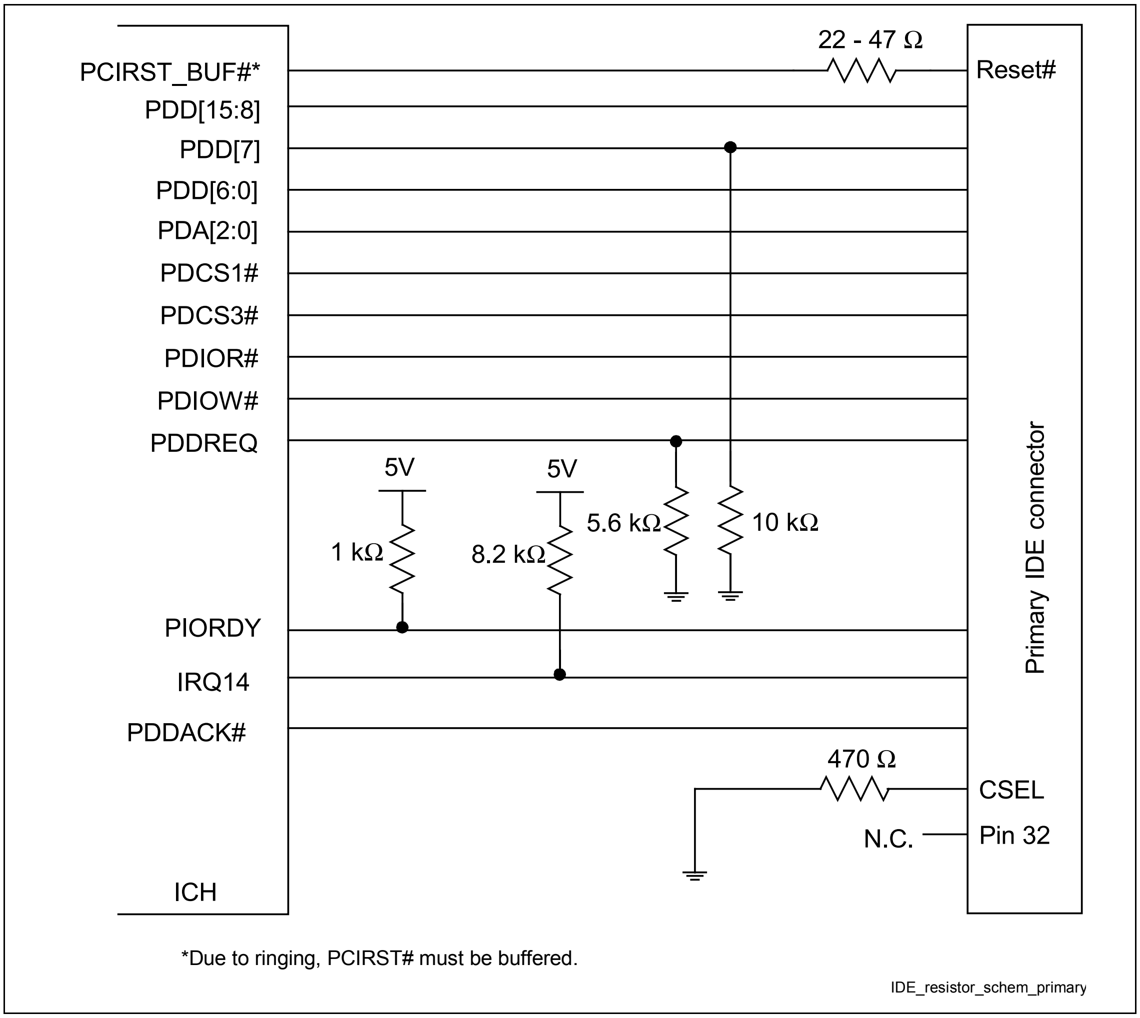
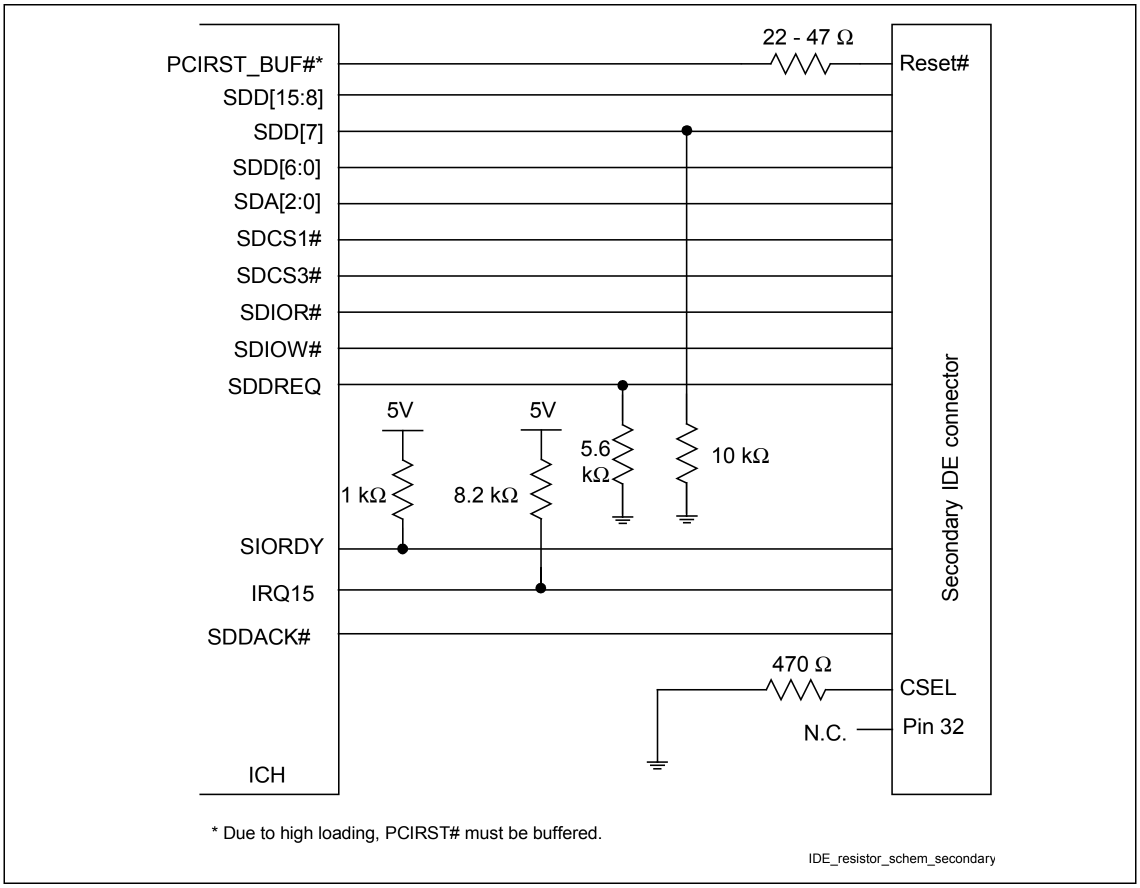


Figure 48. Resistor Schematic for Secondary IDE Connectors



9.1.2. Ultra ATA/66 Detection

The ATA/66 cable is an 80-conductor cable. However, the 40-pin connectors used on motherboards for 40-conductor cables do not change as a result of this new cable. The wires in the cable alternate as follows: ground, signal, ground, signal…. All ground wires are tied together at the connectors on the cable (and they are tied to ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*, which can be obtained from the Small Form Factor Committee.

To determine whether the ATA/66 mode can be enabled, the chipset using the ICH requires the system BIOS to attempt to determine the type of cable used in the system. The BIOS does this in one of two ways:

1. Host-side detection
2. Device-side detection

If the BIOS detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the ICH and the IDE device. Otherwise, the BIOS can only enable modes that do not require an 80-conductor cable (example: Ultra ATA/33 Mode).

After determining the Ultra DMA mode to be used, the BIOS configures the chipset hardware and software to match the selected mode.

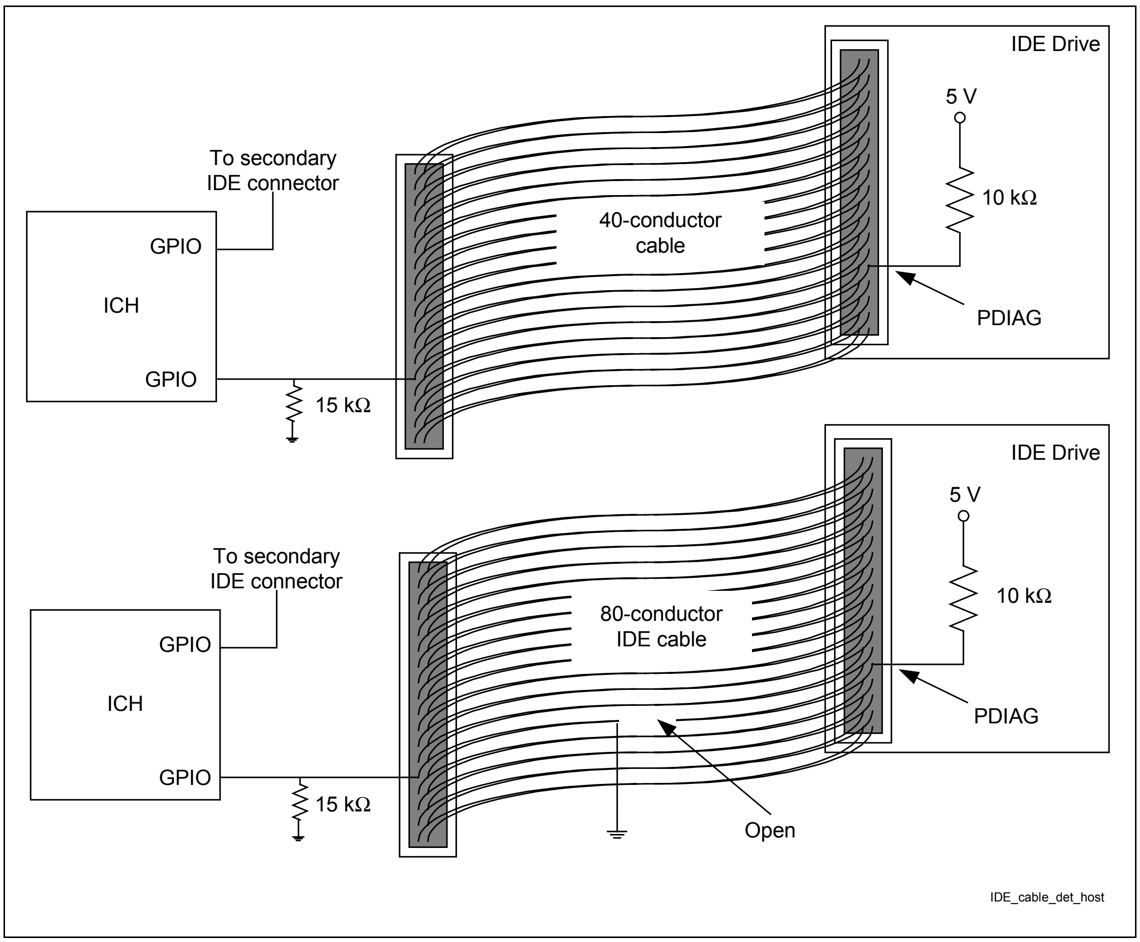
9.1.3. Ultra ATA/66 Motherboard Guidelines

The chipset (using the ICH) can use two methods to detect the cable type. Each mode requires a different motherboard layout.

Host-Side Detection: BIOS Detects Cable Type Using GPIOs

Host-side detection requires the use of two GPI pins (one per IDE controller). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in the following figure. All Ultra ATA/66 devices have a 10-kΩ pull-up resistor to 5 V. Most GPIO pins on the ICH and all GPIs on the FWH are not 5-V tolerant. This requires a resistor divider so that 5 V will not be driven to the ICH or FWH pins. The proper value of the series resistor is 15 kΩ (as shown in the following figure). This creates a 10-kΩ/15-kΩ resistor divider and will produce approximately 3 V for a logic high. This mechanism allows the host to sample PDIAG#/CBLID#, after diagnostics. If PDIAG#/CBLIB# is high, then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG#/CBLID# is low, then there is an 80-conductor cable in the system.

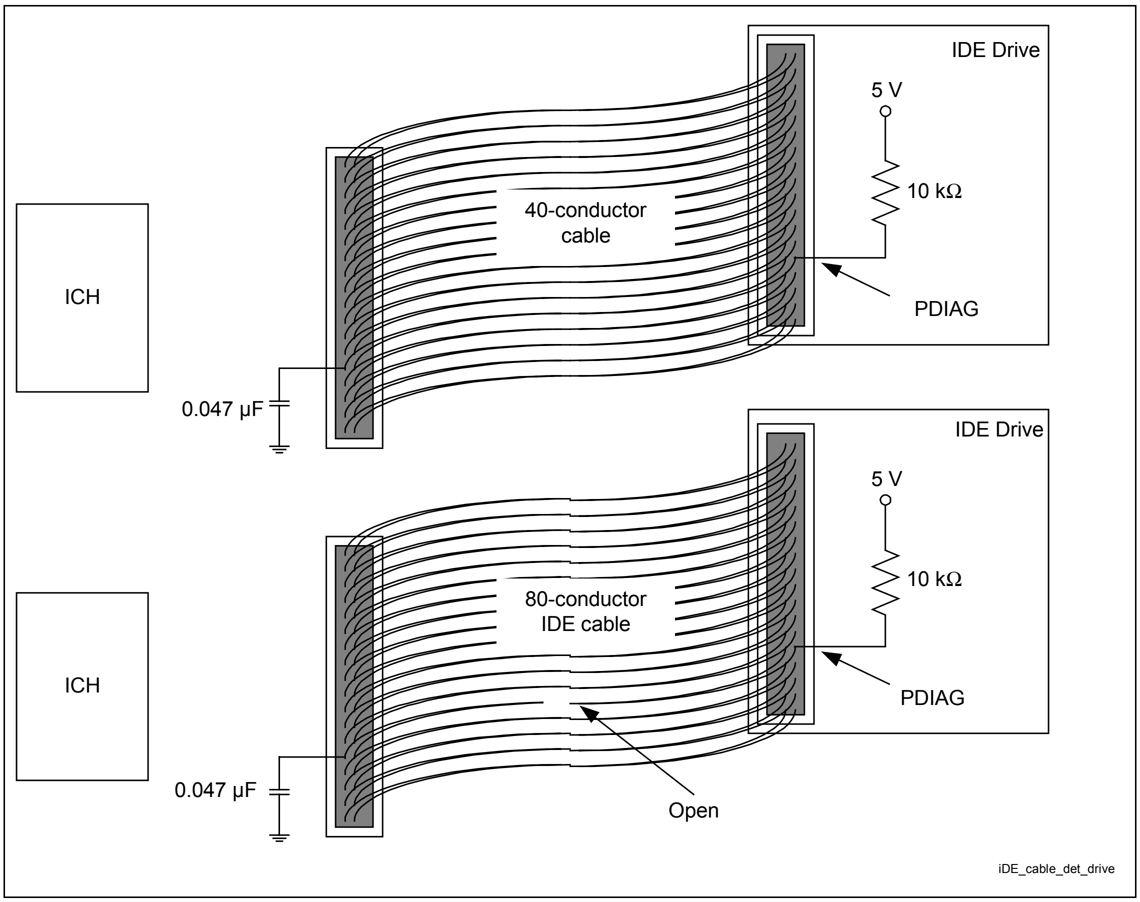
Figure 49. Host-Side IDE Cable Detection



Drive-Side Detection: BIOS Queries IDE Drive for Cable Type

Drive-side detection requires only a 0.047-µF capacitor on the motherboard, as shown in the following figure. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10-kΩ resistor). The drive will sample the PDIAG# signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through, and therefore the capacitor has no effect. In a 40-conductor cable, PDIAG#/CBLID# is connected though to the drive. Therefore the signal will rise more slowly. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot, as described in the ATA/66 specification.

Figure 50. Drive-Side IDE Cable Detection



Layout for BOTH *Host-Side* and *Drive-Side* Cable Detection

It is possible to lay out for both host-side and drive-side cable detection and decide the method to be used during assembly. The following figure shows the layout that allows for both host-side and drive-side detection.

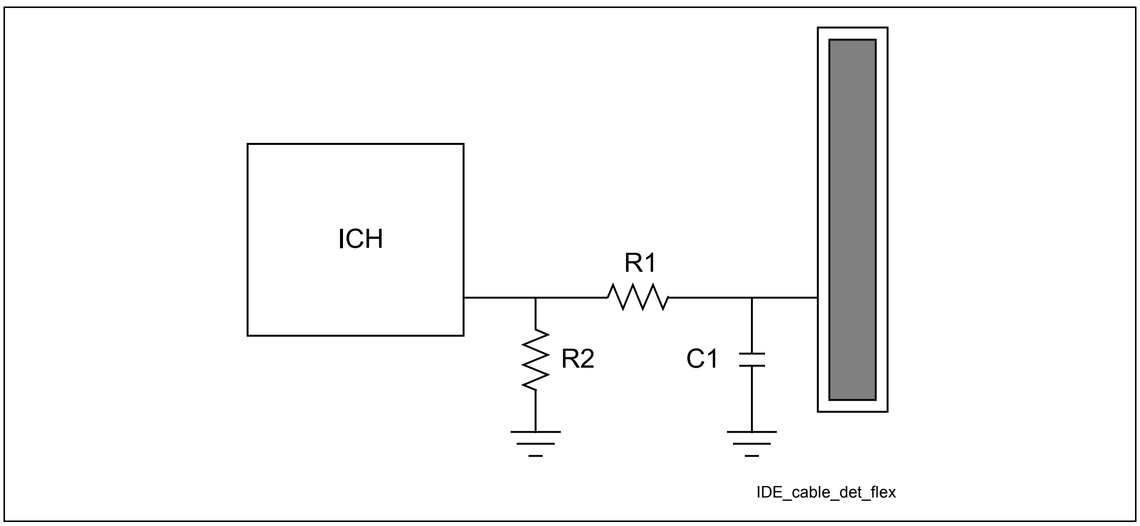
For Host-Side Detection:

- R1 is a 0-Ω resistor.
- R2 is a 15-kΩ resistor.
- C1 is not stuffed.

For Drive-Side Detection:

- R1 is not stuffed.
- R2 is not stuffed.
- C1 is a 0.047-µF capacitor.

Figure 51. Flexible IDE Cable Detection



9.2. AC’97

The ICH implements an AC’97 2.1-compliant digital controller. Any codec attached to the ICH AC-link should be AC’97 2.1 compliant as well. Contact your preferred codec vendor for information on AC’97 2.1-compliant products. The AC’97 2.1 specification is available on the Intel website at the following web page:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The ICH supports the codec combinations listed in the following table.

Table 24. AC’97 Configuration Combinations

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in the table, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC may not be present.

9.2.1. Communications and Networking Riser

Intel has developed a common connector specification known as the Communications and Networking Riser (CNR). This specification defines a mechanism that enables OEM plug-in card options.

The CNR specification provides a mechanism for placing AC’97 codecs on a riser card. This is important for modem codecs, as it facilitates international certification of the modem.

The CNR specification replaces the Audio/Modem Riser specification (AMR).

9.2.2. AC’97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05” wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25” to 0.5” wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05” wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576-MHz crystal or oscillator. Refer to the primary codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288-MHz clock driven by the primary codec to the digital controller (ICH) and by any other codec present. The clock is used as the time base for latching and driving data.

The ICH supports wake-on-ring from S1-S4 via the AC’97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

If no codec is attached to the link, internal pull-downs will prevent the inputs from floating. Therefore, external resistors are not required.

9.2.3. AC’97 Signal Quality Requirements

In a lightly loaded system (e.g., single codec down), AC'97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC'97 2.1 specification, with the specified load of 50 pF.

9.2.4. Motherboard Implementation

The following design considerations are provided for the implementation of an ICH platform using AC’97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH platform.

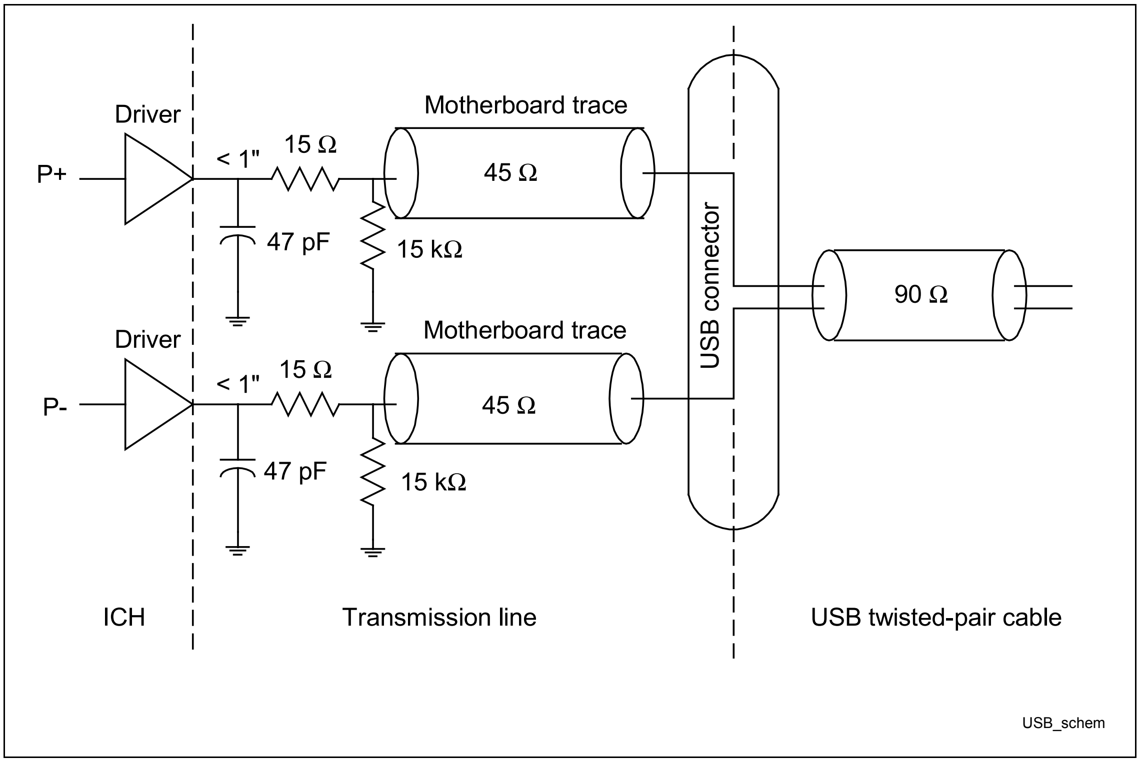
- Codec Implementation
  - Any valid combination of codecs may be implemented on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on a CNR module. However, nothing precludes a modem codec on the motherboard.
  - Only one primary codec may be present on the link. A maximum of two codecs can be supported in an ICH platform.
  - Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
  - The ICH supports wake-on-ring from S1-S4 states via the AC’97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required. The ICH does not wake from the S5 state via the AC’97 link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active. Rather, they should be pulled to ground through a weak (approximately 10-kΩ) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH’s internal pull-down resistors are enabled, so there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that might not be connected to a codec*. For example, if a dedicated audio codec is on the motherboard and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. However, if the SDATAIN signal has no codec connected or is connected to an on-board codec that can be hardware-disabled, then the signal should have an external pull-down resistor to ground.
- The ICH provides internal weak pull-downs. Therefore the motherboard does not need to provide discrete pull-down resistors.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

9.3. USB

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15-kΩ pull-down resistors on both P+/P- data lines.
- 15-Ω series resistors should be placed as close as possible to the ICH (<1”). These series resistors provide source termination of the reflected signal.
- 47-pF caps must be placed as close as possible to the ICH as well as on the ICH side of the series resistors on the USB data lines (P0±, P1±). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15-kΩ±5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±). They provide the signal termination required by the USB specification. The stub should be as short as possible.
- The trace impedance for the P0± and P1± signals should be 45 Ω (to ground) for each USB signal P+ or P-. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 3. The impedance is 90 Ω between the differential signal pairs P+ and P-, to match the 90-Ω USB twisted-pair cable impedance. Note that the twisted-pair characteristic impedance of 90 Ω is the series impedance of both wires, which results in an individual wire presenting a 45-Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as ‘critical signals’ (i.e., hand-routing preferred). The P+/P- signal pair should be routed together and not parallel to other signal traces, to minimize cross-talk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent cross-talk. The P+/P- signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

Figure 52. Recommended USB Schematic



The recommended USB trace characteristics are as follows:

- Impedance 'Z0' = 45.4 Ω
- Line delay = 160.2 ps
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Res @ 20° C = 53.9 mΩ

9.4. IO-APIC (I/O Advanced Programmable Interrupt Controller)

The IO-APIC interrupt controller architecture provides several performance benefits over the 8259 architecture. It is recommended that all uniprocessor (UP) designs connect IO-APIC signals.

- On the ICH
  — Connect PICCLK directly to ground.
  — Connect PICD0, PICD1 to ground through a 10-kΩ resistor.
- On the processor
  — PICCLK must be connected from the clock generator to the PICCLK pin on the processor.
  — Connect PICD0 to 2.5 V through 10-kΩ resistors.
  — Connect PICD1 to 2.5 V through 10-kΩ resistors.

9.5. SMBus

The **Alert on LAN** signals can be used as:

- **Alert on LAN signals:** 4.7-kΩ pull-up resistors to 3.3 VSB are required.
- **GPIOs:** Pull-up resistors to 3.3 VSB and the signals must be allowed to change states on power-up. (For example, on power-up the ICH drives *heartbeat* messages until the BIOS programs these signals as GPIOs.) The values of the pull-up resistors depend on the loading on the GPIO signal.
- **Not Used:** 4.7-kΩ pull-up resistors to 3.3 VSB are required.

If the SMBus is used only for the three SPD EEPROMs (one on each RIMM), both signals should be pulled up with a 4.7-kΩ resistor to 3.3 V.

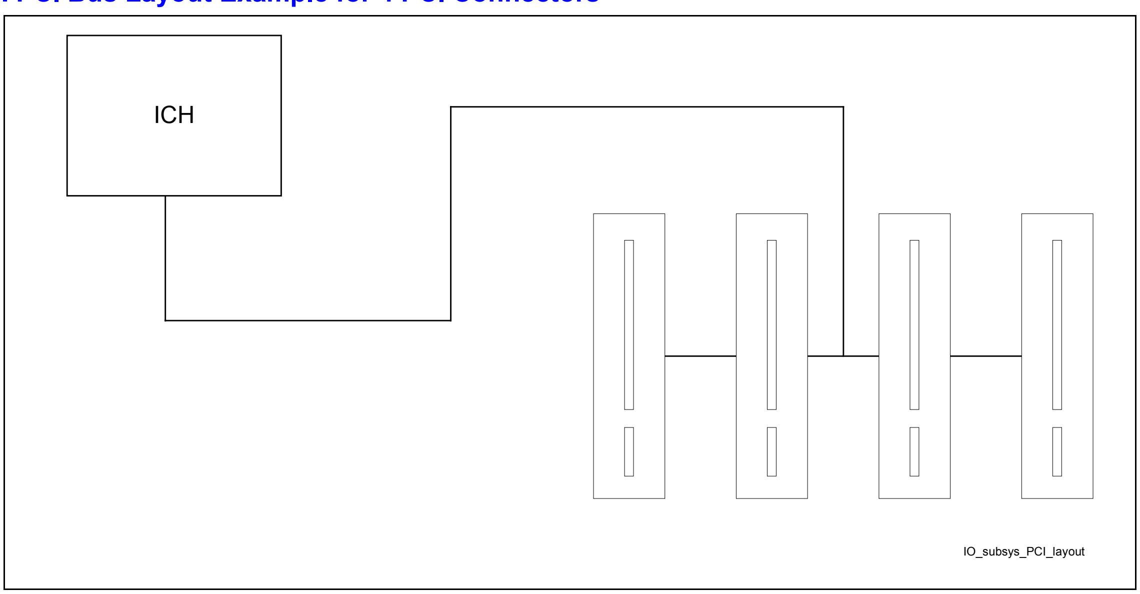
9.6. PCI

The ICH provides a PCI bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH supports 6 PCI Bus masters by providing 6 REQ#/GNT# pairs. In addition, the ICH supports 2 PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Based on simulations performed by Intel, a maximum of 4 PCI slots should be connected to the ICH. This limit is due to timing and loading considerations established during simulations. If a system designer wants 5 PCI slots connected to the ICH, then the designer's company should perform its own simulations to verify a proper design.

Figure 53. PCI Bus Layout Example for 4 PCI Connectors



9.7. LPC/FWH

9.7.1. In-Circuit FWH Programming

All cycles destined for the FWH will appear on the PCI. The ICH hub interface to the PCI bridge puts all processor boot cycles out on the PCI (before sending them out on the FWH interface). If the ICH is set for subtractive decode, these boot cycles can be accepted by a positive decode agent out on PCI. This enables booting from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH in subtractive decode mode. If a PCI boot card is inserted and the ICH is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it also is necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind the 82380AB. After booting from the PCI card, one potentially could program the FWH in circuit and program the ICH CMOS.

9.7.2. FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports a Vpp of 3.3 V or 12 V. If Vpp is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 Vpp for 80 hours. The 12 Vpp would be useful in a programmer environment, if it typically is an event that occurs very infrequently (much fewer than 80 hours). The Vpp pin MUST be tied to 3.3 V on the motherboard.

9.8. RTC

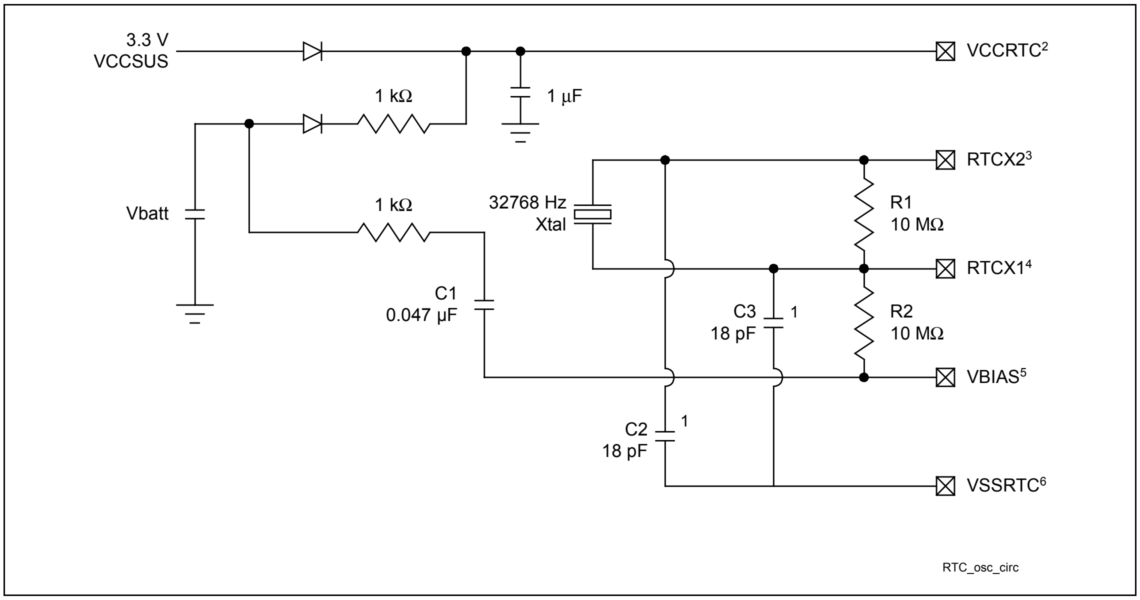
The ICH contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. This internal RTC module provides two key functions: keeping the date and time and storing system data in its RAM when the system is powered down.

This section will explain the recommended hookup for the RTC circuit for the ICH. **This circuit is not the same as the circuit used for the PIIX4.**

9.8.1. RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins.

Figure 54. External Circuitry of RTC Oscillator



NOTES:

1. The exact capacitor value should be based on the crystal vendor's recommendations.
2. VccRTC: Power for RTC well
3. RTCX2: Crystal input 2 – Connected to the 32.768-kHz crystal
4. RTCX1: Crystal input 1 – Connected to the 32.768-kHz crystal
5. VBIAS: RTC bias voltage – This pin is used to provide a reference voltage. This DC voltage sets a current, which is mirrored through the oscillator and buffer circuitry.
6. Vss: Ground

9.8.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C1 should be set to 0.047 µF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer-specified load capacitance (Cload) for the crystal, when combined with the parasitic capacitance of the trace, socket (if used), and package.

The following equation can be used to choose the external capacitance values (C2 and C3):

Cload = (C2*C3) / (C2+C3) + Cparasitic

Where C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain 32.768 kHz.

9.8.3. RTC Layout Considerations

- Keep the lead lengths as short as possible. Approximately 0.25" is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Don't route any switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean. Use a filter, such as an RC low-pass or a ferrite inductor.

9.8.4. RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system.

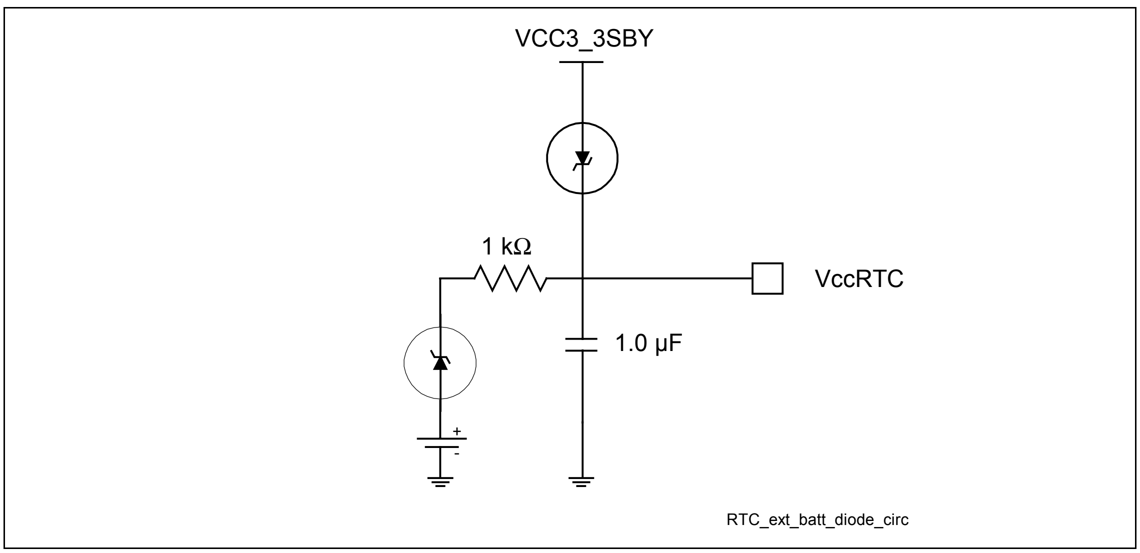
Example batteries are the Duracell* 2032, 2025 or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

170,000 µAh / 3 µA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is within the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse-biased when the system power is not available. This is an example of a diode circuitry that can be used.

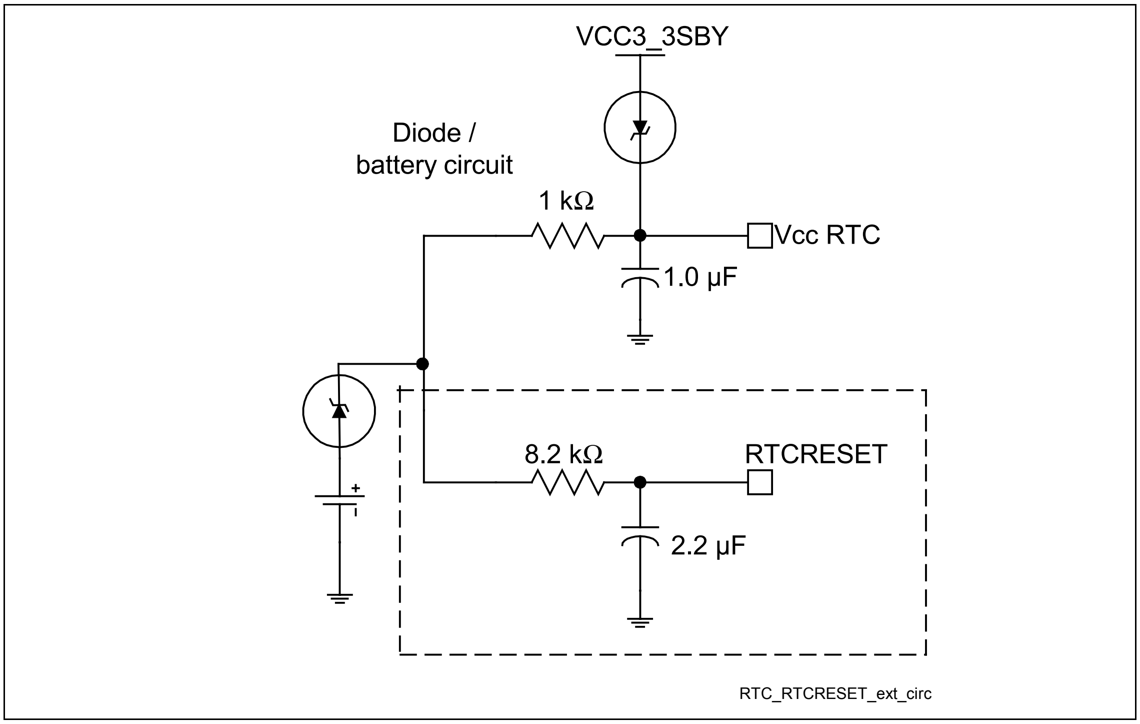
Figure 55. Diode Circuit to Connect RTC External Battery



A standby power supply should be used to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

9.8.5. RTC External RTCRESET Circuit

Figure 56. RTCRESET External Circuit for the ICH RTC



The ICH RTC requires some additional external circuitry. The RTCRESET (RTC Well Test) signal is used to reset the RTC well. The external capacitor (2.2 µF) and the external resistor (8.2 kΩ) between RTCRESET and the RTC battery (Vbat) were selected to create a RC time delay, such that RTCRESET will go high some time after the battery voltage is valid. The RC time delay should be within the range 10–20 ms. When RTCRESET is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and it remains set until software clears it. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRESET circuit is combined with the diode circuit (Figure 55), which allows the RTC well to be powered by the battery when the system power is not available. The previous figure shows an example of this circuitry, which is used in conjunction with the external diode circuit.

9.8.6. RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should be routed with trace lengths shorter than 1". (The shorter, the better.)
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimally by means of a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

9.8.7. Guidelines to Minimize ESD Events

Guidelines to minimize ESD events that may cause loss of CMOS contents:

- Provide a 1-µF 805 X5R dielectric, monolithic, ceramic capacitor on the VCCRTC pin. This capacitor connection should not be stubbed off the trace run and should be as close as possible to the ICH. If a stub is required, its maximum length should be a few mm. The ground connection should be made through a via to the plane, with no trace between the capacitor pad and the via.
- Place the battery, the 1-kΩ series current limit resistor, and the common-cathode isolation diode very close to the ICH. If this is not possible, place the common-cathode diode and the 1-kΩ resistor as close as possible to the 1-µF cap. Do not place these components between the cap and the ICH. The battery can be placed remotely from the ICH.
- On boards that have chassis intrusion utilizing inverters powered by the VCCRTC pin, place the inverters as close as possible to the common-cathode diode. If this is not possible, keep the trace run near the center of the board.
- Keep the ICH VCCRTC trace away from the board edge. If this trace must run from opposite ends of the board, keep the trace run towards the board center, away from the board edge where contact could be made by those handling the board.

9.8.8. VBIAS and DC Voltage and Noise Measurements

- Steady-state VBIAS will be a DC voltage of about 0.38 V ± 0.06 V.
- VBIAS will be “kicked” when the battery is inserted, to about 0.7–1.0 V, but it will return to its DC value within a few msec.
- Noise on VBIAS must be kept to a minimum: 200 mV or less.
- VBIAS is very sensitive and cannot be probed directly. It can be probed through a 0.01-µF capacitor.
- Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely.
- To minimize the VBIAS noise, it is necessary to implement the routing guidelines described previously as well as the required external RTC circuitry.

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10. Clocking

For the Intel® 815 chipset system, there are two clock specifications. One is for a two-DIMM solution, and the other is for a three-DIMM solution.

10.1. 2-DIMM Clocking

10.1.1. Clock Generation

Table 25. Intel® CK815 (2 DIMM) Clocks

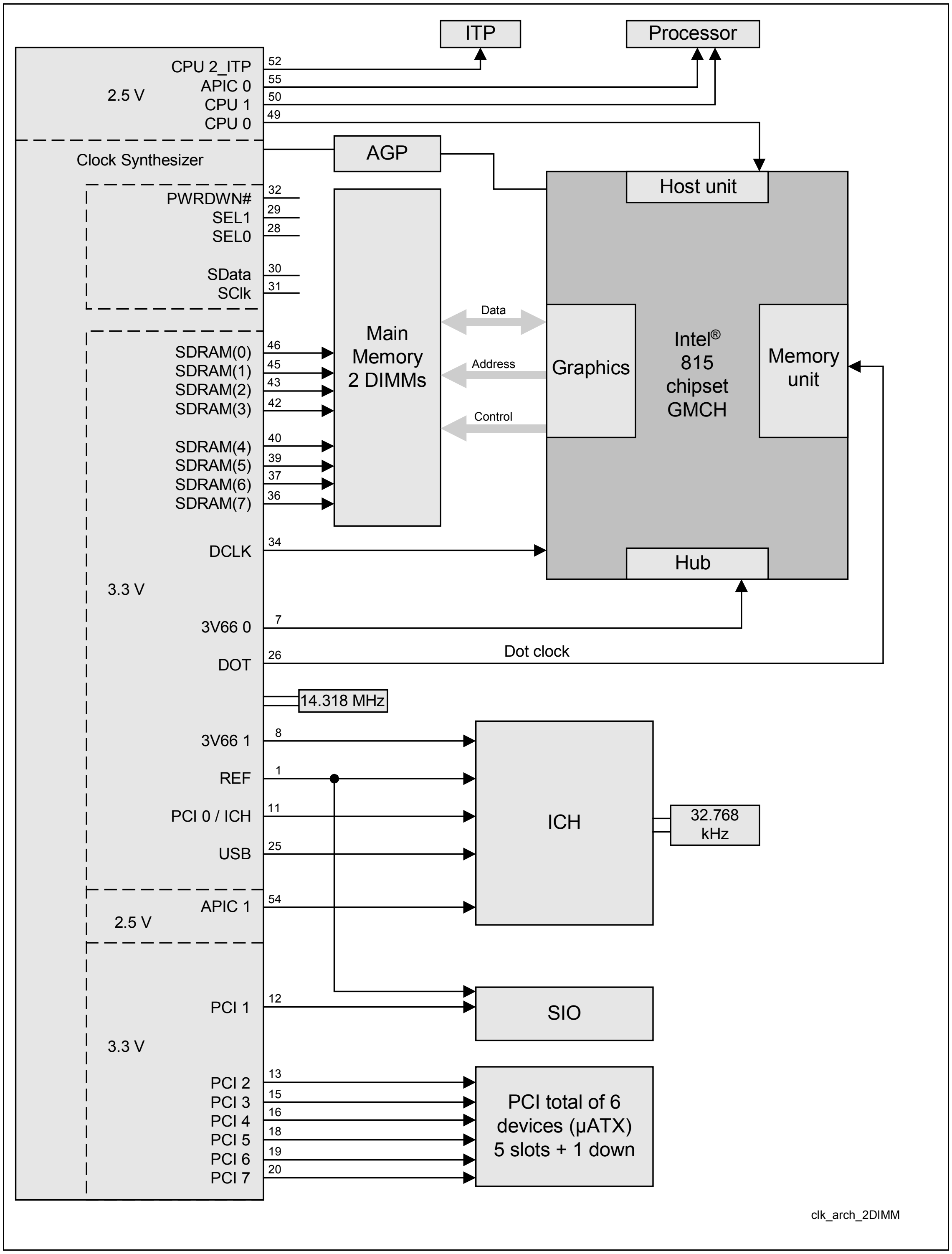
Number	Clock	Frequency
3	Processor clocks	66/100/133 MHz
9	SDRAM clocks	100 MHz
7	PCI clocks	33 MHz
2	APIC clocks	16.67/33 MHz
2	48-MHz clocks	48 MHz
3	3-V, 66-MHz clocks	66 MHz
1	REF clock	14.31818 MHz

Features (56-Pin SSOP Package)

- 9 copies of 100-MHz SDRAM clocks (3.3 V) [SDRAM0–7, DClk]
- 7 copies of PCI clock (33 MHz) (3.3 V)
- 2 copies of APIC clock @ 33 MHz, synchronous to processor clock (2.5 V)
- 1 copy of 48-MHz USB clock (3.3 V) [non-SSC] (type 3 buffer)
- 1 copy of 48-MHz DOT clock (3.3 V) [non-SSC] (see DOT details)
- 3 copies of 3-V, 66-MHz clock (3.3 V)
- 1 copy of REF clock @ 14.31818 MHz (3.3 V)
- Reference 14.31818-MHz xtal oscillator input
- Power-down pin
- Spread-spectrum support
- IIC support for turning off unused clocks

10.1.2. 2-DIMM Clock Architecture

Figure 57. Intel® 815 Chipset Clock Architecture



10.2. 3-DIMM Clocking

10.2.1. Clock Generation

Table 26. Intel® CK815 (3 DIMM) Clocks

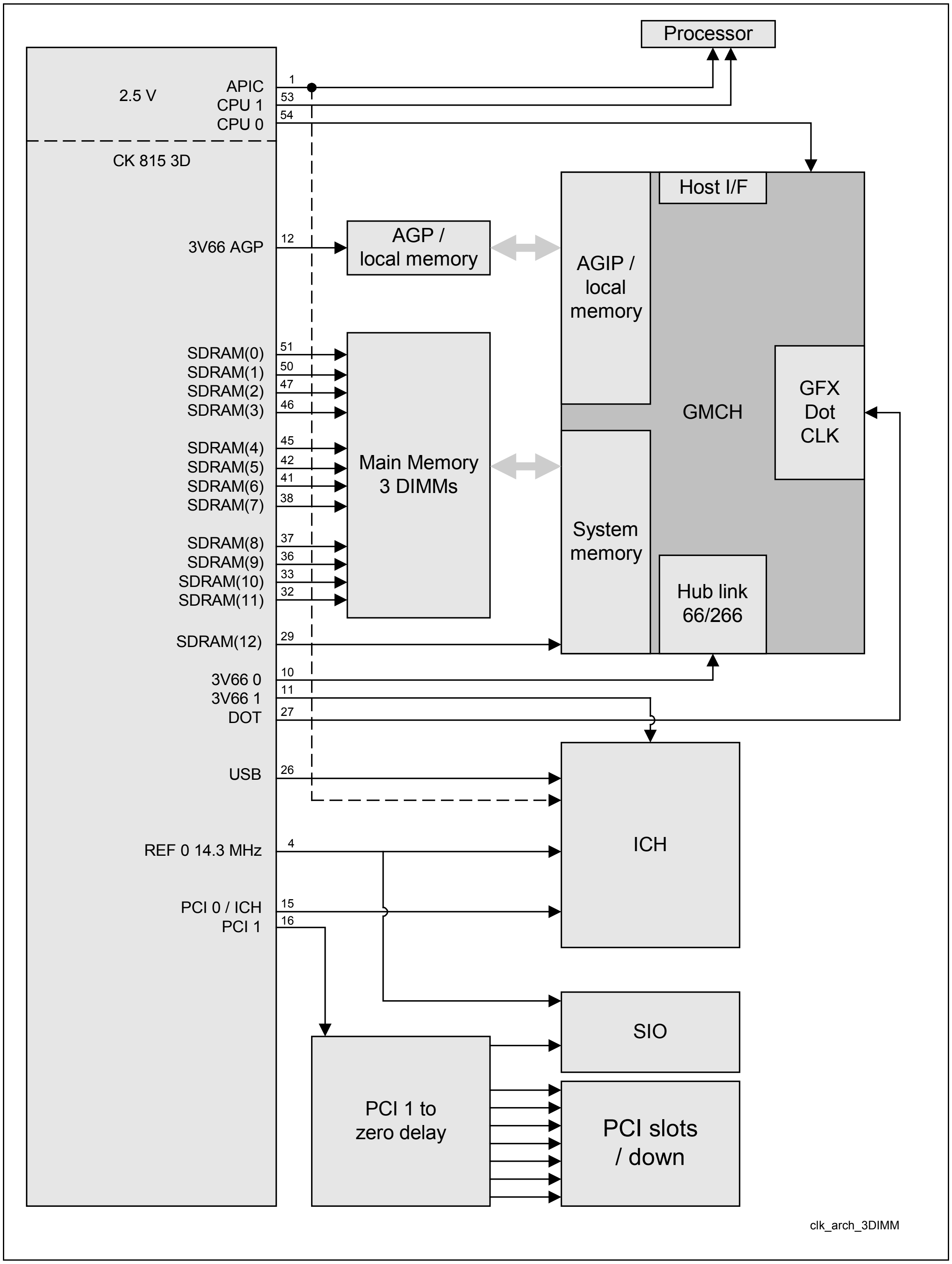
Number	Clock	Frequency
2	Processor clocks	66/100/133 MHz
13	SDRAM clocks	100 MHz
2	PCI clocks	33 MHz
1	APIC clocks	33 MHz
2	48MHz clocks	48 MHz
3	3-V, 66-MHz clocks	66 MHz
1	REF clock	14.31818 MHz

Features (56-Pin SSOP Package)

- 13 copies of SDRAM clocks
- 2 copies of PCI clock
- 1 copy of APIC clock
- 1 copy of 48-MHz USB clock (3.3 V) [non-SSC] (type 3 buffer)
- 1 copy of 48-MHz DOT clock (3.3 V) [non-SSC] (see DOT details)
- 3 copies of 3-V, 66-MHz clock (3.3 V)
- 1 copy of REF clock @ 14.31818 MHz (3.3 V)
- Reference 14.31818-MHz xtal oscillator input
- Spread-spectrum support
- IIC support for turning off unused clocks

10.2.2. 3-DIMM Clock Architecture

Figure 58. Intel® 815 Chipset Clock Architecture



10.3. Clock Routing Guidelines

This section presents the generic clock routing guidelines for both 2-DIMM and 3-DIMM boards. For 3-DIMM boards, additional analysis must be performed by the motherboard designer to ensure that the clocks generated by the external PCI clock buffer meet the PCI specifications for clock skew at the receiver, when compared with the PCI clock at the ICH.

Figure 59. Clock Routing Topologies

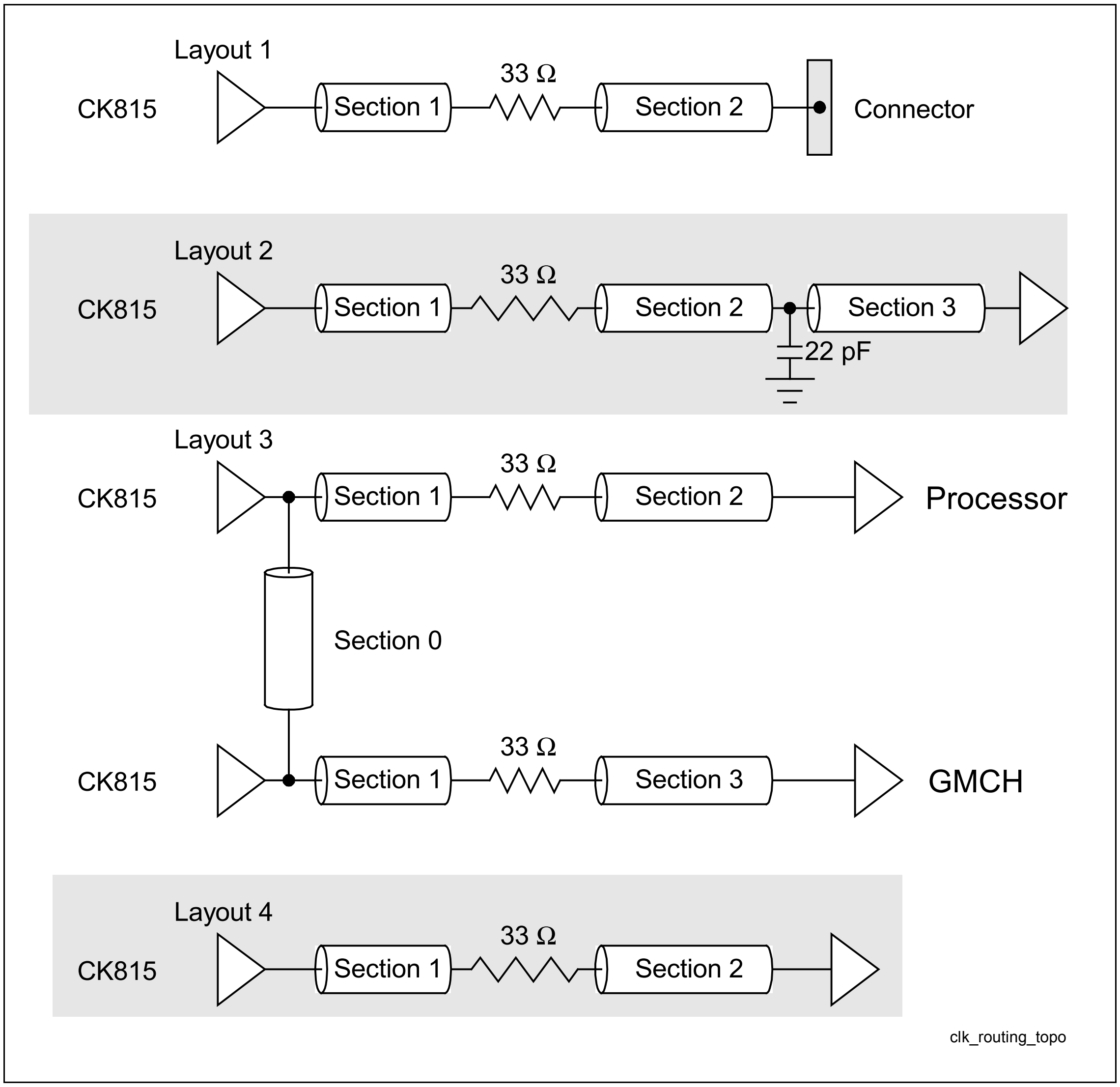


Table 27. Simulated Clock Routing Solution Space

Destination	Topology from Previous Figure	Section 0 Length	Section 1 Length	Section 2 Length	Section 3 Length
SDRAM MCLK	Layout 1	N/A	< 0.5”	A[1]	N/A
GMCH SCLK	Layout 2	N/A	< 0.5”	A + 3.5”	0.5”
Processor BCLK	Layout 3	< 0.1”	< 0.5”	A + 5.2”	A + 8”
GMCH HCLK			<0.5”		
GMCH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH PCICLK	Layout 4	N/A	<0.5”	A + 8”	N/A
AGP CLK	Layout 4	N/A	<0.5”	A + 3" to A + 4"	N/A
PCI Down2	Layout 4	N/A	<0.5”	A + 8.5” to A + 14”	N/A
PCI Slot2	Layout 1	N/A	<0.5”	A + 5” to A + 11”	

NOTES:
1. Length “A” has been simulated up to 6”.
2. All PCI clocks must be within 6” of the ICH PCICLK route length. Routing on PCI add-in cards must be included in this length. In the presented solution space, ICH PCICLK was considered to be the shortest in the 6” trace routing range, and other clocks were adjusted from there. The system designer may choose to alter the relationship between the PCI device and slot clocks, as long as all PCI clock lengths are within 6”. Note that the ICH PCICLK length is fixed, to meet the skew requirements of ICH PCICLK to ICH HUBCLK.

General clock layout guidelines:

- All clocks should be routed 5 mils wide with 15-mil spacing to any other signals.
- It is recommended to place capacitor sites within 0.5” of the receiver of all clocks. They are useful in system debug and AC tuning.
- Series resistor for clock guidelines: 22 Ω for GMCH SCLK and SDRAM clocks. All other clocks use 33 Ω.

10.4. Clock Decoupling

Several general layout guidelines should be followed when laying out the power planes for the CK815 clock generator.

- Isolate the power plane to each clock group.
- Place local decoupling as close as possible to power pins and connect with short, wide traces and copper.
- Connect pins to the appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14-mil finished hole with a 24–26-mil path. An example power via is an 18-mil finished hole with a 33–38-mil path. For large decoupling or power planes with large current transients, it is advisable to use a larger power via.

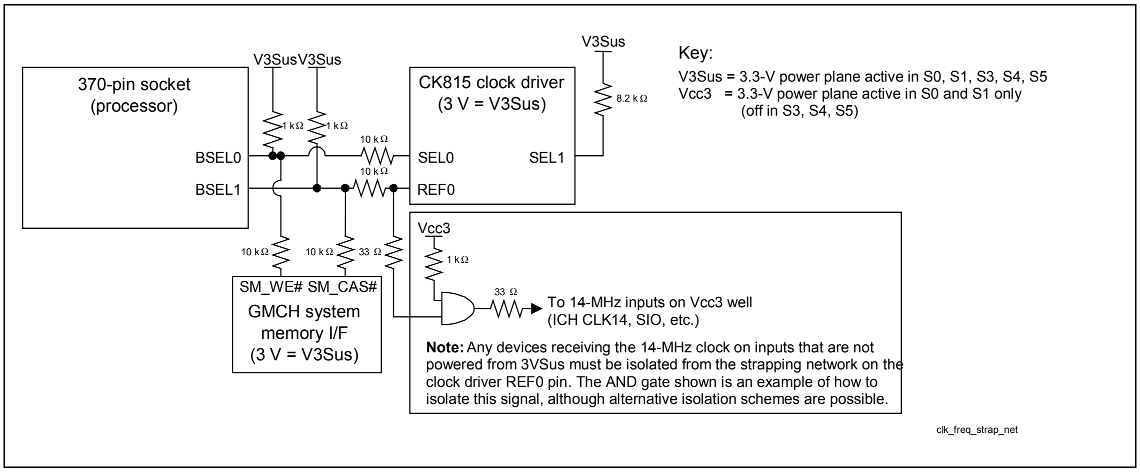
10.5. Clock Driver Frequency Strapping

A CK815-compliant clock driver device uses two of its pins (SEL0 and REF0) to determine whether processor clock outputs should run at 133 MHz, 100 MHz or 66 MHz. In addition, there is a third defined strapping pin, called SEL1, which must be pulled high for normal clock driver operation. Refer to the appropriate CK815 clock driver specification for detailed strap timings and logic encoding of straps.

SEL0 and REF0 are driven by either the processor (dependent on processor populated in the 370-pin socket) or pull-up resistors on the motherboard. While SEL0 is a pure input to a CK815-compliant clock driver, REF0 is also the 14-MHz output that drives the ICH and other devices on the platform. In addition to sampling straps at reset, CK815-compliant clock drivers are configured by the BIOS via a two-wire interface, to drive SDRAM clock outputs at either 100 MHz (default) or 133 MHz (if all system requirements are met).

If ACPI power management is supported on an Intel 815 chipset platform, the motherboard designer should power the clock chip and input straps from the 3.3 Vsus (e.g., active in S0, S1, S3, S4, S5) power supply. This enables the clock driver to seamlessly maintain its configuration register settings while switching between ACPI sleep and wake states. A block diagram of the recommended clock frequency strapping network with implementation considerations is shown in the following figure.

Figure 60. Recommended Clock Frequency Strapping Network



For the platform to come out of a reset properly, clock driver straps powered from the standby supply must be isolated from any logic that powers off in ACPI sleep states.

10.6. Clock Skew Assumptions

The clock skew assumptions in the following table are used in the system clock simulations.

Table 28. Simulated Clock Skew Assumptions

Skew Relationships	Target	Tolerance (±)	Notes
HCLK @ GMCH to HCLK @ processor	0 ns	150 ps	• Assumes ganged clock outputs will allow max. of 50-ps skew
HCLK @ GMCH to SCLK @ GMCH	0 ns	600 ps	• 500-ps pin-to-pin skew • 100-ps board/package skew
SCLK @ GMCH to SCLK @ SDRAM	0 ns	630 ps	• 250-ps pin-to-pin skew • 380-ps board + DIMM variation
HLCLK @ GMCH to SCLK @ GMCH	0 ns	900 ps	• 500-ps pin-to-pin skew • 400-ps board/package skew
HLCLK @ GMCH to HCLK @ GMCH	0 ns	700 ps	• 500-ps pin-to-pin skew • 200-ps board/package skew
HLCLK @ GMCH to HLCLK @ ICH	0 ns	375 ps	• 175-ps pin-to-pin skew • 200-ps board/package skew
HLCLK @ ICH to PCICLK @ ICH	0 ns	900 ps	• 500-ps pin-to-pin skew • 400-ps board/package skew
PCICLK @ ICH to PCICLK @ other PCI devices	0 ns	2.0-ns window	• 500-ps pin-to-pin skew • 1.5-ns board/add-in skew
HLCLK @ GMCH to AGPCLK @ connector			• Total electrical length of AGP connector + add-in card is 750 ps (according to AGP2.0 spec and AGP design guide 1.0). • Motherboard clock routing must account for this additional electrical length. Therefore, AGPCLK routed to the connector must be shorter than HLCLK to the GMCH, to account for this additional 750 ps.

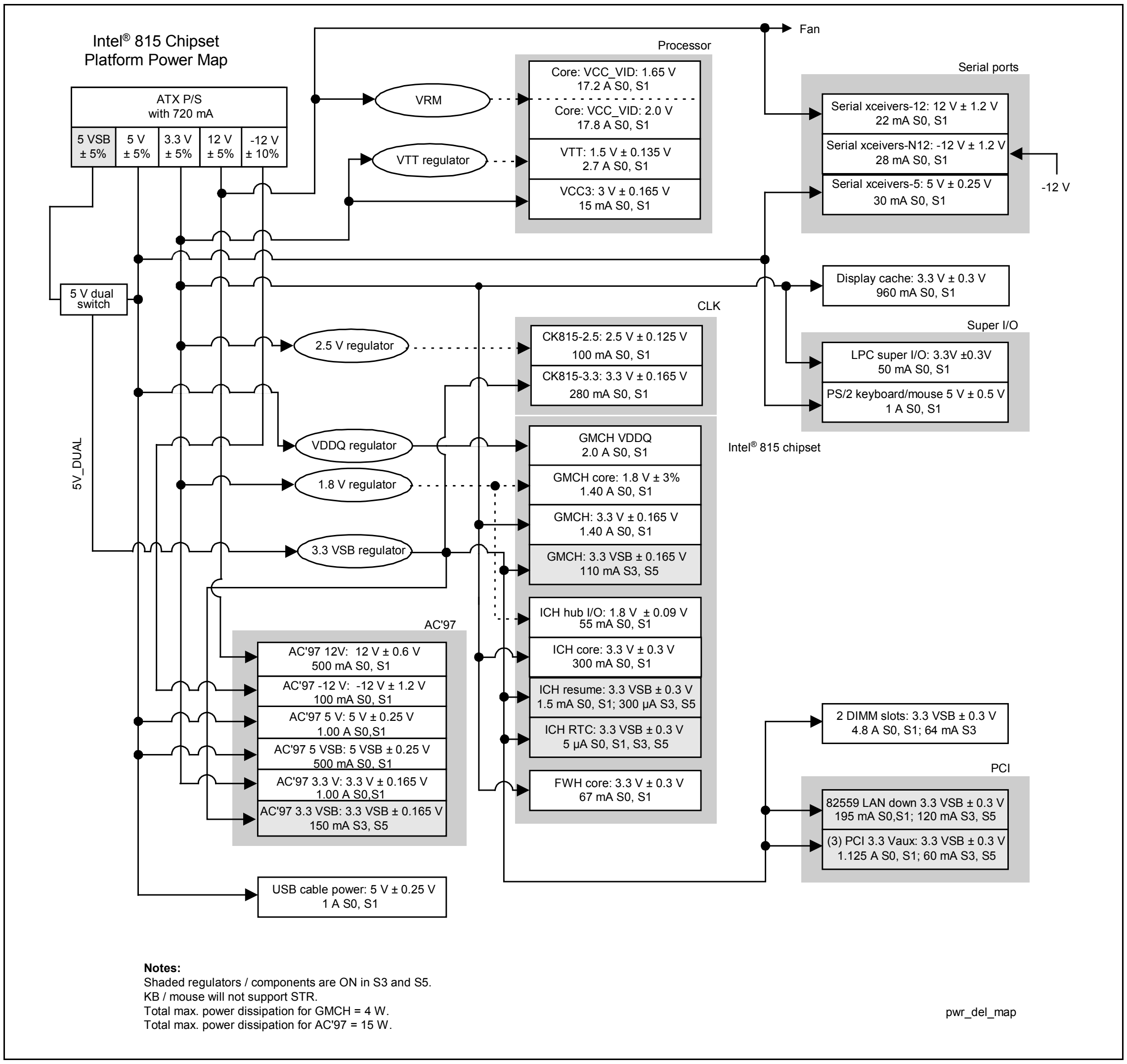
11. Power Delivery

The following figure shows the power delivery architecture for an example Intel® 815 chipset platform. This power delivery architecture supports the "Instantly Available PC Design Guidelines" via the *suspend-to-RAM* (STR) state.

During STR, only the necessary devices are powered. These devices include main memory, the ICH resume well, PCI wake devices (via 3.3 Vaux), AC'97, and optionally the USB. (The USB can be powered only if sufficient standby power is available.) To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *full power*. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual*-power rail.

The solutions given in this design guide are only examples. Many power distribution methods achieve similar results. When deviating from these examples, it is critical to consider the effect of the change.

Figure 61. Power Delivery Map



11.1. Thermal Design Power

Thermal Design Power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP of the 82815 GMCH component is 5.1 W.

11.2. Power Sequencing

This section shows the timings among various signals during different power state transitions.

Figure 62. G3-S0 Transistion

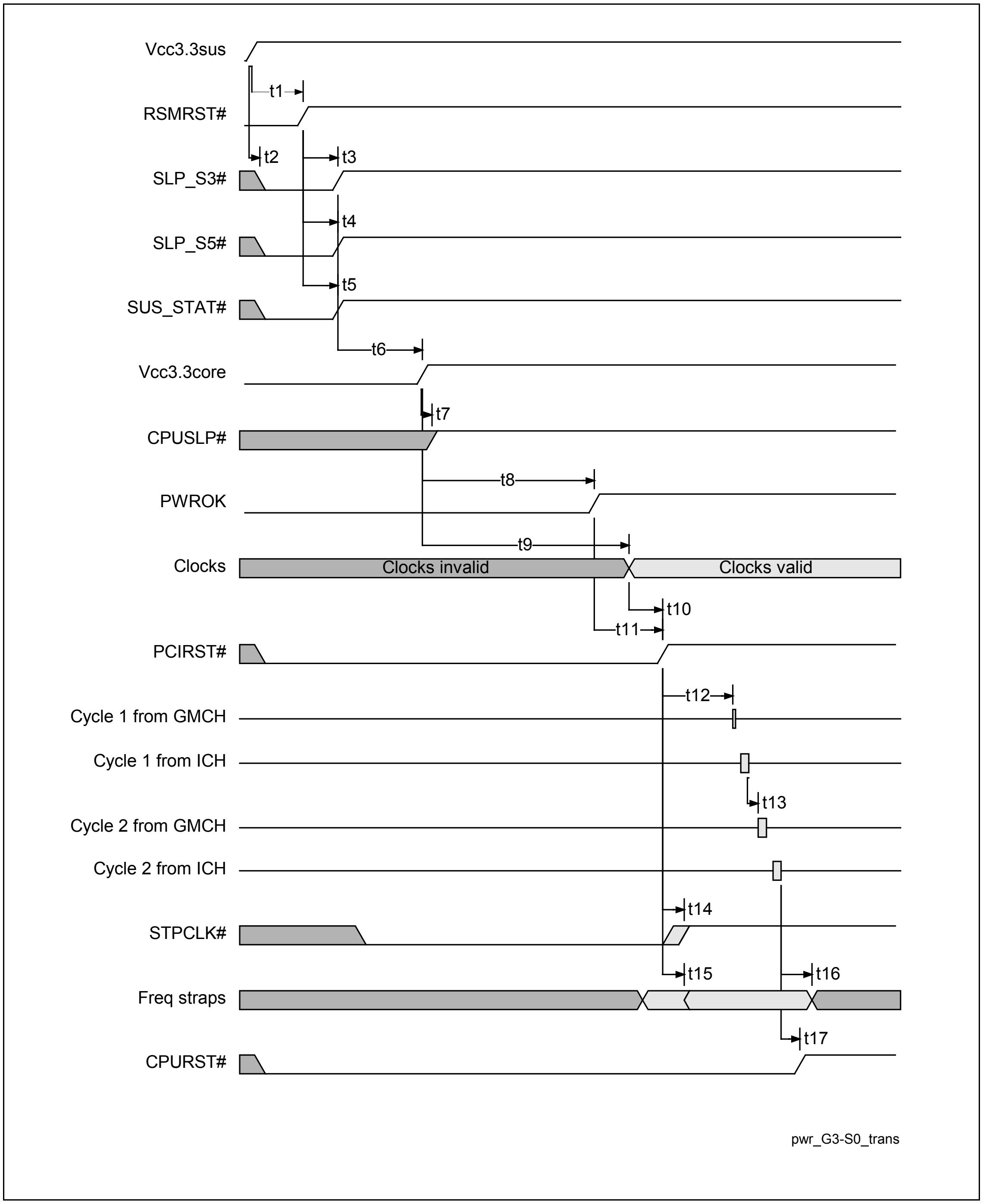


Figure 63. S0-S3-S0 Transition

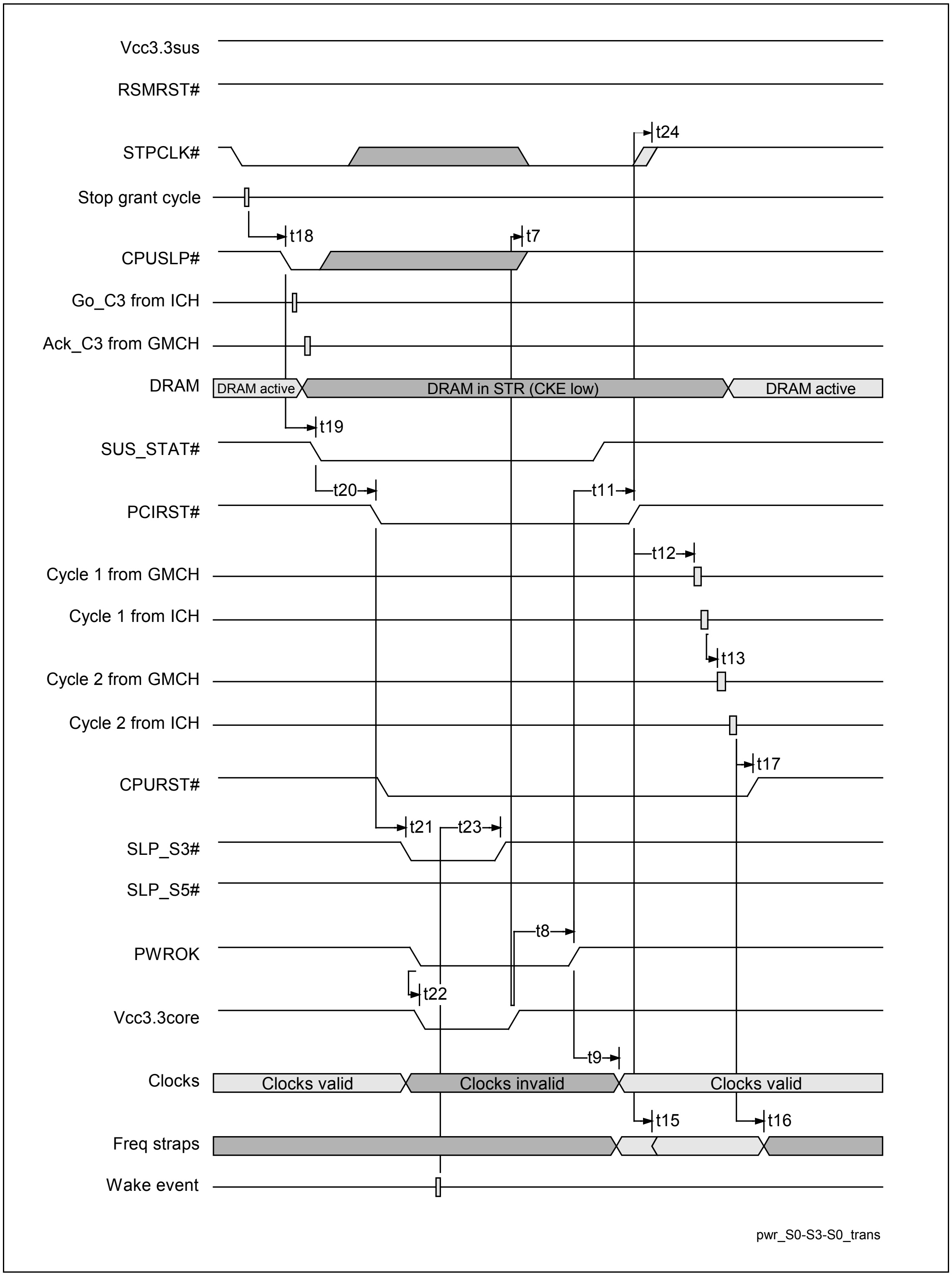


Figure 64. S0-S5-S0 Transition

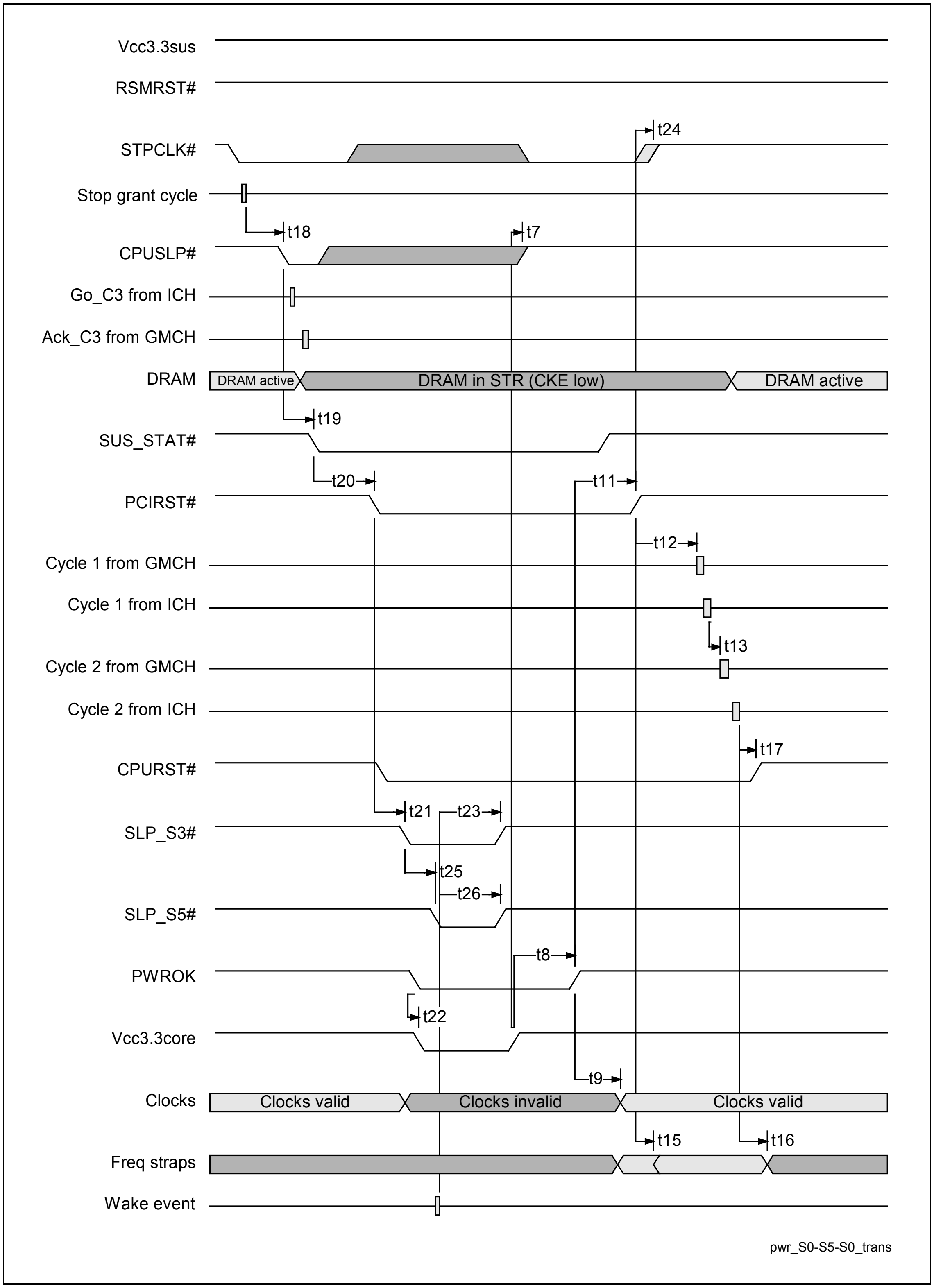


Table 29. Power Sequencing Timing Definitions

Symbol	Parameter	Min.	Max.	Units
t1	VccSUS Good to RSMRST# inactive	1	25	ms
t2	VccSUS Good to SLP_S3#, SLP_S5#, and PCIRST# active		50	Ns
t3	RSMRST# inactive to SLP_S3# inactive	1	4	RTC clocks
t4	RSMRST# inactive to SLP_S5# inactive	1	4	RTC clocks
t5	RSMRST# inactive to SUS_STAT# inactive	1	4	RTC clocks
t6	SLP_S3#, SLP_S5#, SUS_STAT# inactive to Vcc3.3core good	*	*	
t7	Vcc3.3core good to CPUSLP# inactive		50	ns
t8	Vcc3.3core good to PWROK active	*	*	
t9	Vcc3.3core good to clocks valid	*	*	
t10	Clocks valid to PCIRST# inactive	500		µs
t11	PWROK active to PCIRST# inactive	.9	1.1	ms
t12	PCIRST# inactive to Cycle 1 from GMCH		1	ms
t13	Cycle 1 from ICH to Cycle 2 from GMCH		60	ns
t14	PCIRST# inactive to STPCLK de-assertion	1	4	PCI clocks
t15	PCIRST# to frequency straps valid	-4	4	PCI clocks
t16	Cycle 2 from ICH to frequency straps invalid		180	ns
t17	Cycle 2 from ICH to CPURST# inactive		110	ns
t18	Stop Grant Cycle to CPUSLP# active		8	PCI clocks
t19	CPUSLP# active to SUS_STAT# active		1	RTC clock
t20	SUS_STAT# active to PCIRST# active	2	3	RTC clocks
t21	PCIRST# active to SLP_S3# active	1	2	RTC clocks
t22	PWROK inactive to Vcc3.3core not good	20		ns
t23	Wake event to SLP_S3# inactive	2	3	RTC clocks
t24	PCIRST# inactive to STPCLK# inactive	1	4	PCI clocks
t25	SLP_S3# active to SLP_S5# active	1	2	RTC clocks
t26	SLP_S5# inactive to SLP_S3# inactive	2	3	RTC clocks

11.3. Pull-up and Pull-down Resistor Values

Pull-up and pull-down values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be performed to determine the minimum/maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, and other considerations.

A simplistic DC calculation for a pull-up value is:

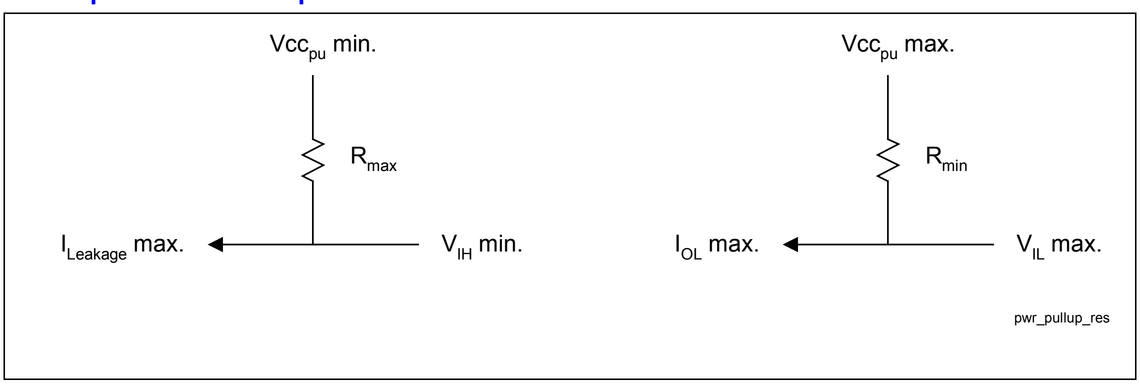
$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{LEAKAGE}\ MAX$

$R_{MIN} = (Vcc_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$

Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} is also determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including input capacitance of the devices to be driven, output capacitance of the driver, and line capacitance. This calculation yields the largest pull-up resistor allowable to meet the rise time t.

$R_{MAX} = -t / (C * In(1-(V_{IH}\ MIN / Vcc_{PU}\ MIN)))$

Figure 65. Pull-up Resistor Example



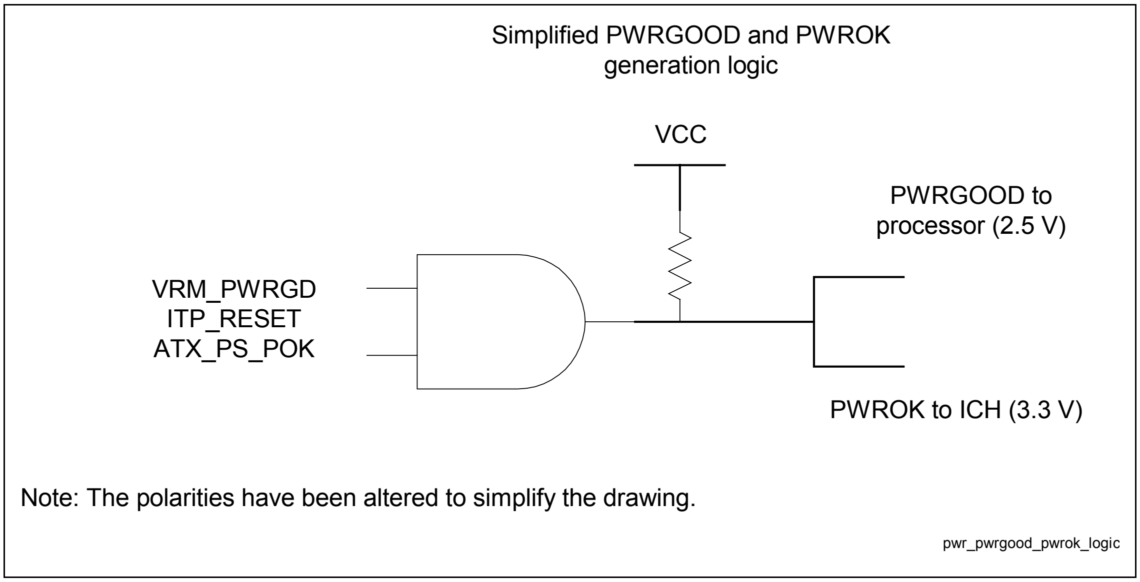
11.4. ATX Power Supply PWRGOOD Requirements

The PWROK signal must be glitch free for proper power management operation. The ICH sets the PWROK_FLR bit (ICH GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at Offset A2h). If this bit is set upon resume from S3 power down, the system will reboot, and control of the system will not be given to the program running when entering the S3 state. System designers should ensure that PWROK signal designs are glitch free.

11.5. Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel's on/off power button. The ICH integrates 16-msec debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a Schmitt trigger to square off and maintain its signal integrity. It should not be connected directly to logic on the board.
- PS_POK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, while making sure that the input to the ICH0/ICH is at the 3-V level. The RSMST# signal requires a minimum time delay of 1 millisecond from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 millisecond delay should be placed before the Schmitt trigger circuit. The reference design implements a 20-ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- It is recommended that 3.3-V logic be used to drive RSMRST#, to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3-V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 msec.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V using a 330-Ω resistor.
- The circuitry checks for both powered-up processor VRM as well as the PS_POK signal from the ATX power supply connector, before asserting PWRGOOD and PWROK to the PROCESSOR and the ICH.

Figure 66. PWRGOOD and PWROK Logic



- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.
- SLP_S3# from the ICH must be inverted and then connected to PSON of the power supply connector, to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

11.5.1. Power Button Implementation

The following items should be considered when implementing a power management model for a desktop system. The power states are as follows:

S1 – Stop grant (PROCESSOR context not lost)
S3 – STR (Suspend-to-RAM)
S4 – STD (Suspend-to-disk)
S5 – Soft-off

- Wake: Pressing the power button wakes the computer from S1-S5.
- Sleep: Pressing the power button signals software/firmware as follows:
- If SCI is enabled, the power button will generate an SCI to the operating system.
  - The operating system will implement the power button policy to allow orderly shutdowns.
  - Do not override this with additional hardware.
- If SCI is not enabled:
  - Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
  - Poll the power button status bit during POST while SMIs are not loaded, and go directly to soft-off if it gets set.
  - Always install an SMI handler for the power button that operates until ACPI is enabled.
- Emergency override: When the power button is pressed for 4 seconds, the state transitions directly to S5.
  - This is only to be used in EMERGENCIES, when the system fails to respond.
  - In most cases, this will cause user data to be lost.
- Do not suggest pressing the power button for 4 sec. as the normal mechanism for powering off the machine. This violates ACPI.
- To be compliant with the latest PC9x specification, machines must appear off to the user when in the S1-S4 sleeping states. This implies the following:
  - All lights except a power state light must be off.
  - The system must be inaudible (i.e., silent or stopped fan, drives off).
- Note: Contact Microsoft* for the latest information concerning PC9x and Microsoft Logo programs.

12. System Design Checklist

This design review checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an Intel® 815 chipset. This is not a complete list and does guarantee that a design will function properly. Besides the items in the following text, refer to the most recent version of the design guide for more detailed instructions on designing a motherboard.

The following tables contain design considerations for the various portions of a design. Each table describes one portion and is titled accordingly. Contact your Intel Field Representative for questions or issues regarding the interpretation of information in these tables.

12.1. Host Interface GTL Bus and GTL Signals

Checklist Items	Recommendations
A[35:3]# [1]	Connect A[31:3]# to GMCH. Leave A[35:32]# as No Connect (not supported by chipset).
ADS#, BNR#, BPRI#, DBSY#, DEFER#, DRDY#, HA[31:3]#, HD[63:0]#, HIT#, HITM#, LOCK#, REQ[4:0]#, RS[2:0]#, TRDY#	Terminate to Vtt1.5 through 56-ohm resistor / Connect to GMCH
BREQ[0]# (BR0#)	10 Ω pulldown resistor to ground.
RESET#/ RESET2#	Terminate to Vtt1.5 through 86-ohm resistor / decoupled through 22-ohm resistor in series with 10 pf capacitor to ground / Connect to GMCH. Also terminated to Vtt1.5 through 86-ohm resistor.

12.2. CMOS (Non-GTL) Signals

Checklist Items	Recommendations
IERR#	150 Ω pullup resistor to VCC_CMOS if tied to custom logic or leave as No Connect (not used by chipset).
PREQ#	~200 Ω–330 Ω pullup resistor to VCC_CMOS / Connect to ITP.
PWRGOOD	150 Ω–330 Ω pull-up to 2.5V, output from the PWRGOOD logic.
THERMTRIP#	150 Ω pullup resistor to VCC_CMOS and connect to power off logic, or leave as No Connect.
A20M#, FERR#, FLUSH#, IGNNE#, INIT#, INTR#, NMI, PICD[1:0], SLP#, SMI#, STPCLK#,	150 Ω PULL-UP TO VCMOS / CONNECT TO ICH
PWRGOOD	330 Ω pull-up to VCC2_5 / Connect to POWERGOOD logic
VTT	Route VTT to all components on the host bus
AA33, AA35, AN21, E23, S33, S37, U35, U37	Since an Intel® 815 chipset platform will not be Intel® Celeron™ processor (PPGA) compatible, these pins must be connected directly to Vtt
G37	It is now recommended that pin G37, normally RESERVED, be connected directly to the 1.5Volt Vtt plane.

12.3. TAP Checklist for 370-Pin Socket Processors

Checklist Items	Recommendations
TCK, TMS	1 KΩ pullup resistor to VCC_CMOS / 47 Ω series resistor to ITP.
TDI	~200 Ω–330 Ω pullup resistor to VCC_CMOS / Connect to ITP.
TDO	150 Ω pullup resistor to VCC_CMOS / Connect to ITP.
TRST#	~680 Ω pulldown resistor to ground / Connect to ITP.
PRDY#	150 Ω pullup resistor to Vtt / 240 Ω series resistor to ITP.

12.4. Miscellaneous Checklist for 370-Pin Socket Processors

Checklist Items	Recommendations
BCLK	Connect to clock generator / 22 Ω–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the GMCH and processor.
BSEL0	Case 1, 66/100/133 MHz support: 1 KΩ pullup resistor to 2.5V, connect to CK810E SEL0 input, connect to GMCH LMD29 pin via 10 KΩ series resistor. Case 2, 100/133 MHz support: 1 KΩ pullup resistor to 2.5V, connect to PWRGOOD logic such that a logic low on BSEL0 negates PWRGOOD.
BSEL1	1 KΩ pullup resistor to 2.5V, connect to CK810E REF pin via 10 KΩ series resistor, connect to GMCH LMD13 pin via 10 KΩ series resistor.
CLKREF	Connect to divider on VCC_2.5 or VCC_3.3 to create 1.25V reference with a 4.7 uF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. Do not use VTT as source voltage for this reference! See Figure 1-9.
CPUPRES#	Tie to ground, leave as No Connect, or could be connected to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1 ΩK–10 KΩ pullup resistor to any voltage.
EDGCTRL/VRSEL	Not needed for Intel® Pentium III processor support – No Connect.
PICCLK	Connect to clock generator / 22 Ω–33 Ω series resistor (though OEM needs to simulate based on driver characteristics).
PLL1, PLL2	Low pass filter on VCC_CORE provided on motherboard. Typically a 4.7 uH inductor in series with VCC_CORE is connected to PLL1 then through a series 33 uF capacitor to PLL2.
RTTCTRL[5] (S35), SLEWCTRL (E27)	110 Ω ±1% pulldown resistor to ground.
THERMDN, THERMDP	No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
VCC_1.5	Connected to same voltage source as VTT. Must have some high and low frequency decoupling.
VCC_2.5	Does not need to be connected for Intel® Pentium III processor support. No Connect.
VCC_CMOS	Used as pull-up voltage source for CMOS signals between processor and chipset and for TAP signals between processor and ITP. Must have some decoupling (HF/LF) present.
VCC_CORE	10 ea (min) 4.7 uF in 1206 package all placed within the PGA370 socket cavity. 8 ea (min) 1 uF in 0612 package placed in the PGA370 socket cavity.
VCORE_DET (E21)	220 Ω pullup resistor to 3.3V, connect to GMCH LMD27 pin via 10 KΩ series resistor.
VID[3:0]	Connect to on-board VR or VRM. For on-board VR, 10 KΩ pullup resistor to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pullups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.
VID[4]	Connect regulator controller pin to ground (not on processor).

Checklist Items	Recommendations
VREF[7:0]	Connect to VREF voltage divider made up of 75 Ω and 150 Ω 1% resistors connected to Vtt. Decoupling Guidelines: 4 ea. (min) 0.1 uF in 0603 package placed within 500 mils of VREF pins.
Vtt	Connect AH20, AK16, AL13, AL21, AN11, AN15, and G35 to 1.5V regulator. Provide high and low frequency decoupling. Decoupling Guidelines: 19 ea (min) 0.1 uF in 0603 package placed within 200 mils of AGTL+ termination resistor packs (r-paks). Use one capacitor for every two (r-paks). 4 ea (min) 0.47 uF in 0612 package
NO CONNECTS	The following pins must be left as no-connects: AA33, AA35, AK30, AM2, AN21, E23, F10, G37, L33, N33, N35, N37, Q33, Q35, Q37, R2, S33, S37, U35, U37, W35, X2, Y1

12.5. ICH Checklist

Checklist Items	Recommendations
RTC circuitry	Refer to design guide for exact circuitry.
PME#, PWRBTN#, LAD[3..0]#/FWH[3..0]#	No external pull-up resistor on those signals with integrated pull-ups.
SPKR	Optional strapping: Internal pull-up resistor is enabled at reset for strapping after - reset the internal pull-up resistor is disabled. Otherwise connect to motherboard speaker logic. (When strapped, use strong pullup e.g. 2 KΩ)
AC_SDOUT, AC_BITCLK	Optional strapping: Internal pull-up resistor is enabled at reset for strapping after - reset the internal pull-up resistor is disabled. Otherwise connect to AC'97 logic.
AC_SDIN[1:0]	Internal pull-down resistor is enabled only when the AC link hut-off bit in the s ICH is set. Use 10 KΩ (approximate) pull down resistors on both signals if using AMR. For onboard AC'97 devices, use a 10 KΩ (approximate) pull down resistor on the signal that is not used. Otherwise connect to AC'97 logic.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	No external series termination resistors on those signals with integrated series resistors.
PCIRST#	The PCIRST# signal should be buffered to the IDE connectors.
No floating inputs (including bi-directional signals):	Unused core well inputs should be tied to a valid logic level (either pulled up to 3.3V or pulled down to ground). Unused resume well inputs must be either pulled up to 3.3VSB or pulled down to ground. Ensure all unconnected signals are OUTPUTS ONLY!
PDD[15:0], SDD[15:0]	PDD7 and SDD7 need a 10 KΩ (approximate) pull down resistor. No other pull-ups/pull-downs are required. Refer to ATA ATAPI-4 spefication.
PIORDY, SDIORDY	Use approximately 1 KΩ pull up resistor to 5V.
PDDREQ, SDDREQ	Use approximately 5.6 KΩ pull down resistor to ground.
IRQ14, IRQ15	Need 8.2 KΩ (approximate) pull-up resistor to 5V.
HL11	No pull-up resistor required. A test point or no stuff resistor is needed to be able to drive the ICH0/ICH into a NAND tree mode for testing purposes.
VccRTC	No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe-mode strapping for clear CMOS.
SMBus: SMBCLK SMBDATA	The value of the SMBus pull ups should reflect the number of loads on the bus. For most implementations with 4-5 loads, 4.7 KΩ resistors are recommended. OEMs should conduct simulation to determine exact resistor value.

Checklist Items	Recommendations
APICD[0:1], APICCLK	If the APIC is used: 150 Ω (approximate) pull ups on APICD[0:1] and connect APICCLK to the clock generator. If the APIC is not used: The APICCLK can either be tied to GND or connected to the clock generator, but not left floating.
GPI[8:13]	Ensure all wake events are routed through these inputs. These are the only GPIs that can be used as ACPI compliant wake events because the are the only GPI signals in the resume well that have associated status bits in the GPE1_STS register.
HL_COMP	RCOMP Method: Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull up resistor to 1.8V via a 10-mil wide, very short(-0.5 inch) trace (targeted for a nominal trace impedance of 40 Ω)
5V_REF	Refer to the most recent version of the Design Guide for implementation of the voltage sequencing circuit.
SERIRQ	Pull-up through 8.2 KΩ resistor (approximate) to 3.3V
SLP_S3#, SLP_S5#	No pullups required. These signals are always driven by the ICH0/ICH.
CLK66	Use 18 pF tuning capacitor as close as possible to ICH.
GPIO27/ALERTCLK GPIO28/ALERTDATA	Add a 10 KΩ pull up resistor to 3VSB (3 volt standby) on both of these signals.
PCI_GNT#	No external pull ups are required on PCI_GNT# signals. However, if external pull ups are implemented, they must be pulled up to 3.3V.

12.6. AGP Interface 1X Mode Signals

Checklist Items	Recommendations
RBF#, WBF#, PIPE#, GREQ#, GGNT#, GPAR, GFRAME#, GIRDY#, GTRDY#, GSTOP#, GDEVSEL#, GPERR#, GSERR# , ADSTB0, ADSTB1, SBSTB	Pull up to VDDQ through 8.2 KΩ
ADSTB0#, ADSTB1#, SBSTB#	Pull down to ground through 8.2 KΩ
PME#	Connect to PCI Connector 0 Device Ah / Connect to PCI Connector 1 Device Bh / Connect to 82559 LAN (if implemented)
TYPEDET#	Connect to AGP Voltage regulator circuitry / AGP Reference circuitry
PIRQ#A, PIRQ#B	Pull up to 5V through 2.7 KΩ / Follow Ref. Schematics (other device connections)

12.7. Hub Interface

Checklist Items	Recommendations
HUBREF	Connect to HUBREF generation circuitry. Refer to design guide update for new circuitry.
HL_COMP	Pull up to VCC1.8 through 40 Ω (both GMCH and ICH side)

12.8. Digital Video Output Port

Checklist Items	Recommendations
VREF – Connector side only	CONNECT TO VOLTAGE DIVIDER CIRCUIT NEAR DIGITAL VIDEO OUT CONNECTOR (SEE REF. SCHEMATICS)

12.9. USB Checklist

Checklist Items	Recommendations
USBP0P, USBP0N, USB_D1_N, USB_D1_P	Decouple through a 47 pf cap to GND Signal goes through 15 Ω resistor Pull down through a 15 KΩ resistor to GND
OC#0	Connected to AGP/AC97 Circuitry (See Intel CRB Schematic pg. 20)
USB_D2_N, USB_D2_P, USB_D3_N, USB_D3_P, USB_D4_N, USB_D4_P, USBP1P, USBP1N, USBP0P, USBP0N	Pull down through a 15 KΩ resistor to GND
D-/D+ data lines	Use 15 Ω series resistors.
VCC USB	Power off 5V standby if wake on USB is to be implemented IF there is adequate standy power. It should be powered off of 5 volt core instead of 5 volt standby if adequate standby power is not available.
Voltage Drop Considerations	The resistive component of the fuses, ferrite beads and traces must be considered when choosing components and Power/GND trace width. This must be done such that the resistance between the Vcc5 power supply and the host USB port is minimized. Minimizing this resistance will minimize voltage drop seen along that path during operating conditions.
Fuse	A minimum of 1A fuse should be used. A larger fuse may be necessary to minimize the voltage drop.
Voltage Droop Considerations	Sufficient bypass capacitance should be located near the host USB receptacles to minimize the voltage droop that occurs upon the hot attach of new device. See most recent version of the USB specification for more information.

12.10. IDE Checklist

Checklist Items	Recommendations
PDCS3#, SDCS3#, PDA[2:0], SDA[2:0], PDD[15:0], SDD[15:0], PDDACK#, SDDACK#, PRIOR#, SDIOR#, PDIOW#, SDIOW#	CONNECT FROM ICH TO IDE CONNECTORS. No external series termination resistors required on those signals with integrated series resistors.
PDD7, SDD7	Pull down through a 10 KΩ resistor to GND.
PDREQ, SDREQ	Pull down through a 5.6 KΩ resistor to GND.
PIORDY, SIORDY	Pull up through a 1 KΩ resistor to Vcc5
PDCS1#, SDCS1#	Connect from ICH to IDE Connectors
PRI_PD1, PRI_SD1	Pull down through a 470 Ω resistor to GND.
IDE_ACTIVE	From IDEACTP# and IDEACTS# connect to HD LED circuitry (see CRB Schematic page 35)
CBLID#/PDIAG#	Refer to the latest design guide for the correct circuit. NOTE: All ATA66 drives will have the capability to detect cables.
IDE Reset	This signal requires a 22 Ω–47 Ω series termination resistor and should be connected to buffered PCIRST#.
IRQ14, IRQ15	Need 8.2 KΩ resistor to 10 KΩ pull up resistor to 5V.
CSEL	Pull down to GND through 4.7 KΩ resistor(approximate).
IDEACTP#, IDEACTS#	For HD LED implementation use a 10 KΩ (approximate) pull up resistor to 5V.

12.11. AC '97 Checklist

Checklist Items	Recommendations
AC_SDOUT	Pulled up to VCC3_3 through a 10 KΩ resistor and a jumper to AC97 Connector and AC97 codec from ICH.
AC_SDIN0 AC_SDIN1	Pull down through a 10 KΩ resistor to GND. The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active – they should be pulled to ground through a weak (approximately 10k ohm) pull down resistor (see section 4.10.3 for more information).
AC97_OC#	Connects to OC# circuitry. (see CRB schematics page 20.
AC_XTAL_OUT, AC_XTAL_IN	Signal comes from Oscillator Y4 Decouple through a 22 pf cap to GND
PRI_DWN#	Connected through jumper to PRI_DWN_U or GND. (see CRB schematic page 27) If the motherboard implements an active primary codec on the motherboard and provides and AMR connector, it must tie PRI_DN# to GND.
PRI_DWN_U	Pull up through a 4.7 KΩ resistor to VCC3SBY
LINE_IN_R	From FB9 decouple through a 100 pf NPO cap to AGND. Run signal through 1uf TANT cap

12.12. PCI Checklist

Checklist Items	Recommendations
AD[31:0]	AD16,17 pass through 100 resistor.
ACK 64# REQ 64#	(5V PCI ENVIRONMENT) 2.7 KΩ (APPROXIMATE) PULL-UP RESISTORS TO VCC5. (3V PCI environment) 8.2 KΩ (approximate) pull-up resistors to VCC3_3. Each REQ 64# and ACK 64# requires it's own pull up.
PTCK	Pull down through 5.6 KΩ to GND Connect to PCI Connectors only.
PTDI, PTRST#, PTMS	Pull up through 5.6 KΩ resistor to Vcc5 Connect to PCI Connectors only.
PRSNT#21, PRSNT#22, PRSNT#31, PRSNT#32	Decoupled with 0.1 uf cap to GND
PIRQ#C, PIRQ#D, U2_ACK64#, U2_REQ64#, U3_ACK64#, U3_REQ64#, PREQ#1, PLOCK#1, STOP#, TRDY#, SERR#, PREQ#3, PIRQ#A, PERR#, PREQ#0, PREQ#2 DEVSEL#, FRAME#, IRDY#	Pull up through 2.7 KΩ resistor to Vcc5
PCIRST#	Pull signal down through 0.1 uf cap when input for USB. Input to buffer for PCIRST_BUF#.
PCPCI_REQ#A, REQ#B/GPIO1, GNT#B/GPIO17, PGNT#0, PGNT#1, PGNT#2, PGNT#3	Pull up through 8.2 KΩ resistor to Vcc3_3
PCLK_3	Signal coming from CK 815 device pass through a 33 Ω resistor to PCI connector.
PCIRST_BUF#	Signal comes from buffered PCIRST# Pull up through 8.2 KΩ resistor to Vcc3_3 Passes through 33 Ω resistor
SDONEP2, SDONEP3, SBOP2, SBOP3	Pull up through 5.6 KΩ resistor to Vcc5
R_RSTP#, R_RSTS#	Signal is from PCIRST_BUF# and passes through a 33 Ω resistor
IDSEL lines to PCI connectors	100 Ω series resistor.
3V_AUX	Optional to 3VSB, but required if PCI devices supporting wake up events.

12.13. LPC Checklist

Checklist Items	Recommendations
RCIN#	Pull up through 8.2 KΩ resistor to Vcc3_3
LPC_PME#	Pull up through 8.2 KΩ resistor to Vcc3_3. Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH0/ICH.
LPC_SMI#	Pull up through 8.2 KΩ resistor to Vcc3_3. This signal can be connected to any ICH0/ICH GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion.
TACH1, TACH2	Pull up through 4.7 KΩ resistor to Vcc3_3 Jumper for decoupling option(decouple with 0.1 uF cap).
J1BUTTON1, JPBUTTON2, J2BUTTON1, J2BUTTON2	Pull up through 1 KΩ resistor to Vcc5. Decouple through 47 pf cap to GND
LDRQ#1	Pull up through 4.7 KΩ resistor to Vcc3SBY
A20GATE	Pull up through 8.2 KΩ resistor to Vcc3_3
MCLK, MDAT	Pull up through 4.7 KΩ resistor to PS2V5.
L_MCLK, L_MDAT	Decoupled using 470 pF to ground
RI#1_C, CTS0_C, RXD#1_C, RXD0_C, RI0_C, DCD#1_C, DSR#1_C, DSR0_C, DTR#1_C, DTR0_C, DCD0_C, RTS#1_C, RTS0_C, CTS#1_C, TXD#1_C, TXD0_C	Decoupled using 100 pF to GND
L_SMBD	Pass through 150 Ω resistor to 82559
SERIRQ	Pull up through 8.2 KΩ to Vcc3_3
SLCT#, PE, BUSY, ACK#, ERROR#	Pull up through 2.2 KΩ resistor to Vcc5_DB25_DR Decouple through 180 pf to GND
LDRQ#0	Connect to ICH from SIO. This signal is actively driven by the Super I/O and does not require a pull up resistor.
STROBE#, ALF#, SLCTIN#, PAR_INIT#	Signal passes through a 33 Ω resistor and is pulled up through 2.2 KΩ resistor to Vcc5_DB25_CR. Decoupled using a180 pF cap to GND.
PWM1, PWM2	Pull up to 4.7 KΩ to Vcc3_3 and connected to jumper for decouple with 0.1 uF cap to GND.
INDEX#, TRK#0, RDATA#, DSKCHG#, WRTPRT#	Pull up through 1 KΩ resistor to Vcc5
PDR0, PDR1, PDR2, PDR3, PDR4, PDR5, PDR6, PDR7	Passes through 33 Ω resistor Pull up through 2.2 KΩ to Vcc5_DB5_CRDecouple through 180 pf cap to GND
SYSOPT	Pull down with 4.7 KΩ resistor to GND or IO address of 0x02E

12.14. System Checklist

Checklist Items	Recommendations
KEYLOCK#	Pull up through 10 KΩ resistor to Vcc3_3
PBTN_IN	Connects to PBSwitch and PBin.
PWRLED	Pull up through a 220 Ω resistor to Vcc5
R_IRTX	Signal IRTX after it is pulled down through4.7 KΩ resistor to GND and passes through 82 Ω resistor
IRRX	Pull up to 100 KΩ resistor to Vcc3_3 When signal is input for SI/O Decouple through 470 pf cap to GND
IRTX	Pull down through 4.7 KΩ to GND Signal passes through 82 Ω resistor When signal is input to SI/O Decouple through 470 pf cap to GND
FP_PD	Decouple through a 470 pf cap. To GND Pull up 470 Ω to Vcc5
PWM1, PWM2	Pull up through a 4.7 KΩ resistor to Vcc3_3

12.15. FWH Checklist

Checklist Items	Recommendations
No floating inputs	Unused FGPI pins need to be tied to a valid logic level.
WPROT, TBLK_LCK	PULL UP THROUGH A 4.7 KΩ TO VCC3_3
R_VPP	Pulled up to Vcc3_3, decoupled with two 0.1 uF caps to GND.
FGPI0_PD, FGPI1_PD, FGPI2_PD, FPGI3_PD, FPGI4_PD, IC_PD	Pull down through a 8.2 KΩ resistor to GND
FWH_ID1, FWH_ID2, FWH_ID3	Pull down to GND
INIT#	FWH INIT# must be connected to processor INIT#.
RST#	FWH RST# must be connected to PCIRST#.
ID[3:0]	For a system with only one FWH device, tie ID[3:0] to ground.

12.16. Clock Synthesizer Checklist

Checklist Items	Recommendations
REFCLK	Connects to R-RefCLK, USB_CLK, SIO_CLK14, and ICHCLK14.
GMCH_3V66/3V66_1	Passes through 33 Ω resistor
ICH_3V66/3V66_0, DOTCLK	Passes through 33 Ω resistor When signal is input for ICH it is pulled down through a 18 pf cap to GND
DCLK/DCLK_WR	Passes through 33 Ω resistor When signal is input for GMCH it is pulled down through a 22 pf cap to GND
CPUHCLK/CPU_0_1	Passes through 33 Ω resistor When signal is input for 370PGA, Decouple through a 18 pf cap to GND
R_REFCLK	REFCLK passed through 10 KΩ resistor When signal is input for 370PGA, pull up through 1 KΩ resistor to Vcc3_3 and pass through 10 KΩ resistor
USB_CLK, ICH_CLK14	REFCLK passed through 10 Ω resistor
XTAL_IN, XTAL_OUT	Passes through 14.318 MHz Osc Pulled down through 18 pf cap to GND
SEL1_PU	Pulled up via MEMV3 circuitry through 8.2 KΩ resistor.
FREQSEL	Connected to clock frequency selection circuitry through 10 KΩ resistor. (see CRB schematic, page 4)
L_VCC2_5	Connects to VDD2_5[0..1] through ferrite bead to Vcc2_5.
GMCHHCLK/CPU_1, ITPCLK/CPU_2, PCI_0/PCLK_OICH, PCI_1/PCLK_1, PCI_2/PCLK_2, PCI_3/PCLK_3, PCI_4/PCLK_4, PCI_5/PCLK_5, PCI_6/PCLK_6, APICCLK_CPU/APIC_0, APICCLK)ICH/APIC_1, USBCLK/USB_0, GMCH_3V66/3V66_1, AGPCLK_CONN	Passes through 33 Ω resistor
MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7, SCLK	Pass through 22 Ω resistor

12.17. LAN Checklist

Checklist Items	Recommendations
TDP, TDN, RDP, RDN	Pull down through 50 Ω resistor to GND
LANAPWR	Passes through 3 KΩ resistor
LANCLKRUN	Pull down through 62 KΩ resistor
LAN_ISOLATE#	Connect to SUS_STAT# and PWROK
LAN_TEST	Pull down through a 4.7 KΩ resistor to GND
LAN_XTAL1, LAN_XTAL2	Signal from 25 MHz oscillator Decouple through a 22 pf cap to GND
FLD5_PD, FLD6_PD, RBIAS10, RBIAS100	Pull down through a 619 Ω resistor to GND
ACTLED/LI_CR	Passes through 330 Ω resistor
LILED	Connect to jumper, pull up through 330 Ω resistor to VCC3SBY
ACT_CR	Pull up through 330 Ω resistor to Vcc3SBY
RD_PD	Pull down RDP through 50 Ω resistor and to RDN through 50 Ω resistor to GND
TD_PD	Pull down TDP through 50 Ω resistor and to TDN through 50 Ω resistor to GND
SPEEDLED	Connect LED anode to VCC3SBY through 330 Ω resistor and cathode to 82559. Jumper to VCC3SBY through 330 resistor.
CHASSIS_GND	Use plane for this signal.
JP7_PU, JP18_PU, JP23_PU	Pull up through 330 Ω resistor to Vcc3SBY
R_LANIDS	Pass through 100 Ω resistor to AD20 from 82559 pin IDSEL.

12.18. ITP Probe Checklist

Checklist Items	Recommendations
When ITP is not used…	Test port pins should not be left floating when not implemented. Use a 10 KΩ pull up to VCMOS. Leaving these pins floating may cause unexpected results.
R_TCK, TCK R_TMS, TMS	Connect to 370-Pin Socket through 47 Ω resistor, pull up to VCMOS.
ITPRDY#, R_ITPRDY#	Connect to 370-Pin Socket through 243 Ω resistor.
TDI	Pull up through 330 Ω resistor to VCMOS
TDO	Pull up through 150 Ω resistor to VCMOS
PLL1	See Design Guide.
PLL2	See Design Guide.

12.19. System Memory Checklist

Checklist Items	Recommendations
SM_CSA#[0:3, SM_CSB#[3:0, SMAA[11:8,3:0], SM_MD[0:63], SM_CKE[0:3], S_DQM[0:7]	Connect from GMCH to DIMM0, DIMM1
SM_MAA[7:4], SM_MAB[7:4]#	Connect from GMCH to DIMM0, DIMM1 through 10 ohm resistors
SM_CAS#	Connected to R_REFCLK through 10 KΩ resistor.
SM_RAS#	Jumpered to GND through 10 KΩ resistor
SM_WE#	Connected to R_BSEL0# through 10 KΩ resistor.
CKE[5..0] (For 3 DIMM implementation)	When implementing a 3 DIMM configuration, all six CKE signals on the GMCH are used. (0,1 for DIMM0; 2, 3 for DIMM1; 4,5 for DIMM2)
REGE	Connect to GND(since 815 C/S does not support registered DIMMS).
WP(Pin 81 on the DIMMS)	Add a 4.7 KΩ ohm pull up resistor to 3.3V. This is a recommendation to write-protect the DIMM's EEPROM.
SRCOMP	Needs a 40 KΩ resistor pulled up to 3.3V

12.20. Power Delivery Checklist

Checklist Items	Recommendations
All voltage regulator components meet maximum current requirements	Consider all loads on a regulator, including other regulators.
All regulator components meet thermal requirements	Ensure the voltage regulator components and dissipate the required amount of heat.
VCC1_8	VCC1_8 power sources must supply 1.85 V
If devices are powered directly from a dual rail (i.e. not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET.	"Dual" voltage rails may not be at the expected voltage.
Dropout Voltage	The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage.
Voltage tolerance requirements are met	See individual component specifications for each voltage tolerance.
Total power consumption in S3 must be less than the rated standby supply current	Adequate power must be supplied by power supply.

13. Third-Party Vendor Information

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the Intel® 815 chipset. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

Super I/O (Vendors Contact Phone)

- SMSC — Dave Jenoff (909) 244-4937
- National Semiconductor — Robert Reneau (408) 721-2981
- ITE — Don Gardenhire (512)388-7880
- Winbond — James Chen (02) 27190505 - Taipei office

Clock Generation (Vendors Contact Phone)

- Cypress Semiconductor — John Wunner 206-821-9202 x325
- ICS — Raju Shah 408-925-9493
- IMI — Elie Ayache 408-263-6300, x235
- PERICOM — Ken Buntaran 408-435-1000

Memory Vendors

http://developer.intel.com/design/motherbd/se/se_mem.htm

Voltage Regulator Vendors (Vendors Contact Phone)

- Linear Tech Corp. — Stuart Washino 408-432-6326
- Celestica — Dariusz Basarab 416-448-5841
- Corsair Microsystems — John Beekley 888-222-4346
- Delta Electronics — Colin Weng 886-2-6988, x233(Taiwan)
- N. America: Delta Products Corp. — Maurice Lee 510-770-0660, x111

Flat Panel (Vendors Contact Phone)

- Silicon Images Inc — Vic Dacosta 408-873-3111

GPA (a.k.a. AIMM) Card (Vendors Contact Phone)

- Kingston — TBD
- Smart Modular — TBD
- Micron Semiconductor — TBD

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Appendix A: Customer Reference Board (CRB)

This appendix provides a set of schematics for the Intel® 815 chipset's Customer Reference Board (CRB).

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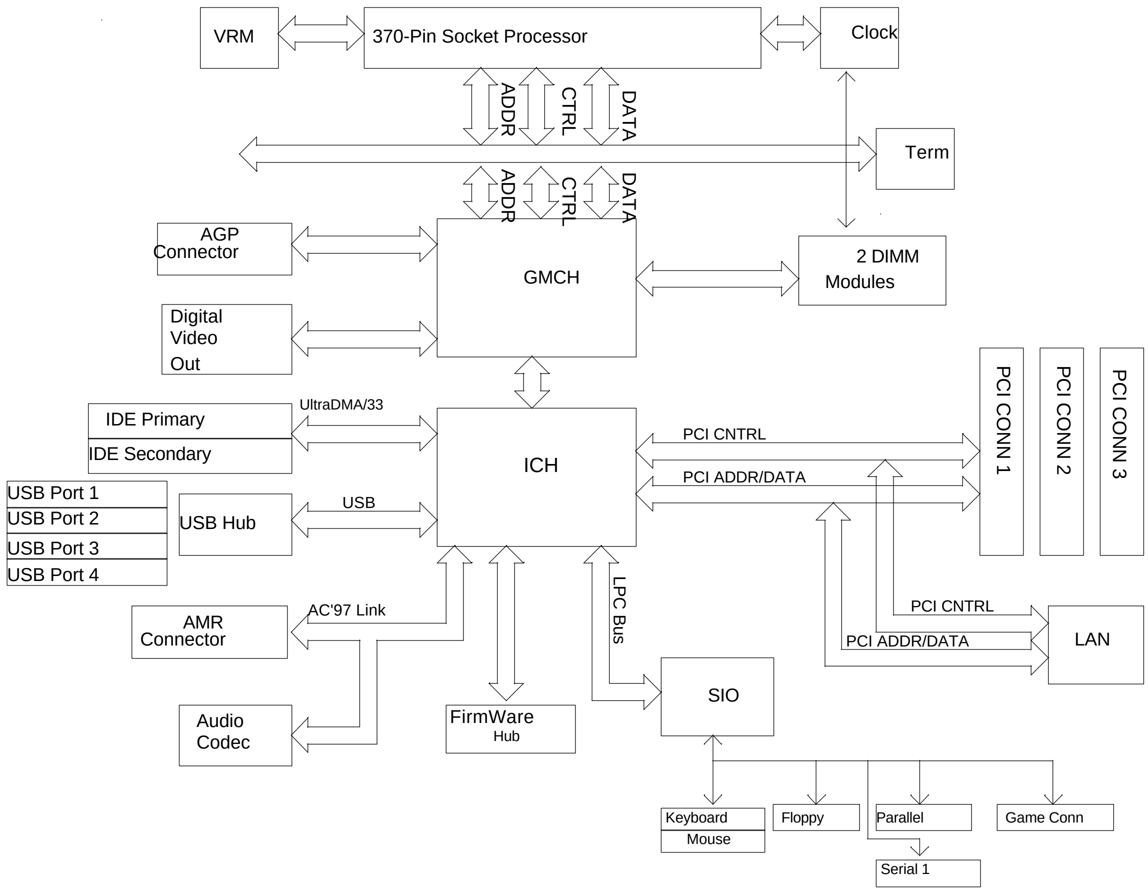
INTEL(R) PENTIUM(R) III & INTEL(R) CELERON(TM) PROCESSOR/INTEL(R) 82815 CHIPSET UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS

REVISION 1.0

** PLEASE NOTE THESE SCHEMATICS ARE SUBJECT TO CHANGE

INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD COVER SHEET			REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG	LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 1 OF 41

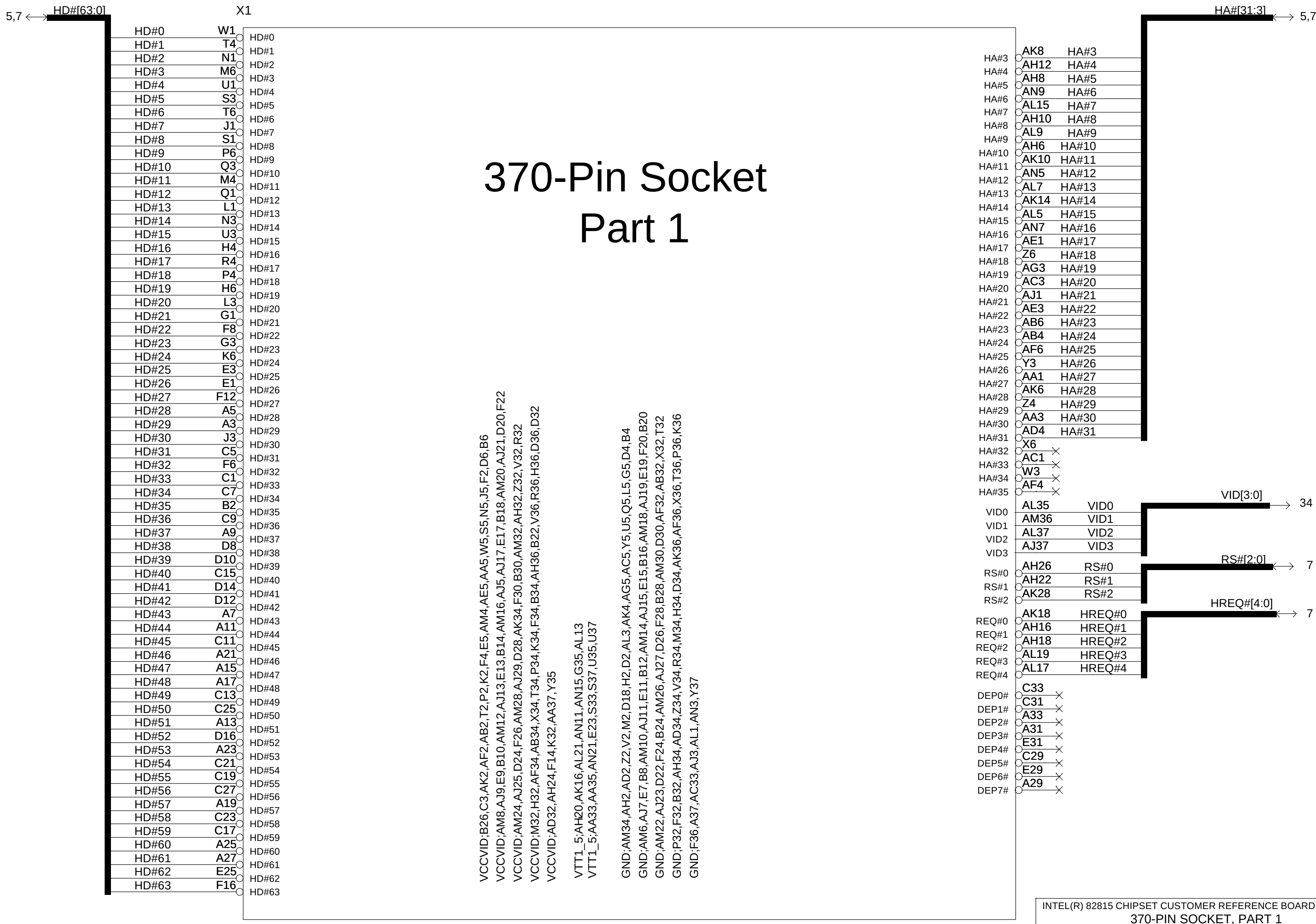
Block Diagram



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
BLOCK DIAGRAM

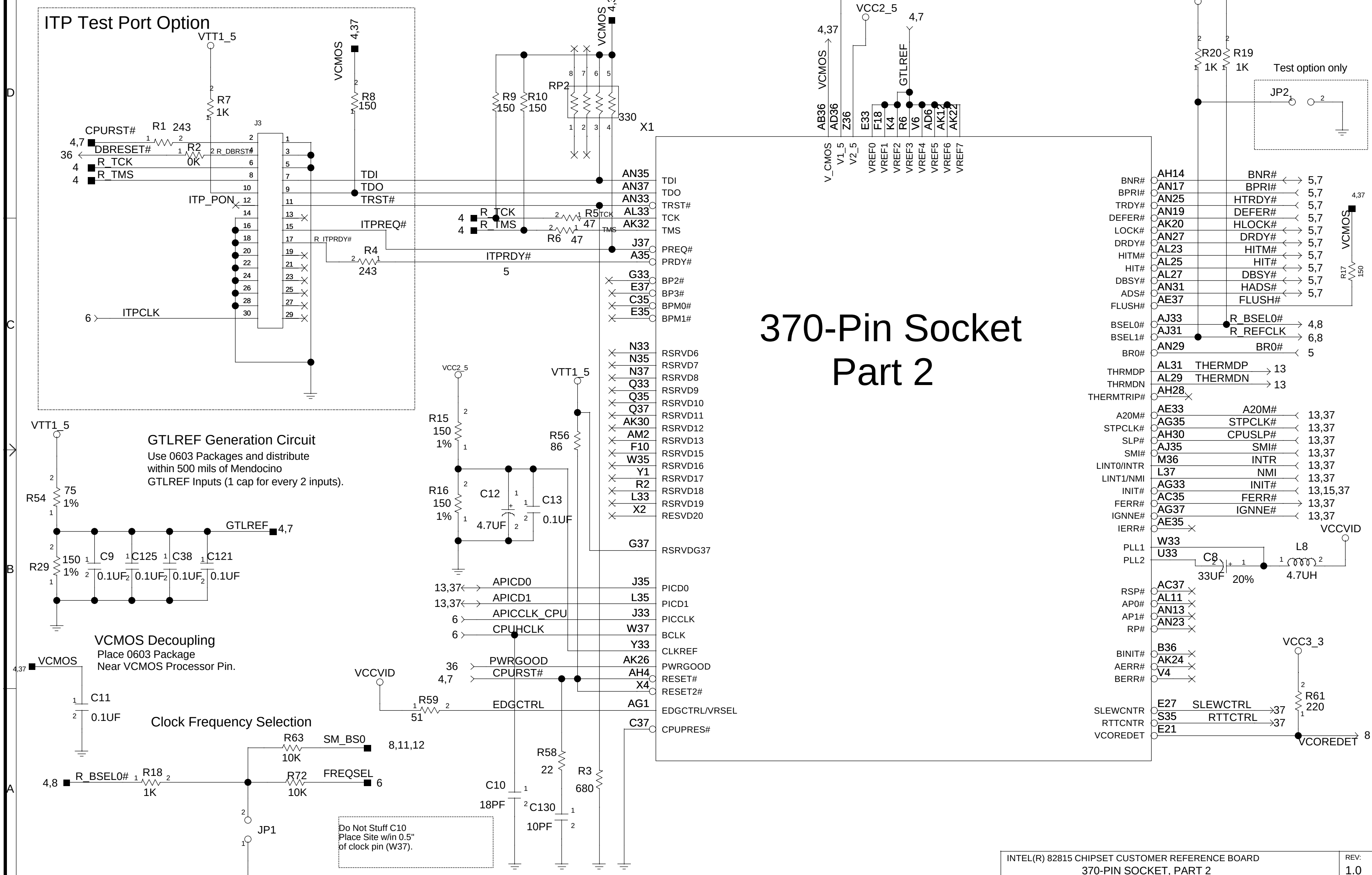
REV: 1.0	DRAWN BY: INTEL (R) PCG	PROJECT: INTEL(R) 82815
PCG PLATFORM DESIGN, 1900 PRAIRIE CITY RD, FOLSOM, CA 95630	LAST REVISED: 5-15-00	SHEET: 2 OF 41

370PGA Socket Part1



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD 370-PIN SOCKET, PART 1		REV: 1.0
intel © PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 3 OF 41

370PGA Socket Part 2



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD

370-PIN SOCKET, PART 2

REV: 1.0

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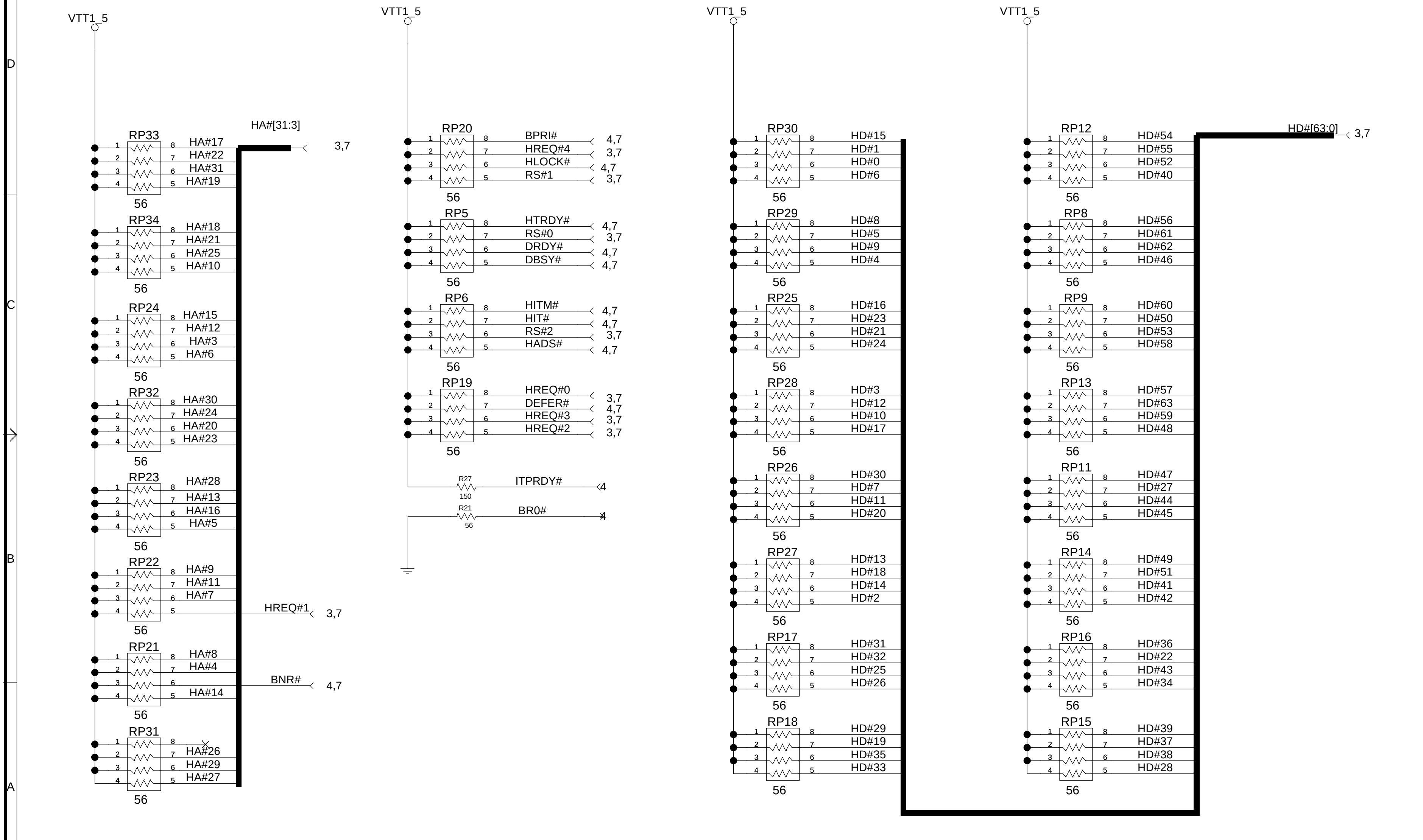
SHEET: 4 OF 41

AGTL Termination



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD

AGTL TERMINATION

REV: 1.0

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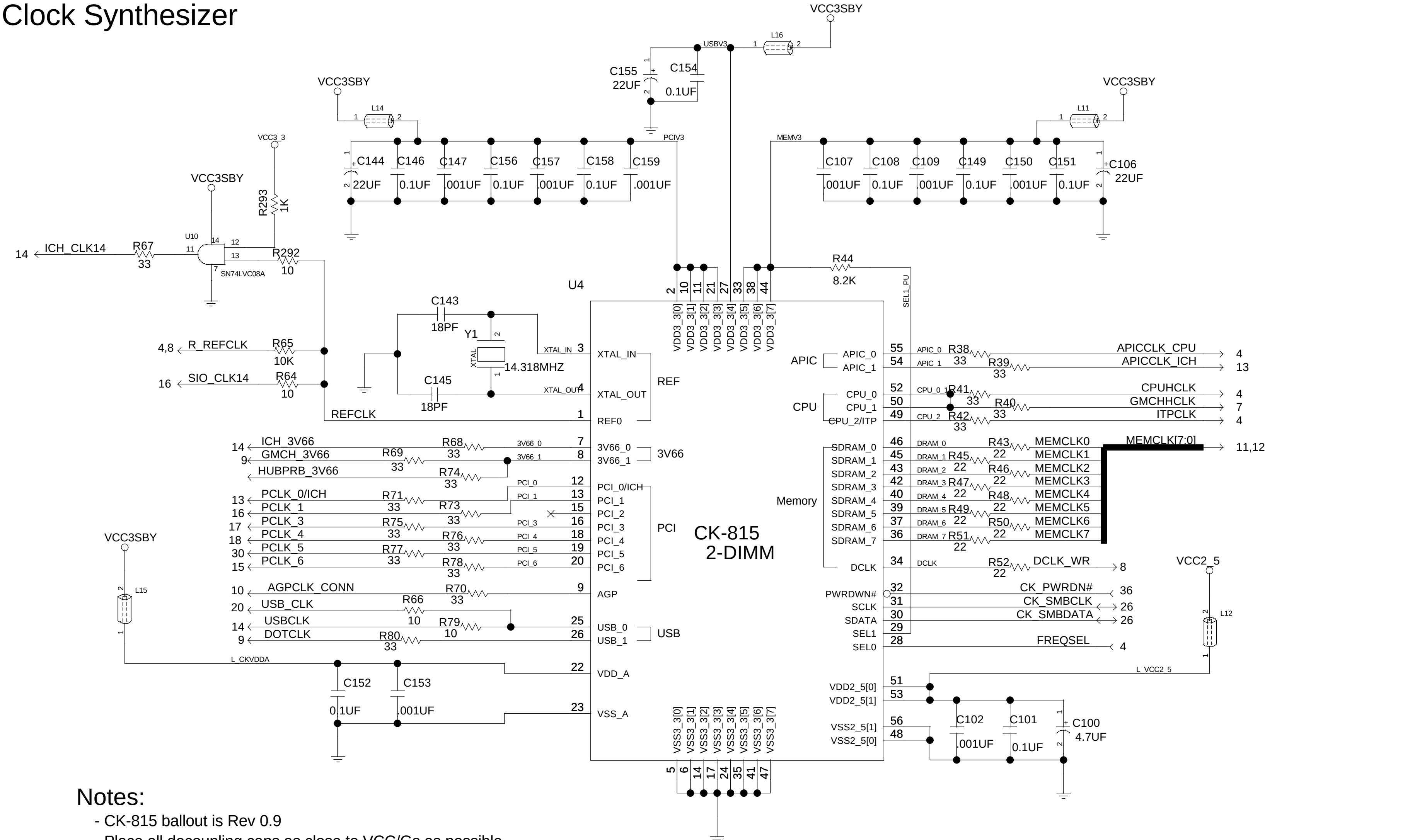
SHEET: 5 OF 38

Clock Synthesizer

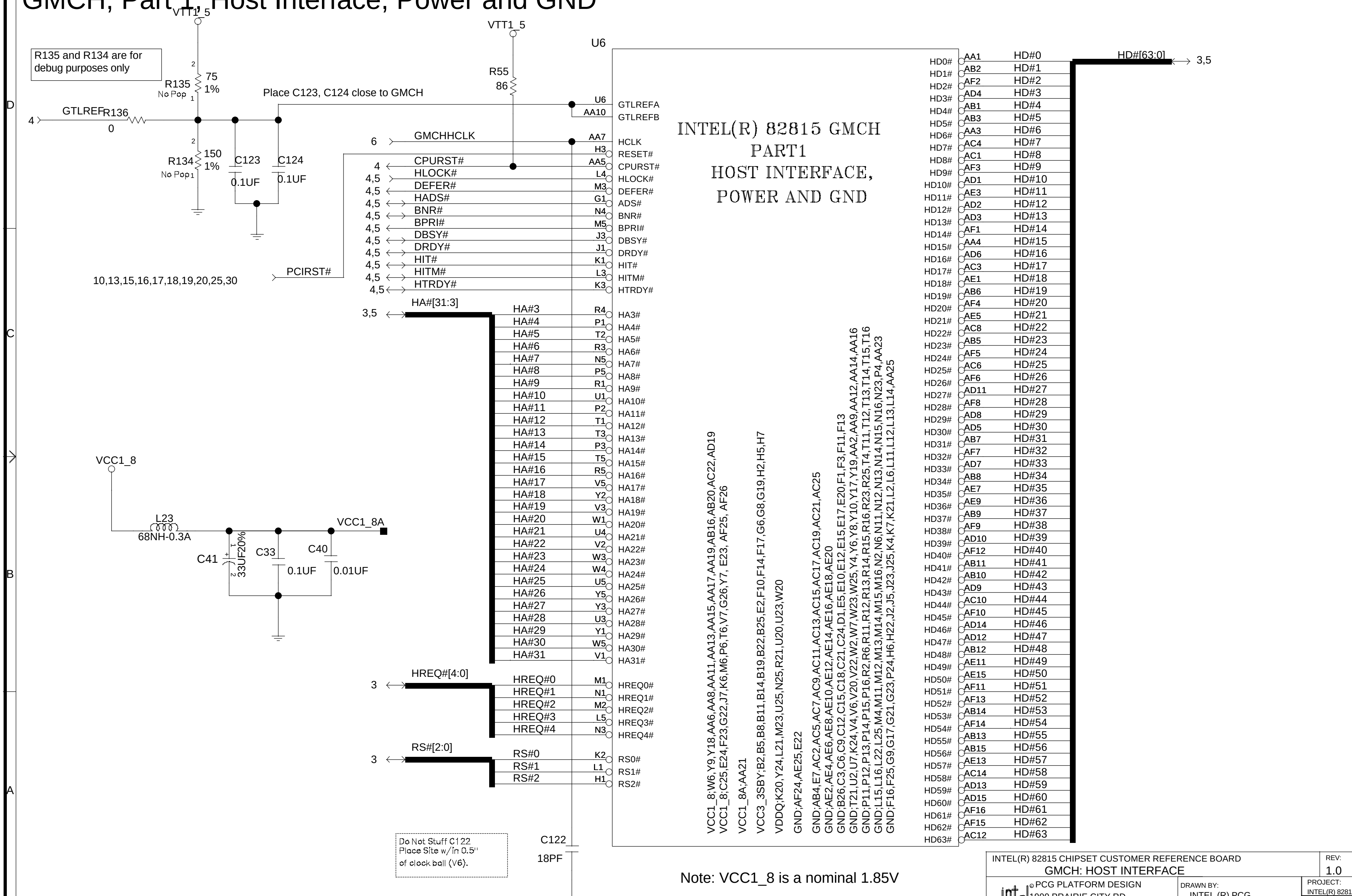


Notes:

- CK-815 ballout is Rev 0.9
- Place all decoupling caps as close to VCC/Gs as possible
- PCI_0/ICH pin has to go to the ICH.
  (This clock cannot be turned off through SMBus)
- CPU_ITP pin has to go to the ITP. It is the only
  CPU CLK that can be shut off through the SMBUS interface.

INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD CLOCK SYNTHESIZER		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 6 OF 41

GMCH, Part 1; Host Interface, Power and GND



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD

GMCH: HOST INTERFACE

REV: 1.0

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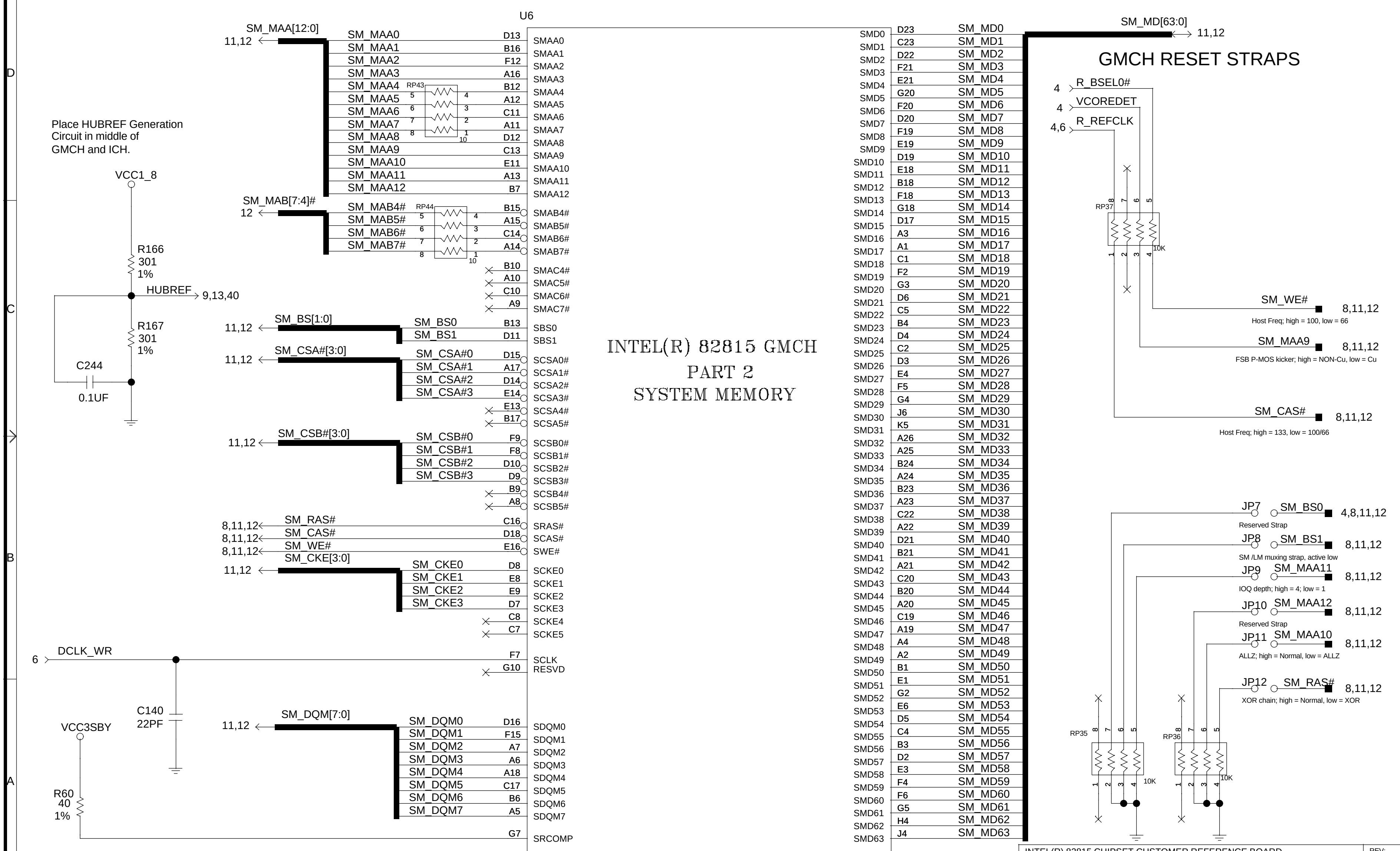
SHEET: 7 OF 41

GMCH, Part 2; Memory Interface



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
GMCH: SYSTEM MEMORY

REV: 1.0

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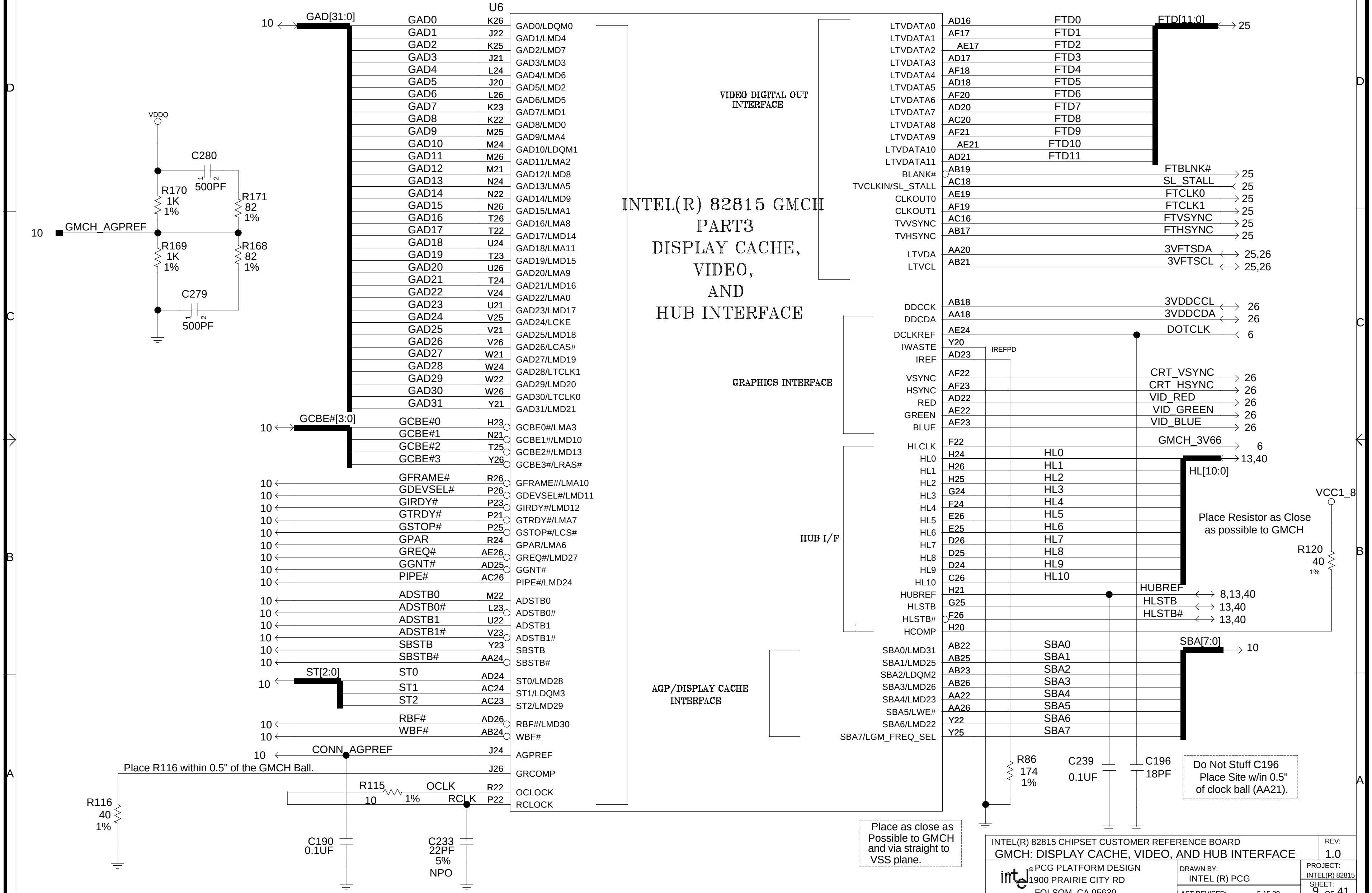
PROJECT: INTEL(R) 82815
SHEET: 8 OF 41

GMCH, Part 3; AGP/Display Cache, and Video Interface



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
GMCH: DISPLAY CACHE, VIDEO, AND HUB INTERFACE
REV: 1.0
intel © PCG PLATFORM DESIGN, 1900 PRAIRIE CITY RD, FOLSOM, CA 95630
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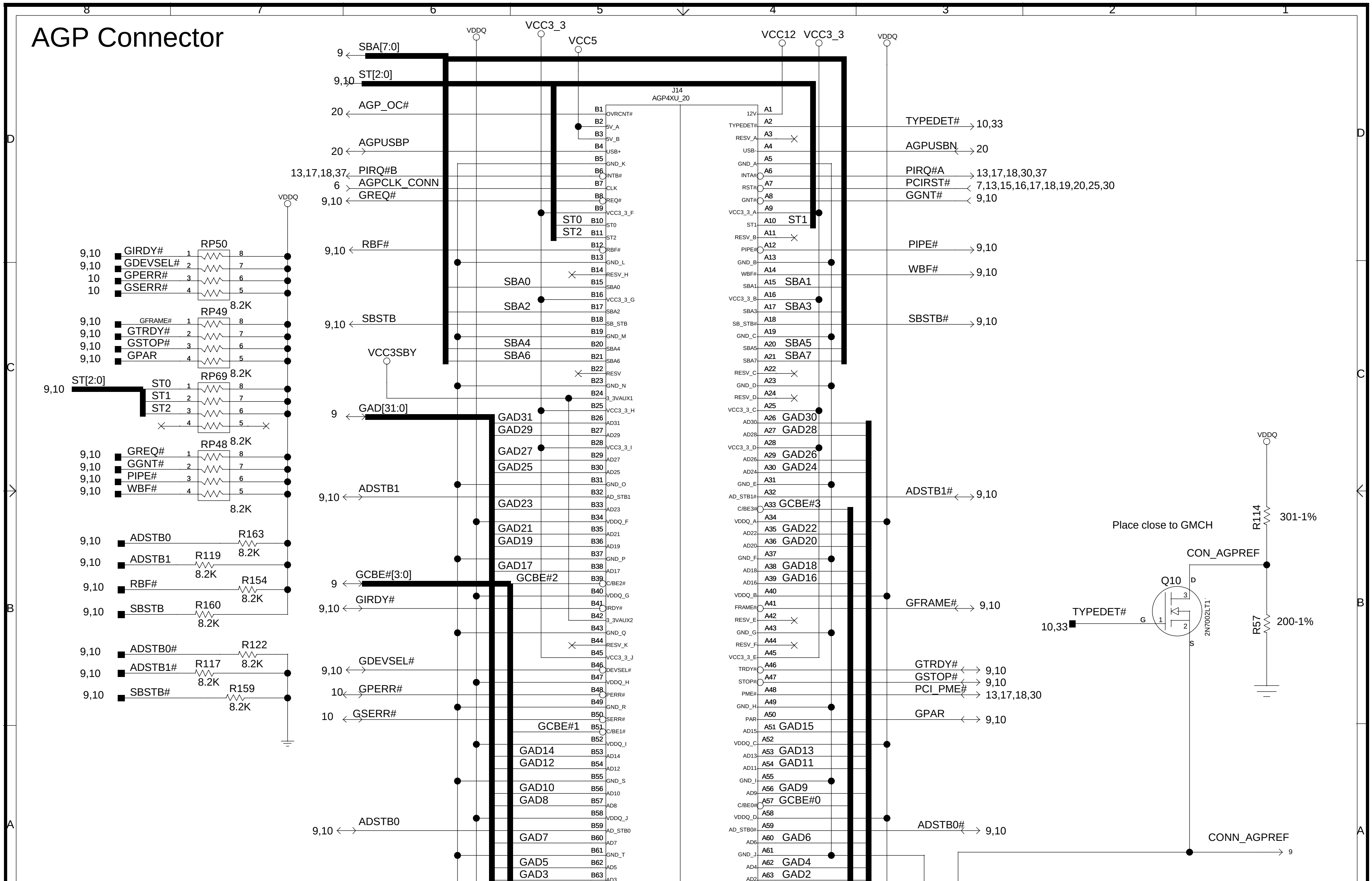
LAST REVISED: 5-15-00
PROJECT: INTEL(R) 82815
SHEET: 9 OF 41

AGP Connector



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
AGP CONNECTOR
REV: 1.0

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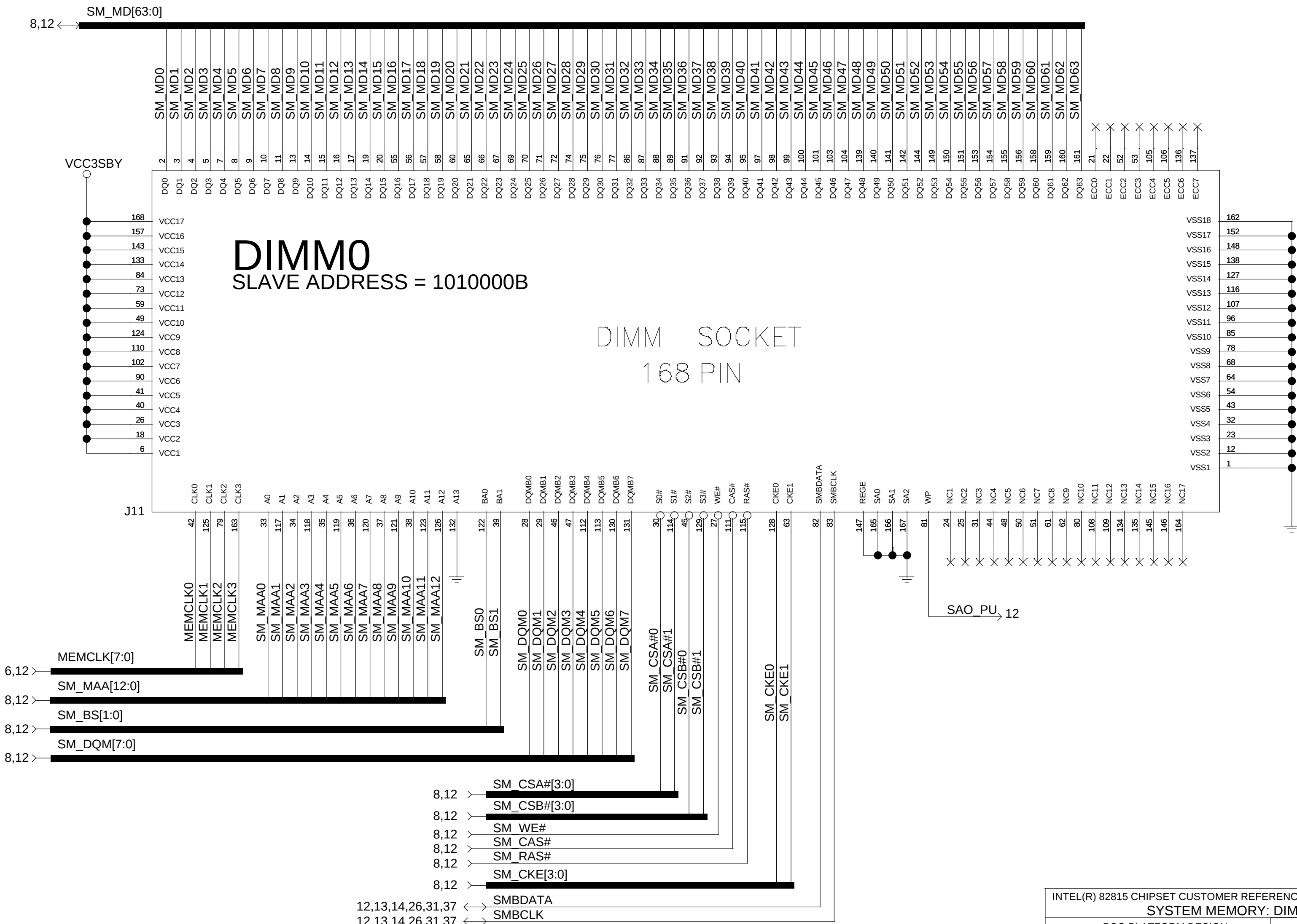
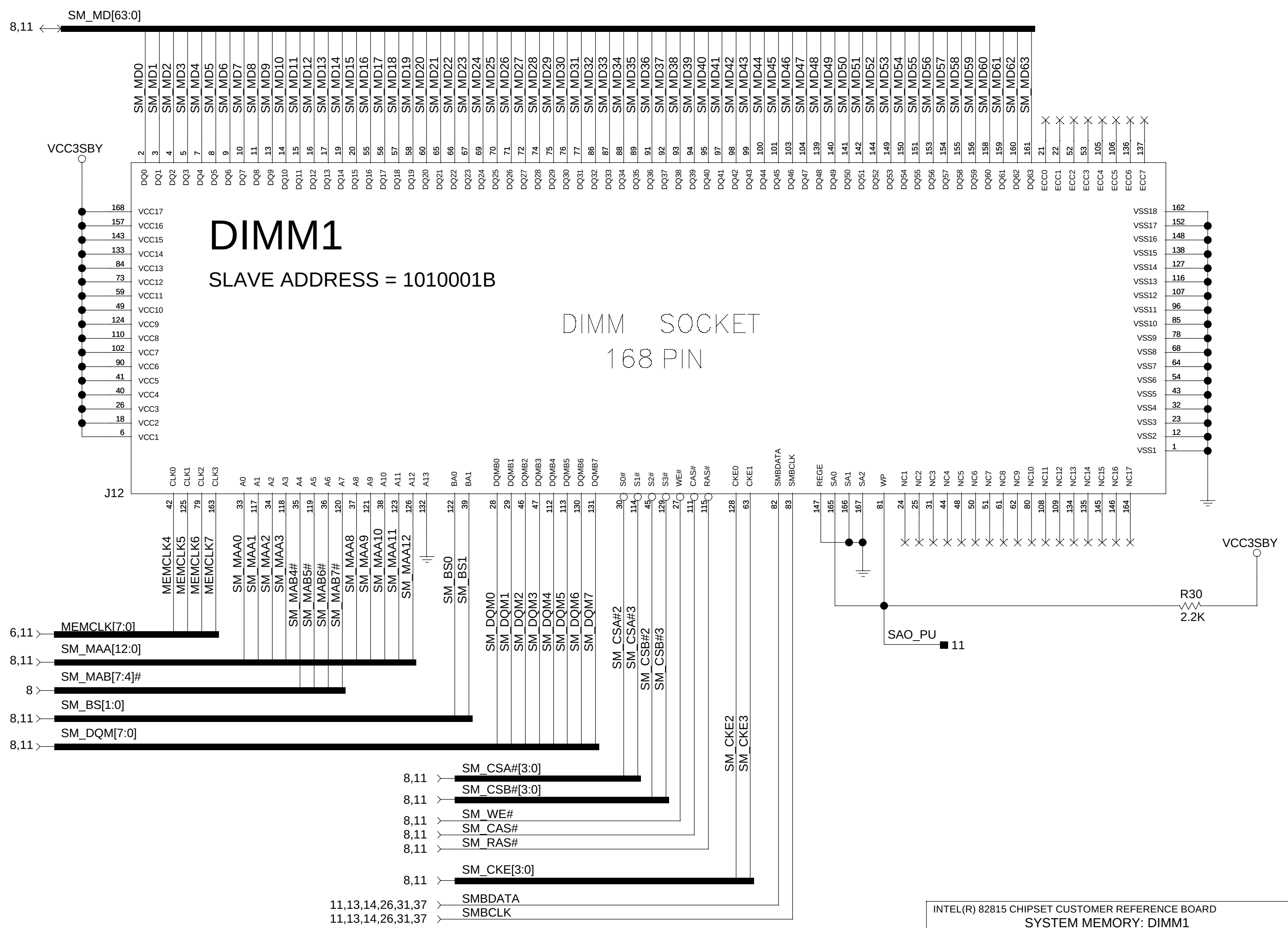
PROJECT: INTEL(R) 82815
SHEET: 10 OF 41

System Memory



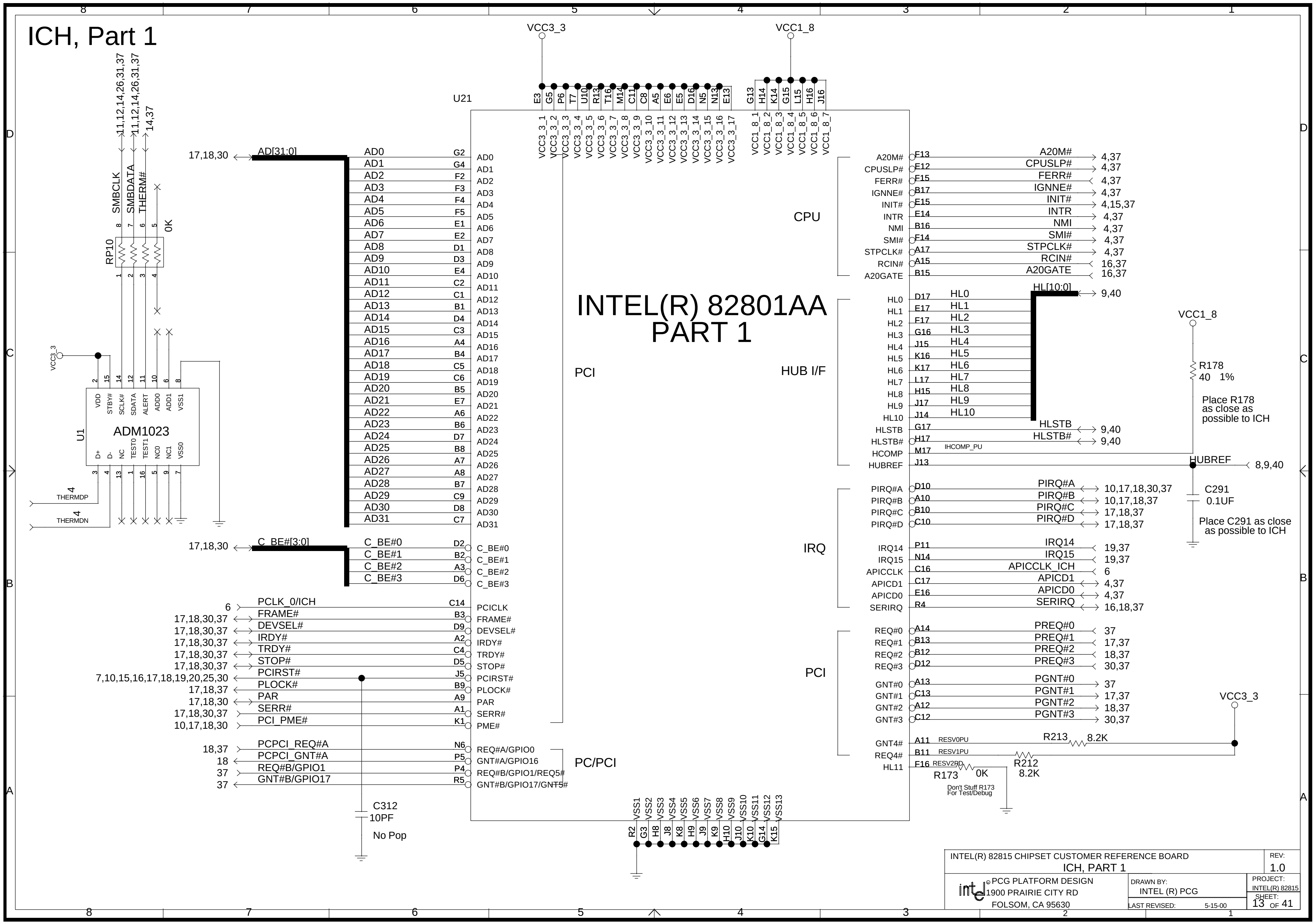
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD SYSTEM MEMORY: DIMM0		REV: 1.0
intel © PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 11 OF 41

System Memory



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD		REV:
SYSTEM MEMORY: DIMM1		1.0
PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG	PROJECT: INTEL(R) 82815
	LAST REVISED: 5-15-00	SHEET: 12 OF 41

ICH, Part 1


ICH, Part 1
U21
INTEL(R) 82801AA
PART 1
VCC3_3
VCC1_8
PCI
HUB I/F
CPU
IRQ
PC/PCI
AD[31:0]
17,18,30
C_BE#[3:0]
PCLK_0/ICH
FRAME#
DEVSEL#
IRDY#
TRDY#
STOP#
PCIRST#
PLOCK#
PAR
SERR#
PCI_PME#
PCPCI_REQ#A
PCPCI_GNT#A
REQ#B/GPIO1
GNT#B/GPIO17
7,10,15,16,17,18,19,20,25,30
C312
10PF
No Pop
A20M#
CPUSLP#
FERR#
IGNNE#
INIT#
INTR
NMI
SMI#
STPCLK#
RCIN#
A20GATE
HL[10:0]
HLSTB
HLSTB#
HCOMP
HUBREF
IHCOMP_PU
R178
40 1%
Place R178
as close as
possible to ICH
C291
0.1UF
Place C291 as close
as possible to ICH
PIRQ#A
PIRQ#B
PIRQ#C
PIRQ#D
IRQ14
IRQ15
APICCLK_ICH
APICD1
APICD0
SERIRQ
PREQ#0
PREQ#1
PREQ#2
PREQ#3
PGNT#0
PGNT#1
PGNT#2
PGNT#3
GNT4#
REQ4#
HL11
RESV0PU
RESV1PU
RESV2PD
R213
8.2K
R212
8.2K
R173
0K
Don't Stuff R173
For Test/Debug
U1
ADM1023
RP10
0K
SMBCLK
SMBDATA
THERM#
11,12,14,26,31,37
14,37
THERMDP
THERMDN
VDD
STBY#
SCLK#
SDATA
ALERT
ADD0
ADD1
VSS1
D+
D-
NC
TEST0
TEST1
NC0
NC1
VSS0
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
ICH, PART 1
REV:
1.0
PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
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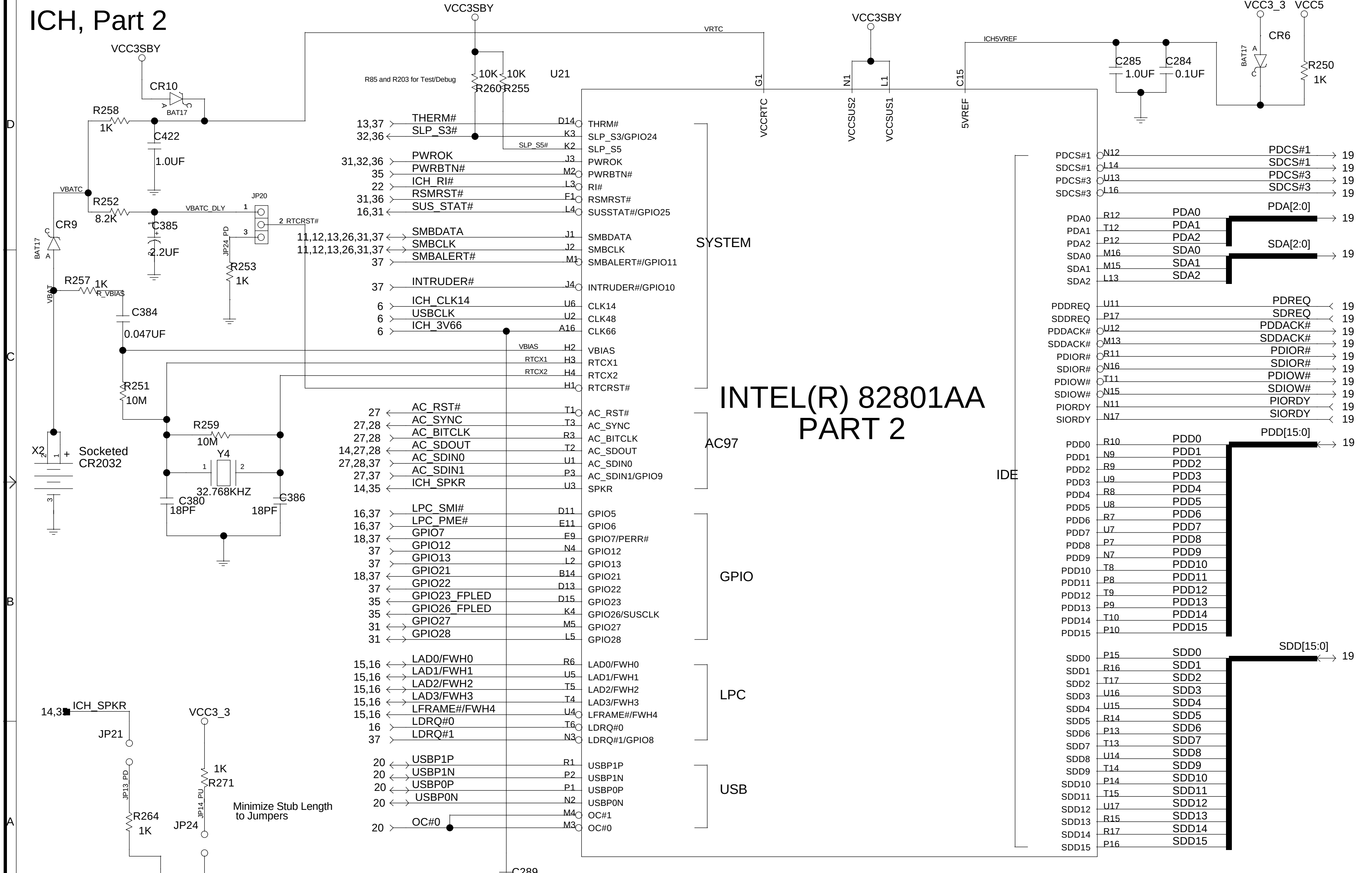
PROJECT:
INTEL(R) 82815
LAST REVISED:
5-15-00
SHEET:
13 OF 41

ICH, Part 2



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
ICH, PART 2

REV: 1.0

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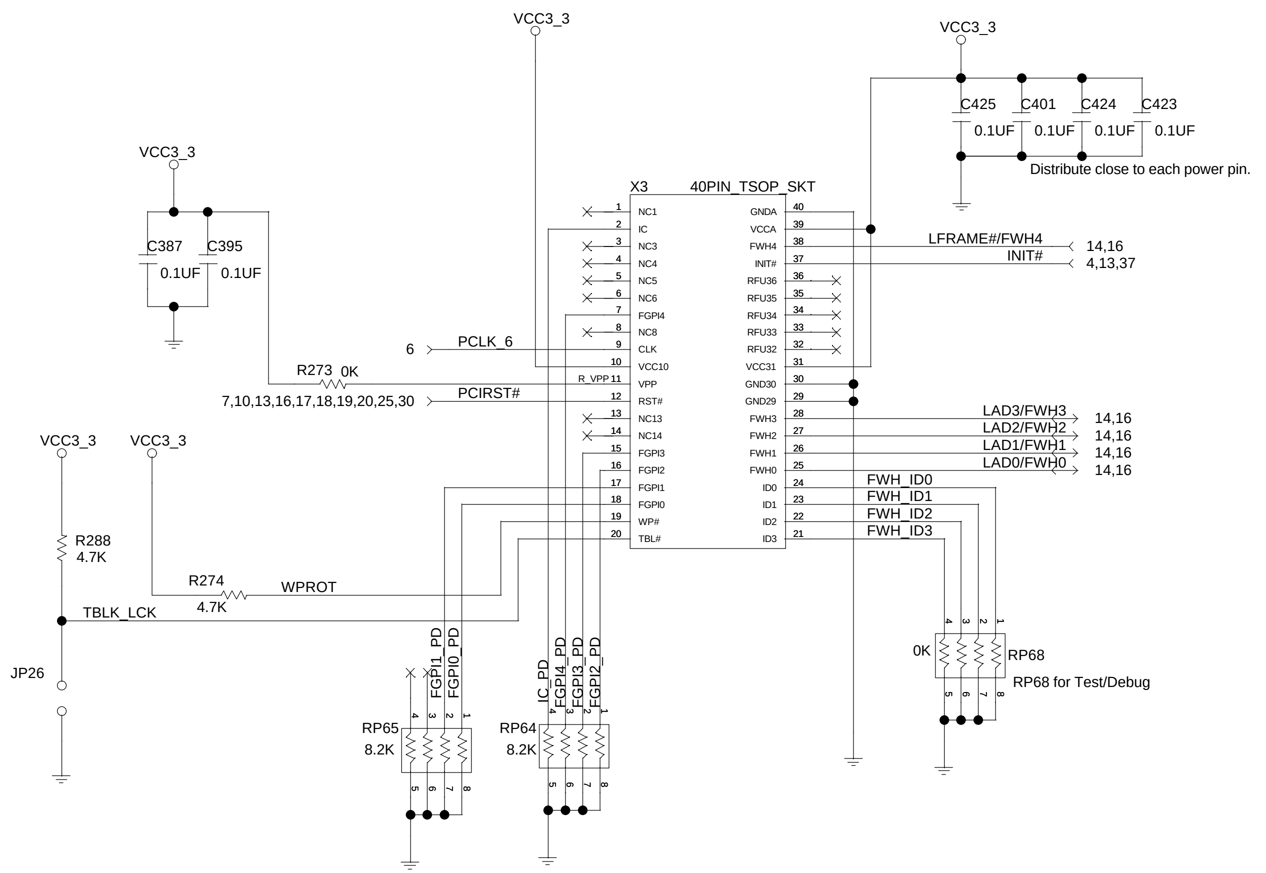
PROJECT: INTEL(R) 82815

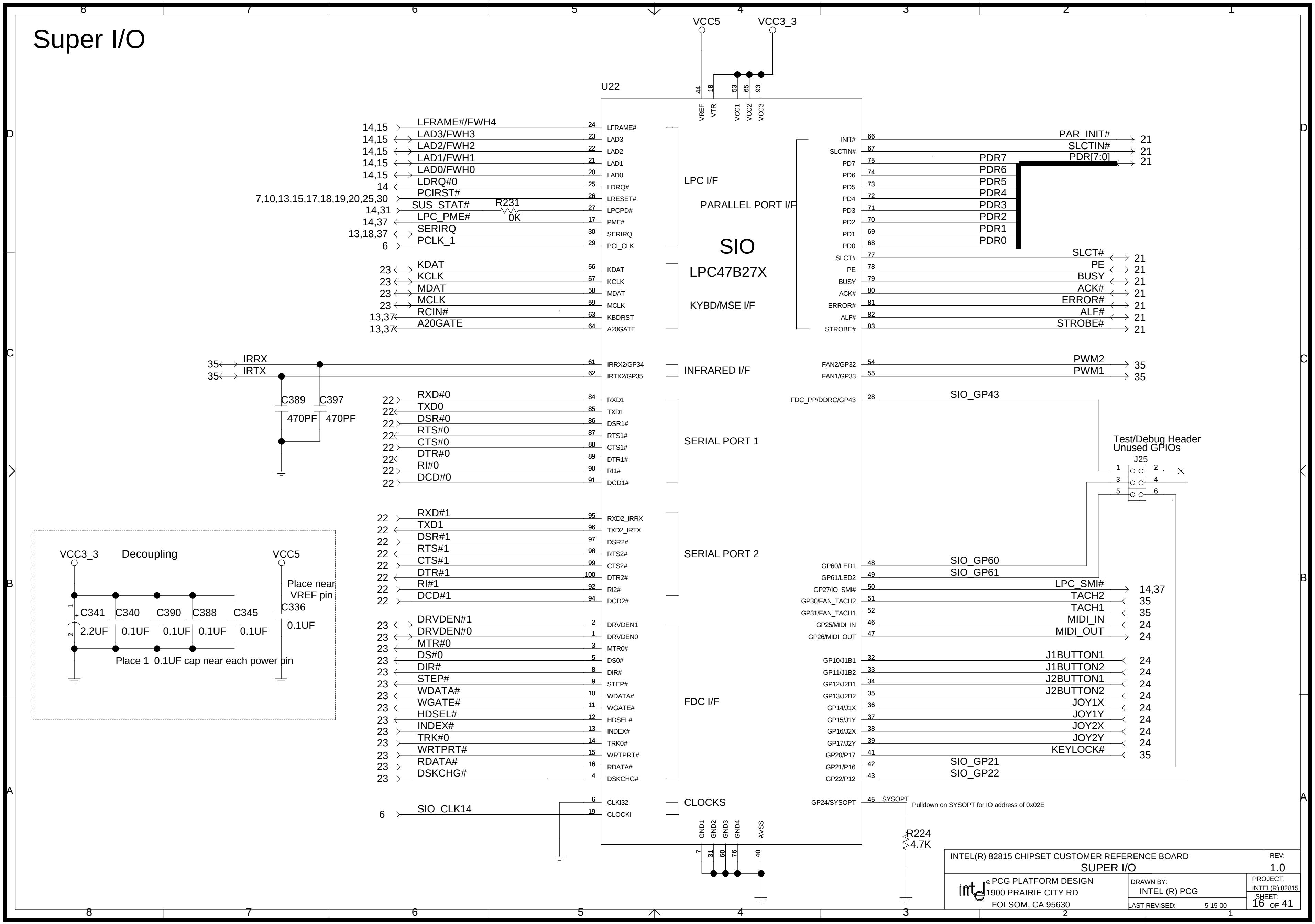
SHEET: 14 OF 41

FirmWare Hub (FWH) Socket

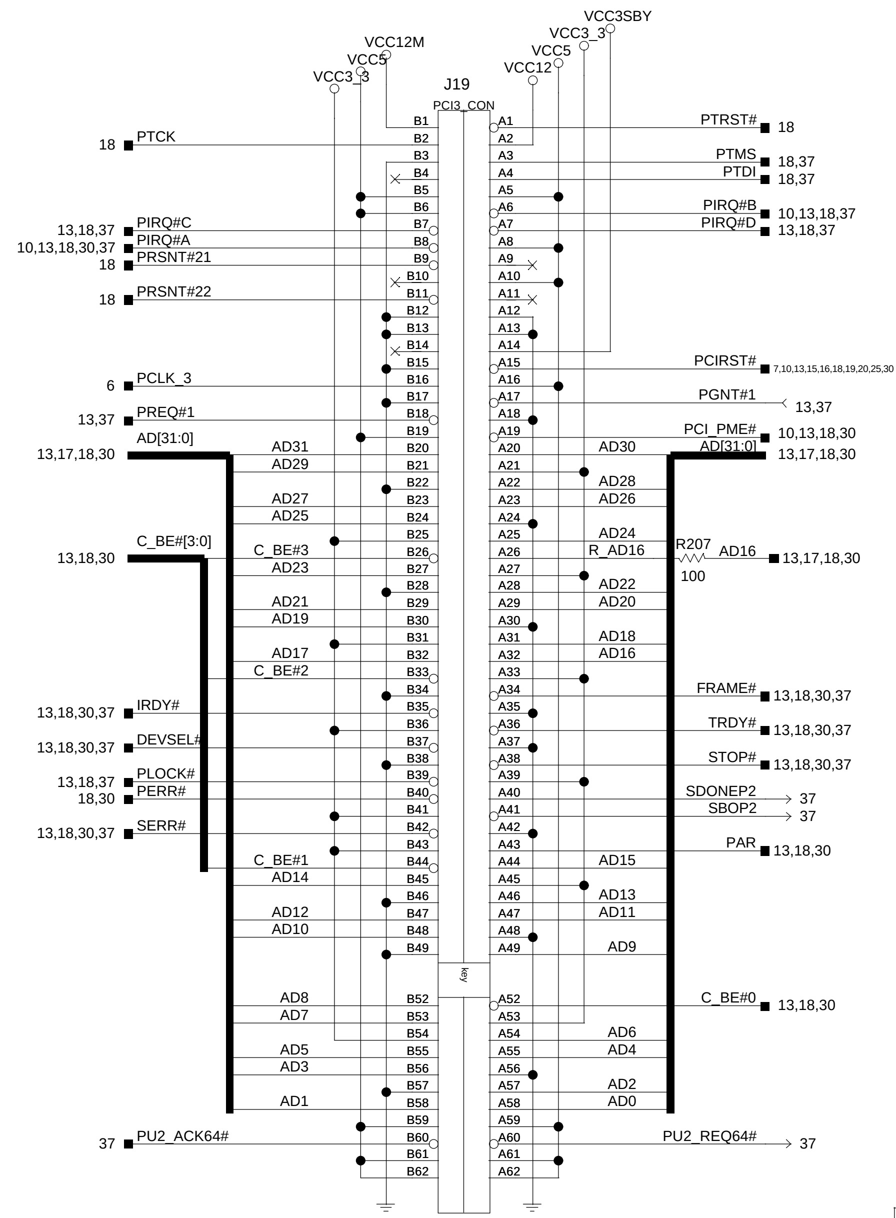
NOTE: This is a TSOP Implementation



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD FIRMWARE HUB (FWH)		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 15 OF 41


Super I/O
VCC5
VCC3_3
U22
SIO
LPC47B27X
LPC I/F
PARALLEL PORT I/F
KYBD/MSE I/F
INFRARED I/F
SERIAL PORT 1
SERIAL PORT 2
FDC I/F
CLOCKS
LFRAME#/FWH4
LAD3/FWH3
LAD2/FWH2
LAD1/FWH1
LAD0/FWH0
LDRQ#0
PCIRST#
SUS_STAT#
LPC_PME#
SERIRQ
PCLK_1
R231
0K
7,10,13,15,17,18,19,20,25,30
KDAT
KCLK
MDAT
MCLK
RCIN#
A20GATE
IRRX
IRTX
C389
C397
470PF
470PF
RXD#0
TXD0
DSR#0
RTS#0
CTS#0
DTR#0
RI#0
DCD#0
RXD#1
TXD1
DSR#1
RTS#1
CTS#1
DTR#1
RI#1
DCD#1
DRVDEN#1
DRVDEN#0
MTR#0
DS#0
DIR#
STEP#
WDATA#
WGATE#
HDSEL#
INDEX#
TRK#0
WRTPRT#
RDATA#
DSKCHG#
SIO_CLK14
Decoupling
VCC3_3
VCC5
C341
C340
C390
C388
C345
C336
2.2UF
0.1UF
0.1UF
0.1UF
0.1UF
0.1UF
Place near VREF pin
Place 1 0.1UF cap near each power pin
PAR_INIT#
SLCTIN#
PDR7
PDR6
PDR5
PDR4
PDR3
PDR2
PDR1
PDR0
PDR[7:0]
SLCT#
PE
BUSY
ACK#
ERROR#
ALF#
STROBE#
PWM2
PWM1
SIO_GP43
Test/Debug Header
Unused GPIOs
J25
SIO_GP60
SIO_GP61
LPC_SMI#
TACH2
TACH1
MIDI_IN
MIDI_OUT
J1BUTTON1
J1BUTTON2
J2BUTTON1
J2BUTTON2
JOY1X
JOY1Y
JOY2X
JOY2Y
KEYLOCK#
SIO_GP21
SIO_GP22
SYSOPT
Pulldown on SYSOPT for IO address of 0x02E
R224
4.7K
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
SUPER I/O
REV:
1.0
PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
DRAWN BY:
INTEL (R) PCG
LAST REVISED:
5-15-00
PROJECT:
INTEL(R) 82815
SHEET:
16 OF 41

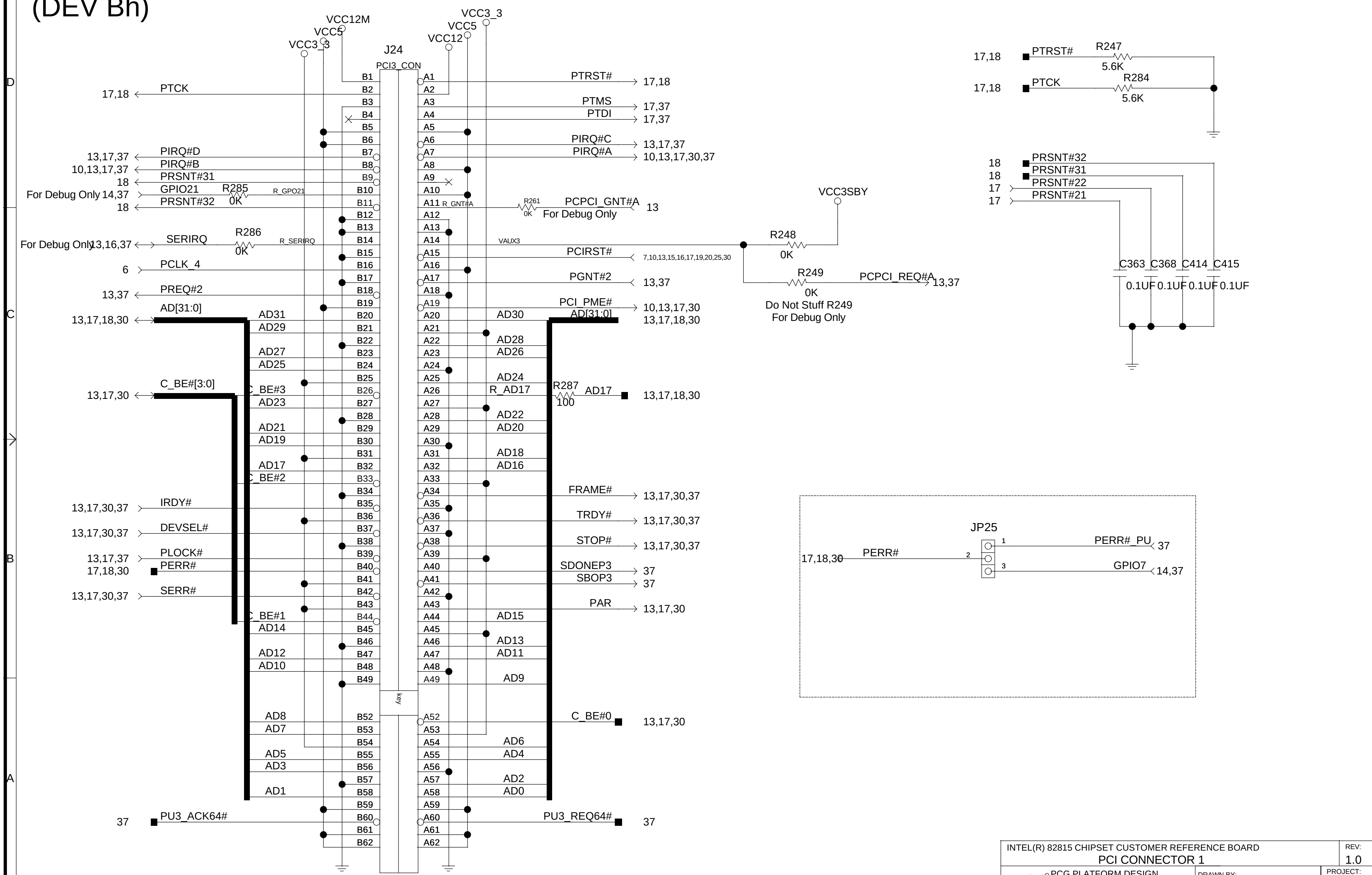
PCI Connector 0
(DEV Ah)



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD PCI CONNECTOR 0		REV: 1.0
intel © PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 17 OF 41

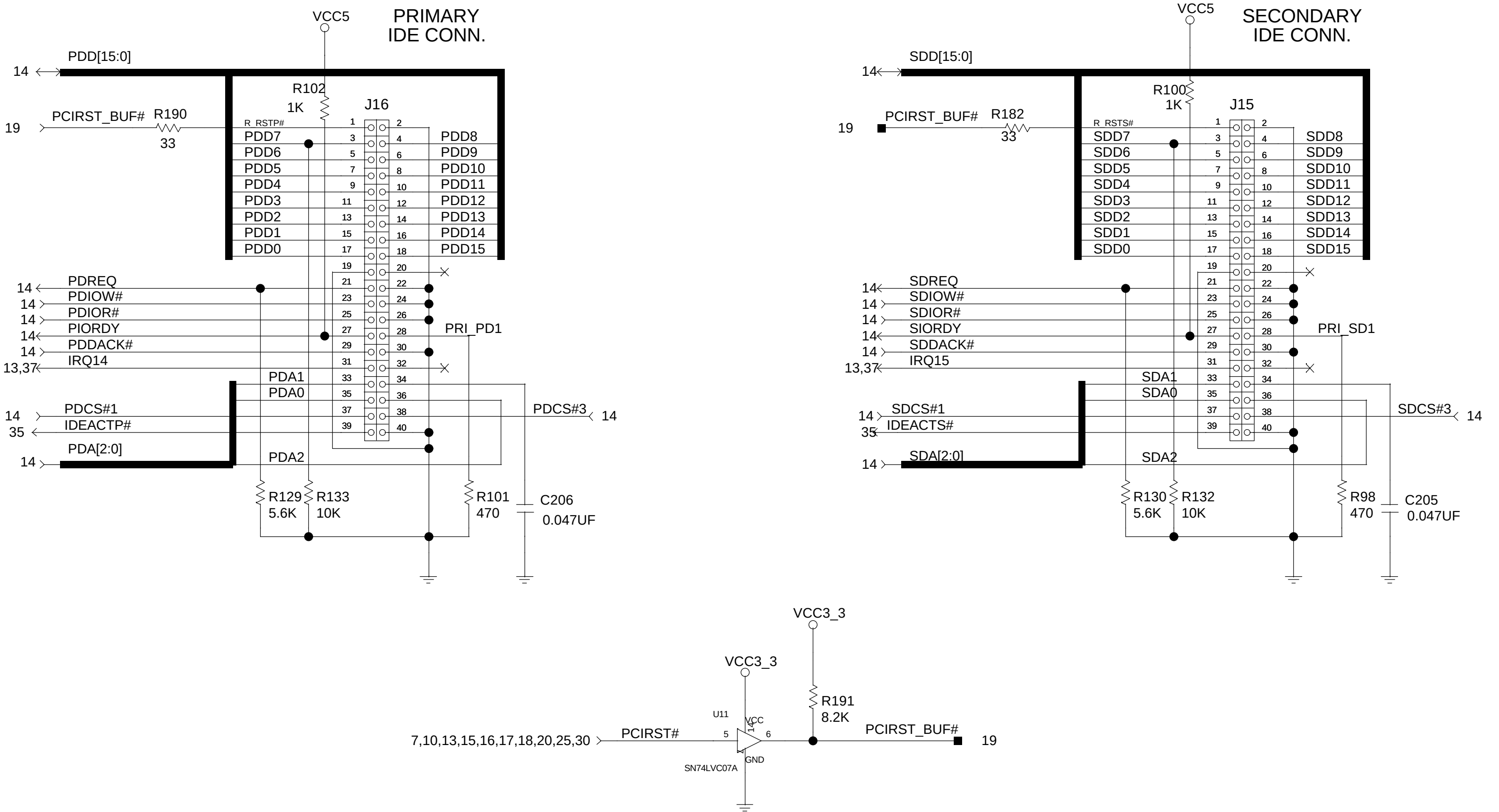
PCI Connector 1
(DEV Bh)

Layout Note: Should be in Slot 0 Position (Outside Edge of Board Furthest from CPU)



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
PCI CONNECTOR 1		
intel© PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 18 OF 41

IDE Connectors



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD

ULTRA DMA/66 CONNECTORS

REV: 1.0

intel® PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630

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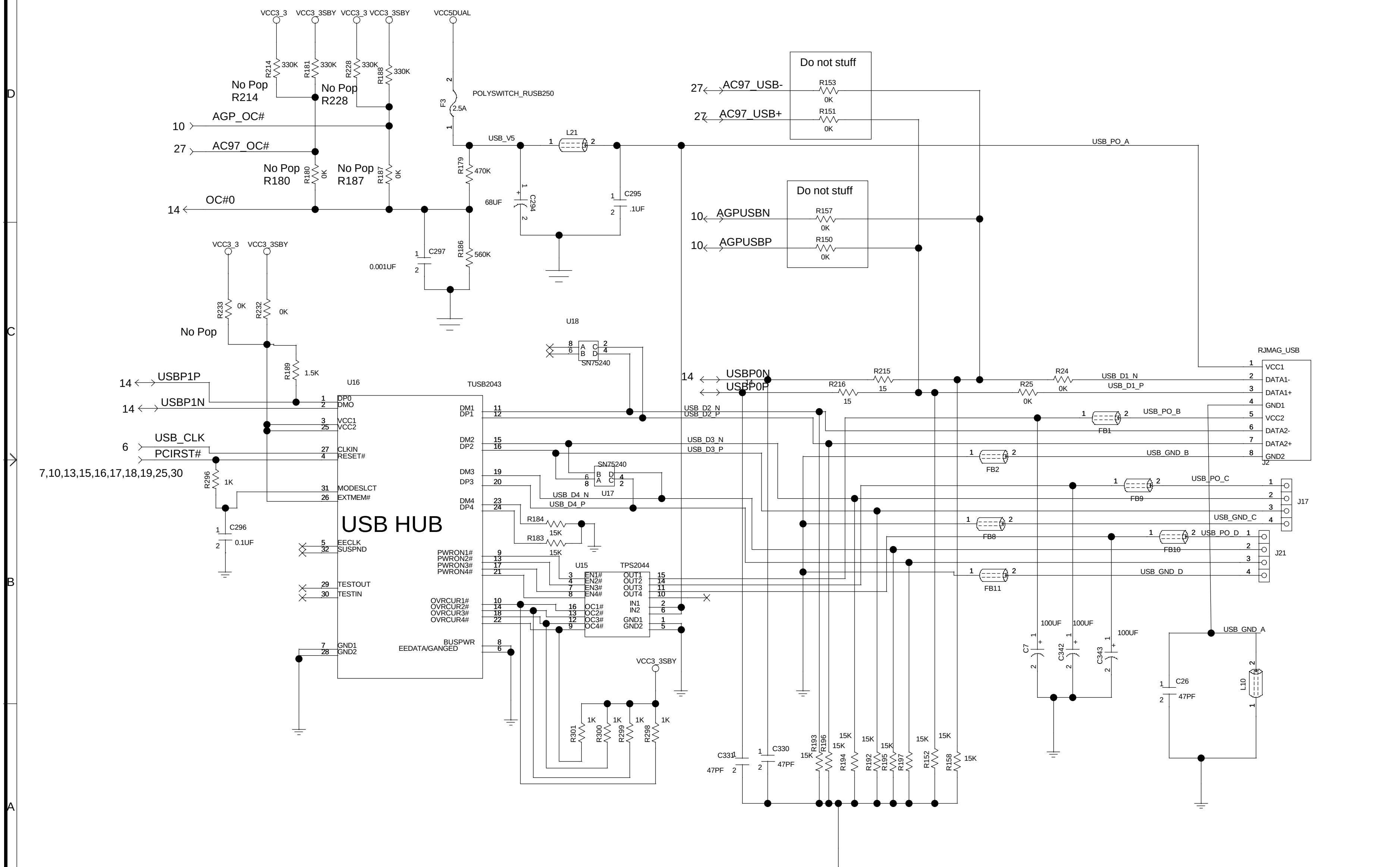
LAST REVISED: 5-15-00

PROJECT: INTEL(R) 82815

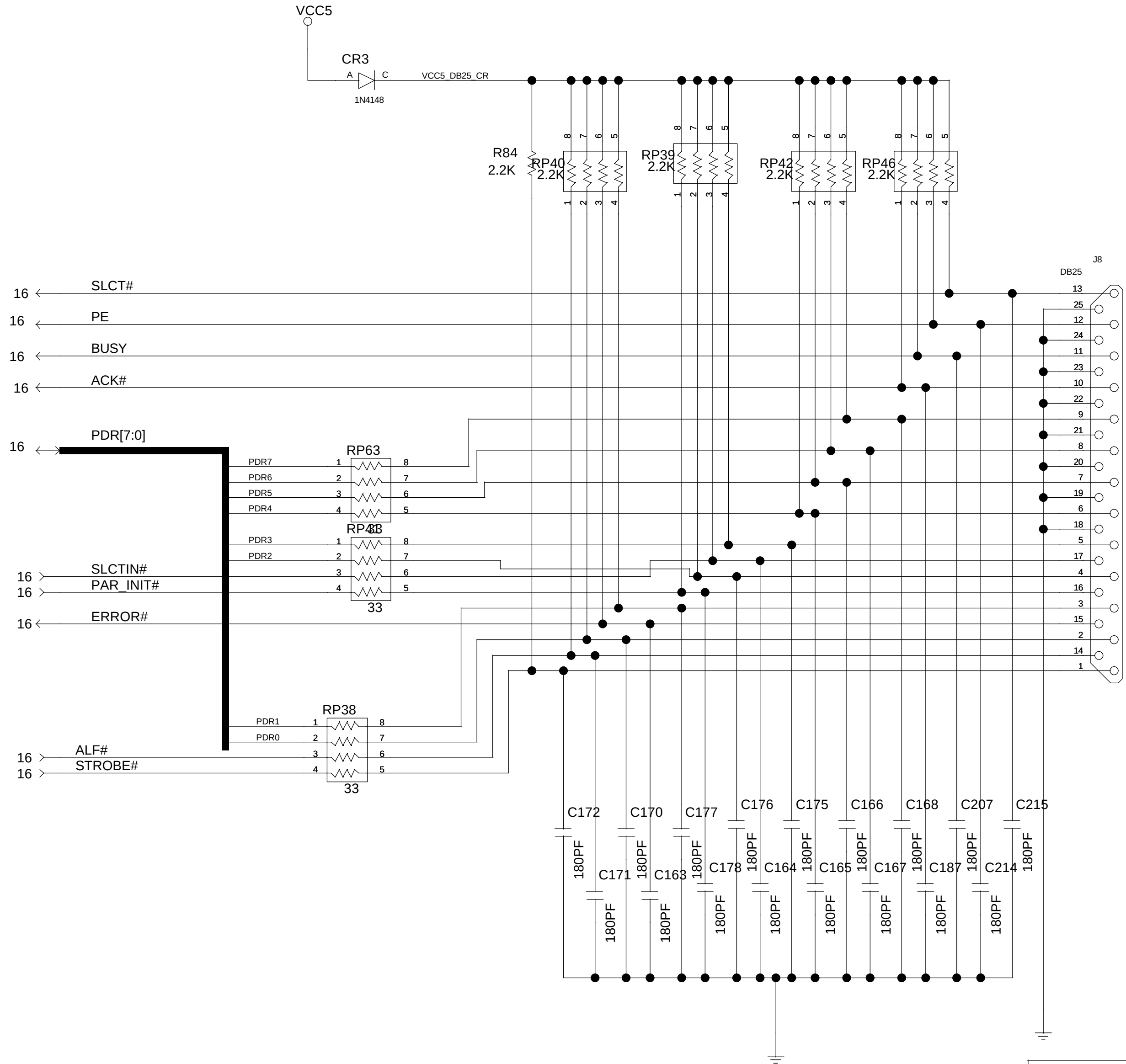
SHEET: 19 OF 41

USB Hub and Connectors



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD USB Hub		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 20 OF 41

Parallel Port



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD

PARALLEL PORT

REV: 1.0

PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630

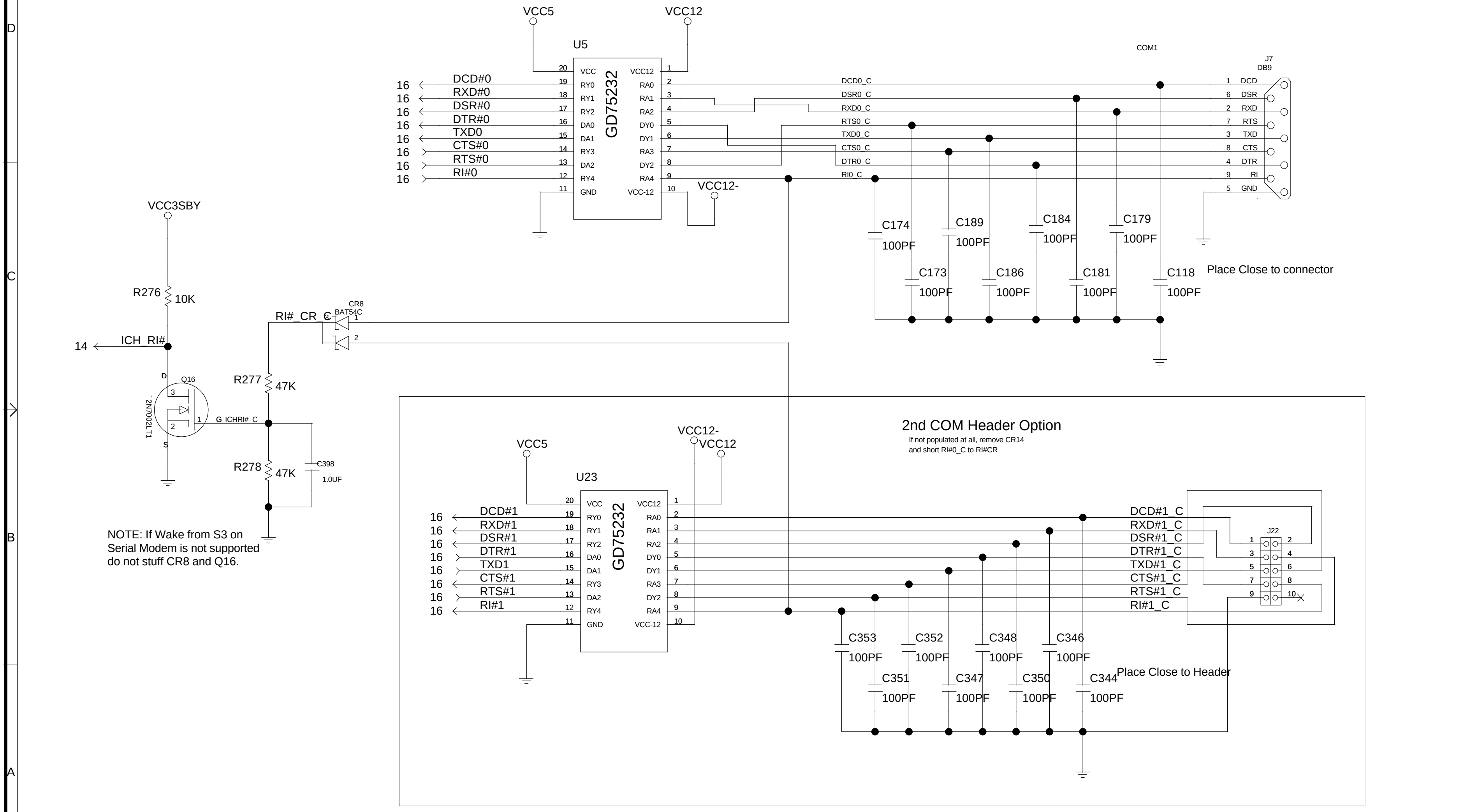
DRAWN BY: INTEL (R) PCG

LAST REVISED: 5-15-00

PROJECT: INTEL(R) 82815

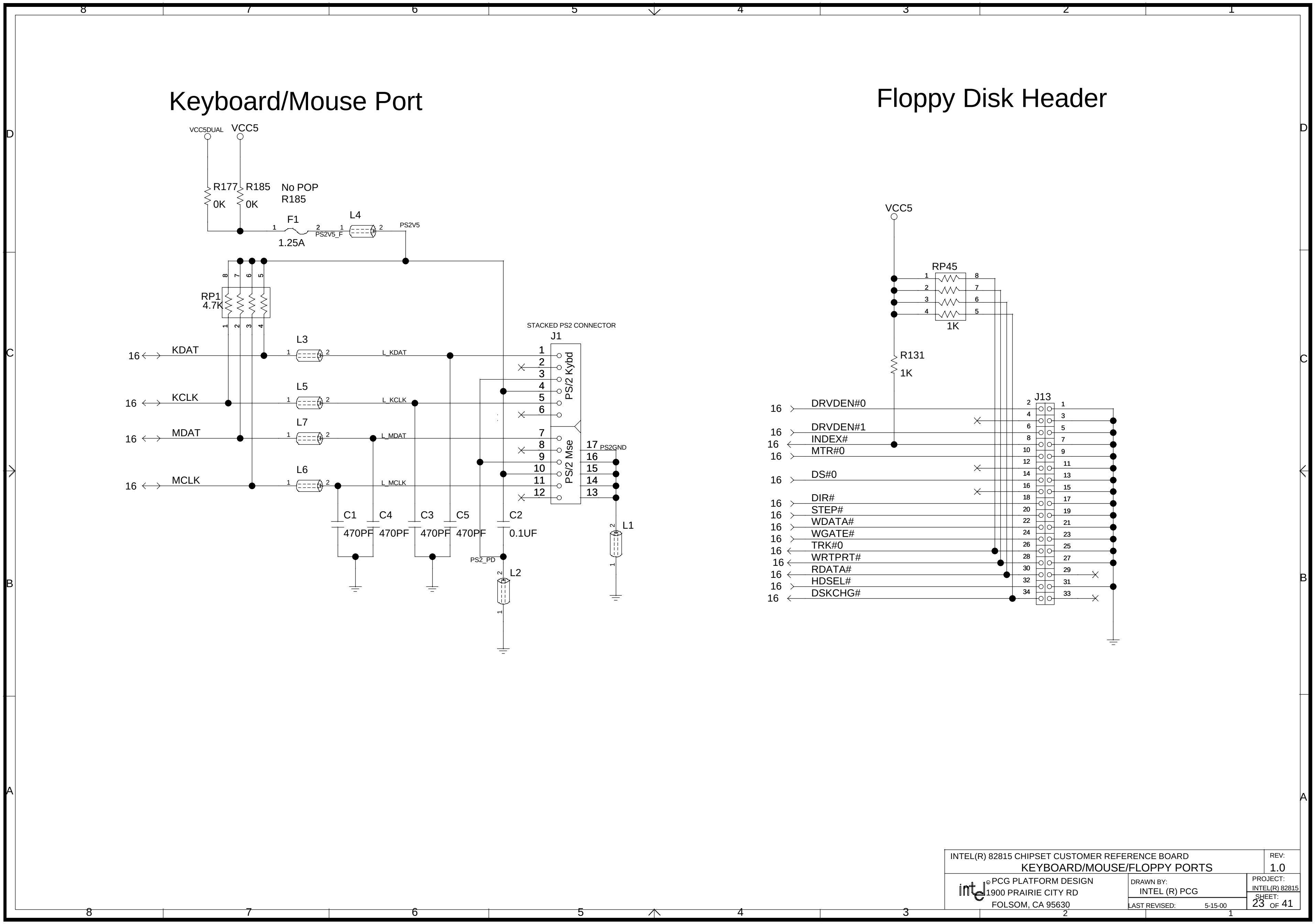
SHEET: 21 OF 41

Serial Port and Header

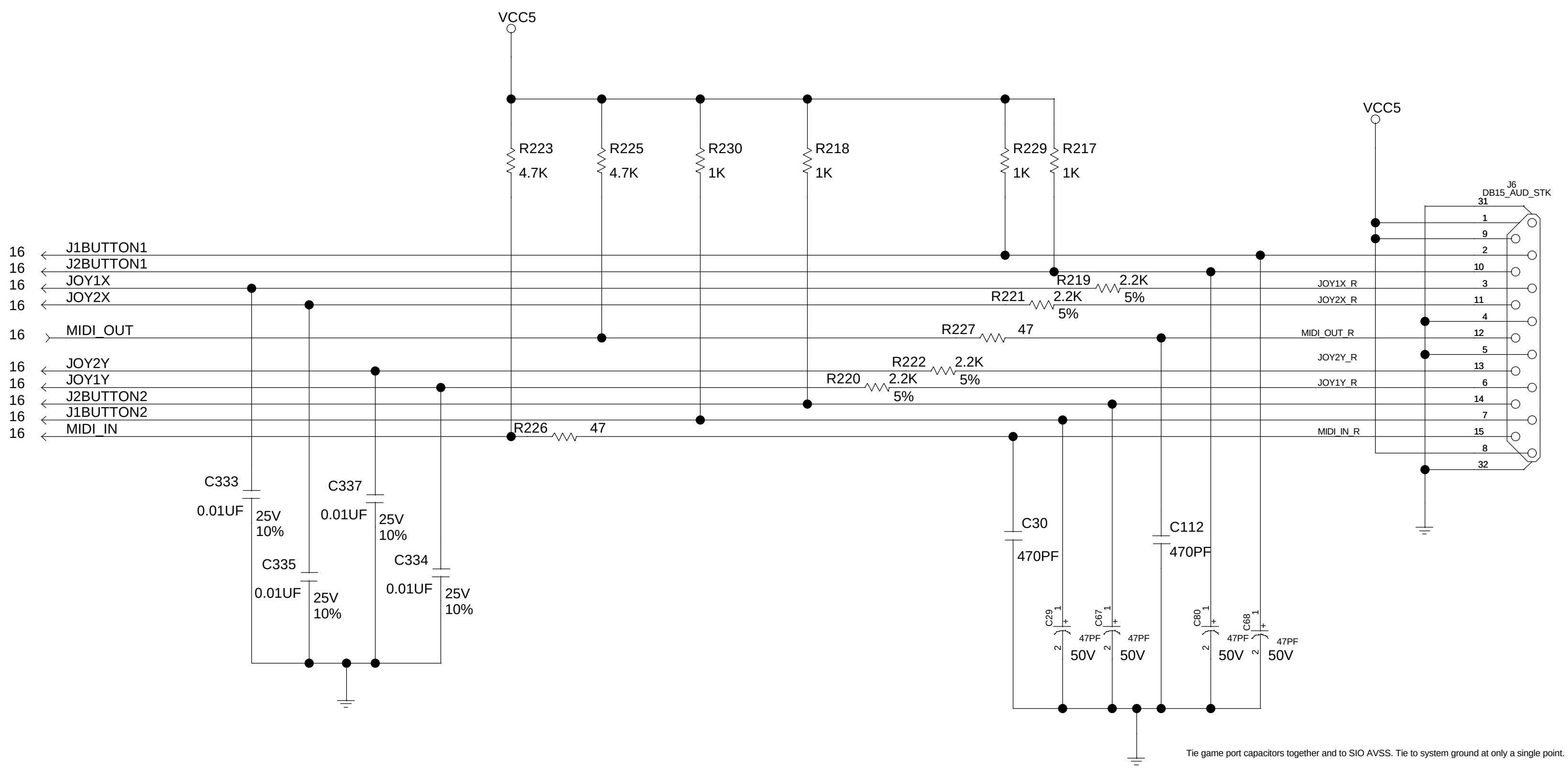


NOTE: If Wake from S3 on Serial Modem is not supported do not stuff CR8 and Q16.

INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD SERIAL AND GAME PORTS	REV: 1.0
PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00
PROJECT: INTEL(R) 82815	SHEET: 22 OF 41

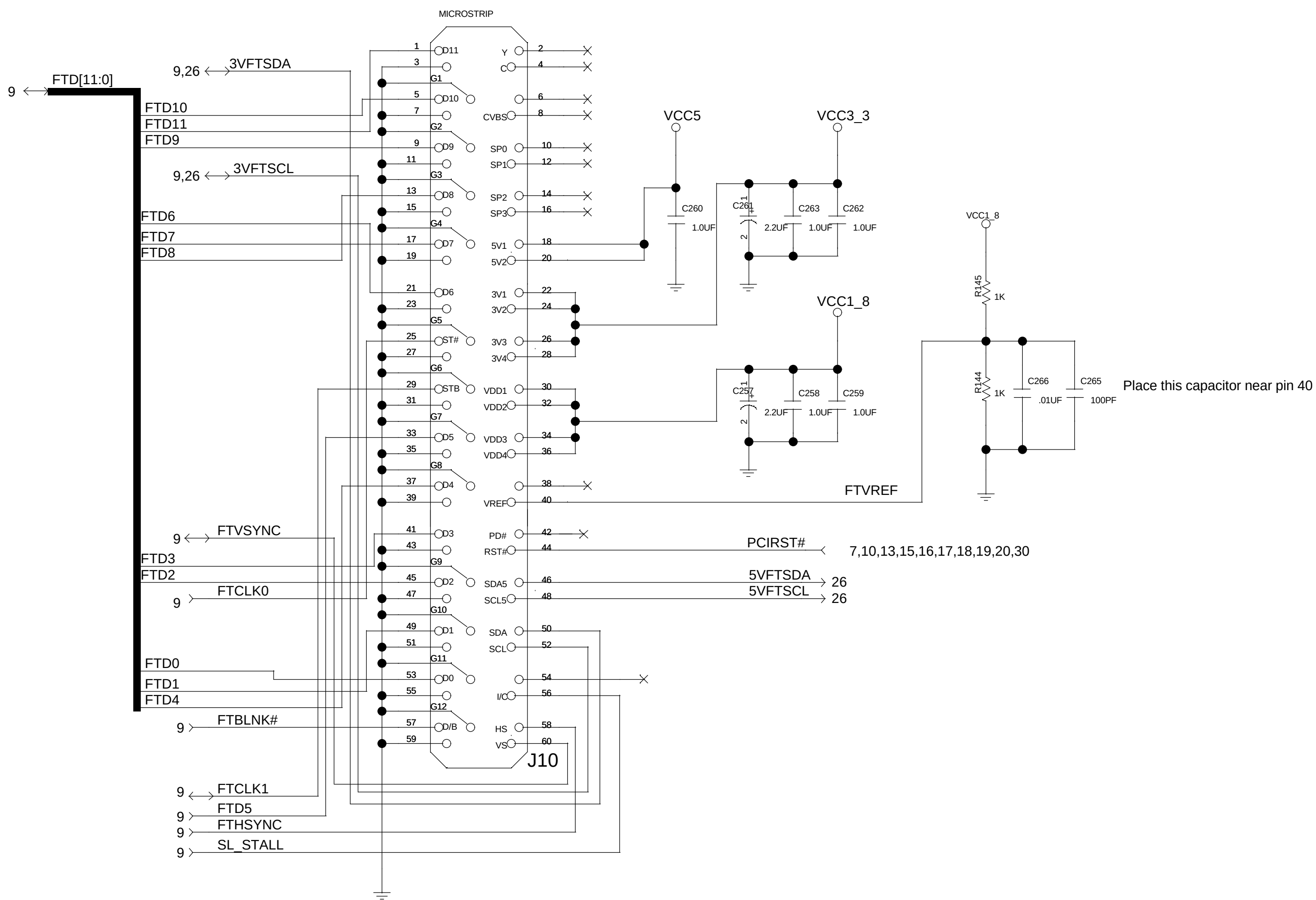

Keyboard/Mouse Port
VCC5DUAL
VCC5
R177
0K
R185
0K
No POP
R185
F1
1.25A
PS2V5_F
L4
PS2V5
RP1
4.7K
STACKED PS2 CONNECTOR
J1
PS/2 Kybd
PS/2 Mse
KDAT
KCLK
MDAT
MCLK
L3
L5
L7
L6
L_KDAT
L_KCLK
L_MDAT
L_MCLK
PS2GND
C1
C4
C3
C5
C2
470PF
470PF
470PF
470PF
0.1UF
PS2_PD
L2
L1
Floppy Disk Header
VCC5
RP45
1K
R131
1K
J13
DRVDEN#0
DRVDEN#1
INDEX#
MTR#0
DS#0
DIR#
STEP#
WDATA#
WGATE#
TRK#0
WRTPRT#
RDATA#
HDSEL#
DSKCHG#
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
KEYBOARD/MOUSE/FLOPPY PORTS
REV:
1.0
PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
DRAWN BY:
INTEL (R) PCG
LAST REVISED:
5-15-00
PROJECT:
INTEL(R) 82815
SHEET:
23 OF 41

Game Port



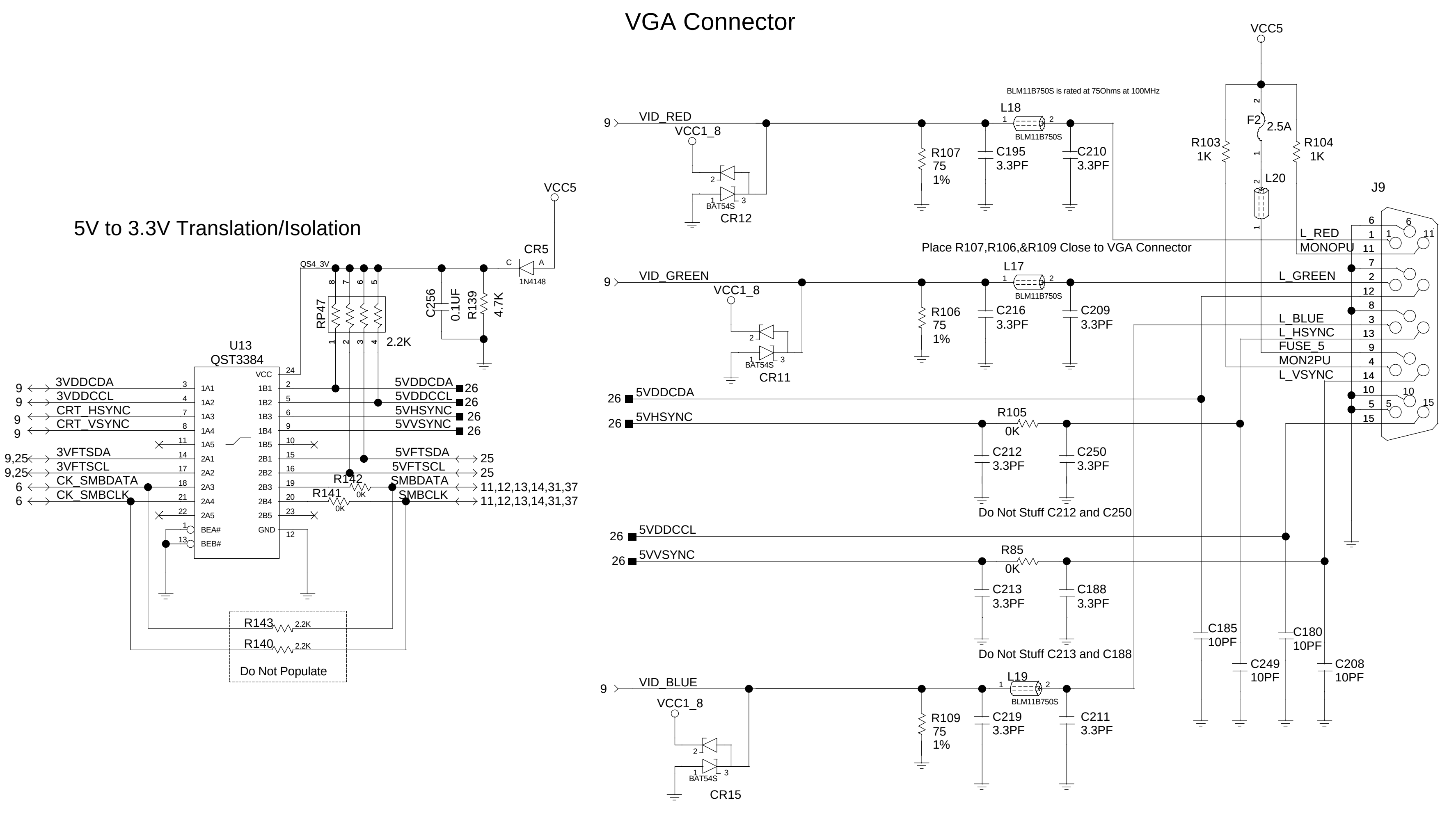
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD GAME PORT		REV: 1.0
intel ® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 24 OF 41

Digital Video Out Connector
(For debug purposes only)



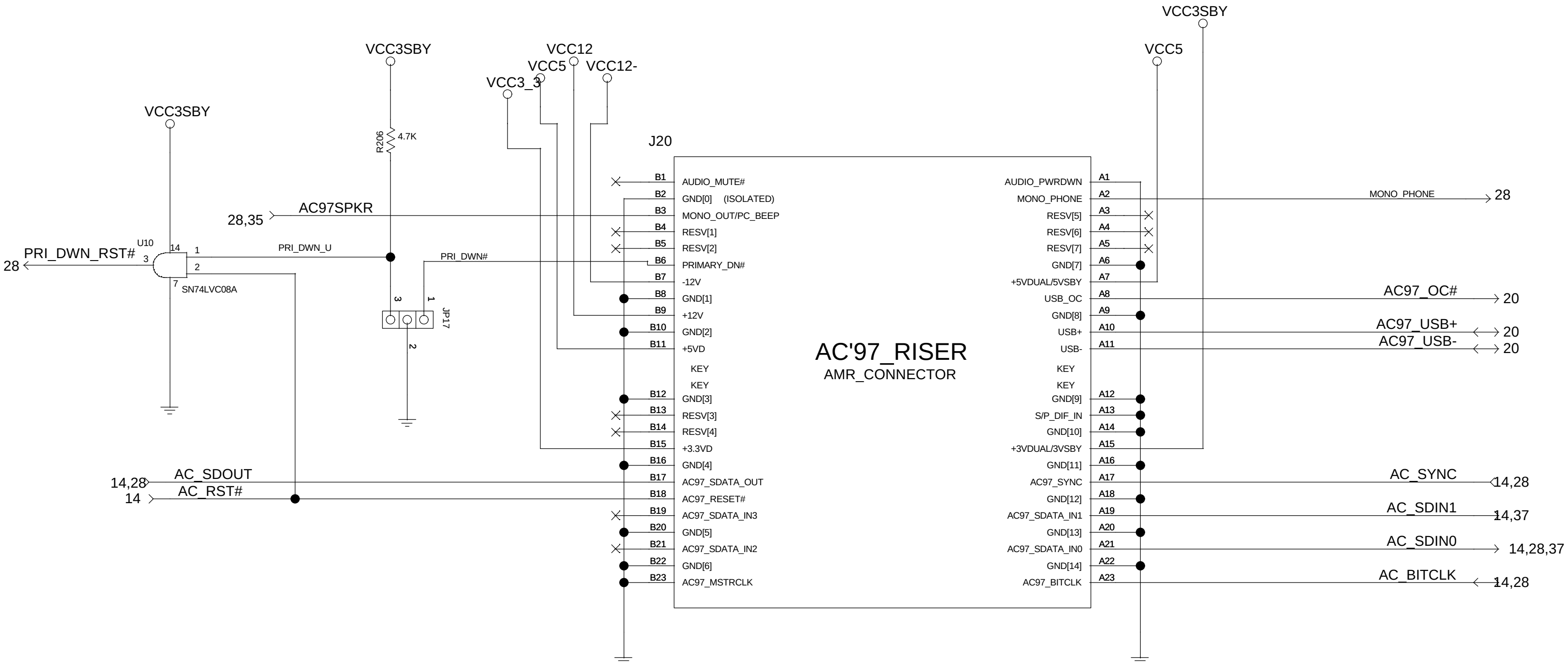
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
DIGITAL VIDEO OUT CONNECTOR
REV: 1.0
intel© PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
DRAWN BY: INTEL (R) PCG
LAST REVISED: 5-15-00
PROJECT: INTEL(R) 82815
SHEET: 25 OF 41

Video Connector



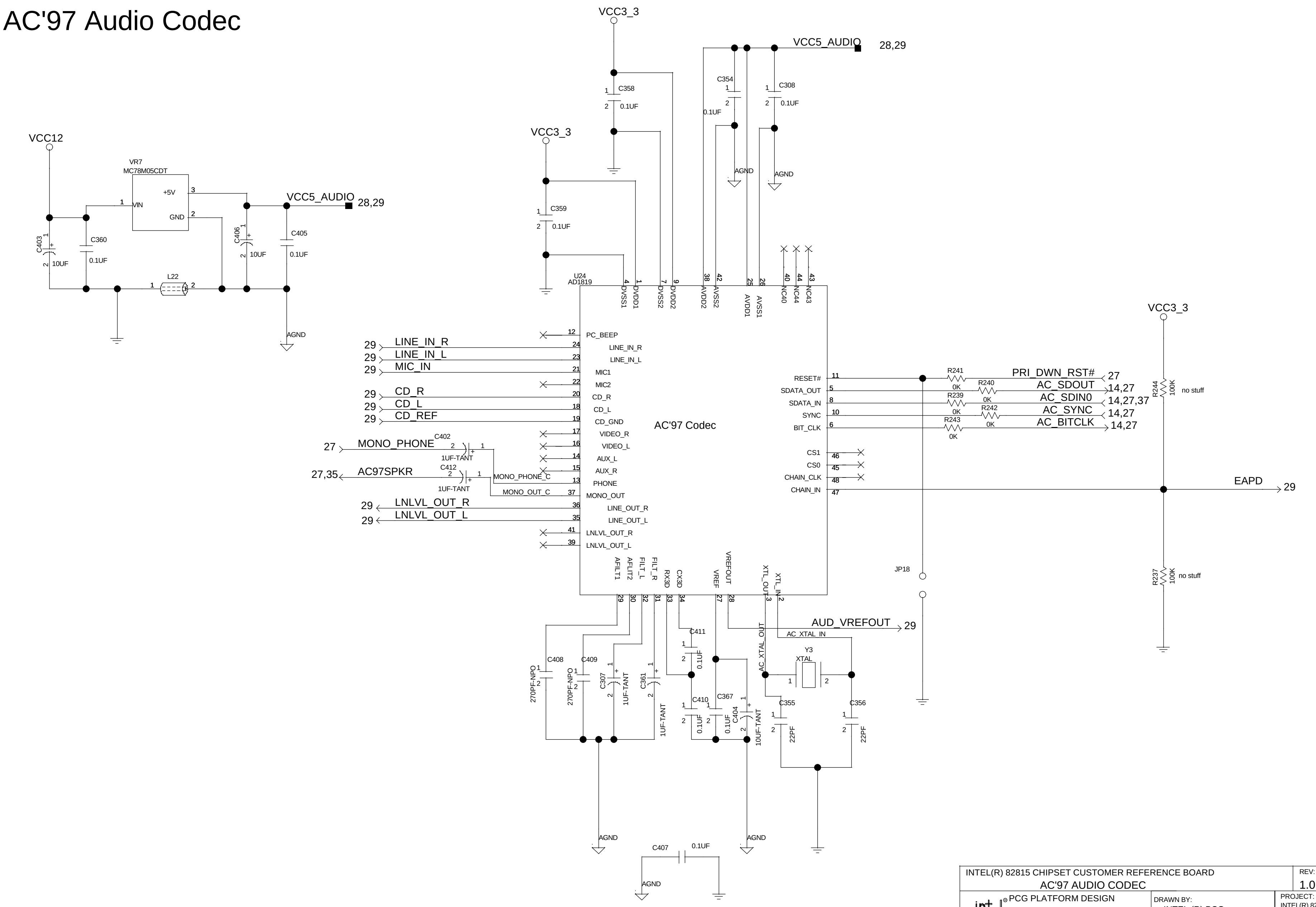
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.0
VIDEO CONNECTOR	
PCG PLATFORM DESIGN, 1900 PRAIRIE CITY RD, FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG
LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815
	SHEET: 26 OF 41

Audio/Modem Riser



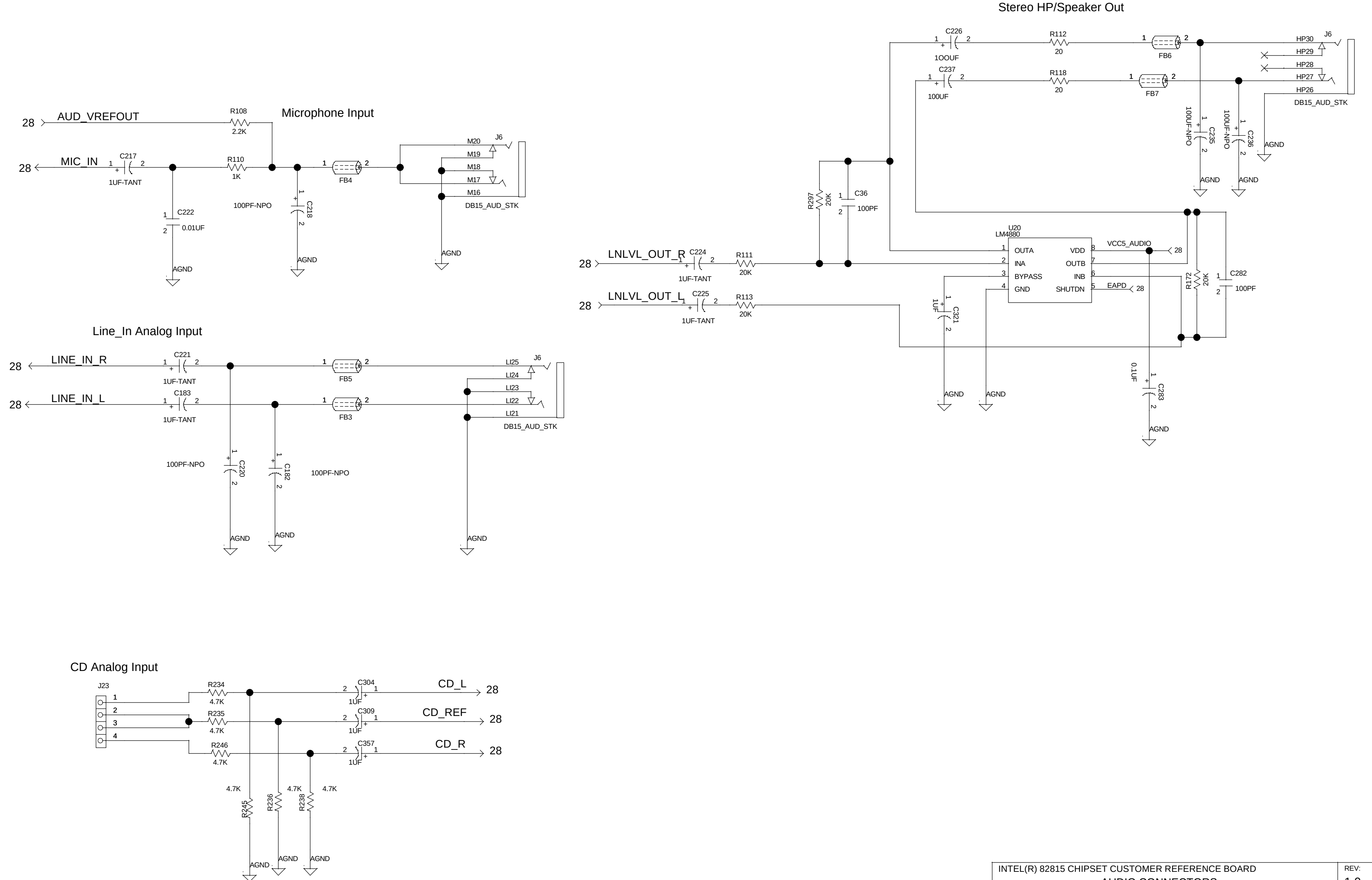
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD AUDIO/MODEM RISER	REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00
PROJECT: INTEL(R) 82815	SHEET: 27 OF 41

AC'97 Audio Codec



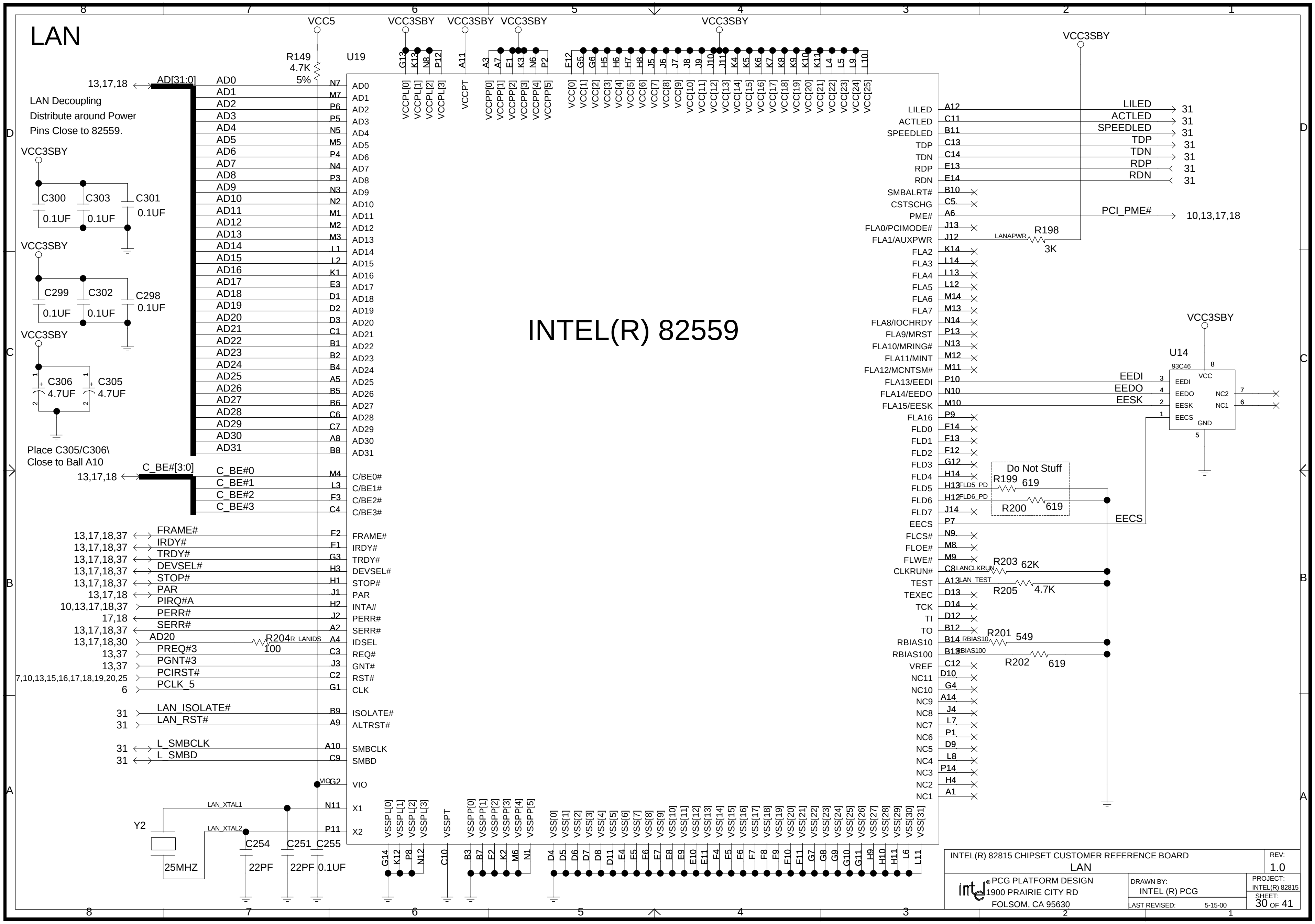
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.0
AC'97 AUDIO CODEC		
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 28 OF 41

Audio Connectors



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
AUDIO CONNECTORS
REV: 1.0
PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
DRAWN BY: INTEL (R) PCG
LAST REVISED: 5-15-00
PROJECT: INTEL(R) 82815
SHEET: 29 OF 41

LAN



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD

LAN

REV: 1.0

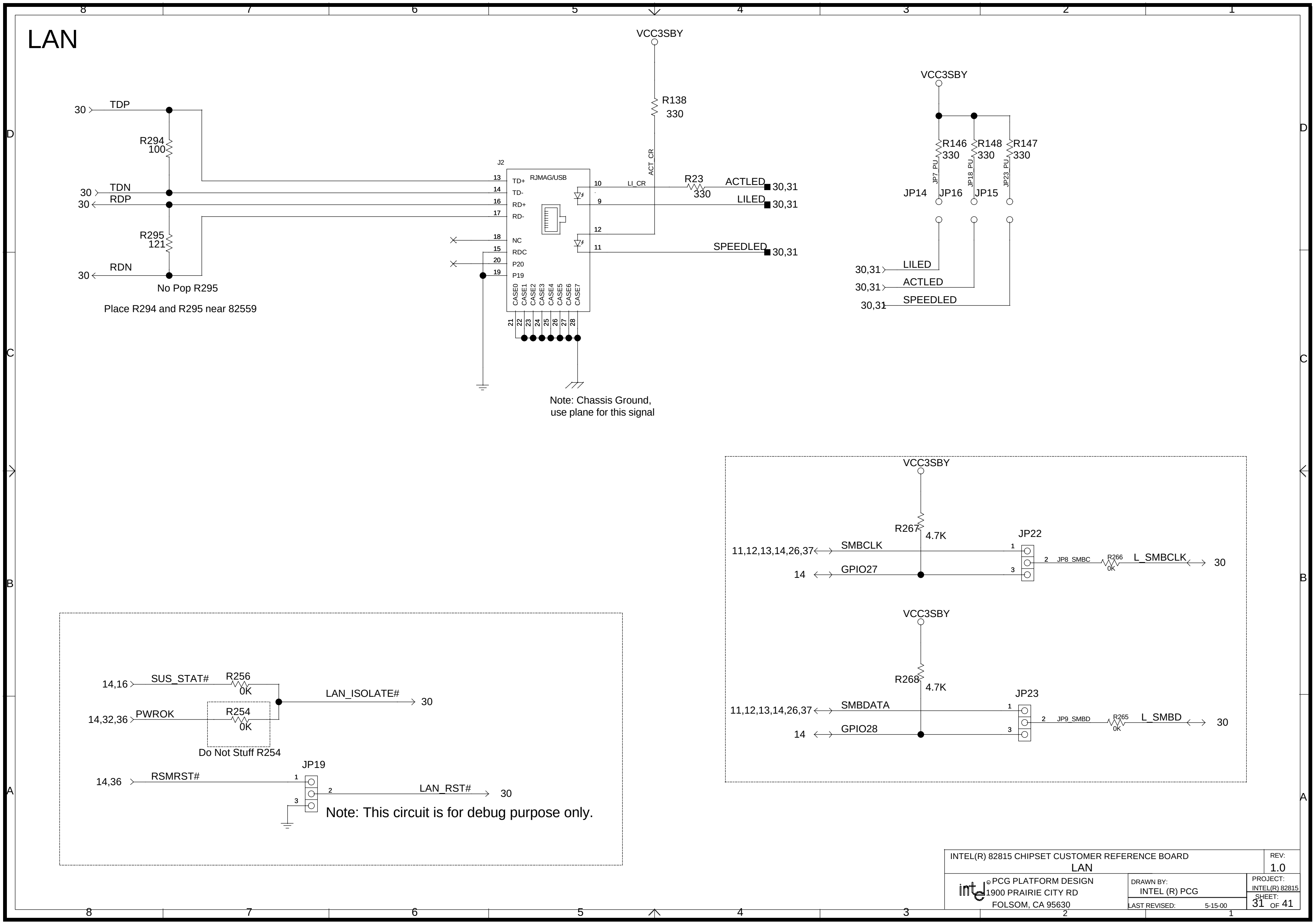
intel® PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630

DRAWN BY: INTEL (R) PCG

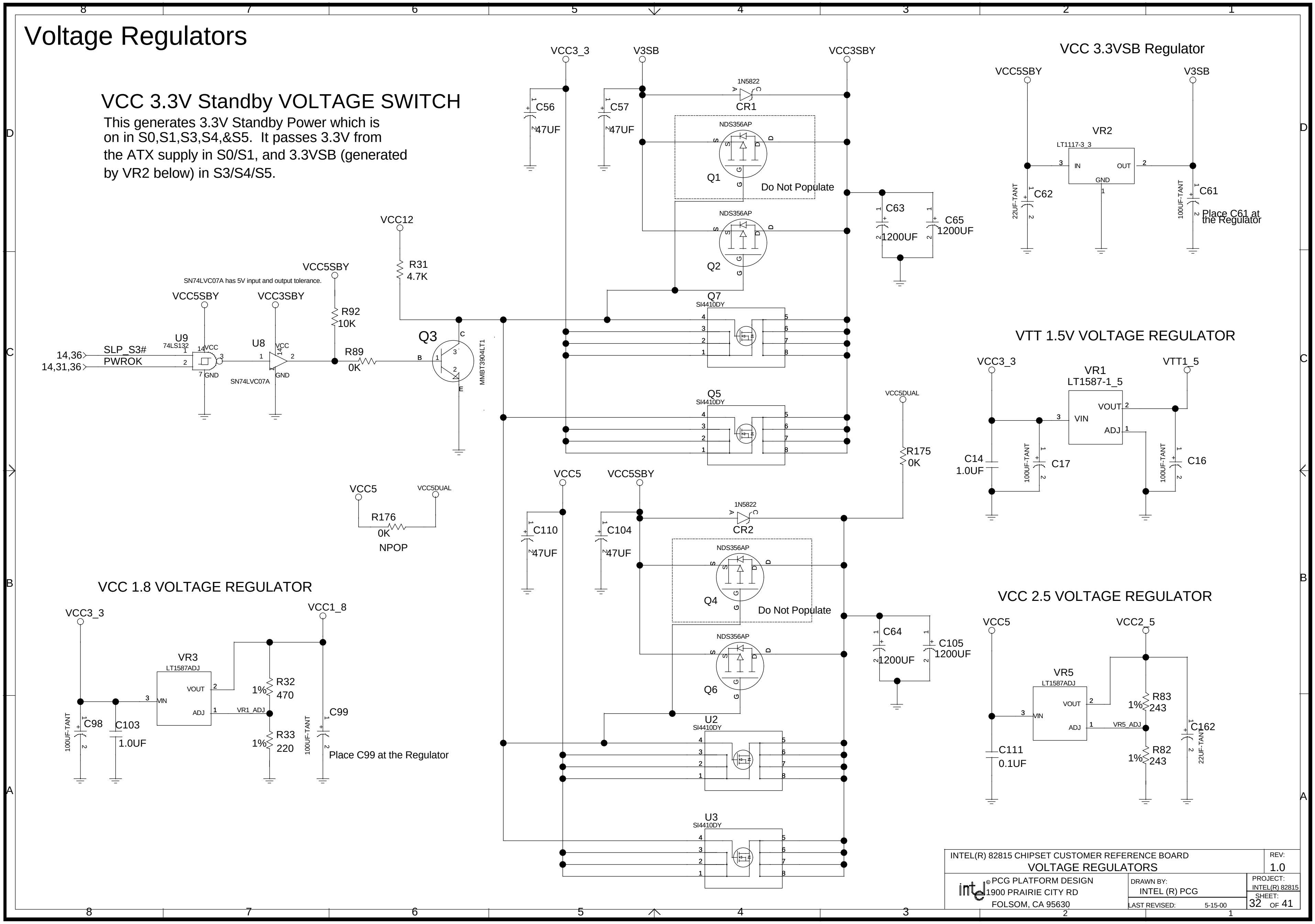
LAST REVISED: 5-15-00

PROJECT: INTEL(R) 82815

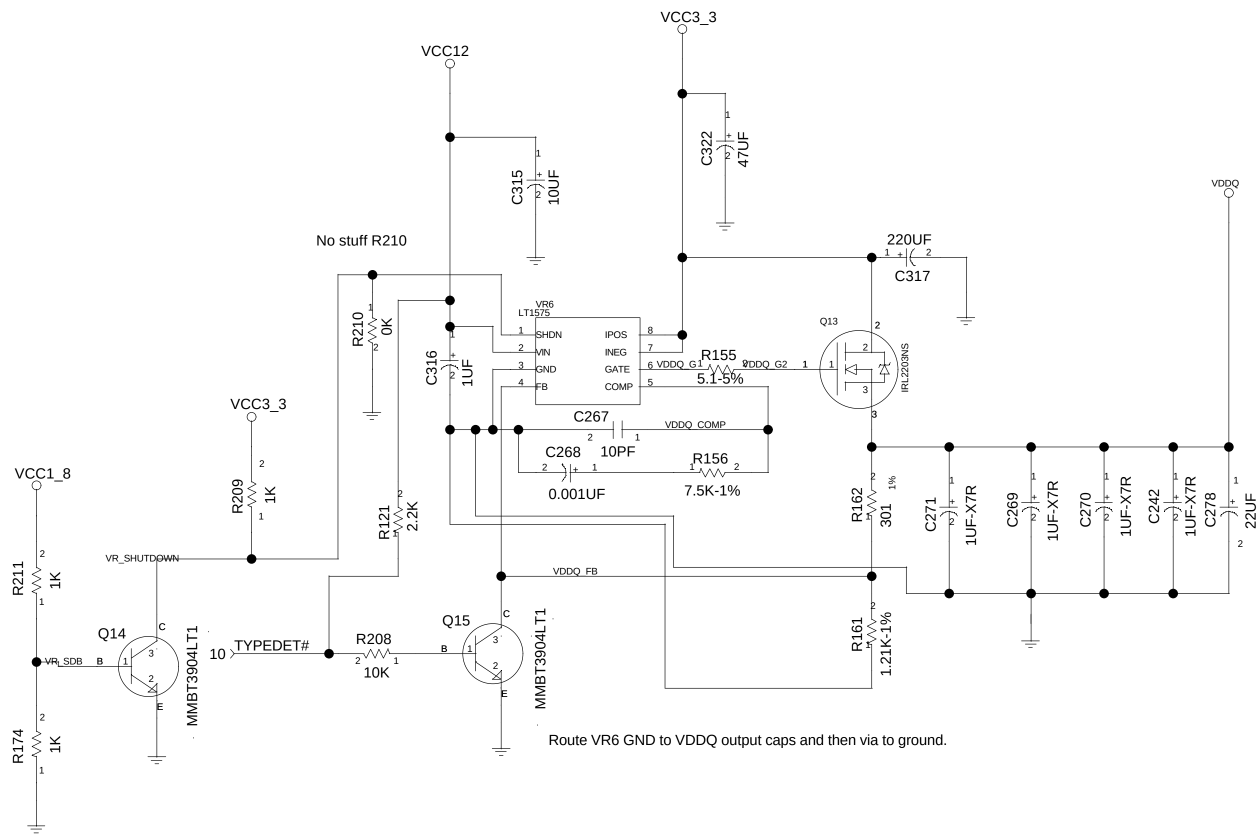
SHEET: 30 OF 41



LAN
VCC3SBY
R138
330
ACT_CR
30 TDP
R294
100
30 TDN
30 RDP
R295
121
30 RDN
No Pop R295
Place R294 and R295 near 82559
J2
RJMAG/USB
TD+
TD-
RD+
RD-
NC
RDC
P20
P19
CASE0 CASE1 CASE2 CASE3 CASE4 CASE5 CASE6 CASE7
LI_CR
R23
330
ACTLED 30,31
LILED 30,31
SPEEDLED 30,31
Note: Chassis Ground,
use plane for this signal
VCC3SBY
R146 330
R148 330
R147 330
JP7_PU
JP18_PU
JP23_PU
JP14 JP16 JP15
30,31 LILED
30,31 ACTLED
30,31 SPEEDLED
VCC3SBY
R267
4.7K
JP22
11,12,13,14,26,37 SMBCLK
14 GPIO27
JP8_SMBC
R266
0K
L_SMBCLK 30
VCC3SBY
R268
4.7K
JP23
11,12,13,14,26,37 SMBDATA
14 GPIO28
JP9_SMBD
R265
0K
L_SMBD 30
14,16 SUS_STAT#
R256
0K
LAN_ISOLATE# 30
14,32,36 PWROK
R254
0K
Do Not Stuff R254
JP19
14,36 RSMRST#
LAN_RST# 30
Note: This circuit is for debug purpose only.
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
LAN
REV:
1.0
PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
DRAWN BY:
INTEL (R) PCG
PROJECT:
INTEL(R) 82815
LAST REVISED:
5-15-00
SHEET:
31 OF 41

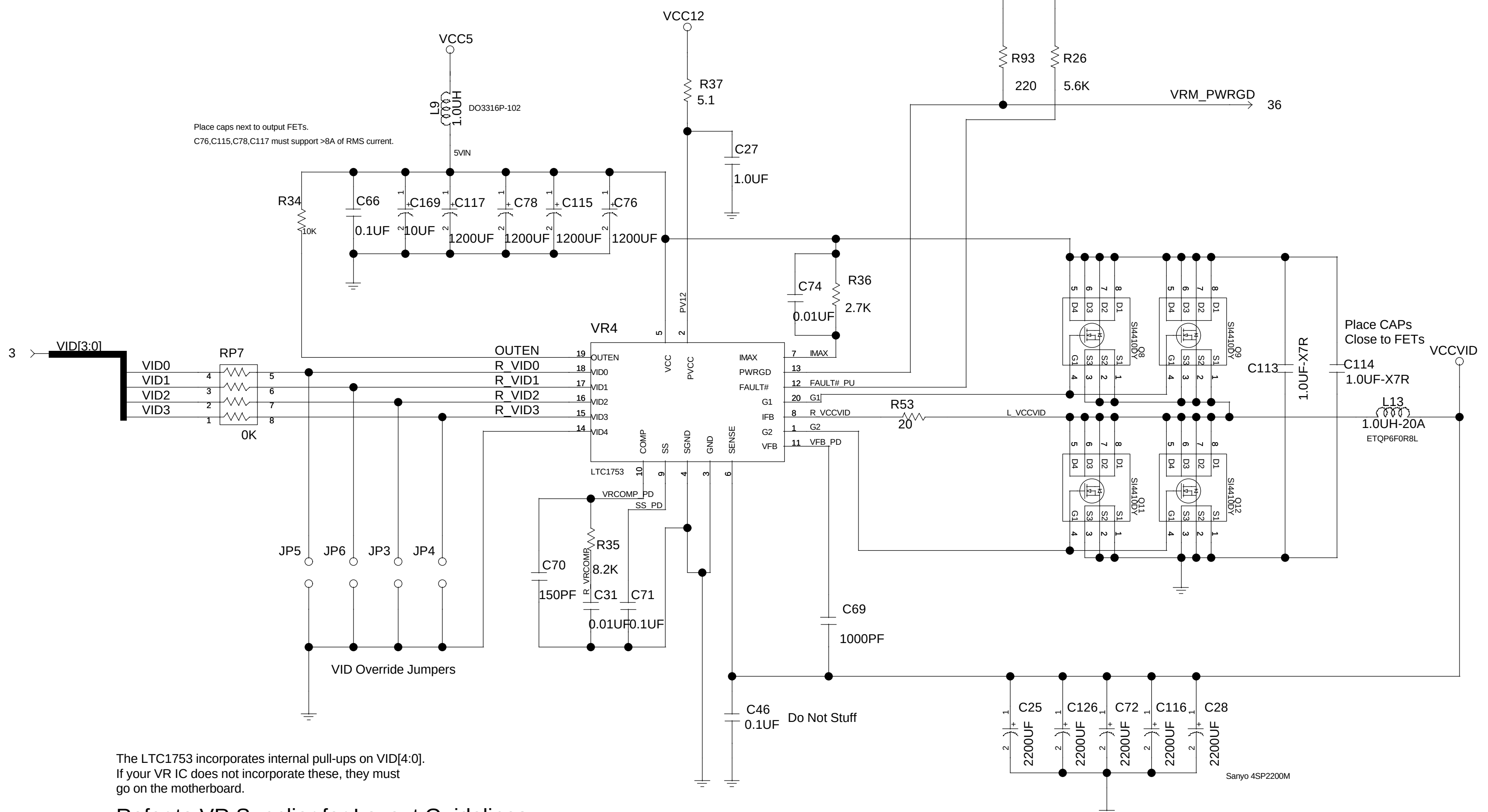

Voltage Regulators
VCC 3.3V Standby VOLTAGE SWITCH
This generates 3.3V Standby Power which is on in S0,S1,S3,S4,&S5. It passes 3.3V from the ATX supply in S0/S1, and 3.3VSB (generated by VR2 below) in S3/S4/S5.
SN74LVC07A has 5V input and output tolerance.
VCC3_3
V3SB
VCC3SBY
1N5822
CR1
C56
47UF
C57
47UF
NDS356AP
Q1
Do Not Populate
Q2
C63
1200UF
C65
1200UF
VCC12
R31
4.7K
VCC5SBY
R92
10K
VCC5SBY
VCC3SBY
U9
74LS132
U8
SN74LVC07A
14,36
SLP_S3#
14,31,36
PWROK
R89
0K
Q3
MMBT3904LT1
Q7
SI4410DY
Q5
SI4410DY
VCC5DUAL
R175
0K
VCC5
VCC5DUAL
R176
0K
NPOP
VCC5
VCC5SBY
1N5822
CR2
C110
47UF
C104
47UF
Q4
Do Not Populate
Q6
C64
1200UF
C105
1200UF
U2
SI4410DY
U3
SI4410DY
VCC 3.3VSB Regulator
VCC5SBY
V3SB
VR2
LT1117-3_3
IN
OUT
GND
22UF-TANT
C62
100UF-TANT
C61
Place C61 at the Regulator
VTT 1.5V VOLTAGE REGULATOR
VCC3_3
VTT1_5
VR1
LT1587-1_5
VIN
VOUT
ADJ
C14
1.0UF
100UF-TANT
C17
100UF-TANT
C16
VCC 1.8 VOLTAGE REGULATOR
VCC3_3
VCC1_8
VR3
LT1587ADJ
VIN
VOUT
ADJ
VR1_ADJ
R32
1%
470
R33
1%
220
100UF-TANT
C98
C103
1.0UF
100UF-TANT
C99
Place C99 at the Regulator
VCC 2.5 VOLTAGE REGULATOR
VCC5
VCC2_5
VR5
LT1587ADJ
VIN
VOUT
ADJ
VR5_ADJ
R83
1%
243
R82
1%
243
C111
0.1UF
C162
22UF-TANT
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
REV:
1.0
VOLTAGE REGULATORS
PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
DRAWN BY:
INTEL (R) PCG
LAST REVISED:
5-15-00
PROJECT:
INTEL(R) 82815
SHEET:
32
OF 41

AGP Voltage Regulator



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD AGP VOLTAGE REGULATOR		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 33 OF 41

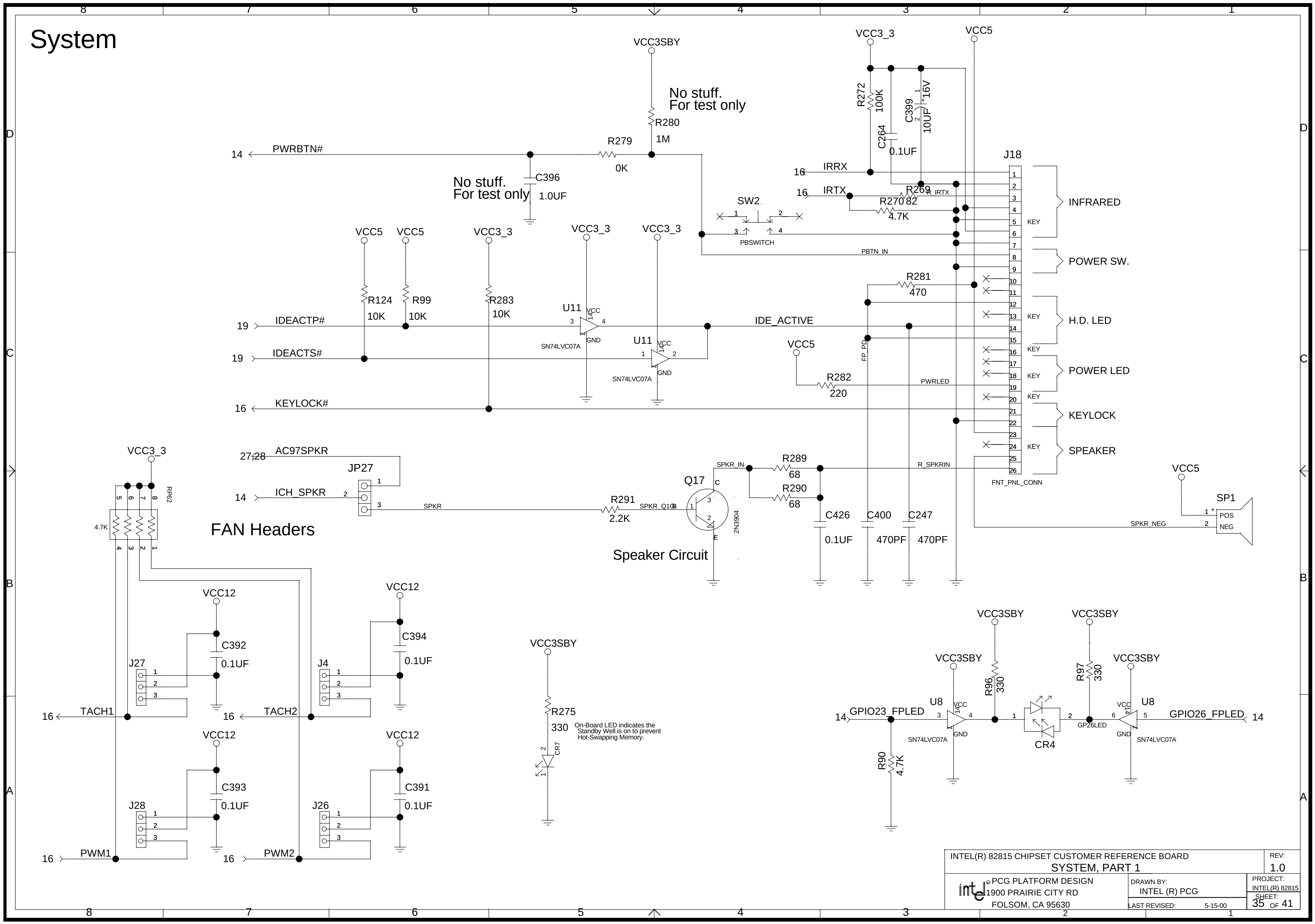
Processor Voltage Regulator



The LTC1753 incorporates internal pull-ups on VID[4:0].
If your VR IC does not incorporate these, they must
go on the motherboard.

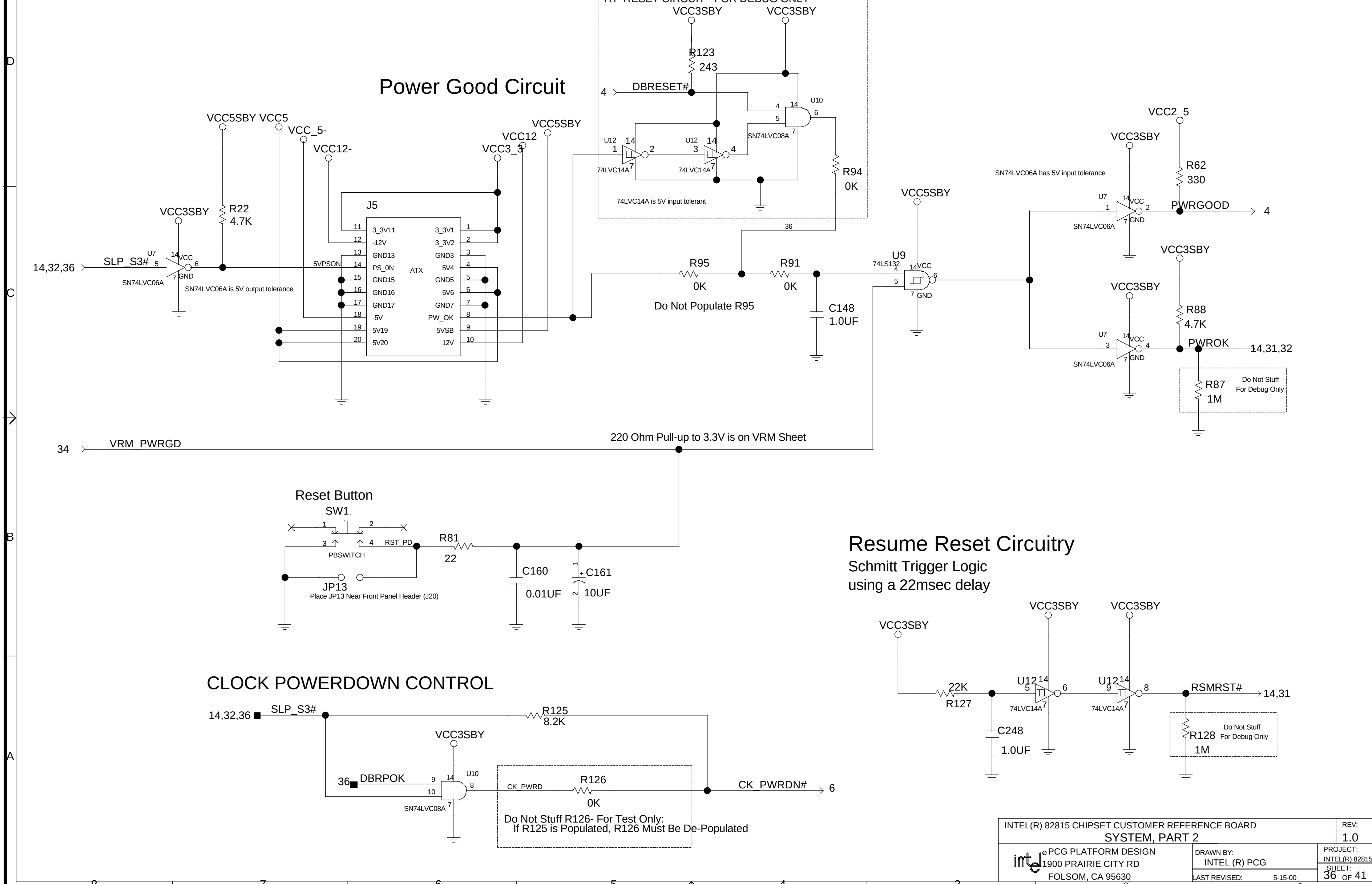
Refer to VR Supplier for Layout Guidelines

INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD VRM 8.4		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 34 OF 41

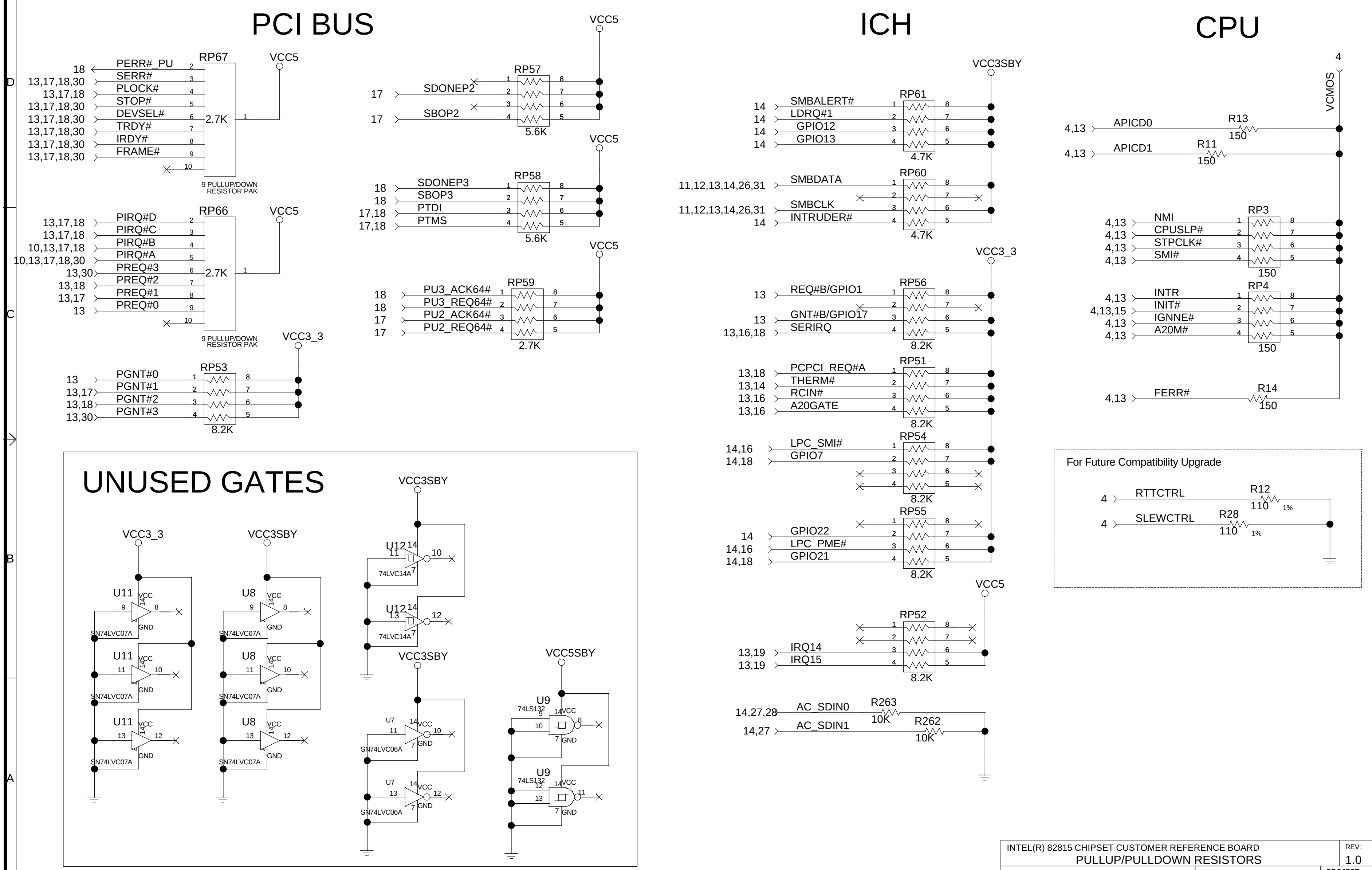

System
No stuff.
For test only
No stuff.
For test only
VCC3SBY
R280
1M
R279
0K
C396
1.0UF
14 PWRBTN#
VCC3_3
VCC5
R272
100K
C399
10UF
16V
C264
0.1UF
16 IRRX
16 IRTX
R269 82
R270
4.7K
IRTX
SW2
PBSWITCH
PBTN_IN
J18
INFRARED
POWER SW.
H.D. LED
POWER LED
KEYLOCK
SPEAKER
KEY
FNT_PNL_CONN
R281
470
FP_PD
IDE_ACTIVE
VCC5
R124
10K
R99
10K
R283
10K
U11
SN74LVC07A
19 IDEACTP#
19 IDEACTS#
16 KEYLOCK#
R282
220
PWRLED
27,28 AC97SPKR
14 ICH_SPKR
JP27
SPKR
R291
2.2K
SPKR_Q10
Q17
2N3904
SPKR_IN
R289
68
R290
68
R_SPKRIN
C426
0.1UF
C400
470PF
C247
470PF
Speaker Circuit
VCC5
SP1
POS
NEG
SPKR_NEG
FAN Headers
VCC3_3
RP62
4.7K
VCC12
C392
0.1UF
J27
16 TACH1
C394
0.1UF
J4
16 TACH2
C393
0.1UF
J28
16 PWM1
C391
0.1UF
J26
16 PWM2
VCC3SBY
R275
330
CR7
On-Board LED indicates the Standby Well is on to prevent Hot-Swapping Memory.
R96
330
R97
330
U8
SN74LVC07A
14 GPIO23_FPLED
R90
4.7K
CR4
GP26LED
GPIO26_FPLED 14
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
SYSTEM, PART 1
REV:
1.0
PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630
DRAWN BY:
INTEL (R) PCG
LAST REVISED:
5-15-00
PROJECT:
INTEL(R) 82815
SHEET:
35 OF 41

System

Power Connector and Reset Control



Pull-up Resistors and unused gates



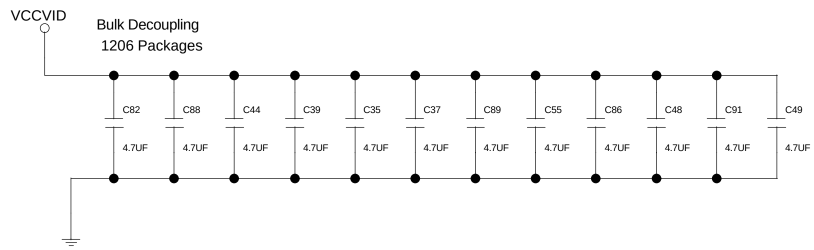
INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.0
PULLUP/PULLDOWN RESISTORS			
intel® PCG PLATFORM DESIGN, 1900 PRAIRIE CITY RD, FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG		PROJECT: INTEL(R) 82815
	LAST REVISED: 5-15-00		SHEET: 37 OF 41

370-pin Socket Decoupling

VCCVID Decoupling

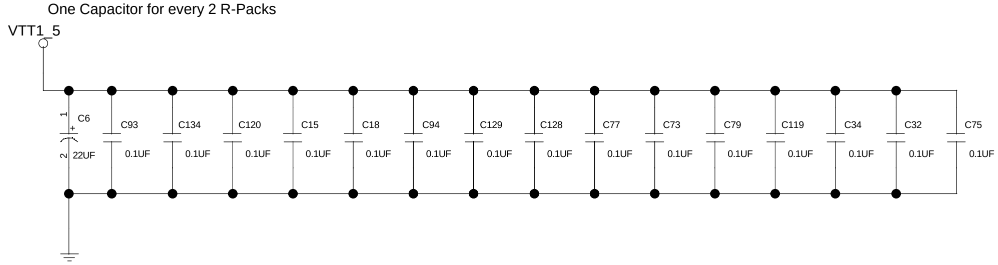
Place in 370 PGA Socket Cavity

Bulk Decoupling
1206 Packages



VTT Decoupling

0603 Package placed within 200mils of VTT Termination R-packs
One Capacitor for every 2 R-Packs



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD
VRM DECOUPLING

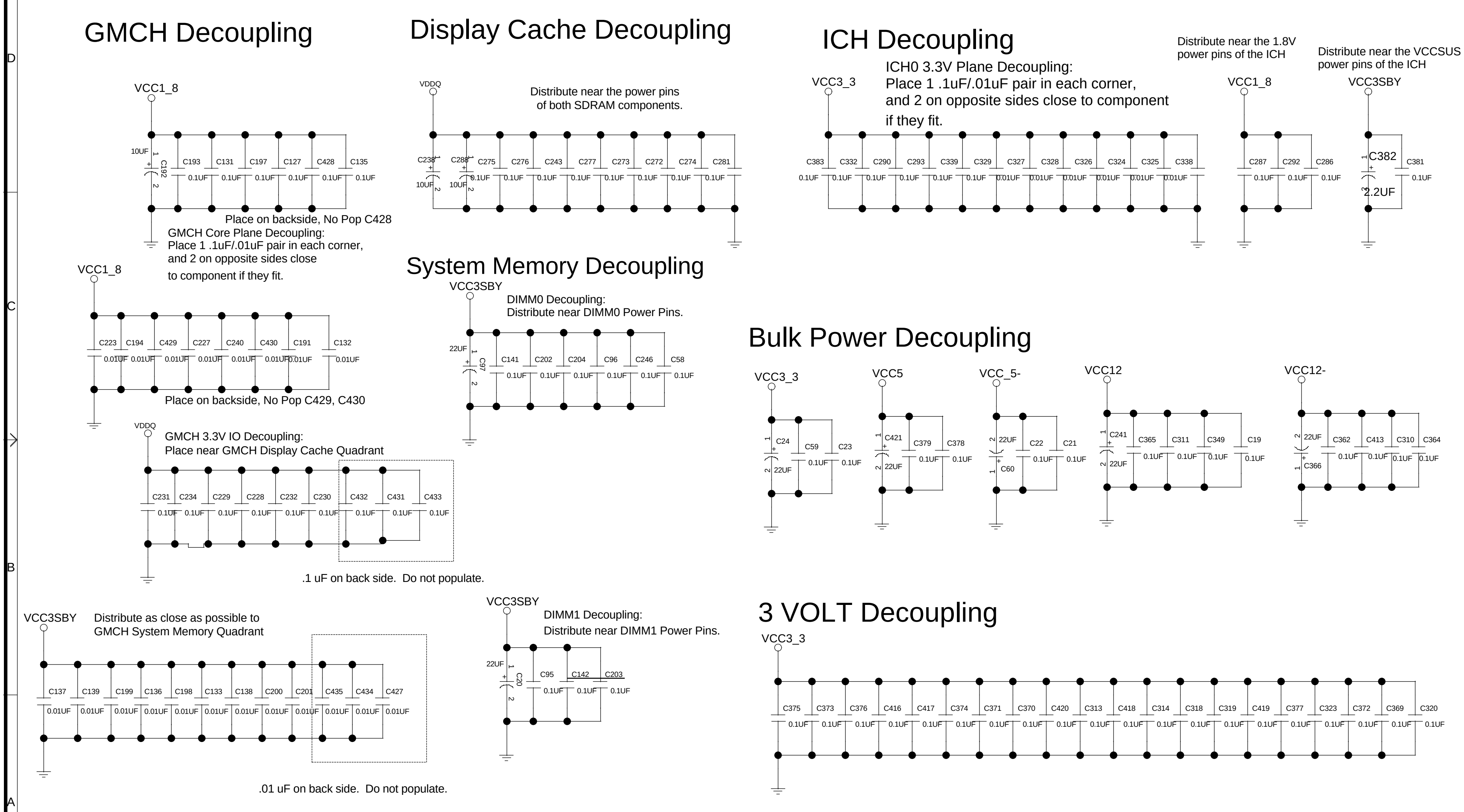
REV: 1.0

PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630

DRAWN BY: INTEL (R) PCG
LAST REVISED: 5-15-00

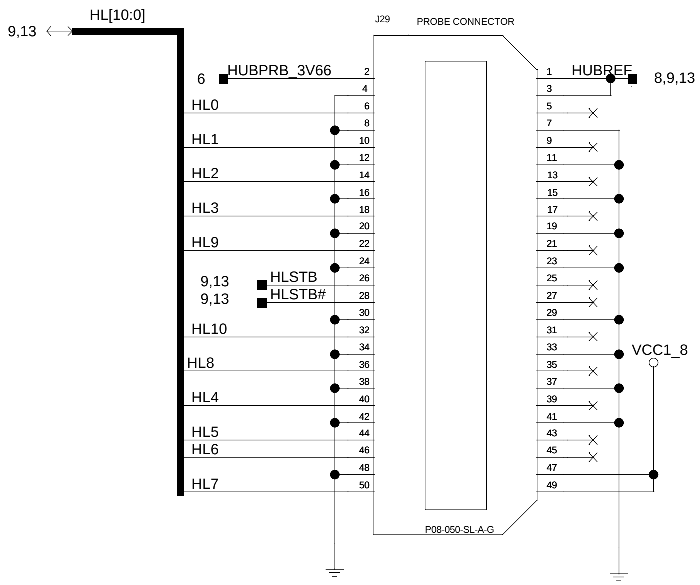
PROJECT: INTEL(R) 82815
SHEET: 38 OF 41

DRAM, Chipset, and Bulk Power Decoupling



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD DRAM, ICH, AND GMCH DECOUPLING		REV: 1.0
intel PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 39 OF 41

Hub Interface Connector



INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD

DISPLAY CACHE

REV: 1.0

PCG PLATFORM DESIGN
1900 PRAIRIE CITY RD
FOLSOM, CA 95630

DRAWN BY: INTEL (R) PCG

LAST REVISED: 5-15-00

PROJECT: INTEL(R) 82815

SHEET: 40 OF 41

Revision History

- Initial release revision 1.0

INTEL(R) 82815 CHIPSET CUSTOMER REFERENCE BOARD REVISION HISTORY		REV: 1.0
intel© PCG PLATFORM DESIGN 1900 PRAIRIE CITY RD FOLSOM, CA 95630	DRAWN BY: INTEL (R) PCG LAST REVISED: 5-15-00	PROJECT: INTEL(R) 82815 SHEET: 41 OF 41