Intel® 860 Chipset Memory Expansion Card (MEC)

Design Guide

May 2001

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Revision History

Rev. No.	Description	Date
-001	Initial Release.	May 2001

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1 Introduction

This document provides design guidelines for developing a Memory Expansion Card (MEC). These memory cards will be designed to support PC800 RDRAM* devices when interfacing with the Intel® 860 chipset. These Direct RDRAM device-based MECs are intended as the main memory subsystem for workstation and server designs.

This design guide organizes Intel's design recommendations for memory expansion cards. In addition to providing expansion card design recommendations (e.g., layout and routing guidelines) this document also addresses system design issues. Design recommendations, board schematics, debug recommendations and a MEC checklist are provided. The design recommendations should be followed strictly for all MEC designs. These design guidelines have been developed to ensure maximum flexibility for MEC designers while reducing the risk of board-related issues.

The schematics for a Memory Expansion Card are provided in Appendix A and are intended as a reference for MEC board designers. The schematics provide a reference for a Direct RDRAM device-based MEC. Additional flexibility is possible through other permutations of these options and components.

1.1 Terminology

Term	Description
Direct RDRAM	
RSL	Rambus Signaling Level. RSL is a multi-drop, bidirectional bus connection signaling technology. Operating up to a GHz transfer rate, RSL uses low swing signaling, a common reference voltage and precise clocking to transfer two bits per clock cycle.
Rclk	Rclk refers to the RSL bus high-speed clock in a generic fashion, often in the context of clock counts in timing specifications.
RAC	Direct RDRAM ASIC Cell. It is the embedded cell designed by Direct RDRAM Rambus* ASIC Cell. The RAC is a library macrocell used in ASIC controller designs to interface the core logic of a CMOS ASIC device to the Rambus Channel. It is the embedded cell designed by Rambus that interfaces with the Direct RDRAM* devices using RSL signaling. The RAC communicates with the RMC.
RMC	Rambus* Memory Controller. The RMC is a block of digital logic residing on a Rambus-based controller IC to drive and manage the memory transactions of a Rambus memory system. This is the logic that directly interfaces to the RAC.
RIMM* Connector	The Rambus RIMM connector provides the necessary mechanical and electrical interface for interfacing RIMM modules or Continuity RIMM modules to the Rambus Channel.
RIMM* Module	A RIMM module is a memory module consisting of RDRAM devices assembled on a specified PCB.

Term	Description
Components	
MCH	The Memory Controller Hub component that contains the processor interface, Direct RDRAM device controller, and AGP interface. It communicates with the I/O Controller Hub over a proprietary interconnect called “Hub Interface”.
MRH-R	The Intel® 82803AA Memory Repeater Hub for Direct RDRAM devices.
Expansion channel	The RSL bus that connects the MCH to the MRH-R. This term only applies to the interface between the MCH and MRH-R component.
Stick channel	An RSL Direct RDRAM device bus that connects the MCH to the MRH-R. This term only applies to the interface between the MCH and MRH-R component.
Rambus* Channel	The Rambus Channel consists of a two-byte wide data path capable of transferring data and address information at rates of 800MHz and beyond. The Rambus Channel has defined mechanical and electrical interfaces and consists of a memory controller, RDRAM devices, DRCG and all interconnect components.

1.2 Reference Documents

Title	Document Number
Intel® 82803AA Memory Repeater Hub for RDRAM (MRH-R) Datasheet	298022
Intel® 860 Chipset: 82860 Memory Controller Hub MCH Datasheet	290713
Intel® Xeon™ Processor and Intel® 860 Chipset Platform Design Guide	298252
Intel Impedance Test Methodology Document	http://developer.intel.com/technology/memory/rdram
Intel Controlled Impedance Design and Test Document	http://developer.intel.com/technology/memory/rdram
Rambus* RDRAM Device Documentation	www.rambus.com

NOTE: The related documents contain information that is critical to this design guide.

1.3 MEC Memory Components

A Memory Expansion Card can be used to increase memory size configurations that are required for most server and workstation designs. The Intel 82803AA Memory Repeater Hub for Direct RDRAM devices (MRH-R) provides memory expandability up to 4 GB. The MRH-R support includes:

- Support for PC800 Direct RDRAM devices
- Support for 128-Mbit and 256-Mbit Direct RDRAM device technologies
- 400 MHz Direct RDRAM device interface

2 Memory Expansion Card Ballout

2.1 Edge Connector Example Ballout

Contact your local Intel representative for an example ballout.

2.2 Edge Connector Ball Description

The following pin description is only for the balls that are required/recommended to implement a fully functional Memory Expansion Card using Intel chipsets.

2.2.1 RSL and CMOS Balls

Signal	Type	Description
CHx_EXP1	RSL	**Row Control:** This signal carries the row control packets from the memory controller to attached MRH-Rs only.
CHx_EXP0	RSL	**Column Control:** This signal carries the column control packets from the memory controller to attached MRH-Rs only.
CHx_DQA[8:0]	RSL	**RDRAM Data Bus, Data Byte A:** Bi-directional 9-bit data bus A. These correspond to the CHx_DQA[8:0] signals on the MCH.
CHx_DQB[8:0]	RSL	**RDRAM Data Bus, Data Byte B:** Bi-directional 9-bit data bus B. These correspond to the CHx_DQB[8:0] signals on the MCH.
CHx_RQ[7:5]/ ROW[2:0]	RSL	**RDRAM Row Request:** These signals carry row request packets from the memory controller to the MRH-Rs.
CHx_RQ[4:0]/ COL[4:0]	RSL	**RDRAM Column Request:** These signals carry column request packets from the memory controller to the MRH-Rs.
CHx_CTM	RSL	**RDRAM Clock to MCH:** One of the two differential transmit clock signals used for MRH-R to MCH operations.
CHx_CTM#	RSL	**RDRAM Clock to MCH Complement:** One of the two differential transmit clock signals used for MRH-R to MCH operations.
CHx_CFM	RSL	**RDRAM Clock from MCH:** One of the differential receive clock signals used for MCH to MRH-R operation.
CHx_CFM#	RSL	**RDRAM Clock from MCH Complement:** One of the differential receive clock signals used for MCH to MRH-R operation.
CHx_SIO	CMOS	**RDRAM Serial IO Chain:** Serial input/output pins used for reading and writing control registers. These correspond to the SIO signals on the MCH.

Signal	Type	Description
CHx_SCK	CMOS	**RDRAM Serial Clock:** Clock source used to used for timing of the CHx_SIO and CHx_CMD signals. This corresponds to the SCK signal on the MCH.
CHx_CMD	CMOS	**RDRAM Serial Command:** Serial command input used for control register read and write operations. This corresponds to the CMD signal on the MCH.
SDA	CMOS	**SMBus Data:** SMBus interface for RIMM SPD and reading of any on-board FRU EEPROM.
SCLK	CMOS	**SMBus Clock:** SMBus clock used for timing on SDA.
SMBWE	CMOS	**Write Protect for SMBus EEROMS:** This signal is used to write protect all SMBus EEPROM devices to avoid SPD data corruption. This can be controlled by a system GPO.
M_SEL[1:0]	CMOS	**SMBus MUX Select:** These pins are used to control an SMBus Mux on an MRH-R MEC.
PWROK	CMOS	**PWROK for CMOS Shunting Logic on MEC:** The system PWROK signal is used to shunt the SCK CMOS signal to GND when entering/exiting the STR state. See Section 3.6.5 for details.
RESET#	CMOS	**Reset:** When asserted this signal will asynchronously reset the MRH-R logic. This is the system reset signal used for resetting the MCH, ICH, etc. **Note:** Review MRH-R documentation for proper RESET# recommendations for STR implementations.

NOTE: "x" denotes MCH 'Expansion' channel A and channel B.

2.2.2 Voltage/Ground References

Signal	Description
CHx_RAMREF_FM	**Source Generated RSL Reference Voltage (1.4V):** CHx_RAMREF_FM is from the voltage divider network near the memory controller on the motherboard to the MRH-R on the MEC.
CHx_RAMREF_TM	**Source Generated RSL Reference Voltage (1.4V):** CHx_RAMREF_TM is from the voltage divider network on the MEC to the memory controller on the motherboard.
1_8V	**1.8V Power Pins:** Power pins for the MRH-R and all Vterm (1.85 V) on the MEC.
12V	**12V Power Pins:** Power pins for the on-board DC-to-DC converter for 2.5 V (Direct RDRAM device) generation on the MEC.
3_3V	**3.3V Power Pins:** Power pins for the DRCG devices and SMBus interface.
GND	**Ground Pins:** Ground pins placed between all RSL signals.
5V SB	

NOTE: "x" denotes channel A and channel B.

3 MEC Layout and Routing Guidelines

This chapter describes layout and routing recommendations to ensure a robust MEC design. Follow these guidelines as closely as possible. Any deviations from the guidelines listed here should be simulated to ensure adequate margin is still maintained in a MEC design.

Caution: If the guidelines listed in this document are **not** followed, it is very important that thorough signal integrity and timing simulations are completed for each design. **Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely.** Any deviation from these guidelines must be simulated.

3.1 Routing Recommendations

For the Intel 860 chipset using a MEC, all RSL and clock signals must be routed stripline (inner layer) from the MCH-to-MEC connector.

3.2 General Recommendations

When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. In addition, the PCB should be fabricated as documented in Section 3.4.

All recommendations in this section (except where noted) assume wider traces in trying to achieve a 28 Ω Rambus* Channel impedance. If the trace width is greater than this recommendation, the trace spacing requirements must be adjusted accordingly (linearly).

Additionally, these routing guidelines are created using the stack-up described in Section 3.4. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

3.2.1 Test Coupon Design Guidelines

Characterization and understanding of the trace impedance is critical for delivering reliable systems at the increased bus frequencies. Incorporating a test coupon design into the MEC will make testing simpler and more accurate. The test coupon pattern must match the probe type being used.

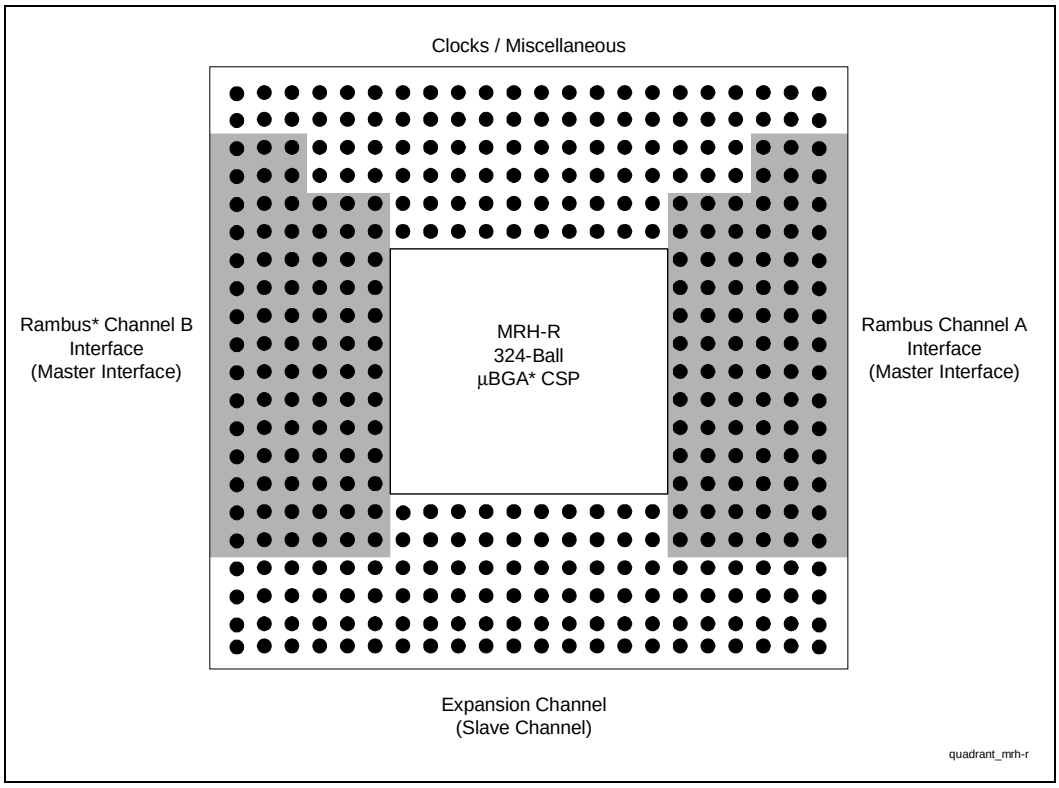
The *Intel Impedance Test Methodology* Document should be used to ensure the MEC are within the 28 Ω ±10% requirement. The *Intel Controlled Impedance Design and Test* Document should be used for the test coupon design and implementation. These documents can be found at:

http://developer.intel.com/design/chipsets/applnots/index.htm#rdram – Select "Application Notes"

3.3 Intel® 82803AA MRH-R Quadrant Layouts

The quadrant layouts shown in Figure 1 should be used to conduct routing analysis. These quadrant layouts are also designed for use during component placement.

Figure 1. 82803AA MRH-R 324-Ball µBGA*CSP Quadrant Layout (top view)



3.4 Printed Circuit Board Description

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM device interface to work properly. Maintaining 28 Ω ±10% loaded impedance for every RSL (Rambus Signaling Level) signal has changed the standard requirements for trace width and prepreg thickness across Intel chipset platforms and Memory Expansion Card designs.

A Memory Expansion Card printed circuit board stack-up recommendation calls for eight layers. However, the MEC design depends on the memory capacity required. The PCB stack-up must be designed to achieve the following calculated board characteristics (see examples below).

Table 1. PCB Calculated Parameters

Parameter	Min	Max	Notes
Propagation delay: S_0 (ps/in) (outer layers)	150	160	3
Propagation delay: S_0 (ps/in) (inner layers)	175	185	3
Trace impedance: Z_0 (Ω) (RSL signal layers: 28 Ω ±10%)	25.2	30.8	1, 2

NOTES:
1. Required Dielectric: 4.1 to 4.3.
2. This is a strict requirement for routing all RSL signals.
3. Assumptions based on stack-up examples below.

The following stack-up examples allow for a uniform channel impedance of 28 Ω ±10%. Typically, to achieve 28 Ω nominal impedance with a standard prepreg requires wider traces (i.e., 28 mils wide with 7 mil standard prepreg thickness). Wider traces can make it difficult to break out of and break into the rows of RSL signals on the MRH-R. To reduce the trace width, a thinner prepreg is required. This thinner prepreg allows smaller trace widths to meet the 28 Ω ±10% nominal impedance requirement (i.e., 18 mil wide traces).

Figure 2 is an example of a 6-layer stack-up that can be used to design a MEC using the MRH-R component.

Assumptions

1. Example stack-up should meet the RSL impedance requirement of 28 Ω ±10% on inner/outer signal layers.
2. Recommend routing all RSL signals referenced to a GND plane to insure proper current return paths.
3. 18 mil wide RSL traces on outer layers.
4. 12–15mil wide RSL traces on inner layers.

Figure 2. Example 6-Layer Direct RDRAM Device-Based MEC PCB Stackup

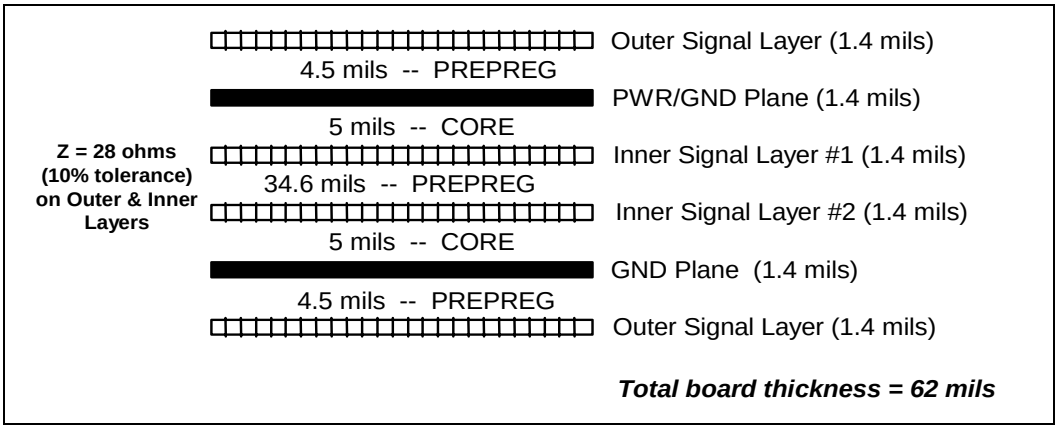
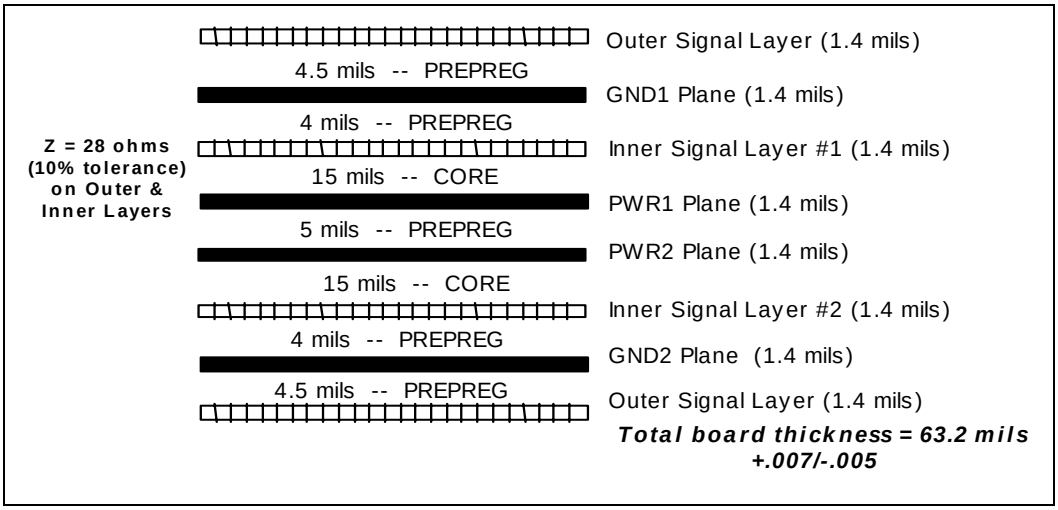


Figure 3 is an example of an 8-layer stack-up that can be used to design a MEC using the MRH-R.

Assumptions

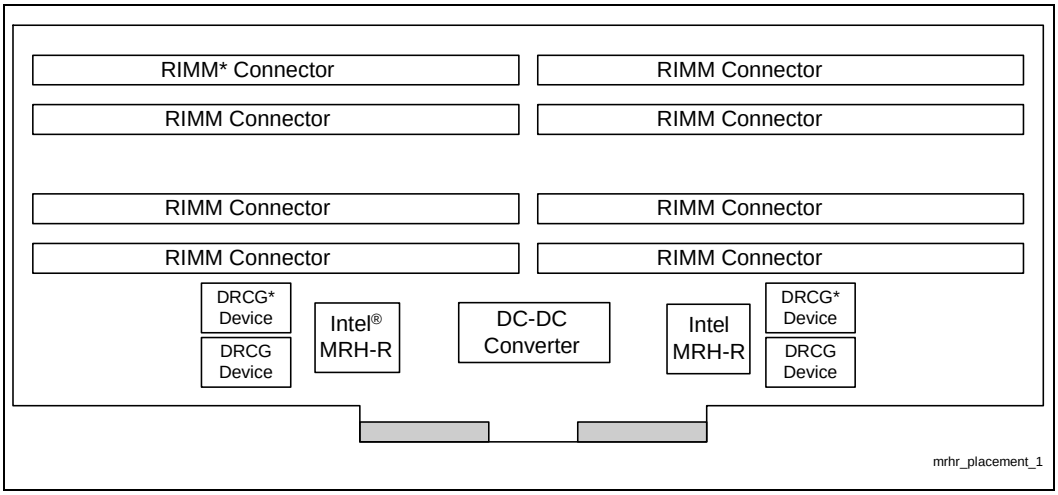
1. Example stack-up should meet the RSL impedance requirement of 28 Ω ±10% on inner/outer signal layers.
2. Recommend routing all RSL signals referenced to a GND plane to insure proper current return paths.
3. 18 mil wide RSL traces on outer layers.
4. 12.5 mil wide RSL traces on inner layers.

Figure 3. Example 8-Layer RDRAM Device-Based MEC PCB Stackup



3.5 MEC Component Placement

Figure 4. Example 8 RIMM* Connectors / 2 Intel® MRH-R MEC Component Placement



NOTES:

1. The component placements and layout shown in Figure 4 is conceptual.
2. The trace length limitation between critical connections will be addressed later in this document.
3. This placement was chosen based on the Intel 860 chipset customer reference board (CRB). The RIMM connector on the CRB needed to be placed higher so the processor heatsink would not interfere with the RIMM connectors.

3.6 Rambus* Channel Overview

The Rambus Channel is a multi-symbol interconnect. Due to the length of the interconnect and the frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. The driving device sends the next data out before the previous data has left the bus.

The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in signal reflections is required. The interconnect transmission lines must be terminated at their characteristic impedance; otherwise, the signal reflections resulting from a mismatch in impedance will degrade signal quality. These reflections will reduce noise, timing margins and the maximum operating frequency of the bus. Potentially, the reflections could create data errors.

Due to the tolerances of components (e.g., PCBs, connectors, and termination resistors), there will be noise on the interconnect. In this multi-symbol interconnect, timings are pattern dependent due to the reflections interfering with the next transfer.

Additionally, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source synchronous designs, the odd and even mode propagation velocity change creates skew between the clock and data or command lines that reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease crosstalk, as well as the other sources of skew.

To achieve these bus requirements, the Rambus Channel is designed to operate as a transmission line. All components, including the individual Direct RDRAM devices, are incorporated into the design to create a uniform bus structure that can support repeater hubs running at 800 MegaTransfers/second (MT/s).

3.6.1 Rambus* Channel Layout Guidelines

The signals on the Rambus Channel are broken into three groups: RSL signals, CMOS signals, and clocking signals. The signal groups are listed in Table 2.

Table 2. Rambus* Channel Signal Groups

RSL Signal	CMOS Signals	Clocking Signals
DQA[8:0]	CMD[1]	CTM
DQB[8:0]	SCK[1]	CTM#
RQ[7:0]	SIO	CFM
		CFM#

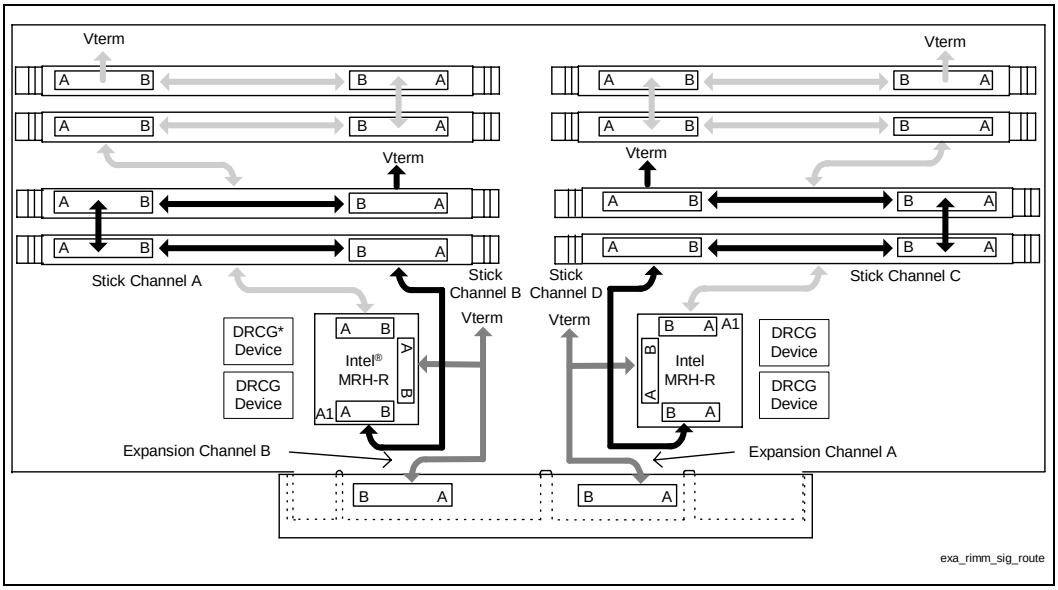
NOTES:
1. High-speed CMOS signal

3.6.1.1 RSL Signal Routing (MEC Expansion Channels and Stick Channels)

To ensure a solid memory subsystem design, the RSL signal routing rules need to be followed for both inner layer (microstrip) and outer layer (stripline) routing to the “expansion” and “stick” channels.

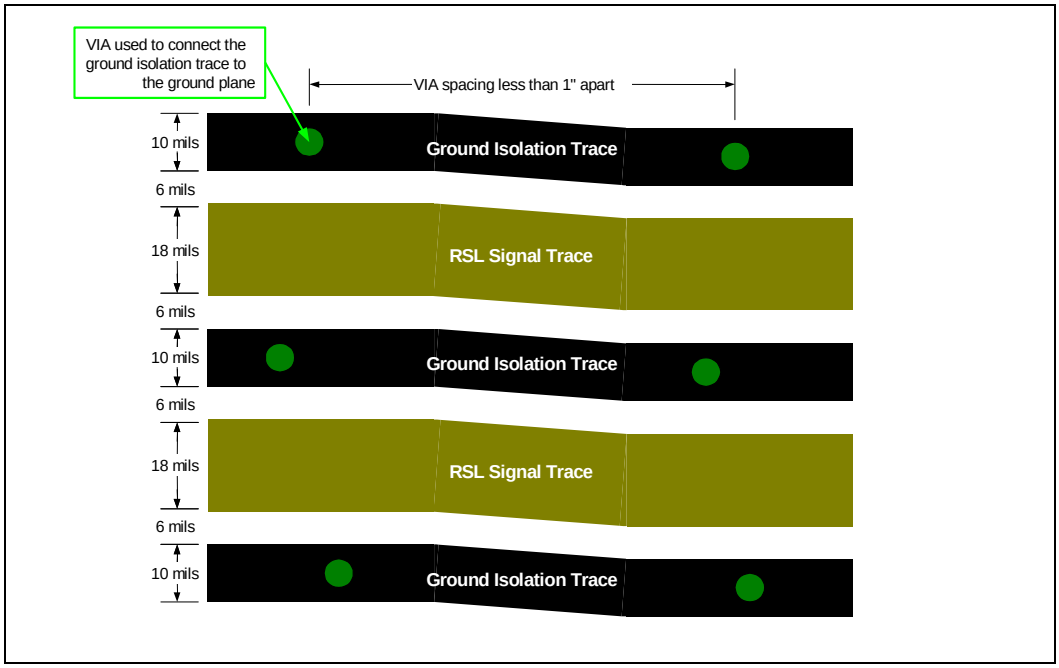
Figure 5 shows an example layout of the expansion and stick channel for a two MRH-R card.

Figure 5. Example 8 RIMM Connectors/ 2 Intel® MRH-R MEC RSL Signal Routing



To control crosstalk and odd/even mode velocity deltas for both the expansion and stick channels, there must be a 10 mil ground isolation trace between adjacent RSL signals (see Figure 6). The 10 mil ground isolation traces must be connected to ground with vias distributed less than every 1 inch. A via must be placed within less than 0.5 inch of the beginning and end of the ground isolation trace. A 6-mil gap is required between RSL signals and the ground isolation trace.

Figure 6. RSL Routing Diagram Showing Ground Isolation Traces with Via Around RSL Signals



3.6.1.1.1 Stick Channel Routing

The stick channel RSL signals from the MRH-R enter the first RIMM connector on either side, propagate through the RIMM connector, and then exit on the opposite side. The signals continue through the second RIMM connector until they are terminated at Vterm. All unpopulated slots must have continuity modules in place to ensure that the signals propagate to the termination. However, the MRH-R has the added feature of allowing for its stick channels to be powered-down if not in use; thus, avoiding the population of continuity modules. For example, stick channel A can be populated with RIMM connectors and stick channel B can be powered off if not used.

Table 3 shows the trace length recommendations (trace lengths for stick channel RSL are microstrip/stripline independent).

Table 3. Recommended Trace Lengths for an Intel® MRH-R MEC Stick Channel

Reference Section	Trace Description	Trace Length (Inches)
A	MRH-R to 1st RIMM connector	0" to 3.8"
B	1st RIMM connector to 2nd RIMM connector	0.4" to 1.0"
C	2nd RIMM connector to Termination	0" to 2.0"

NOTES:
1. These numbers apply to both stick channels (A and B).
2. These numbers apply to a 2-RIMM connector per stick channel implementation

RSL signals must be length matched to ±10 mils in section "A" and ±2 mils in sections "B" using the trace length matching methods described in the next section. There is no trace length-matching requirement for traces in section 'C'. If signals are routed on inner and outer layers, the trace velocity differences needs to be accounted for to minimize channel skew. Refer to http://www.rambus.com/ for more information regarding the Direct RDRAM device technology.

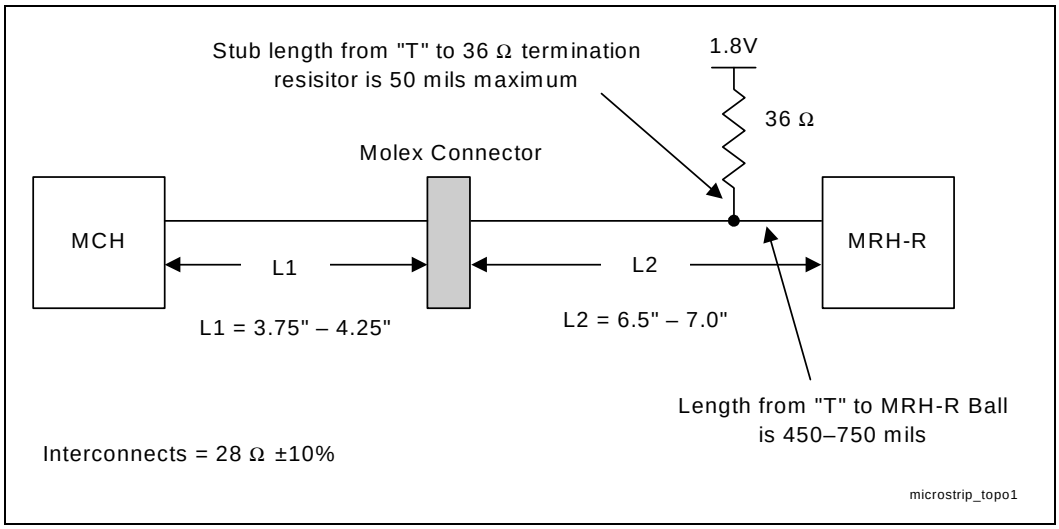
3.6.1.1.2 Expansion Channel Routing

The 'expansion' channel RSL signals are routed from the MCH to the MECC and from the MECC to the MRH-R. The signals from the MECC to the MRH-R are routed to a "T" junction where they get terminated to VTERM and proceed to the MRH-R. See Figure 5 for an example layout of the expansion channels for a two MRH-R card. The MECC-to-MRH-R portion of the 'expansion' channel can be routed microstrip or stripline. Simulations have found three microstrip topologies and three stripline topologies that will allow the expansion to work well. If the guidelines presented in this document are not followed, then the designer must perform appropriate simulations to ensure that a different topology will work.

Note: The path from MCH-to-MEC connector (represented by "L1" in the following six topology figures) lies on the motherboard and is always routed stripline. The path from MEC connector to the MRH-R (represented by "L2") lies on the expansion card and may be routed microstrip or stripline. Resistor "T" shown in the following figures has a 36 Ω value.

Microstrip MEC Routing Guidelines

Figure 7. Microstrip MEC RSL Routing Guidelines (Topology 1)



For outer layer (microstrip) RSL routing, an 18-mil wide trace allows for a 28 Ω channel impedance if using either the Direct RDRAM device-based MEC stack-up example defined in Figure 3 (8 layer). Three topologies are possible for microstrip routing; guidelines and trace lengths are indicated in Table 4, Table 5, and Table 6.

Table 4. Recommended Microstrip Intel® MRH-R Trace Lengths (Topology 1)

Route	From	To	Min (Inches)	Max (Inches)	Notes
Expansion Channel	MCH	Card Edge Fingers	3.75”	4.25”	1
Expansion Channel	Card Edge Fingers	MRH-R	6.5”	7.0”	1,2
Expansion Channel	Resistor - T	MRH-R	0.45”	0.75”	1,2
Expansion Channel	Resistor - T	Resistor	0.00”	0.05”	1,2

NOTES:
1. These numbers apply to both ‘expansion’ channels A and B.
2. These lengths include the RSL length matching as described in Section 3.6.1.2.1

Figure 8. Microstrip MEC RSL Routing Guidelines (Topology 2)

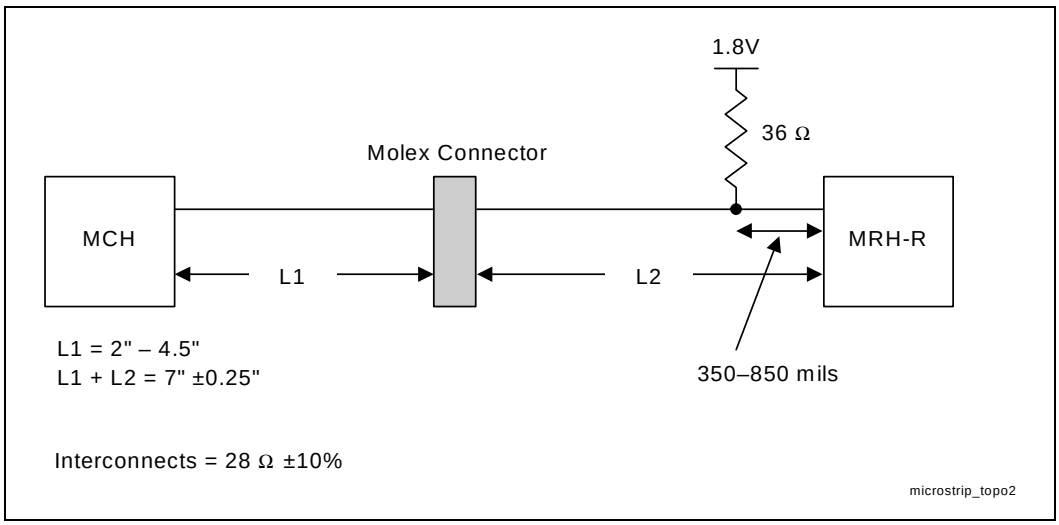


Table 5. Recommended Microstrip Intel® MRH-R Trace Lengths (Topology 2)

Route	From	To	Min (Inches)	Max (Inches)	Notes
Expansion Channel	MCH	Card Edge Fingers	2”	4.5”	1
Expansion Channel	MCH	MRH-R	6.75”	7.25”	1,2
Expansion Channel	Resistor - T	MRH-R	0.35”	0.85”	1,2
Expansion Channel	Resistor - T	Resistor	0.00”	0.05”	1,2

NOTES:
1. These numbers apply to both ‘expansion’ channels A and B.
2. These lengths include the RSL length matching as described in Section 3.6.1.2.1

Figure 9. Microstrip MEC RSL Routing Guidelines (Topology 3)

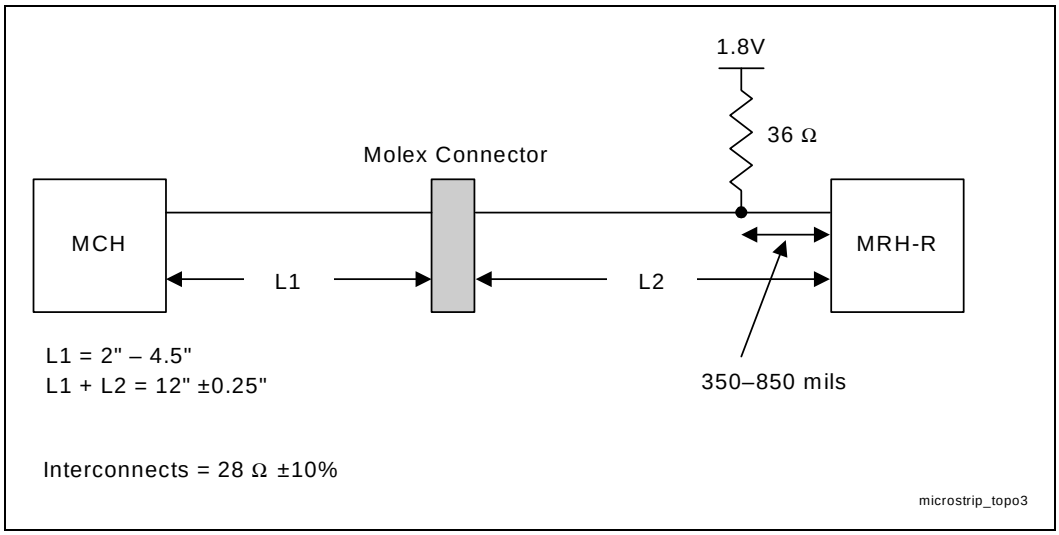


Table 6. Recommended Microstrip Intel® MRH-R Trace Lengths (Topology 3)

Route	From	To	Min (Inches)	Max (Inches)	Notes
Expansion Channel	MCH	Card Edge Fingers	2”	4.5”	1
Expansion Channel	MCH	MRH-R	11.75”	12.25”	1,2
Expansion Channel	Resistor - T	MRH-R	0.35”	0.85”	1,2
Expansion Channel	Resistor - T	Resistor	0.00”	0.05”	1,2

NOTES:
1. These numbers apply to both ‘expansion’ channels A and B.
2. These lengths include the RSL length matching as described in Section 3.6.1.2.1

Stripline MEC Routing Guidelines

For inner layer (stripline) RSL routing, the same routing methods apply as described for outer layer routing. Figure 3 shows a Direct RDRAM device-based MEC stack-up example using 12.5 mil-wide RSL traces when routing on inner layers for an 8-layer stackup.

Three topologies are possible for stripline routing. Guidelines and trace lengths are indicated in Table 7, Table 8, and Table 9

Figure 10. Stripline MEC RSL Signal Routing (Topology 1)

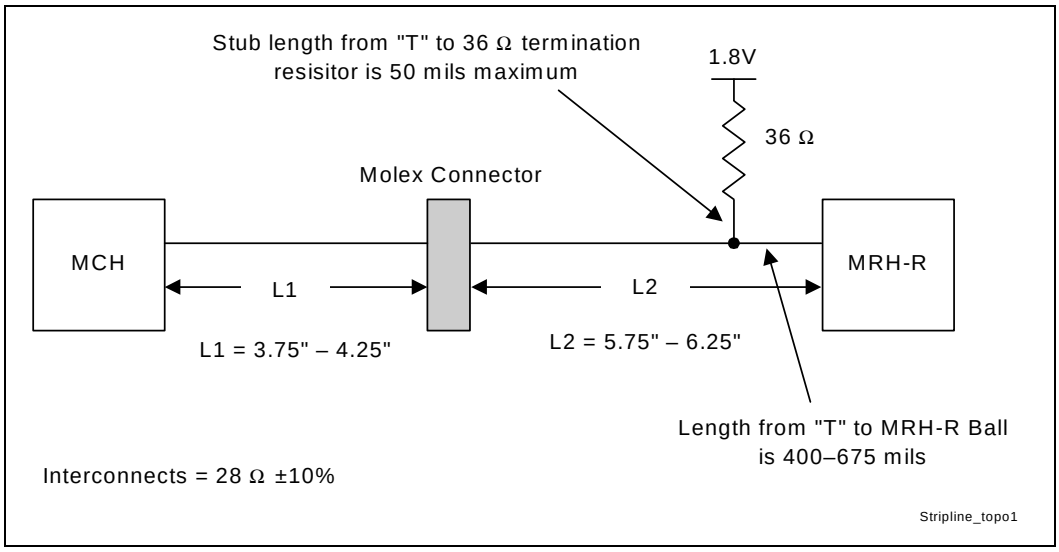


Table 7. Recommended Stripline Intel® MRH-R Trace Lengths (Topology 1)

Route	From	To	Min	Max	Notes
Expansion Channel	MCH	Card Edge Fingers	3.75”	4.25”	1
Expansion Channel	Card Edge Fingers	MRH-R	5.75”	6.25”	1,2
Expansion Channel	Resistor - T	MRH-R	0.40”	0.675”	1,2
Expansion Channel	Resistor - T	Resistor	0.00”	0.05”	1,2

NOTES:
1. These numbers apply to both ‘expansion’ channels A and B.
2. These lengths include the RSL length matching as described in Section 3.6.1.2.1.

Figure 11. Stripline MEC RSL Signal Routing Guidelines (Topology 2)

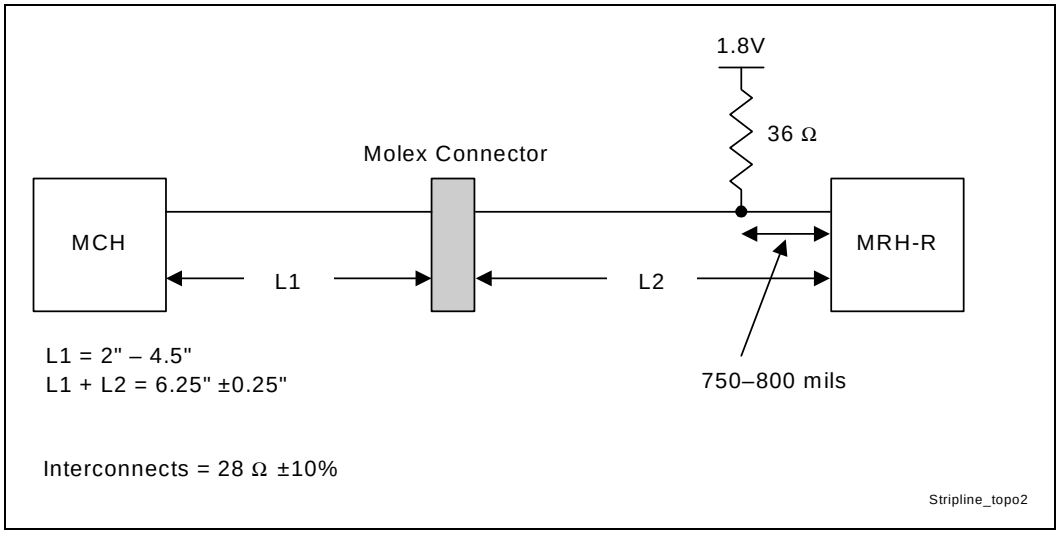


Table 8. Recommended Stripline Intel® MRH-R Trace Lengths (Topology 2)

Route	From	To	Min (Inches)	Max (Inches)	Notes
Expansion Channel	MCH	Card Edge Fingers	2”	4.5”	1
Expansion Channel	Card Edge Fingers	MRH-R	6.0”	6.5	1,2
Expansion Channel	Resistor - T	MRH-R	0.30”	0.75”	1,2
Expansion Channel	Resistor - T	Resistor	0.00”	0.05”	1,2

NOTES:
1. These numbers apply to both ‘expansion’ channels A and B.

These lengths include the RSL length matching as described in Section 3.6.1.2.1.

Figure 12. Stripline MEC RSL Signal Routing Guidelines (Topology 3)

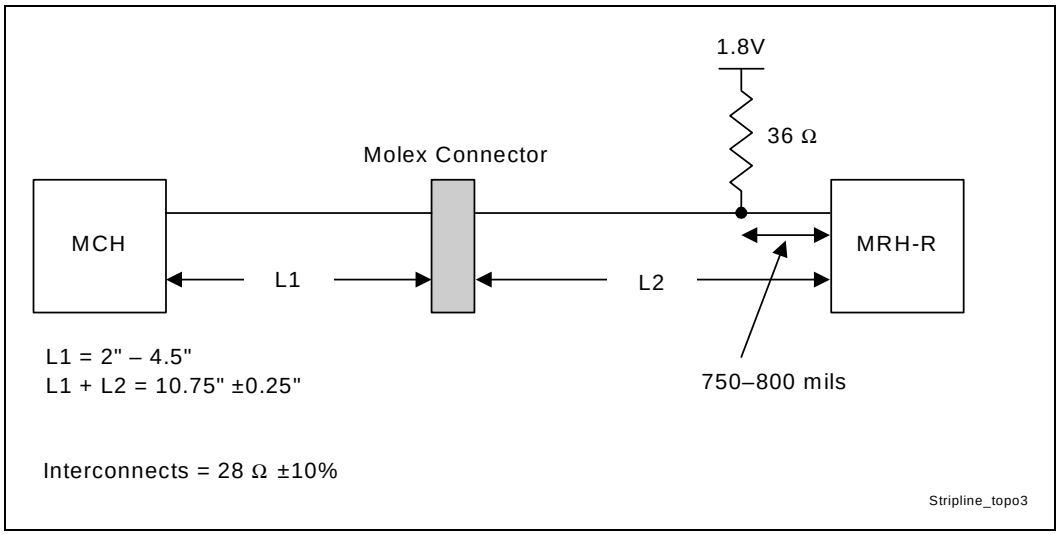


Table 9. Recommended Stripline Intel® MRH-R Trace Lengths (Topology 3)

Route	From	To	Min (Inches)	Ma (Inches)x	Notes
Expansion Channel	MCH	Card Edge Fingers	2”	4.5”	1
Expansion Channel	Card Edge Fingers	MRH-R	10.5”	11”	1,2
Expansion Channel	Resistor - T	MRH-R	0.30”	0.75”	1,2
Expansion Channel	Resistor - T	Resistor	0.00”	0.05”	1,2

NOTES:
1. These numbers apply to both ‘expansion’ channels A and B.
2. These lengths include the RSL length matching as described in Section 3.6.1.2.1

3.6.1.2 Rambus Signaling Level (RSL) Channel Compensation

The RSL and clocking signals require special compensation for any discontinuities introduced in the channel. Since the Rambus Channel has very little interconnect skew, it is critical to minimize skew and to match the skew on RSL and clocking signals within a given channel. The next few sections show how to compensate for skew due to package trace differences, vias, differential clock routing, and connector.

When compensating a channel, the compensating techniques must be performed in the following order:

1. Package trace compensation
2. Differential clock compensation
3. Via Compensation
4. Alternating signal layer for RIMM connector pin compensation
5. RIMM connector impedance compensation

3.6.1.2.1 Package Trace Compensation (Length Matching Method)

To allow for greater routing flexibility, the RSL signals require the following trace length matching methods:

1. *pad-to-pad* length matching between the MCH and MRH-R
2. *pad-to-pin* length matching between the MRH and the first RIMM connector.

If only the PCB trace lengths between the balls of the MCH and the balls of the MRH-R are matched, then the length mismatch between the pad (on the die) and the ball for each component has not been compensated. However, given the package dimension for each component, which is a representation of the length from the pad (on the die) to the ball, the PCB routing can compensate for this *package mismatch*.

The RSL channel requires matching trace lengths from *pad-to-pad* and *pad-to-pin* to within ±10 mils.

Definitions

- **Package Dimension (ΔL_{PKG}):** A representation of the length from the pad to the ball.
- **Board Trace Length (L_{MB})**: The trace length on the board.
- **Nominal RSL Length:** The length that all signals are matched. (Note: there is not necessarily a trace that is **exactly** to nominal length, but all RSL signals must be matched to within ±10 mils of a nominal length). The Nominal RSL Length is an arbitrary length (within the limits of the routing guidelines) that all the RSL signals will be matched (within ±10 mils).

Figure 13. Rambus* Channel Trace Length Matching Example from Intel® MRH-R-to-RIMM Connector

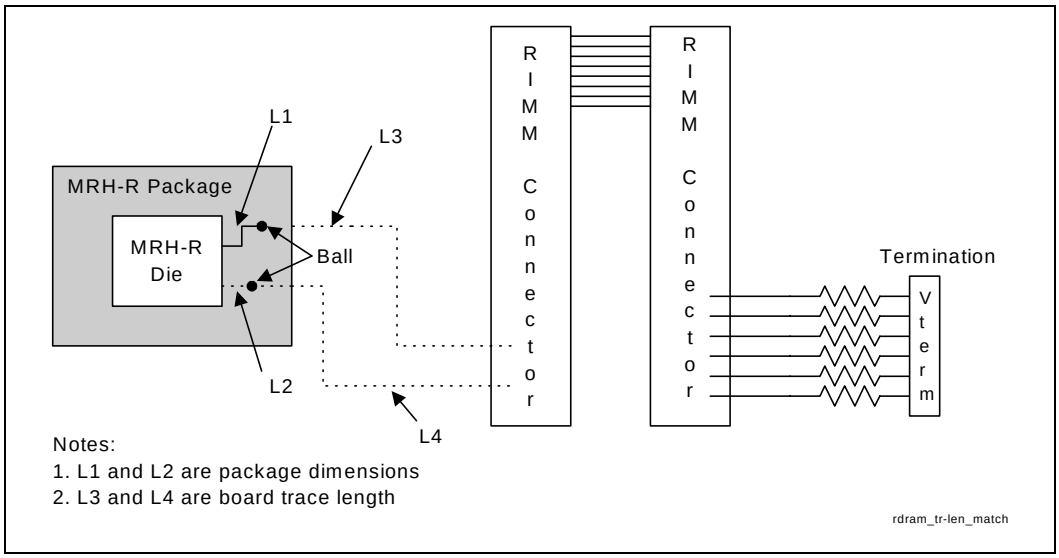
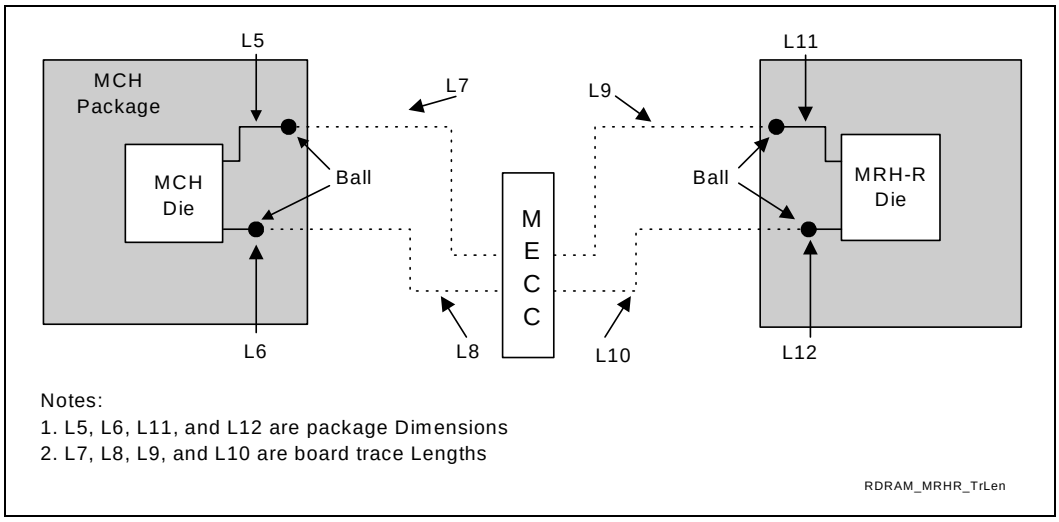


Figure 14. Rambus* Channel Trace Length Matching Example from MCH-to- Intel® MRH-R



RSL Signals Length Match Requirement

For stick channel RSL length compensation on a Memory Expansion Card, L1 and L3 must be length matched to L2 and L4 within ±10 mils. See Figure 13.

For expansion channel RSL length matching on a Memory Expansion Card between MEC connector and MRH-R, L11 and L9 must be length matched to L12 and L10 on the MEC within ±10 mils. Also, RSL signal length between the MCH die and MEC connector, L5 and L7 must be length match to L6 and L8 (see Figure 14).

Equation 1. Compensated Trace Length Calculation

$$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\ TRACE\_VELOCITY}) / PCB_{TRACE\_VELOCITY}$$

The PCB trace length for each signal is a calculated value and may vary with designs. The nominal MCH package trace velocity is 167.64 ps/in. $PCB_{TRACE\_VELOCITY}$ is board and layer dependent. $PCB_{TRACE\_VELOCITY}$ can change depending on which layer the board designer plans to route the RSL channel. Below are the $PCB_{TRACE\_VELOCITY}$ values for Stripline and Microstrip routing used on the Intel 860 chipset customer reference board (CRB).

- Stripline velocity typically equals 172 ps/in
- Microstrip velocity typically equals 154 ps/in

Refer to the appropriate Intel chipset datasheet for specific package information.

Note: The *Intel® 860 Chipset: 82860 Memory Controller Hub (MCH)* Datasheet provides signal lengths **Normalized to the longest** RSL trace length in each package. They do not represent the actual lengths from pad-to-ball. By normalizing to the longest length, PCB trace lengths can be reduced. Additional RSL length matching on the MEC is recommended, with the MRH-R.

The RSL signal lengths (ΔL_{PKG}) can be normalized to either the shortest or longest RSL trace using the following equation.

Equation 2. Normalized Trace Length Calculation

$$\text{New } \Delta L_{PKG} = \Delta L_{PKG} - \Delta L_{NORMALIZED\ RSL}$$

It is not necessary to account for CMOS signal package compensation. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as minimum as possible.

3.6.1.2.2 Differential Clock Compensation

Expansion Channel

The RDRAM clocks (CHx_CTM, CHx_CTM#, CHx_CFM and CHx_CFM#) routed from MECC-to-MRH-R must be longer than the Direct RDRAM device signals due to their increased trace velocity, if they are routed as a differential pair. Differential Clock Compensation **should not be done** for clock routing from MCH-to-MECC.

Equation 3. Clock Trace Length Calculation for Microstrip Routing

Clock Length = Nominal RSL Signal Length (package + card)* 1.03

- The compensation factor (1.03) is based on the 8-layer stack-up in Figure 3.

Equation 4. Clock Trace Length Calculation for Stripline routing

Clock Length = Nominal RSL Signal Length (package + card)* 1.00

- The compensation factor (1.00) is based on the 8-layer stack-up in Figure 3.

See Section 3.7, *RDRAM Clock Routing Guidelines*, for additional requirements.

Stick Channel

If the Direct RDRAM device clocks (CHx_CTM, CHx_CTM#, CHx_CFM, and CHx_CFM#) are routed differentially, the clock signals must be longer than the RSL signals due to their increased trace velocity because they are routed as a differential pair. To calculate the length for each clock use Equation 3 for microstrip and Equation 4 for stripline routing.

The lengthening of the clock signals, to compensate for their trace velocity change, only applies to routing between the MRH-R and first RIMM connector. The clock signals should be matched in length to the RSL signals between RIMM connectors.

See Section 3.7, *RDRAM Clock Routing Guidelines*, for additional requirements.

3.6.1.2.3 Via Compensation

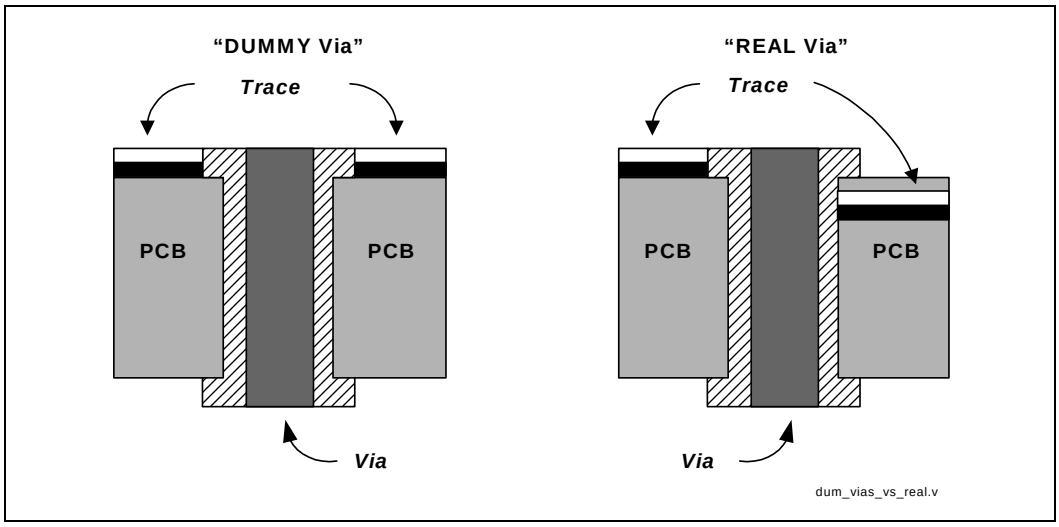
All RSL and clocking signals must have the same number of vias. As a result, each trace will have at least one via because some of the RSL signals must be routed on other layers of the motherboard. The via should be placed as close as possible to the MCH package ball. For the channel routed on outer layers, it will be necessary to place dummy vias on all signals routed on the top layer. The electrical characteristics between “dummy” and “real” vias are not exact, so additional compensation is needed on each signal that has a dummy via.

Dummy vias are not required on the channel routed on the inner layers (stripline) because all signals will require a real via.

Each signal with a dummy via must have 25 mils of additional trace length. The additional 25 mils trace length must be added to the signal routed on the top layer, after length matching.

“Real” via = “Dummy” via + 25 mils of trace length

Figure 15. "Dummy" vs. "Real" Vias

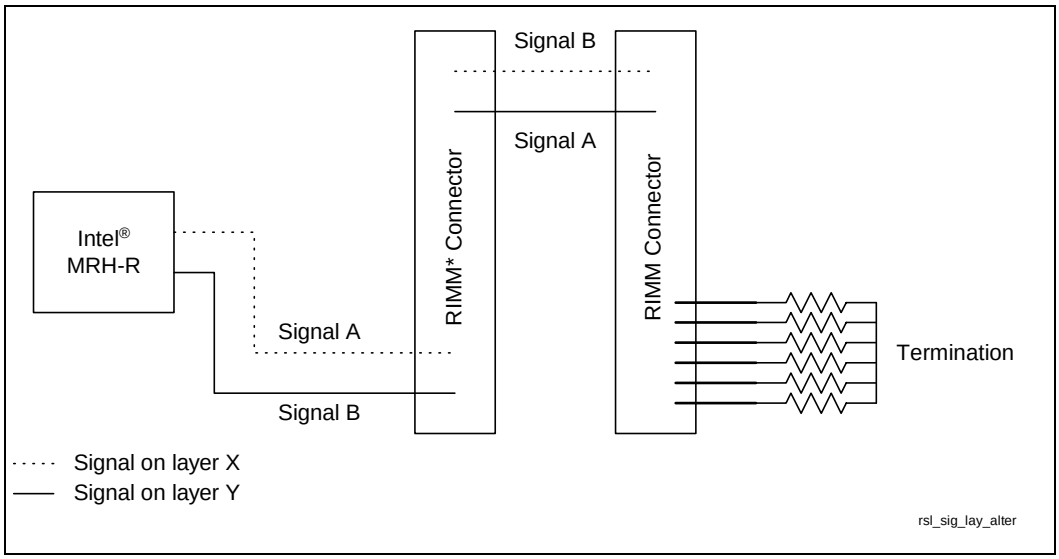


3.6.1.2.4 Signal Layer Alternation for RIMM Connector Pin Compensation

RSL and clocking signals must alternate layers as they are routed through the channel; this is to compensate for signals on the bottom layer having to travel a longer distance through the pin connector (see Figure 16). For example, if a signal is routed on the top layer from the MRH-R to the first RIMM connector, it must be routed on the bottom layer from the first RIMM connector to the second RIMM connector. This rule also holds true for inner layer routing. If a signal is routed on the top inner layer from the MRH-R to the first RIMM connector socket, it must be routed on the bottom inner layer from the first RIMM connector to the second RIMM connector.

All RSL and clocking signals from the second RIMM connector to the termination resistor should be routed on the top layer.

Figure 16. RSL Signal Layer Alternation



3.6.1.2.5 RIMM Connector Impedance Compensation

The RIMM connector inductance has been shown to cause an impedance discontinuity on the Rambus Channel. This can reduce voltage and timing margin. To compensate for the inductance of the connector, a compensating capacitance is required on each RSL and clocking connector pin. This compensating capacitance must be added to the following connector pins at each connector.

LCTM	LCFM	LROW[2:0]	RDQA[8:0]
LCTM#	LCFM#	RROW[2:0]	LDQA[8:0]
RCTM	RCFM	LCOL[4:0]	RDQB[8:0]
RCTM#	RCFM#	RCOL[4:0]	LDQB[8:0]

The copper tab area for the recommended stack-up was determined through simulation. The amount of capacitance required is determined by the layer the RSL or clocking signal is routed. The placement of the copper tabs can be on any signal layer, independent of the layer that the RSL signal is routed.

Capacitance for a different stack-up assuming a 62-mil board thickness can be computed by linear interpolation. The equation for determining the amount of capacitance needed on any stripline layer can be found by Equation 5.

Equation 5. Calculation for a Stripline CTAB

$$Ctab_{LayerX} = 0.8\ pF + (1.35\ pF - 0.8\ pF)(X/62)$$

- X = distance in mils from the top of the board to the stripline signal layer in which the RSL or clocking signals are routed.

Equation 6 is an approximation that can be used for calculating copper tab area on the microstrip (outer) layer.

Equation 6. Copper Tab Capacitance Calculation

$$Length * Width = Area = [C_{plate} * Thickness\ of\ prepreg] / [\varepsilon_0 * \varepsilon_r * 1.1]$$

- C_{plate} = Capacitance of the plates
- ε_0 = 2.25 x 10–16 Farads/mil
- ε_r = Relative dielectric constant of prepreg material
- Thickness of prepreg = Stackup dependent
- Length, Width = Dimensions in mils of copper plate to be added
- Factor of 1.1 accounts for fringe capacitance.

Table 10 provides an example calculation for a board where ε_r is 4.2 and thickness of prepreg is 4.5. Note that these numbers will vary with differences in prepreg thickness.

Table 10. Copper Tab Area Calculation

Layer	Dielectric Thickness	Separation Between Signal Traces & Copper Tab	Minimum Ground Flood	Air Gap between Signal & GND Flood	Compensating Capacitance in Cplate (pF)(1)	CTAB Area in sq mils
Top	4.5	6	10	6	0.80	~3463
Inner 1	4.5	6	10	6	0.90	~3896
Inner 2	4.5	6	10	6	1.25	~5300
Bottom	4.5	6	10	6	1.36	~5887

NOTES:
1. These numbers are based on an 8-layer stack-up.

More than one copper tab shape may be used as shown in Figure 17. The dimensions are based on copper area over the ground plane. Area over anti-pads does not count. The actual length and width of the tabs may be different due to routing constraints (e.g., if tab must extend to center of hole or anti-pad). Figure 17, Figure 18, and Figure 19 show a routing example of tab compensation capacitors.

The capacitor tabs must not interrupt ground floods around the RIMM connector pins; they must be connected to avoid discontinuity in the ground plane as shown.

Figure 17. Top Layer CTAB with RSL Signal Routed on the Same Layer (Ceff = 0.8 pF)

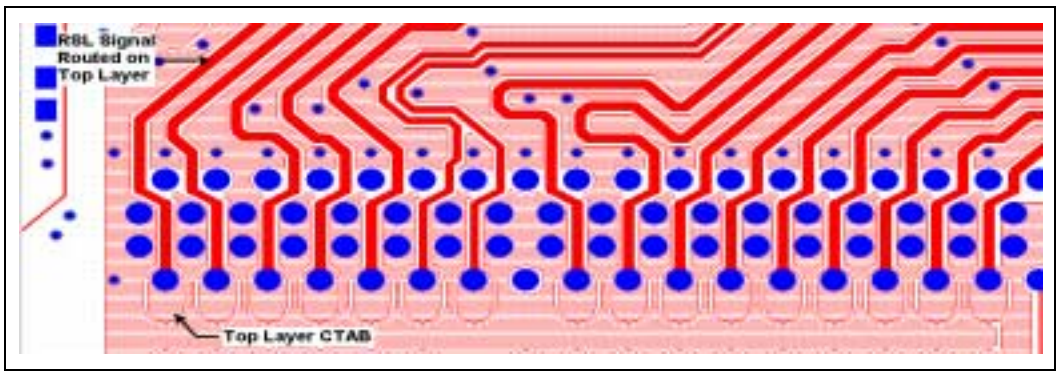
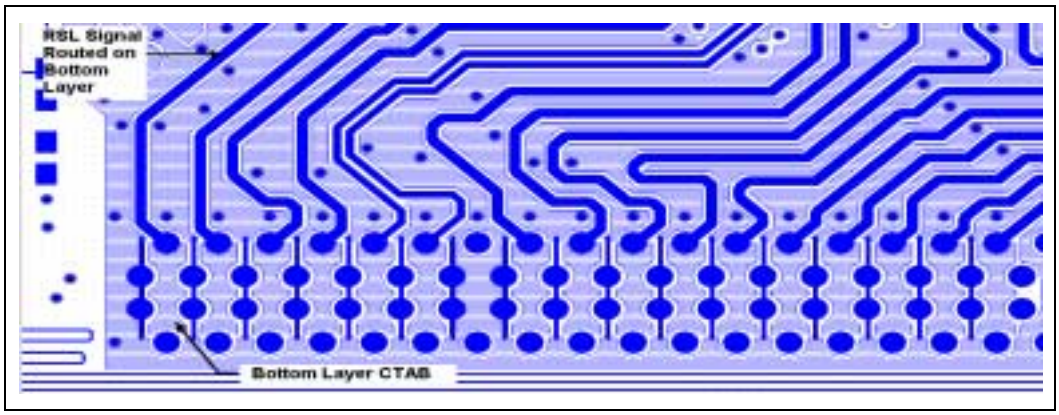
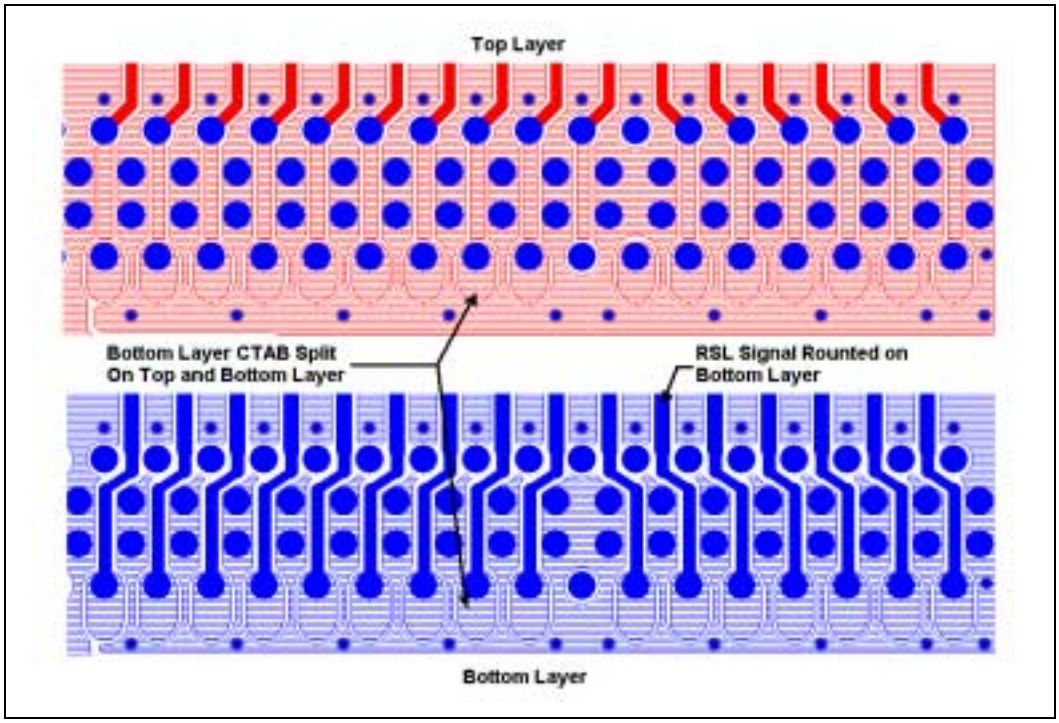


Figure 18. Bottom Layer CTAB with RSL Signal Routed on the Same Layer (Ceff = 1.35 pF)



The CTAB can be implemented on the multiple layers to minimize routing and space constrains. Figure 19 issues the use of CTABs on the top and bottom layer for bottom layer RSL and clocking signals routed between RIMM connectors.

Figure 19. Bottom Layer CTABs Split Across the Top and Bottom Layer (to Achieve Ceff ~1.35 pF)

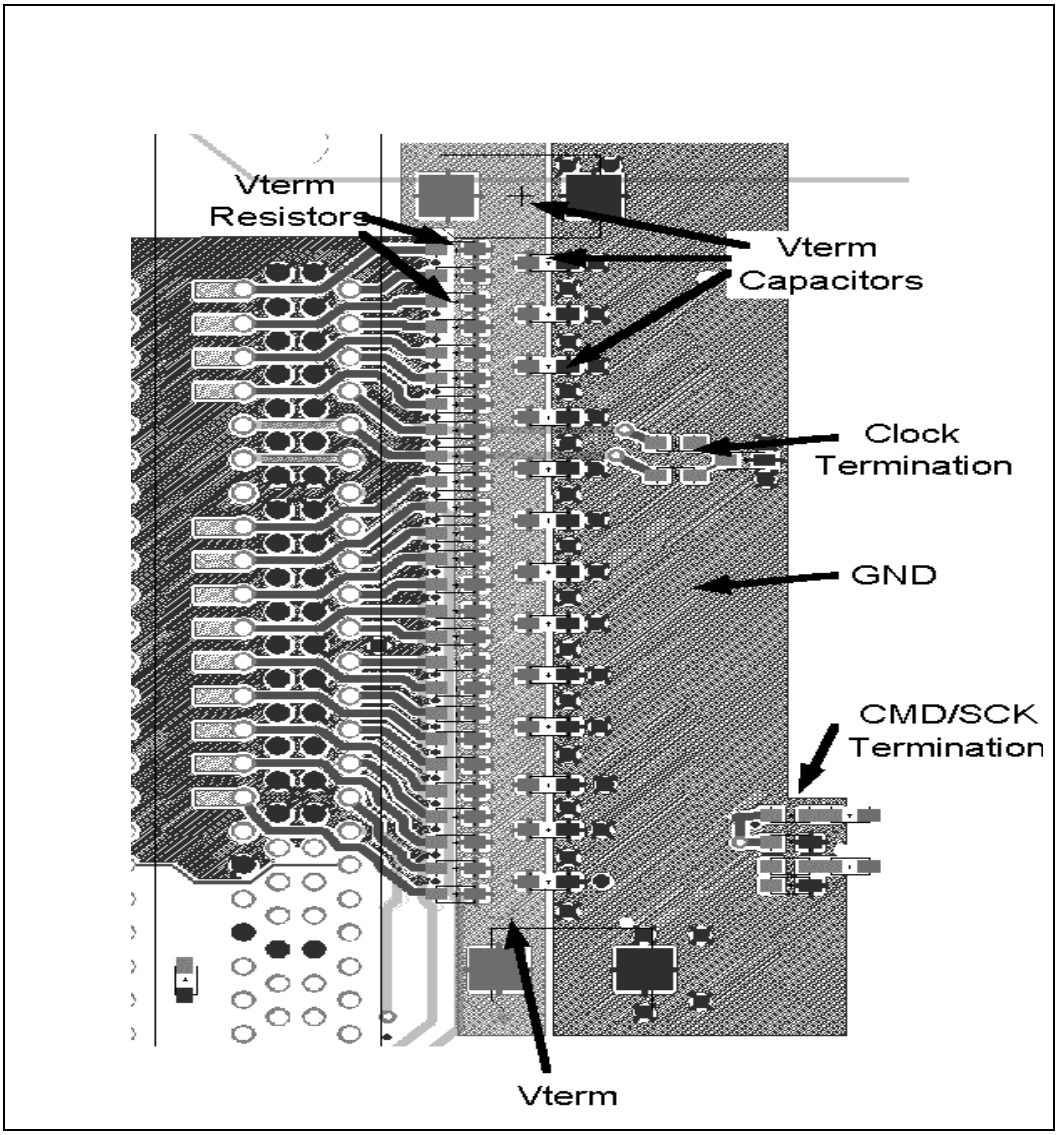


3.6.1.3 RSL Signal Termination

All RSL signals must be terminated to 1.8V (Vterm) on the Memory Expansion Card using 27 Ω ±1% or 28 Ω ±2% resistors at the end of both the 'expansion' channel opposite the MCH and at the end of the stick channels opposite the MRH-R. Discrete resistors are recommended.

Vterm must be decoupled using very high-speed bypass capacitors (one 0.1 µF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, two 100 µF tantalum capacitors of bulk capacitance are required. The trace length between the last RIMM connector and the termination resistors should be less than 2 inches. Length matching in this section of the channel is not required. The Vterm power island should be **at least** 50 mils wide. This voltage does not need to be supplied during a Suspend-to-RAM sleep state.

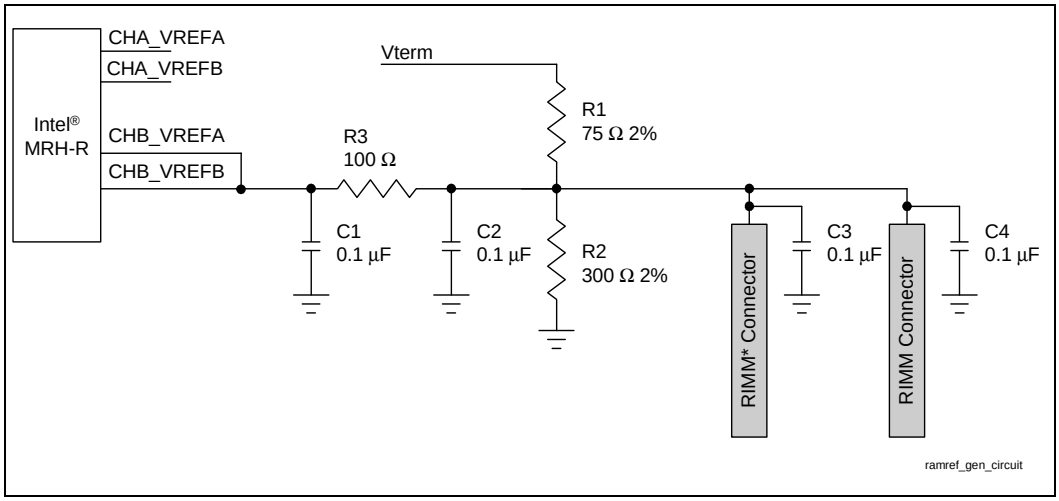
Figure 20. Direct RDRAM* Device Termination Example



3.6.2 Direct RDRAM Device Reference Voltage

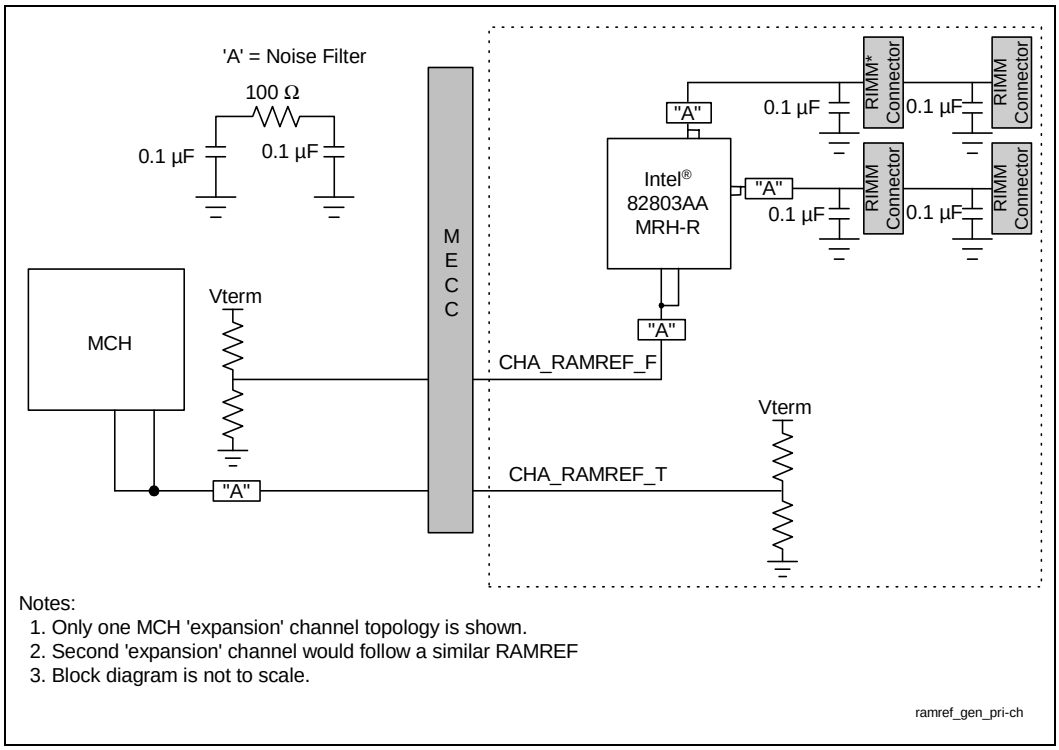
The Direct RDRAM device reference voltage (RAMREF) must be generated on all stick channels as shown in Figure 21. RAMREF should be generated from a resistor divider network using 2% tolerant resistors and the values shown. It is also recommended that a separate RAMREF resistor divider network for each MRH-R stick channel be implemented. Additionally, RAMREF should be routed with a 6-mil trace and must be properly decoupled. Finally, as shown in Figure 21, a noise filter network composed of a 100 Ω series resistor with two 0.1 µF capacitors is recommended near the CHx_VREF / EXVREF / RAMREF pins on the memory repeater hubs and near the CHx_REF pins on the MCH.

Figure 21. Secondary Rambus* Channel RAMREF Generation



The generation of RAMREF on ‘expansion’ channels is different. To account for potential differences between RAMREF and GND on the motherboard and on the memory expansion cards, Intel recommends using *source generated RAMREF* for the expansion channels. That is, the RAMREF signal is generated at the memory repeater hubs on the MEC and *sent* down the memory expansion card connector to the MCH; a separate RAMREF is generated on the motherboard at the MCH and *sent* up the memory expansion card connector to the repeater hubs. The signal names are EXVREFx for MRH-Rs where x-denotes the channel (refer to Figure 22).

Figure 22. Primary Rambus* Channel RAMREF Generation



There are four pins defined on the MEC connector pinout example to allow for this RAMREF passing. These pins are:

- CHx_RAMREF_TM RAMREF from the MEC to the chipset
- CHx_RAMREF_FM RAMREF from the chipset to the MEC

“x” denotes expansion channel A and B

The voltage divider network consists of DC elements as shown in Figure 21. The RAMREF divider network should be placed as close to the memory repeater hubs as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the RAMREF signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity. In addition the RAMREF signals should be routed with 6–8 mil wide traces.

3.6.3 High-Speed CMOS Routing

Due to the synchronous requirements between the RSL signals and the high-speed CMOS signals, these signals should be routed as part of the RSL channel. They must be impedance matched and properly terminated (using a **different** termination scheme than the RSL signals; see Figure 23).

It is not necessary to perform the length matching calculation (described in Section 3.6.1.2.1) for the high-speed CMOS signals. For routing on the motherboard, the mismatch between the CMOS signals (CMD and SCK) and the RSL signals should be kept to within 1200 mils (1.2 in) due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit. Route the

CMOS signals PCB with a trace length equal to the nominal RSL PCB trace length. The high-speed CMOS signals should be routed in their respective positions in the channel.

Figure 23. High-Speed CMOS Termination on Intel® MRH-R Stick Channels

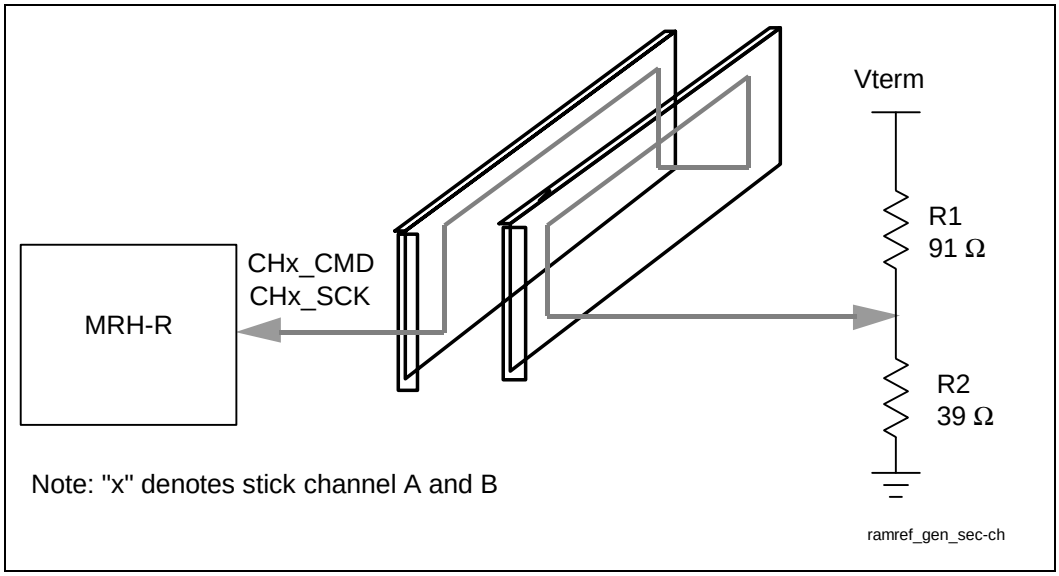
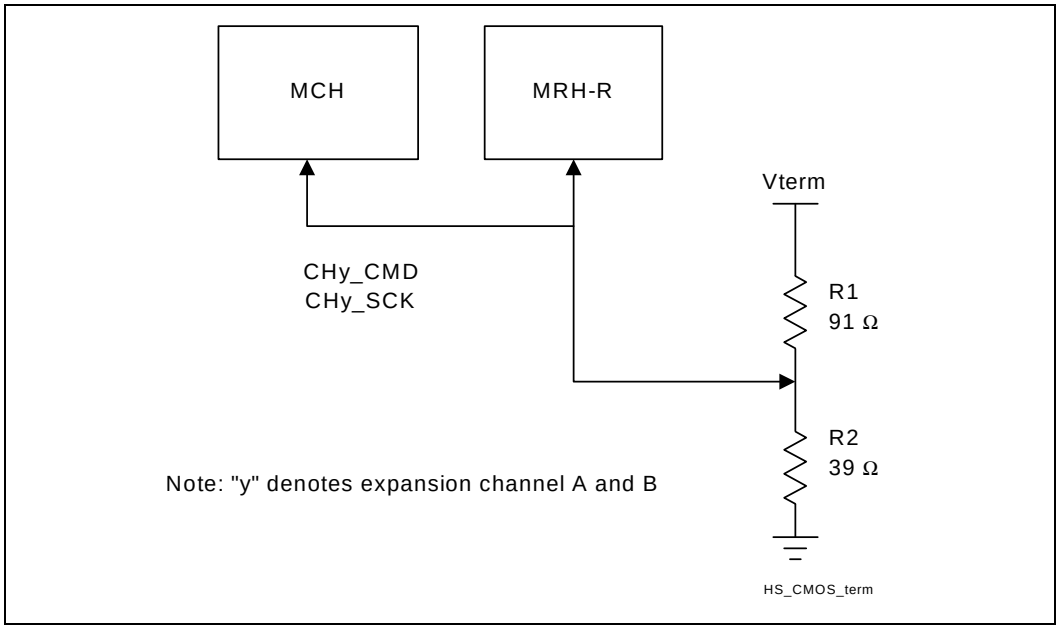


Figure 24. High-Speed CMOS Termination from MCH to Intel® MRH-R



A CMOS voltage must be supplied to each RIMM connector. This CMOS voltage is used by the Direct RDRAM devices CMOS interface. This voltage (Vcmos) must be 1.80V and the maximum load is 3 mA. Additionally, this voltage must be supplied during Suspend-to-RAM. Therefore, Vterm and Vcmos cannot be generated from the same source (i.e., they can not be the same power plane). Due to the low power requirements of Vcmos, it can be generated by a 36 Ω / 100 Ω resistor divider from 2.5V.

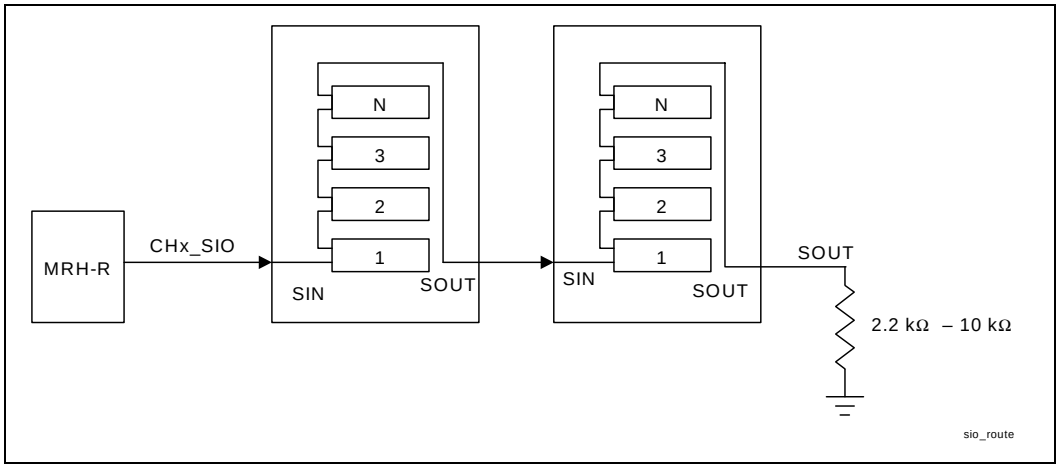
3.6.4 SIO Routing

The SIO signal is a bi-directional signal that operates at 1 MHz. The SIO signal enters the first RIMM connector, propagates through all the devices (this signal is buffered by each device) on the RIMM connector, and then exits the RIMM connector. The signal continues through the rest of the existing RIMM connectors and is terminated.

A pull-down through a 2.2 KΩ–10 KΩ resistor must be placed on the end of the SIO signal as shown in Figure 25.

The SIO signal is routed with a 5-mil wide 60-Ω trace with no need for ground isolation. Route from CHx_SIO (MRH-R) to SIN (RIMM #1, pin B36), from SOUT (RIMM #1, pin A36) to SIN (RIMM# 2, pin B36), and from SOUT (RIMM #2, pin A36) to termination.

Figure 25. SIO Routing Example



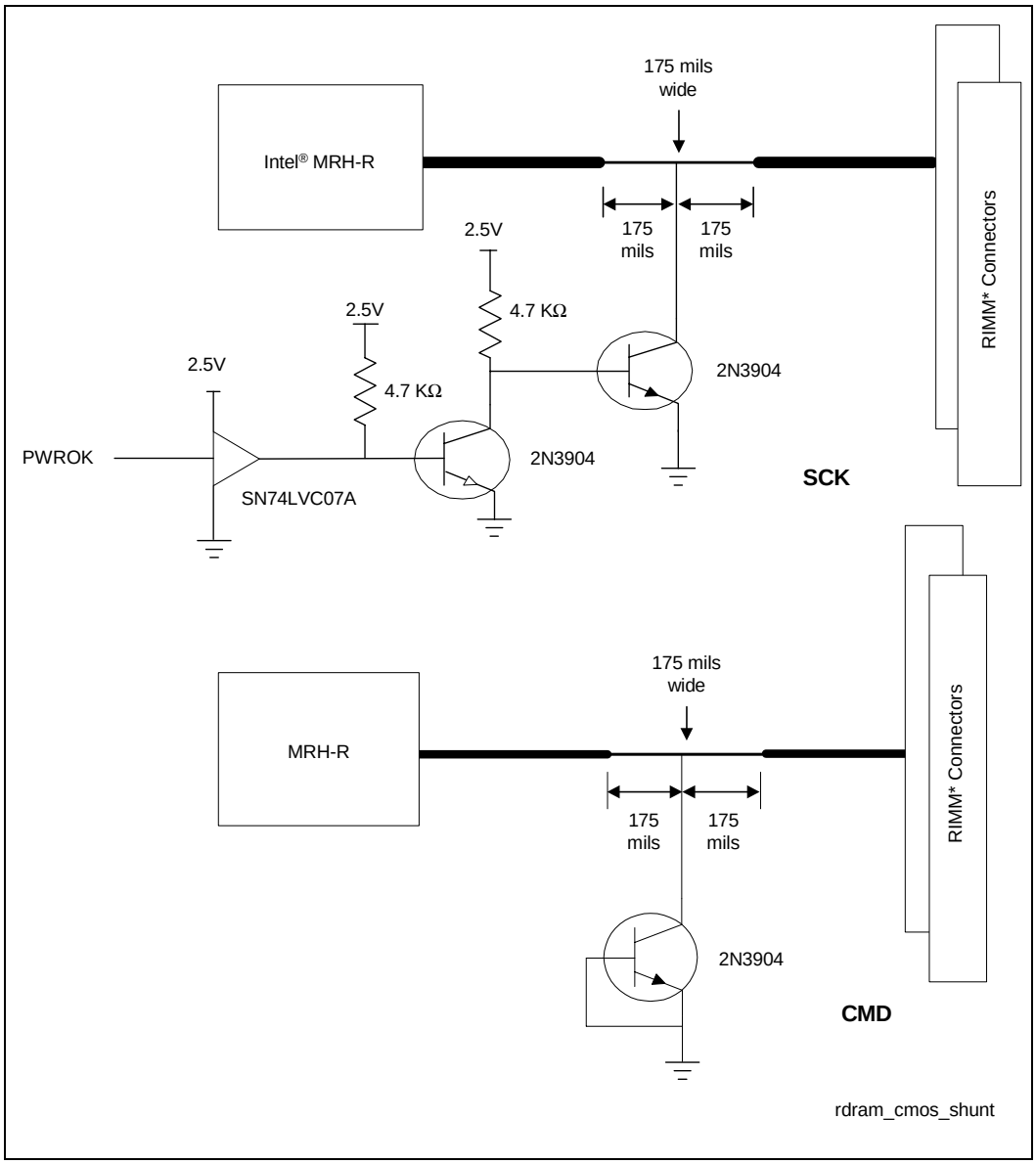
3.6.5 Suspend-to-RAM Shunt Transistor

When Intel Workstation/Server chipset-based systems enter or exit *Suspend-to-R*AM, power will be ramping to both the MCH and MRH-R (i.e., they will be powering up or powering down). When power is ramping, the state of the their CMOS outputs is not guaranteed. Therefore, the MCH could drive the CMOS signals through the MRH-R and issue some CMOS commands. One of the commands (the only one the Direct RDRAM devices would respond to) is the Powerdown Exit command. To avoid the MCH inadvertently taking the Direct RDRAM devices out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal must be shunted to ground when the MCH and MRH-R are entering and exiting *Suspend-to-RAM*. This shunting can be accomplished by placing the NPN transistor between the MRH-Rs and RIMM connectors as shown in Figure 26. The transistor should have a C_{obo} of 4 pF or less (i.e., MMBT3904LT1).

In addition, to match the electrical characteristics on the SCK signals, the CMD signals need a *dummy* transistor placed between the MRH-R and RIMM connectors. This transistor's base should be tied to ground (i.e., always turned off).

To minimize impedance discontinuities, the traces for the CMD and SCK signals should have a neckdown from the routed trace widths down to 5 mil traces for 175 mils on either side of the SCK/CMD attach points as shown in Figure 26.

Figure 26. Direct RDRAM* Device CMOS Shunt Transistor

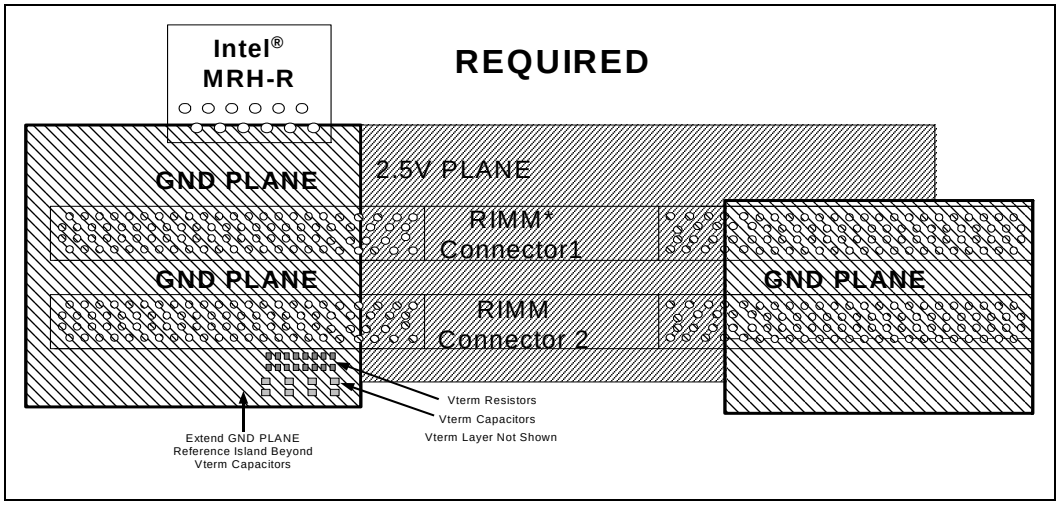


NOTE: This implementation is different from the MCH: A different shunt transistor is recommended.

3.6.6 Direct RDRAM* Device Ground Plane Reference

All RSL signals must be referenced to GND to provide an optimal current return path. The ground reference must be continuous from MRH-R to the RIMM connectors. This may require a GND reference island on the plane layers closest to the RSL signals. Choose the reference island shape such that power delivery to components is not compromised. By referencing all RSL signals to ground, the optimized current return paths will improve system operation.

Figure 27. MEC with Ground Reference for RSL Signals



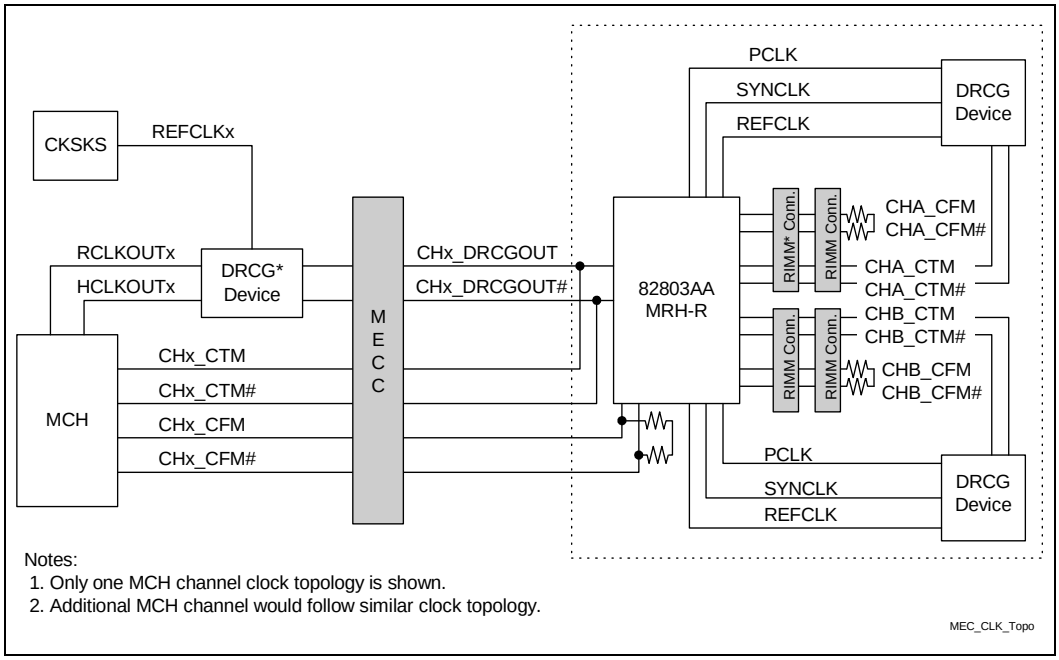
The ground reference island under the RSL signals **must** be connected to the ground pins on the RIMM connector and the ground vias used to connect the ground isolation on the outer layers. The Direct RDRAM device ground plane reference must be continuous to the Vterm capacitors.

The ground reference island under the RSL signals must be continuous from the last RIMM connector to the back of the termination capacitors. The return current will flow through the Vterm capacitors into the ground island and under the RSL traces. Any split in the ground island will provide a sub-optimal return path.

3.7 RDRAM Clock Routing Guidelines

Figure 28 shows a conceptual overview of the RDRAM-based Memory Expansion Card clock topologies.

Figure 28. RDRAM-Based MEC Clock Topology

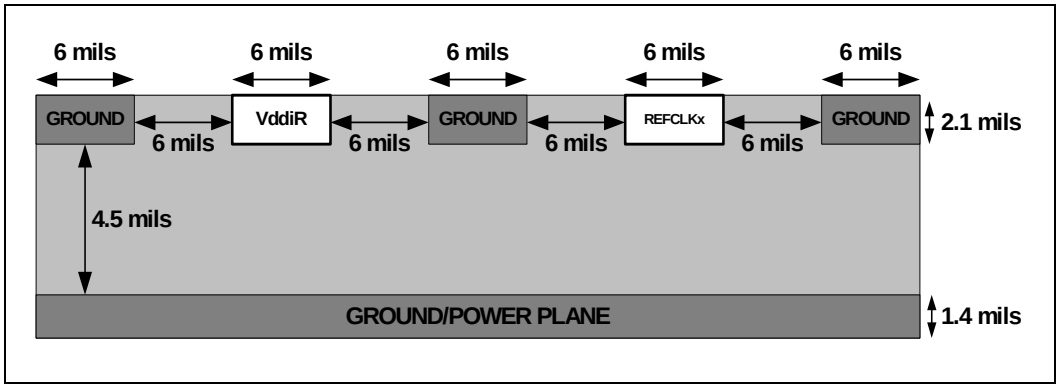


3.7.1 Intel® MRH-R to DRCG* Devices

3.7.1.1 REFCLKA and REFCLKB

VddiR is the 1.8 V line that is referenced by the REFCLKA and REFCLKB signals. An example of VddiR and REFCLKx routing is shown in Figure 29.

Figure 29. Intel® MRH-R to DRCG* Device Routing Example 1



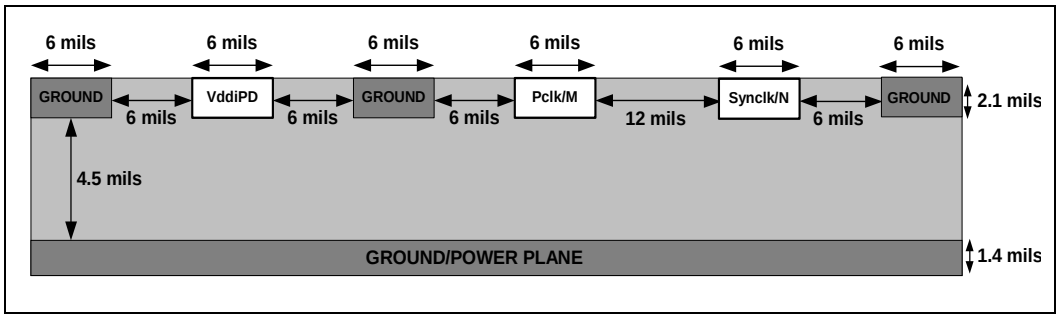
If a 1.8V plane can be placed near the DRCG device, then the VddiR pin should be connected directly to the 1.8V plane. However, it may be difficult to place a 1.8V power plane near the DRCG device. If necessary, a 1.8V trace (VddiR) should be routed from the 1.8V plane near the MRH-R to the DRCG device and routed as shown in Figure 29. VddiR should be decoupled with a 0.1 µF, 0603, ceramic chip capacitor.

The maximum routing length for REFCLKx is 8 inches.

3.7.1.2 PCLKMA, PCLKMB, SYNCLKNA, and SYNCLKNB

VddiPD is the 1.8V line that is referenced by the PCLKMA, PCLKMB, SYNCLKNA, and SYNCLKNB signals. An example of VddiPD, PCLKM and SYNCLKN routing is shown in Figure 30.

Figure 30. Intel® MRH-R to DRCG* Device Routing Example 2



If a 1.8V power plane can be placed near the DRCG device, then the VddiPD pin should be connected directly to the 1.8V plane. However, it may be difficult to place a 1.8V power plane near the DRCG device. If necessary, a 1.8V trace (VddiPD) should be routed from the 1.8V plane near the
MRH-R to the DRCG device and routed as shown in Figure 30. VddiPD should be decoupled with a 0.1 µF, 0603, ceramic chip capacitor. If VddiPD is connected to the 1.8V plane using a via (e.g., a trace is not run from the clock synthesizer), PCLK/M and SYNCLK/N (HCLKOUT and RCLKOUT) must still be routed differentially and ground isolated.

The PCLKM and SYNCLKN signals need to be routed on the same layer. If these signals need to be on different signal planes to escape the MRH-R, they must via back to the same layers after escaping the BGA package. If these signals must have vias, the via counts for these signals must be matched. Further, these signals should be run on the signal layer adjacent to a ground layer (refer to Section 3.4).

The maximum routing length for PCLKMx and SYNCLKNx is 6 inches. Additionally, PCLKMx and SYNCLKNx must be length matched (to each other) within 50 mils.

3.7.2 DRCG* Device to Rambus* Channel

The Direct RDRAM device clock signals (CHx_CTM/CTM# and CHx_CFM/CFM# on both the expansion channels and stick channels) are high-speed, impedance matched transmission lines. The Direct RDRAM device clocks begin at the end of the Rambus Channel and propagate to the MRH-R end as CHx_CTM/CTM#, where it loops back as CHx_CFM/CFM# to the Direct RDRAM devices and terminates at the end of the channel (see Figure 31). If any signals are routed on the top or bottom layers of the board from the 2nd RIMM connector to the termination, then the ground reference island must extend to the ground side of the termination capacitors.

Figure 31. Direct Rambus* Clock Generator (DRCG* Device) Routing Recommendations

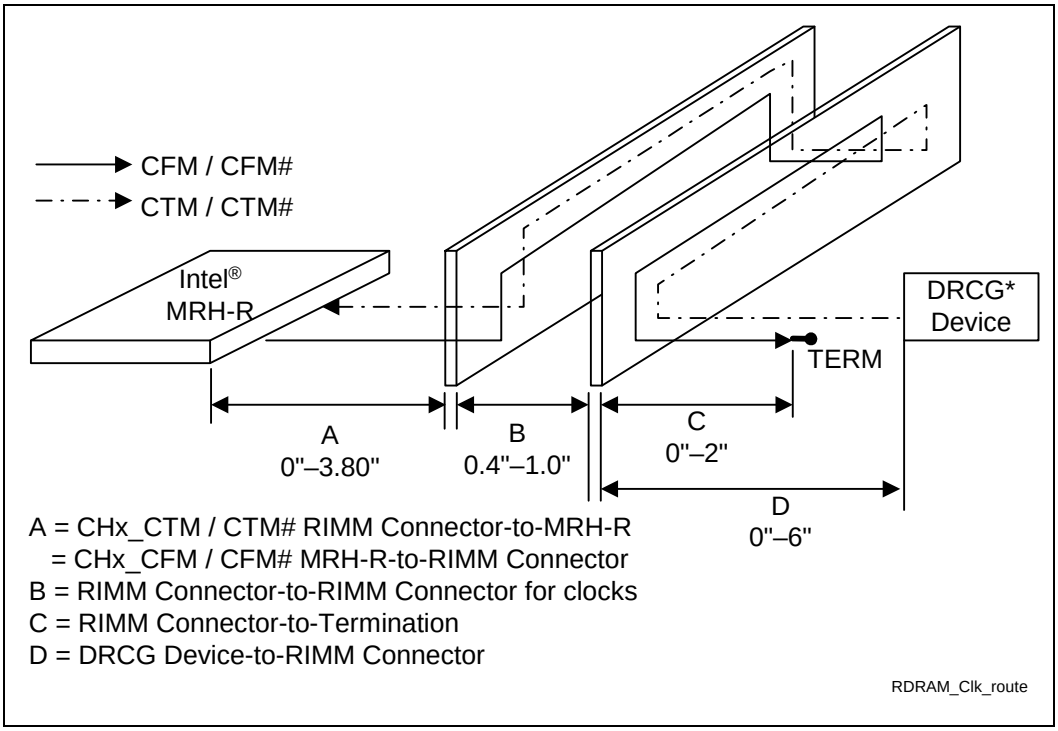


Table 11. Recommended Trace Lengths (Direct Rambus* Device Clock Generator Routing Length Guidelines)

Clock	From	To	Length (inches)	Section
CHx_CTM/ CHx_CTM#	DRCG Device	2nd RIMM Connector	0.000 – 6.000	D
	RIMM Connector	RIMM Connector	0.400 – 1.000	B
	1st RIMM Connector	MRH-R	0.000 – 3.800	A
CHx_CFM/ CHx_CFM#	MRH-R	1st RIMM Connector	0.000 – 3.800	A
	RIMM Connector	RIMM Connector	0.400 – 1.000	B
	2nd RIMM Connector	Termination	0.000 – 2.000	C

NOTE: "x" denotes stick channel A and B

Trace Geometry

In Sections labeled ‘A’ and ‘D’ in Figure 31, the clock signals (CHx_CTM/CTM# and CHx_CFM/CFM#) are routed differentially as shown in Figure 32. Sections ‘A’ and ‘D’ in the differential routing example are 14 mils wide in order to meet the 28 Ω channel impedance with the stack-up shown. There must be a ground isolation trace routed around the differential clock pair (22 mils wide as shown in the example in Figure 32). The ground isolation traces must be connected to ground with a via every 1 inch. A 6-mil gap is required between the clock signals (Note that this gap should be exactly 6 mil – not greater, not less). When these clocks are routed on outer layers, 0.021 inches of CLK trace per 1 inch of RSL trace length must be added to compensate for the clocks faster trace velocity on outer (Stripline) layers.

For section ‘B’ and ‘C’, the clock signals are routed non-differentially as shown in Figure 32. The clock signals in this section, as shown in the routing example, must be routed with 18 mil wide traces to meet the 28 Ω channel impedance. In addition, a ground isolation trace and a 6-mil gap between the ground isolation traces and the clock signals (same routing as RSL signals) are recommended. The ground isolation traces must also be connected to ground with a via every 1 inch.

Trace Length

For the section labeled “A” in Figure 31 (1st RIMM connector-to-MRH-R and MRH-R-to-1st RIMM connector), CHx_CTM/CTM# and CHx_CFM/CFM# must be length matched within ±2mils (exact trace length matching is recommended).

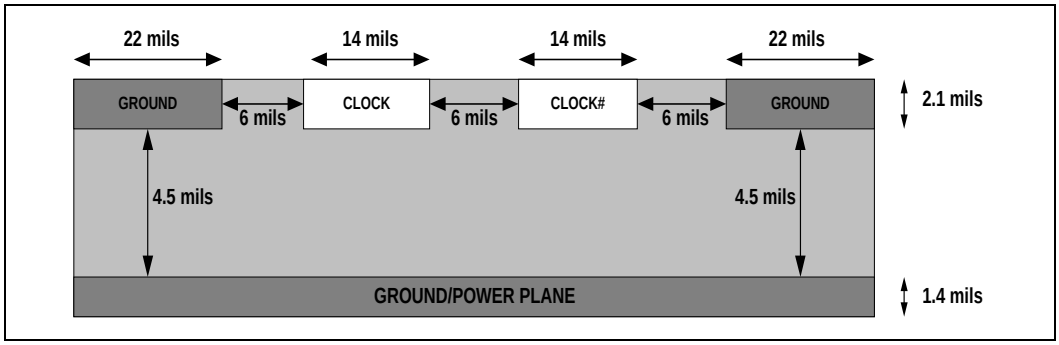
Package trace compensation (as described in Section 3.6.1.2.1), via compensation (as described in Section 3.6.1.2.3), Differential clock compensation (as described in Sections 3.6.1.2.2) and RSL signal layer alternation (as described in Section 3.6.1.2.4) must also be completed on the clock signals.

For the line sections labeled ‘B’ in Figure 31 (RIMM connector-to-RIMM connector), the clock signals must be matched within ±2mils to the trace length of every RSL signal. Exact length matching is preferred.

For the line section labeled ‘D’ (DRCG-to-2nd RIMM connector), the CHx_CTM/CTM# must be length matched within ±2 mils (exactly is recommended), **and for the section labeled ‘C’, ±2 mil trace length matching is required for the CHx_CFM/CFM# signals.**

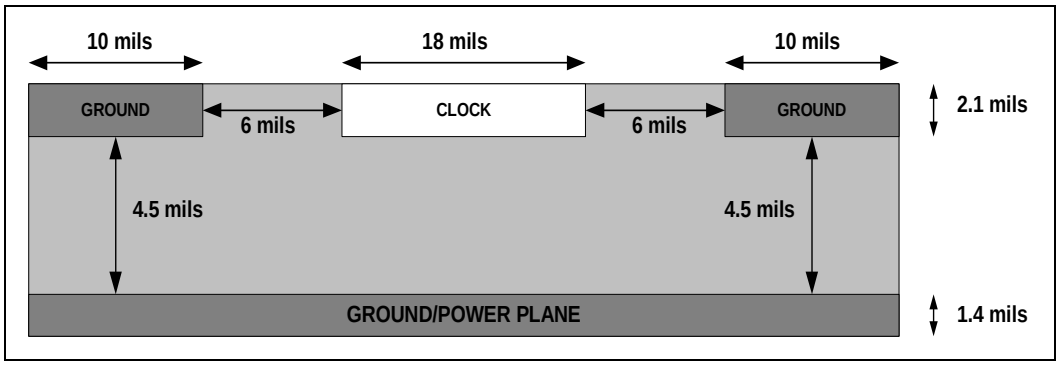
Note: The total trace length matching for the entire CHx_CTM/CTM# signal traces (Sections A+B+D) and for the CHx_CFM/CFM# signal traces (Sections A+B) is ±2 mils (exact length matching is recommended).

Figure 32. Differential Clock Routing Diagram



NOTE: "CLOCK" refers to the CTM and CFM signals; "CLOCK#" refers to the CTM# and CFM# signals.

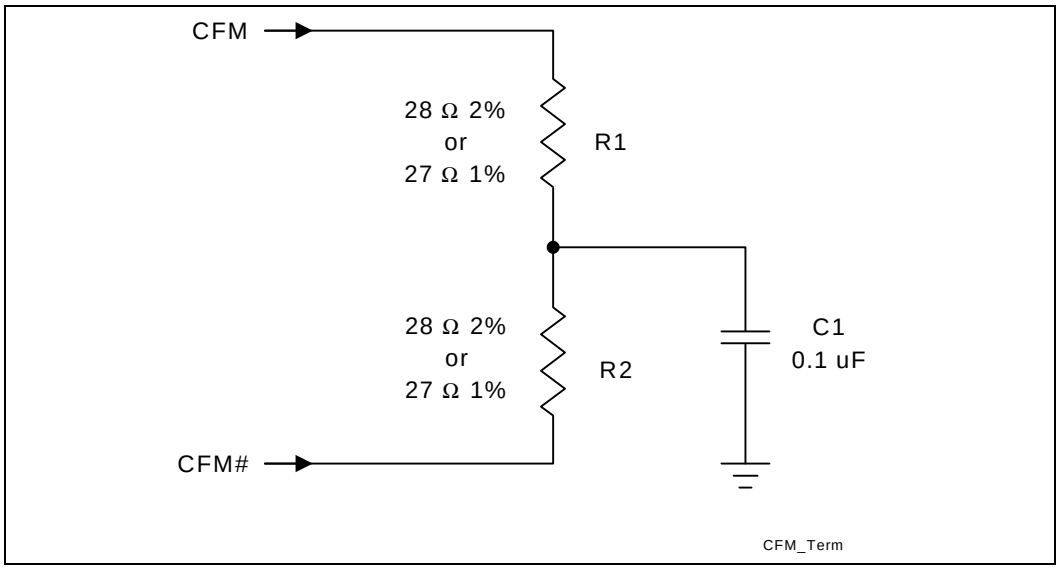
Figure 33. Non-Differential Clock Routing Diagram



NOTE: "CLOCK" refers to the CTM, CTM#, CFM and CFM# signals.

The CHx_CFM/CFM# differential pair signals require termination using either 27 Ω 1% or 28 Ω 2% resistors and a 0.1 µF capacitor as shown in Figure 34.

Figure 34. Termination for Direct RDRAM* Device CHx_CFM/CFM# Clocking Signals



3.7.3 DRCG* Device Impedance Matching Circuit

The external DRCG device impedance matching circuit is shown in Figure 35.

Figure 35. DRCG* Device Impedance Matching Network

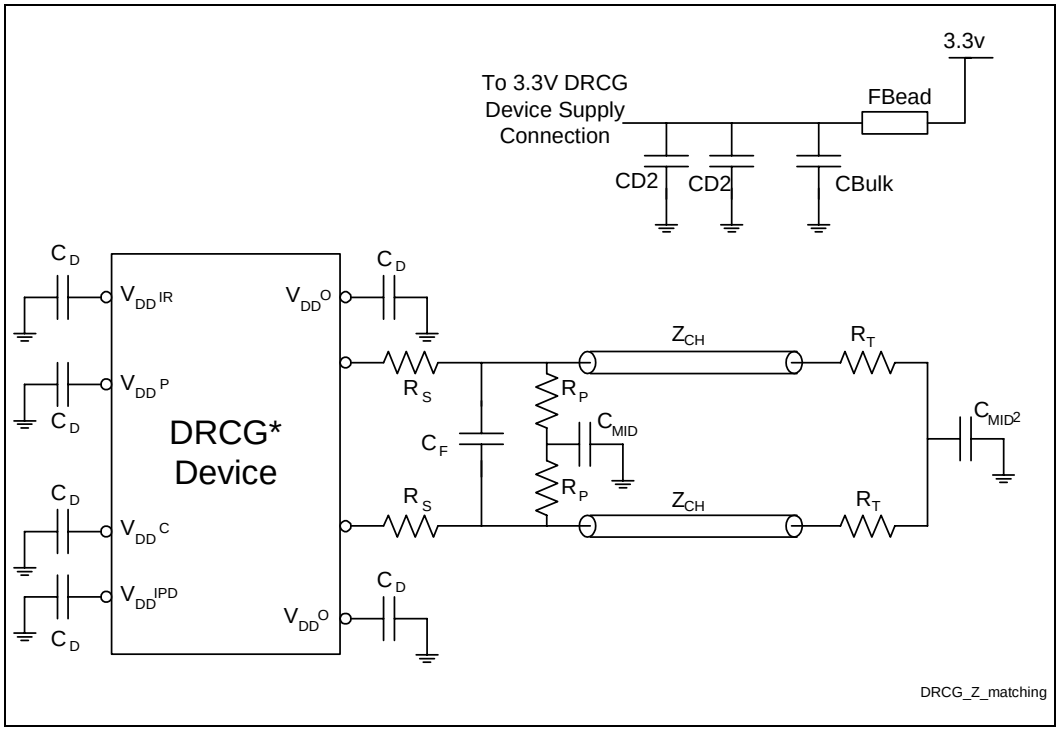


Table 12. DRCG* Device Impedance Matching Network Values

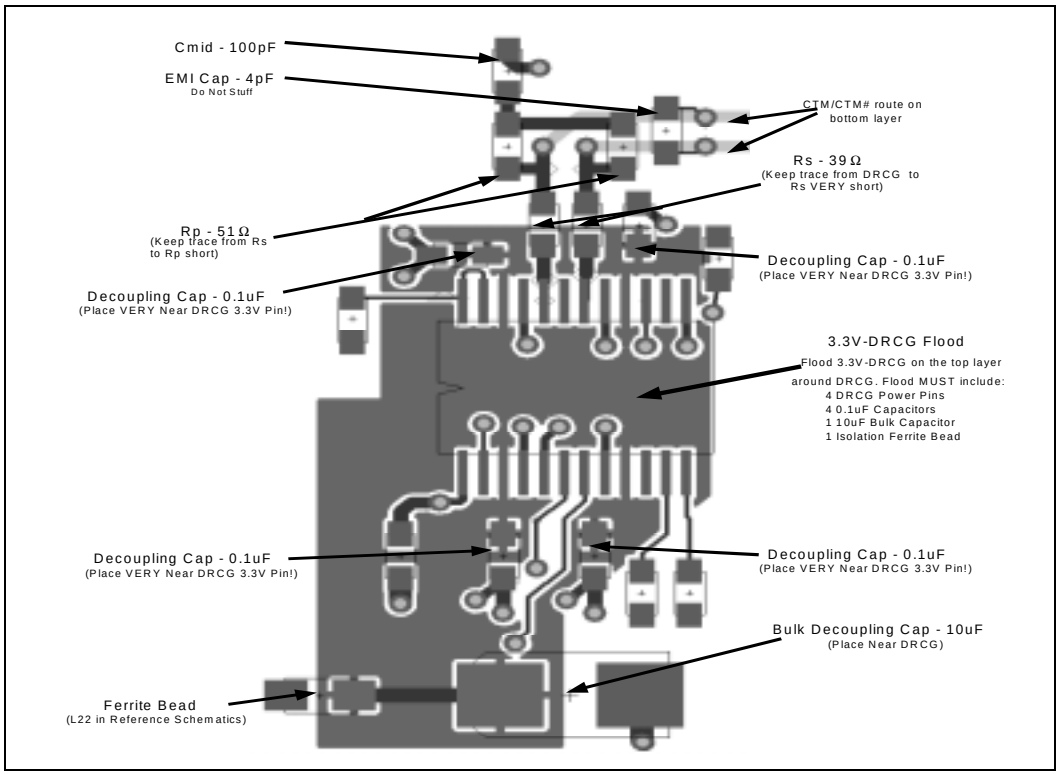
Component	Nominal Value	Notes
C_D	0.1 µF	Decoupling caps to GND
R_S	39 Ω	Series termination resistor
R_P	51 Ω	Parallel termination resistor
C_{MID1}, C_{MID2}	0.1 µF	Virtual GND capacitors
R_T	27 Ω	End of channel termination
C_F	4–15 pF	Do Not Stuff, leave pads for future use
FBead	50 Ω @ 100 MHz	Ferrite bead
CD2	0.1 µF	Additional 3.3V decoupling caps
CBulk	10 µF	Bulk cap on device side of ferrite bead

NOTES: For Figure 35 and Table 11

1. The removal of the original EMI capacitors between the junctions of RS, RP, and ground. These capacitors had minimal impact on EMI and increased DRCG device output jitter by approximately 2X.
2. The intent of component CF is to decouple CLK and CLKB outputs to each other; however, data shows this actually increases device jitter. CF should not be stuffed at this time.
3. The ferrite bead and 10 µF bulk capacitor combination improves jitter and helps to keep the clock noise away from the rest of the system. The additional 3.3V capacitors (CD2) have a minor positive impact, but the ideal values have not been extensively optimized.
4. 0.1 µF capacitors are better than 0.01 µF or 0.001 µF capacitors for DRCG device decoupling. Most decoupling experiments that replaced 0.1 µF capacitors with higher frequency capacitors ended up with the same or worse jitter. Replacing the existing 0.1 µF capacitors with higher frequency capacitors is not advised.
5. C_{mid} at 0.1 µF has improved jitter versus C_{mid} at 100 pF. However, this will increase the latency coming out of a stop clock or tri-state mode.
6. R_S, R_P, R_T were modified to improve channel signal integrity through increasing CTM/CTM# swing.
7. The circuit shown is required to match the impedance of the DRCG device to the 28 Ω channel impedance. More detailed information can be found in the Direct RDRAM Device Clock Generator Specification.
8. The previously recommended 15 pF capacitors on CTM/CTM# should be removed. The 4 pF capacitor shown in the figure should not be stuffed.

3.7.4 DRCG* Device Layout

Figure 36. DRCG* Device Layout Example



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4 MEC Power Delivery

4.1 Terminology

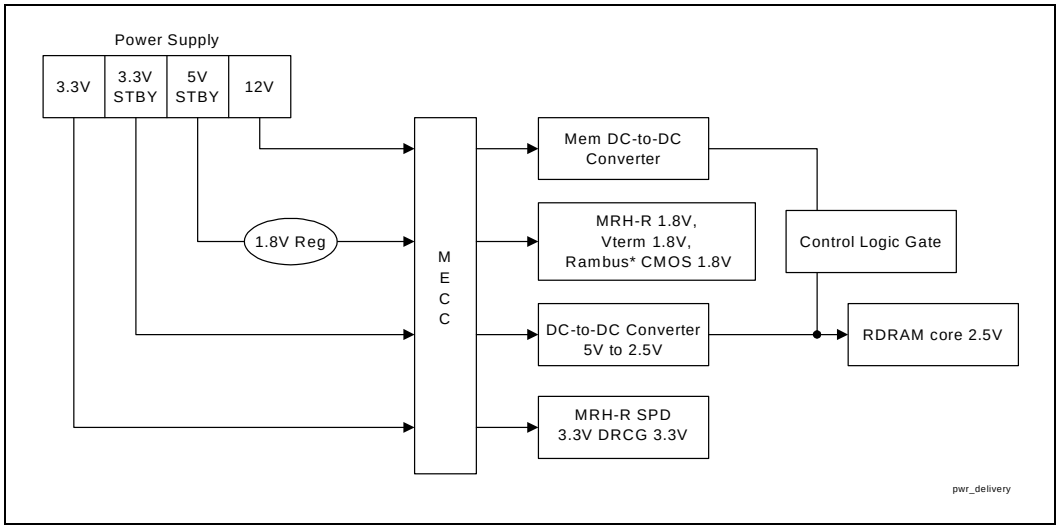
Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.
Full-power operation	During *full-power* operation, all components on the Memory Expansion Card remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (processor stop grant state) state.
Suspend operation	During *suspend* operation, power is removed from some components on the Memory Expansion Card. MEC designs may support the following two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Core power rail	A power rail that is only on during full-power operation.
Standby power rail	A power rail that is on during suspend operation (these rails are also on *during full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). These standby rails are created with a DC-to-DC converter on the MEC.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator or a voltage divider network. For example, 1.8 V CMOS can be derived (on the MEC) from either the 2.5 V generated using a DC-to-DC converter.

4.2 Power Delivery Block Diagrams

Figure 37 shows the power delivery architecture for Direct RDRAM device-based Memory Expansion Cards. This power delivery architecture supports the Suspend-to-RAM (STR). During STR, only the necessary devices are powered and this includes main memory. To ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device's power requirements, both in suspend and in full-power. The power requirements must be compared against the power budget supplied by the power supply.

There are many power distribution methods that achieve similar results. It is critical, when deviating from the examples in this design guide in any way, to consider the effect of the change.

Figure 37. Intel® MRH-R/Direct RDRAM* Device MEC Power Delivery



The requirements for each power plane are documented in this section. In addition, an on-board DC-to-DC converter is recommended if the designer needs to minimize the number of power pins required on the MECC. Systems implementing an ATX type power supply should follow these guidelines, but make the appropriate power rail changes where needed.

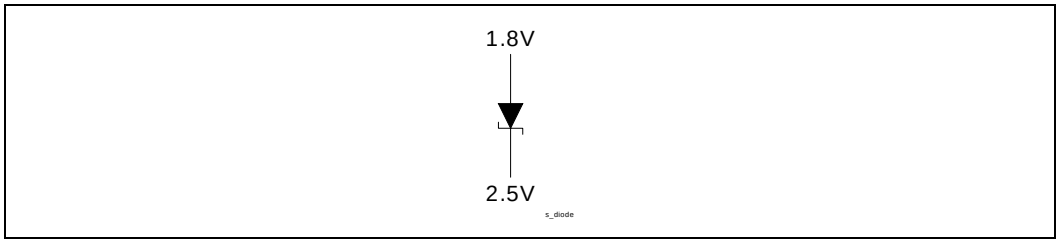
- **12V:** In a system with a DC-to DC converter, the 12V plane powers the DC-to-DC converter on the MEC. The DC-to-DC converter provides 2.5V as an output for the Direct RDRAM device MEC. This implementation minimizes the number of power pins required on the MECC.
- **2.5V:** The 2.5V power plane is used to power the Direct RDRAM device core and the Vcmos rail on the Direct RDRAM devices. The Direct RDRAM device core requires 2.0A *maximum average DC current* at 2.5V. On the Memory Expansion Card power delivery examples shown, the 2.5V plane is powered by both the 12V to 2.5V DC-to-DC and the 5V standby to 2.5V combined. During normal operation, these two outputs need to be combined. However, during STR, the outputs need to be separate. On the CRB, these two planes are combined using a MOSFET and the RIMM connectors are tied directly to the standby side. In STR, the MOSFET turns off, isolating the 2.5V plane generated by the regulator voltage.

  The Vcmos rail requires a maximum of 3 mA at 1.8V. This rail MUST be powered during Suspend-to-RAM; therefore, the Vcmos rail should NOT be connected to the Vterm rail. Because the current requirements of Vcmos are so low, a resistor divider can be used to generate Vcmos from 2.5V, which remains powered during STR. The resistor divider should be 36 Ω (top) / 100 Ω (bottom). Additionally, it should be bypassed with a 0.1 µF chip capacitor.
- **1.8V:** The 1.8V plane powers the MRH-R core and the Direct RDRAM device termination resistors, Vterm (1.85V). This 1.8V power plane should be generated on the motherboard via a switching regulator. The MRH-R component requires 1.8V for operation. The MRH-R is not required to be powered during the *Suspend-to-RAM* state. Thus, this power rail can be powered off when the system enters an STR state. The termination resistors do NOT need to be powered during the STR state.
- **3.3V:** The 3.3V plane powers the DRCG device cores and the SPD bus on the MEC. This power rail can be powered off when entering a STR state.

4.3 Vterm/Vdd Power Sequencing Requirement

Power MUST NOT be applied to the Direct RDRAM device termination resistors (Vterm) prior to applying power to the Direct RDRAM device core. This can be guaranteed by placing a Schottky diode between 1.8V and 2.5V as shown in Figure 38.

Figure 38. 1.8V and 2.5V Power Sequencing (Schottky Diode)



4.4 RIMM Connector/ 2 Intel® MRH-R Memory Expansion Card Thermal Considerations

Table 13. Direct RDRAM* Device Power States [1, 2, 3]

Power State	Power (W)
ActiveRead	1.524
ActiveWrite	1.683
Active	0.3922
Standby	0.2677
NAP	0.0111

NOTES:
1. Assumes Latest Direct RDRAM device 2.5V Current Specification values
2. Assumes 144-Mbit components (x18 devices)
3. Assumes Vddmax = 2.65V

Table 14. Direct RDRAM* Device Pool Definition [1]

Power State	# of Devices
ActiveRead	2
Active	14
Standby	112
NAP	0

NOTES:
1. Assumes NO NAP for best performance.

Refer to the *Intel® 860 Chipset: 82860 Memory Controller Hub (MCH)* Datasheet for pooling information.

Table 15. MEC Direct RDRAM* Device Power (Reads)

Power State	Power (W)
ActiveRead	3.048
Active	5.5
Stby	30.0
NAP	0.0
Total	**38.5**

Table 16. MEC Direct RDRAM* Device Power (Writes)

Power State	Power (W)
ActiveWrite	3.366
Active	5.5
Stby	30.0
NAP	0.0
Total	**38.8**

Table 17. MEC Discrete Device Power

Device	Power (W)	Quantity	Total (W)
DRCG (3.3V)	0.33	4	1.32
DRCG (1.8V, per pin)	0.0036	8	0.0288
MRH-R (1.8V)	2.2	2	4.4
Vterm (1.85V, per pin)	0.054	88	4.752

Table 18. MEC Power Rails

Rail	Current (A)	Power (W)
1.8 V	5.10	9.180
3.3 V	0.40	1.320
2.5 V	15.53	38.80
12 V	3.80	45.70

NOTES:
1. 2.5 V is derived from a DC-DC converter with 12 V input.
2. Efficiency of the DC-to-DC converter is rated at ~85%.

4.4.1 MRH-R SVSTRAP Pin

If this pin is left unconnected, the MRH-R will stop responding to clocks; this prevents initialization from completing. To prevent failures, this pin (MRH-R reserved pin, ball D5) must be connected to VSS.

5 Schematic Checklist

5.1 Memory Expansion Connector Checklist

Checklist Items	Recommendations	Reason/Impact
CHx_SIO	• CHx_SIO should connect to SIO/SIN of MRH-R. Then should be daisy chained between RIMM connectors: CHx_ SIO/SOUT pin on MRH-R connects to 1st RIMM connector SIN (B36) SOUT (A36) on 1st RIMM connector connects to 2nd RIMM connector SIN (B36)	• Refer to Section 3.6.4 for more information.
CHx_SCK, CHx_CMD	• Connect to appropriate pins on the MRH-Rs. The “x” denotes Channel A and Channel B	• Proper termination and impedance matched must be met due to synchronous requirements between the RSL signals and the high-speed CMOS signals • As a result of the buffer strengths in the MCH, the following termination is required: 91 Ω pull-up to 1.8 V with 39 Ω pull-down to ground
CHx_EXP1, CHx_EXP0, CHx_DQA[8:0], CHx_DQB[8:0], Chx_RQ[7:5]/ ROW[2:0], Chx_RQ[7:5]/ ROW[2:0]	• Connect to appropriate pins on MRH-Rs. The “x” denotes Channel A and Channel B • Terminate with 36.5 Ω resistor for each signal with 0.01 µF capacitor to ground between both signals	• For 28 Ω impedance to be maintained, perfect matching of transmission line impedance is essential for the Direct RDRAM device interface to work properly
CHx_CTM, CHx_CTM#, CHx_CFM, CHx_CFM#	• Connect to appropriate pins on MRH-Rs. The “x” denotes Channel A and Channel B. • Terminate signals with 28 Ω 1% resistor to ground with 0.1 µF capacitor to ground between two signals	• For 28 Ω impedance to be maintained, perfect matching of transmission line impedance is essential for the Direct RDRAM device interface to work properly
SDA, SCLK	• MRH-R SMBus pull-ups must turn off during STR to eliminate leakage. • The ICH SMBus controller should be used in place of the 82803AA MRH-R SMBus controller due to an erratum with the MRH-R. Careful attention should be given to selecting SMBus addresses to avoid address contention when making this change.	• Refer to the latest MRH-R Specification Update, Errata Section

Checklist Items	Recommendations	Reason/Impact
SMBWE	• It is recommended that this signal be tied to a GPO pin from either the ICH2 or the SIO. • If an OEM does not need to write to the SPD devices, it is recommended that this signal be tied to 3.3 V via a weak pull-up resistor (4.7 kΩ).	• SWP = 1, write protected. SWP = 0, not write protected. These signals must be driven, do not leave floating. • Refer to the Rambus datasheets at http://www.rambus.com
CHx_RAMREF_TM	• Connect to appropriate pins on the MRH-Rs. The “x” denotes Channel A and Channel B. • RAMREF Generation Circuit: At resistor divider – The RAMREF generation circuitry should be placed near the MRH-R. A 162 Ω ±2% pull-up resistor and 562 Ω ±2% pull-down resistor is required for proper reference voltage. With a 0.1 µF decoupling capacitor to ground.	• To avoid current overloading on each channel, separate reference divider circuit is recommended
CHx_RAMREF_FM	• Connect appropriate EXVREF pins on MRH-Rs. “x” denotes Channel A and Channel B. • MCH: Locally – A value of two 0.1 µF capacitors are required for local decoupling and a 100 Ω series resistor is required near the MRH-R, but before the voltage divider circuit.	• Refer to Section 3.6.2 for more information
M_SEL[1:0]		
RCI_AUX	• Connect to S0 and S1 of DRCG devices	• Some 64-/72-Mbit Direct RDRAM devices interpret non-broadcast, device-directed commands as broadcast commands
PWROK	• Connect to shunting logic (transistors) used on the MRH-R SCK/CMD CMOS signals.	• Required **only** when supporting the S3 state with MRH-R components.
RESET#	• Connect to MRH-R reset signals.	
CHx_DRCGOUT_L CHx_DRCGOUT	• Connect between DRCG CLK outputs on the motherboard and MRH-R components to create clocks for expansion channels.	• CTM/CTM# clocks between the MRH-Rs and MCH are generated from these nets at a point closest to the MRH-R component. These new clocks are routed as CTM/CTM# for transactions traveling from MRH-R to MCH.
SLP_L	• Control signal for S3 logic	• Refer to schematics.
BF_CUT	• Control signal for S3 logic	• Refer to schematics.
2_5VSENSE	• Used to sense 2.5 V down on the baseboard with Heceta* component to insure proper voltage levels on the	
5V_STB	• Used to provide standby power during S3. Connect to the S3 logic	• Refer to schematics.
12V	• Power pin for on board DC-DC converter for 2.5 V generation on the MEC	• Refer to the Section 4.2

Checklist Items	Recommendations	Reason/Impact
1_8V	• Power pin for MRH-R and all Vterm on the MEC	• Refer to the Section 4.2
3_3V	• Power pins for the DRCG device, CKBFs and SMBus interface	• Refer to Section 4.2
GND	• Ground pins placed between all RSL Signals	• Ground reference for Direct RDRAM device core and interface logic.

5.2 RIMM* Connectors Checklist

- S3 (Suspend To RAM):
  - Direct RDRAM device Support → 2.5 V (ON), 1.8 V (ON), 3.3 V (N/A)
- S5 – 2.5 V (OFF), 1.8 V (OFF), 3.3 V (OFF)

Checklist Items	Recommendations	Reason/Impact
LCTM, LCTM# RCTM, RCTM# LCFM, LCFM# RCFM, RCFM# LROW[2:0] RROW[2:0] LCOL[4:0] RCOL[4:0] RDQA[8:0] LDQA[8:0] RDQB[8:0] LDQB[8:0] CMD SCK	• Connect to appropriate pins on MRH-Rs to appropriate pins on RIMM connectors	
RSL Signal Termination	• All RSL signals must be terminated to 1.8 V (Vterm) using 27 Ω 1% or 28 Ω 2% tolerance resistors at the end of the channel opposite the MCH.	• Rpacks are OK.
RC Termination	• Due to the buffer strengths in the MCH, the high-speed CMOS signals require DC termination. • Terminate with 91 Ω ±2% pull-up and a 39 Ω ±2% pull-down resistor to ensure proper resuming from S3.	• The MCH tri-states SCK during STR entry causing a glitch on SCK. • Refer to Section 3.7.2

Checklist Items	Recommendations	Reason/Impact
SVDD (A56 and B56)	• Should be tied to 3.3V for EEPROM (SPD) on RIMM connector. • If the SMBus is tied to 3.3VSB, then either: — provide proper isolation on SCL /SDA and pull SVDD to 3.3V OR — tie SVDD to 3.3VSB.	• Ensure proper isolation if some SMBUS devices are powered by 3.3VSB. • Refer to the Rambus datasheets at http://www.rambus.com
SA Pins	• Should be connected to VCC3_3 or GND to set the SMBus address for that RIMM connector's EEPROM. • If the SMBus is tied to 3.3VSB, then either: — provide proper isolation on SCL /SDA and pull the HIGH SA pins to 3.3V OR — tie the HIGH SA pins to 3.3VSB.	• This sets the SMBus address. Each device on the SMBus must have an address to distinguish it from another device of the same type. That is, each RIMM connector's EEPROM must be strapped to a different address or they will all respond on an access. • Refer to the Rambus datasheets at http://www.rambus.com
SIN & SOUT	• Should be daisy-chained between RIMM connectors: — SIO pin connects to 1st RIMM connector SIN (B36) — SOUT (A36) on 1st RIMM connector connects to 2nd RIMM connector SIN (B36) — A 2.2 kΩ–10 kΩ terminating resistor, tied to GND, is required on the last RIMM connector's SOUT pin.	• Refer to the Rambus datasheets at http://www.rambus.com
SWE (A57)	• If an OEM needs to write to the SPD devices, it is recommended that this signal be tied to a GPO pin from either the ICH2 or the SIO. • If an OEM does not need to write to the SPD devices, it is recommended that this signal be tied to 3.3 V via a weak pull-up resistor (4.7 kΩ).	• If SWE = 1, write protected. • If SWE = 0, not write protected. • These signals must be driven; do not leave floating. • Refer to the Rambus datasheets at http://www.rambus.com
RESET	• For the 168-pin RIMM connector connector, this is a reserved pin.	• The connector pad is reserved for future use for the 168-pin RIMM connector connector. • Refer to the Rambus datasheets at http://www.rambus.com
V_{DD}	• This is connected to 2.5 V (or 2.5VSB) • It is REQUIRED that the voltage regulator to the Direct RDRAM devices (2.5 V Direct RDRAM device Core) is turned OFF in S5. This can be accomplished by connecting the SLP_S5# signal to the 2.5 V Direct RDRAM device Core voltage regulator.	• It supplies the core voltage for the Direct RDRAM device and interface logic. • Refer to the schematics and Section 4.3

Checklist Items	Recommendations	Reason/Impact
V_{CMOS}	• This is connected to 1.8 V for Direct RDRAM devices • Vcmos must be OFF in S5. • Vcmos can be generated with a voltage divider consisting of a 36 Ω pull-up resistor to VCC2_5 and 100 Ω resistor to GND.	• S5 is a suspend state and power is removed from some components on the motherboard. Therefore, Vcmos should be off while in suspend state. • Refer to Section 4.2
2.5 V (V_{DD}) decoupling	• Low frequency decoupling: • This needs to be done on the board with bulk capacitors. • Linear regulator design: 8x 100 µF • Switching regulator: 5x 47 µF or 6x 20 µF	• These are **examples**. The exact decoupling requirements are dependent on the voltage regulator design. Refer to the Direct RDRAM device specification for the power delivery requirements.
1.8 V (V_{TERM}) decoupling	• High frequency decoupling: — One 0.1 µF ceramic capacitor per 2 RSL signals. These should be placed near the termination resistor pack. • Low frequency decoupling: — 2 x 100 µF tantalum capacitors.	• RSL termination voltage decoupling is required on the motherboard. Both high and low frequency decoupling needs to be added on the motherboard. • These are **examples**. The exact decoupling requirements are dependent on the voltage regulator design. Refer to the Direct RDRAM device specification for the power delivery requirements.
1.4 V (RAMREF) decoupling	• This plane must be decoupled in the following manner: — Each RIMM Connector: Locally – A value of 0.1 µF is required for local decoupling. — RAMREF Generation Circuit: At resistor divider – The RAMREF generation circuitry should be placed near the MRH-R. A 162 Ω ±2% pull-up resistor and 562 Ω ±2% pull-down resistor is required for proper reference voltage. — MCH: Locally – A value of 0.1 µF is required for local decoupling and a 100 Ω series resistor is required near the MCH, but before the voltage divider circuit.	• Refer to section 2.2.2 for more information.

5.3 Intel® MRH-R Checklist

Checklist Items	Recommendations	Reason/Impact
Testing	• Pull-up with 10 kΩ resistor to 1.8 V	
RESET	• Connect to PCI RESET from MECC to MRH-R and DRCG RESET	
SVSTRAP(Reserve pin D5)	• Connect to ground	• When this pin floats high enough, the MRH-R will stop responding to clocks; thus, preventing initialization to complete
SMBUS Pins	• Pull up 1 kΩ resistor to 2.5 V	

5.4 Direct Rambus* Clock Generator (DRCG* Device) Checklist

Checklist Items	Recommendations	Reason/Impact
VddiR	• Connect to 3.3 V	• Provides the voltage reference for the Refclk clock output from CK_SKS clock generator • Refer to the reference schematics in Section 3.7.1
Refclk	• Connect Refclk pin of DRCG1 and DRCG2 to appropriate Refclk pins on the MRH-R	• Refer to the reference schematics.
VddP, VddC, VddO,	• These are all 3.3 V voltage pins. Tie directly to VCC3_3 supply. • Place a 0.1 µF capacitor between each pin and the VSS plane for decoupling purposes.	• Refer to the reference schematics.
GndP, GndI, GndC, GndO	• Connect to GND.	• These are all ground pins. • Refer to the reference schematics.
PclkM	• Connect to appropriate PclkM pins on MRH-R.	• This is a host clock feedback input. • Refer to the reference schematics.
SynclkN	• Connect to appropriate Syncline on MRH-R.	• This is a RAMBUS* clock feedback input. • Refer to the reference schematics.
VddIPD	• Connect to 1.8 V power plane.	• This is a voltage reference for PclkM and SynclkN signals. • Refer to the reference schematics.
STOPB#	• Connect to appropriate STOPB# pins on MRH-R.	• Refer to the reference schematics.

Checklist Items	Recommendations	Reason/Impact
PWRDN#	• Terminate to 3.3 V through a 4.7 KΩ resistor.	• Refer to the reference schematics.
S1, S0	• Connect 1 KΩ ±5% series resistors to S0 and S1 and connect signals together. Connect joined signals through a 4.7 KΩ ±5% pull-down resistor to GND and connect a series resistor to a GPIO	• A low voltage (logic “0”) on S1 and S0 places the DRCG device in normal operation mode. The GPIO connection allows software adjustable mode control over CLK and CLKB
Mult[1:0]	• Connect to MULT0 to ground via a 10 KΩ pull-down. • Connect MULT1 to V3_3 via a 10 KΩ pull-up	• These pins determine the internal PLL divider ratio in the DRCG device. The MRH-R only supports 400 MHz (PC800) RAMBUS* operation only. • Refer to the reference schematics.
ClkB/Clk	• Connect a 39 Ω ±5% series resistor near the pins. Connect 51 Ω ±5% parallel resistors after the series resistors through a 0.1 µF capacitor to ground. Connect to RIMM connector. • These signals should be terminated with 28 Ω ±2% or 27Ω ±1% resistors to ground through a 0.1 µF capacitor.	• This is the main clock (CTM/CTM#) for the Rambus Channel. • Refer to the reference schematics.
Global decoupling	• It is recommended that a ferrite filter with 2 capacitors (10 µF and 0.1 µF) be placed near the part for both the 3.3 V planes. Capacitors should be placed on the device side of the Ferrite Bead. Ferrite bead should be 50 Ω at 100 MHz. • Discrete capacitors are recommended for all the aforementioned decoupling. • Cpacks are not recommended.	• This recommendation is to reduce jitter and voltage supply noise for the part. • Cpacks will increase the parasitic inductance of the capacitors, and may require more capacitors than specified above. • Refer to the reference schematics.

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6 Design Checklist

Use the following checklist as a final check to ensure the MEC incorporates solid design practices. This list is only a reference. For correct operation, all of the design guidelines within this document must be followed.

Table 19. Signal List

RSL Signals	High-Speed CMOS Signals	Serial CMOS Signal	Clocks
DQA[8:0]	CMD	SIO	CTM
DQB[8:0]	SCK		CTM#
RQ[7:0]			CFM
			CFM#

- Ground Isolation Well Grounded
  - Via to ground every ½ inch around edge of isolation island
  - Via to ground very ½ inch between RIMM connectors
  - Via to ground every ½ inch between RSL signals
  - Via between every signal within 100 mils of the MRH edge and the connector edge
  - No unconnected ground floods
  - All ground isolation at lest 10 mils wide
  - Ground isolation fills between serpentines
  - Ground isolation not broken by CTABs
  - Ground isolation connects to the ground pins in the middle of the RIMM connectors
  - Ground isolation vias connect on all layers and **should not** have thermal relieves
  - Ground pins in RIMM connector connect on all layers

- Vterm Layout Yields Low Noise (Decoupling Vterm is CRITICAL!)
  - Solid Vterm island is on top routing layer – do not split this plane
  - Ground island (for ground side of Vterm caps) is on top routing layer
  - Termination Resistors connect **directly** to the Vterm island on the routing (without vias)
  - Decoupling capacitors connect to top layer Vterm island and top routing layer ground island directly (see layout example)
  - Use **at least** 2 vias per decoupling capacitor in the top layer ground island
  - Use 2 x 100 µF Tantalum capacitors to decouple Vterm (Aluminum/Electrolytic capacitors are too slow!)
  - High-frequency decoupling capacitors **must** be spread-out across the termination island so that all termination resistors are near high-frequency capacitors
  - 100 µF Tantalum capacitors should be at each end of the Vterm island
  - 100 µF Tantalum capacitors must be connected to Vterm island directly
  - 100 µF Tantalum capacitors must have **at least** 2 vias/cap to ground
  - Vterm island should be 50 – 75 mils wide
  - Vterm island should not be broken
  - If any RSL signals are routed out of the 2nd RIMM connector (towards termination) on a plane referenced to power (even for a short distance), ensure Ground Reference Plane (on the power plane) is continuous under the termination resistors/capacitors
  - Ensure current path for power delivery to the MRH-R does not go through the Vterm island
  - Refer to Section 3.6.1.3 in this design guide.
- CTM/CTM# Routed Properly
  - CTM/CTM# are routed differentially from DRCG device to 2nd RIMM connector
  - CTM/CTM# are ground isolated from DRCG device to 2nd RIMM connector
  - CTM/CTM# are ground referenced from DRCG device to 2nd RIMM connector
  - Vias are placed in ground isolation and ground reference every ½ inch
  - When CTM/CTM# serpentine together, they **must** maintain **exactly** 6 mils spacing
- Clean DRCG Device Power Supply
  - 3.3 V DRCG device power flood on the top layer. This should connect to each
  - High frequency (0.1µF) capacitors are near the DRCG device power pins. One capacitor next to each power pin.
  - 10µF bulk tantalum capacitor near DRCG device connected directly to the 3.3 V DRCG device power flood on the top layer
  - Ferrite bead isolating DRCG device power flood from 3.3 V main power also connecting directly to the 3.3 V DRCG device power flood on the top layer
  - Use 2 vias on the ground side of each

- Good DRCG Device Output Network Layout
  - Series resistors (39 Ω) should be very near CTM/CTM# pins
  - Parallel resistors (51 Ω) should be very near series resistors
  - CTM/CTM# should be 18mils wide from the CTM/CTM# pins to the resistors
  - CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network
  - When not 14 on 6, the clocks should be 18 mils wide
  - Ensure CTM/CTM# are ground referenced and the ground reference is connected to the ground plane every ½ inch to 1 inch
  - Ensure CTM/CTM are ground isolated and the ground isolation is connected to the ground plane every ½ inch to 1 inch
  - Ensure 15 pF EMI capacitors to ground are removed (the pads are not necessary and removing the pads provides more space for better placement of other components)
  - Ensure the 4 pF EMI capacitor described in Section 3.7.3 of this design guide is implemented (but do not assemble the capacitor)
- Good RSL Transmission Lines
  - RSL traces are 18 mils wide
  - RSL traces do NOT neckdown when routing into the RIMM connector
  - If tight serpentining is necessary, 10 mil ground isolation **must** be between serpentine segments (i.e., an RSL signal **cannot** serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines).
  - RSL traces do not cross power plane splits. RSL signals must also not be routed on next to a power plane splits
  - Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times
  - ALL RSL, CMD/SCK and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin
  - All RSL signals are routed adjacent to a ground reference plane. This includes all signals from the 2nd RIMM connector to the termination. If signals are routed referenced to ground from the 2nd RIMM connector to the termination, the ground reference plane **must** extend under these signals AND include the ground side of the Vterm decoupling capacitors.
  - CTABs must not cross (or be on top of) power plane splits. They must be **entirely** referenced to ground.
  - At least 10 mils ground flood isolation required around **all** RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MRH-R (and the 1st RIMM connector) as possible. If possible connect the flood to the ground balls/pins on the MRH-R/connector.
- Clean Vref Routing
  - Ensure 1 x 0.1 µF capacitor on Vref at each connector
  - Use 10 mil wide trace (6 mils minimum)
  - Do not route Vref near high-speed signals

- RSL Routing
  - All signals must be length matched within ±10 mils of the Nominal RSL Length as described in the Section 3.6.1.2.1. Ensure that signals with a dummy via are compensated correctly.
  - ALL RSL signals must have 1 via near the MRH BGA pad. Signals routed on the bottom layer of the MB will have a “real via” while signals routed on the top layer will have a “dummy via”. Additionally, all signals with a dummy via must have an additional trace length of 25 mils.
  - Signals must “alternate” layers as shown in Section 3.6.1.2.4.
  - Clock signals must be routed as a differential pair. The traces must be 14 mils wide and 6 mils apart (with no ground isolation) when they are routed as a differential pair. For very short sections under the MRH-R and under the 1st RIMM connector, it will not be possible to route as a differential pair. In these sections, the clocks signals MUST neck up to 18 mils and be ground isolated with at least 10 mils ground isolation.
  - Clock signals must be length compensated (using the length factor described in Sections 3.6.1.2.2). Ensure that each clock pair is length matched within ±2 mils.
  - When clock signals serpentine, they must serpentine together (to maintain differential 14:6 routing).
  - 22 mils ground isolation required on each side of the differential pair.
- Other
  - MRH-R Reserved Pin ball D5 must be connected to VSS.

Appendix A: Schematics

The MRH-R MEC schematics shown assume the MRH-R component is completely powered off if support for Suspend to Ram (S3) is required.

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INTEL(R) 82860 MEMORY EXPANSION CARD SCHEMATICS [MRH-R]
REVISION 1.2

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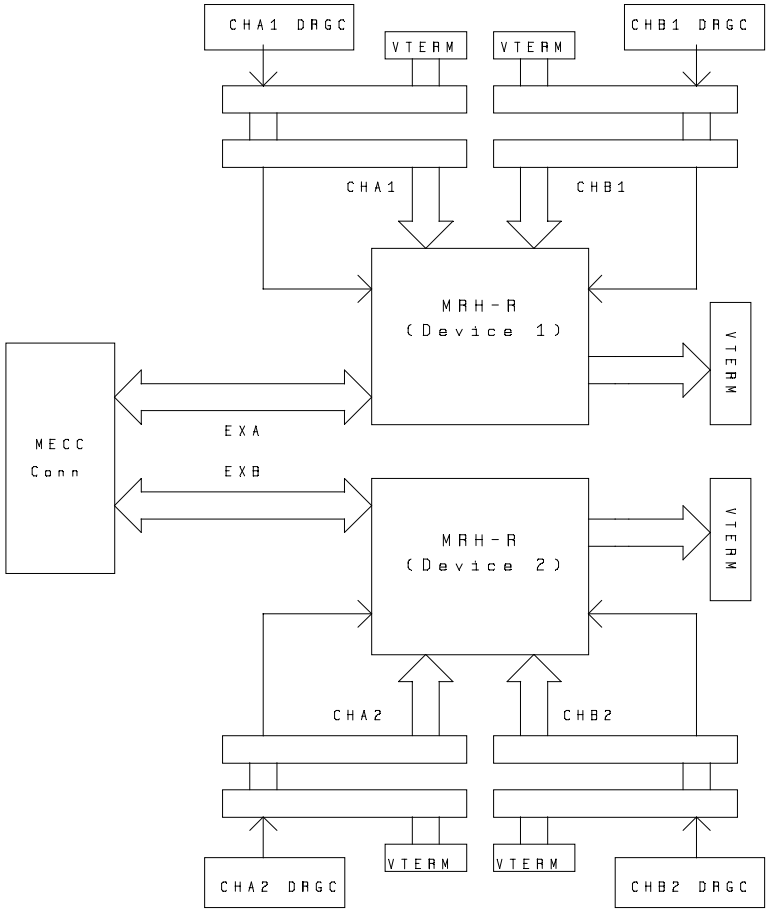
2 MRH-R Block Diagram (8 RIMM*)



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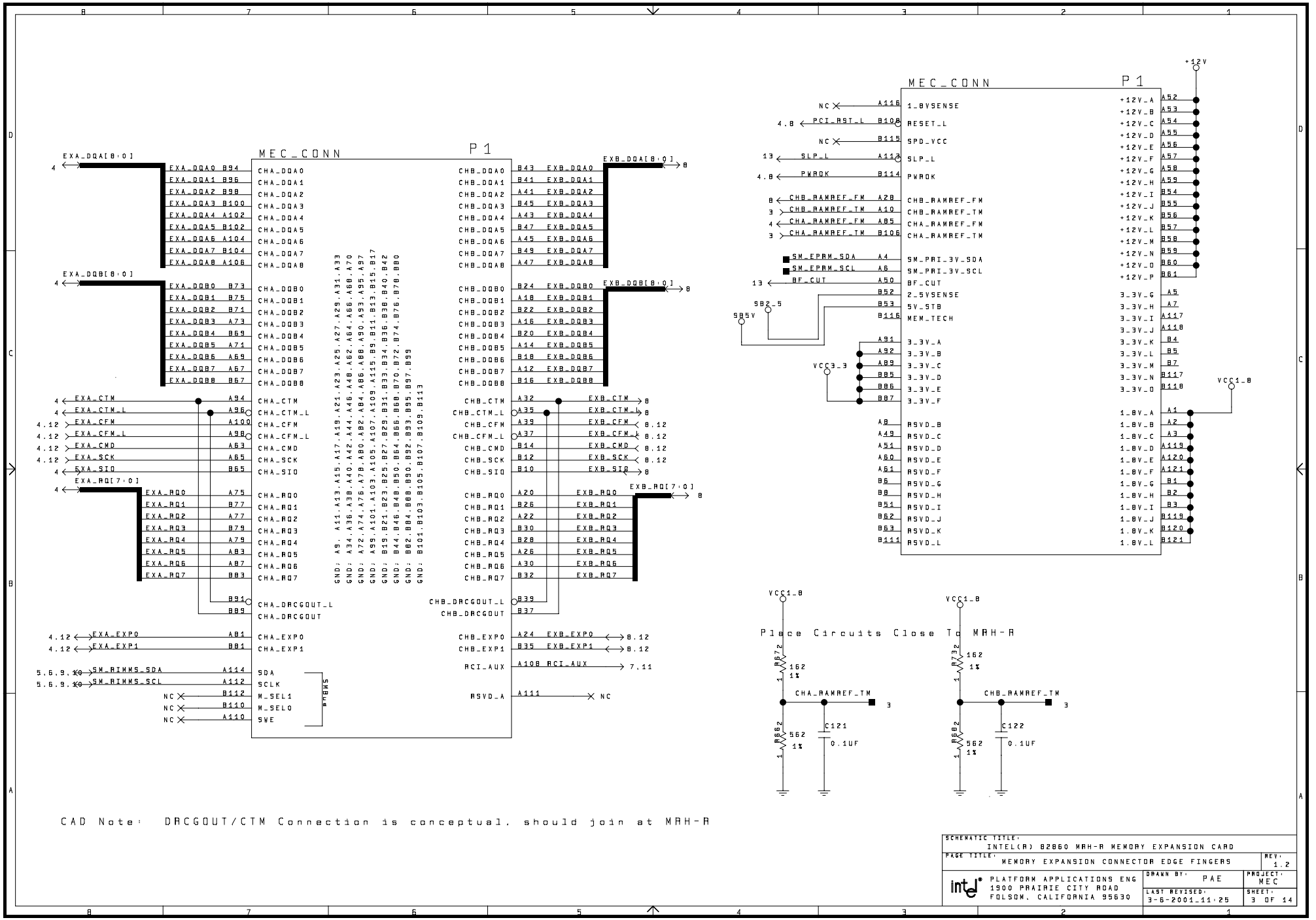

CAD Note: DRCGOUT/CTM Connection is conceptual, should join at MRH-R

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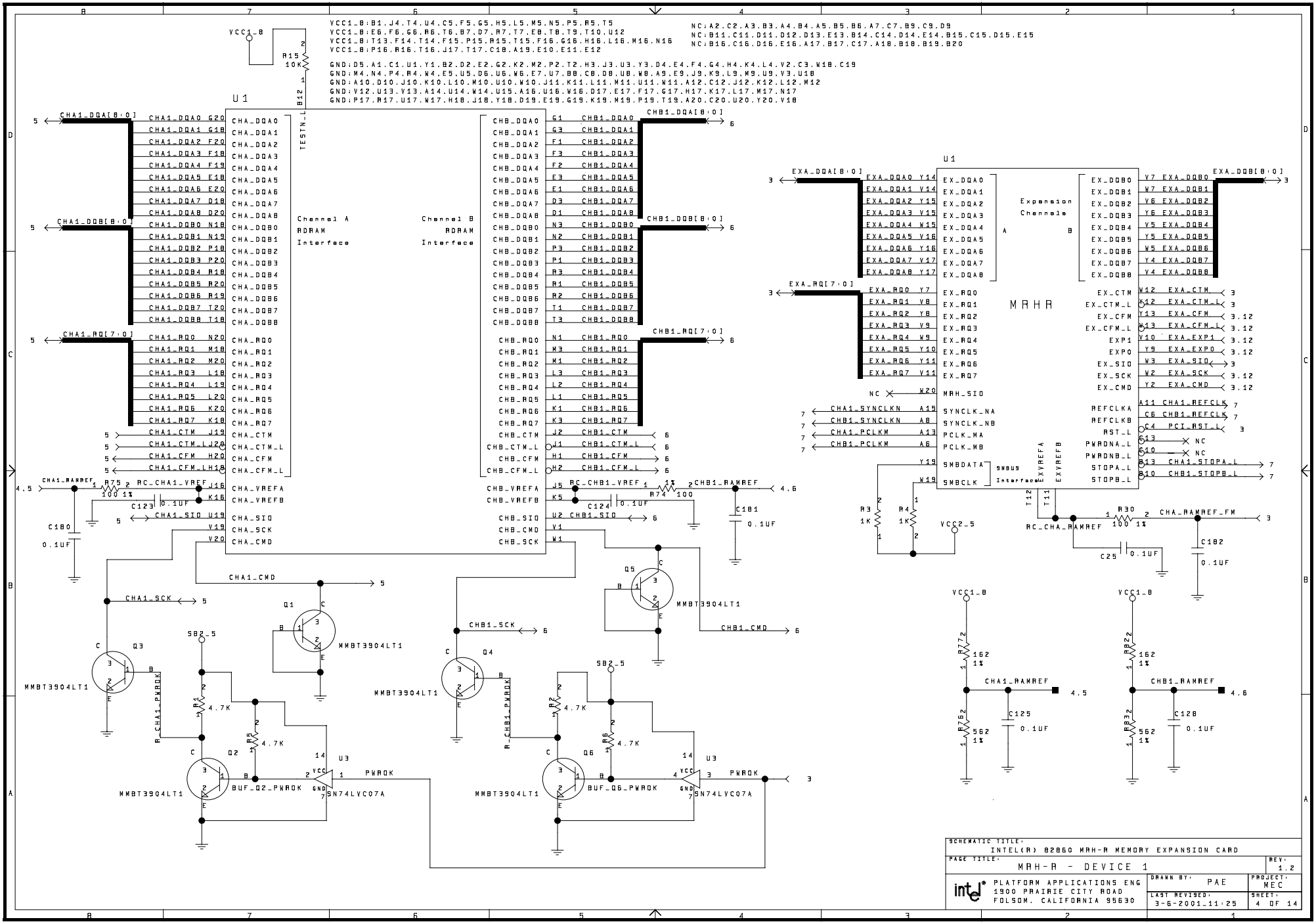
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VCC1_8:T13,F14,T14,F15,P15,R15,T15,F16,G16,H16,L16,M16,N16
VCC1_8:P16,R16,T16,J17,T17,C18,A19,E10,E11,E12
GND:D5,A1,C1,U1,Y1,B2,D2,E2,G2,K2,M2,P2,T2,H3,J3,U3,Y3,D4,E4,F4,G4,H4,K4,L4,V2,C3,W18,C19
GND:M4,N4,P4,R4,W4,E5,U5,D6,U6,W6,E7,U7,B8,C8,D8,U8,W8,A9,E9,J9,K9,L9,M9,U9,V3,U18
GND:A10,D10,J10,K10,L10,M10,U10,W10,J11,K11,L11,M11,U11,N11,A12,C12,J12,K12,L12,M12
GND:V12,U13,V13,A14,U14,W14,U15,A16,U16,W16,D17,E17,F17,G17,H17,K17,L17,M17,N17
GND:P17,R17,U17,W17,H18,J18,Y18,D19,E19,G19,K19,M19,P19,T19,A20,C20,U20,Y20,V18
NC:A2,C2,A3,B3,A4,B4,A5,B5,B6,A7,C7,B9,C9,D9
NC:B11,C11,D11,D12,D13,E13,B14,C14,D14,E14,B15,C15,D15,E15
NC:B16,C16,D16,E16,A17,B17,C17,A18,B18,B19,B20
U1
Channel A RDRAM Interface
Channel B RDRAM Interface
TESTN_L
MRH-R
Expansion Channels
SMBUS Interface
SN74LVC07A
MMBT3904LT1
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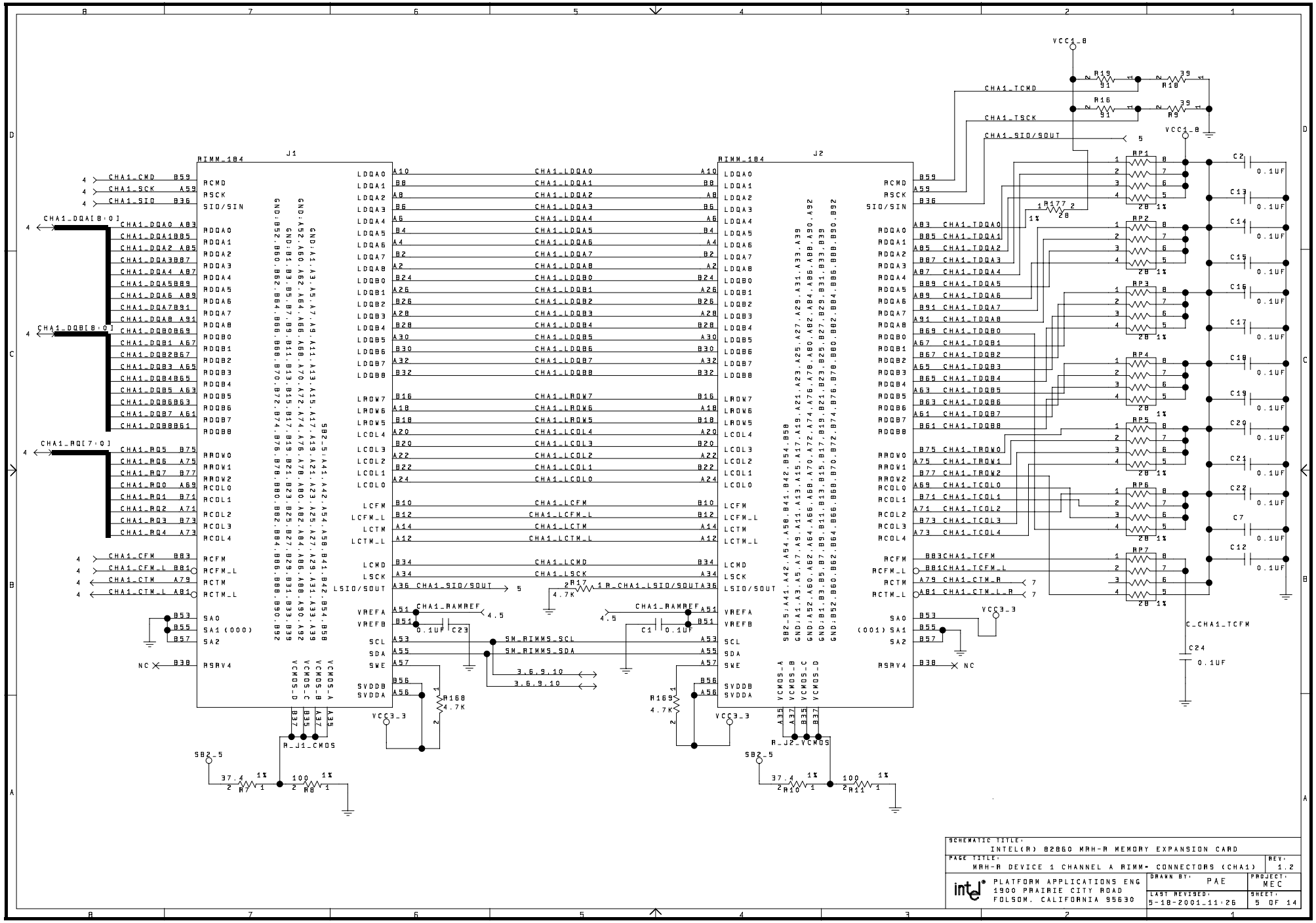
RIMM_184
J1
J2
CHA1_CMD
CHA1_SCK
CHA1_SIO
CHA1_DQA[8:0]
CHA1_DQB[8:0]
CHA1_RQ[7:0]
CHA1_CFM
CHA1_CFM_L
CHA1_CTM
CHA1_CTM_L
CHA1_TCMD
CHA1_TSCK
CHA1_SIO/SOUT
CHA1_TDQA0
CHA1_TDQA1
CHA1_TDQA2
CHA1_TDQA3
CHA1_TDQA4
CHA1_TDQA5
CHA1_TDQA6
CHA1_TDQA7
CHA1_TDQA8
CHA1_TDQB0
CHA1_TDQB1
CHA1_TDQB2
CHA1_TDQB3
CHA1_TDQB4
CHA1_TDQB5
CHA1_TDQB6
CHA1_TDQB7
CHA1_TDQB8
CHA1_TROW0
CHA1_TROW1
CHA1_TROW2
CHA1_TCOL0
CHA1_TCOL1
CHA1_TCOL2
CHA1_TCOL3
CHA1_TCOL4
CHA1_TCFM
CHA1_TCFM_L
CHA1_CTM_R
CHA1_CTM_L_R
R_CHA1_LSIO/SOUTA36
CHA1_RAMREF
SM_RIMMS_SCL
SM_RIMMS_SDA
R_J1_CMOS
R_J2_VCMOS
VCC1_8
VCC3_3
SB2_5
C_CHA1_TCFM
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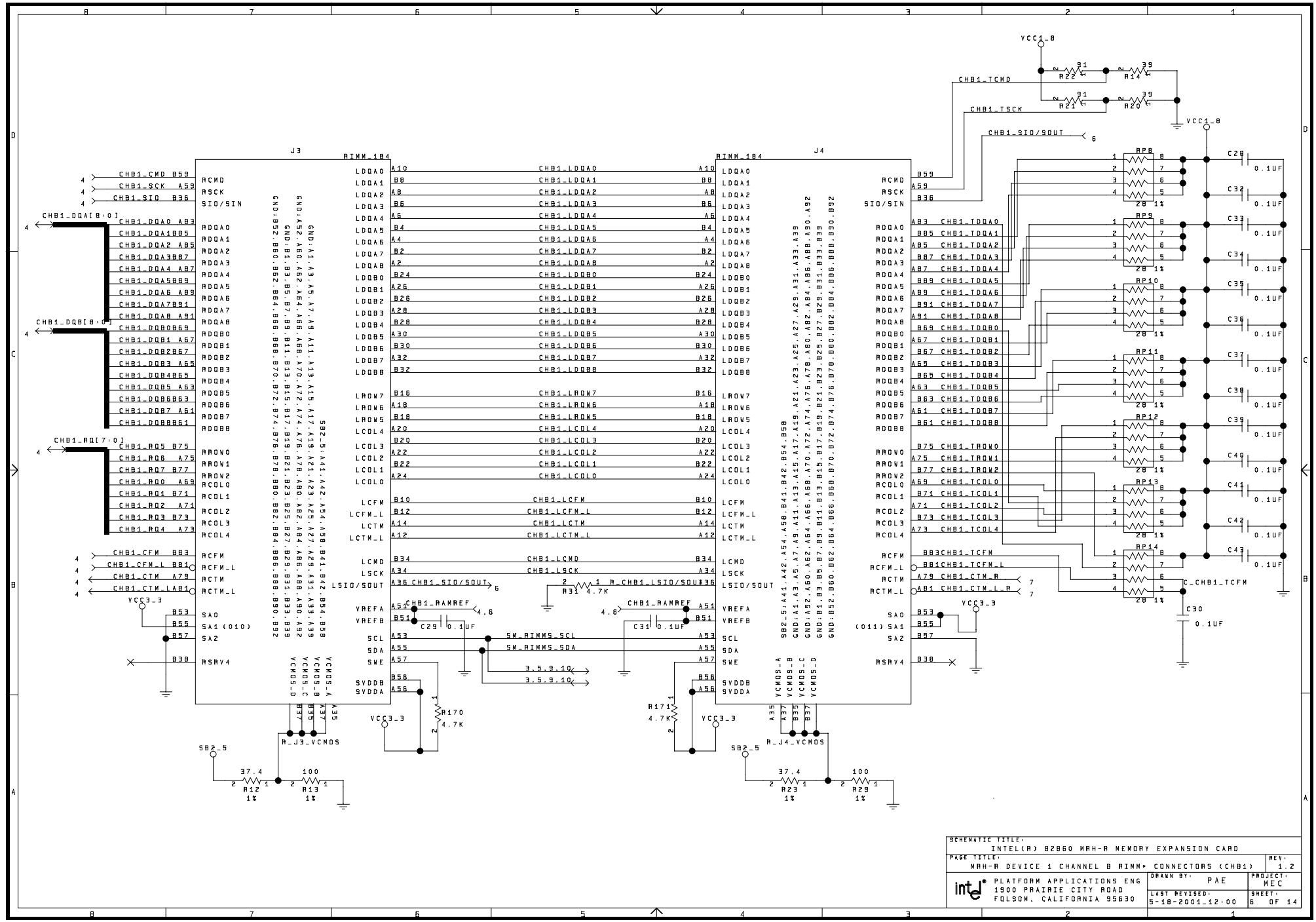

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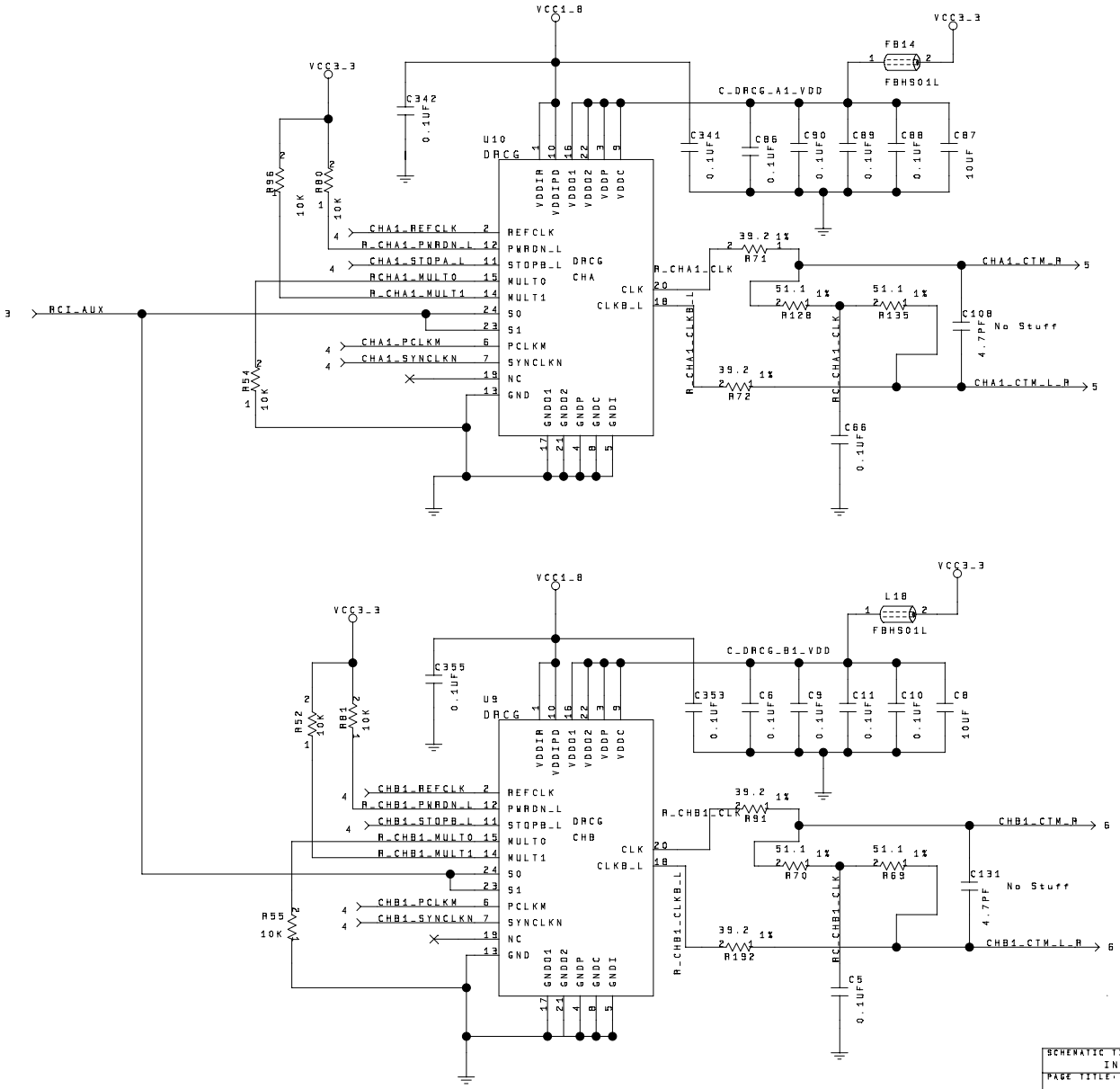

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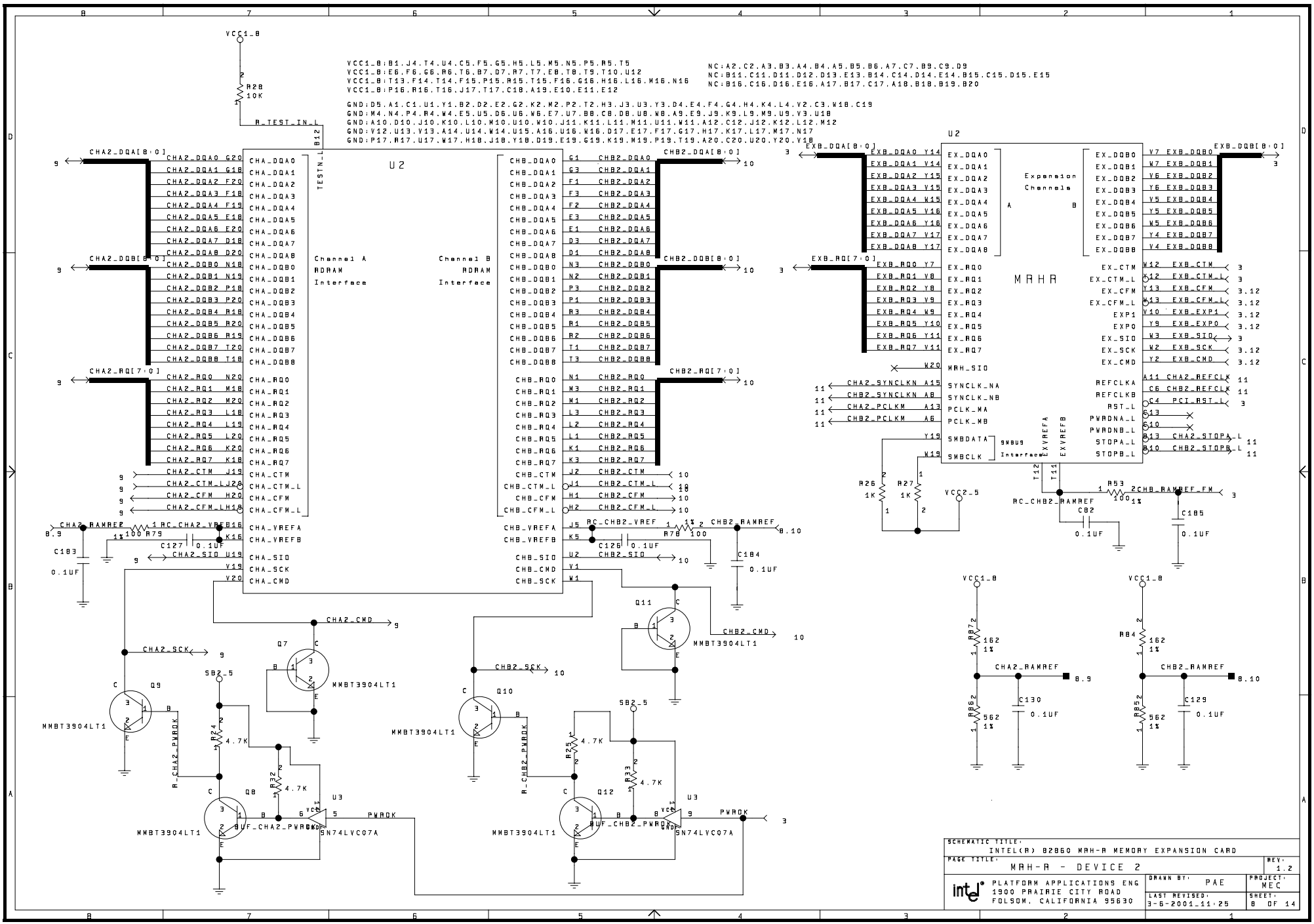
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VCC1_8: E6, F6, G6, R6, T6, B7, D7, R7, T7, E8, T8, T9, T10, U12
VCC1_8: T13, F14, T14, F15, P15, R15, T15, F16, G16, H16, L16, M16, N16
VCC1_8: P16, R16, T16, J17, T17, C18, A19, E10, E11, E12
NC: A2, C2, A3, B3, A4, B4, A5, B5, B6, A7, C7, B9, C9, D9
NC: B11, C11, D11, D12, D13, E13, B14, C14, D14, E14, B15, C15, D15, E15
NC: B16, C16, D16, E16, A17, B17, C17, A18, B18, B19, B20
GND: D5, A1, C1, U1, Y1, B2, D2, E2, G2, K2, M2, P2, T2, H3, J3, U3, Y3, D4, E4, F4, G4, H4, K4, L4, V2, C3, W18, C19
GND: M4, N4, P4, R4, W4, E5, U5, D6, U6, W6, E7, U7, B8, C8, D8, U8, W8, A9, E9, J9, K9, L9, M9, U9, V3, U18
GND: A10, D10, J10, K10, L10, M10, U10, W10, J11, K11, L11, M11, U11, W11, A12, C12, J12, K12, L12, M12
GND: V12, U13, V13, A14, U14, W14, U15, A16, U16, W16, D17, E17, F17, G17, H17, K17, L17, M17, N17
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U2
CHA2_DQA[8:0]
CHA2_DQB[8:0]
CHA2_RQ[7:0]
CHA_DQA0 CHA_DQA1 CHA_DQA2 CHA_DQA3 CHA_DQA4 CHA_DQA5 CHA_DQA6 CHA_DQA7 CHA_DQA8
CHA_DQB0 CHA_DQB1 CHA_DQB2 CHA_DQB3 CHA_DQB4 CHA_DQB5 CHA_DQB6 CHA_DQB7 CHA_DQB8
CHA_RQ0 CHA_RQ1 CHA_RQ2 CHA_RQ3 CHA_RQ4 CHA_RQ5 CHA_RQ6 CHA_RQ7
CHA_CTM CHA_CTM_L CHA_CFM CHA_CFM_L
CHA_VREFA CHA_VREFB
CHA_SIO CHA_SCK CHA_CMD
TESTN_L
Channel A RDRAM Interface
Channel B RDRAM Interface
CHB_DQA0 CHB_DQA1 CHB_DQA2 CHB_DQA3 CHB_DQA4 CHB_DQA5 CHB_DQA6 CHB_DQA7 CHB_DQA8
CHB_DQB0 CHB_DQB1 CHB_DQB2 CHB_DQB3 CHB_DQB4 CHB_DQB5 CHB_DQB6 CHB_DQB7 CHB_DQB8
CHB_RQ0 CHB_RQ1 CHB_RQ2 CHB_RQ3 CHB_RQ4 CHB_RQ5 CHB_RQ6 CHB_RQ7
CHB_CTM CHB_CTM_L CHB_CFM CHB_CFM_L
CHB_VREFA CHB_VREFB
CHB_SIO CHB_CMD CHB_SCK
CHB2_DQA[8:0]
CHB2_DQB[8:0]
CHB2_RQ[7:0]
C183 0.1UF
C127 0.1UF
R79 100 1%
RC_CHA2_VREF
CHA2_RAMREF
C126 0.1UF
R78 100 1%
RC_CHB2_VREF
CHB2_RAMREF
C184 0.1UF
Q7 MMBT3904LT1
Q8 MMBT3904LT1
Q9 MMBT3904LT1
Q10 MMBT3904LT1
Q11 MMBT3904LT1
Q12 MMBT3904LT1
R24 4.7K
R32 4.7K
R25 4.7K
R33 4.7K
R_CHA2_PWROK
R_CHB2_PWROK
SB2_5
U3
BUF_CHA2_PWROK
BUF_CHB2_PWROK
SN74LVC07A
PWROK
EXB_DQA[8:0]
EXB_DQB[8:0]
EXB_RQ[7:0]
EX_DQA0 EX_DQA1 EX_DQA2 EX_DQA3 EX_DQA4 EX_DQA5 EX_DQA6 EX_DQA7 EX_DQA8
EX_DQB0 EX_DQB1 EX_DQB2 EX_DQB3 EX_DQB4 EX_DQB5 EX_DQB6 EX_DQB7 EX_DQB8
EX_RQ0 EX_RQ1 EX_RQ2 EX_RQ3 EX_RQ4 EX_RQ5 EX_RQ6 EX_RQ7
MRH_SIO
SYNCLK_NA SYNCLK_NB PCLK_MA PCLK_MB
SMBDATA SMBCLK SMBus Interface
EXVREFA EXVREFB
EX_CTM EX_CTM_L EX_CFM EX_CFM_L EXP1 EXP0 EX_SIO EX_SCK EX_CMD
REFCLKA REFCLKB RST_L PWRDNA_L PWRDNB_L STOPA_L STOPB_L
Expansion Channels
A
B
MRHR
CHA2_SYNCLKN CHB2_SYNCLKN CHA2_PCLKM CHB2_PCLKM
EXB_CTM EXB_CFM EXB_EXP1 EXB_EXP0 EXB_SIO EXB_SCK EXB_CMD
CHA2_REFCLK CHB2_REFCLK PCI_RST_L
CHA2_STOPA_L CHB2_STOPB_L
R26 1K
R27 1K
VCC2_5
RC_CHB2_RAMREF
R53 100 1%
CHB_RAMREF_FM
C82 0.1UF
C185 0.1UF
R87 162 1%
R84 162 1%
R862 562 1%
R852 562 1%
C130 0.1UF
C129 0.1UF
SCHEMATIC TITLE: INTEL(R) 82860 MRH-R MEMORY EXPANSION CARD
PAGE TITLE: MRH-R - DEVICE 2
REV: 1.2
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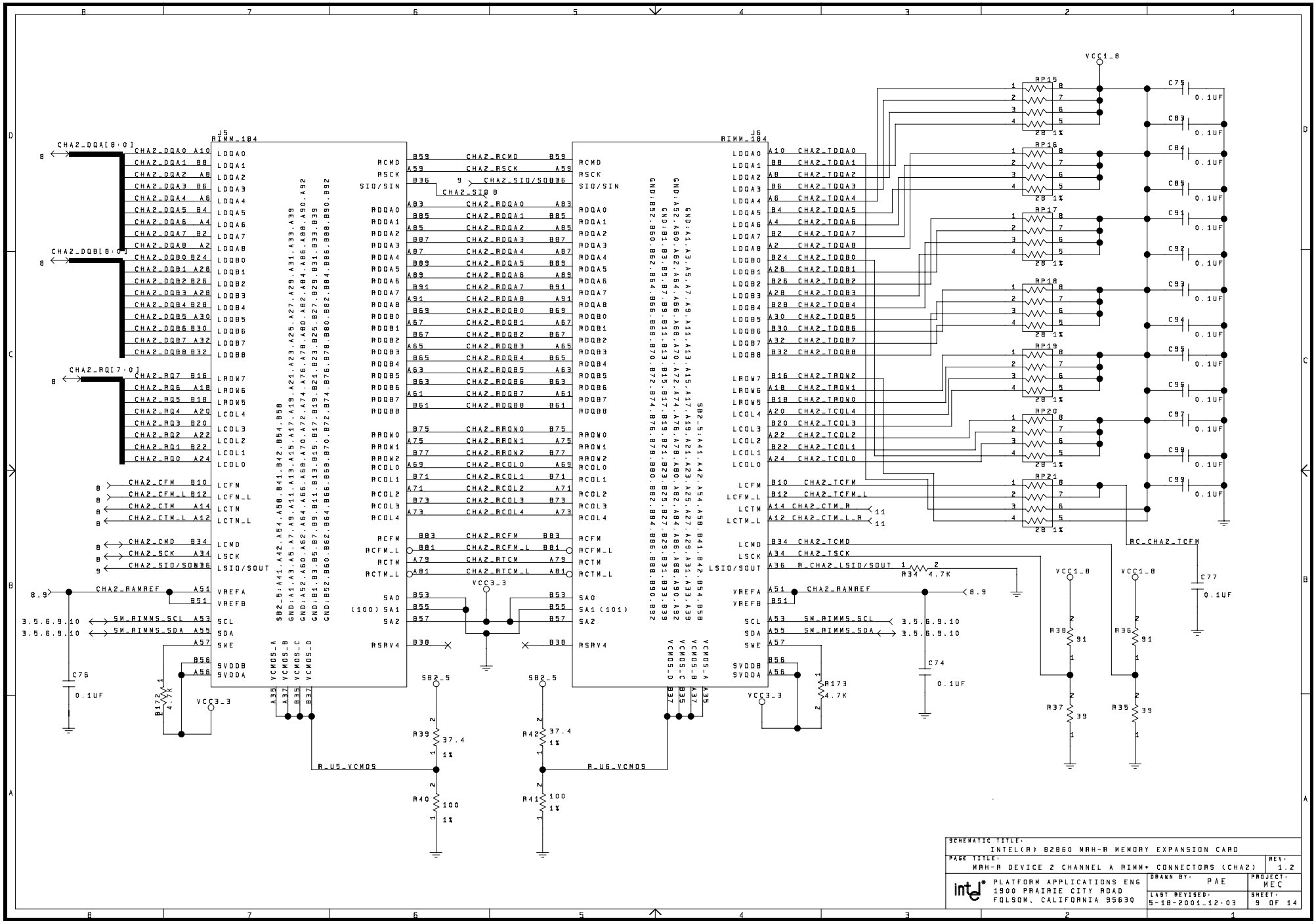
DRAWN BY: PAE
PROJECT: MEC
LAST REVISED: 3-6-2001 11:25
SHEET: 8 OF 14



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INTEL(R) 82860 MRH-R MEMORY EXPANSION CARD

PAGE TITLE:
MRH-R DEVICE 2 CHANNEL A RIMM* CONNECTORS (CHA2)

REV: 1.2

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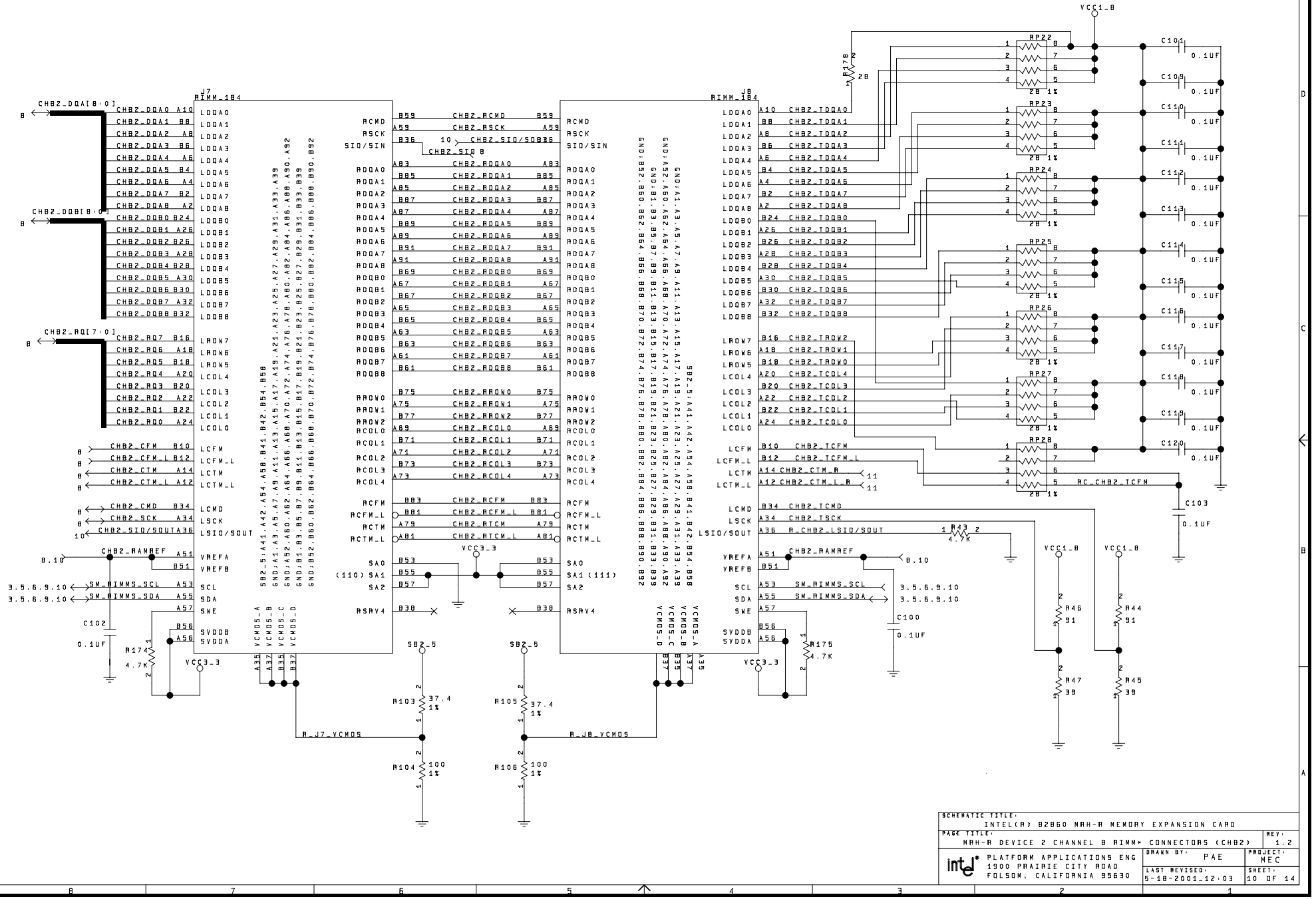

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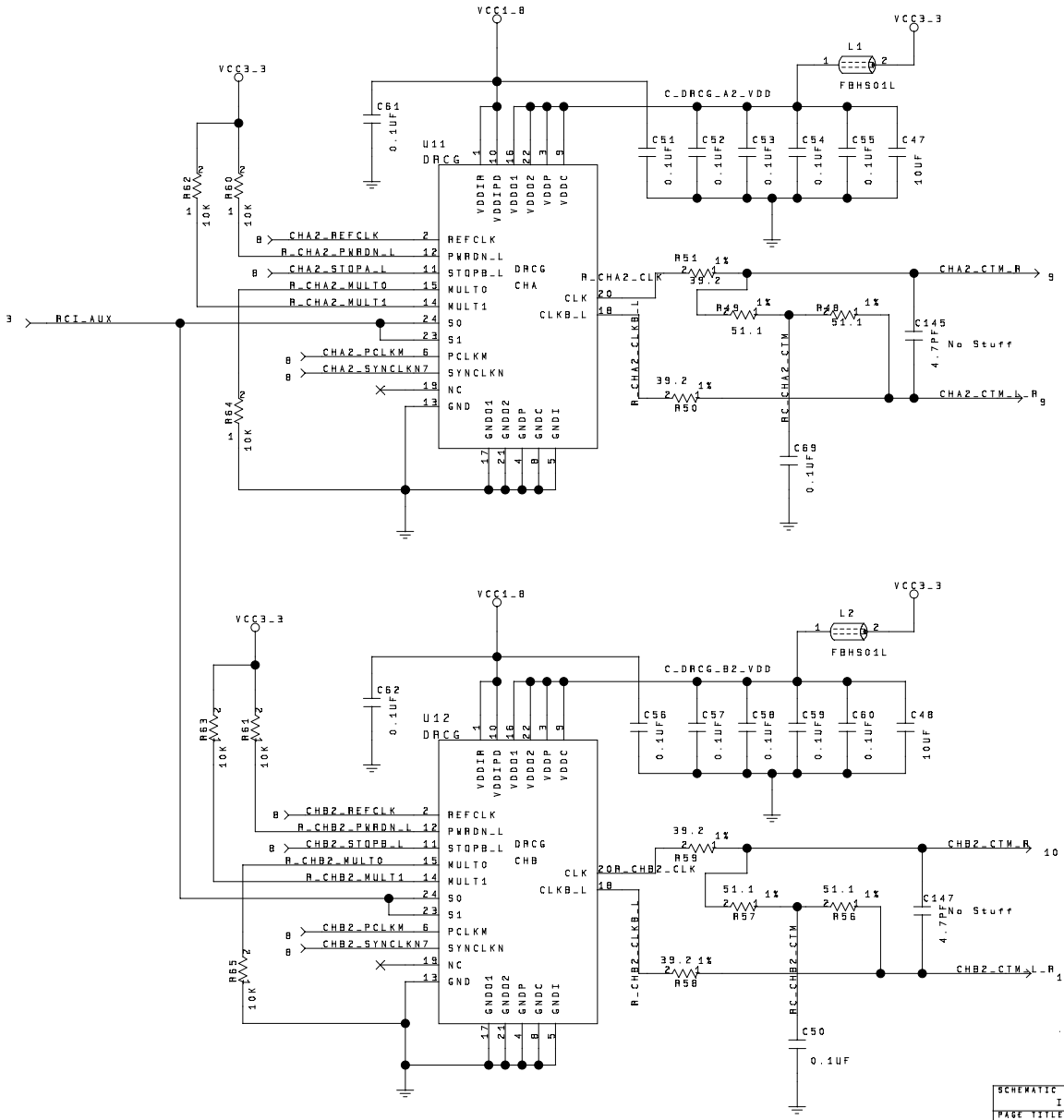

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PAGE TITLE: MRH-R DEVICE 2 DRCG+ SYNTHESIZERS

REV: 1.2

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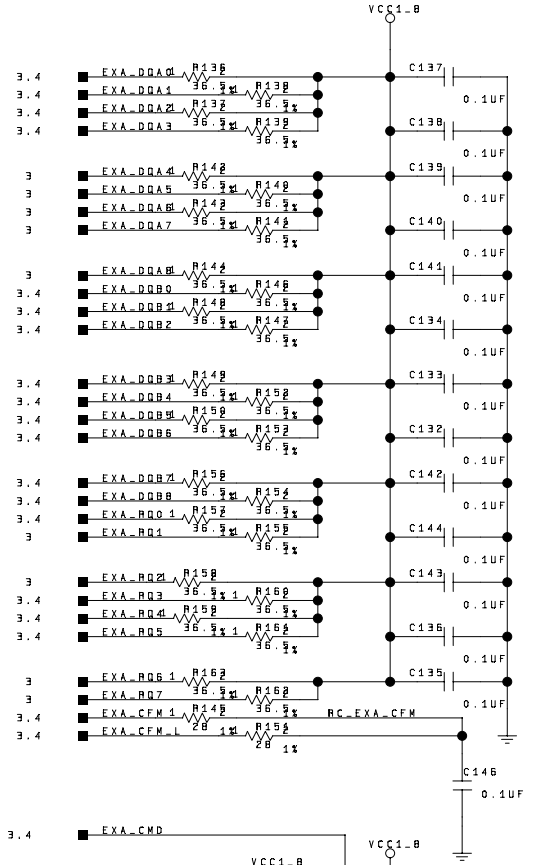
Expansion Channel A



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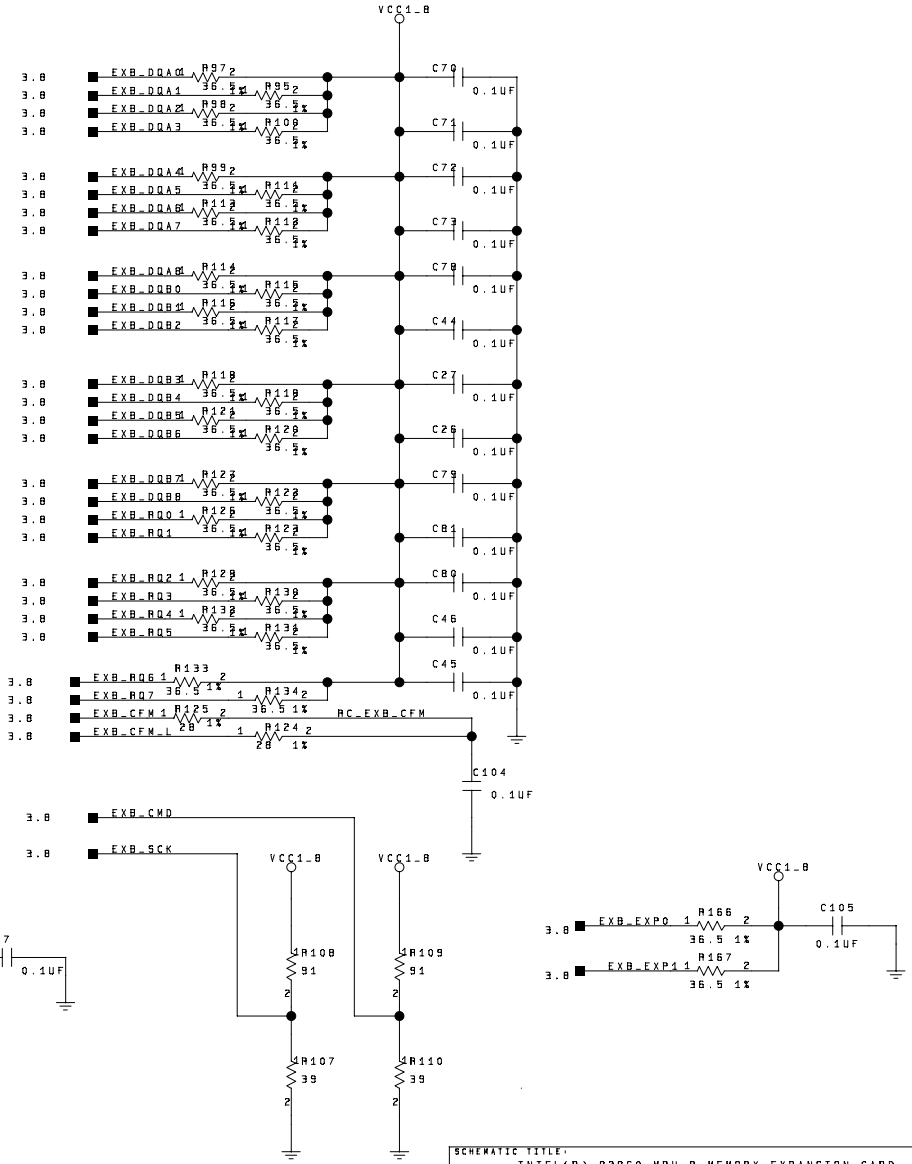

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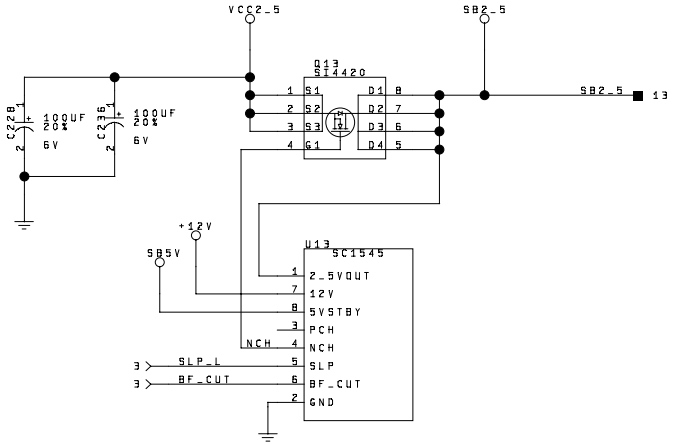
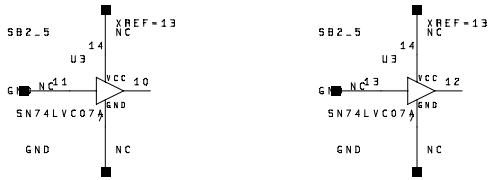
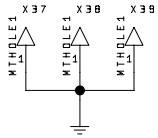


Spares



Mounting Holes



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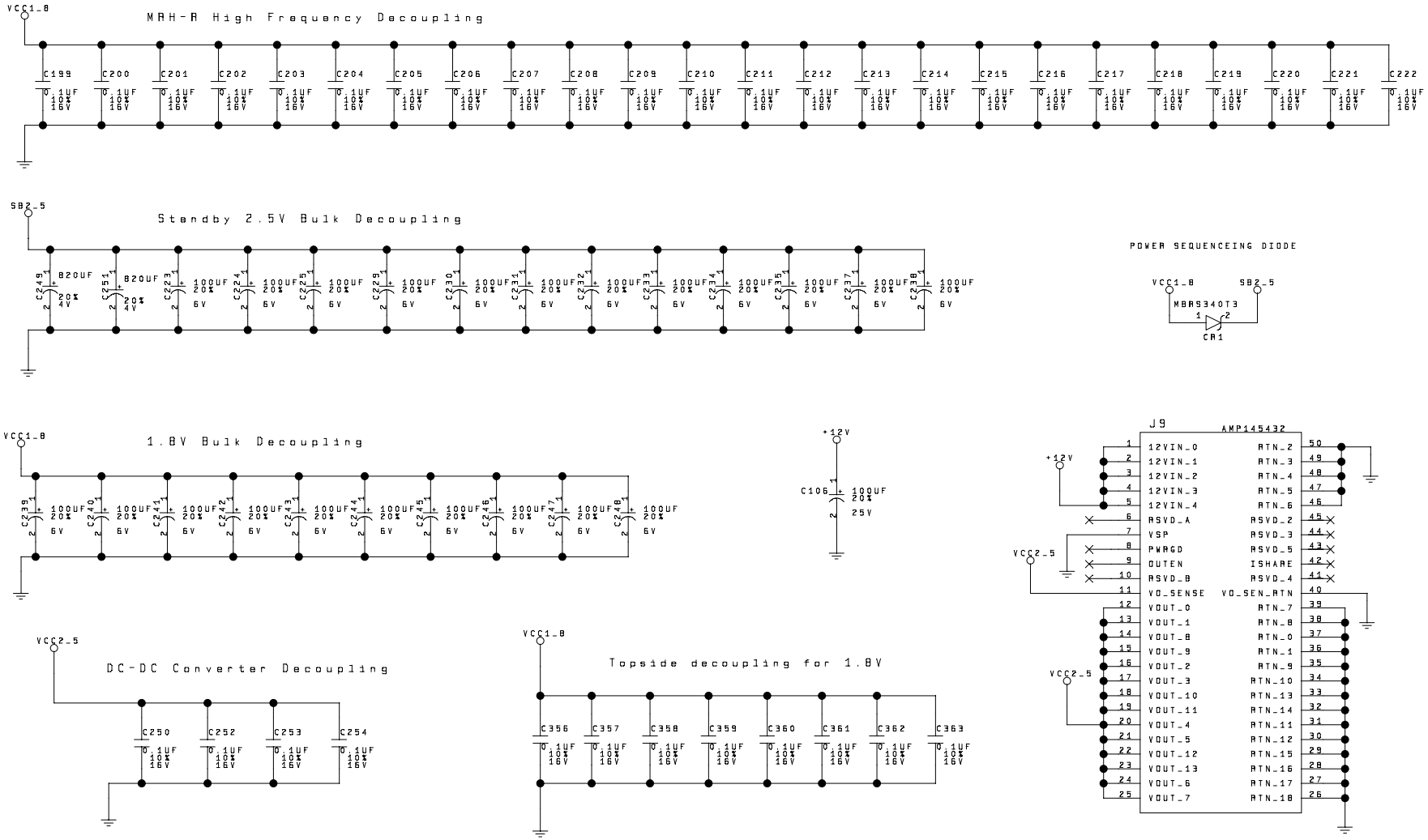

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	LAST REVISED: 3-6-2001_11:25	SHEET: 14 OF 14