Intel® 810E2 Chipset Platform

Design Guide Update

April 2002

Notice: The Intel® 810E2 Chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 298305-002

Contents

Revision History

Revision	Changes	Date
1.0	Initial Release	March 2002
2.0	Added Documentation Changes #31	April 2002

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 810E2 Chipset Platform Design Guide	298248

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 810E2 Chipset.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Shaded: This item is either new or modified from the previous version of the document.

Number	GENERAL DESIGN CONSIDERATIONS
	There are no General Design Considerations updates in this Design Guide Update revision.

Number	SCHEMATIC, LAYOUT AND ROUTING UPDATES
	There are no Schematic, Layout, or Routing Updates in this Design Guide Update revision

Number	DOCUMENTATION CHANGES
1	Added: RTC-Well Input Strap Requirements, Section 3.20.8
2	Changed: LAN Layout Guidelines, Section 3.21; Expanded
3	Changed: Point-To-Point Interconnect, Section 3.21.1.2; Table Modified
4	Changed: General Trace Routing Considerations, Section 3.21.2.1; Modified
5	Changed: 82562ET / 82562EM Termination Resistors, Section 3.21.4.3; Modified
6	Changed: 82562ET / 82562EH Dual Footprint Guidelines, Section 3.21.5; Modified
7	Changed: Compensation, Section 3.6.4; Figures Modified
8	Changed: VCCcore Decoupling Design, Section 2.2.1.1; Modified
9	Changed: PCI Interface, Section 7.2.1; Modified
10	Changed: Power Management, Section 7.2.9; Modified
11	Changed: RTC-Well Input Strap Requirements, Section 3.20.8; Title Changed
12	Changed: RTC Crystal, Section 3.20.1, Modified
13	Changed: RTC, RTCX1-RTCX2 Checklist Item, Section 7.2.13; Modified
14	Changed: Section 3.1, General Recommended; Expanded
15	Changed: 82562ET / 82562EH Dual Footprint Guidelines, Section 3.21.5; Modified
16	Changed: FWH Vpp Design Guidelines, Section 3.22.2; Expanded
17	Added: 82562ET/EM Disable Guidelines, Section 3.21.4.6
18	Changed: RTC, Section 7.2.13; Expanded
19	Changed: USB, Section 3.15; Modified
20	Added Information and Figure to Section 3.20.8, (see documentation changes #11 for details) Power-Well Isolation Control Strap Requirements.
21	Changed Section 7.2.9, Power Management.
22	Added Section 6.5 Power Supply PS_ON Considerations
23	Changed Section 7.2.13, RTC, Add SUSCLK To The Checklist
24	Changed Section 7.2.16, Power, Modify Checklist Recommendations for 5V_REF_SUS
25	Changed Section 6.4.3, 3.3V/V5REF Sequencing
26	Changed Figure 48, Trace Routing, in Section 3.21.2.1, General Trace Routing Considerations
27	RTC Power Well Isolation Control, in Section 3.20.8, Power Well Isolation Control Strap Requirements
28	Changed Section 6.4.3, 3.3V/5VREF Sequencing on first and third paragraphs
29	Changed: Section 7.2.16, Power, Modify Checklist Recommendations for 5V_REF_SUS
30	Changed: Section 7.2.6, Interrupt interface, Modify Checklist items for APIC
31	Changed: Figure 81, Replaced Power Delivery Map

General Design Considerations

There are no General Design Considerations updates in this Design Guide Update revision.

Schematic, Layout and Routing Updates

There are no Schematic, Layout, or Routing Updates in this Design Guide Update revision.

Documentation Changes

1. Added: RTC-Well Input Strap Requirements, Section 3.20.8

3.20.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 43 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

2. Changed: LAN Layout Guidelines, Section 3.21; Expanded

Two sentences are added to the first paragraph of Section 3.21, *LAN Layout Guidelines*, as shown.

> The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

3. Changed: Point-To-Point Interconnect, Section 3.21.1.2; Table Modified

Table 23, *Single-Solution Interconnect Length Requirement*, the new 82562ET length is 3.5 inches instead of 4.5 inches.

Configuration	L	Comment
82562EH	4.5” to 10”	Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected.
82562ET	3.5” to 10”	
CNR	3” to 9”	The trace length from the connector to LOM should be 0.5” to 3.0”

4. Changed: General Trace Routing Considerations, Section 3.21.2.1; Modified

Bullet 5 of Para 3.21.2.1, General Trace Routing Considerations is changed to read:

- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.

5. Changed: 82562ET / 82562EM Termination Resistors, Section 3.21.4.3; Modified

The first paragraph shown under Section 3.21.4.3, *82562ET / 82562EM Termination Resistors*, has an incorrect resistor value for the 1% receive differential pairs (RDP/RDN). The value is changed from 100 Ω to 120 Ω. The paragraph should read:

> The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the LAN connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

6. Changed: 82562ET / 82562EH Dual Footprint Guidelines, Section 3.21.5; Modified

The first paragraph shown under Section 3.21.5, *82562ET / 82562EM Dual Footprint Guidelines*, references an incorrect section of the Design Guide. The fourth sentence of the paragraph should read:

> The guidelines called out in Sections 3.21.1 through 3.21.4 apply to this configuration.

7. Changed: Compensation, Section 3.6.4; Figures Modified

Figure 23, *Single Hub Interface Reference Divider Circuit*, 1.85 V label needs to be changed to 1.80 V.

Figure 24, *Locally Generated Hub Interface Reference Dividers*, both 1.85 V labels need to be changed to 1.80 V.

8. Changed: VCCcore Decoupling Design, Section 2.2.1.1; Modified

In Section 2.2.1.1, *VCCcore Decoupling Design*, add second bullet:

- 8 ea (min) 1 µF 0612 package placed in the Intel® PGA370 socket cavity.

9. Changed: PCI Interface, Section 7.2.1; Modified

The PME# checklist item in Section 7.2.1, *PCI Interface*, is changed as shown below:

PME#	This signal has an integrated pull-up of 24K.

10. Changed: Power Management, Section 7.2.9; Modified

The PWRBTN# checklist item in Section 7.2.9, *Power Management*, is changed as shown below:

PWRBTN#	This signal has an integrated pull-up of 24K.

11. Changed: RTC-Well Input Strap Requirements, Section 3.20.8; Title Changed

The title of Section 3.20.8. is changed to *Power-Well Isolation Control Strap Requirements*.

12. Changed: RTC Crystal, Section 3.20.1, Modified

Section 3.20.1, *RTC Crystal*, Figure 52, *External Circuitry for the ICH2 RTC*, Note 1, is changed as shown below:

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C2 and C3 are 18 pF for a crystal with C_{LOAD}=12.5 pF)

13. Changed: RTC, RTCX1-RTCX2 Checklist Item, Section 7.2.13; Modified

The first sentence in the RTCX1-RTCX2 checklist item in Section 7.2.13, RTC is changed as shown below:

RTCX1 RTCX2	Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling caps (assuming crystal with CLOAD=12.5 pF) at each signal.

14. Changed: Section 3.1, General Recommended; Expanded

The last paragraph of Section 3.1, General Recommendations, has the following material added to it so that the paragraph reads as follows:

> Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in the following figure. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

15. Changed: 82562ET / 82562EH Dual Footprint Guidelines, Section 3.21.5; Modified

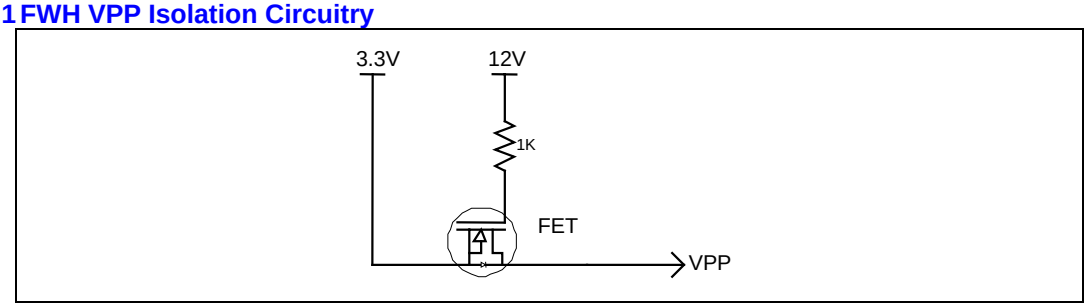
The bullets under Figure 55, *Dual-Footprint Analog Interface*, describe additional guidelines for Figures 55 and 56. The first bullet defines the “L” in Figure 56, *Dual Footprint LAN Connect Interface*. The “L” value is changed to 3.5 inches to 10 inches.

16. Changed: FWH Vpp Design Guidelines, Section 3.22.2; Expanded

Section 3.22.2., FWH Vpp Design Guidelines, has the following paragraph and figure added as shown below:

> In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 56.1 FWH VPP Isolation Circuitry

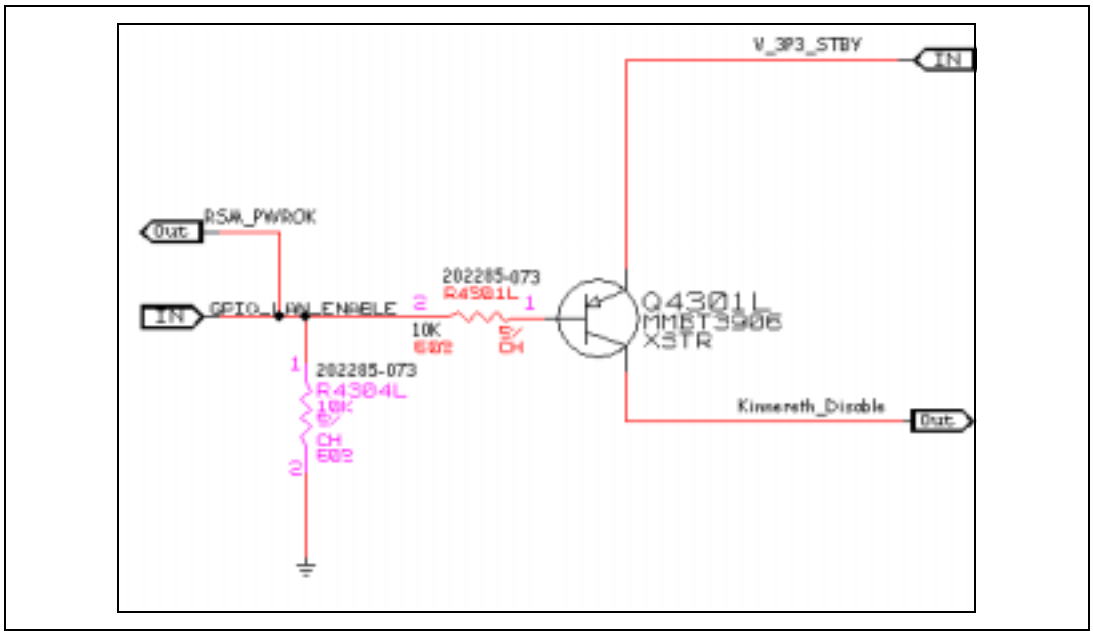


17. Added: 82562ET/EM Disable Guidelines, Section 3.21.4.6

3.21.4.6 82562ET/EM Disable Guidelines

To disable the 82562ET/EM (82562ET/EM), the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS, by controlling the GPIO, can disable the LAN microcontroller.

Figure 53-1: 82562ET/EM Disable Circuit



There are four pins which are used to put the 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

The four control signals shown in the above table should be configured as follows: Test_En should be pulled-down through a 100 Ω resistor. The remaining 3 control signals should each be connected through 100 Ω series resistors to the common node “82562ET/EM_Disable” of the disable circuit.

18. Changed: RTC, Section 7.2.13; Expanded

The following checklist item is added to Section 7.2.13, *RTC*:

RTCRST#	Ensure 10 ms-20 ms RC delay (8.2 K & 2.2 µF) See Figure, *RTCRST External Circuit for the ICH2 RTC*.

19. Changed: USB, Section 3.15; Modified

The third bullet in Section 3.15, *USB*, is changed to read as follows:

An optional cap (0 pF – 47pF) may be placed as close to the USB connector side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap should be sized to minimize EMI radiation while still maintaining signal quality (rise/fall time, Vcrs, etc).

20. Added Information and Figure to Section 3.20.8, Power-Well Isolation Control Strap Requirements

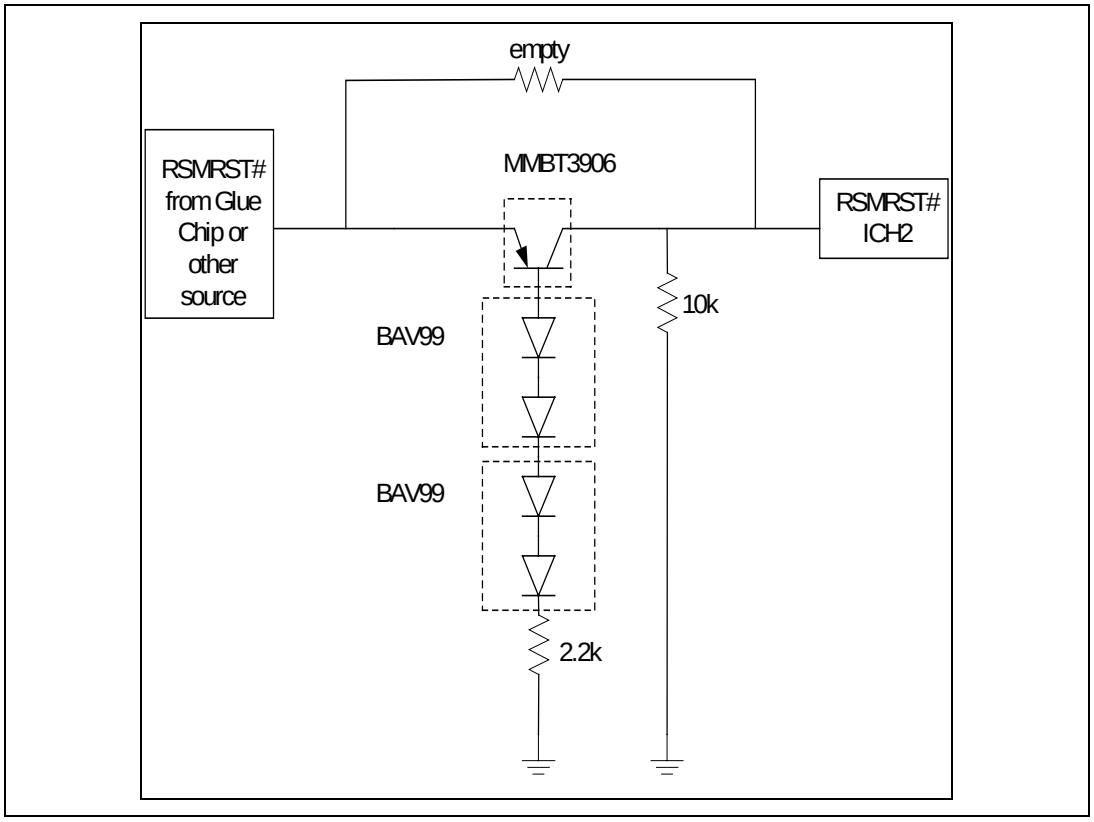
Add the following information and figure to Section 3.20.8, Power-Well Isolation Control Strap Requirements:

The circuit shown in the figure below should be implemented to control well isolation between the

3.3V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on

the VCCRTC node during Sx- to-G3 power state transitions (removal of AC power).

A RTC Power Well Isolation Control



21. Changed Section 7.2.9, Power Management

Change the Recommendations for RSMRST# in Section 7.2.9, Power Management, to read as shown below:

"Connect to power monitoring logic, and should go high no sooner than 10mS after both VccSUS3_3 and VccSus1_8 have reached their nominal voltages. Requires weak pull-down. Also requires well isolation control as directed in section 3.20.8.

22. Added: Section 6.5 Power_Supply PS_ON Considerations

The following new section is added:

6.5 Power_Supply PS_ON Considerations

If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10-100mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

23. Changed: Section 7.2.13, RTC, Add SUSCLK To The Checklist

Add the following as a new checklist item to Section 7.2.13, RTC:

SUSCLK	To assist in RTC circuit debug, route SUSCLK to a test point if it is unused.

24. Changed: Section 7.2.16, Power, Modify Checklist Recommendations for 5V_REF_SUS

Change the second bullet in the Recommendations column of the 5V_REF_SUS to the following:

V5REF_SUS affects 5V-tolerance for all USB pins and can be connected to VccSUS3_3 if ICH2 USB is not supported in the platform. If USB is supported, 5VREF_SUS must be connected to 5V_AUX, which remains powered during S5.

25. Changed: Section 6.4.3, 3.3V/V5REF Sequencing

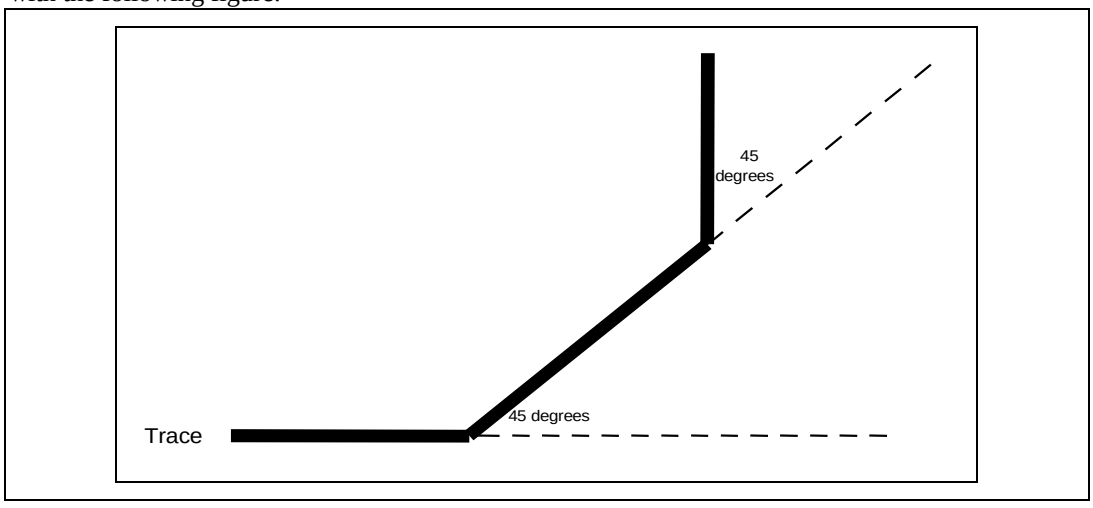
Change the second and third paragraphs of Section 6.4.3, 3.3V/V5REF Sequencing to the following:

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX, which remains powered during S5.

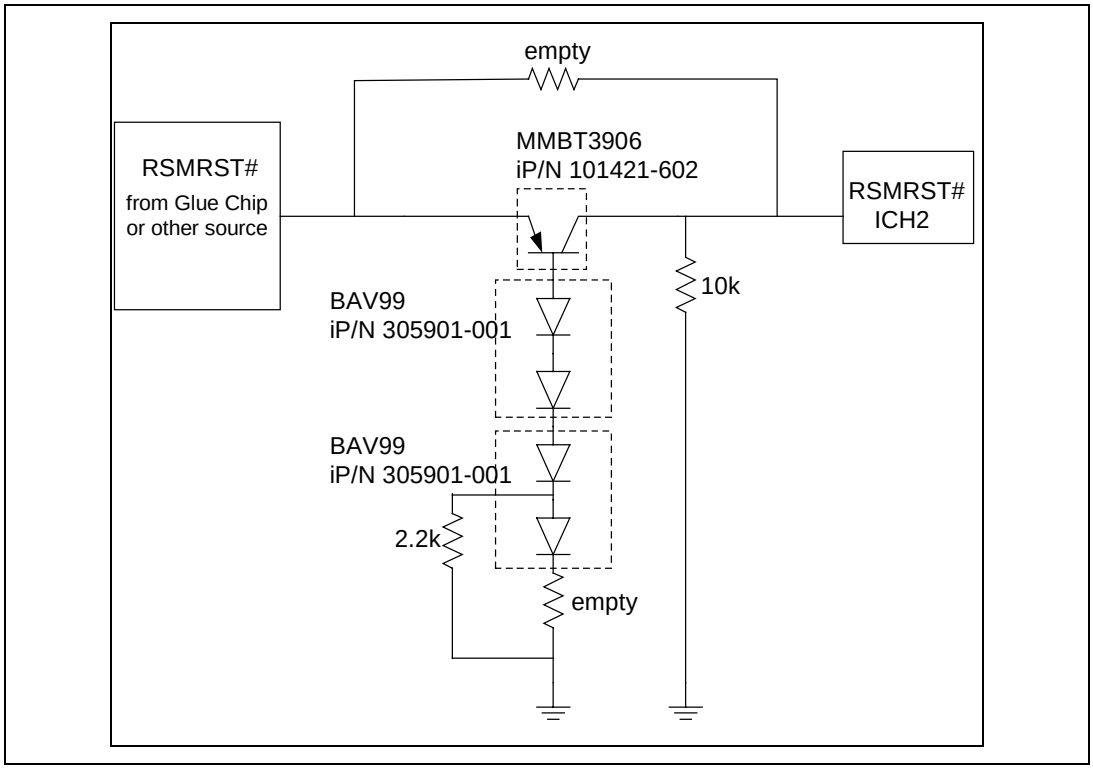
26. Changed: Figure 48, Trace Routing, in Section 3.21.2.1, General Trace Routing Considerations.

Figure 48, Trace Routing, in Section 3.21.2.1, General Trace Routing Considerations, is replaced with the following figure:



27. Changed RTC Power Well Isolation Control, in Section 3.20.8, Power Well Isolation Control Strap Requirements

RTC Power Well Isolation Control table was been added in Intel® 810E2 Chipset Platform Design Guide Update, dated July 18, 2001, Document Number 298305-002, as document change #20 and is now changed to the following:



28. Changed: Section 6.4.3, 3.3V/5VREF Sequencing

Change the first and third paragraphs of Section 6.4.3, 3.3V/5VREF Sequencing to the following:

V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within .7V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within .7V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 87 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

As an additional consideration, during suspend, the only signals that are 5V tolerant capable are USB OC:[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX. If OC:[3:0]# is needed during suspend and 5V tolerance

is required then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX rails.

29. Changed: Section 7.2.16, Power, Modify Checklist: Recommendations for 5V_REF_SUS

V5REF_SUS only affects 5V-tolerance for USB OC:[3:0]# pins and can be connected to either VccSUS3_3 or 5V_Always/5V_AUX if 5V tolerance on these OC:[3:0]# is not needed. If 5V tolerance on OC:[3:0]# is needed then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5.

30. Changed: Section 7.2.6, Interrupt interface, Modify: Checklist items for APIC

Intel® Pentium® 4 processor based systems:

These processors do not have APIC pins so all platforms using this processor should both tie APICCLK to ground and tie APICD:[1:0] to ground via a 1K-10K pull-down resistor.

Non- Pentium® 4 processor based systems:

If the APIC is used: 150Ω pull-up resistors on APICD[1:0]

Connect APICCLK to CK133 with a 20-33Ω series termination resistor.

If the APIC is not used on up systems:

The APICCLK can either be tied to GND or connected to CK133, but not left floating.

Pull APICD[1:0] to GND through 10kΩ pull-down resistors.

31. Changed: Figure 81, Power Delivery Map

Two existing ICH2 power planes are added to figure 81, Power Delivery Map.

Figure 81. Power Delivery Map