Intel® 815EP Chipset Platform

For Use with Universal Socket 370

Design Guide

September 2002

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Revision History

Rev. No.	Description	Rev. Date
-001	• Initial Release. This document is written as an Intel® 82815EP Design Guide for Use with the Universal Socket 370. This document does not replace Document Number 290692-001, which is an 82815EP design guide for use only with 0.18 micron technology Intel® Celeron® and Intel® Pentium® III processors	September 2001
-002	• Added Section 9.4, Power Supply PS_ON Considerations • Added SUSCLK to Section 13.4.12, RTC Checklist • Revised Section 13.4.15, Power Checklist recommendations for V5_REF_SUS • Revised Section 12.4.3, 3.3V/V5REF Sequencing • Replaced Figure 82, RTC Power Well Isolation Control, in Section 10.8.6, Power Well Isolation Control • Revised Table 40, CK-815 (2-DIMM) Clocks, in Section 11.1, 2-DIMM Clocking • Revised Table 41, CK-815 (3-DIMM) Clocks, in Section 11.2, 3-DIMM Clocking • Replaced Figure 101, Power Delivery Map, in Section 12, Power Delivery • Added Section 2.4, Electrostatic Discharge Platform Recommendations	September 2002

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1 Introduction

1.1 Design Guide and Chipset Basic Information

This design guide organizes Intel design recommendations for the Intel® 815EP chipset platform for use with universal socket 370. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document also addresses system design issues such as thermal requirements for the Intel® 82815EP chipset platform.

This design guide contains design recommendations, debug recommendations, and a system checklist. These design guidelines are developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

Consult the debug recommendations when debugging your design. However, these debug recommendations should be understood before completing board design to ensure that the debug port, in addition to other debug features, are implemented correctly.

There is no internal graphics capability in the 82815EP MCH. The 82815EP uses an external AGP card only.

There are six chipsets in the 815 chipset family:

- Intel® 82815 chipset: This chipset contains the 82815 and the Intel® 82801AA ICH.
- Intel® 82815E chipset: This chipset contains the 82815E and the Intel® 82801BA ICH2.
- Intel® 82815P chipset: This chipset contains the 82815P and the 82801AA ICH. There is no internal graphics capability. This GMCH uses an AGP port only.
- Intel® 82815EP chipset: This chipset contains the 82815EP and the 82801BA ICH2. There is no internal graphics capability. This GMCH uses an AGP port only.
- Intel® 82815G chipset: This chipset contains the 82815G GMCH and 82801AA ICH. There is no AGP port capability. This GMCH uses internal graphics only.
- Intel® 82815EG chipset. This chipset contains the 82815EG GMCH and 82801BA ICH2. There is no AGP port capability. This GMCH uses internal graphics only.

The only component difference between the 82815 GMCH and the 82815E GMCH is the I/O Controller Hub. The only component difference between the 82815P GMCH and the 82815EP GMCH is the I/O Controller Hub. The only component difference between the 82815G GMCH and the 82815EG GMCH is the I/O Controller Hub.

The 815EP chipset platform supports the following processors:

- Future Intel® Celeron® and Intel® Pentium® III processors based on 0.13 micron socket 370 processors.
- Pentium III processor based on 0.18 micron technology (CPUID = 068xh).

- Celeron processor based on 0.18 micron technology (CPUID = 068xh). This applies to Celeron 533A MHz and ≥566 MHz processors.

Note: The system bus speed supported by the design is based on the capabilities of the processor, chipset, and clock driver.

Note: The 815EP chipset for use with the universal socket 370 is **not** compatible with the Intel® Pentium® II processor (CPUID = 066xh) 370-pin socket.

1.2 Terminology

This section describes some of the terms used in this document. Additional power delivery term definitions are provided at the beginning of *Chapter12, "*Power Delivery*"*.

Term	Description
AGP	Accelerated Graphics Port
AGTL/AGTL+	Refers to processor bus signals that are implemented using either Assisted Gunning Transceiver Logic (AGTL+) or its lower voltage variant (AGTL), depending on which processor is being used.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk–coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Crosstalk–coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
MCH	Memory Controller Hub. A component of the Intel® 815EP chipset platform for use with the Universal Socket 370
ICH	82801AA I/O Controller Hub component.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.

Term	Description
Network Length	The distance between agent 0 pins and the agent pins at the far end of the bus.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on a substrate such as the motherboard. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) Effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or “push-out”), or a decrease in propagation delay (or “pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
System Bus	The system bus is the processor bus.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.
Universal Socket 370	Refers to the 815EP chipset using the “universal” PGA370 socket. In general, these designs support 66/100/133 MHz system bus operation, Intel® VRM guidelines for future 0.13 micron processors, and Intel® Celeron® processors (CPUID=068xh), Intel® Pentium® III processor (CPUID=068xh), and future Celeron and Pentium III processors using 0.13 micron technology processors in single-microprocessor based designs.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

1.3 Reference Documents

Document	Document Number / Location
Intel® 815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH) for use with the Universal Socket 370 Datasheet	290720 Intel Developer Website
Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet	290658 Intel Developer Website
Intel® 82801BA I/O Controller Hub (ICH2) *and Intel® 82801BAM I/O Controller Hub* (ICH2-M) Datasheet	290687 Intel Developer Website
Intel® Pentium® III Processor Specification Update (latest revision from website)	Intel Developer Website
AP 907 Intel® Pentium® III Processor Power Distribution Guidelines	245085 Intel Developer Website
Accelerated Graphics Port Specification, Revision 2.0	http://www.intel.com/technology/agp/agp_index.htm)
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/specifications/conventional_pci
Universal Serial Bus Specification, Revision 2.0	http://www.usb.org/developers/usb20/
AC '97 Component Specification, Revision 2.2(1)	http://developer.intel.com/pc-supp/platform/ac97/index.htm
Low Pin Count Interface Specification, Version 1.0	http://www.intel.com/design/chipsets/industry/lpc.htm

NOTES: 1. Throughout this document, this specification will be referred to as *AC '97 v2.2*

1.4 System Overview

The 815EP chipset platform for future use with the universal socket 370 contains a Memory Controller Hub (MCH) component and I/O Controller Hub 2 (ICH2) component for desktop platforms.

The MCH provides the processor interface (optimized for future 0.13 micron technology Celeron and Pentium III socket 370 processors and the Pentium III processor (CPUID = 068xh)), DRAM interface, hub interface, and an Accelerated Graphics Port (AGP) interface. It does not provide support for internal graphics. This product provides flexibility and scalability in memory subsystem performance. Competitive graphics may be scaled via an AGP card interface, and PC100 SDRAM system memory may be scaled to PC133 system memory.

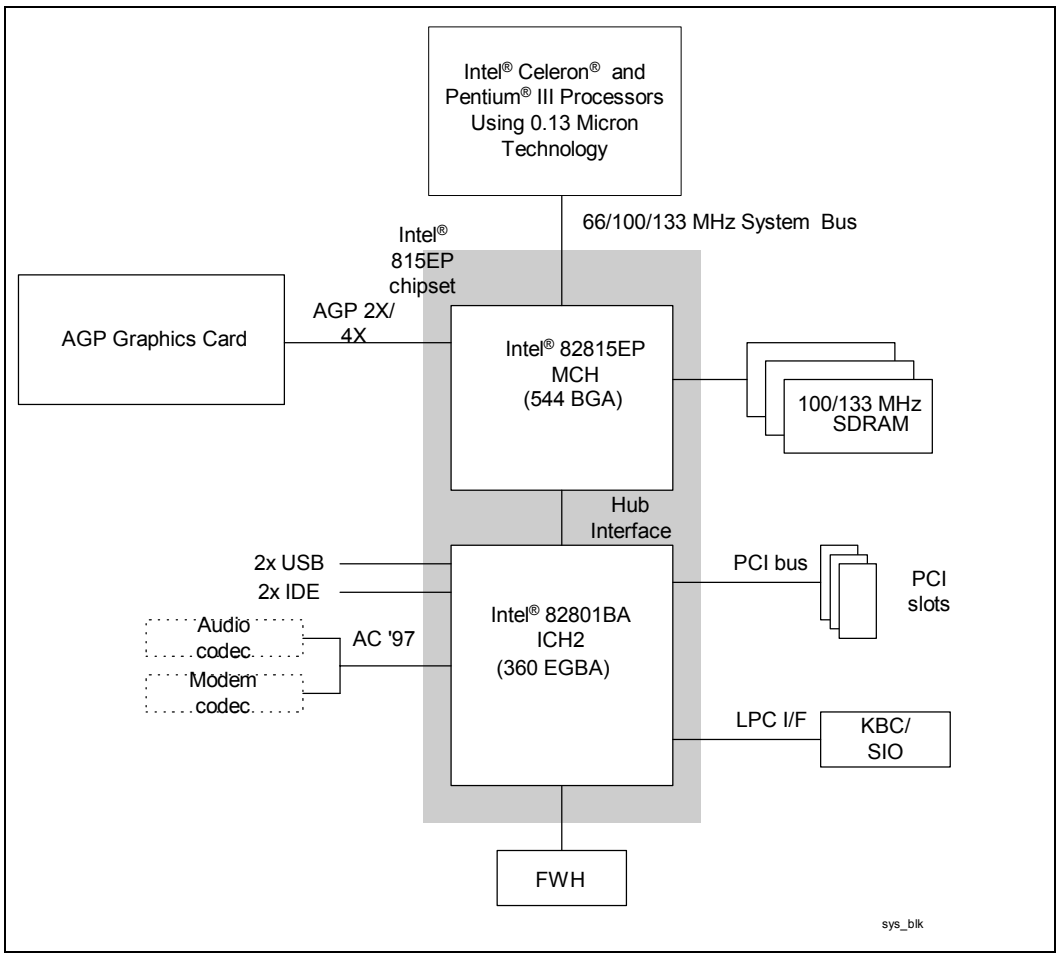
The Accelerated Hub Architecture interface (i.e., the chipset component interconnect) is designed into the chipset to provide an efficient, high-bandwidth communication channel between the MCH and the I/O controller hub. The chipset architecture also enables a security and manageability infrastructure through the Firmware Hub component.

An ACPI-compliant 815EP chipset platform can support the *Full-on (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4),* and *Soft-off (S5)* power management states. The chipset also supports *wake-on-LAN** for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC ’97 allows the OEM to use *software-configurable* AC ’97 audio and modem coder/decoders (codecs), instead of the traditional ISA devices.

1.4.1 System Features

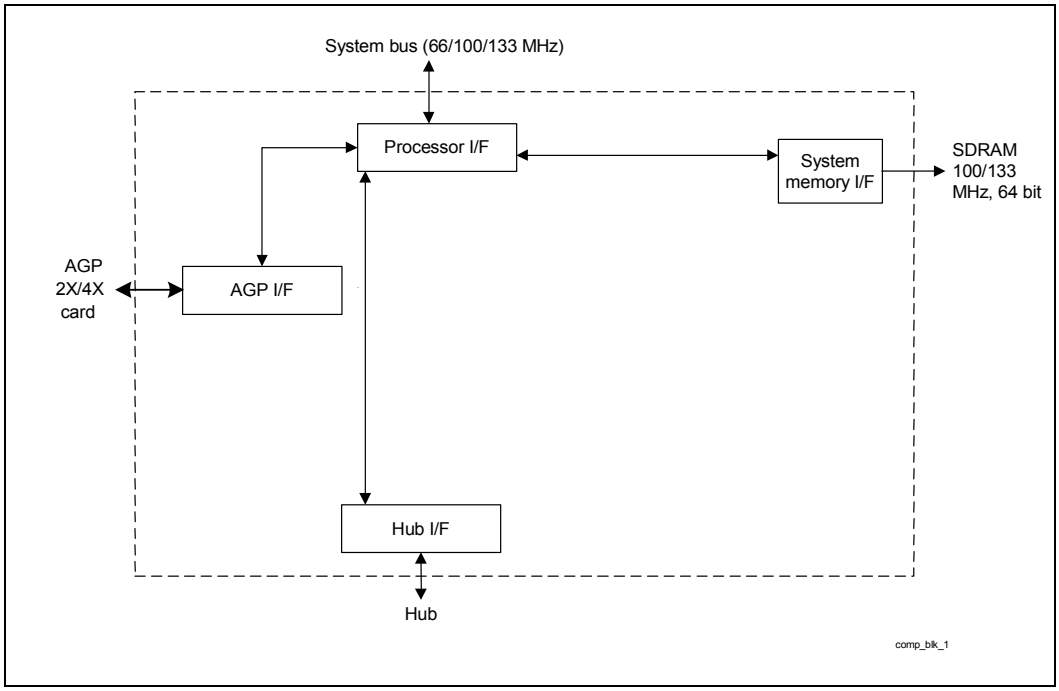
The 815EP chipset platform contains two components: the 82815EP Memory Controller Hub (MCH) and the 82801BA I/O Controller Hub 2 (ICH2). The MCH integrates a 66/100/133 MHz P6 family system bus controller, 100/133 MHz SDRAM controller, and a high-speed accelerated hub architecture interface for communication with the ICH2. The MCH supports an external AGP (2X/4X) discrete graphics card. The ICH2 integrates an UltraATA/100 controller, 2 Universal Serial Bus (USB) host controllers with a total of 4 ports, Low Pin Count (LPC) interface controller, Firmware Hub (FWH) interface controller, PCI interface controller, AC-link, integrated LAN controller, and a hub interface for communication with the MCH.

Figure 1.Intel® 82815EP System Block Diagram



1.4.2 Component Features

Figure 2. 82815EP Component Block Diagram



1.4.2.1 Intel® 82815EP MCH Features

- Processor/System Bus Support
  - Optimized for Celeron and Pentium III processors which use 0.13 micron technology at 133 MHz system bus frequency
  - Support for Celeron and Pentium III processors (CPUID = 068xh) (66 MHz system bus)
  - Supports 32-bit AGTL or AGTL+ bus addressing
  - Supports uniprocessor systems only
  - Utilizes AGTL and AGTL+ bus driver technology (gated AGTL/AGTL+ receivers for reduced power)
- Integrated DRAM controller
  - 32 MB to 512 MB using 16Mb/64Mb/128 Mb technology
  - Supports up to 3 double-sided DIMMS (6 rows)
  - 100 MHz, 133 MHz SDRAM interface
  - 64-bit data interface
  - Standard Synchronous DRAM (SDRAM) support (x-1-1-1 access)
  - Supports only 3.3 V DIMM DRAM configurations
  - No registered DIMM support
  - Support for symmetrical and asymmetrical DRAM addressing
  - Support for x8, x16 DRAM device widths
  - Refresh mechanism: CAS-before-RAS only
  - Support for DIMM serial PD (presence detect) scheme via SMBus interface
  - Suspend-To-RAM (STR) power management support via self-refresh mode using CKE
- Accelerated Graphics Port (AGP) Interface
  - Supports AGP 2.0, including 4X AGP data transfers, but not the 2X/4X Fast Write protocol
  - AGP universal connector support via dual-mode buffers to allow AGP 2.0 3.3 V or 1.5 V signaling
  - 32-deep AGP request queue
  - AGP address translation mechanism with integrated fully associative 20-entry TLB
  - High-priority access support
  - Delayed transaction support for AGP reads that can not be serviced immediately
  - AGP semantic traffic to the DRAM not snooped on system bus and therefore not coherent with processor caches
- Packaging/Power
  - 544 BGA with local memory port
  - 1.85 V core and mixed 3.3 V, 1.5 V, and AGTL, AGTL+ I/O. Note that the 82801BA ICH2 has a 1.8V requirement and the 82815EP MCH has a 1.85 V requirement. Instead of separate voltage regulators to meet these requirements, a single voltage regulator can be set to 1.795 V to 1.910 V. See Figure 101, the Power Delivery Map.

1.4.2.2 Intel® 82815E to 82815EP Signal Name Changes

82815E pins associated with display interface signals, digital video out/TV-out signals, and some clock, power, and ground signals have name changes. Table 1 shows the old 82815E signal name, the ball number, and the new 82815EP signal name. New designs for new 815EP boards should use pull-ups or pull-downs as indicated by the 815EP signal name. 815E boards using 815EP devices may leave the associated 815EP pins in the original 815E configuration.

Table 1. Intel® 82815E to Intel® 82815EP Signal Name Changes

815E Signal Name	Ball#	815EP Signal Name
LTVDATA0	AD16	NC
LTVDATA1	AF17	NC
LTVDATA2	AE17	NC
LTVDATA3	AD17	NC
LTVDATA4	AF18	NC
LTVDATA5	AD18	NC
LTVDATA6	AF20	NC
LTVDATA7	AD20	NC
LTVDATA8	AC20	NC
LTVDATA9	AF21	NC
LTVDATA10	AE21	NC
LTVDATA11	AD21	NC
LTVBLANK#	AB19	NC
TVCLKIN/INT#	AC18	PU1.8
LTVCLKOUT0	AE19	NC
LTVCLKOUT1	AF19	NC
LTVVSYNC	AC16	NC
LTVHSYNC	AB17	NC

815E Signal Name	Ball#	815EP Signal Name
LTVDA	AA20	PU3.3
LTVCK	AB21	PU3.3
DDCK	AB18	PU3.3
DDDA	AA18	PU3.3
DCLKREF	AE24	PD
IWASTE	Y20	CDG
IREF	AD23	PD
VSYNC	AF22	NC
HSYNC	AF23	NC
RED	AD22	NC
GREEN	AE22	NC
BLUE	AE23	NC
LOCLK	R22	NC
LRCLK	P22	PD
VSSDA	Y19	VSS
VSSDACA	AE25	VSS
VCCDA	AA21	VCCDA

Note:

1. NC = No Connect. These pins should float
2. PU3.3 = Pull Up to 3.3 V through a weak pull-up resistor. (8.2 kΩ to 10 kΩ resistor.) Note that these pins in an 815P platform can no longer function as GPIO(x) pins.
3. PD = Pull Down. These pins should be pulled down to ground through a weak pull-down resistor. (8.2 kΩ to 10 kΩ resistor.)
4. VSS = Connect to ground.
5. PU1.8 = Pull Up to 1.8V through a weak pull-up resistor. (8.2 kΩ to 10 kΩ resistor.)
6. VCCDA = VCCDA, VCCDACA1, and VCCDACA2 (using the 815E signal names.) These pins in a new platform designed to use only the 815EP device provide bias to the core voltage. The original 815E VCCDA, VCCDACA1, and VCCDACA2 connections to a VCC1.8 supply must be retained in an 815EP platform.
7. CDG = Connect directly to ground. IWASTE (Ball# Y20) does not require a pull down resistor. Connect this pin directly to ground.

1.4.2.3 82801BA I/O Controller Hub 2 (ICH2)

The Intel® I/O Controller Hub 2 allows the I/O subsystem to access the rest of the system, as follows:

- Upstream accelerated hub architecture interface for access to the MCH
- PCI 2.2 interface (6 PCI Request/Grant pairs)
- 2 channel Ultra ATA/100 Bus Master IDE controller
- USB controller (Expanded capabilities for 4 ports)
- I/O APIC
- SMBus controller
- FWH interface
- LPC interface
- *AC '97 v2.2* interface
- Integrated system management controller
- Alert-on-LAN*
- Integrated LAN controller
- Packaging/Power
  - 360 EBGA
  - 1.8V (± 3% within margins of 1.795 V to 1.9 V) core and 3.3 V standby

1.4.2.4 Firmware Hub (FWH)

The hardware features of the firmware hub include:

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 General Purpose Interrupts (GPI)
- Packaging/Power
  - 40L TSOP and 32L PLCC
  - 3.3 V core and 3.3 V / 12 V for fast programming

1.4.3 Platform Initiatives

1.4.3.1 Universal Motherboard Design

The 815EP chipset platform for use with the universal socket 370 allows systems designers to build one system that is compatible with the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors. When implemented, the 815EP chipset universal socket 370 platform can detect which processor is present in the socket and function accordingly.

1.4.3.2 Intel® PC 133

The PC133 initiative provides the memory bandwidth necessary to obtain high performance from the processor and AGP graphics controller. The platform's SDRAM interface supports 100 MHz

and 133 MHz operation. The latter delivers 1.066 GB/s of theoretical memory bandwidth compared with the 800 MB/s theoretical memory bandwidth of 100 MHz SDRAM systems.

1.4.3.3 Accelerated Hub Architecture Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge becomes significant. With the addition of AC ’97 and Ultra ATA/100, coupled with the existing USB, I/O requirements could impact PCI bus performance. The 815EP platform’s *accelerated hub architecture* ensures that the I/O subsystem, both PCI and the integrated I/O features (IDE, AC ’97, USB, LAN), receives adequate bandwidth. By placing the I/O bridge on the accelerated hub architecture interface instead of PCI, I/O functions integrated into the ICH2 and the PCI peripherals are ensured the bandwidth necessary for peak performance.

1.4.3.4 Internet Streaming SIMD Extensions

The Pentium III processors provide 70 new SIMD (single instruction, multiple data) instructions. The new extensions are floating-point SIMD extensions. Intel® MMX™ technology provides integer SIMD instructions. The Internet Streaming SIMD extensions complement the MMX technology SIMD instructions and provide a performance boost to floating-point-intensive 3D applications.

1.4.3.5 AGP 2.0

The AGP 2.0 interface allows graphics controllers to access main memory at over 1 GB/s, twice the bandwidth of previous AGP platforms. AGP 2.0 provides the infrastructure necessary for *photorealistic 3D.* In conjunction with the Internet Streaming SIMD extensions, AGP 2.0 delivers the next level of 3D graphics performance.

1.4.3.6 Integrated LAN Controller

The 815EP chipset platform incorporates an ICH2 integrated LAN Controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of LAN connect components to target the desired market segment. The 82562EH provides a HomePNA 1 Mbit/sec connection. The 82562ET provides a basic Ethernet 10/100 connection. The 82562EM provides an Ethernet 10/100 connection with the added flexibility of Alert on LAN. More advanced LAN solutions can be implemented with the 82550 or other PCI based product offerings.

1.4.3.7 Ultra ATA/100 Support

The 815EP chipset platform incorporates an IDE controller with two sets of interface signals (primary and secondary) that can be independently enabled, tri-stated or driven low. The component supports Ultra ATA/100, Ultra ATA/66, Ultra ATA/33, and multiword PIO modes for transfers up to 100 MB/sec.

1.4.3.8 Expanded USB Support

The 815EP chipset platform contains two USB Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of 4 USB ports. The addition of a second USB Host Controller expands the functionality of the platform.

1.4.3.9 Manageability and Other Enhancements

The 815EP chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups, without the aid of an external microcontroller.

SMBus

The ICH2 integrates an SMBus controller. The SMBus provides an interface for managing peripherals such as serial presence detection (SPD) and thermal sensors. The slave interface allows an external microcontroller to access system resources.

Interrupt Controller

The interrupt capabilities of the platform expand support for up to 8 PCI interrupt pins and PCI 2.2 message-based interrupts. In addition, the ICH2 supports system bus interrupt delivery.

Firmware Hub (FWH)

The platform supports firmware hub BIOS memory sizes up to 8 MB for increased system flexibility.

1.4.3.10 AC ’97 6-Channel Support

The *Audio Codec ’97 Specification, Revision 2.2* (*AC ’97 v2.2*) Specification defines a digital interface that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and an MC. The *AC ’97 v2.2* defines the interface between the system logic and the audio or modem codec known as the “AC-link.”

The 815EP chipset platform’s AC ’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC-link. Using the platform’s integrated AC-link reduces cost and eases migration from ISA.

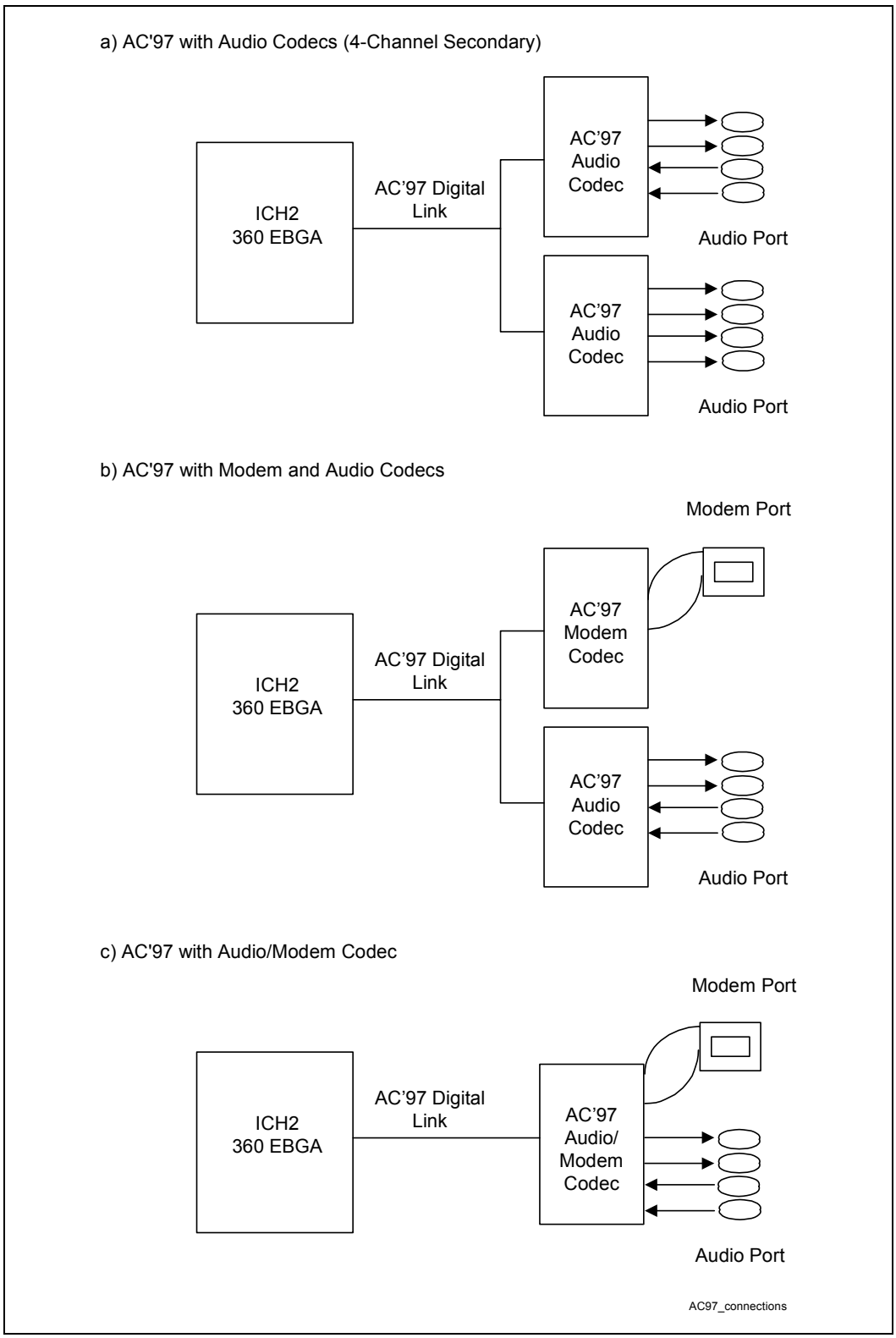
By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC ’97. The 815EP chipset platform’s integrated AC-link allows several external codecs to be connected to the ICH2. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (Figure 3c). The AC-link is expanded to support two audio codecs (Figure 3a) or a combination of an audio and modem codec (Figure 3b).

Modem implementation for different countries must be taken into consideration, as telephone systems may vary. By implementing a split design, the audio codec can be on board, and the modem codec can be placed on a riser. Intel is developing an AC-link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The AC-link in the ICH2 is *AC '97 v2.2* compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high-quality, two-speaker audio solution. Wake-on-ring-from-suspend also is supported with the appropriate modem codec.

The 815EP chipset platform expands audio capability with support for up to six channels of PCM audio output (i.e., full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer, for a complete surround sound effect. ICH2 has expanded support for two audio codecs on the AC-link.

Figure 3. AC '97 Audio and Modem Connections



1.4.3.11 Low-Pin-Count (LPC) Interface

In the 815EP chipset platform, the Super I/O (SIO) component has migrated to the Low-Pin-Count (LPC) interface. Migration to the LPC interface allows for lower-cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended because the AC ’97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of the devices offered and the features supported.

In addition, depending on system requirements, specific system I/O requirements may be integrated into the LPC Super I/O. For example, a USB hub may be integrated to connect to the ICH2 USB output and extend it to multiple USB connectors. Other SIO integration targets include a device bay controller or an ISA-IRQ-to-serial-IRQ converter to support a PCI-to-ISA bridge. Contact your Super I/O vendor to ensure the availability of desired LPC Super I/O features.

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2 General Design Considerations

This design guide provides motherboard layout and routing guidelines for systems based on the 815EP chipset for use with the universal socket 370. The document does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations be completed for each design. Even when the guidelines are followed, critical signals should be simulated to ensure the proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely. Any deviation from these guidelines should be simulated.

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the "nominal" trace impedance for a 5 mil-wide trace. That is, it is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace, based on the switching of neighboring traces. The use of wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

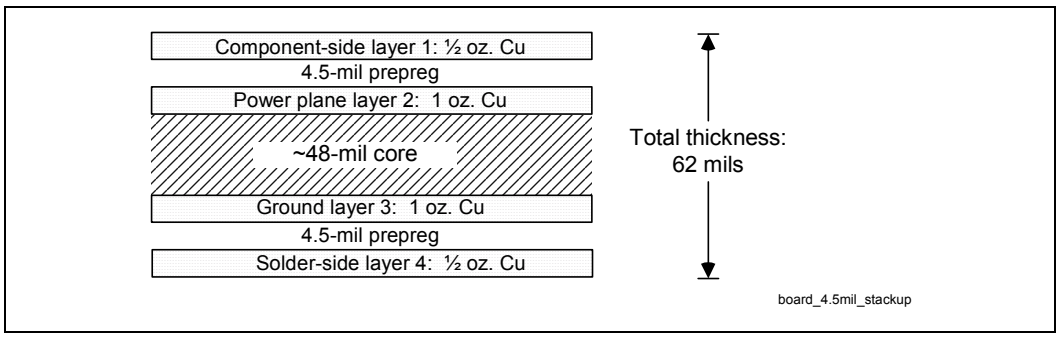
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section.

The routing guidelines in this design guide have been created using a PCB *stack-up* similar to that shown in Figure 4. If this stack-up is NOT used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

2.1 Nominal Board Stack-up

The 815EP chipset platform requires a board stack-up yielding a target impedance of 60 Ω ±15% with a 5 mil nominal trace width. Figure 4 shows an example stack-up that achieves this. It is a 4-layer printed circuit board (PCB) construction using 53%-resin FR4 material.

Figure 4. Board Construction Example for 60 Ω Nominal Stack-up



2.2 Future Designs Require Pull-Ups and Pull-Downs on Any Unused Input and I/O Pins

Any new 815EP platform Universal Socket 370 design should insure no input or I/O pin is left floating. For example, the TVCLKIN/INT# pin on many current 815E designs is left floating. This pin should be pulled up to 1.8V by a weak pull-up resistor (8.2 kΩ to 10 kΩ) on any future 815EP Universal Socket 370 design.

2.3 Support For P-MOS Kicker "ON": SMAA[9] Is Strapped High by an Internal 50 kΩ Pull-Up Resistor

The PSB P-MOS Kicker circuit should be enabled on all new, future 82815EP Universal Socket 370 designs. Use of the P-MOS Kicker circuit improves PSB timings by improving AGTL and AGTL+ signal flight time. The 82815EP SMAA[9] is strapped high through an internal 50 kΩ pull-up resistor to enable the PSB P-MOS Kicker.

Existing 815E designs that have implemented the pull-down resistor circuit on the SMAA[9] signal as shown in the 815 Customer Reference Board schematics and populated the resistor site to over-ride the internal pull-up resistor, may depopulate the site to enable the P-MOS Kicker circuit. This activity should be based on timing analysis of the specific platform.

P-MOS Kicker circuit "ON" is the recommended setting for 82815EP Universal Socket 370 designs using future 0.13 micron technology processors.

2.4 Electrostatic Discharge Platform Recommendations

Electrostatic discharge (ESD) into a system can lead to system instability, and possibly cause functional failures when a system is in use. There are system level design methodologies that when followed can lead to higher ESD immunity. Electromagnetic fields due to ESD are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and cause the system to malfunction. One can reduce the potential for issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in Figures 1-4. In addition, a ground fill cutout should be placed on the Vcc layer in the area where the ground fill is done on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as seen in Figure 2). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100-150 mils apart or less.

In conclusion, Intel recommends the following:

1. Fill the I/O area with the ground fill in all layers including signal layers whenever possible
2. Extend the ground fill along the entire back I/O area
3. Connect the ground fill to mounting holes
4. Place stitching vias 100-150 mils apart in the entire ground fill

Figure 5. Top Signal Layer before the Ground Fill Near the I/O Layer

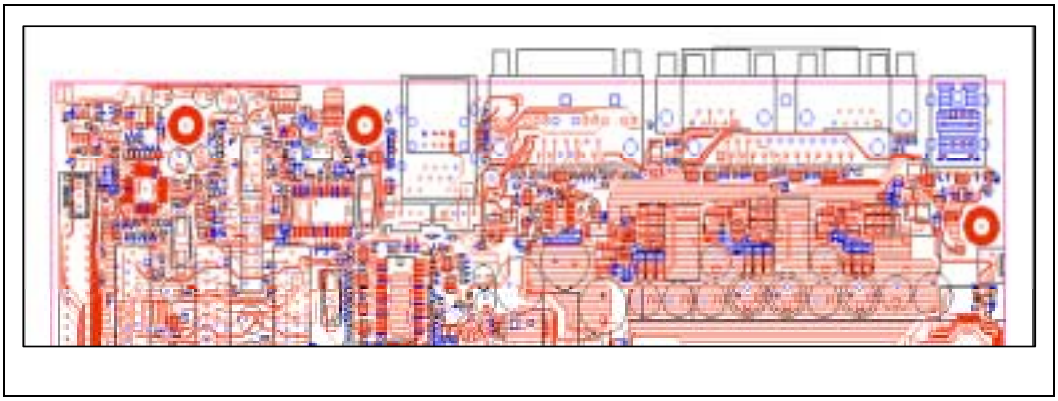


Figure 6. Top Signal Layer after the Ground Fill Near the I/O Layer

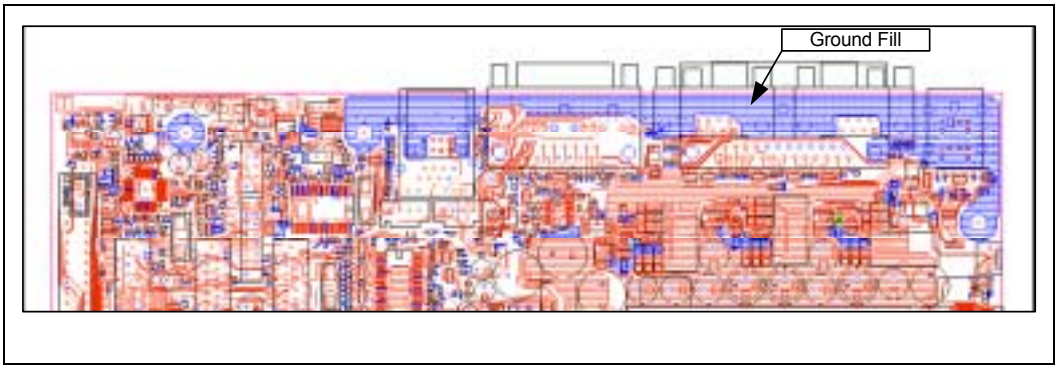


Figure 7. Bottom Signal Layer before the Ground Fill Near the I/O Area

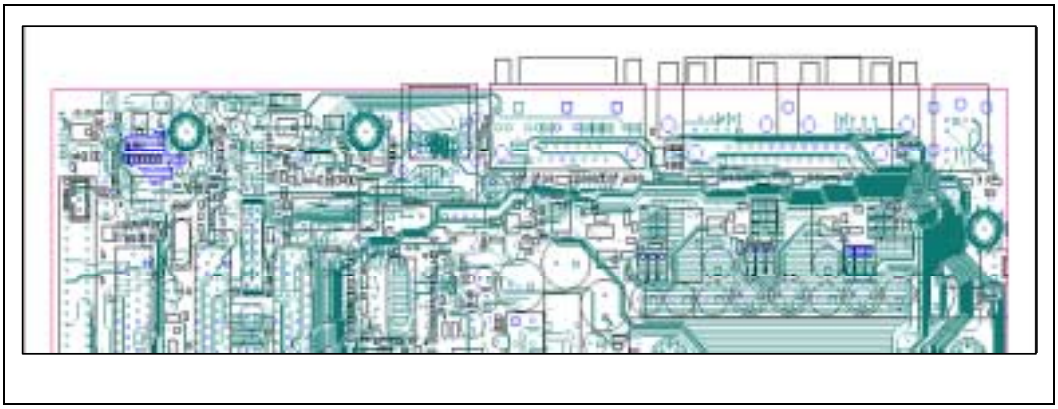
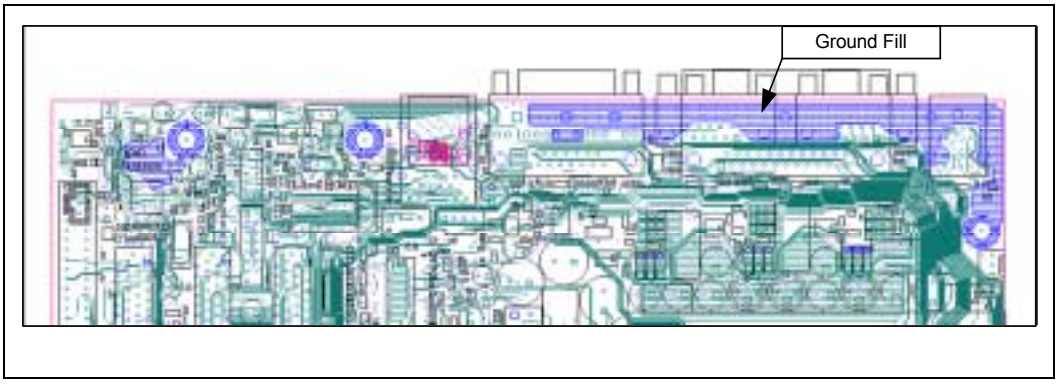


Figure 8. Bottom Signal Layer after the Ground Fill Near the I/O Area



3 Component Layouts

Figure 9 illustrates the relative signal quadrant locations on the MCH ballout. It does not represent the actual ballout. Refer to the *Intel® 82815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH) for use with the Universal Socket 370* Datasheet for the actual ballout.

Figure 9. 82815EP MCH 544-µBGA Quadrant Layout (Top View)

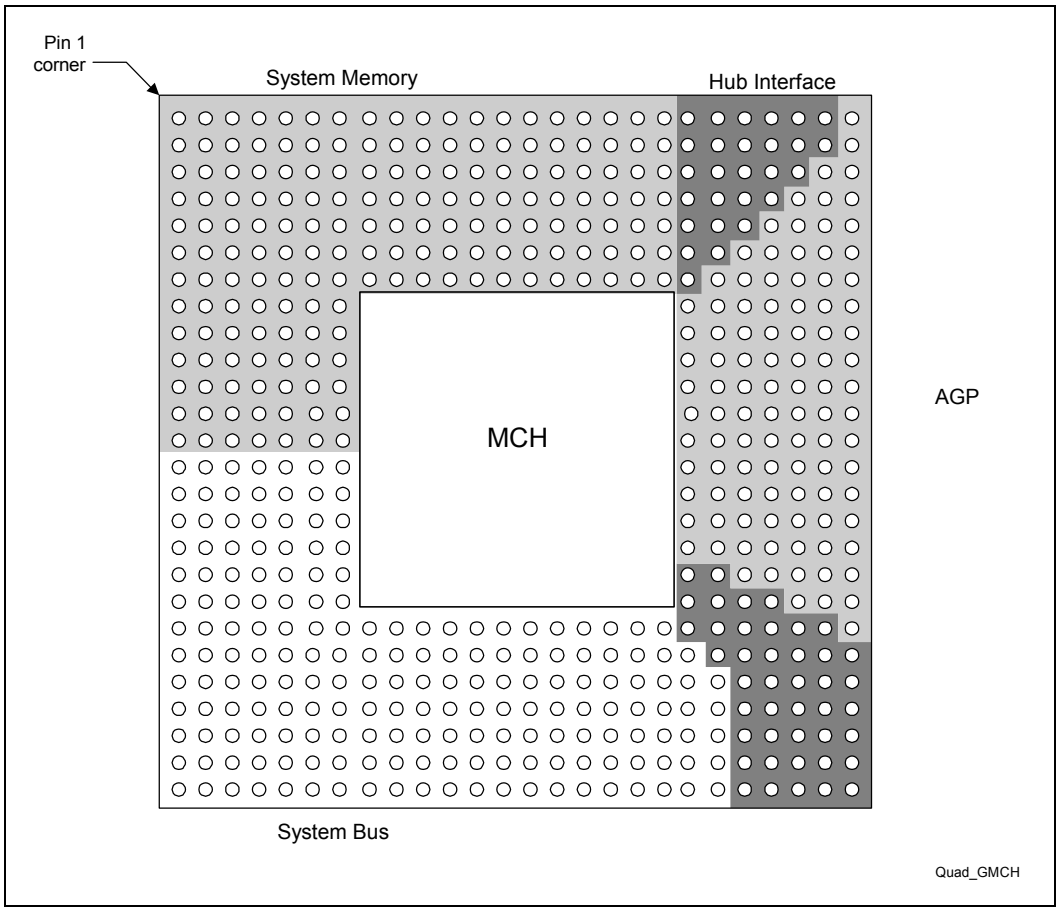


Figure 10 illustrates the relative signal quadrant locations on the ICH2 ballout. It does not represent the actual ballout. Refer to the *Intel® 82801BA I/O Controller Hub (ICH2) and Intel® 82801BAM I/O Controller Hub (ICH2-M)* Datasheet for the actual ballout.

Figure 10. ICH2 360 EBGA Quadrant Layout (Top View)

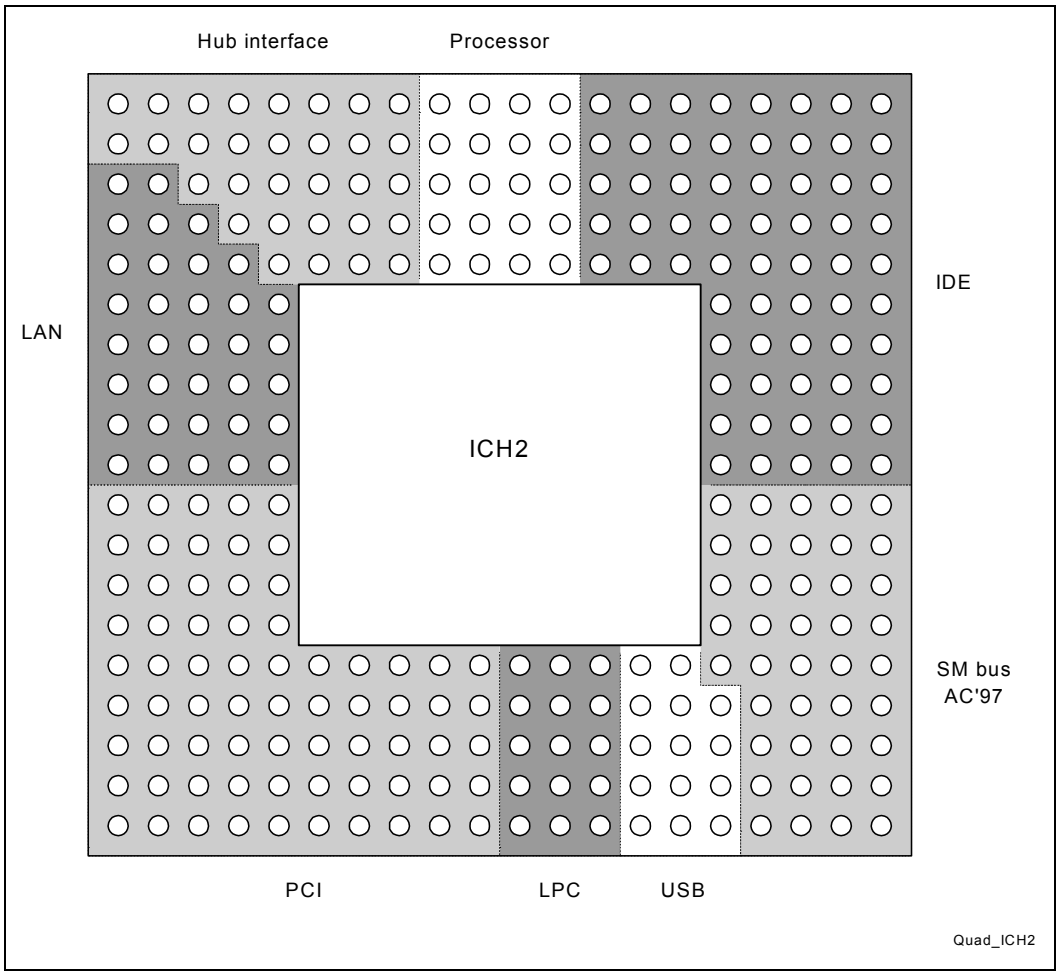
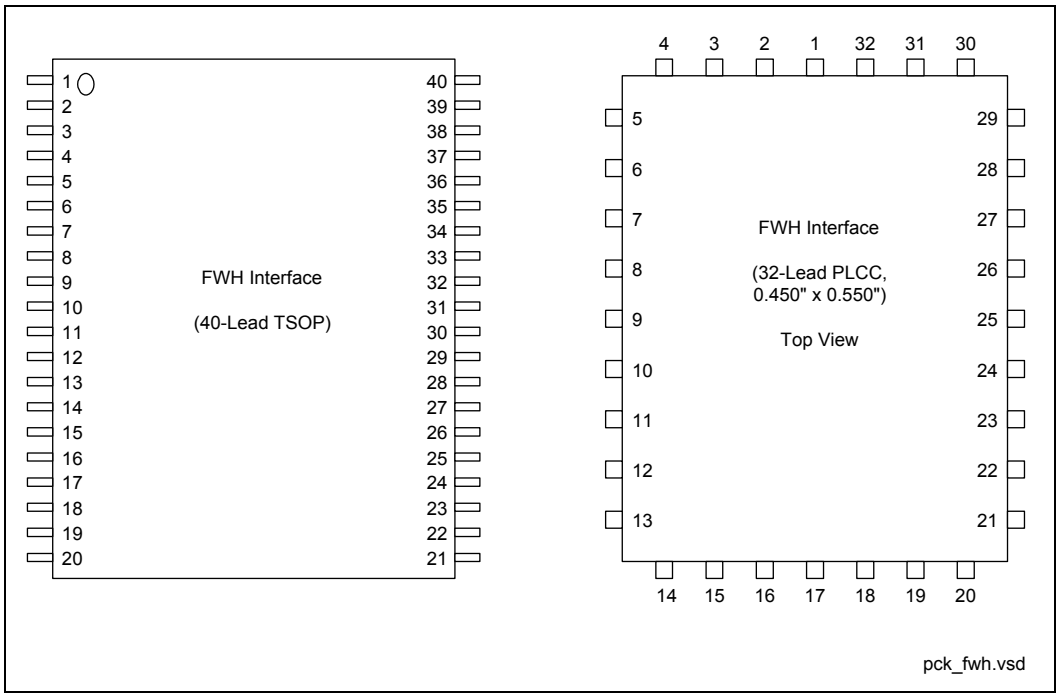


Figure 11. Firmware Hub (FWH) Packages



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4 Universal Socket 370 Design

4.1 Universal Socket 370 Definitions

The universal socket 370 platform supports future Celeron and Pentium III processors which use 0.13 micron technology, as well as Pentium III processors (CPUID=068xh) and Celeron processors (CPUID=068xh). The Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) have different requirements for functioning properly in a platform than the future 0.13 micron socket 370 processors. It is necessary to understand these differences and how they affect the design of the platform. Refer to Table 2 through Table 5 for a high-level description of the differences that require additional circuitry on the motherboard. Specific details on implementing this circuitry are discussed further in this chapter. For a detailed description of the differences between the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processor pins, refer to Section 5.4.

Table 2. Processor Considerations for Universal Socket 370 Design

Signal Name or Pin Number	Function In Intel® Pentium® III Processor (CPUID=068xh) and Intel® Celeron® Processor (CPUID=068xh)	Function In Future 0.13 Micron Socket 370 Processors	Implementation for Universal Socket 370 Design
AF36	VSS	DETECT	Addition of circuitry that generates a processor identification signal used to configure board-level operation.
AG1	VSS	VTT	Addition of FET switch to ground or VTT, controlled by processor identification signal. **Note:** FET must have no more than 100 milliohms resistance between source and drain.
AJ3	VSS	RESET2#	Addition of stuffing option for pull-down to ground, which lets designer prevent future 0.13 micron socket 370 processors from being used with incompatible stepping of 82815EP MCH.
AK22	GTL_REF	VCMOS_REF	Addition of resistor-divider network to provide 1.0 V, which will satisfy voltage tolerance requirements of the Intel® Pentium® III processor (CPUID=068xh) and Intel® Celeron® processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors.
PICCLK	Requires 2.5 V	Requires 2.0 V	Addition of FET switch to provide proper voltage, controlled by processor identification signal.

Signal Name or Pin Number	Function In Intel® Pentium® III Processor (CPUID=068xh) and Intel® Celeron® Processor (CPUID=068xh)	Function In Future 0.13 Micron Socket 370 Processors	Implementation for Universal Socket 370 Design
PWRGOOD	Requires 2.5 V	Requires 1.8V	Addition of resistor-divider network to provide 2.1V, which will satisfy voltage tolerance requirements of the Intel® Pentium® III processor (CPUID=068xh) and Intel® Celeron® processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors.
VTT	Requires 1.5 V	Requires 1.25 V	Modification to VTT generation circuit to switch between 1.5 V or 1.25 V, controlled by processor identification signal.
VTTPWRGD	Not used	Input signal to future 0.13 micron socket 370 processors to indicate that VID signals are stable	Addition of VTTPWRGD generation circuit.

Table 3. MCH Considerations for Universal Socket 370 Design

Pin Name/Number	Issue	Implementation For Universal Socket 370 Design
SMAA[12]	New strap required for determining Intel® Pentium® III Processor (CPUID=068xh) and Intel® Celeron® Processor (CPUID=068xh) or Future 0.13 micron socket 370 processors	Addition of FET switch controlled by processor identification signal.

Table 4. ICH2 Considerations for Universal Socket 370 Design

Signal	Issue	Implementation For Universal Motherboard Design
PWROK	MCH and CK-815 must not sample BSEL[1:0] until VTTPWRGD is asserted. The ICH2 must not initialize before the CK-815 clocks stabilize.	Addition of circuitry to have VTTPWRGD gate PWROK from power supply to ICH2. The ICH2 will hold the MCH in reset until VTTPWRGD asserted plus 20 ms time delay to allow CK-815 clocks to stabilize.

Table 5. Clock Synthesizer Considerations for Universal Socket 370 Design

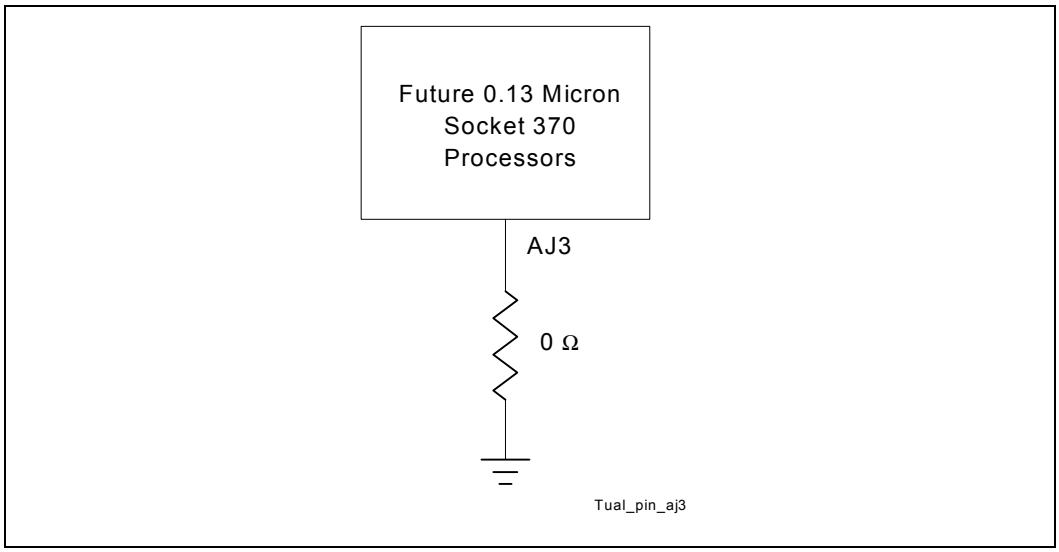
Signal	Issue	Implementation For Universal Motherboard Design
VDD	CK-815 does not support VTTPWRGD	Addition of FET switch that supplies power to VDD only when VTTPWRGD is asserted. **Note:** FET must have no more than 100 milliohms resistance between source and drain.

4.2 Processor Design Requirements

4.2.1 Use of Universal Socket 370 Design With Incompatible MCH

The universal socket 370 design is intended for use with the 815EP chipset platform for use with the universal socket 370. A universal socket 370 design populated with an earlier stepping of the MCH is not compatible with future 0.13 micron socket 370 processors and, if used, will cause eventual failure of these processors. To prevent a future 0.13 micron socket 370 processor from being used with an incompatible stepping of the MCH, the recommendation is to lay out the site for a 0 Ω pull-down to ground on processor pin AJ3. This pin is a RESET# signal on future 0.13 micron socket 370 processors and, by populating the resistor, these future processors will be prevented from functioning when placed in a board with an incompatible stepping of the MCH. All Pentium III (CPUID=068xh) and Celeron (CPUID=068xh) processors will continue to boot normally. Not populating the resistor will allow future 0.13 micron socket 370 processors to boot. Refer to Figure 12 for an example implementation.

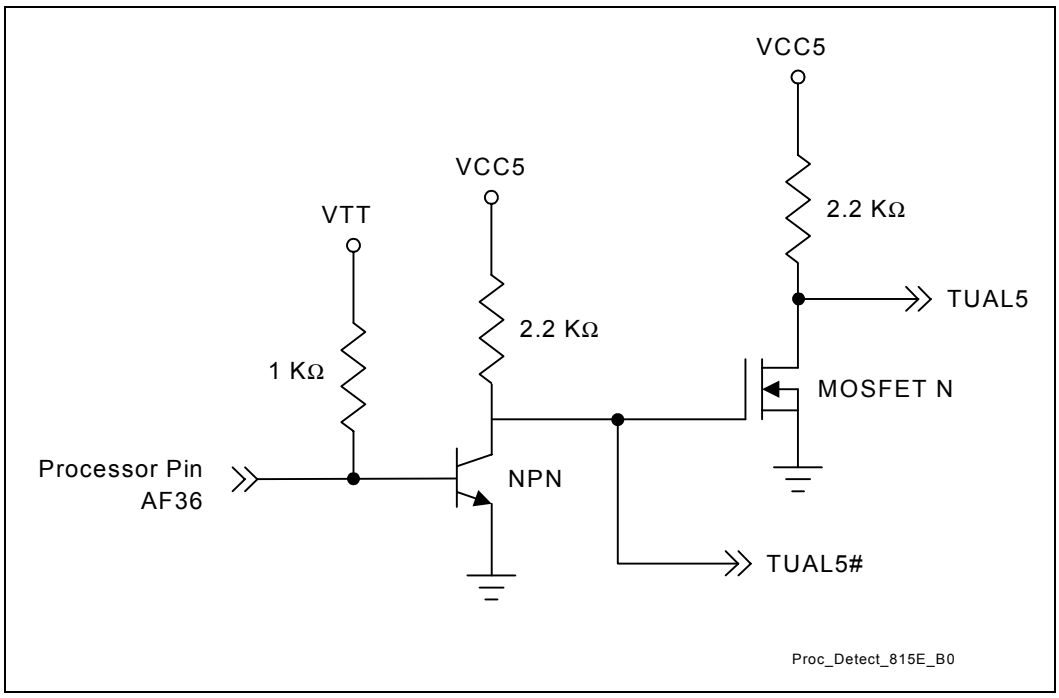
Figure 12. Future 0.13 Micron Socket 370 Processor Safeguard for Universal Motherboard Designs Using A-2 MCH



4.2.2 Identifying the Processor at the Socket

For the platform to configure for the requirements of the processor in the socket, it must first identify whether the processor is a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), or a future 0.13 micron socket 370 processors. Pin AF36 is a VSS pin on an Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh); pin AF36 is an DETECT pin on future 0.13 micron Socket 370 processors. Referring to Figure 13, the platform uses a detect circuit connected to this processor pin. If a future 0.13 micron Socket 370 processor is present in the socket, the TUAL5 reference schematic signal will be pulled to the 5 V rail and the TUAL5# reference schematic signal will be pulled to ground. Otherwise, for a Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh), the TUAL5 reference schematic signal will be pulled to ground and the TUAL5# will be pulled to the 5 V rail.

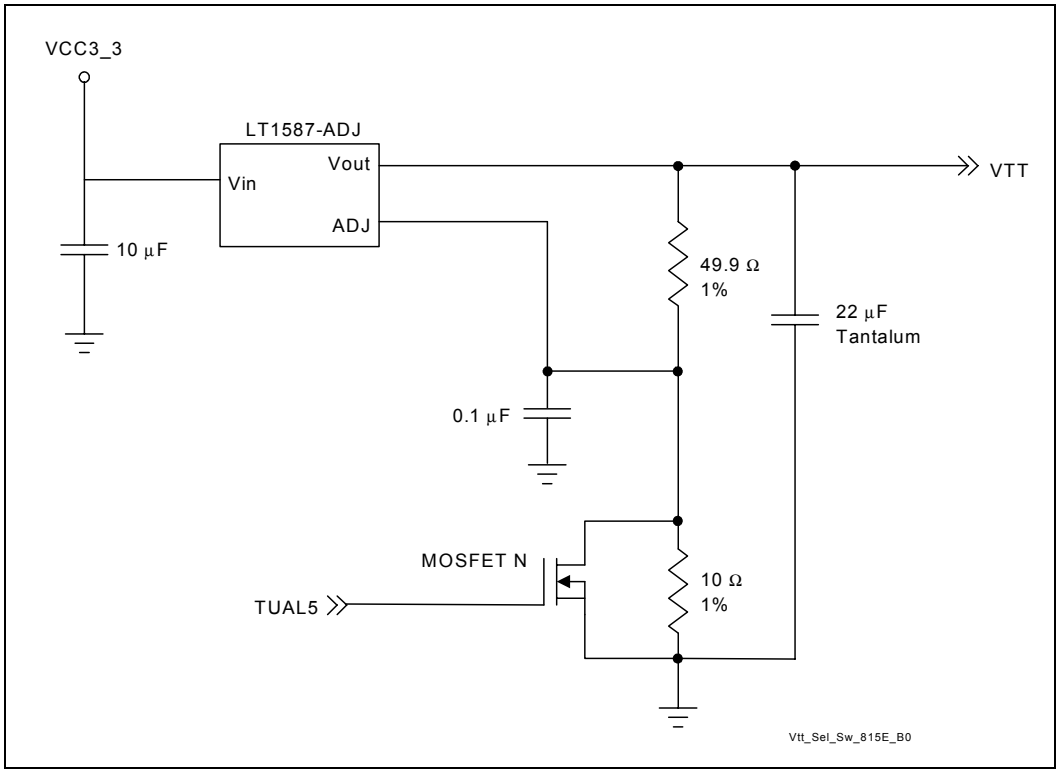
Figure 13. Processor Detect Mechanism at Socket/TUAL5 Generation Circuit



4.2.3 Setting the Appropriate Processor VTT Level

Because the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors require different VTT levels, the platform must be able to provide the appropriate voltage level after determining which processor is in the socket. Referring to Figure 14, the TUAL5 reference schematic signal serves to control the FET, and by doing so determines whether the voltage regulator supplies 1.25 V or 1.5 V to VTT for AGTL or AGTL+, respectively.

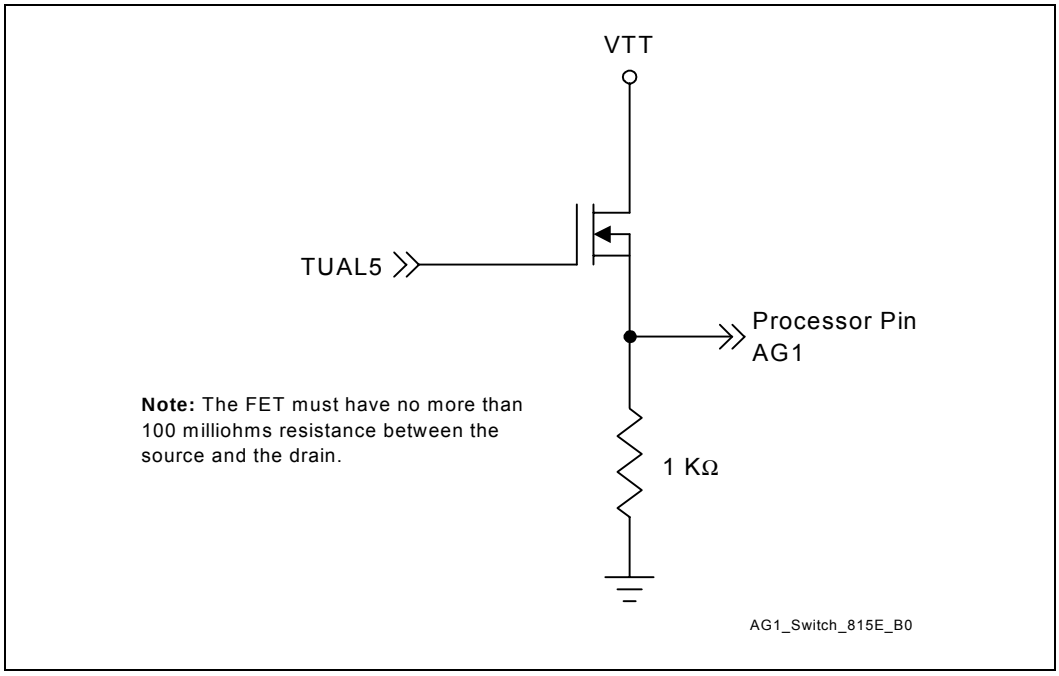
Figure 14. VTT Selection Switch



4.2.4 VTT Processor Pin AG1

Processor pin AG1 requires additional attention since it is a ground pin on a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) and a VTT pin on a future 0.13 micron socket 370 processor. A separate switch controlled by the TUAL5 reference schematic signal determines whether pin AG1 is pulled to ground or VTT. Refer to Figure 15 for an example implementation.

Figure 15. Switching Pin AG1



4.2.5 Identifying the Processor at the MCH

The MCH determines whether the socket contains a future 0.13 micron socket 370 processor or Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) based on the input to pin SMAA12 on the MCH. In a system using future 0.13 micron socket 370 processors, SMAA12 will be pulled down during reset to indicate to the MCH that a future 0.13 micron socket 370 processor is in the socket. Refer to Figure 16. for an implementation example.

Figure 16. Processor Identification Strap on MCH

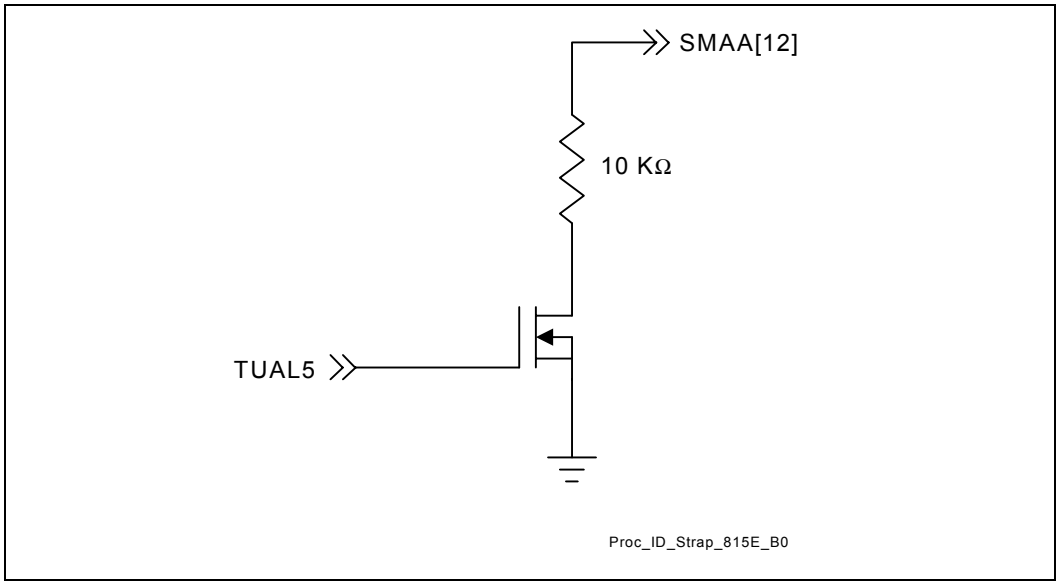


Table 6 provides the logic decoding to determine which processor is installed in a PGA370 design.

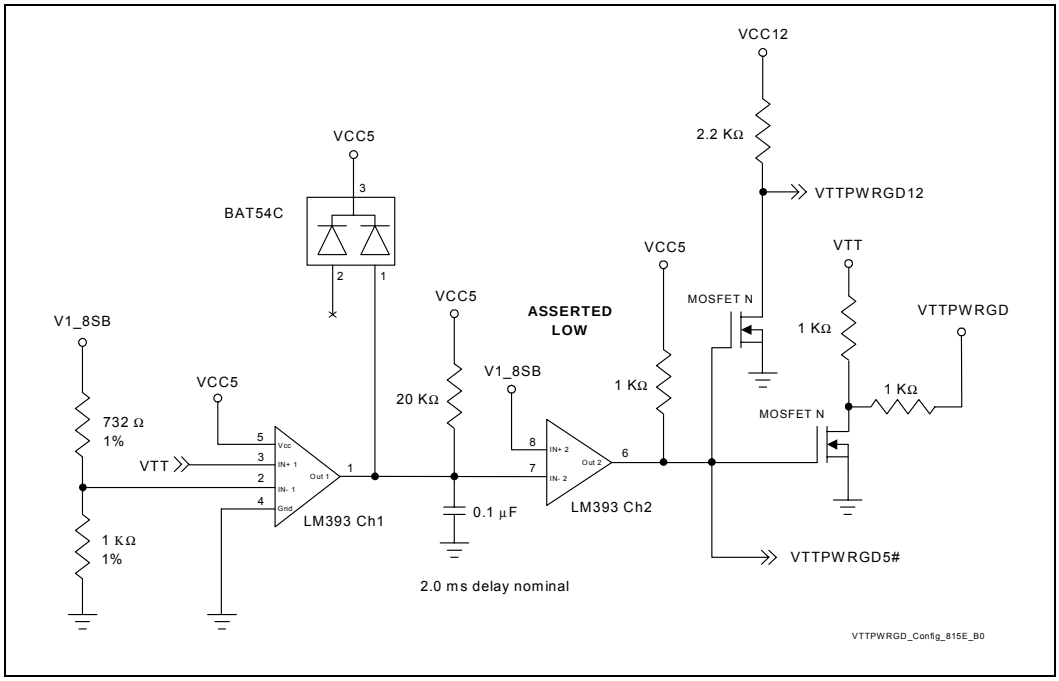
Table 6. Determining the Installed Processor via Hardware Mechanisms

Processor Pin AF36	CPUPRES#	Notes
Hi-Z	0	Future 0.13 micron socket 370 processor installed.
Low	0	Intel® Pentium® III processor (CPUID=068xh) or Intel® Celeron® processor (CPUID=068xh) installed.
X	1	No processor installed.

4.2.6 Configuring Non-VTT Processor Pins

When asserted, the VTTPWGRD signal must be level-shifted to 12 V to properly drive the gating circuitry of the CK-815. Furthermore, while the VTTPWRGD signal is connected to the VTTPWRGD pin on a future 0.13 micron socket 370 processor, on a Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh) that same pin is a ground. To provide proper functionality, a 1.0 kΩ resistor must be placed in series between the circuitry that generates the signal VTTPWRGD and the processor pin VTTPWRGD. Refer to Figure 17 for an example implementation. Voltage regulators that generate the standard VTTPWRGD signal are available.

Figure 17. VTTPWRGD Configuration Circuit

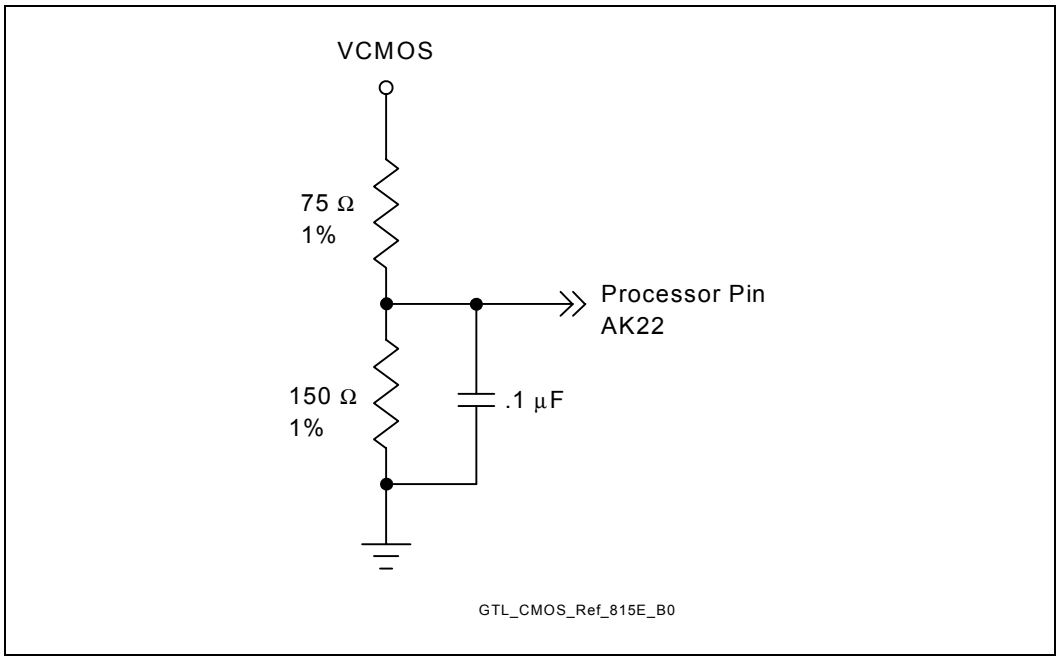


NOTE: the diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20 ms delay.

4.2.7 VCMOS Reference

In previous platforms supporting the Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh), VCMOS was generated by the same power plane as VTT. The future 0.13 micron socket 370 processors do not generate VCMOS, and the universal platform is required to generate this separately on the motherboard. Processor pin AK22, which is a GTL_REF pin on a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh), has been changed to a VCMOS_REF pin on future 0.13 micron socket 370 processors. Referring to Figure 18, a network of resistors and a capacitor must be added so that this pin operates appropriately for whichever processor is in the socket.

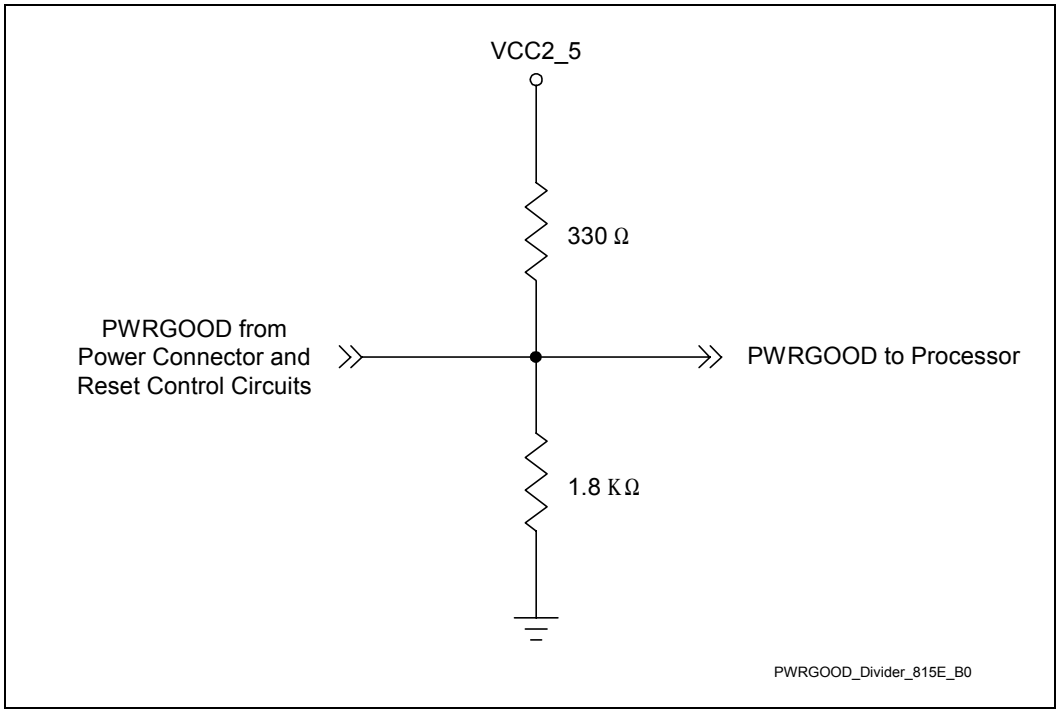
Figure 18. GTL_REF/VCMOS_REF Voltage Divider Network



4.2.8 Processor Signal PWRGOOD

The processor signal PWRGOOD is specified at different voltage levels depending on whether it is an Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), or whether it is a future 0.13 micron socket 370 processor. As there is an overlap between the ranges of accepted voltage levels for these two processor groups, a resistor divider network that provides 2.1V will satisfy the requirements of all supported processors. See Figure 19 for an example implementation.

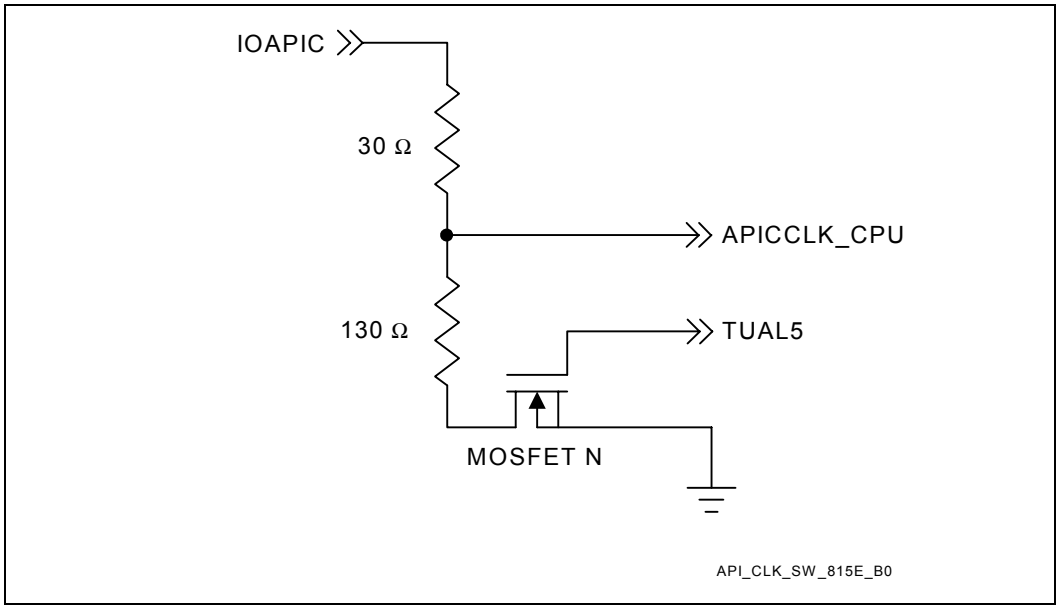
Figure 19. Resistor Divider Network for Processor PWRGOOD



4.2.9 APIC Clock Voltage Switching Requirements

The processor's APIC clock is also specified at different voltage levels depending on whether it is for the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) or whether it is for a future 0.13 micron socket 370 processor. There is no overlap in the range of accepted voltage levels for the two processor groups, so a voltage switch is required to ensure proper operation. Figure 20 shows an example implementation.

Figure 20 Voltage Switch For Processor APIC Clock



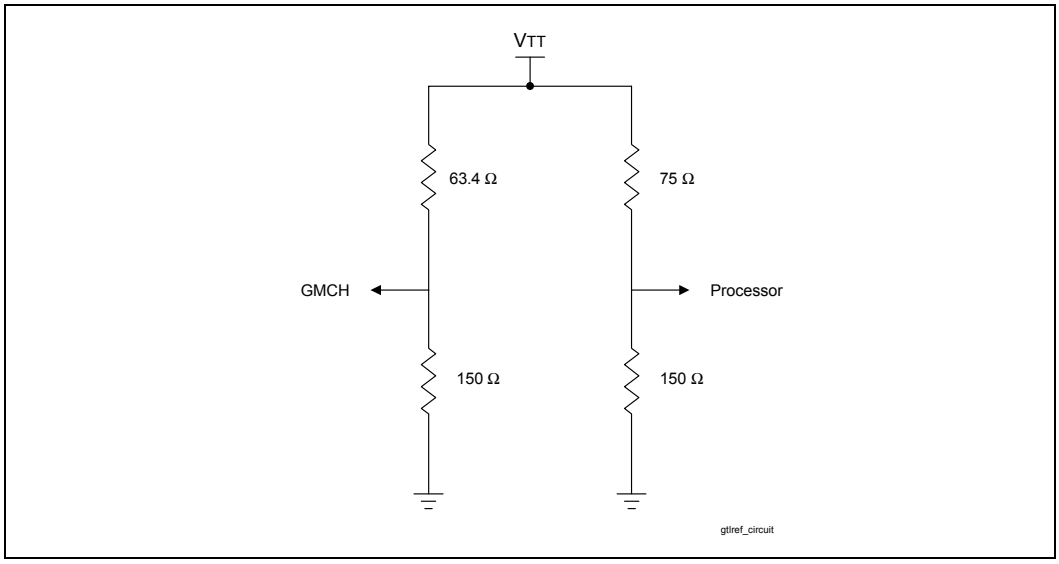
NOTE: The 30 Ω resistor represents the series resistor typically used in connecting the APIC clock to the processor.

4.2.10 GTLREF Topology and Layout

In a platform supporting the future 0.13 micron socket 370 processors, the voltage requirements for GTLREF are different for the processor and the chipset. The GTLREF on the processor is specified to be 2/3 * VTT, while the GTLREF on the chipset is 0.7 * VTT. This difference requires that separate resistor sites be added to the layout to split the GTLREF sources. In a universal motherboard design, a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) will be unaffected by the difference in GTLREF. The recommended GTLREF circuit topology is shown in Figure 21.

Note: If an A-2 stepping of the MCH is used with the universal motherboard design, the GTLREF for the MCH should be set at 2/3 * VTT. This requires changing the 63.4 Ω, 1% resistor on the MCH side to 75 Ω, 1%.

Figure 21. GTLREF Circuit Topology



GTLREF Layout and Routing Guidelines

- Place all resistor sites for GTLREF generation close to the MCH.
- Route GTLREF with as wide a trace as possible.
- Use one 0.1 µF decoupling capacitor for every two GTLREF pins at the processor (four capacitors total). Place as close as possible (within 500 mils) to the Socket 370 GTLREF pins.
- Use one 0.1 µF decoupling capacitor for each of the two GTLREF pins at the MCH (two capacitors total). Place as close as possible to the MCH GTLREF balls.

Given the higher GTLREF level for the MCH, a debug test hook should be added for validation purposes. The debug test hook should be placed on the processor signal ADS# and consists of laying down the site for a 56 Ω pull-up to VTT. The resistor site should be located within 150 mils of the MCH, and placed as close to the ADS# signal trace as possible.

4.3 Power Sequencing on Wake Events

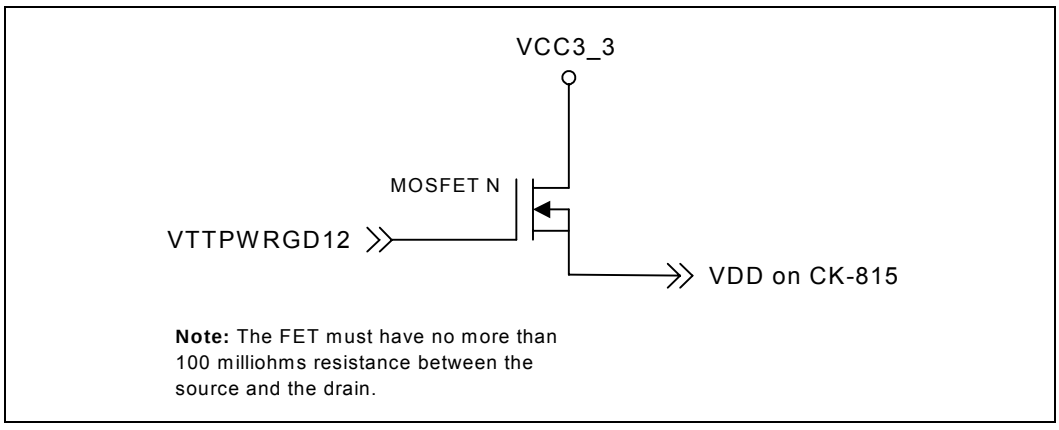
In addition to the mechanism for identifying the processor in the socket, special handling of wake events is required for the 815EP chipset platform that support functionality of the future 0.13 micron socket 370 processors. When a wake event is triggered, the MCH and the CK-815 must not sample BSEL[1:0] until the signal VTTPWRGD is asserted. This is handled by setting up the following sequence of events:

5. Power is not connected to the CK-815-compliant clock driver until VTTPWRGD12 is asserted.
6. Clocks to the ICH2 stabilize before the power supply asserts PWROK to the ICH2. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus it is necessary to gate PWROK to the ICH2 from the power supply while the CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.
7. ICH2 takes the MCH out of reset.
8. MCH samples BSEL[1:0]. CK-815 will have sampled BSEL[1:0] much earlier.

4.3.1 Gating of CK-815 to VTTPWRGD

System designers must ensure that the VTTPWRGD signal is asserted before the CK-815-compliant clock driver receives power. This is handled by having the 3.3 V rail of the clock driver gated by the VTTPWRGD12 reference schematic signal. Unlike previous 815EP chipset designs, the 3.3 V standby rail is not used to power the clock because the VTTPWRGD12 reference schematic signal will cut power to the clock when going into any sleep state. Refer to Figure 22 for an example implementation.

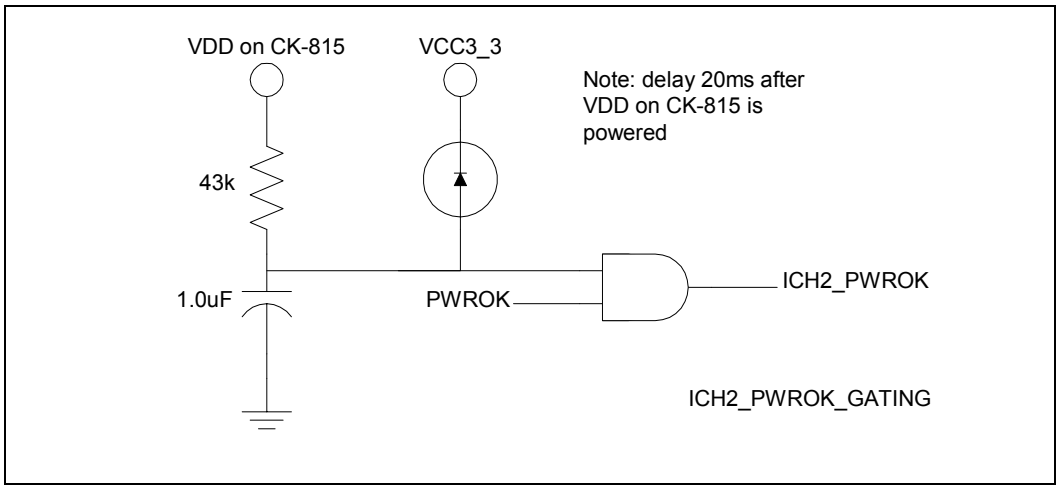
Figure 22. Gating Power to CK-815



4.3.2 Gating of PWROK to ICH2

With power being gated to the CK-815 by the signal VTTPWRGD12, it is important that the clocks to the ICH2 are stable before the power supply asserts PWROK to the ICH2. As the clocking power gating circuitry relies on the 12 V supply, there is no guarantee that these conditions will be met. This is why an estimated minimum time delay of 20 ms must be added after power is connected to the CK-815 to give the clock driver sufficient time to stabilize. This time delay will gate the power supply's assertion of PWROK to the ICH2. After the time delay, the power supply can safely assert PWROK to the ICH2, with the ICH2 subsequently taking the MCH out of reset. Refer to Figure 23 for an example implementation.

Figure 23 PWROK Gating Circuit For ICH2



NOTE: The diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20ms delay.

5 System Bus Design Guidelines

The Pentium III processor delivers higher performance by integrating the Level 2 cache into the processor and running it at the processor's core speed. The Pentium III processor runs at higher core and system bus speeds than previous-generation IA-32 processors while maintaining hardware and software compatibility with earlier Pentium III processors. The new Flip Chip-Pin Grid Array 2 (FC-PGA2) package technology enables compatibility with previous Flip Chip-Pin Grid Array (FC-PGA) packages using the PGA370 socket.

This section presents the considerations for designs capable of using the 815EP universal platform with the full range of Pentium III processors using the PGA370 socket.

5.1 System Bus Routing Guidelines

The following layout guide supports designs using Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors with the 815 chipset platform. The solution covers system bus speeds of 66/100/133 MHz for the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors. All processors must also be configured to 56 Ω on-die termination.

5.1.1 Initial Timing Analysis

Table 7 lists the AGTL/AGTL+ component timings of the processors and 815EP universal platform's MCH defined at the pins.

Note: **These timings are for reference only.** Obtain each processor's specifications from the respective processor datasheet and the chipset values from the appropriate 815 chipset datasheet.

Table 7. Intel® Pentium® III Processor AGTL/AGTL+ Parameters for Example Calculations

IC Parameters	Intel® Pentium® III Processor at 133 MHz System Bus	MCH	Notes
Clock to Output maximum (T_{CO_MAX})	3.25 ns (for 66/100/133 MHz system bus speeds)	4.1 ns	1, 2
Clock to Output minimum (T_{CO_MIN})	0.40 ns (for 66/100/133 MHz system bus)	1.05 ns	1, 2
Setup time (T_{SU_MIN})	1.20 ns for BREQ Lines 0.95 ns for all other AGTL/AGTL+ Lines @ 133 MHz 1.20 ns for all other AGTL/AGTL+ Lines @ 66/100 MHz	2.65 ns	1, 2,3
Hold time (T_{HOLD})	1.0 ns (for 66/100/133 MHz system bus speeds)	0.10 ns	1

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only**. These timing parameters are subject to change. Check the appropriate component documentation for the valid timing parameter values.
3. T_{SU_MIN} = 2.65 ns assumes that the MCH sees a minimum edge rate equal to 0.3 V/ns.

Table 8 contains an example AGTL+ initial maximum flight time, and Table 9 contains an example minimum flight time calculation for a 133 MHz, uniprocessor system using the Pentium III processor and the 815EP chipset platform's system bus. Note that assumed values were used for the clock skew and clock jitter.

Note: The clock skew and clock jitter values depend on the clock components and the distribution method chosen for a particular design, and must be budgeted into the initial timing equations as appropriate for each design.

Table 8 and Table 9 were derived assuming the following:

- CLK_{SKEW} = 0.20 ns (Note: This assumes that the clock driver pin-to-pin skew is reduced to 50 ps by tying the two host clock outputs together (i.e., "ganging") at the clock driver output pins, and that the PCB clock routing skew is 150 ps. The system timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together as well as the use of a clock driver that meets the CK-815 Clock Synthesizer/Driver Specification.)
- CLK_{JITTER} = 0.250 ns

See the respective processor datasheet and the appropriate 815EP chipset platform documentation for details on clock skew and jitter specifications. Exact details regarding the host clock routing topology are provided with the platform design guideline.

Table 8. Example T_{FLT_MAX} Calculations for 133 MHz Bus

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}
Processor	MCH	7.50	3.25	2.65	0.20	0.25	0.40	1.1
MCH	Processor	7.50	4.1	1.20	0.20	0.25	0.40	1.35

NOTES:
1. All times in nanoseconds
2. BCLK period = 7.50 ns @ 133.33 MHz

Table 9. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	THOLD	ClkSKEW	TCO_MIN	Recommended TFLT_MIN
Processor	MCH	0.10	0.20	0.40	0.10
MCH	Processor	1.00	0.20	1.05	0.15

NOTE: All times in nanoseconds

The flight times in Table 8 include margin to account for the following phenomena that Intel observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect the flight time and signal quality and sometimes are not accounted for during simulation. Accordingly, the maximum flight times depend on the baseboard design, and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in
- Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay
- Crosstalk on the PCB and inside the package which can cause variation in the signals

Additional effects exist that **may not necessarily** be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. These effects are included as M_{ADJ} in the example calculations in Table 8. Examples include:

- The effective board propagation constant (SEFF), which is a function of:
  - Dielectric constant (ε_r) of the PCB material
  - Type of trace connecting the components (stripline or microstrip)
  - Length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time, **but not necessarily equal to** the flight time.

5.2 General Topology and Layout Guidelines

Figure 24. Topology for 370-Pin Socket Designs with Single-Ended Termination (SET)

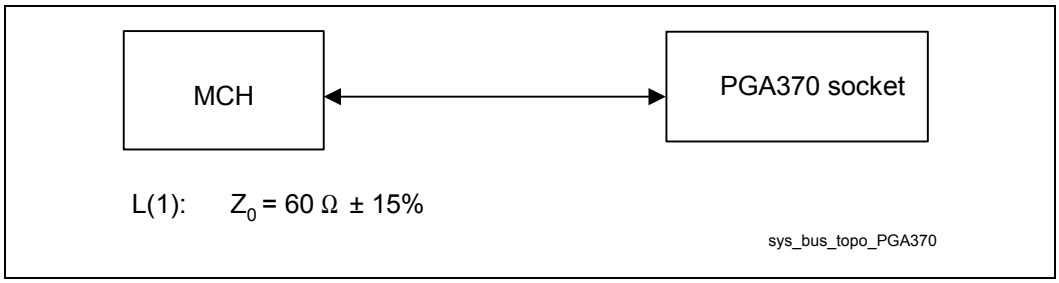


Table 10. Trace Guidelines for Figure 24 [1, 2, 3]

Description	Min. Length (inches)	Max. Length (inches)
MCH to PGA370 socket trace	1.90	4.50

NOTES:
1. All AGTL/AGTL+ bus signals should be referenced to the ground plane for the entire route.
2. Use an intragroup AGTL/AGTL+ spacing : line width : dielectric thickness ratio of at least 2:1:1 for microstrip geometry. If ε_r = 4.5, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10 mil spacing, 5 mil traces, and a 5 mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
3. The recommended trace width is 5 mils, but not greater than 6 mils.

Table 11 contains the trace width : space ratios assumed for this topology. Three types of crosstalk are considered in this guideline: Intragroup AGTL/AGTL+, Intergroup AGTL/AGTL+, and AGTL/AGTL+ to non-AGTL/AGTL+. Intragroup AGTL/AGTL+ crosstalk involves interference between AGTL/AGTL+ signals within the same group. Intergroup AGTL/AGTL+ crosstalk involves interference from AGTL/AGTL+ signals in a particular group to AGTL/AGTL+ signals in a different group. An example of AGTL/AGTL+ to non-AGTL/AGTL+ crosstalk is when CMOS and AGTL/AGTL+ signals interfere with each other. The AGTL/AGTL+ signals consist of the following groups: data signals, control signals, clock signals, and address signals.

Table 11. Trace Width:Space Guidelines

Crosstalk Type	Trace Width:Space Ratios[1, 2]
Intragroup AGTL/AGTL+ signals (same group AGTL/AGTL+)	5:10 or 6:12
Intergroup AGTL/AGTL+ signals (different group AGTL/AGTL+)	5:15 or 6:18
AGTL/AGTL+ to System Memory Signals	5:30 or 6:36
AGTL/AGTL+ to non-AGTL/AGTL+	5:25 or 6:24

NOTES:
1. Edge-to-edge spacing.
2. Units are in mils.

5.2.1 Motherboard Layout Rules for AGTL/AGTL+ Signals

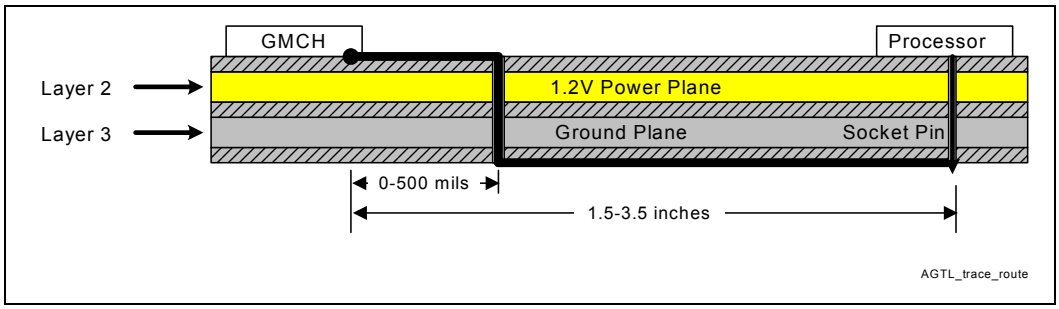
Ground Reference

It is strongly recommended that AGTL/AGTL+ signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide an effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane. If a signal has to go through routing layers, the recommendations are:

Note: Following these layout rules is critical for AGTL/AGTL+ signal integrity, particularly for 0.18 micron and smaller process technology.

- For signals going from a ground reference to a power reference, add capacitors between ground and power near the vias to provide an AC return path. One capacitor should be used for every three signal lines that change reference layers. Capacitor requirements are as follows: C=100nF, ESR=80mΩ, ESL=0.6nH. Refer to Figure 25 for an example of switching reference layers.
- For signals going from one ground reference to another, separate ground reference, add vias between the two ground planes to provide a better return path.

Figure 25. AGTL/AGTL+ Trace Routing



Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance.

Processor Connector Breakout

It is strongly recommended that AGTL/AGTL+ signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the connector on the same layer. If routing is tight, break out from the connector on the opposite routing layer over a ground reference and cross over to main signal layer near the processor connector.

Minimizing Crosstalk

The following general rules minimize the impact of crosstalk in a high-speed AGTL/AGTL+ bus design:

- Maximize the space between traces. Where possible, maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges. It may be necessary to use tighter spacing when routing between component pins. When traces must be close and parallel to each other, minimize the distance that they are close together and maximize the distance between the sections when the spacing restrictions are relaxed.
- Avoid parallelism between signals on adjacent layers, if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL/AGTL+ is a low-signal-swing technology, it is important to isolate AGTL/AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings (e.g., 5 V PCI).
- AGTL/AGTL+ signals must be well isolated from system memory signals. AGTL/AGTL+ signal trace edges must be at least 30 mils from system memory trace edges within 100 mils of the ball of the 82815EP MCH.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL/AGTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes crosstalk.
- Route AGTL/AGTL+ address, data, and control signals in separate groups to minimize crosstalk between groups. Keep at least 15 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross-sectional area of the traces. This can be done by means of narrower traces and/or by using thinner copper, but the trade-off for this smaller cross-sectional area is higher trace resistivity, which can reduce the falling-edge noise margin because of the I*R loss along the trace.

5.2.2 Motherboard Layout Rules for Non-AGTL/AGTL+ (CMOS) Signals

Table 12. Routing Guidelines for Non-AGTL/AGTL+ Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 9”
FERR#	5 mils	10 mils	1” to 9”
FLUSH#	5 mils	10 mils	1” to 9”
IERR#	5 mils	10 mils	1” to 9”
IGNNE#	5 mils	10 mils	1” to 9”

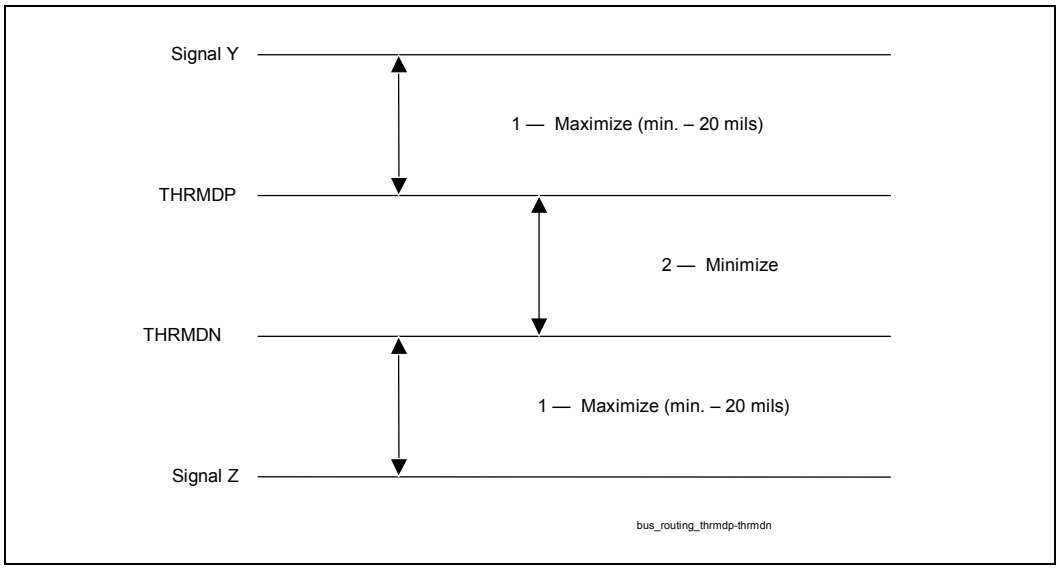
INIT#	5 mils	10 mils	1” to 9”
LINT[0] (INTR)	5 mils	10 mils	1” to 9”
LINT[1] (NMI)	5 mils	10 mils	1” to 9”
PICD[1:0]	5 mils	10 mils	1” to 9”
PREQ#	5 mils	10 mils	1” to 9”
PWRGOOD	5 mils	10 mils	1” to 9”
SLP#	5 mils	10 mils	1” to 9”
SMI#	5 mils	10 mils	1” to 9”
STPCLK	5 mils	10 mils	1” to 9”
THERMTRIP#	5 mils	10 mils	1” to 9”

NOTE: Route these signals on any layer or combination of layers.

5.2.3 THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor’s thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance.

Figure 26. Routing for THRMDP and THRMDN



NOTES:
1. Route these traces parallel and equalize lengths within ±0.5 inch.
2. Route THRMDP and THRMDN on the same layer.

5.2.4 Additional Routing and Placement Considerations

- Distribute VTT with a wide trace. A 0.050 inch minimum trace is recommended to minimize DC losses. Route the VTT trace to all components on the host bus. Be sure to include decoupling capacitors.
- The VTT voltage should be 1.5 V ± 3% for static conditions, and 1.5 V ± 9% for worst-case transient conditions when the Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh) is present in the socket. If a future 0.13 micron socket 370 processor is being used, the VTT voltage should then be 1.25 V ± 3% for static conditions, and 1.25 V ± 9% for worst-case transient conditions.
- Place resistor divider pairs for VREF generation at the MCH component. VREF also is delivered to the processor.

5.3 Electrical Differences for Universal PGA370 Designs

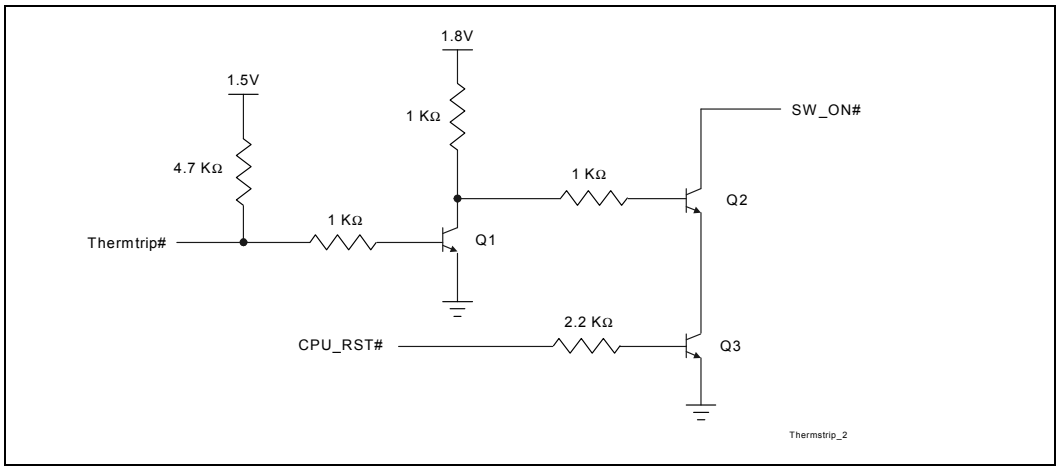
There are several electrical changes between previous PGA370 designs and the *universal PGA370* design, as follows:

- Changes to the PGA370 socket pin definitions.
- Addition of VTTPWRGD signal to ensure stable VID selection for future 0.13 micron socket 370 processors.
- Addition of THERMTRIP circuit to allow processor to detect catastrophic overheat.
- Addition of VID[25mV] signal to support future 0.13 micron socket 370 processors.
- Processor VTT level is switchable to 1.25 V or 1.5 V, depending on which processor is present in the socket.
- In designs using future 0.13 micron socket 370 processors, the processor does not generate V_{CMOS}_REF.

5.3.1 THERMTRIP Circuit

To ensure that the processor detects and prevents catastrophic overheat, THERMTRIP is required on all designs that support future 0.13 micron socket 370 processors. Figure 27 offers one possible implementation that makes use of the 4s Power Button feature on the ICH2.

Figure 27. Example Implementation of THERMTRIP Circuit



NOTES:

1. The pull-up voltage on the collector of Q1 is required to be 1.8V derived from a 3.3 V source.
2. THERMTRIP is not valid until after CPU_RST# is deasserted. This is handled by gating the assertion of THERMTRIP with CPU_RST#. Using the CPU_RST# in this manner has minimal impact to the signal quality.
3. THERMTRIP must not go higher than VccCMOS levels. The pull-up on THERMTRIP is now connected to 1.5 V.
4. CPU_RST# must gate SW_ON# from ground. This prevents glitching on SW_ON# during power-up and power-down.
5. The resistance to the base of the transistor gating CPU_RST# must be at least 2.2 KΩ for proper Vih levels on CPU_RST#.

5.3.1.1 THERMTRIP Timing

When the THERMTRIP signal is asserted, both the VCC and VTT supplies to the processor must be turned off to prevent thermal runaway of the processor. The time required from THERMTRIP asserted to VCC rail at ½ nominal is 5 s, and THERMTRIP asserted to VTT rail at ½ nominal is 5 s. System designers must ensure that the decoupling scheme used on these rails does not violate the THERMTRIP timing specifications.

5.3.1.2 THERMTRIP Support For 0.13 Micron Technology Processors, A-1 Stepping

A platform supporting the 0.13 micron technology processor must implement a workaround required for the A-1 stepping of that processor, identified by CPUID = 6B1h. The internal control register bit responsible for operation of the THERMTRIP circuit functionality may power up in an un-initialized state. As a result, THERMTRIP# may be incorrectly asserted during de-assertion of RESET# at nominal operating temperatures. When THERMTRIP# is asserted as a result of this, the processor may shut down internally and stop execution. In addition, when the THERMTRIP# pin is asserted the processor may incorrectly continue to execute, leading to intermittent system power-on boot failures. The occurrence and repeatability of failures is system dependent, however, all systems and processors are susceptible to failure.

To prevent the risk of power-on boot failures, a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:

•Rising edge occurs after Vcc_core is valid and stable

•Rising edge occurs before or at the de-assertion of RESET#

•Rising edge occurs after all Vref input signals are at valid voltage levels

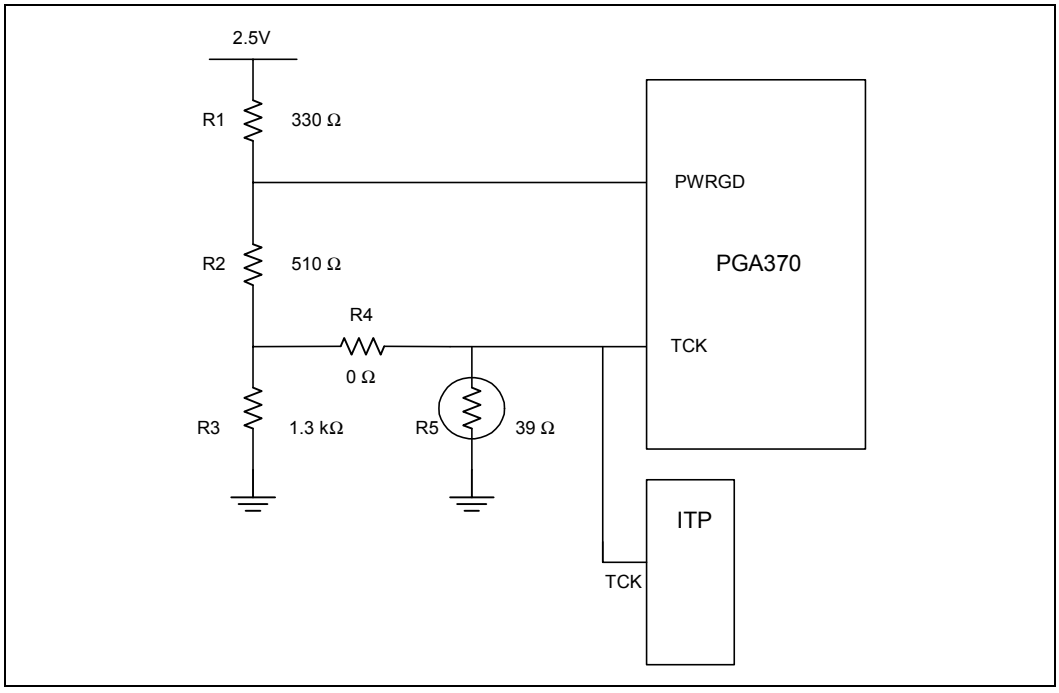
•TCK input meets the Vih min (1.3 V) and max (1.65 V) spec requirements

Specific workaround implementations may be platform specific. The following examples have been tested as acceptable workaround implementations.

Note: the example workaround circuits shown in Figure 28 require circuit modification for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Review the accompanying notes with each workaround for ITP modification details. If the system fails to boot when using ITP, issuing the ITP 'Reset Target' command on failing systems will reset the system and provide a sufficient rising edge on the TCK pin to ensure proper system boot.

In addition, the example workaround circuits shown below do not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround solutions must be found if such test capability is required.

Figure 28. THERMTRIP Support for A-1 Stepping 0.13 Micron Technology Celeron® Processors



NOTES: 1. For Production Boards: Depopulate Resistor R5.

2. To Use ITP: Install Resistor R5 and Depopulate Resistor R4.

5.4 PGA370 Socket Definition Details

Table 13 compares the pin names and functions of the Intel processors supported in the 815EP universal platform.

Table 13. Processor Pin Definition Comparison

Pin #	Pin Name Intel® Celeron® Processor (CPUID=068xh)	Pin Name Intel® Pentium® III Processor (CPUID=068xh)	Pin Name Future 0.13 Micron Socket 370 Processors	Function
AA33	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AA35	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AB36	VCC_{CMOS}	VCC_{CMOS}	VTT	• CMOS voltage level for Intel® Pentium® III processor (CPUID=068xh) and Intel® Celeron® processor (CPUID=068xh). • AGTL termination voltage for future 0.13 micron socket 370 processors.
AD36	VCC1.5	VCC1.5	VTT	• VCC1.5 for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • VTT for future 0.13 micron socket 370 processors.
AF36	VSS	VSS	DETECT	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • DETECT for future 0.13 micron socket 370 processors.
AG1[1]	VSS	VSS	VTT	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • VTT for future 0.13 micron socket 370 processors
AH4	Reserved	RESET#	RESET#	• Processor reset for the Pentium III processor (068xh) and future 0.13 micron socket 370 processors
AH20	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AJ3[2]	VSS	VSS	RESET2#	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • RESET2# for future 0.13 micron socket 370 processors
AK4	VSS	VSS	VTTPWRGD	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • VID control signal on future 0.13 micron socket 370 processors.
AK16	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage

Pin #	Pin Name Intel® Celeron® Processor (CPUID=068xh)	Pin Name Intel® Pentium® III Processor (CPUID=068xh)	Pin Name Future 0.13 Micron Socket 370 Processors	Function
AK22	GTL_REF	GTL_REF	VCMOS_REF	• GTL reference voltage for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • CMOS reference voltage for future 0.13 micron socket 370 processors
AK36	VSS	VSS	VID[25mV]	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • 25mV step VID select bit for future 0.13 micron socket 370 processors
AL13	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AL21	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN3	GND	GND	DYN_OE	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • Dynamic output enable for future 0.13 micron socket 370 processors
AN11	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN15	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN21	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
E23	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
G35	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
G37	Reserved	Reserved	VTT	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • AGTL termination voltage for future 0.13 micron socket 370 processors
N37[2]	NC	NC	NCHCTRL	• No connect for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • NCHCTRL for future 0.13 micron socket 370 processors
S33	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
S37	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
U35	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
U37	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
W3	Reserved	A34#	A34#	• Additional AGTL/AGTL+ address
X4[2]	RESET#	RESET2#	VSS	• Processor reset for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • Ground for future 0.13 micron socket 370 processors

Pin #	Pin Name Intel® Celeron® Processor (CPUID=068xh)	Pin Name Intel® Pentium® III Processor (CPUID=068xh)	Pin Name Future 0.13 Micron Socket 370 Processors	Function
X6	Reserved	A32#	A32#	• Additional AGTL/AGTL+ address
X34[2]	VCC_{CORE}	VCC_{CORE}	V_{TT}	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • AGTL termination voltage for future 0.13 micron socket 370 processors
Y1	Reserved	Reserved	RESERVED	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • RESERVED for future 0.13 micron socket 370 processors
Y33	Reserved	CLKREF	CLKREF	• 1.25 V PLL reference
Z36[2]	VCC2.5	VCC2.5	RESERVED	• VCC2.5 for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). • RESERVED for future 0.13 micron socket 370 processors

NOTES:
1. Refer to Section 4.
2. Refer to Section 13.2 .

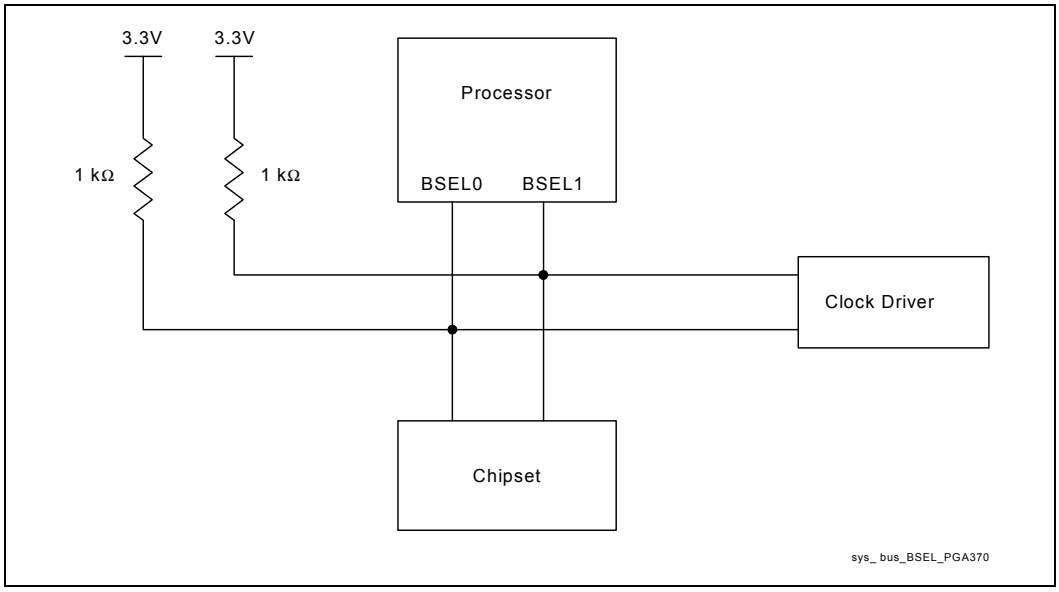
5.5 BSEL[1:0] Implementation Differences

A future 0.13 micron socket 370 processor will select the 133 MHz system bus frequency setting from the clock synthesizer. A Pentium III processor (CPUID=068xh) utilizes the BSEL1 pin to select either the 100 MHz or 133 MHz system bus frequency setting from the clock synthesizer. A Celeron processor (CPUID=068xh) will use both BSEL pins to select 66 MHz system bus frequency from the clock synthesizer. Processors in an FC-PGA or an FC-PGA2 are 3.3 V tolerant for these signals, as are the clock and chipset.

The CK-815 has been designed to support selections of 66 MHz, 100 MHz, and 133 MHz. The REF input pin has been redefined to be a frequency selection strap (BSEL1) during power-on and then becomes a 14 MHz reference clock output. Figure 29 details the new BSEL[1:0] circuit design for *universal PGA370* designs. Note that BSEL[1:0] now are pulled up using 1 kΩ resistors. Also refer to Figure 30 for more details.

Note: In a design supporting future 0.13 micron socket 370 processors, the BSEL[1:0] lines are not valid until VTTPWRGD is asserted. Refer to Section 4.3 and Section 11.6 for full details.

Figure 29. BSEL[1:0] Circuit Implementation for PGA370 Designs



5.6 CLKREF Circuit Implementation

The CLKREF input (used by the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors) requires a 1.25 V source. It can be generated from a voltage divider on the VCC2.5 or VCC3.3 sources utilizing 1% tolerant resistors. A 4.7 µF decoupling capacitor should be included on this input. See Figure 30 and Table 14 for example CLKREF circuits. **Do not use VTT as the source for this reference!**

Figure 30. Examples for CLKREF Divider Circuit

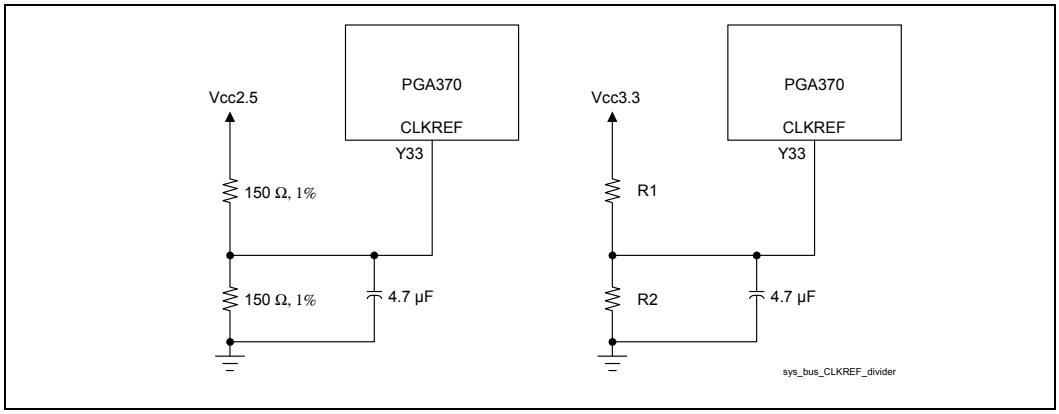


Table 14. Resistor Values for CLKREF Divider (3.3 V Source)

R1 (Ω), 1%	R2 (Ω), 1%	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

5.7 Undershoot/Overshoot Requirements

Undershoot and overshoot specifications become more critical as the process technology for microprocessors shrinks due to thinner gate oxide. Violating these undershoot and overshoot limits will degrade the life expectancy of the processor.

The Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors have more restrictive overshoot and undershoot requirements for system bus signals than previous processors. These requirements stipulate that a signal at the output of the driver buffer and at the input of the receiver buffer must not exceed the maximum absolute overshoot voltage limit or the minimum absolute undershoot voltage limit. Exceeding either of these limits will damage the processor. There is also a time-dependent, non-linear overshoot and undershoot requirement that depends on the amplitude and duration of the overshoot/undershoot. See the appropriate processor datasheet for more details on the processor overshoot/undershoot specifications.

5.8 Processor Reset Requirements

Universal PGA370 designs must route the AGTL/AGTL+ reset signal from the chipset to two pins on the processor as well as to the debug port connector. This reset signal is connected to the following pins at the PGA370 socket:

- **AH4 (RESET#).** The reset signal is connected to this pin for the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors
- **X4 (Reset2# or GND, depending on processor).** The X4 pin is RESET2# for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). X4 is GND for future 0.13 micron socket 370 processors. An additional 1 kΩ resistor is connected in series with pin X4 to the reset circuitry since pin X4 is a ground pin in future 0.13 micron socket 370 processors.

Note: The AGTL/AGTL+ reset signal must always terminate to VTT on the motherboard.

Designs that do not support the debug port will not utilize the 240 Ω series resistor or the connection of RESET# to the debug port connector**.** RESET2# is not required for platforms that do not support the Celeron processor (CPUID=068xh). Pin X4 should then be connected to ground.

The routing rules for the AGTL/AGTL+ reset signal are shown in Figure 31.

Figure 31. RESET#/RESET2# Routing Guidelines

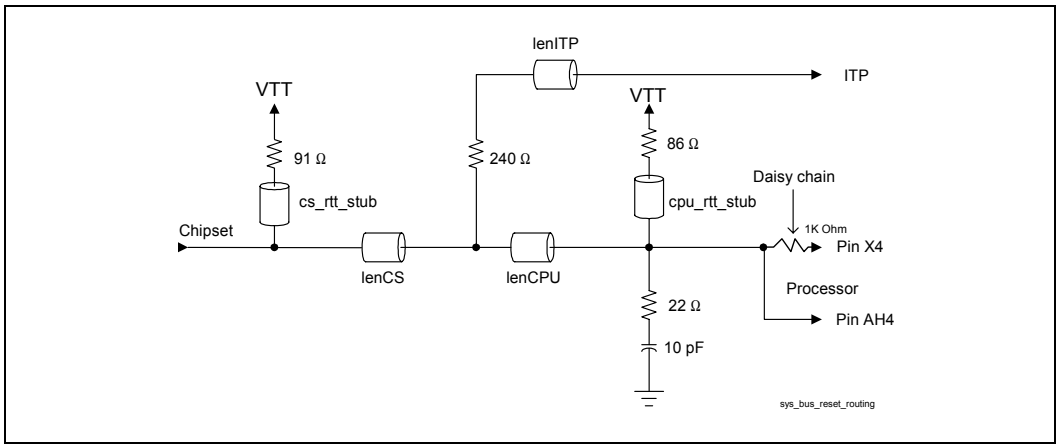


Table 15. RESET#/RESET2# Routing Guidelines (see Figure 31)

Parameter	Minimum (in)	Maximum (in)
LenCS	0.5	1.5
LenITP	1	3
LenCPU	0.5	1.5
cs_rtt_stub	0.5	1.5
cpu_rtt_stub	0.5	1.5

5.9 Processor PLL Filter Recommendations

Intel® PGA370 processors have internal phase lock loop (PLL) clock generators that are analog and require quiet power supplies to minimize jitter.

5.9.1 Topology

The general desired topology for these PLLs is shown in Figure 33. Not shown are the parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

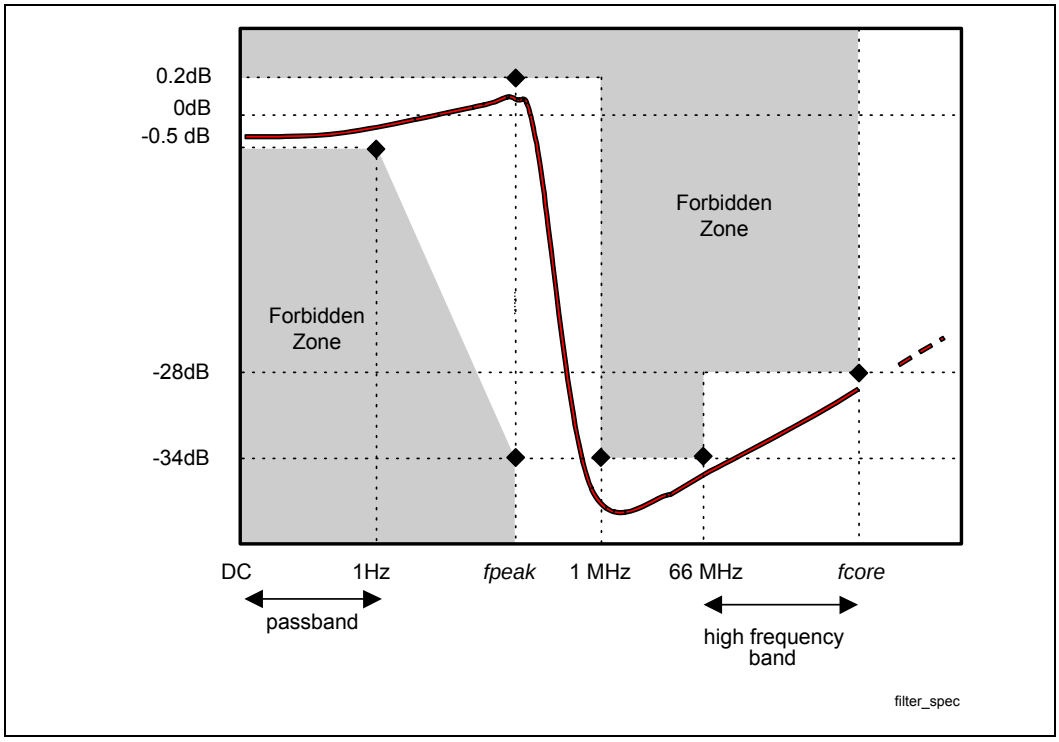
5.9.2 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 32.

Figure 32. Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak* should be less than 0.05 MHz.

Other requirements:

- Use shielded-type inductor to minimize magnetic pickup.
- Filter should support DC current > 30 mA.
- DC voltage drop from VCC to PLL1 should be < 60 mV, which in practice implies series R < 2 Ω. This also means pass-band (from DC to 1 Hz) attenuation < 0.5 dB for VCC = 1.1 V, and < 0.35 dB for VCC = 1.5 V.

5.9.3 Recommendation for Intel Platforms

The following tables contains examples of components that meet Intel recommendations when configured in the topology of Figure 33.

Table 16. Component Recommendations – Inductor

Part Number	Value	Tolerance	SRF	Rated Current	DCR (Typical)
TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max.)
Murata LQG21N4R7K00T1	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (±50%)
Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3 Ω max.

Table 17. Component Recommendations – Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%	2.5 nH	0.2 Ω

Table 18. Component Recommendation – Resistor

Value	Tolerance	Power	Note
1 Ω	10%	1/16 W	Resistor may be implemented with trace resistance, in which case a discrete R is not needed. See Figure 34.

To satisfy damping requirements, total series resistance in the filter (from VCC_{CORE} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component or routing or both. For example, if the chosen inductor has minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1 (1 Ω ± 1%), the maximum DCR of the L (trace plus inductor) should be less than 2.0 – 1.1 = 0.9 Ω, which precludes the use of some inductors and sets a max. trace length.

Other routing requirements:

- The capacitor (C) should be close to the PLL1 and PLL2 pins, < 0.1 Ω per route. These routes do not count towards the minimum damping R requirement.
- The PLL2 route should be parallel and next to the PLL1 route (i.e., minimize loop area).
- The inductor (L) should be close to C. Any routing resistance should be inserted between VCC_{CORE} and L.
- Any discrete resistor (R) should be inserted between VCC_{CORE} and L.

Figure 33. Example PLL Filter Using a Discrete Resistor

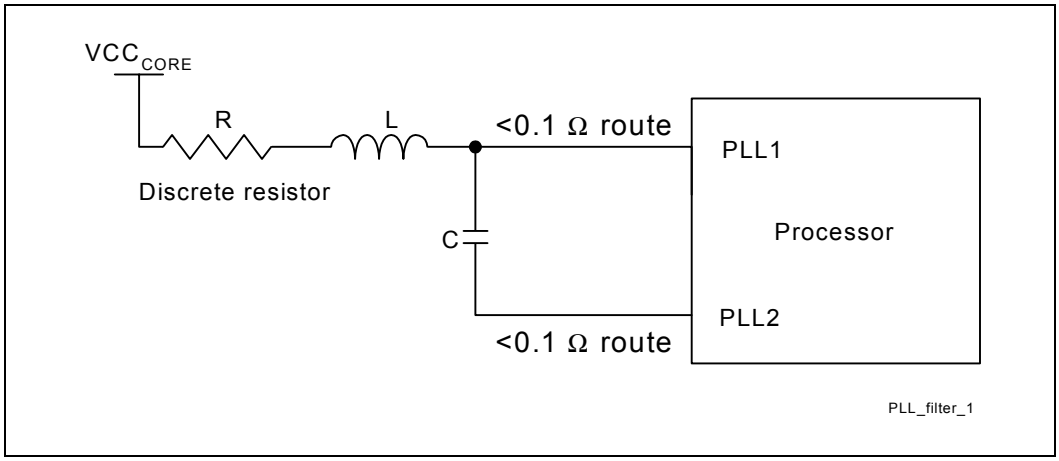
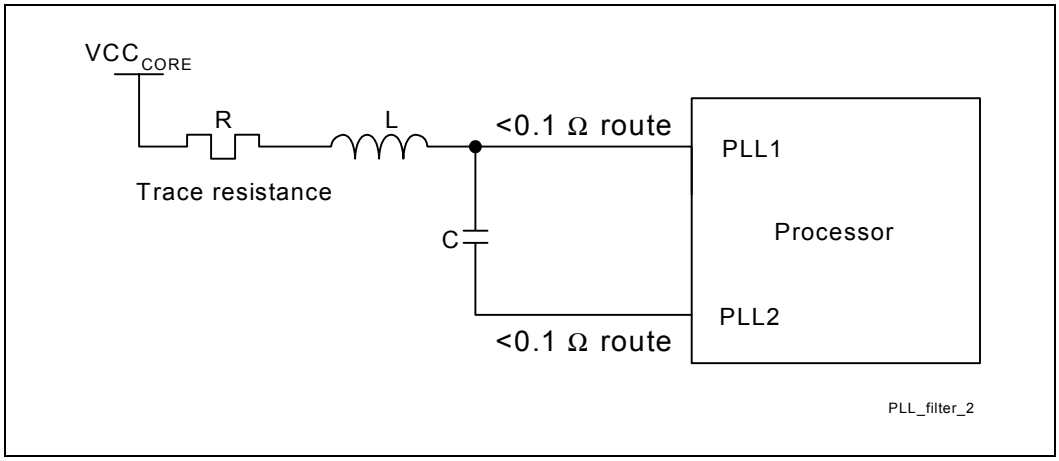


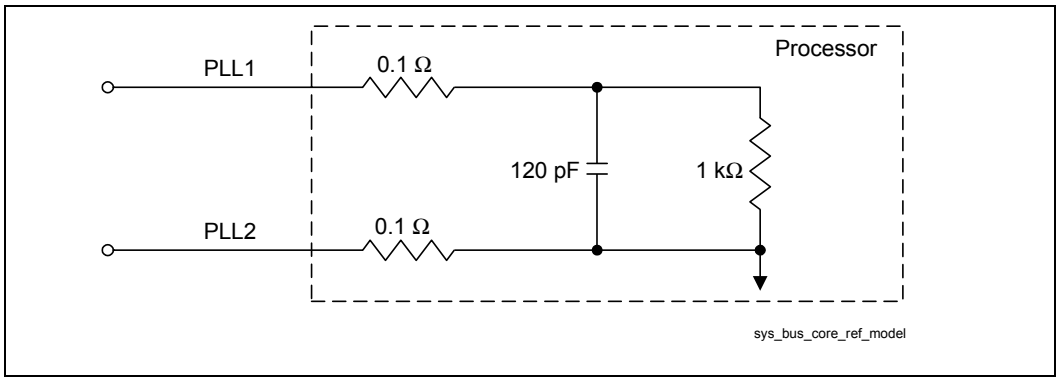
Figure 34. Example PLL Filter Using a Buried Resistor



5.9.4 Custom Solutions

As long as designers satisfy filter performance and requirements as specified and outlined in Section 5.9.2, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in Figure 35.

Figure 35. Core Reference Model



NOTES:
1. 0.1 Ω resistors represent package routing.
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1 kΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum VCC_{CORE} level.
7. For other modules (interposer, DMM, etc.), adjust routing resistor if desired, but use minimum numbers.

5.10 Voltage Regulation Guidelines

A universal PGA370 design will need the voltage regulation module (VRM) or on-board voltage regulator (VR) to be compliant with Intel® VRM guidelines for future 0.13 micron processors.

5.11 Decoupling Guidelines for Universal PGA370 Designs

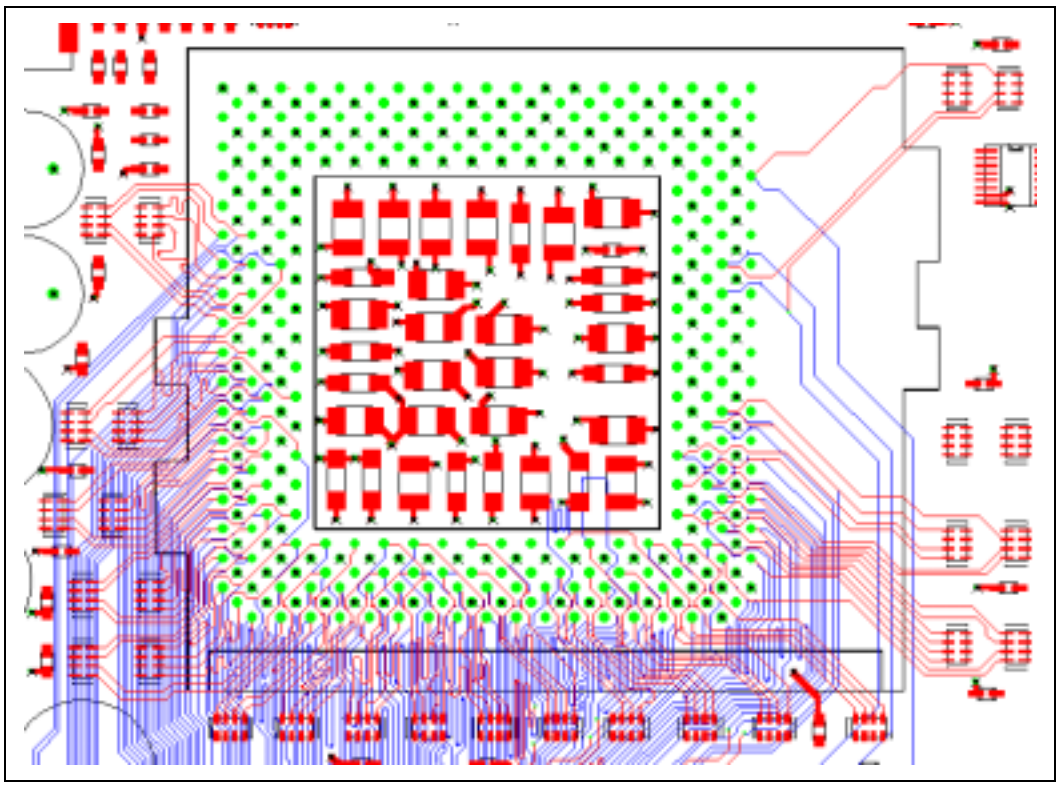
These preliminary decoupling guidelines for *universal PGA370* designs are estimated to meet the specifications of VRM guidelines for future 0.13 micron processors.

5.11.1 VCC_{CORE} Decoupling Design

- Sixteen or more 4.7 µF capacitors in 1206 packages.

All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between the VCC_{CORE}/VSS power pins, as shown in Figure 36.

Figure 36. Capacitor Placement on the Motherboard



5.11.2 VTT Decoupling Design

For Itt = 2.3 A (max.)

- Twenty 0.1 µF capacitors in 0603 packages placed as closed as possible to the processor VTT pins. The capacitors are shown on the exterior of Figure 36.

5.11.3 VREF Decoupling Design

- Four 0.1 µF capacitors in 0603 package placed near VREF pins (within 500 mils).

5.12 Thermal Considerations

5.12.1 Heatsink Volumetric Keep-Out Regions

Current heatsink recommendations are only valid for supported Celeron and Pentium III processor frequencies up to 1GHz.

Figure 37 shows the system component keep-out volume above the socket connector required for the reference design thermal solution for high frequency processors. This keep-out envelope provides adequate room for the heatsink, fan and attach hardware under static conditions as well as room for installation of these components on the socket. The heatsink must be compatible with the Integrated Heat Spreader (IHS) used by higher frequency Pentium III processors.

Figure 38 shows component keep-outs on the motherboard required to prevent interference with the reference design thermal solution. Note portions of the heatsink and attach hardware hang over the motherboard.

Adhering to these keep-out areas will ensure compatibility with Intel boxed processor products and Intel enabled third party vendor thermal solutions for high frequency processors. While the keep-out requirements should provide adequate space for the reference design thermal solution, systems integrators should check with their vendors to ensure their specific thermal solutions fit within their specific system designs. Please ensure that the thermal solutions under analysis comprehend the specific thermal design requirements for higher frequency Pentium III processors.

While thermal solutions for lower frequency processors may not require the full keep-out area, larger thermal solutions will be required for higher frequency processors, and failure to adhere to the guidelines will result in mechanical interference.

Figure 37. Heatsink Volumetric Keep-Out Regions

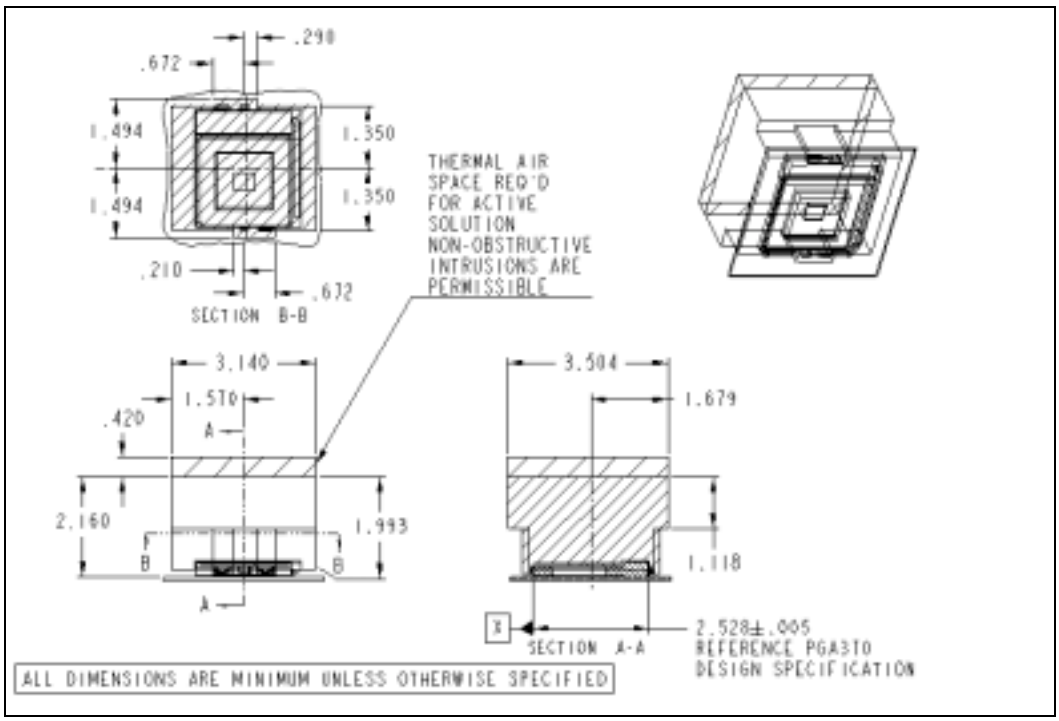
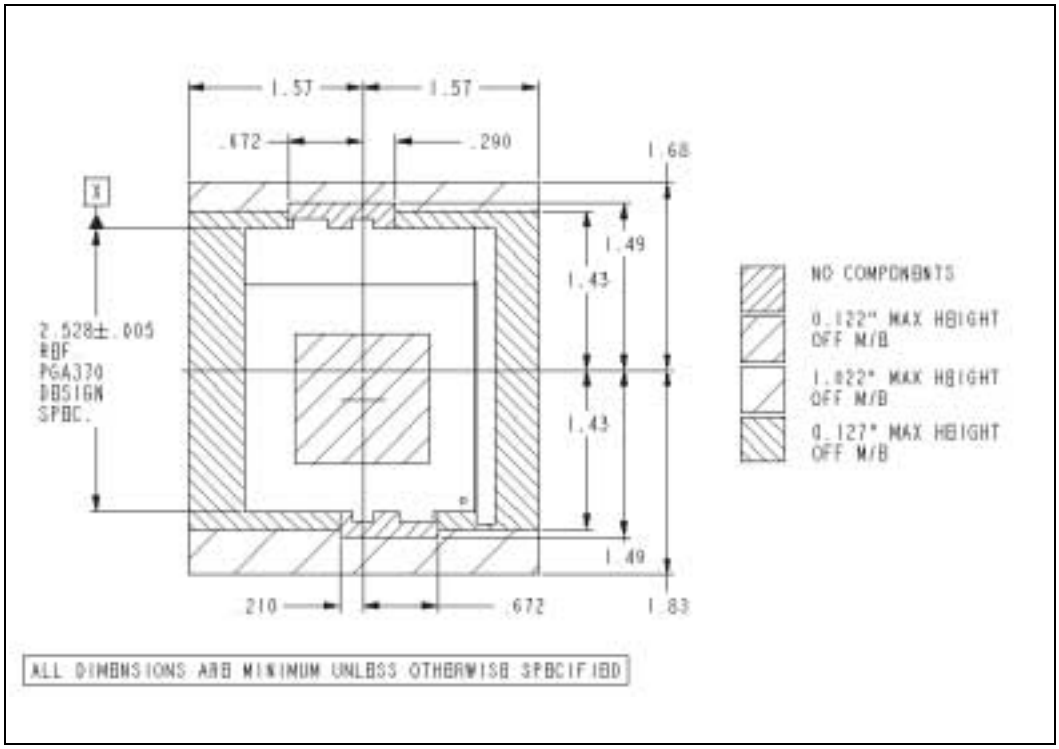


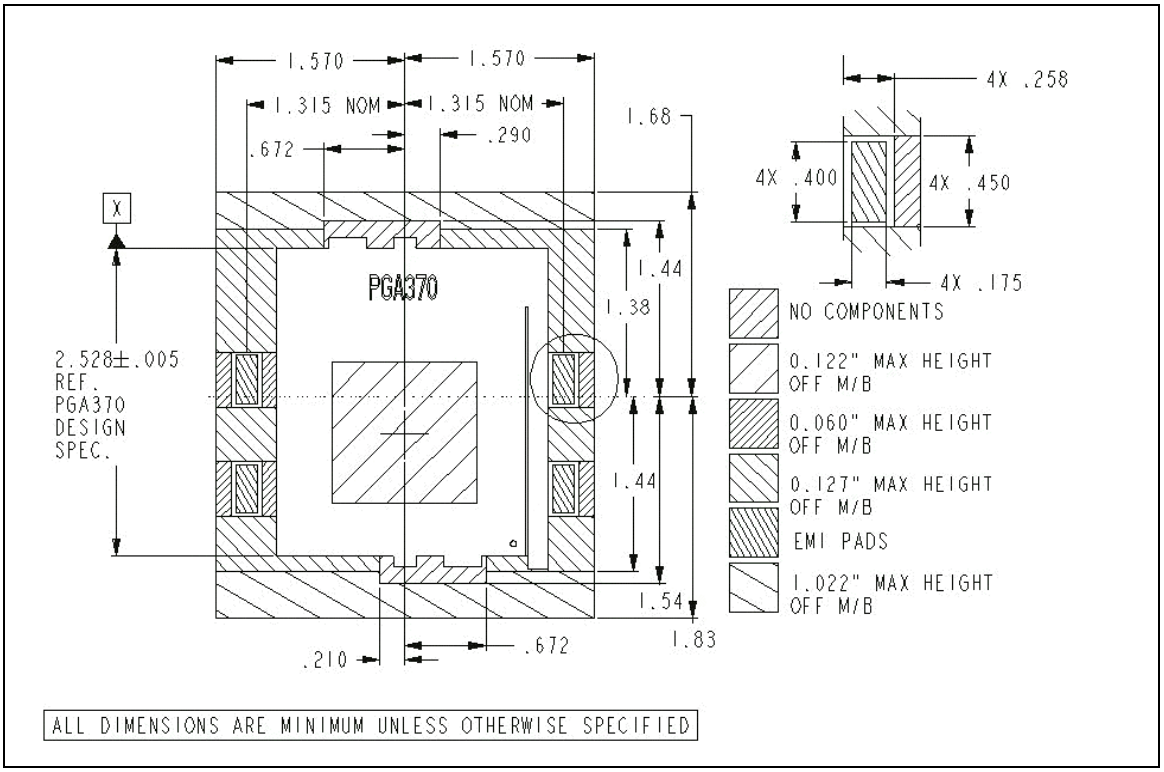
Figure 38. Motherboard Component Keep-Out Regions



5.12.2 Fan Heatsink Keep-Out Adherence for Future Boxed Intel® Celeron® Processors

Mother board designs intended to support future boxed Celeron processors manufactured on the 0.13 micron process technology must meet fan heatsink keep-out requirements as specified in the *Intel® Celeron® Processor EMTS*. (Also see Figure 39 below.) Future Celeron processors will use the larger fan heatsink, which demands adherence to maximum keep-out dimensions. Several previous 815 and 815E chipset based motherboards did not adhere to Intel specified keep-out requirements. When revising previous 815E motherboard designs to support the boxed Intel Celeron processor manufactured on the 0.13-micron process technology, ensure motherboard components do not interfere with fan-heatsink maximum keep-out area.

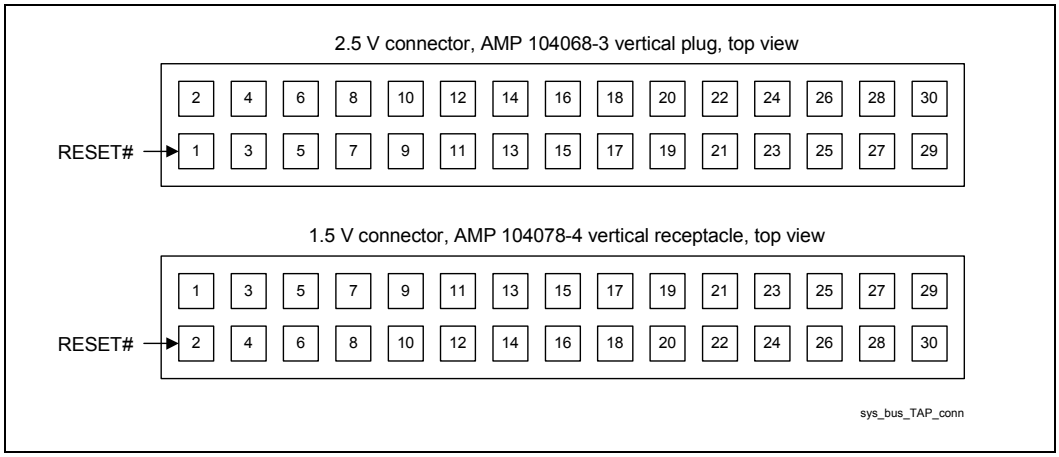
Figure 39. Keep-Out Requirements for the 370-Pin (Top View)



5.13 Debug Port Changes

Due to the lower voltage technology employed with newer processors, changes are required to support the debug port. Previously, test access port (TAP) signals used 2.5 V logic, as is the case with the Celeron processor in the PPGA package. Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors utilize 1.5 V logic levels on the TAP. As a result, the type of debug port connecter used in *universal PGA370* designs is dependent on the processor that is currently in the socket. The 1.5 V connector is a mirror image of the older 2.5 V connector. Either connector will fit into the same printed circuit board layout. Only the pin numbers change (Figure 40). Also required, along with the new connector, is an In-Target Probe* (ITP) that is capable of communicating with the TAP at the appropriate logic levels.

Figure 40. TAP Connector Comparison



Caution: The Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) require an in-target probe (ITP) compatible with 1.5 V signal levels on the TAP. Previous ITPs were designed to work with higher voltages and may damage the processor if connected to any of these specified processors.

See the processor datasheet for more information regarding the debug port.

6 System Memory Design Guidelines

6.1 System Memory Routing Guidelines

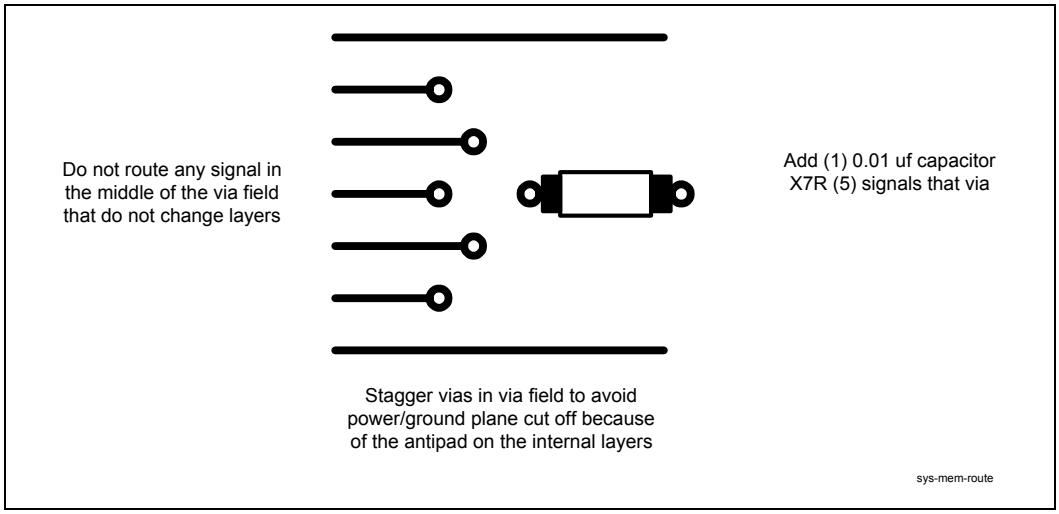
Ground plane reference all system memory signals. To provide a good current return path and limit noise on the system memory signals, the signals should be ground referenced from the MCH to the DIMM connectors and from DIMM connector-to-DIMM connector. If ground referencing is not possible, system memory signals should be, at a minimum, referenced to a single plane. If single plane referencing is not possible, stitching capacitors should be added no more than 200 mils from the signal via field. System memory signals may via to the backside of the PCB under the MCH without a stitching capacitor as long as the trace on the topside of the PCB is less than 200 mils.

Note: Intel recommends that a parallel plate capacitor between VCC3.3SUS and GND be added to account for the current return path discontinuity (See Decoupling section). Use (1) 0.01 µf X7R capacitor per every (5) system memory signals that switch plane references. No more than two vias are allowed on any system memory signal.

If a group of system memory signals must change layers, a via field should be created and a decoupling capacitor should be added at the end of the via field. Do not route signals in the middle of a via field, this causes noise to be generated on the current return path of these signals and can lead to issues on these signals (see Figure 41). The traces shown are on layer 1 only. The figure shows signals that are changing layer and two signals that are not changing layer.

Note: The two signals around the via field create a keep-out zone where no signals that do not change layer should be routed.

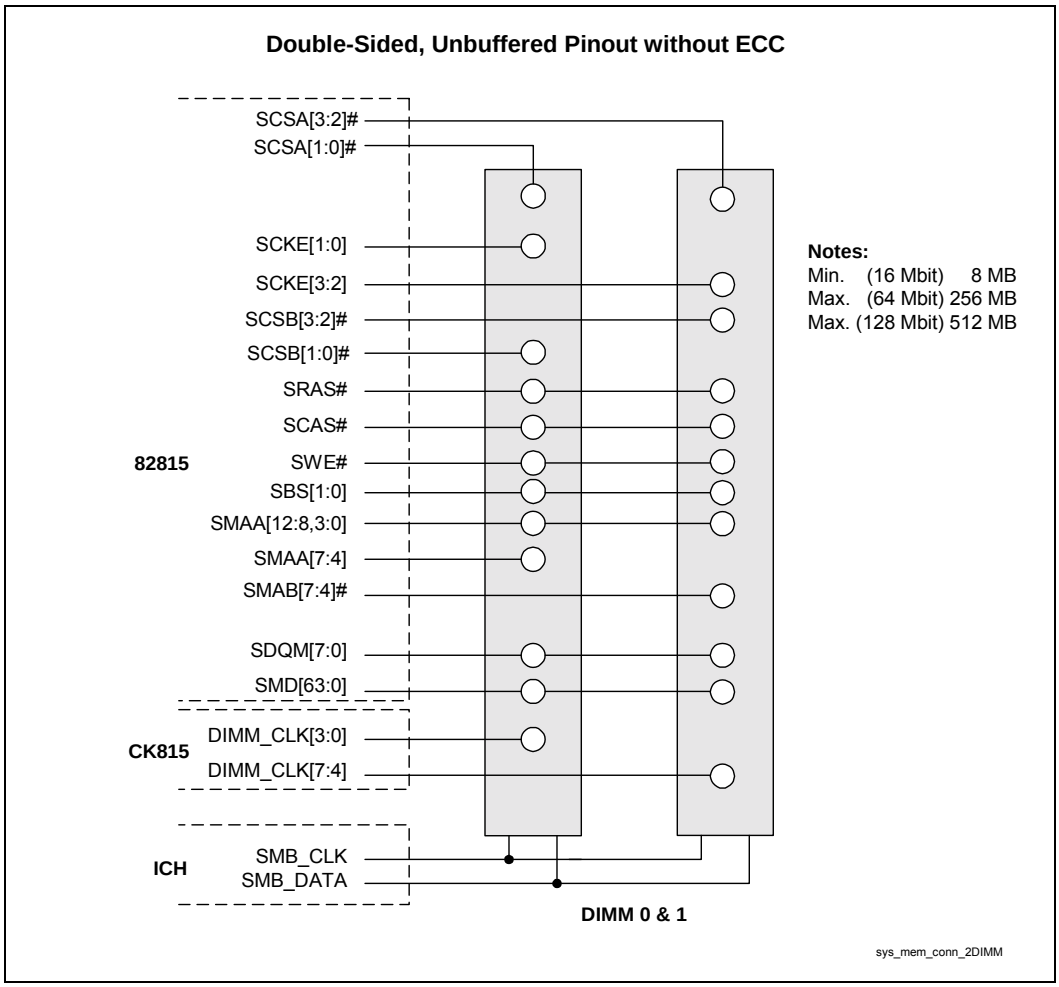
Figure 41. System Memory Routing Guidelines



6.2 System Memory 2-DIMM Design Guidelines

6.2.1 System Memory 2-DIMM Connectivity

Figure 42. System Memory Connectivity (2 DIMM)



6.2.2 System Memory 2-DIMM Layout Guidelines

Figure 43. System Memory 2-DIMM Routing Topologies

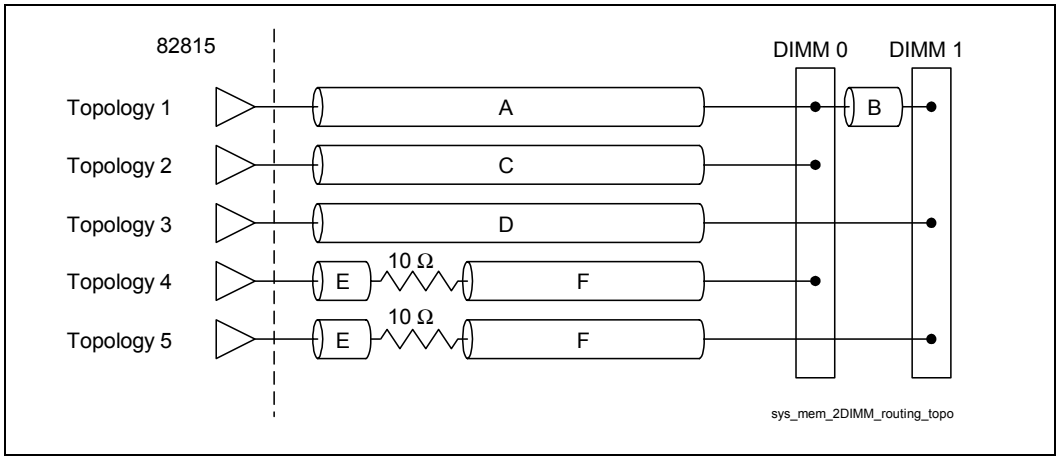
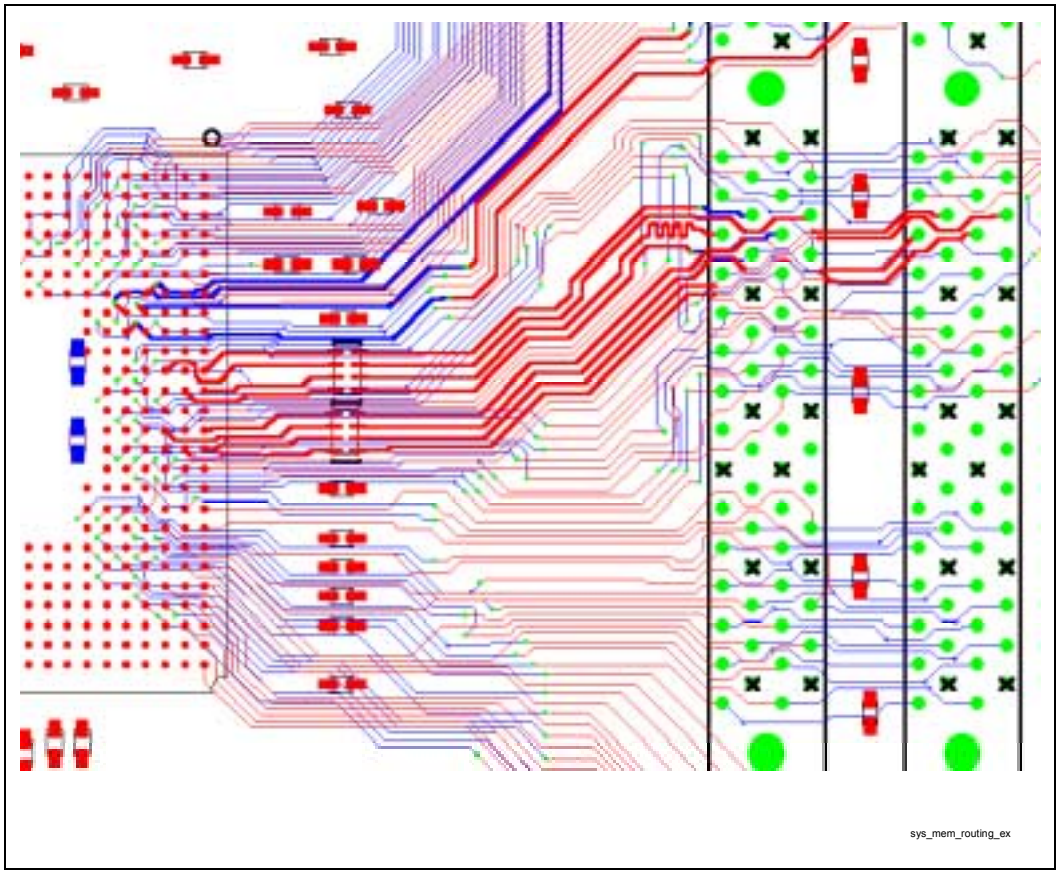


Table 19. System Memory 2-DIMM Solution Space

Signal	Top.	Trace (mils)		Trace Lengths (inches)											
				A		B		C		D		E		F	
		Width	Spacing	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SCS[3:2]#	3	5	10							1	4.5				
SCS[1:0]#	2	5	10					1	4.5						
SMAA[7:4]	4	10	10									0.4	0.5	2	4
SMAB[7:4]#	5	10	10									0.4	0.5	2	4
SCKE[3:2]	3	10	10							3	4				
SCKE[1:0]	2	10	10					3	4						
SMD[63:0]	1	5	10	1.75	4	0.4	0.5								
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5								
SCAS#, SRAS#, SWE#	1	5	10	1	4.0	0.4	0.5								
SBS[1:0], SMAA[12:8,3:0]	1	5	10	1	4.0	0.4	0.5								

In addition to meeting the spacing requirements outlined in Table 19, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

Figure 44. System Memory Routing Example

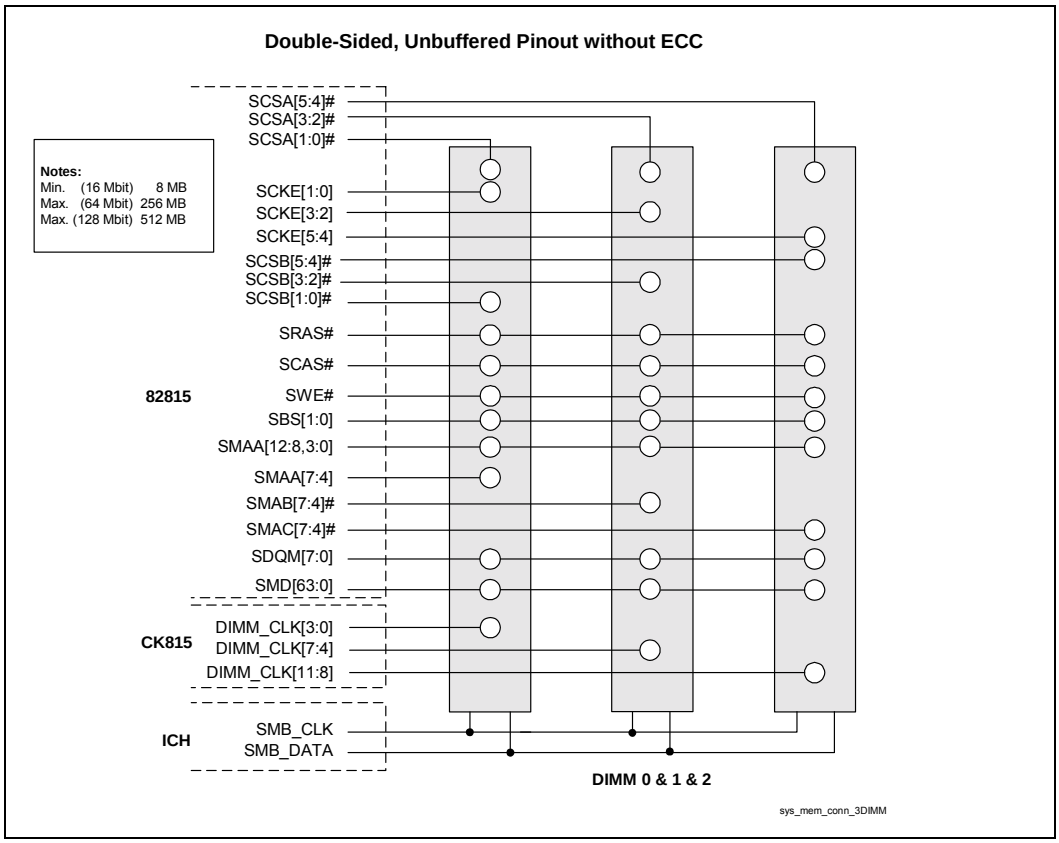


NOTE: Routing in this figure is for example purposes only. It does not necessarily represent complete and correct routing for this interface.

6.3 System Memory 3-DIMM Design Guidelines

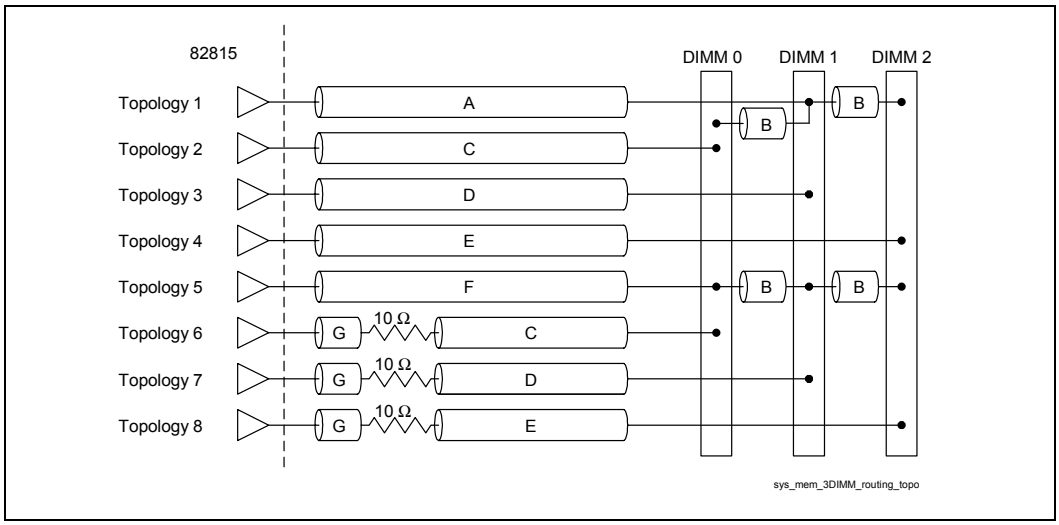
6.3.1 System Memory 3-DIMM Connectivity

Figure 45. System Memory Connectivity (3 DIMM)



6.3.2 System Memory 3-DIMM Layout Guidelines

Figure 46. System Memory 3-DIMM Routing Topologies



In addition to meeting the spacing requirements outlined in Table 20, system memory signal trace edges must be at least 30 mils from any other non-system memory signal trace edge.

Table 20. System Memory 3-DIMM Solution Space

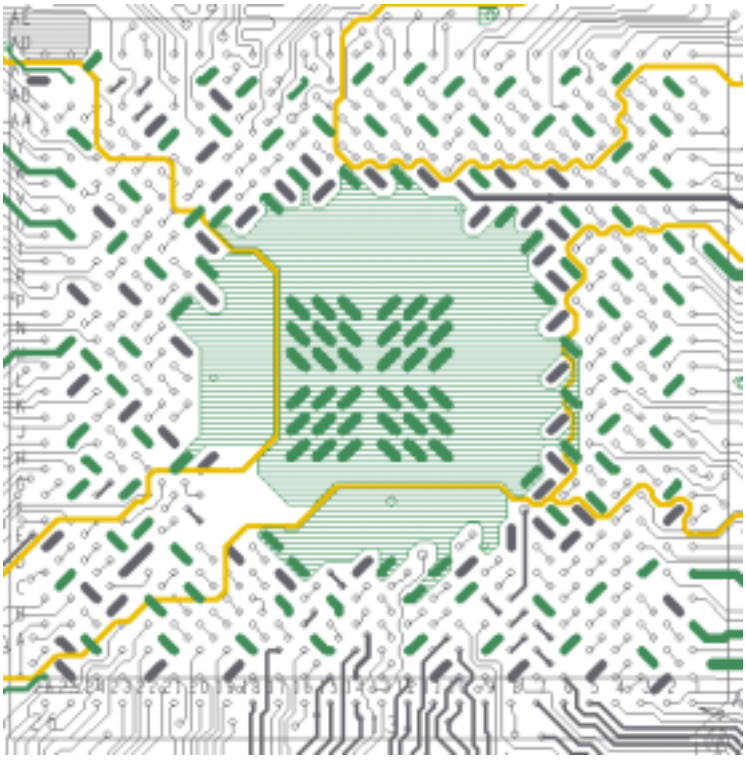
Signal	Top.	Trace (mils)		Trace Lengths (inches)													
				A		B		C		D		E		F		G	
		Width	Spacing	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
SCS[5:4]#	4	5	10									1	4.5				
SCS[3:2]#	3	5	10							1	4.5						
SCS[1:0]#	2	5	10					1	4.5								
SMAA[7:4]	6	10	10					2	4							0.4	0.5
SMAB[7:4]#	7	10	10							2	4					0.4	0.5
SMAC[7:4}	8	10	10									2	4			0.4	0.5
SCKE[5:4]	4	10	10									3	4				
SCKE[3:2]	3	10	10							3	4						
SCKE[1:0]	2	10	10					3	4								
SMD[63:0]	1	5	10	1.75	4	0.4	0.5										
SDQM[7:0]	1	10	10	1.5	3.5	0.4	0.5										
SCAS#,SRAS#, SWE#	5	5	10			0.4	0.5							1	4		
SBS[1:0], SMAA[12:8,3:0]	5	5	10			0.4	0.5							1	4		

6.4 System Memory Decoupling Guidelines

A minimum of eight 0.1 µF low-ESL ceramic capacitors (e.g., 0603 body type, X7R dielectric) are required and must be as close as possible to the MCH. They should be placed within at most 70 mils to the edge of the MCH package edge for VSUS_3.3 decoupling, and they should be evenly distributed around the system memory interface signal field including the side of the MCH where the system memory interface meets the host interface. There are power and GND balls throughout the system memory ball field of the MCH that need good local decoupling. Make sure to use at least 14 mil drilled vias and wide traces from the pads of the capacitor to the power or ground plane to create a low inductance path. If possible multiple vias per capacitor pad are recommended to further reduce inductance. To add the decoupling capacitors within 70 mils of the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (500mils max).

To further de-couple the MCH and provide a solid current return path for the system memory interface signals it is recommended that a parallel plate capacitor be added under the MCH. Add a topside or bottom side copper flood under center of the MCH to create a parallel plate capacitor between VCC3.3 and GND (see Figure 47). The dashed lines indicate power plane splits on layer 2 or layer 3 depending on stack-up. The filled region in the middle of the MCH indicates a ground plate (on layer 1 if the power plane is on layer 2 or on layer 4 if the power layer is on layer 3).

Figure 47. Intel® 815 Chipset Platform Decoupling Example



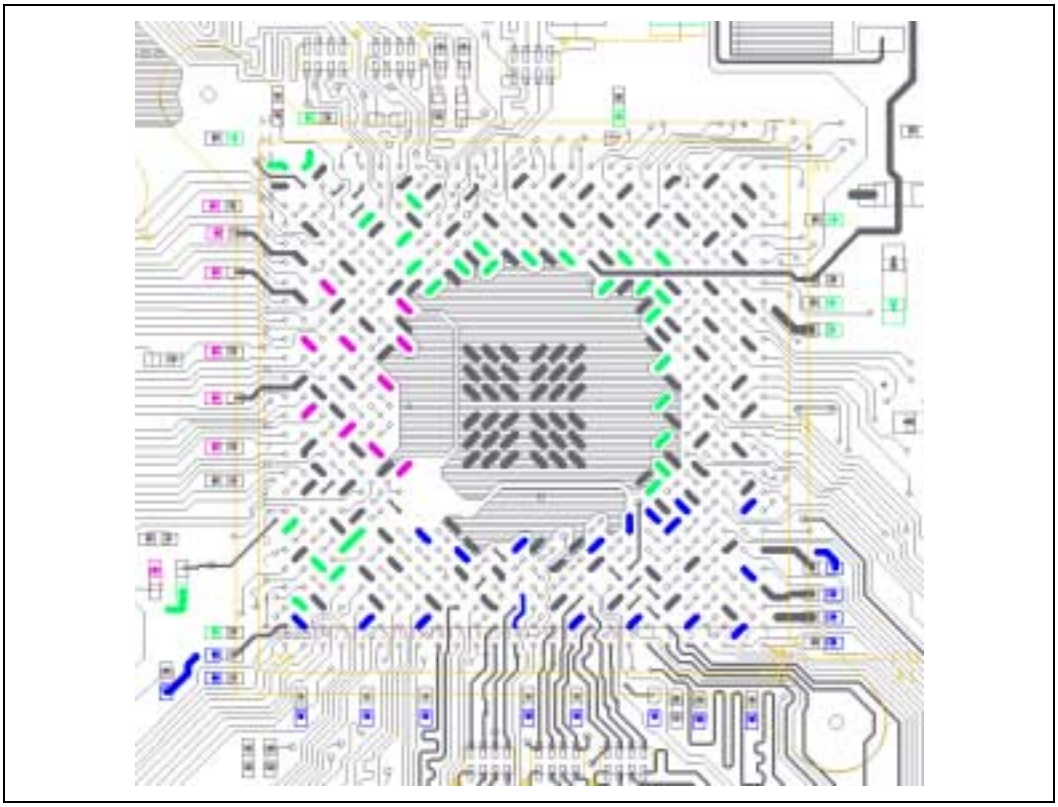
Yellow lines in Figure 47 show layer two plane splits. (Printed versions of this document will show the layer two plane splits in the left-side, bottom, right-side, and upper right-side quadrants

enclosed in gray lines.) Note that the layer 1 shapes **do not** cross the plane splits. The bottom shape is a VSS fill over VddSDRAM. The left-side shape is a VSS fill over VddAGP. The larger upper-right-side shape is a VSS fill over VddCORE.

Additional decoupling capacitors should be added between the DIMM connectors to provide a current return path for the reference plane discontinuity created by the DIMM connectors themselves. One 0.01uf X7R capacitor should be added per every ten SDRAM signals. Capacitors should be placed between the DIMM connectors and evenly spread out across the SDRAM interface.

For debug purposes, four or more 0603 capacitor sites should be placed on the backside of the board, evenly distributed under the 815EP chipset platform's system memory interface signal field.

Figure 48. Intel® 815 Chipset Decoupling Example



6.5 Compensation

A system memory compensation resistor (SRCOMP) is used by the MCH to adjust the buffer characteristics to specific board and operating environment characteristics. Refer to the *Intel® 815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH) for use with the Universal Socket 370* Datasheet for details on compensation. Tie the SRCOMP pin of the MCH to a 40 Ω 1% or 2% pull-up resistor to 3.3 Vsus (3.3 V standby) via a 10 mil-wide, 0.5 inch trace (targeted for a nominal impedance of 40 Ω).

7 AGP Design Guidelines

For the detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to the latest *AGP Interface Specification*, *Revision 2.0*, which can be obtained from http://www.agpforum.org. This design guide focuses only on specific 815EP chipset platform recommendations.

7.1 AGP Interface

A single AGP connector is supported by the MCH AGP interface. LOCK# and SERR#/PERR# are not supported.

The AGP buffers operate in one of two selectable modes, to support the AGP universal connector:

- 3.3 V drive, not 5 V safe. This mode is compliant with the AGP 1.0 66 MHz specification
- 1.5 V drive, not 3.3 V safe. This mode is compliant with the AGP 2.0 specification

The AGP 4X must operate at 1.5 V and only use differential clocking mode. The AGP 2X can operate at 3.3 V or 1.5 V. The AGP interface supports up to 4X AGP signaling, though 4X fast writes are not supported. AGP semantic cycles to DRAM are not snooped on the host bus.

The MCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. The MCH contains a 32-deep AGP request queue. High-priority accesses are supported. All AGP semantic accesses hitting the graphics aperture pass through an address translation mechanism with a fully-associative, 20-entry TLB.

Accesses between AGP and the hub interface are limited to hub interface-originated memory writes to AGP. Cacheable accesses from the IOQ queue flow through one path, while aperture accesses follow another path. Cacheable AGP (SBA, PIPE#, and FRAME#) reads to DRAM all snoop the cacheable global write buffer (GWB) for system data coherency. Aperture AGP (SBA, PIPE#) reads to DRAM snoop the aperture queue (GCMCRWQ). Aperture AGP (FRAME#) reads and writes to DRAM proceed through a FIFO and there is no RAW capability, so no snoop is required.

The AGP interface is clocked from the 66 MHz clock (3V66). The AGP-to-host/memory interface is synchronous with a clock ratio of 1:1 (66 MHz : 66 MHz), 2:3 (66 MHz : 100 MHz) and 1:2 (66 MHz : 133 MHz).

7.1.1 AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that AGP cards may come unseated during system shipping and handling without proper retention. To avoid disengaged AGP cards, Intel recommends that AGP-based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket that is used to properly locate the card with respect to the chassis and to assist with card retention. The AGP RM is available in two different handle orientations: left-handed (see Figure 49) and right-handed. Most system boards accommodate the left-handed AGP RM. The manufacturing capacity of the left-handed RM currently exceeds the right-handed capacity, and as a result Intel recommends that customers design their systems to insure they can use the left-handed version of the AGP RM. The right-handed AGP RM is identical to the left-handed AGP RM, except for the position of the actuation handle. This handle is located on the same end as the primary design, but extends from the opposite side (mirrored about the center axis running parallel to the length of the part). Figure 50 contains keep-out information for the left hand AGP retention mechanism. Use this information to make sure that the motherboard design leaves adequate space to install the retention mechanism.

The AGP interconnect design requires that the AGP card must be retained to the extent that the card not back out more than 0.99 mm (0.039 in) within the AGP connector. To accomplish this it is recommended that new cards implement an additional notch feature in the mechanical keying tab to allow an anchor point on the AGP card for interfacing with an AGP RM. The retention mechanism's round peg engages with the AGP or GPA card's retention tab and prevents the card from disengaging during dynamic loading. The additional notch feature in the mechanical keying tab is required for 1.5 V AGP cards and is recommended for the new 3.3 V AGP cards.

Figure 49. AGP Left-Handed Retention Mechanism

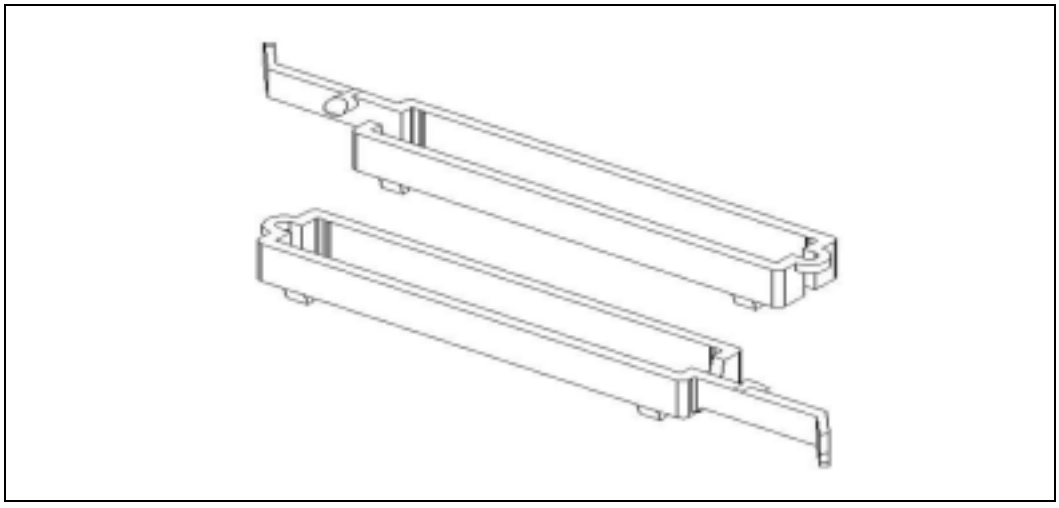
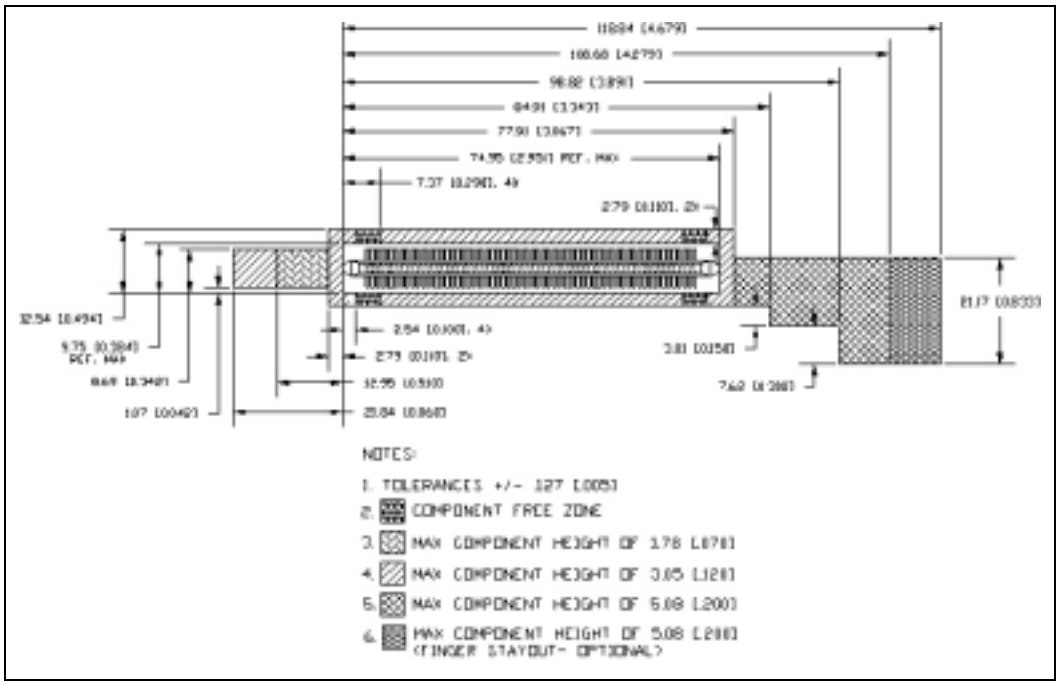


Figure 50. AGP Left-Handed Retention Mechanism Keep-Out Information



Engineering Change Request number 48 (ECR #48) of the AGP specification details the AGP RM, which is recommended for all AGP cards. These are approved changes to the *Accelerated Graphics Port (AGP) Interface Specification, Revision 2.0*. Intel intends to incorporate the AGP RM changes into later revisions of the AGP Interface Specification. In addition, Intel has defined a reference design of a mechanical device to utilize the features defined in ECR #48.

ECR #48 can be viewed off the Intel website at:

http://developer.intel.com/technology/agp/ecr.htm

More information regarding this component (AGP RM) is available from the following vendors.

Table 21. Retention Mechanism Vendors

Resin Color	Supplier Part Number	"Left Handed" Orientation (Preferred)	"Right Handed" Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

7.2 AGP 2.0

The *Accelerated Graphics Port (AGP) Interface Specification, Revision 2.0*. enhances the functionality of the original *AGP Interface Specification, Revision 1.0*, by allowing 4X data transfers (4 data samples per clock) and 1.5 V operation. The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66 MHz AGP clock, which means that each data cycle is ¼ of a 15 ns (66 MHz) clock, or 3.75 ns. Note that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66 MHz clock cycle, so the data cycle time is 7.5 ns. To allow for such high-speed data transfers, the 2X mode of AGP operation uses source-synchronous data strobing. During 4X operation, the AGP interface uses differential source-synchronous strobing.

With data-cycle times as small as 3.75 ns and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines causes the settling time to be long. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled. The low-voltage operation on the AGP (1.5 V) requires even more noise immunity. For example, during 1.5 V operation, Vil_{max} is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

7.2.1 AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: *1X timing domain signals*, *2X/4X timing domain signals*, and *miscellaneous signals*. Each group has different routing requirements. In addition, within the *2X/4X timing domain signals*, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. However, trace length matching requirements only must be satisfied within each set of 2X/4X timing domain signals. The signal groups are listed in Table 22.

Table 22. AGP 2.0 Signal Groups

Groups	Signal
1X Timing Domain	CLK (3.3 V), RBF#, WBF#, ST[2:0], PIPE#, REQ#, GNT#, PAR, FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#
2X/4X Timing Domain	**Set #1:** AD[15:0], C/BE[1:0]#, AD_STB0, AD_STB0#[1] **Set #2:** AD[31:16], C/BE[3:2]#, AD_STB1, AD_STB1#[1] **Set #3:** SBA[7:0], SB_STB, SB_STB#[1]
Miscellaneous, async.	USB+, USB-, OVRCNT#, PME#, TYPDET#, PERR#, SERR#, INTA#, INTB#

NOTE: These signals are used in 4X AGP mode ONLY.

Table 23. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section the term *data* refers to AD[31:0], C/BE[3:0]#, and SBA[7:0]. The term *strobe* refers to AD_STB[1:0], AD_STB[1:0]#, SB_STB, and SB_STB#. When the term *data* is used, it refers to one of the three sets of data signals, as listed in Table 22. When the term *strobe* is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (*1X timing domain signals*, *2X/4X timing domain signals*, *miscellaneous signals)* will be addressed separately.

7.3 Standard AGP Routing Guidelines

These routing guidelines cover a standard AGP solution. This uses an AGP compliant device on an external add-in card that plugs into an AGP connector on the motherboard.

7.3.1 1X Timing Domain Routing Guidelines

7.3.1.1 External AGP Card Motherboard Guidelines

- The AGP 1X timing domain signals (Table 22) have a maximum trace length of 7.5 inches for motherboards that will **NOT** support a Graphics Performance Accelerator (GPA) card. This maximum applies to ALL signals listed as 1X timing domain signals in Table 22.
- All AGP 1X timing domain signals can be routed with 5-mil minimum trace separation.
- There are no trace length matching requirements for 1X timing domain signals.

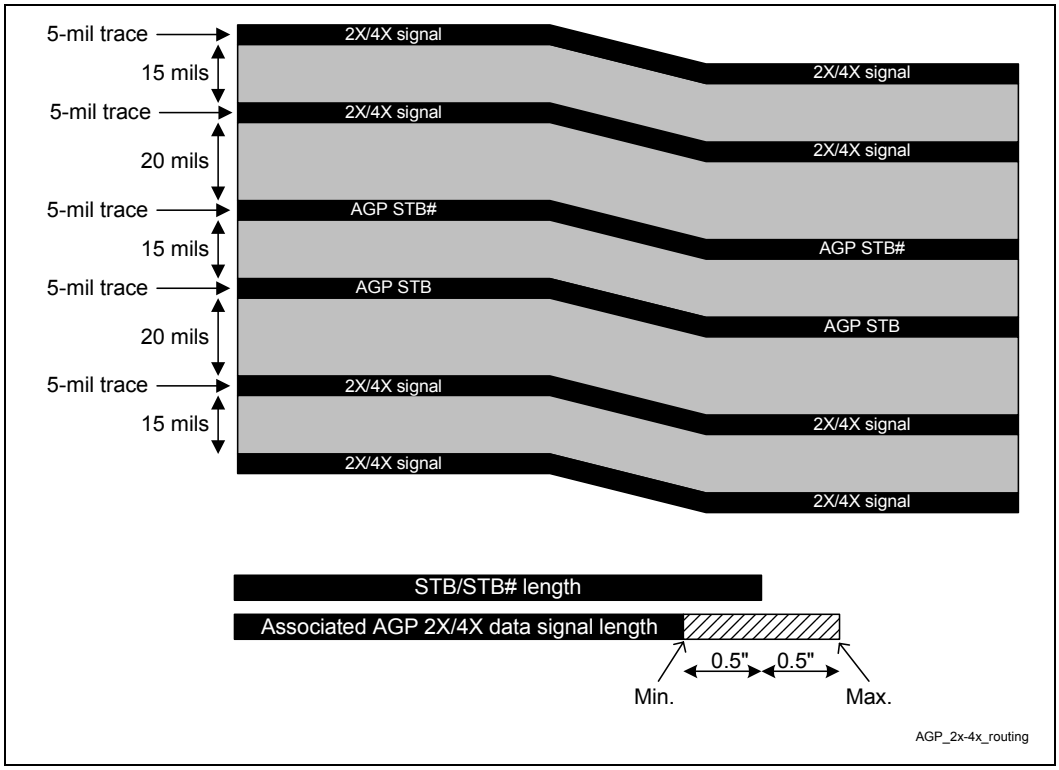
7.3.2 2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to ALL signals listed in Table 22 as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

The maximum line length and length mismatch requirements depend on the routing rules used on the motherboard. These routing rules were created to provide design freedom by making trade-offs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6 inches) and long AGP interfaces (e.g., > 6 inches and < 7.25 inches) are documented

separately. The maximum length allowed for the AGP interface on external AGP card motherboards is 7.25 inches.

Figure 51. AGP 2X/4X Routing Example for Interfaces < 6 inches and GPA/AGP Solutions



7.3.2.1 External AGP Card Motherboard Guidelines

For motherboards that will use an external AGP card in the AGP slot, the maximum AGP 2X/4X signal trace length is 7.25 inches. However, there are different guidelines for AGP interfaces shorter than 6 inches (e.g., all AGP 2X/4X signals are shorter than 6 inches) and those longer than 6 inches but shorter than the 7.25 inches maximum.

AGP Interfaces Shorter Than 6 Inches

The following guidelines are for designs that require less than 6 inches between the AGP connector and the MCH:

- 1:3 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 22), within ±0.5 inch.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 4.8 inches to 5.8 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 3.7 inches to 4.7 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1 inches (i.e., a strobe and its complement must be the same length, within 0.1 inches). Refer to Table 22 for an illustration of these requirements.

AGP Interfaces Longer Than 6 inches

Since longer lines have more crosstalk, they require wider spacing between traces to reduce the skew. The following guidelines are for designs that require more than 6 inches (but less than the 7.25 inches max.) between the AGP connector and the MCH:

- 1:4 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 22), within ±0.125 inches.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 6.475 inches to 6.625 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 6.075 inches to 6.325 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1 inch (i.e., a strobe and its complement must be the same length, within 0.1 inch).

7.3.3 AGP Routing Guideline Considerations and Summary

This section applies to all AGP signals in any motherboard support configuration (e.g., “external AGP card”):

- The 2X/4X timing domain signals can be routed with 5 mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.3 inches of the MCH package.
- When matching trace lengths for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.
- Reduce line length mismatch to ensure added margin. The trace length mismatch for all signals within a signal group should be as close as possible to zero, to provide timing margin.
- To reduce trace-to-trace coupling (i.e., crosstalk), separate the traces as much as possible.
- All signals in a signal group should be routed on the same layer.
- The trace length and trace spacing requirements **must not** be violated by any signal.

Table 24. AGP 2.0 Routing Summary

Signal	Maximum Length	Trace Spacing (5 Mil Traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	7.5" [4]	5 mils	No requirement	N/A	None
2X/4X Timing Domain Set 1	7.25" [4]	20 mils	±0.125"	AD_STB0 and AD_STB0#	AD_STB0 and AD_STB0# must be the same length.
2X/4X Timing Domain Set 2	7.25" [4]	20 mils	±0.125"	AD_STB1 and AD_STB1#	AD_STB1 and AD_STB1# must be the same length.
2X/4X Timing Domain Set 3	7.25"[4]	20 mils	±0.125"	SB_STB and SB_STB#	SB_STB and SB_STB# must be the same length.
2X/4X Timing Domain Set 1	6" [3]	15 mils[1]	±0.5"	AD_STB0 and AD_STB0#	AD_STB0 and AD_STB0# must be the same length.
2X/4X Timing Domain Set 2	6"[3]	15 mils[1]	±0.5"	AD_STB1 and AD_STB1#	AD_STB1 and AD_STB1# must be the same length.
2X/4X Timing Domain Set 3	6"[3]	15 mils[1]	±0.5"	SB_STB and SB_STB#	SB_STB and SB_STB# must be the same length.

NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils.
2. These guidelines apply to board stack-ups with 15% impedance tolerance.
3. 4 inches is the maximum length for flexible motherboards.
4. Solution valid for AGP-only motherboards

7.3.4 AGP Clock Routing

The maximum total AGP clock skew, between the MCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but also at all points on a clock edge that falls within in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew. (The motherboard designer must determine how the 0.9 ns is allocated between the board and the synthesizer.)

For the 815EP universal platform's AGP clock routing guidelines, refer to Section 11.3.

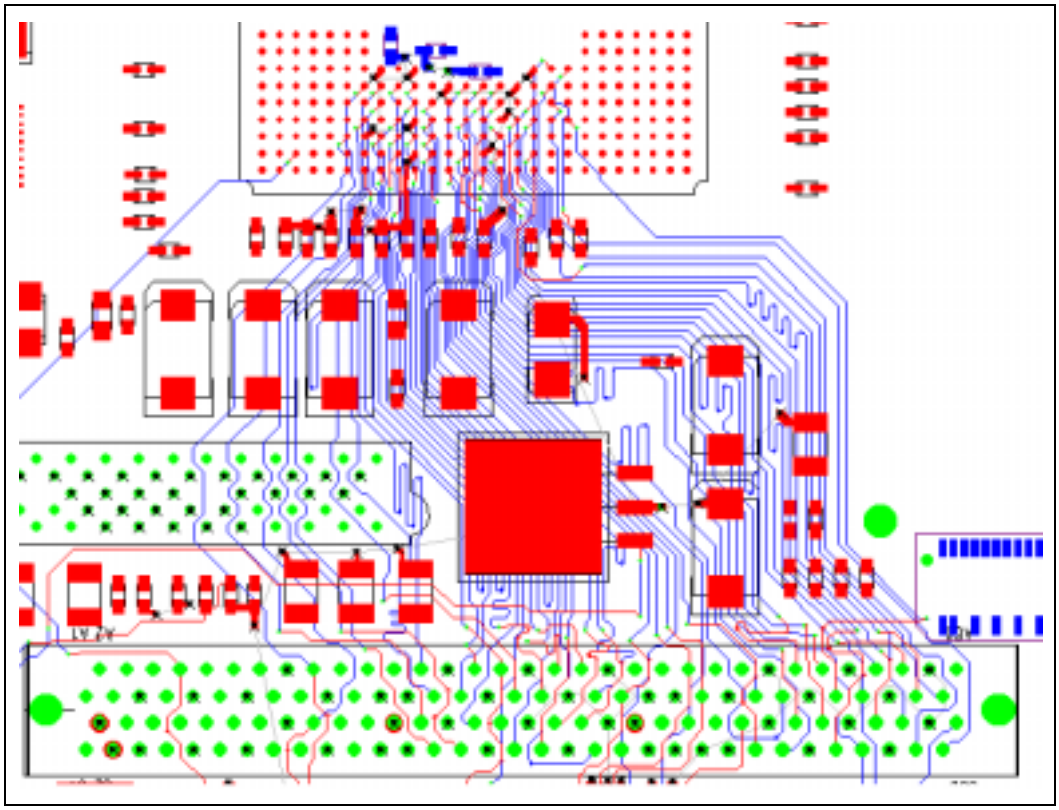
7.3.5 AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for an optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the MCH. The following guidelines are not intended to replace thorough system validation of products based on the 815EP chipset platform:

- A minimum of six 0.01 µF capacitors are required and must be as close as possible to the MCH. These should be placed within 70 mils of the outer row of balls on the MCH for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute the placement of decoupling capacitors within the AGP interface signal field.
- It is recommended that the designer use a low-ESL ceramic capacitor (e.g., a 0603 body-type X7R dielectric)
- To add the decoupling capacitors within 70 mils of the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of the space between traces should be minimal and for as short a distance as possible (1 inch max.).
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. *In a typical four-layer PCB design, the signals transition from one side of the board to the other.* One extra 0.01 µF capacitor is required per 10 vias. The capacitor should be placed as close as possible to the center of the via field.

The designer should ensure that the AGP connector is well decoupled, as described in the *AGP Design Guide,* Revision 1.0, Section 1.5.3.3.

Figure 52. AGP Decoupling Capacitor Placement Example



NOTE: This figure is for example purposes only. It does not necessarily represent complete and correct routing for this interface.

7.3.6 AGP Routing Ground Reference

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector (or to an AGP video controller if implemented as a "down" solution on an AGP-only motherboard), using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the minimum signal set listed previously, it is strongly recommended that half of all AGP signals be reference to ground, depending on board layout. In an ideal design, the entire AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all designs using the 815EP chipset platform.

7.4 AGP Down Routing Guidelines

The routing guidelines in this section are for AGP down implementations with AGP-compliant devices that are implemented directly on the motherboards, eliminating the need for connectors or add-in cards.

7.4.1 1X AGP Down Option Timing Domain Routing Guidelines

Routing guidelines for an AGP device on the motherboard are very similar to those when the device is implemented with an AGP connector.

- AGP 1X timing domain signals (Table 22) have a maximum trace length of 7.5 inches. This maximum applies to ALL signals listed as 1X timing domain signals in Table 25.
- All AGP 1X timing domain signals can be routed with 5 mil minimum trace separation
- There are no trace length matching requirements for 1X timing domain signals

7.4.2 2X/4X AGP Down Timing Domain Routing Guidelines

These trace length guidelines apply to ALL signals listed in Table 22 as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

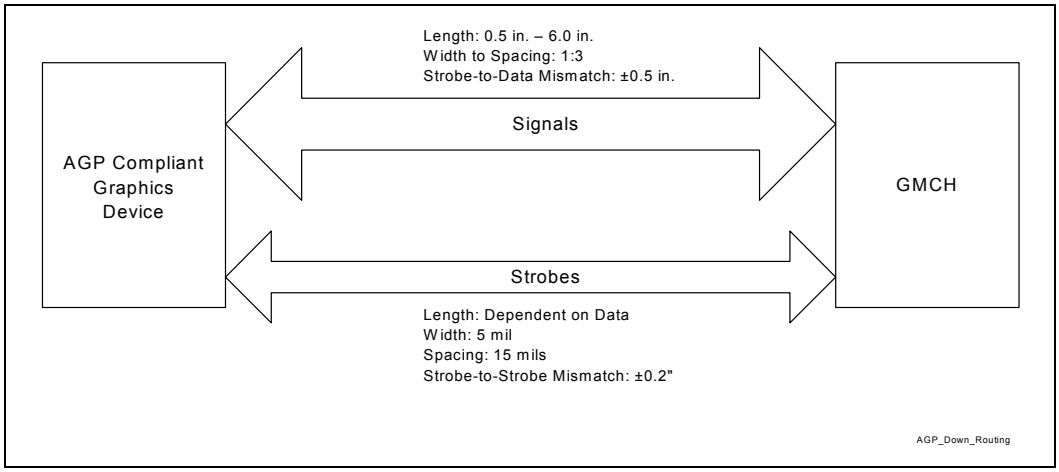
- The maximum AGP 2X/4X signal trace length is 6 inches.
- 1:3 trace width-to-spacing is required for AGP 2X/4X timing domain signal traces.
- AGP 2X/4X signals must be matched with their associated strobe (as outlined in Table 22), within ±0.5 inch.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) is 5.3 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) could be 4.8 inches to 5.8 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) could be 3.7 inches to 4.7 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be

routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals and all other signals by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.2 inch (i.e., a strobe and its complement must be the same length, within 0.2 inch).

Figure 53. AGP Down 2X/4X Routing Recommendations



7.4.3 AGP Routing Guideline Considerations and Summary

This section applies to all AGP signals, as follows:

- The 2X/4X timing domain signals can be routed with 5 mil spacing when breaking out of the MCH. The routing must widen to the documented requirements, within 0.3 inch of the MCH package.
- When matching the trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the ball on the AGP compliant device. It is not necessary to compensate for the lengths of the AGP signals on the MCH package.
- Reduce line length mismatch to ensure added margin. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.
- To reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible.
- All signals in a signal group should be routed on the same layer.
- The trace length and trace spacing requirements **must not** be violated by any signal.

Table 25. AGP 2.0 Down Routing Summary

Signal	Max. Length	Trace Spacing (5 mil Traces)	Length Mismatch	Relative to	Notes
1X Timing Domain	7.5”	5 mils	No requirement	N/A	None
2X/4X Timing Domain Set 1	6”	15 mils[1]	±0.5”	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set 2	6”	15 mils[1]	±0.5”	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set 3	6”	15 mils[1]	±0.5”	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils.

7.4.4 AGP Clock Routing

The maximum total AGP clock skew, between the MCH and the graphics component, is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but at all points on the clock edge that fall within the switching range. For AGP clock routing guidelines for the 815EP chipset platform, refer to Section 11.3.

7.4.5 AGP Signal Noise Decoupling Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the MCH. The following guidelines are not intended to replace thorough system validation for products based on the 815EP chipset platform.

- A minimum of six 0.01 µF capacitors are required and must be as close as possible to the MCH. These should be placed within 70 mils of the outer row of balls on the MCH for VDDQ decoupling. The closer the placement, the better.
- The designer should evenly distribute placement of decoupling capacitors in the AGP interface signal field.
- It is recommended that the designer use a low-ESL ceramic capacitor, such as with a 0603 body-type X7R dielectric.
- To add the decoupling capacitors within 70 mils of the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1 inch max.).
- In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition the AGP signal from one reference signal plane to another. On a typical four-layer PCB design, the signals transition from one side of the board to the other. One extra 0.01 µF capacitor is required per ten vias. The capacitor should be placed as close as possible to the center of the via field.

7.4.6 AGP Routing Ground Reference

It is strongly recommended that at least the following critical signals be referenced to ground from the MCH to an AGP video controller on an AGP-only motherboard using a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to this minimum signal set, it is strongly recommended that half of all AGP signals be referenced to ground, depending on the board layout. In an ideal design, the complete AGP interface signal field would be referenced to ground. This recommendation is not specific to any particular PCB stack-up, but should be applied to all 815EP chipset platform designs.

7.5 AGP 2.0 Power Delivery Guidelines

7.5.1 VDDQ Generation and TYPEDET#

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. This voltage is **always** 3.3 V. VDDQ is the interface voltage. In AGP 1.0 implementations, VDDQ also was 3.3 V. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ, since both are tied to the 3.3 V power plane on the motherboard.

AGP 2.0 requires that these power planes be separate. In conjunction with the 4X data rate, the AGP 2.0 Interface Specification provides for low-voltage (1.5 V) operation. The AGP 2.0 specification implements a TYPEDET# (type detect) signal on the AGP connector that determines the operating voltage of the AGP 2.0 interface (VDDQ). The motherboard must provide either 1.5 V or 3.3 V to the add-in card, depending on the state of the TYPEDET# signal (see Table 26). 1.5 V low-voltage operation applies **only** to the AGP interface (VDDQ). VCC is always 3.3 V.

Note: The motherboard provides 3.3 V to the VCC pins of the AGP connector. If the graphics controller needs a lower voltage, then the add-in card must regulate the 3.3VCC voltage to the controller's requirements. The graphics controller may **only** power AGP I/O buffers with the VDDQ power pins.

The TYPEDET# signal indicates whether the AGP 2.0 interface operates at 1.5 V or 3.3 V. If TYPEDET# is floating (i.e., No Connect) on an AGP add-in card, the interface is 3.3 V. If TYPEDET# is shorted to ground, the interface is 1.5 V.

Table 26. TYPDET#/VDDQ Relationship

TYPEDET# (on Add-in Card)	VDDQ (Supplied by MB)
GND	1.5 V
N/C	3.3 V

As a result of this requirement, the motherboard must provide a *flexible* voltage regulator or key the slot to preclude add-in cards with voltage requirements incompatible with the motherboard. This regulator must supply the appropriate voltage to the VDDQ pins on the AGP connector. For specific design recommendations, refer to the schematics in Appendix A. VDDQ generation and

AGP VREF generation must be considered together. Before developing VDDQ generation circuitry, refer to Section 7.5.1 and the *AGP 2.0 Interface Specification*.

Figure 54. AGP VDDQ Generation Example Circuit

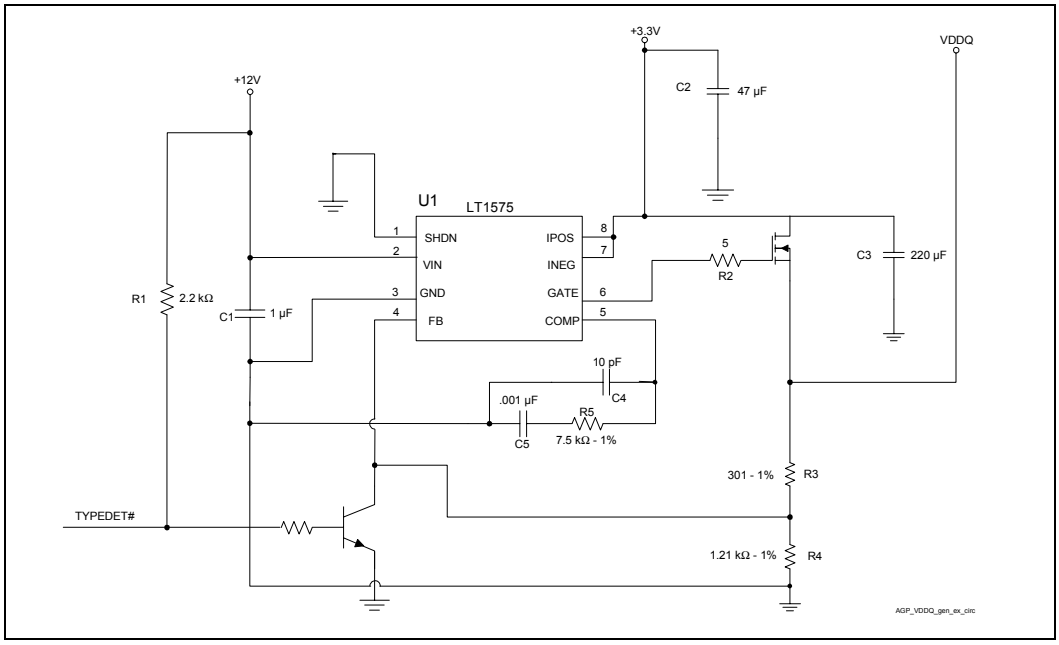


Figure 54 demonstrates **one** way to design the VDDQ voltage regulator. This regulator is a linear regulator with an external, low-Rds_{on} FET. The source of the FET is connected to 3.3 V. This regulator converts 3.3 V to 1.5 V or passes 3.3 V, depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3 V (not 5 V) to control thermals. (i.e., 5 V regulated down to 1.5 V with a linear regulator will dissipate approximately 7 W at 2 A.) Because it must draw power from 3.3 V and, in some situations, must simply pass that 3.3 V to VDDQ (when a 3.3 V add-in card is placed in the system), the regulator MUST use a low-Rds_{on} FET.

AGP 1.0 ECR #44 modified VDDQ 3.3_{min} to 3.1 V. When an ATX power supply is used, the 3.3 V_{min} is 3.168. Therefore, 68 mV of drop is allowed across the FET at 2 A. This corresponds to an FET with an Rds_{on} of 34 mΩ.

How does the regulator switch? The feedback resistor divider is set to 1.5 V. When a 1.5 V card is placed in the system, the transistor is off and the regulator regulates to 1.5 V. When a 3.3 V card is placed in the system, the transistor is on, and the feedback will be pulled to ground. When this happens, the regulator will drive the gate of the FET to nearly 12 V. This will turn on the FET and pass 3.3 V – 2 A * Rds_{on} to VDDQ.

7.5.2 VREF Generation for *AGP* 2.0 (2X and 4X)

VREF generation for AGP 2.0 is different, depending on the AGP card type used. The 3.3 V AGP cards generate VREF locally. That is, they have a resistor divider on the card that divides VDDQ down to VREF (see Figure 55). To account for potential differences between VDDQ and GND at the MCH and graphics controller, 1.5 V cards use source-generated VREF. That is, the VREF signal is generated at the graphics controller and sent to the MCH, and another VREF is generated at the MCH and sent to the graphics controller (see Figure 55).

Both the graphics controller and the MCH must generate VREF and distribute it through the connector (1.5 V add-in cards only). The following two pins defined on the AGP 2.0 universal connector allow this VREF passing:

- VREFGC VREF from the graphics controller to the chipset
- VREFCG VREF from the chipset to the graphics controller

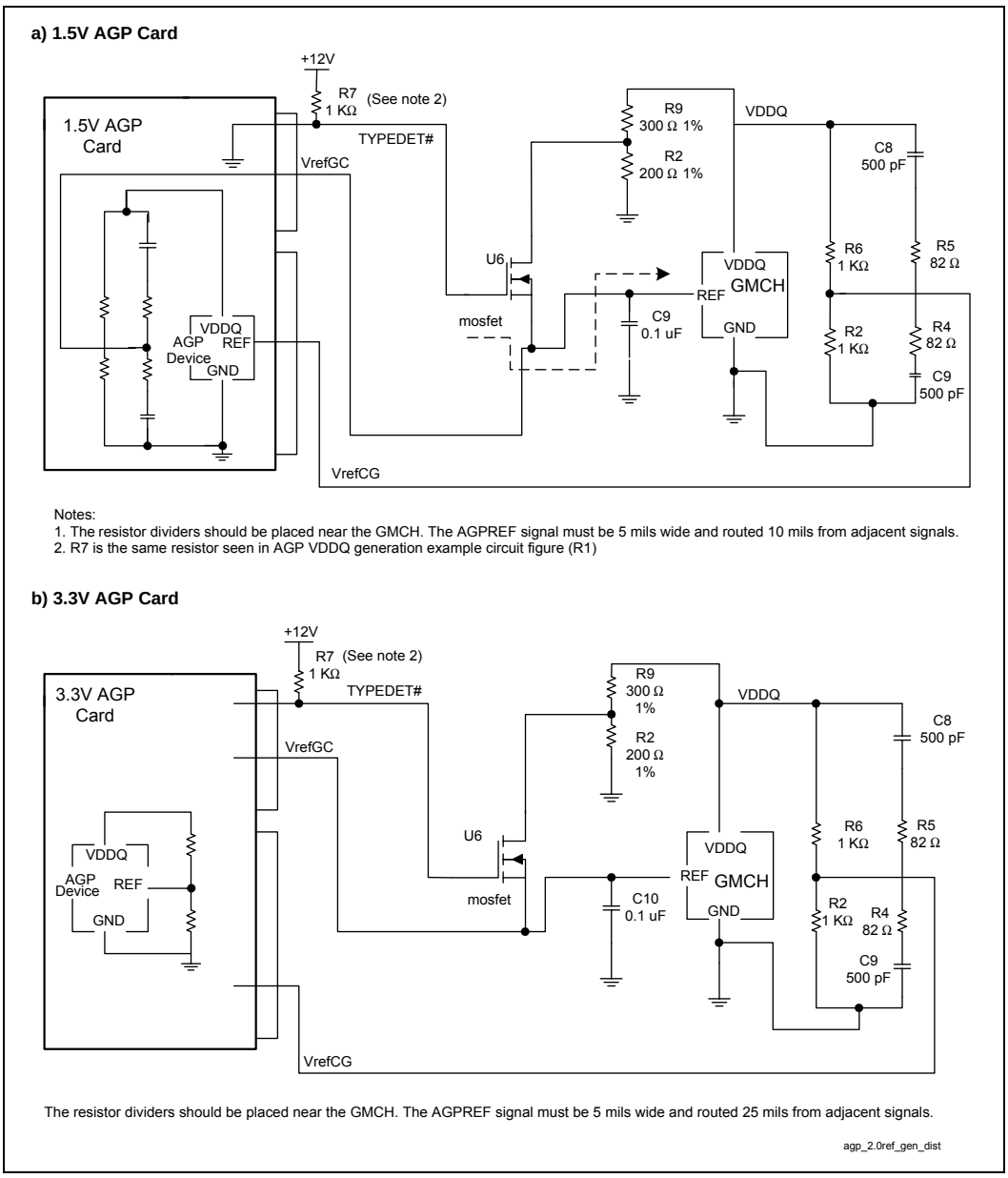
To preserve the common-mode relationship between the VREF and data signals, the routing of the two VREF signals must be matched in length to the strobe lines, within 0.5 inch on the motherboard and within 0.25 inch on the add-in card.

The voltage divider networks consist of AC and DC elements, as shown in Figure 55.

The VREF divider network should be placed as close as practical to the AGP interface, to get the benefit of the common-mode power supply effects. However, the trace spacing around the VREF signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity.

During 3.3 V AGP 2.0 operation, VREF must be 0.4 VDDQ. However, during 1.5 V AGP 2.0 operation, VREF must be 0.5 VDDQ. This requires a flexible voltage divider for VREF. Various methods of accomplishing this exist, and one such example is shown in Figure 55.

Figure 55. AGP 2.0 VREF Generation and Distribution



The flexible VREF divider shown in Figure 55 uses a FET switch to switch between the locally generated VREF (for 3.3 V add-in cards) and the source-generated VREF (for 1.5 V add-in cards).

Use of the source-generated VREF at the receiver is optional and is a product implementation issue beyond the scope of this document.

7.6 Additional AGP Design Guidelines

7.6.1 Compensation

The MCH AGP interface supports resistive buffer compensation (RCOMP). Tie the GRCOMP pin to a 40 Ω, 2% (or 39 Ω, 1%) pull-down resistor (to ground) through a 10 mil-wide, very short (<0.5 inch) trace.

7.6.2 AGP Pull-Ups

AGP control signals require pull-up resistors to VDDQ on the motherboard, to ensure that they contain stable values when no agent is actively driving the bus. The pull-up/pull-down resistor value requirements are Rmin = 4 kΩ and Rmax = 16 kΩ. The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

1X Timing Domain Signals Requiring Pull-Up Resistors

The following bullets list the 1X timing domain signals that require pull-up resistors.

- FRAME#
- TRDY#
- IRDY#
- DEVSEL#
- STOP#
- SERR#
- ST[2:0]
- PERR#
- RBF#
- PIPE#
- REQ#
- WBF#
- GNT#

Note: It is **critical** that these signals be pulled up to VDDQ, not 3.3 V.

The trace stub to the pull-up resistor on 1X timing domain signals should be kept shorter than 0.5 inch to avoid signal reflections from the stub.

Note: INTA# and INTB# should be pulled to 3.3 V, not VDDQ.

2X/4X Timing Domain Signals Requiring Pull-Up/Pull-Down Resistors

The following bullets list the 2X/4X timing domain signals that require pull-up/pull-down resistors. The strobe signals require pull-up/pull-downs on the motherboard to ensure that they are at a stable level when no agent is driving the bus.

- AD_STB[1:0] Pull-up to VDDQ
- SB_STB Pull-up to VDDQ
- AD_STB[1:0]# Pull-down to Ground
- SB_STB# Pull-down to Ground

The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept shorter than 0.1 inch to avoid signal reflections from the stub.

7.6.2.1 AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3 V tolerant during 1.5 V operation:

- PME#
- INTA#
- INTB#
- GPERR#
- GSERR#
- CLK
- RST

The following signals on the AGP interface are 5 V tolerant (see USB specification):

- USB+
- USB-
- OVRCNT#

The following signal is a special AGP signal. It is either grounded or left as a no connect on an AGP card.

- TYPEDET#

Note: All other signals on the AGP interface are in the VDDQ group. They are not 3.3 V tolerant during 1.5 V AGP operation!

7.7 Motherboard / Add-in Card Interoperability

There are three AGP connectors: *3.3 V AGP connector, 1.5 V AGP connector*, and *Universal AGP connector*. To maximize add-in flexibility, it is highly advisable to implement the universal connector in systems based on the 815EP platform. All add-in cards are *either* 3.3 V or 1.5 V cards. The 4X transfers at 3.3 V are not allowed due to timings.

Table 27. Connector/Add-in Card Interoperability

Card	1.5 V Connector	3.3 V Connector	Universal Connector
1.5 V card	Yes	No	Yes
3.3 V card	No	Yes	Yes

Table 28. Voltage/Data Rate Interoperability

Voltage	1X	2X	4X
1.5 V VDDQ	Yes	Yes	Yes
3.3 V VDDQ	Yes	Yes	No

8 Hub Interface

The MCH ball assignment and ICH2 ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals be routed directly from the MCH to the ICH2 on the top signal layer. Refer to Figure 56.

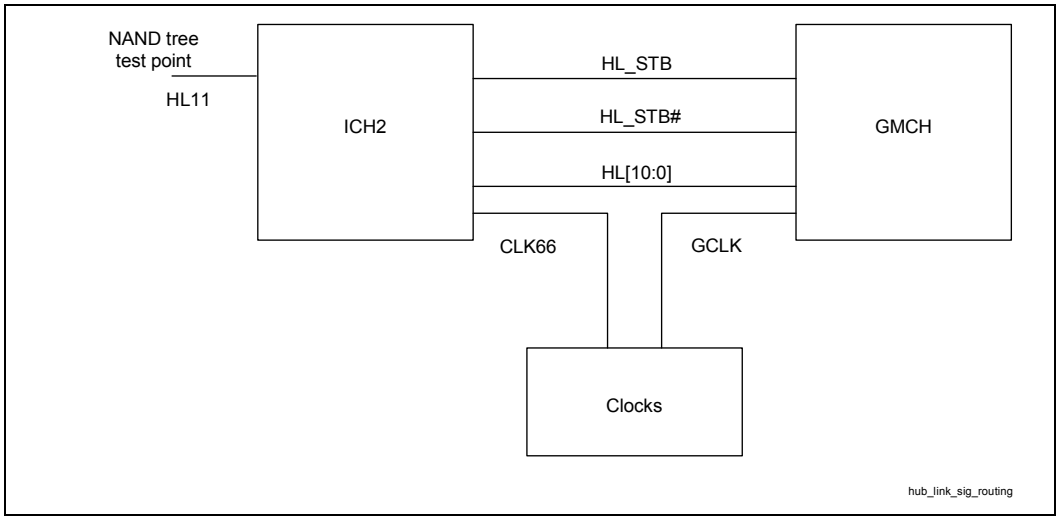
The hub interface is divided into two signal groups: data signals and strobe signals.

- Data Signals:
  - HL[10:0]
- Strobe Signals:
  - HL_STB
  - HL_STB#

Note: HL_STB/HL_STB# is a differential strobe pair.

No pull-ups or pull-downs are required on the hub interface. HL11 on the ICH2 should be brought out to a test point for NAND Tree testing. Each signal should be routed such that it meets the guidelines documented for its signal group.

Figure 56. Hub Interface Signal Routing Example



8.1.1 Data Signals

Hub interface data signals should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the MCH and the ICH2, the hub interface data signals can be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals should be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the MCH/ICH2 components.

The maximum trace length for the hub interface data signals is 8 inches. These signals should each be matched within ±0.1 inch of the HL_STB and HL_STB# signals.

8.1.2 Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 8 inches, and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes, within ±0.1 inch.

8.1.3 HREF Generation/Distribution

HREF, the hub interface reference voltage, is 0.5 * 1.85 V = 0.92 V ± 2%. It can be generated using a single HREF divider or locally generated dividers (as shown in Figure 57 and Figure 58). The resistors should be equal in value and rated at 1% tolerance, to maintain 2% tolerance on 0.92 V. The values of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from a minimum of 100 Ω to a maximum of 1 kΩ (300 Ω shown in example).

The single HREF divider should not be located more than 4 inches away from either MCH or ICH2. If the single HREF divider is located more than 4 inches away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor must be close to the component HREF pin.

8.1.4 Compensation

Independent hub interface compensation resistors are used by the MCH and ICH2 to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH) for use with the Universal Socket 370* Datasheet and the *Intel® 82801BA I/O Controller Hub* (ICH2) *and Intel® 82801BAM I/O Controller Hub* (ICH2-M) Datasheet for details on compensation. The resistive Compensation (RCOMP) guidelines are as follows:

- **RCOMP:** Tie the HLCOMP pin of each component to a 40 Ω, 1% or 2% pull-up resistor (to 1.8 V) via a 10 mil-wide, 0.5 inch trace (targeted at a nominal trace impedance of 40 Ω). The MCH and ICH2 each requires its own RCOMP resistor.

Figure 57. Single Hub Interface Reference Divider Circuit

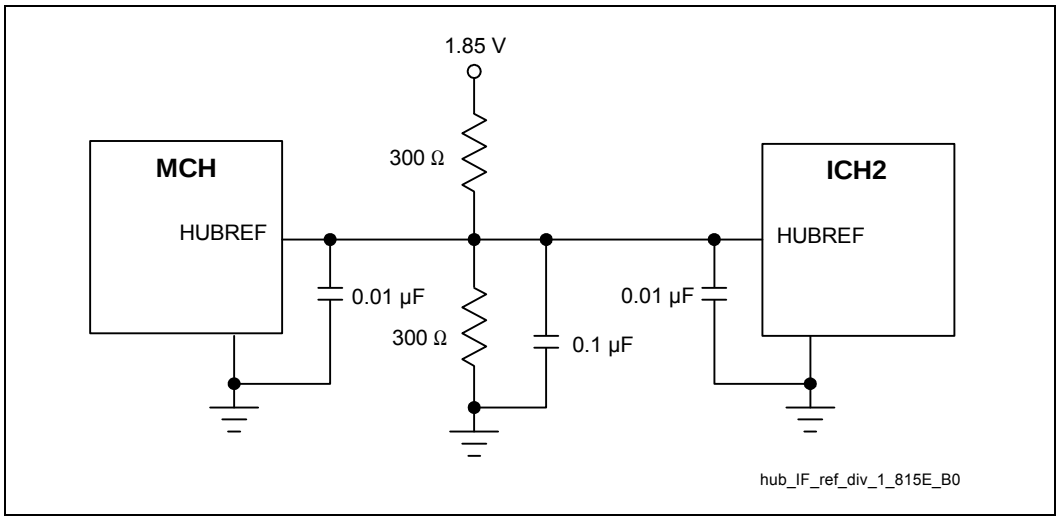
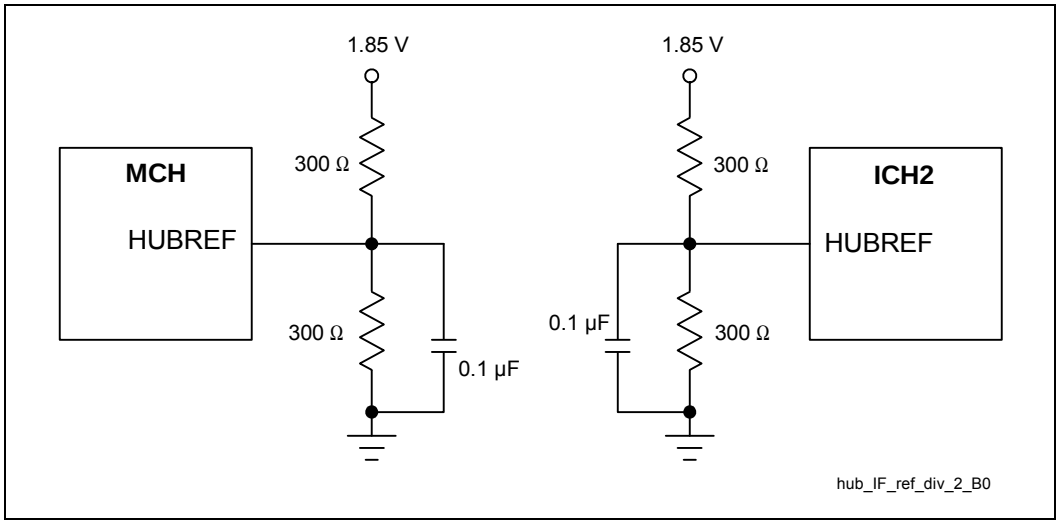


Figure 58. Locally Generated Hub Interface Reference Dividers



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9 I/O Controller Hub 2 (ICH2)

9.1 Decoupling

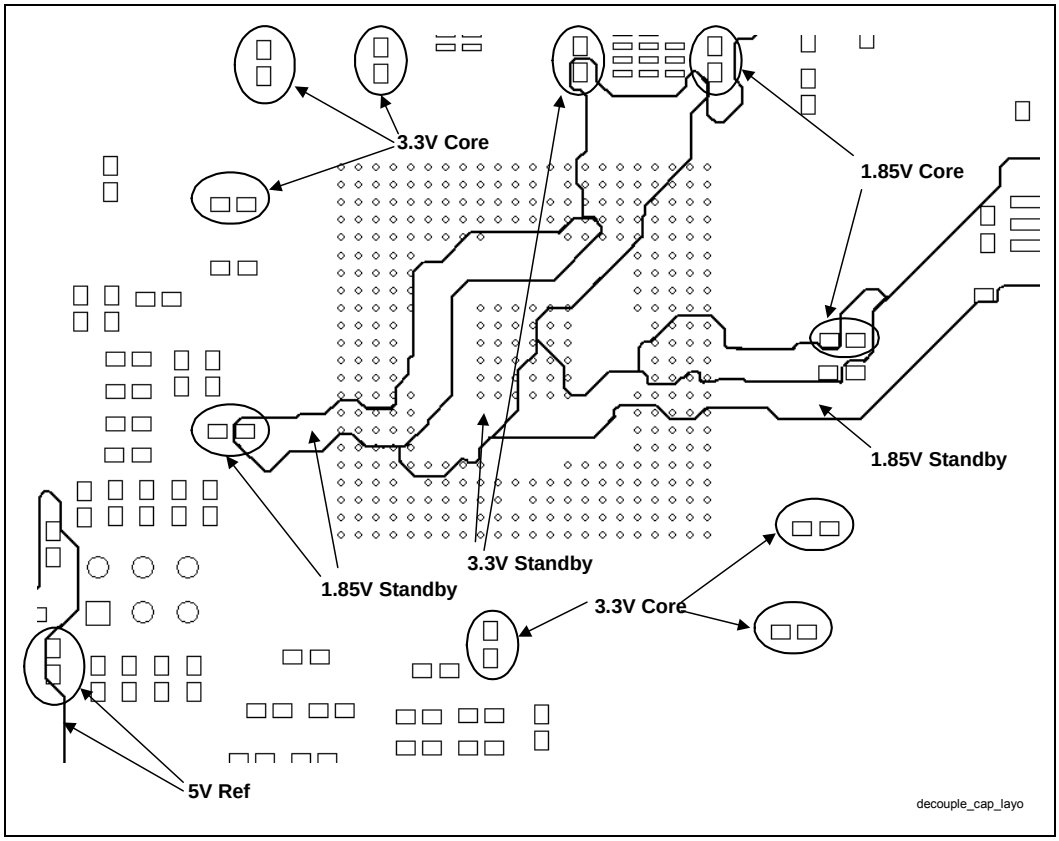
The ICH2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 29 to ensure that the component maintains stable supply voltages. The capacitors should be placed as close as possible to the package, without exceeding 400 mils (200 mils nominal).

Note: Routing space around the ICH2 is tight. A few decoupling caps may be placed more than 300 mils away from the package. System designers should simulate the board to ensure that the correct amount decoupling is implemented. Refer to Figure 59 for a layout example, with the decoupling capacitors circled with an arrow showing which power plane/trace they are connected to. Intel recommends that, for prototype board designs, the designer include pads for extra power plane decoupling capacitors.

Table 29. Decoupling Capacitor Recommendation

Power Plane/Pins	Decoupling Capacitors	Capacitor Value
3.3 V core	6	0.1 µF
3.3 V standby	1	0.1 µF
Processor interface (1.3 ~ 2.5 V)	1	0.1 µF
1.85 V core	2	0.1 µF
1.85 V standby	1	0.1 µF
5 V reference	1	0.1 µF
5 V reference standby	1	0.1 µF

Figure 59. Intel® ICH2 Decoupling Capacitor Layout



9.2 Power Sequencing on Wake Events

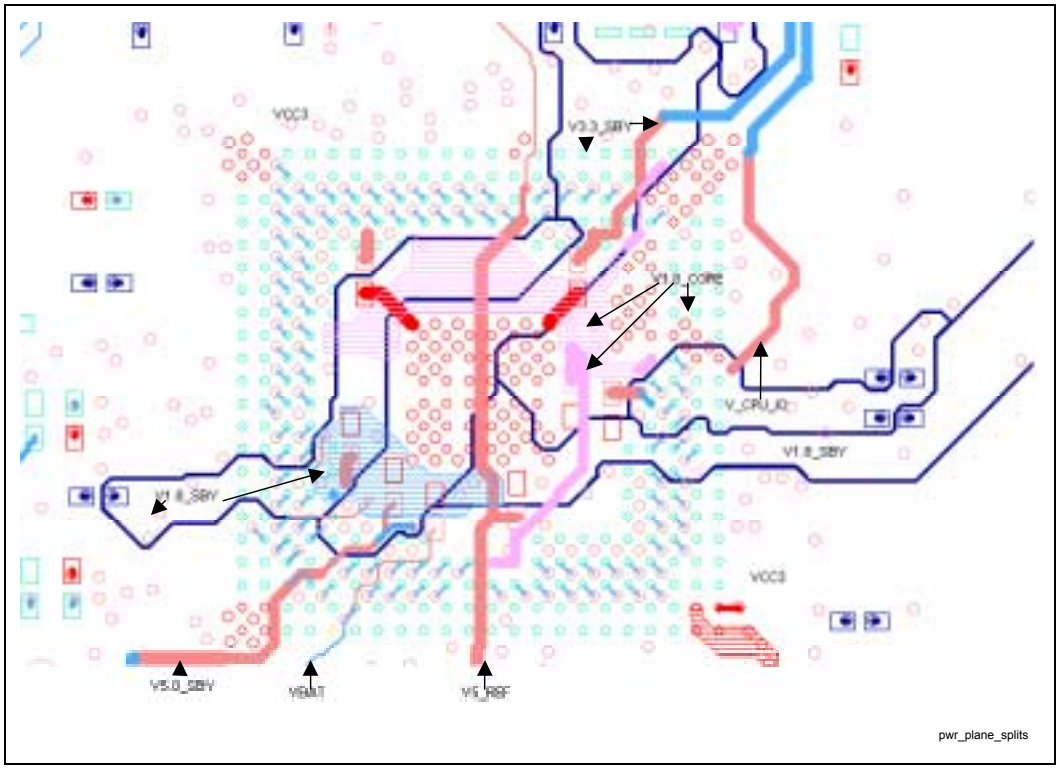
For systems providing functionality with future 0.13 micron socket 370 processors, special handling of wake events is required. When a wake event is triggered, the MCH and the CK-815 must not sample BSEL[1:0] until the signal VTTPWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the CK-815-compliant clock driver until schematic signal VTTPWRGD12 is asserted.
2. Clocks to the ICH2 stabilize before the power supply asserts PWROK to the ICH2. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus, it is necessary to gate PWROK to the ICH2 from the power supply while the CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.
3. ICH2 takes the MCH out of reset.
4. MCH samples BSEL[1:0]. (CK-815 will have sampled BSEL[1:0] much earlier.)

Refer to Section 4.3 for full implementation details.

9.3 Power Plane Splits

Figure 60. Power Plane Split Example



9.4 Power Supply PS_ON Considerations

- If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.
- The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).
- The platform designer must ensure that the power supply used with the platform is not affected by this issue.

10 I/O Subsystem

This chapter provides guidelines for connecting and routing the IDE, AC '97, USB, I/O APIC, SMBus, PCI, LPC/FWH, and RTC subsystems.

10.1 IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement and signal termination for both IDE channels. The ICH2 has integrated the series resistors that typically have been required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. Intel does not anticipate requiring additional series termination, but OEMs should verify the motherboard signal integrity via simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by providing future stuffing options.

The IDE interface can be routed with 5 mil traces on 7 mil spaces and must be less than 8 inches long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inch shorter than the longest IDE signal (on that channel).

10.1.1 Cabling

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the connector next closest to the end of the cable (6 inches away from the end of the cable).
- **Grounding:** Provide a direct, low-impedance chassis path between the motherboard ground and hard disk drives.
- **ICH2 Placement:** The ICH2 must be placed at most 8 inches from the ATA connector(s).

10.2 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE controller supports PIO, multiword (8237-style) DMA, and Ultra DMA modes 0 through 5. The ICH2 must determine the type of cable present, to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal' etc. All ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms

to the Small Form Factor Specification SFF-8049, which is obtainable from the Small Form Factor Committee.

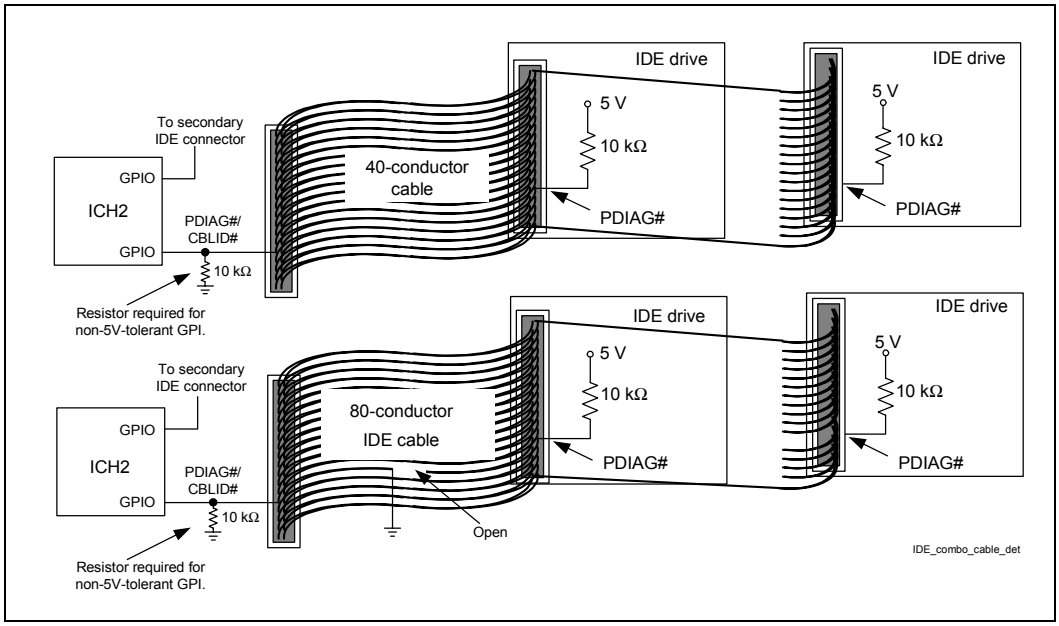
To determine whether the ATA/66 or ATA/100 mode can be enabled, the ICH2 requires that the system software attempt to determine the type of cable used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination host-side/device-side detection mechanism. Note that host-side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the device-side detection mechanism only.

10.2.1 Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the *ATA/ATAPI-4 Standard*, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 61. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. Not all GPI and GPIO pins on the ICH2 are 5 V tolerant. If non 5 V tolerant inputs are used, a resistor divider is required to prevent 5 V on the ICH2 or FWH pins. The proper value of the divider resistor is 10 kΩ (as shown in Figure 61).

Figure 61. Combination Host-Side / Device-Side IDE Cable Detection



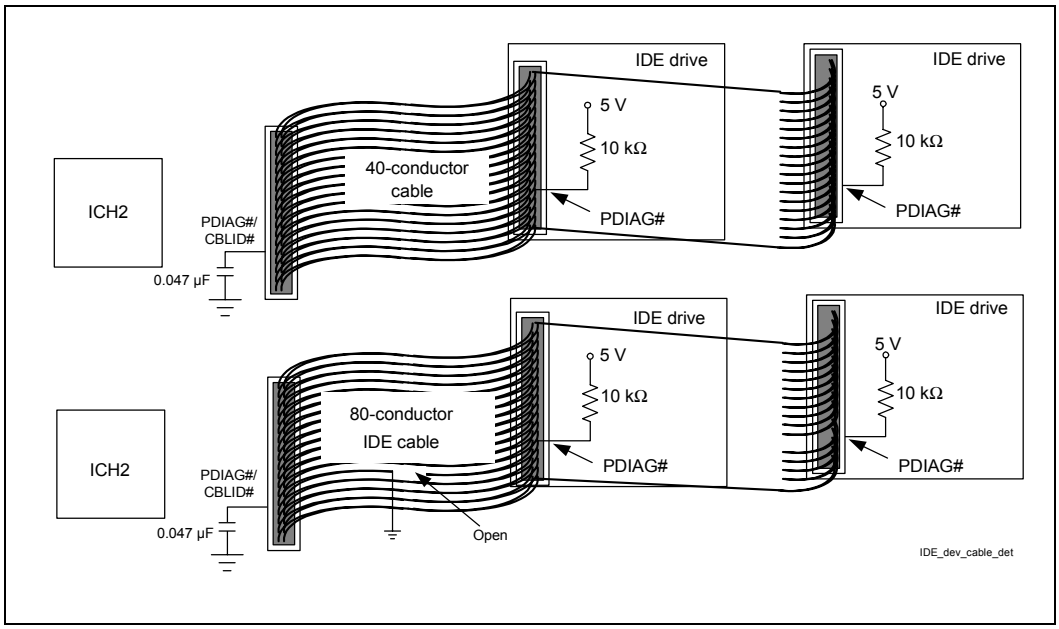
This mechanism allows BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is High, then there is 40-conductor cable in the system and ATA modes 3, 4 and 5 must not be enabled.

If PDIAG#/CBLID# is detected Low, then there may be an 80-conductor cable in the system or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the **Identify Device** information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13, is set to 1, then an 80-conductor cable is present. If this bit is set to 0, then a legacy slave (Device 1) is preventing proper cable detection, so BIOS should configure the system as though a 40-conductor cable were present and then notify the user of the problem.

10.2.2 Device-Side Cable Detection

For platforms that must implement device-side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 62. This capacitor **should not be populated** when implementing the recommended combination host-side/device-side cable detection mechanism described previously.

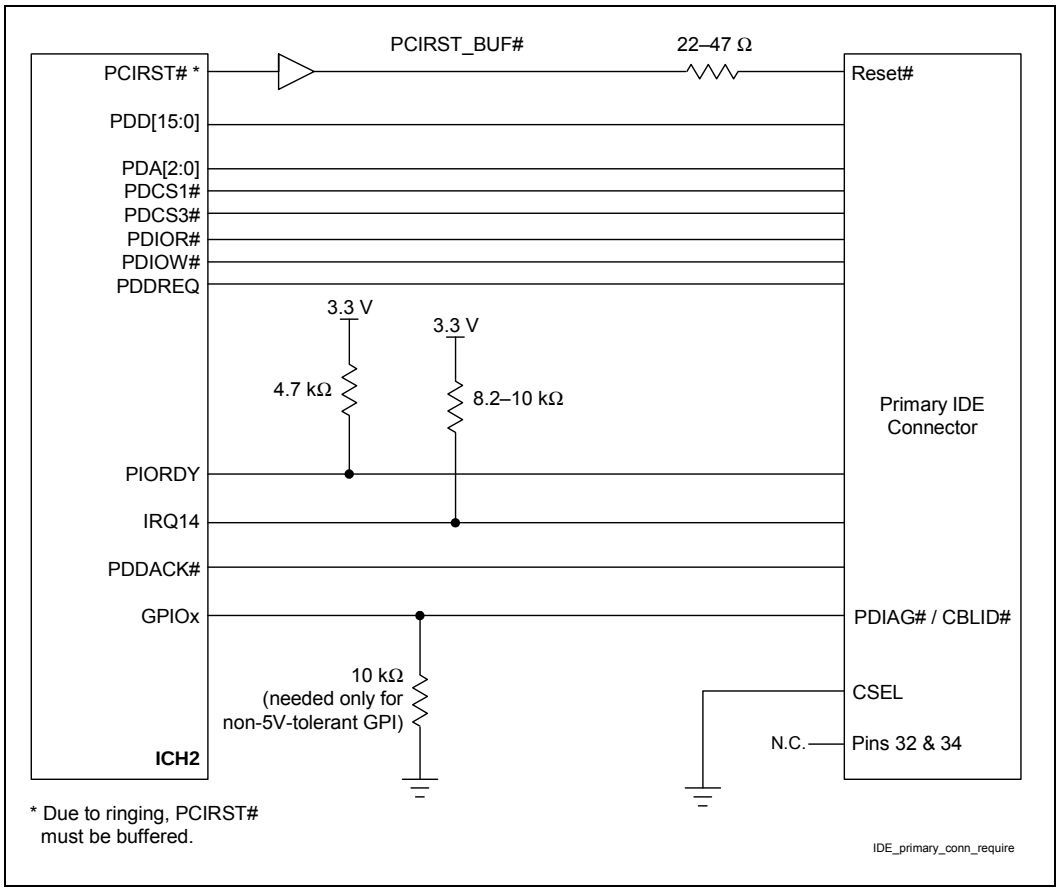
Figure 62. Device-Side IDE Cable Detection



This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4 or 5 drive will drive PDIAG#/CBLID# Low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host, so the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host, so the signal will rise more slowly as the capacitor charges. The drive can detect the difference in rise times and will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot, as described in the ATA/66 specification.

10.2.3 Primary IDE Connector Requirements

Figure 63. Connection Requirements for Primary IDE Connector

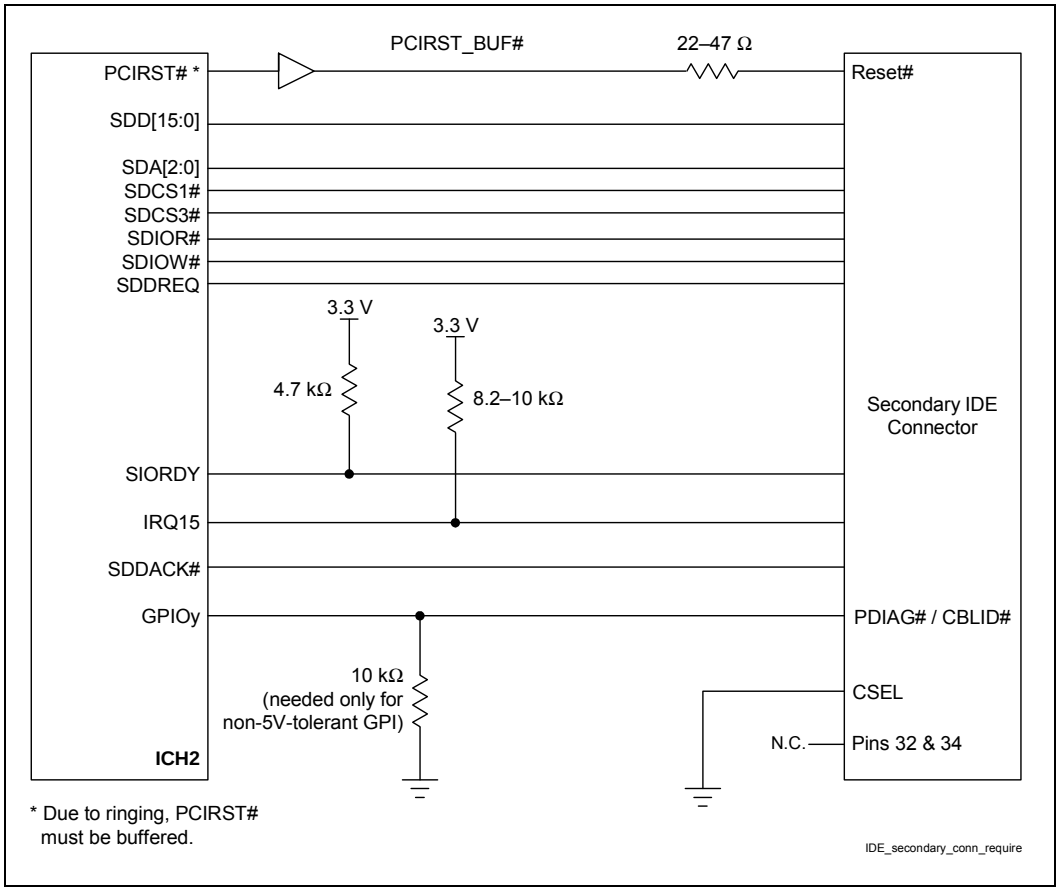


NOTES:

1. 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.
3. A 4.7 kΩ pull-up resistor to VCC3 is required on PIORDY and SIORDY.
4. Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close as possible to the connector. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

10.2.4 Secondary IDE Connector Requirements

Figure 64. Connection Requirements for Secondary IDE Connector



NOTES:

1. 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
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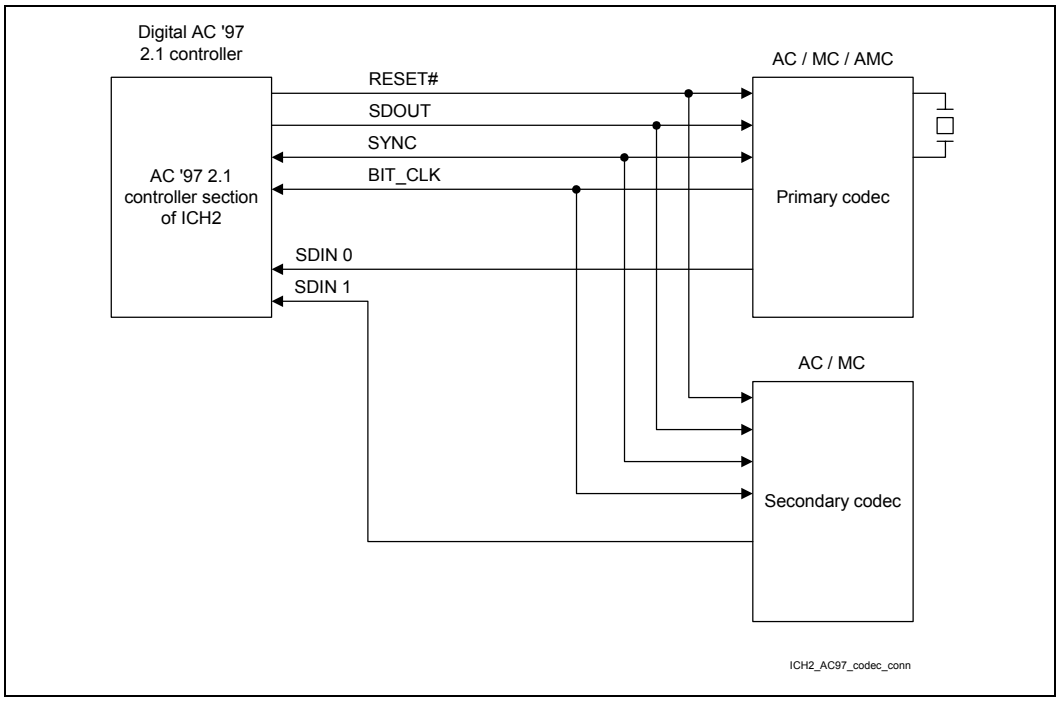
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

10.3 AC ’97

The ICH2 implements an *AC ’97 v2.2*-compliant digital controller. Any codec attached to the ICH2 AC-link must be *AC ’97 v2.2*compliant, as well. Contact your codec IHV for information on *AC ’97 v2.2*-compliant products. For information on the *AC ’97 v2.2*, see Section 1.3, *“Reference Documents”*.

The AC-link is a bidirectional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, by employing a time-division-multiplexed (TDM) scheme. The AC-link architecture enables data transfer through individual frames transmitted serially. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. Figure 65 shows a two-codec topology of the AC-link for the ICH2.

Figure 65. Intel® ICH2 AC ’97– Codec Connection



Intel has developed an advanced common connector for both AC ’97 as well as networking options. This is known as the Communications and Network Riser (CNR). Refer to Section 10.3.1.

The AC ’97 interface can be routed using 5 mil traces with 5 mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14 inches in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC-link. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital

controller (ICH2) and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH2 supports wake-on-ring from S1-S5 via the AC-link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH2 has weak pull-downs/pull-ups that are enabled only when the AC-Link Shut-off bit in the ICH2 is set. This keeps the link from floating when the AC-link is off or when there are no codecs present.

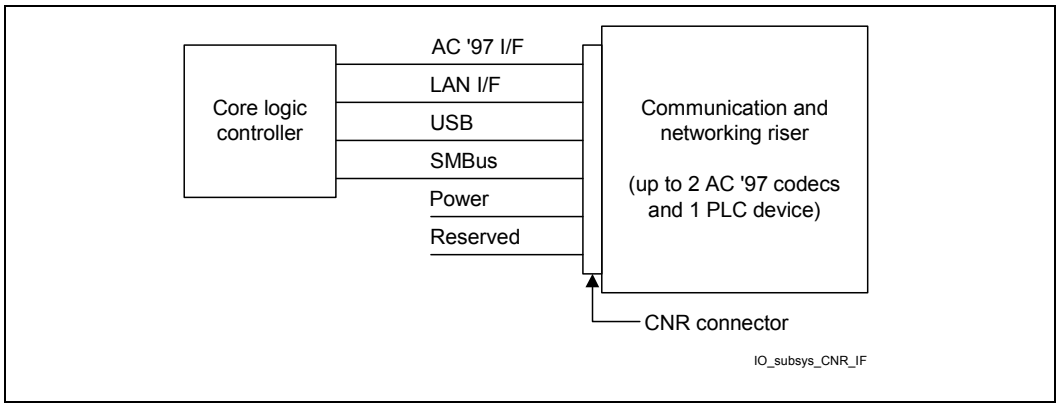
If the Shut-off bit is not set, it means that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH2, respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, it may be assumed that there is at least one codec. If there is one or no codec onboard, then the unused AC_SDIN pin(s) should have a weak (10 kΩ) pull-down to keep it from floating.

10.3.1 Communications Network Riser (CNR)

For related documents on the Communication Network Riser, refer to the Communication Network Riser Specification, Revision 1.1 (See Section 1.3, “Reference Documents”). The Communication and Networking Riser (CNR) Specification defines a hardware-scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, a V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface that should be configured before system shipment. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Unlike in the case of the AMR, the system designer will not sacrifice a PCI slot after deciding not to include a CNR in a particular build. It is required that the CNR A0-A2 pins be set to a unique address, so that the CNR EEPROM can be accessed.

The Figure 66 indicates the interface for the CNR connector. The Platform LAN Connection (PLC) can either be an 82562EH or 82562ET component. Refer to the CNR specification for additional information.

Figure 66. CNR Interface



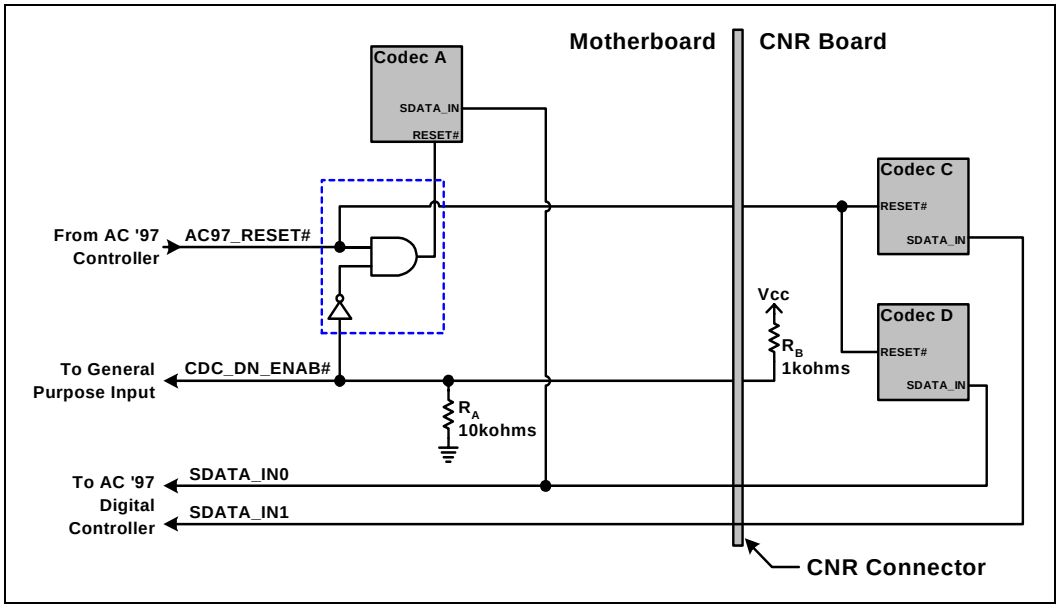
10.3.2 AC ’97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. For Intel recommended codec configurations, refer to the Intel White Paper, *Recommendations for ICHx/AC ’97 Audio (Motherboard and Communication and Network Riser).*

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC ’97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 67, Figure 68, Figure 69, and Figure 70) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 67. CDC_DN_ENAB# Support Circuitry for a Single Codec on Motherboard



As shown in Figure 67, when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented, on the motherboard. This circuitry is required to disable the motherboard codec when a CNR is installed which contains two AC ’97 codecs (or a single AC ’97 codec which must be the primary codec on the AC-link).

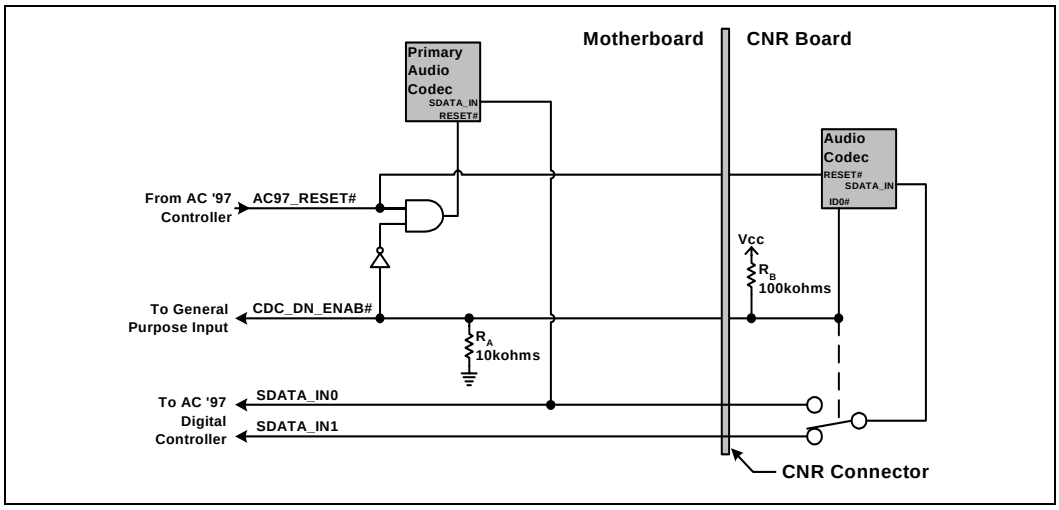
By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-link. One possible example of

using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 68 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 68 and Figure 69 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN*n* line as to not conflict with the motherboard codec(s).

Figure 68. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade



NOTE: Figure 69 shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, R_B, has been changed to 100 kΩ.

Figure 69. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR

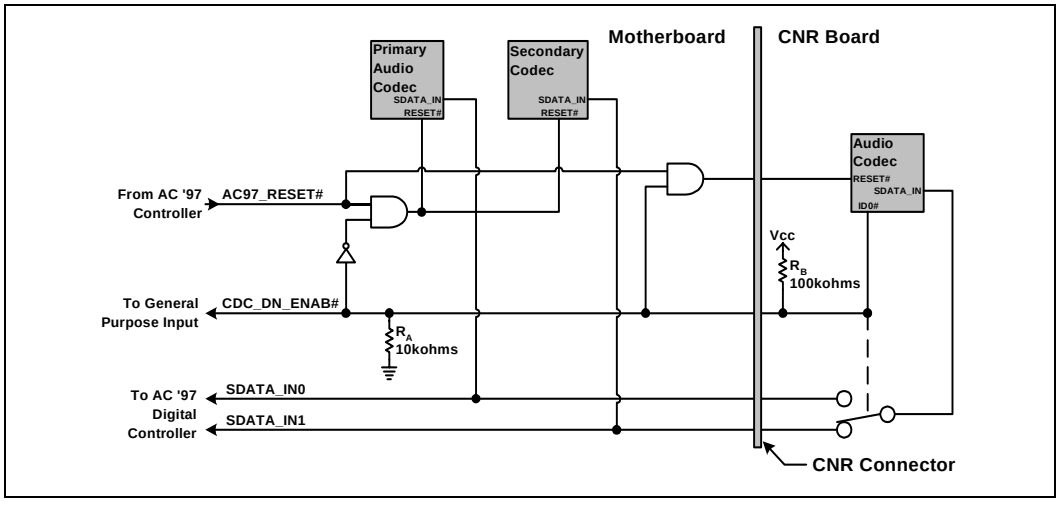
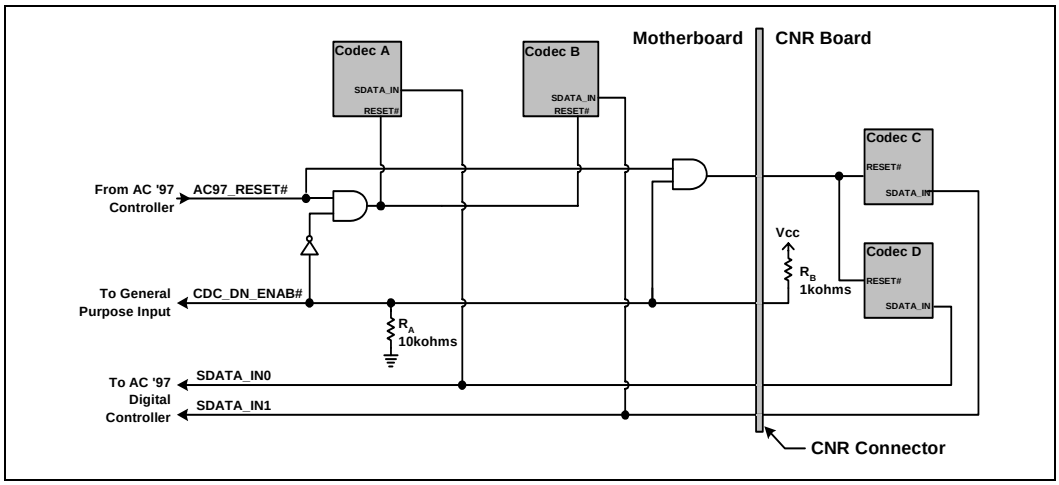


Figure 70 shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ.

Figure 70. CDC_DN_ENAB# Support for Two-Codecs on Motherboard / Two-Codecs on CNR



NOTES:

1. While it is possible to disable down codecs, as shown in Figure 67 and Figure 70, it is recommended against for reasons cited in the ICHx/AC '97 White Paper, including avoidance of shipping redundant and/or non-functional audio jacks.
2. All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
3. Any CNR with two codecs must implement R_B with value 1 kΩ. If there is one codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
4. A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
5. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is *strongly recommended* for testing purposes.

Table 30. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC ’97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC ’97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC ’97 Interface.
AC97_RESET#	Reset signal from the AC ’97 Digital Controller (ICH2).
SDATA_Inn	AC ’97 serial data from an AC ’97-compliant codec to an AC ’97-compliant controller (i.e., the ICH2).

10.3.2.1 Valid Codec Configurations

Table 31. Codec Configurations

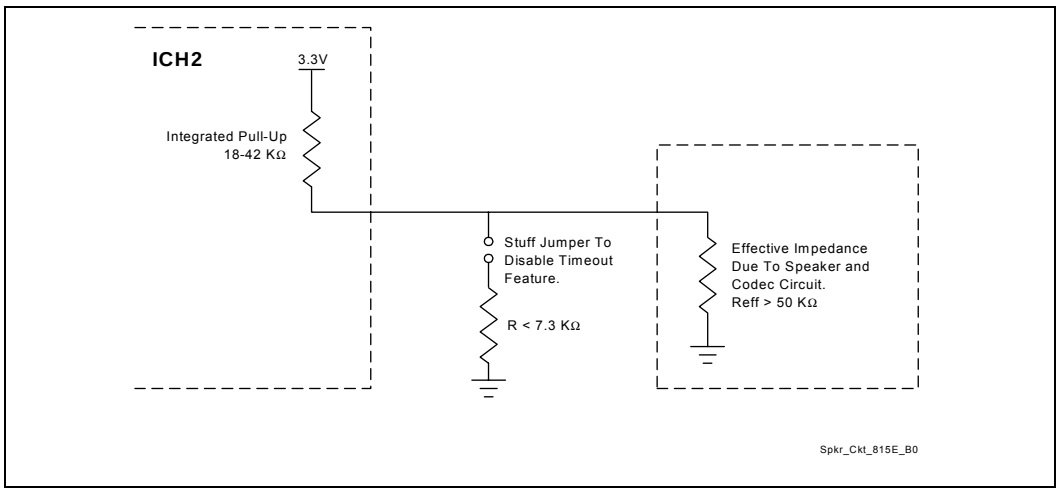
Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

10.3.3 SPKR Pin Considerations

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull up resistor (the resistor is only enabled during boot/reset). Therefore it's default state when the pin is a "no connect" is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see Figure 71). The value of the pull-down must be such that the voltage divider caused by the pull down and integrated pull up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

Figure 71. Example Speaker Circuit



10.3.4 AC '97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2) and by any other codec present. The clock is used as the time base for latching and driving data.

10.3.5 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH2 platform using AC ’97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH2 platform.

- Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH2 supports wake-on-ring from S1–S4 states via the AC-link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required. The ICH2 does not wake from the S5 state via the AC-link.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.4 USB

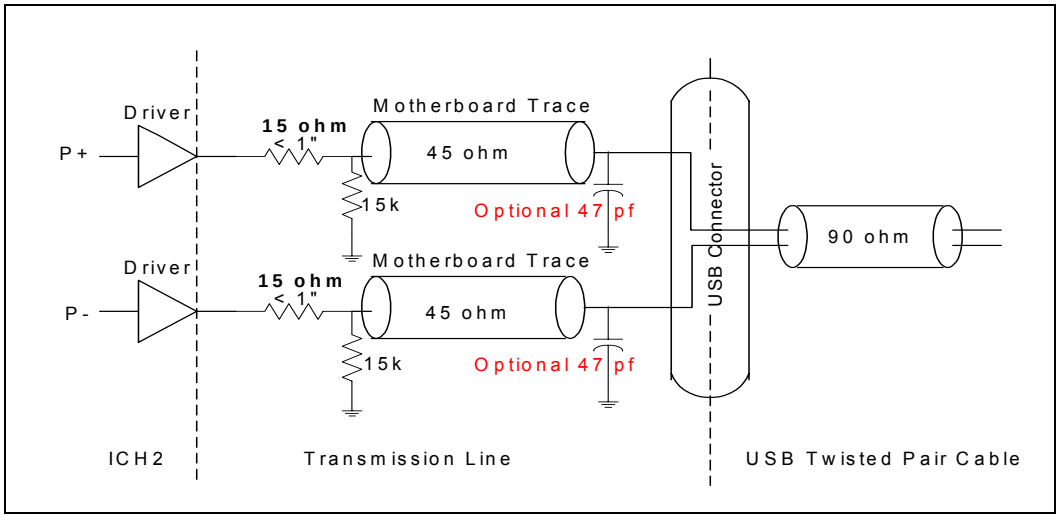
10.4.1 Using Native USB Interface

The general guidelines for the USB interface are as follows:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.
- An optional 0 pF - 47 pF cap may be placed as close to the USB connector side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This capacitor should be used to minimize EMI radiation while still maintaining signal quality (rise/fall time, Vcrs, etc).
- 15 kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0± … P3±), and they are REQUIRED for signal termination by the USB specification. The stub should be as short as possible.
- The trace impedance for the P0±…P3± signals should be 45 Ω (to ground) for each USB signal P+ or P-. When the stack-up recommended in Section 2.1 is used, the USB requires 9-mil traces. The impedance is 90 Ω between the differential signal pairs P+ and P-, to match the 90 Ω USB twisted-pair cable impedance. Note that the twisted-pair’s characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

Figure 72 illustrates the recommended USB schematic.

Figure 72. USB Data Signals



The recommended USB trace characteristics are:

- Impedance ‘Z0’ = 45.4 Ω
- Line Delay = 160.2 ps
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Res @ 20° C = 53.9 mΩ

10.4.2 Disabling the Native USB Interface of ICH2

The ICH2 native USB interface can be disabled. This can be done when an external PCI based USB controller is being implemented in the platform. To disable the native USB Interface, ensure the differential pairs are pulled down thru 15 kΩ resistors, ensure the OC[3:0]# signals are de-asserted by pulling them up weakly to VCC3SBY, and that both function 2 and 4 are disabled via the D31:F0;FUNC_DIS register. Ensure that the 48 MHz USB clock is connected to the ICH2 and is kept running. This clock must be maintained even though the internal USB functions are disabled.

10.5 I/O APIC Design Recommendation

Systems not using the I/O APIC should comply with the following recommendations:

- On the ICH2:
  - Tie PICCLK directly to ground.
  - Tie PICD0, PICD1 to ground through a 10 kΩ resistor.
- On the processor:
  - PICCLK requires special implementation for universal motherboard designs. See Section 4.2.9.
  - Tie PICD0 to 2.5 V through 10 kΩ resistors.
  - Tie PICD1 to 2.5 V through 10 kΩ resistors.

10.5.1 PIRQ Routing Example

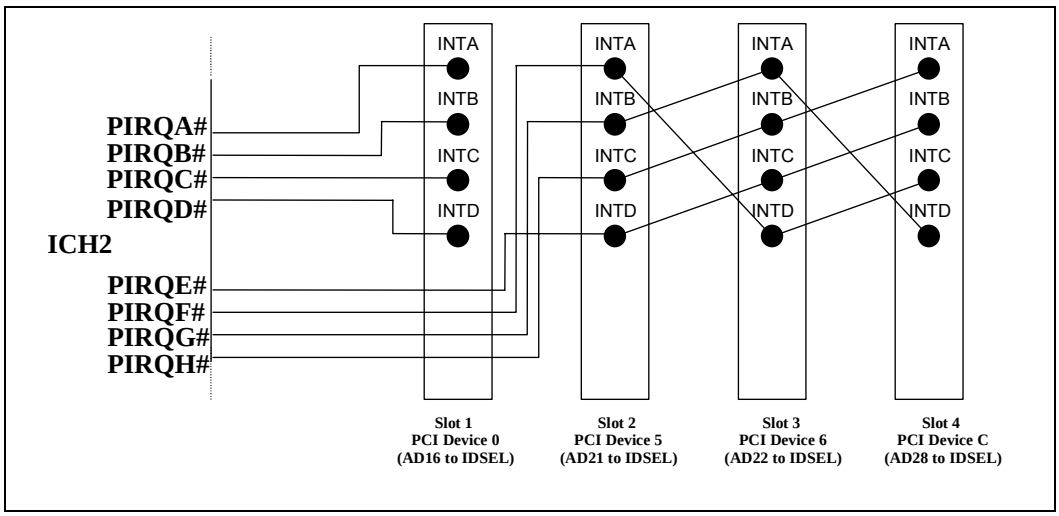
PCI interrupt request signals E-H are new to the ICH2. These signals have been added to lower the latency caused by having multiple devices on one Interrupt line. With these new signals, each PCI slot can have an individual PCI interrupt request line (assuming that the system has four PCI slots). Table 32 shows how the ICH2 uses the PCI IRQ when the I/O APIC is active.

Table 32. IOAPIC Interrupt Inputs 16 thru 23 Usage

No	IOAPIC INTIN PIN	Function in ICH2 using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	
2	IOAPIC INTIN PIN 17 (PIRQB)	AC '97, Modem and SMBus
3	IOAPIC INTIN PIN 18 (PIRQC)	
4	IOAPIC INTIN PIN 19 (PIRQD)	USB Controller #1
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN Device
6	IOAPIC INTIN PIN 21 (PIRQF)	
7	IOAPIC INTIN PIN 22 (PIRQG)	
8	IOAPIC INTIN PIN 23 (PIRQH)	USB Controller #2 (starting from ICH2 B0 stepping)

Interrupts B, D, E and H service devices internal to the ICH2. Interrupts A, C, F, and G are unused and can be used by PCI slots. Figure 73 shows an example of IRQ line routing to the PCI slots.

Figure 73. Example PIRQ Routing



The PCI IRQ Routing shown in Figure 73 allows the ICH2 internal functions to have a dedicated IRQ (assuming add-in cards are single function devices and use INTA). If a P2P bridge card or a multifunction device uses more than one INTn# pin on the ICH2 PCI Bus, the ICH2 internal functions will start sharing IRQs. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH2's internal device/functions.

10.6 SMBus/SMLink Interface

The SMBus interface on the ICH2 is the same as that on the ICH. It uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller. The SMBus host controller resides inside the ICH2.

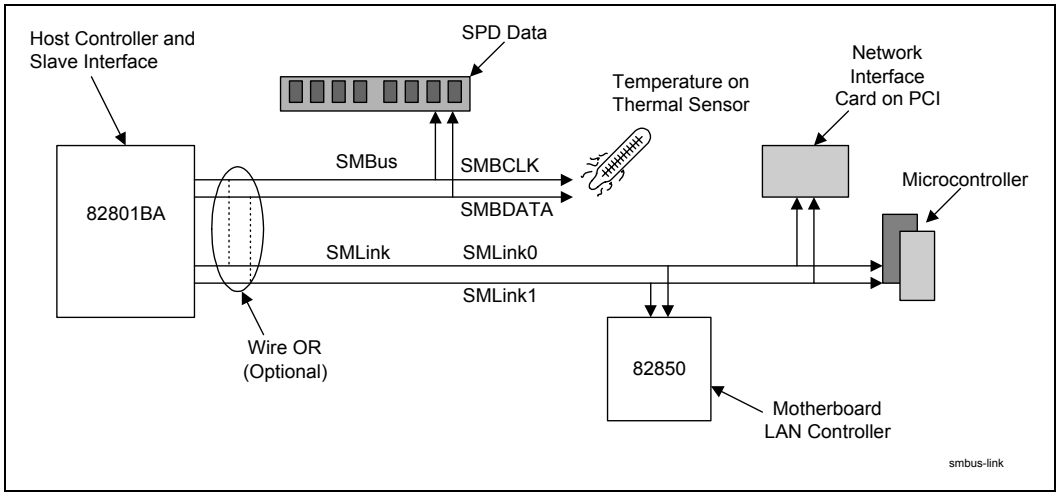
The ICH2 incorporates a new SMLink interface supporting AOL*, AOL2*, and slave functionality. It uses two signals, SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal, and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB slave interface.

For Alert on LAN (AOL) functionality, the ICH2 transmits heartbeat and event messages over the interface. When the 82562EM LAN connect component is used, the ICH2's integrated LAN controller claims the SMLink heartbeat and event messages and sends them out over the network. An external, AOL2-enabled LAN controller will connect to the SMLink signals, to receive heartbeat and event messages as well to as access the ICH2 SMBus slave interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus slave interface obey the SMBus protocol, so the two interfaces can be externally wire-ORed together to allow an external management ASIC to access targets on the SMBus as well as the ICH2 slave interface. This is performed by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA, as shown in Figure 74. Since the SMBus

and SMLINK are pulled up to VCCSUS3_3, system designers must ensure that they implement proper isolation for any devices that may be powered down while VCCSUS3_3 is still active (i.e., thermal sensors).

Figure 74. SMBus/SMLink Interface



Note: Intel does not support external access to the ICH2's integrated LAN controller via the SMLink interface. Also, Intel does not support access to the ICH2's SMBus slave interface by the ICH2's SMBus host controller. Table 33 describes the pull-up requirements for different implementations of the SMBus and SMLink signals.

Table 33. Pull-Up Requirements for SMBus and SMLink

SMBus / SMLink Use	Implementation
Alert-on-LAN* signals	4.7 kΩ pull-up resistors to 3.3 VSB are required.
GPIOs	Pull-up resistors to 3.3 VSB and the signals must be allowed to change states on power-up. (For example, on power-up the ICH2 will drive *heartbeat* messages until the BIOS programs these signals as GPIOs.) The value of the pull-up resistors depends on the loading on the GPIO signal.
Not Used	4.7 kΩ pull-up resistors to 3.3 VSB are required.

10.6.1 SMBus Architecture and Design Considerations

There are several possibilities for designing an SMBus using the ICH2. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs, where all devices are powered by either VCC_{CORE} or VCC_Suspend, and a mixed design where some devices are powered by each of the two supplies.

Primary considerations in choosing a design are based on:

- Whether there are there devices that must run in STR
- Amount of VCC_Suspend current available, i.e. minimizing load of VCC_Suspend.

10.6.1.1 General Design Issues and Notes

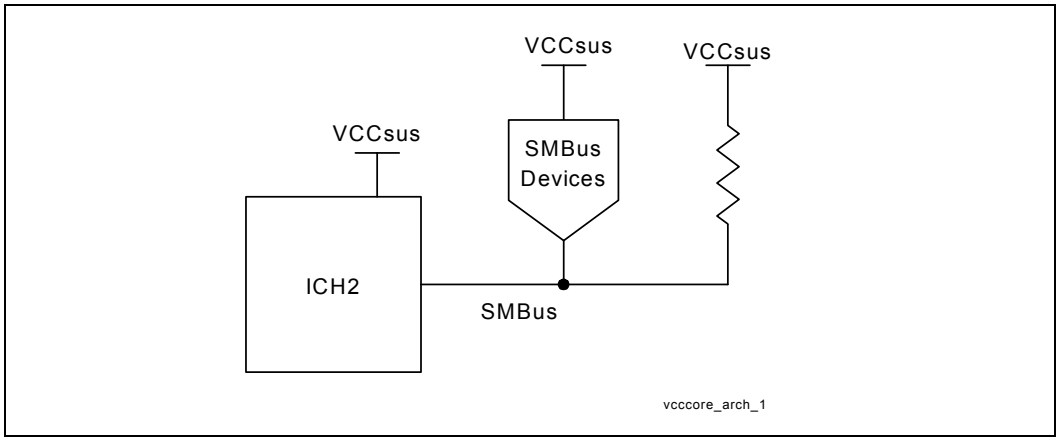
Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2 kΩ. This should prevent the SMBus signals from floating, which could cause leakage in the ICH2 and other devices.
- SDRAM DIMMs have their SPD device powered by the same power plane as that used for the DRAM array. Thus, in a system where STR is supported, the SPD device must be powered by VCC_Suspend. In a system not supporting STR, this DIMM can be powered by the core supply.
- RIMM memory modules have a separate power source from the RDRAM array for the SPD device. If this SPD device needs to operate in STR, then it should be connected to the VCC_Suspend supply.
- The ICH2 does not run SMBus cycles while in STR.
- SMBus devices that can operate in STR must be powered by the VCC_Suspend supply.

10.6.1.1.1 The Unified VCC_Suspend Architecture

In this design all SMBus devices are powered by the VCC_Suspend supply. Consideration must be made to provide enough VCC_Suspend current while in STR.

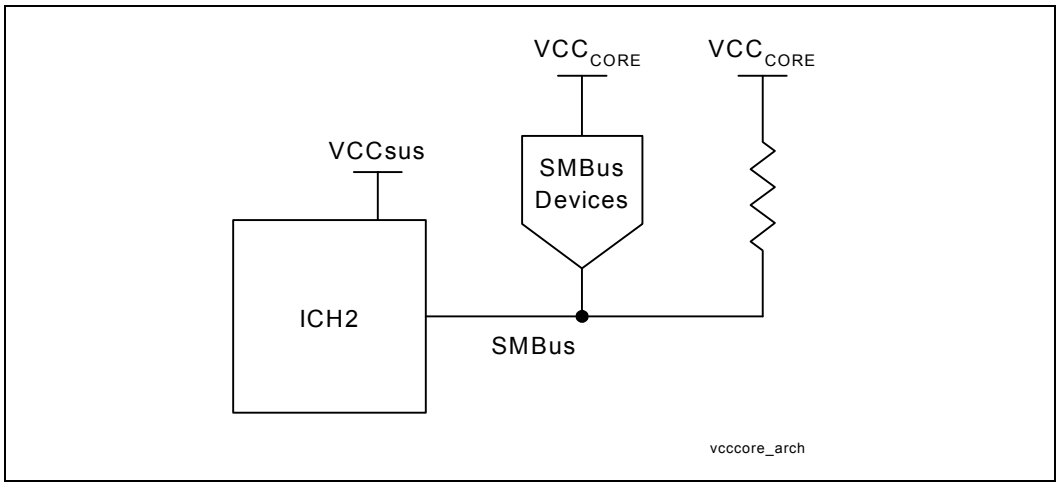
Figure 75. Unified VCC_Suspend Architecture



10.6.1.1.2 The Unified VCC_{CORE} Architecture

In this design, all SMBUS devices are powered by the VCC_{CORE} supply. This architecture allows none of the devices to operate in STR, but minimizes the load on VCC_Suspend (VCCsus).

Figure 76. Unified VCC_{CORE} Architecture

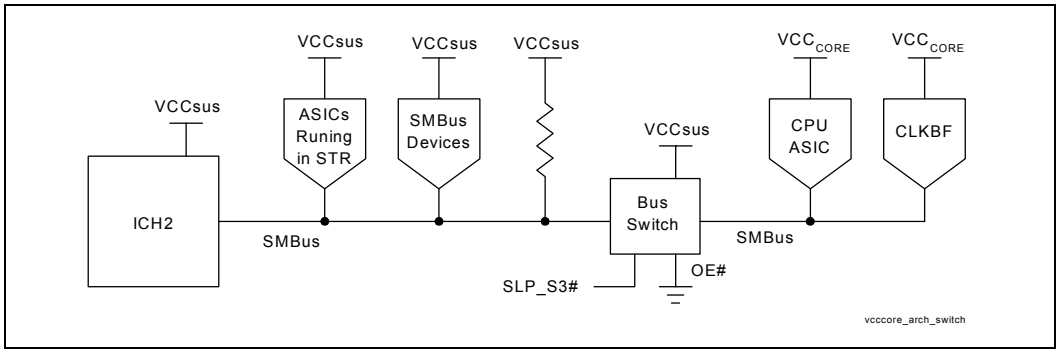


NOTES:
1. The SMBus device needs to be back-drive safe while its supply (VCC_{CORE}) is off and VCC_Suspend is still powered.
2. In suspended modes where VCC_{CORE} is OFF and VCC_Suspend is on, the VCC_{CORE} node will be very near ground. In this case the input leakage of the ICH will be approximately 10 uA.

10.6.1.1.3 Mixed Architecture

This design allows for SMBus devices to communicate while in STR, yet minimizes VCC_Suspend (VCCsus) leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a “bus switch” to isolate the devices powered by the core and suspend supplies (see Figure 77).

Figure 77. Mixed VCC_Suspend/VCC_{CORE} Architecture



Added Considerations for Mixed Architecture

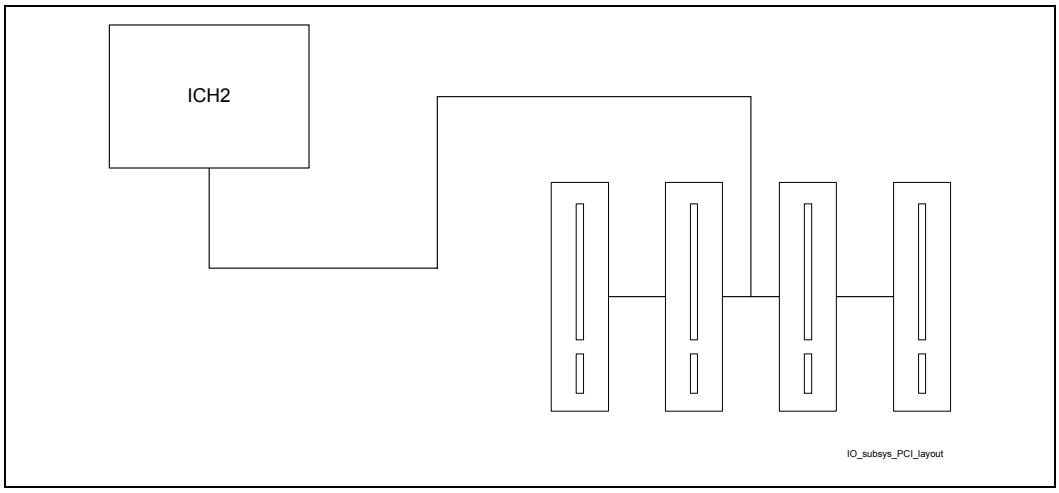
- The bus switch must be powered by VCC_Suspend (VCCsus)
- If there are 5 V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3 V signal levels.
- Devices that are powered by the VCC_Suspend well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.

10.7 PCI

The ICH2 provides a PCI Bus interface compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH2 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH2 supports six PCI Bus masters (excluding the ICH2), by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 78. PCI Bus Layout Example



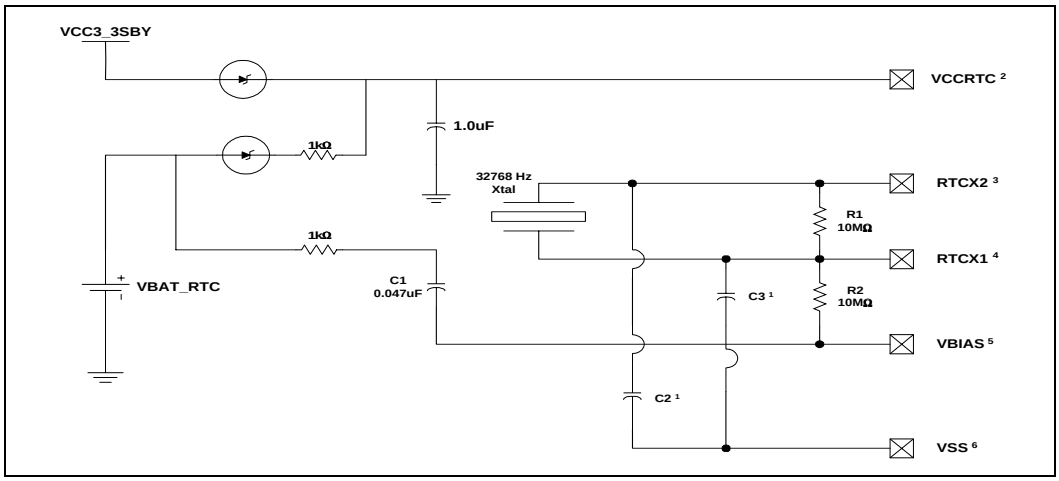
10.8 RTC

The ICH2 contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping the date and time and storing system data in its RAM when the system is powered down. This section will present the recommended implementation for the RTC circuit for the ICH2.

10.8.1 RTC Crystal

The ICH2 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. Figure 79 shows the external circuitry that comprises the oscillator of the ICH2 RTC.

Figure 79. External Circuitry for the Intel® ICH2 RTC



NOTES:

1. The exact capacitor value must be based on the crystal maker's recommendation. (The typical values for C2 and C3 are 18 pF with C_{LOAD} = 12.5 pF.)
2. VccRTC: Power for RTC well
3. RTCX2: Crystal input 2 – Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal input 1 – Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS voltage – This pin is used to provide a reference voltage. This DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground

10.8.2 External Capacitors

To maintain RTC accuracy the external capacitor C1 must be 0.047 µF. The external capacitor values for C2 and C3 should be chosen to provide the manufacturer-specified load capacitance (Cload) for the crystal, when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC.

The following equation can be used to choose the external capacitance values (C2 and C3):

Cload = (C2 * C3) / (C2 + C3) + Cparasitic

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain 32.768 kHz.

10.8.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible. Approximately 0.25 inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean. Use a filter, such as an RC low-pass or a ferrite inductor.

10.8.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system.

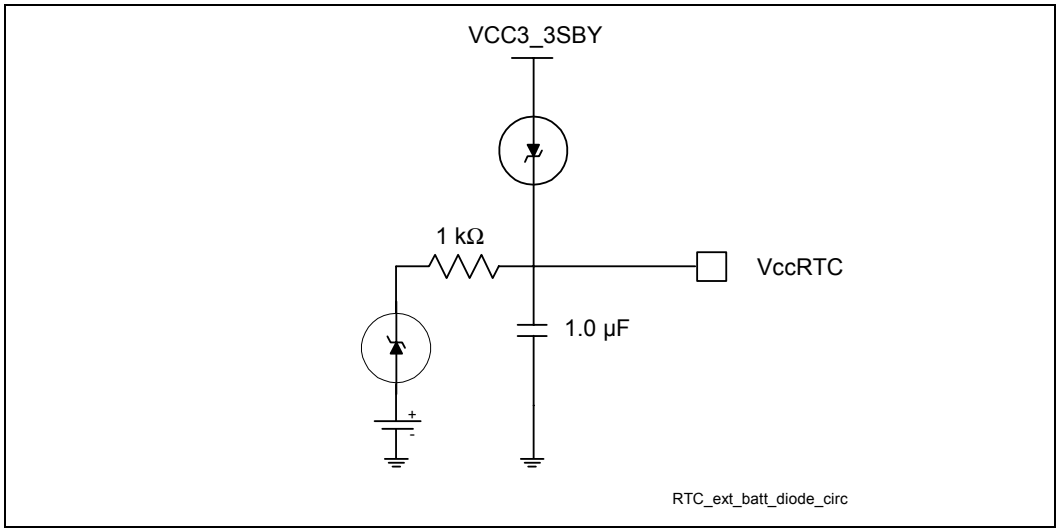
Example batteries include the Duracell* 2032, 2025 or 2016 (or equivalent), which give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

170,000 µAh / 3 µA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is within the range 3.0 V to 3.3 V.

The battery must be connected to the ICH2 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC well to be powered by the battery when system power is unavailable, but by system power when it is available. So, the diodes are set to be reverse-biased when system power is unavailable. Figure 80 shows an example of the used diode circuitry.

Figure 80. Diode Circuit to Connect RTC External Battery

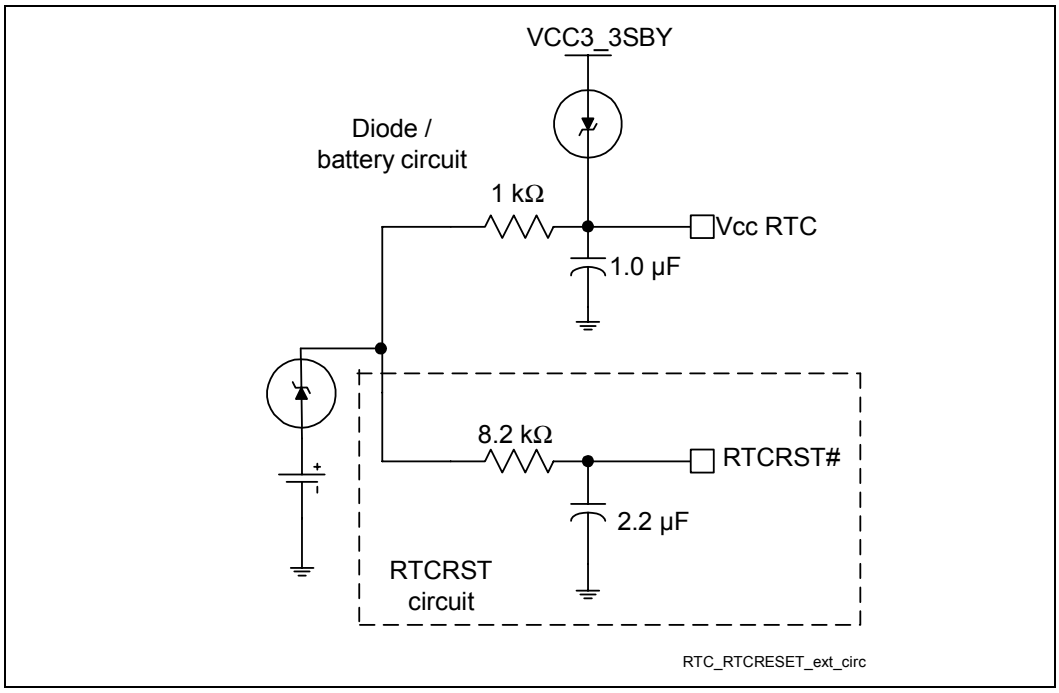


A standby power supply should be used in a desktop system, to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and, thereby, the RTC accuracy.

10.8.5 RTC External RTCRST Circuit

The ICH2 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go High some time after the battery voltage is valid. The RC time delay should be within the range of 10–20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until cleared by software. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

Figure 81. RTCRST External Circuit for ICH2 RTC



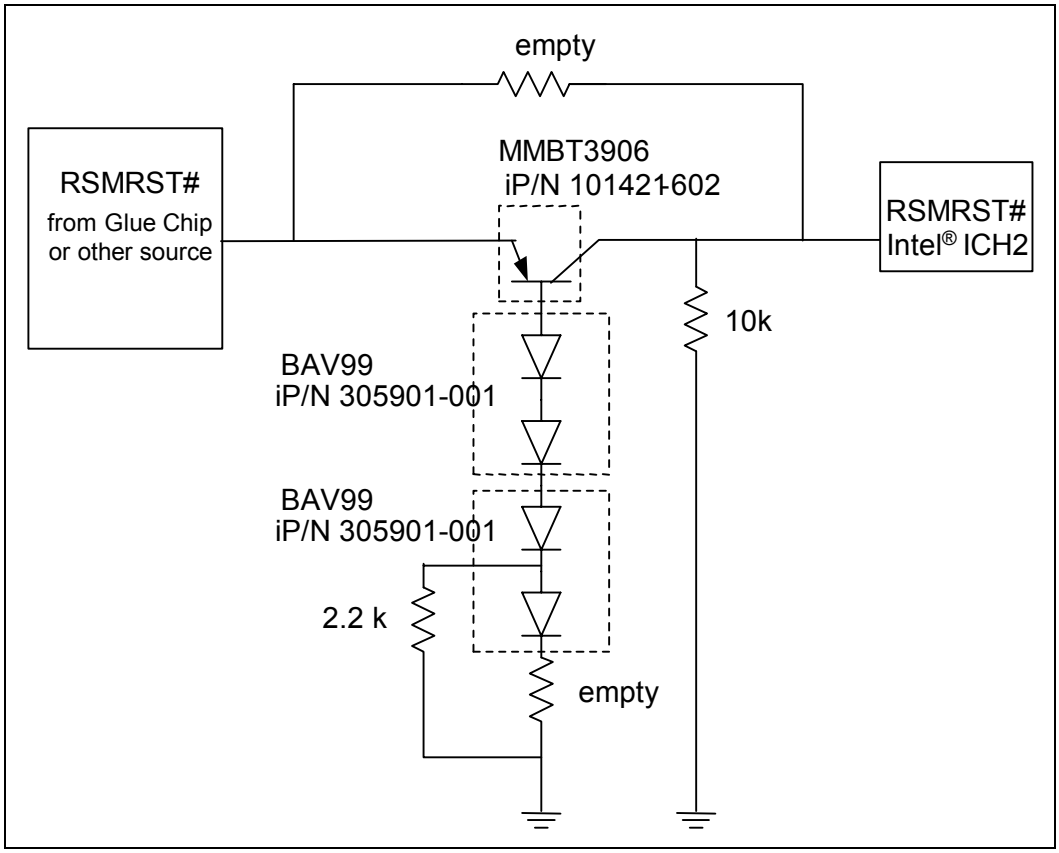
This RTCRST# circuit is combined with the diode circuit (see Figure 81), which allows the RTC well to be powered by the battery when system power is unavailable. Figure 81shows an example of this circuitry when used in conjunction with the external diode circuit.

10.8.6 Power-Well Isolation Control

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VccRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 81 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent IccRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

The circuit shown in the figure below should be implemented to control well isolation between the 3.3 V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VccRTC node during Sx-to-G3 power state transitions (removal of AC power).

Figure 82. RTC Power Well Isolation Control



10.8.7 RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths less than 1 inch. The shorter, the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing. (Optimally, there would be a ground line between them.)
- Put a ground plane under all external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

10.8.8 VBIAS DC Voltage and Noise Measurements

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths less than 1 inch. The shorter, the better.
- Steady-state VBIAS is a DC voltage of about 0.38 V ± .06 V.
- When the battery is inserted, VBIAS will be "kicked" to about 0.7–1.0 V, but it will return to its DC value within a few ms.
- Noise on VBIAS must be kept to a minimum (200 mV or less).
- VBIAS is very sensitive and cannot be directly probed, but it can be probed through a .01 µF capacitor.
- Excessive noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.
- To minimize VBIAS noise, it is necessary to implement the routing guidelines described previously as well as the required external RTC circuitry, as described in the *Intel® 82801BA I/O Controller Hub* (ICH2*) and Intel® 82801BAM I/O Controller Hub* (ICH2-M) Datasheet.

10.9 LAN Layout Guidelines

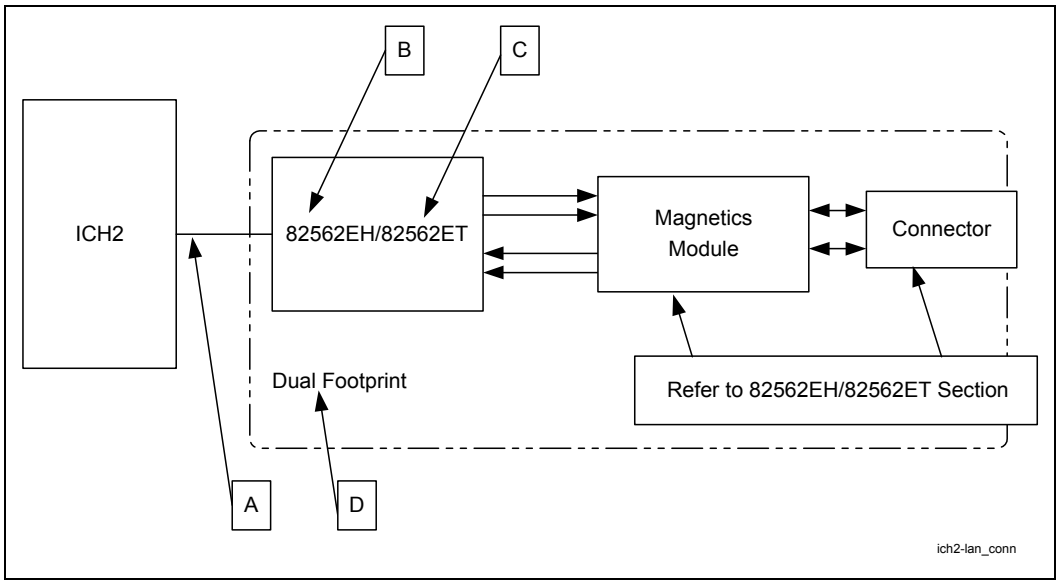
The ICH2 provides several options for integrated LAN capability. The platform supports several components, depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

Table 34. LAN Connect

LAN Connect Component	Connection	Features
82562EM	Advanced 10/100 Ethernet	AOL* and Ethernet 10/100 connection
82562ET	10/100 Ethernet	Ethernet 10/100 connection
82562EH	1 Mb HomePNA* LAN	1 Mb HomePNA connection

Intel developed a dual footprint for 82562ET and 82562EH, to minimize the required number of board builds. A single layout with the specified dual footprint allows the OEM to install the appropriate LAN connect component to satisfy market demand. Design guidelines are provided for each required interface and connection. Refer Figure 83 and table for the corresponding section of the design guide.

Figure 83. Intel® ICH2 / LAN Connect Section



10.9.1 Intel® ICH2 – LAN Interconnect Guidelines

This section contains the guidelines for the design of motherboards and riser cards that comply with LAN connect. It should not be considered a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be taken to match the **LAN_CLK** traces with those of the other signals, as follows. The following guidelines are for the ICH2-to-LAN component interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/82562EM components. Both components share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0]. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed. The AC characteristics for this interface are found in the *Intel® 82801BA I/O Controller Hub* (ICH2*) and Intel® 82801BAM I/O Controller Hub* (ICH2-M) Datasheet (document number: 290687). Dual footprint guidelines are found in Section 10.9.6.

10.9.1.1 Bus Topologies

The LAN connect interface can be configured in several topologies:

- Direct point-to-point connection between the ICH2 and the LAN component
- Dual footprint
- LOM/CNR implementation

10.9.1.2 Point-to-Point Interconnect

The following guidelines are for a single-solution motherboard. Either 82562EH, 82562ET or CNR is installed.

Figure 84. Single-Solution Interconnect

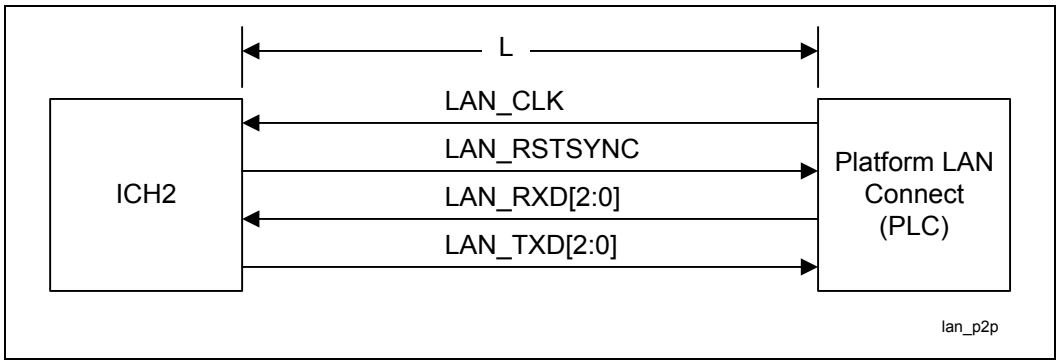


Table 35. Single-Solution Interconnect Length Requirements (See Figure 84)

Configuration	L	Comment
82562EH	4.5” to 10”	Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected.
82562ET	3.5” to 10”	
82562EM	4.5” to 8.5”	
CNR	3” to 9”	The trace length from the connector to LOM should be 0.5” to 3.0”

10.9.1.3 LOM/CNR Interconnect

The following guidelines allow for an all-inclusive motherboard solution. This layout combines the LOM, dual-footprint, and CNR solutions. The resistor pack ensures that either a CNR option or a LAN on Motherboard option can be implemented at one time, as shown in Figure 85, which shows the recommended trace routing lengths.

Figure 85. LOM/CNR Interconnect

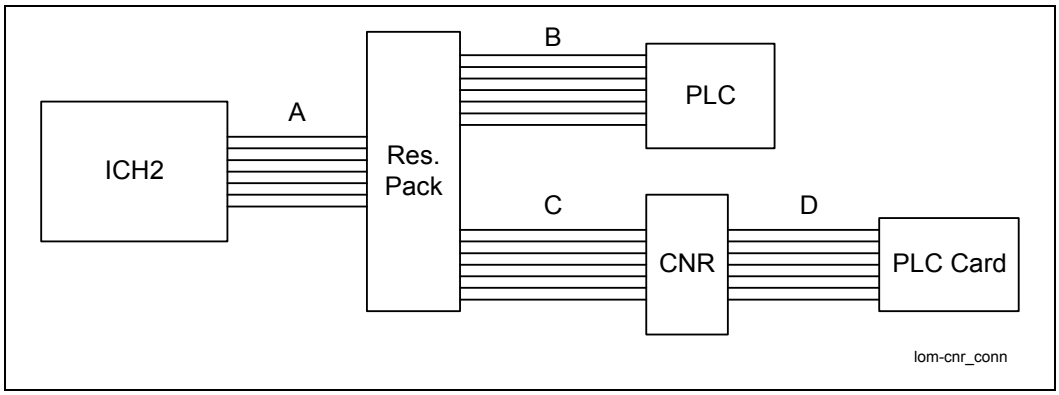


Table 36. LOM/CNR Length Requirements (See Figure 85)

Configuration	A	B	C	D
82562EH	0.5” to 6.0”	4.0” to (10.0” – A)		
82562ET	0.5” to 7.0”	3.0” to (10.0” – A)		
Dual footprint	0.5” to 6.5”	3.5” to (10.0” – A)		
82562ET/EH card*	0.5” to 6.5”		2.5” to (9” – A)	0.5” to 3.0”

NOTE: The total trace length should not exceed 13 inches.

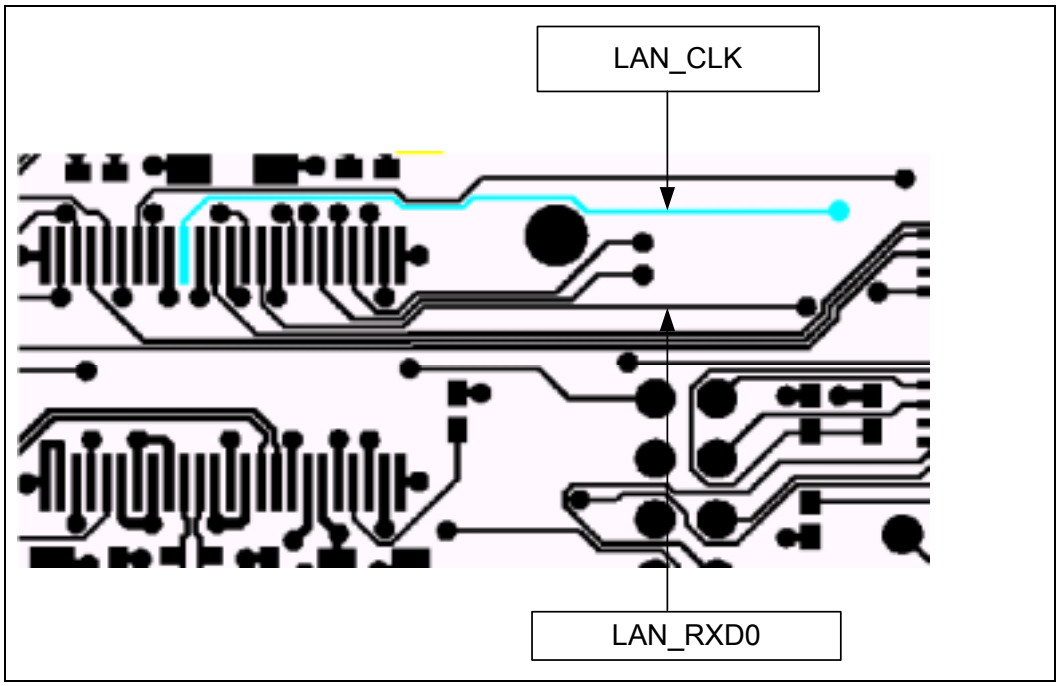
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω or 22 Ω.
- LAN on Motherboard PLC can be a dual-footprint configuration.

10.9.1.4 Signal Routing and Layout

LAN connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. Following are general guidelines that should be followed. It is recommended that the board designer simulate the board routing, to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard, the length of each data trace is either equal in length to the **LAN_CLK** trace or up to 0.5 inch shorter than the **LAN_CLK** trace. (**LAN_CLK** should always be the longest motherboard trace in each group.) The trace spacing, unless specified otherwise, is 5:10.

Figure 86. LAN_CLK Routing Example



10.9.1.5 Crosstalk Consideration

Noise due to crosstalk must be carefully minimized. Crosstalk is the main cause of timing skews and is the largest part of the t_{RMATCH} skew parameter.

10.9.1.6 Impedances

Motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ± 15% is strongly recommended. Otherwise, signal integrity requirements may be violated.

10.9.1.7 Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew-rate-controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33 Ω series resistor can be installed at the driver side of the interface, if the developer has concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.9.2 General LAN Routing Guidelines and Considerations

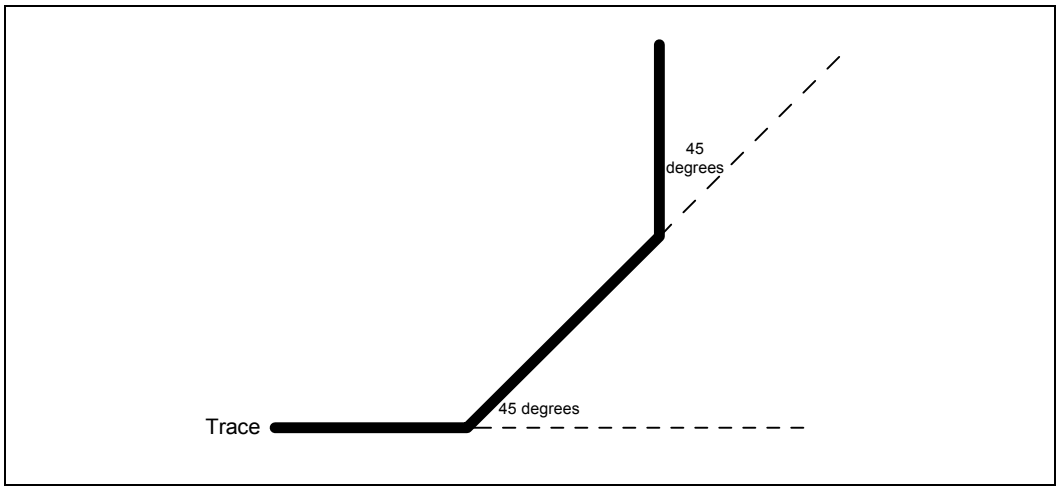
10.9.2.1 General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

- The maximum mismatch between the clock trace length and the length of any data trace is 0.5 inch.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.)
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils recommended).
- Keep to 7 mils the maximum separation between differential pairs.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45 degree bends instead. Refer to Figure 87.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures, by a distance exceeding the largest aperture dimension.

Figure 87. Trace Routing for High Speed Signal 90 Degree Bend



10.9.2.1.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, high-speed signals and signal layers close to a ground or power plane should be as short and wide as practical. Ideally, this ratio of trace width to height above the ground plane is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another, if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 0.030 inch (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long-and-thin traces are more inductive and would reduce the intended effect of the decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should have diameters sufficiently large to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

10.9.2.1.2 Signal Isolation

Comply with the following rules for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together.

Note: Over the length of the trace run, each differential pair should be at least 0.3 inch away from any parallel signal trace.

- Physically group together all components associated with one clock trace, to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.

- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor or other similar device.

10.9.2.2 Power and Ground Connections

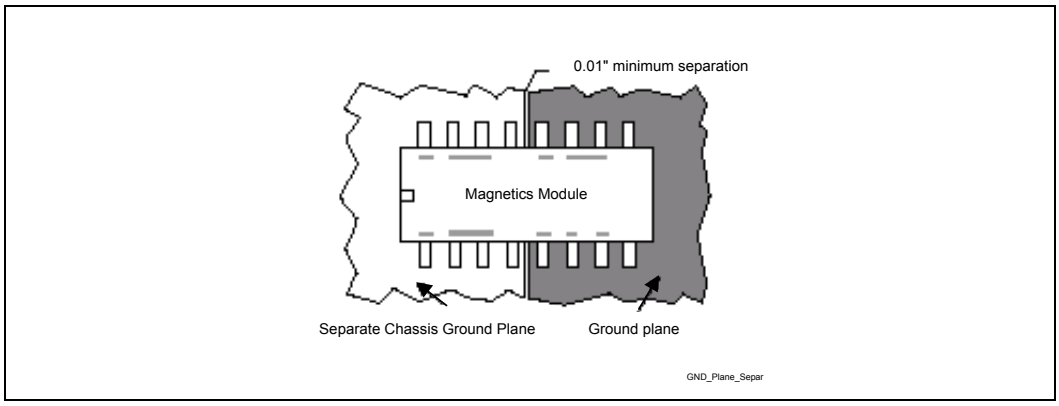
Comply with the following rules and guidelines for power and ground connections:

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7 µF capacitors are recommended.
- Place decoupling as close as possible to power pins.

10.9.2.2.1 General Power and Ground Plane Considerations

To properly implement the common-mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be physically separated from the digital or input ground (primary side) by at least 100 mils.

Figure 88. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections. Keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return significantly reduces EMI radiation.

Comply with the following rules to help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions (i.e., do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- To reduce coupling, separate noisy digital grounds from analog grounds.
- Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.

- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between adjacent coils in the transformer. There should not be a power plane under the magnetics module.
- Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6mm (59.0 mil). This is a **critical** requirement needed to past FCC part 68 testing for Phoneline connection. Note that for worldwide certification a trench of 2.5 mm is required. In North America, the spacing requirement is 1.6mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

10.9.2.3 A 4-Layer Board Design

Top-Layer Routing

Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

Ground Plane

A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.

Power Plane

Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply planes VDD_A. Analog power may be a metal fill “island,” separated from digital power, and better filtered than digital power.

Bottom-Layer Routing

Digital high-speed signals, which include all LAN interconnect interface signals, are routed on the bottom layer.

10.9.2.4 Common Physical Layout Issues

Common physical layer design and layout mistakes in LAN On Motherboard designs are as follows:

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise, and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (<= 1 inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk on the receive channel will induce degraded long-cable BER. When crosstalk gets onto the transmit channel, it can cause excessive emissions (below the FCC standard) and can cause poor transmit BER on long cables. Other signals should be kept at least 0.3 inch from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace closest to one of the receive traces will put more crosstalk onto the closest receive trace, which can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inch or more away from the nearest receive trace. In the vicinities where the traces enter or exit the magnetics, the RJ-45/11 and the PLC are the only possible exceptions.
6. Use of an inferior magnetics module. The magnetics modules used by Intel have been fully tested for IEEE PLC conformance, long-cable BER problems, and emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto-transformer in the transmit channel.)
7. Another common mistake is using an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different, and there also are differences in the receive circuit. Use the appropriate reference schematic or application notes.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and capacitor or termination plane. If these are not terminated properly, there can be emission (FCC) problems, IEEE conformance issues, and long-cable noise (BER) problems. The application notes contain schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω. (To calculate the differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close

(see Note) to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. A 10 Ω to 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. Another common problem is to use a too-large capacitor between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors with capacitances exceeding a few pF in either of these locations can slow the 100 Mbps rise and fall times so much that they fail the IEEE rise time and fall time specs, which will cause the return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (Reasonably good success has been achieved by using 6 pF to 12 pF values in past designs.) Unless there is some overshoot in the 100 Mbps mode, these caps are not necessary.

Note: It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces. Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

10.9.3 Intel® 82562EH Home/PNA* Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.9.2. Additional guidelines for implementing an 82562EH Home/PNA* LAN connect component are as follows are provided in the following subsections.

10.9.3.1 Power and Ground Connections

Obey the following rule for power and ground connections:

- For best performance, place decoupling capacitors on the back side of the PCB, directly under the 82562EH, with equal distance from both pins of the capacitor to power/ground.

The analog power supply pins for 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS as well as the VCCA and VSSA power supplies.

10.9.3.2 Guidelines for Intel® 82562EH Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section discusses guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the HomePNA LAN interface, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

10.9.3.3 Crystals and Oscillators

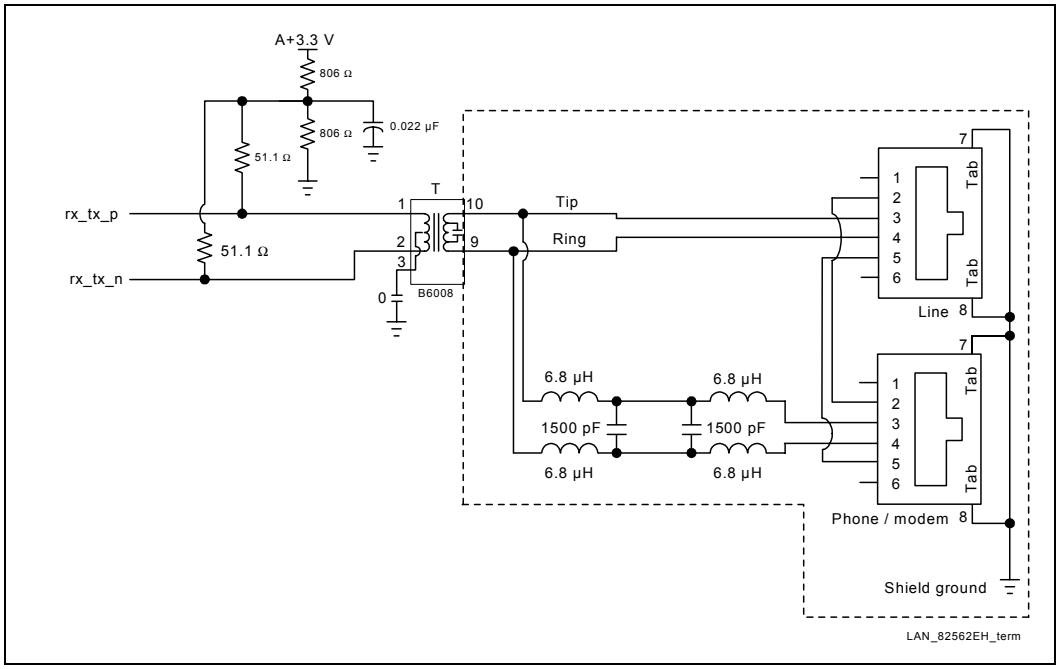
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA magnetics module to prevent communication interference. If they exist, the crystal's retaining straps should be grounded to prevent the possibility of radiation from the crystal case, and the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discrete components as close as possible to the 82562EH. Minimize the length and do not route any noisy signals in this area.

10.9.3.4 Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1 Ω (1%) resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1 Ω resistors is connected to a voltage-divider network. The opposite end of one 806 Ω resistor is tied to VCCA (3.3 V), and the opposite end of the other 806 Ω resistor and the cap are connected to ground. The termination is shown in Figure 89.

Figure 89. Intel® 82562EH Termination



The filter and magnetics component T1 integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA LAN interface.

One RJ-11 jack (labeled “LINE” in Figure 89) allows the node to be connected to the Phoneline, and the second jack (labeled “PHONE” in the previous figure) allows other down-line devices to be connected at the same time. This second connector is not required by the HomePNA. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack, also is recommended by the HomePNA to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This restricts of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Refer to the HomePNA website (www.homepna.org) for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA certifications.

10.9.3.5 Critical Dimensions

There are three dimensions to consider during layout. Distance ‘B’ from the line RJ11 connector to the magnetics module, distance ‘C’ from the phone RJ11 to the LPF (if implemented), and distance ‘A’ from 82562EH to the magnetics module (see Figure 90).

Figure 90. Critical Dimensions for Component Placement

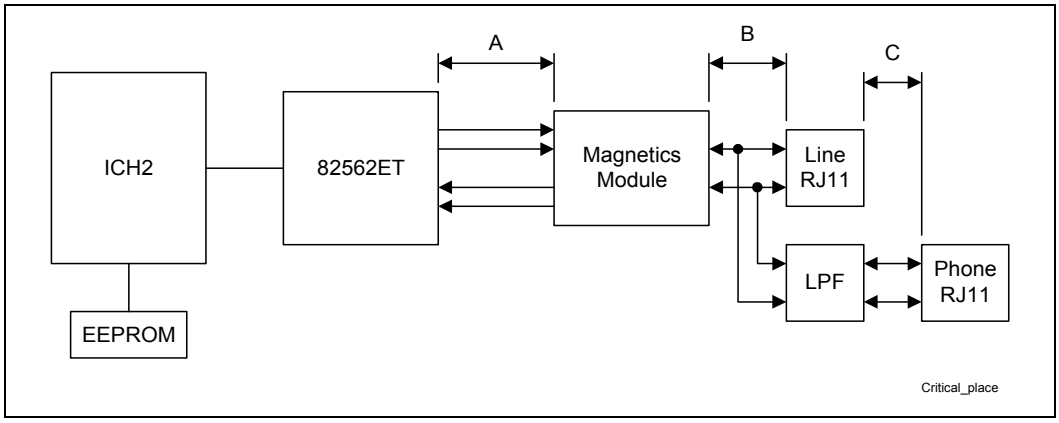


Table 37. Critical Dimensions for Component Placement (Refer to Figure 90)

Distance	Priority	Guideline
B	1	< 1”
A	2	< 1”
C	3	< 1”

10.9.3.5.1 Distance from Magnetics Module to Line RJ11 (Distance B)

This distance ‘B’ should be given highest priority and should be less then 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequally long differential pairs contribute to common-mode noise. This can degrade the receive circuit performance and contribute to emissions radiated from the transmit side.

10.9.3.5.2 Distance from Intel® 82562EH to Magnetics Module (Distance A)

Due to the high speed of signals present, distance ‘A’ between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance from connects to the magnetics module.

Generally speaking, any section of trace intended for use with high-speed signals should be subject to proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between the device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

10.9.3.5.3 Distance from LPF to Phone RJ11 (Distance C)

This distance ‘C’ should be less then 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequally long differential pairs contribute to common-mode noise. This can degrade the receive circuit performance and contribute to emissions radiated from the transmit side.

10.9.4 Intel® 82562ET / 82562EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.9.2. Additional guidelines for implementing an 82562ET or 82562EM LAN connect component are provided in the following subsections. For related documents, see Section 1.3, *“Reference Documents”*.

10.9.4.1 Guidelines for Intel® 82562ET / 82562EM Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the Ethernet LAN interface, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space. In addition, the 82562ET or 82562EM should be placed more than 1.5 inches away from any board edge to minimize the potential for EMI radiation problems.

10.9.4.2 Crystals and Oscillators

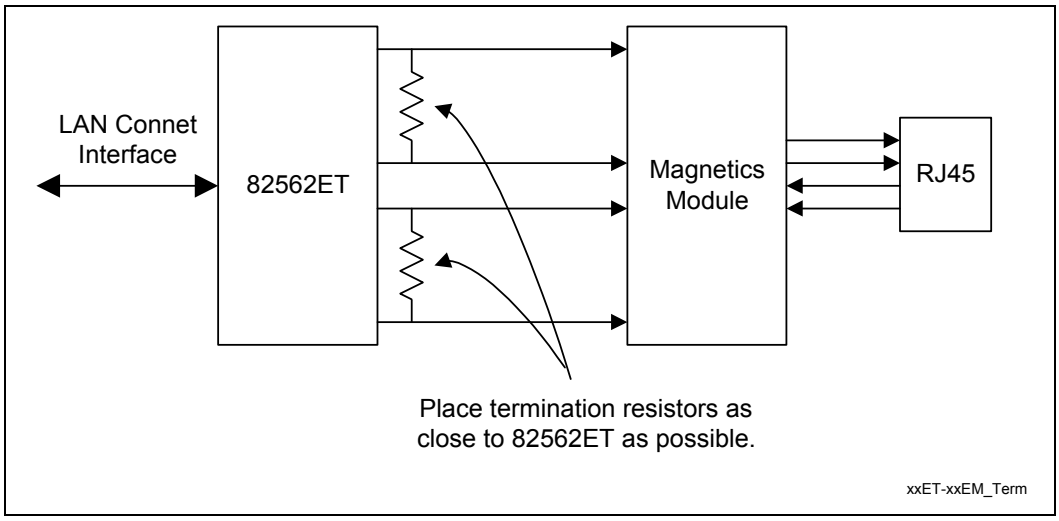
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference with communication. If they exist, the retaining straps of the crystal should be grounded to prevent possible radiation from the crystal case. Also, the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discrete components as close as possible to the 82562ET or 82562EM. Keep the trace length as short as possible and do not route any noisy signals in this area.

10.9.4.3 Intel® 82562ET / 82562EM Termination Resistors

The 100 Ω 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω 1% receive differential pairs (RDP/RDN) should be placed as close as possible to the LAN connect component (82562ET or 82562EM). This is due to the fact that these resistors terminate the entire impedance seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

Figure 91. Intel® 82562ET/82562EM Termination



10.9.4.4 Critical Dimensions

There are two dimensions to consider during layout. Distance ‘B’ from the line RJ45 connector to the magnetics module and distance ‘A’ from the 82562ET or 82562EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches) (see Figure 92).

Figure 92. Critical Dimensions for Component Placement

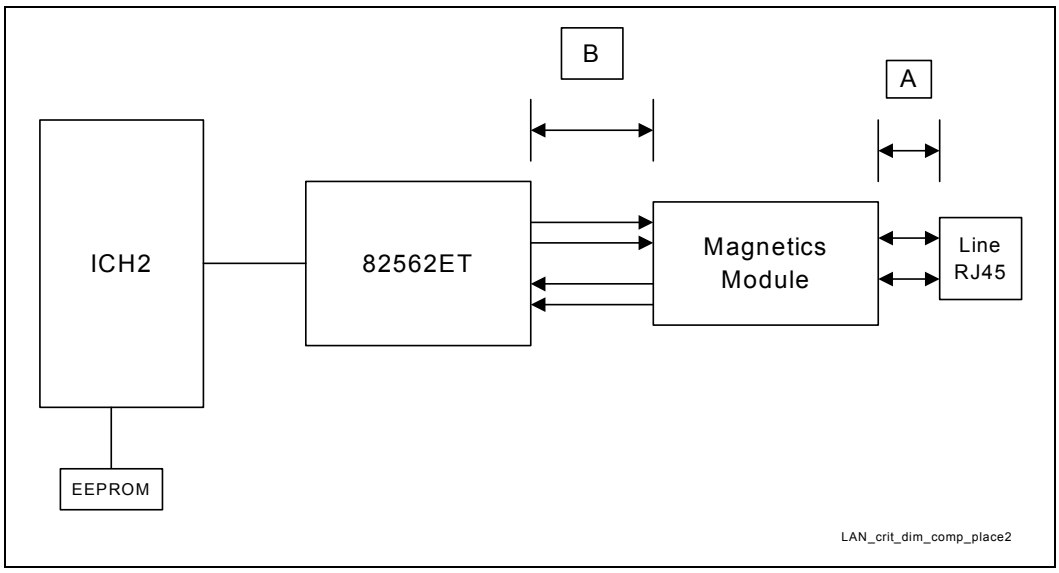


Table 38. Critical Dimensions for Component Placement (see Figure 92)

Distance	Priority	Guideline
A	1	< 1”
B	2	< 1”

10.9.4.4.1 Distance from Magnetics Module to RJ45

The distance A in Figure 92 should be given the highest priority in board layout. The separation between the magnetics module and the RJ45 connector should be kept less than 1 inch. The following trace characteristics are important and should be observed:

- Differential impedance: The differential impedance should be 100 Ω. The single-ended trace impedance will be approximately 50 Ω. However, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (e.g., TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (e.g., width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common-mode noise. This can degrade the receive circuit’s performance and contribute to emissions radiated from the transmit circuit. If the 82562ET must be placed farther than a couple of inches from the RJ45 connector, distance B can be sacrificed. It should be a priority to keep the total distance between the 82562ET and RJ-45 as short as possible.

Note: The measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layouts accordingly. If the actual impedance is consistently low, a target of 105–110 Ω should compensate for second-order effects.

10.9.4.4.2 Distance from Intel® 82562ET to Magnetics Module

Distance B should also be designed to be less than 1 inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces intended for use with high-speed signals should be subject to proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that contributes more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and of equal length within each differential pair.

10.9.4.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both backplanes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems, such as analog-to-digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane. Similarly, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds so as to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high-frequency harmonics, that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

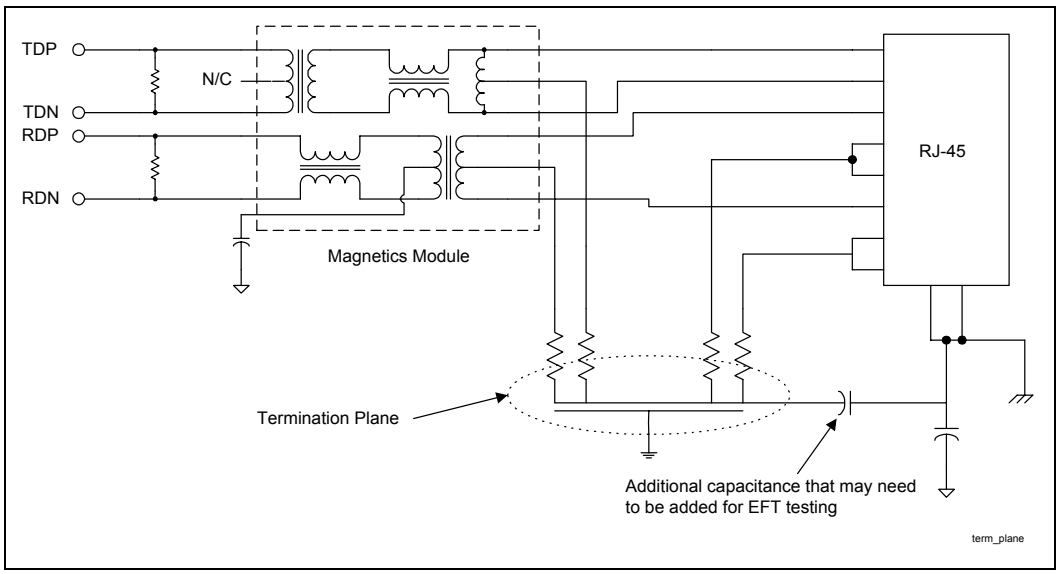
Terminating Unused Connections

In Ethernet designs, it is common practice to terminate to ground both unused connections on the RJ-45 connector and the magnetics module. Depending on the overall shielding and grounding design, this may be done to the chassis ground, signal ground or a termination plane. Care must be taken when using various grounding methods to ensure that emission requirements are met. The method most often implemented is called the “Bob Smith” termination. In this method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

Termination Plane Capacitance

The recommended minimum termination plane capacitance is 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (electrical fast transient) testing. If a discrete capacitor is used, it should be rated for at least 1000 Vac, to satisfy the EFT requirements.

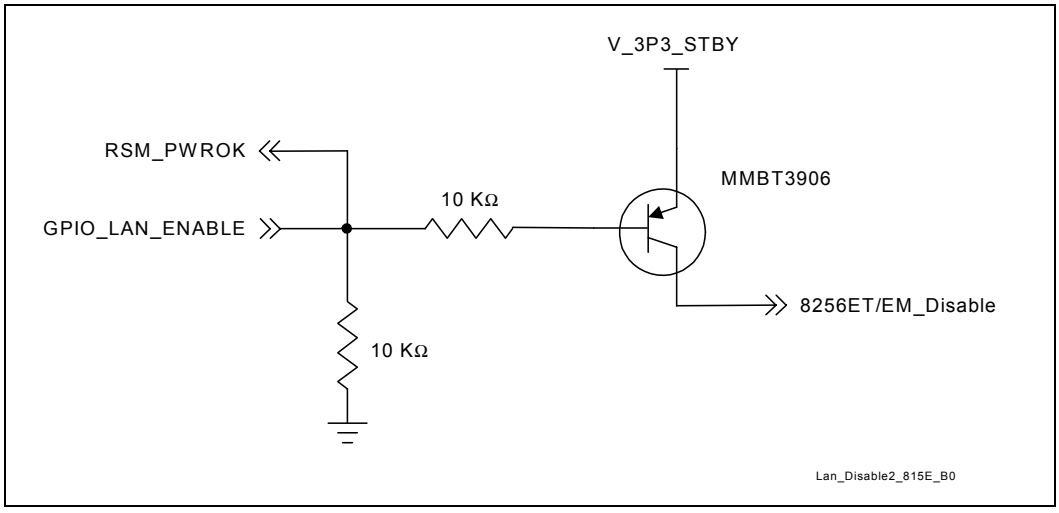
Figure 93. Termination Plane



10.9.5 Intel® 82562ET/82562EM Disable Guidelines

To disable the 82562ET/82562ETEM, the device must be isolated (disabled) prior to reset (RSM_PWROK) being asserted. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. The circuit shown in Figure 94 allows this behavior. BIOS can disable the LAN microcontroller by controlling the GPIO.

Figure 94. Intel® 82562ET/82562EM Disable Circuit



There are 4 pins that are used to put the 82562ET controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 39 describes the operational/disable features for this design.

The four control signals shown in the Table 39 should be configured as follows: Test_En should be pulled-down thru a 100 Ω resistor. The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node “82562ET_Disable” of the disable circuit.

Table 39. Intel® 82562ET Operating States

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled with Clock (low power)
1	1	1	1	Disabled without Clock (lowest power)

10.9.6 Intel® 82562ET / 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual-footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM components, while using only one motherboard design. The following guidelines are for the 82562ET/82562EH dual-footprint option. The guidelines called out in Sections 10.9.1 through 10.9.4 apply to this configuration. The dual footprint for this particular solution uses a SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in Figure 95 and Figure 96.

Figure 95. Dual-Footprint LAN Connect Interface

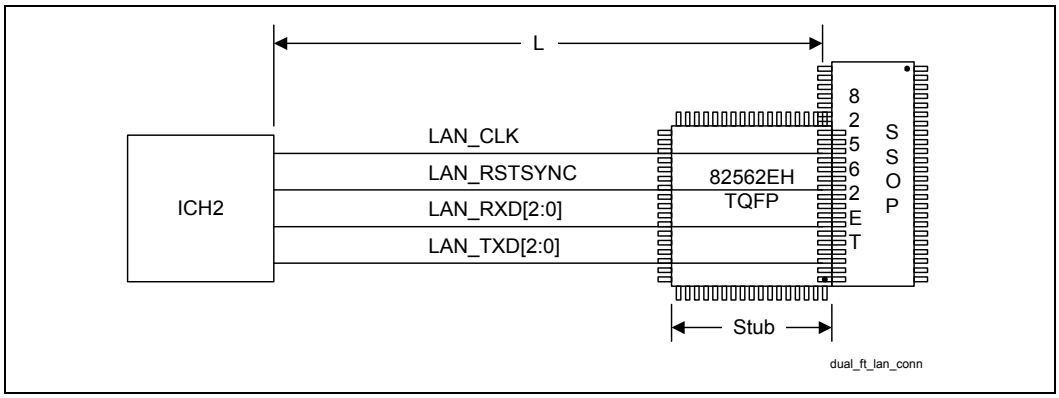
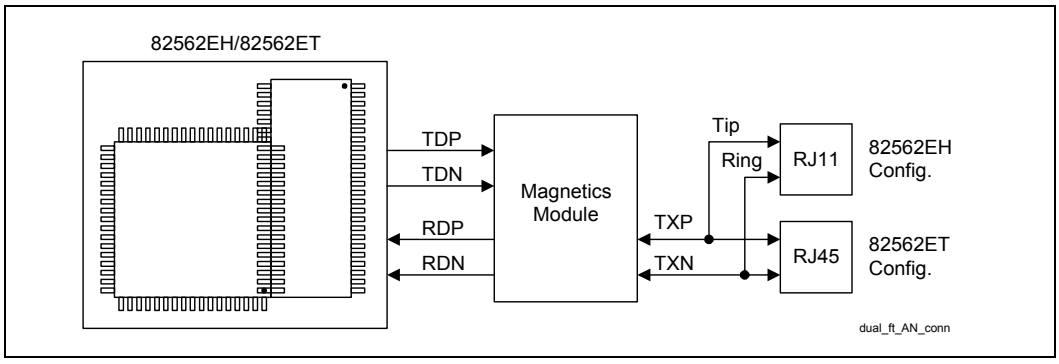


Figure 96. Dual-Footprint Analog Interface



The following are additional guidelines for this configuration:

- L = 3.5 inches to 10 inches
- Stub < 0.5 inch
- Either 82562EH or 82562ET/82562EM can be installed, but not both.
- 82562ET pins 28,29, and 30 overlap with 82562EH pins 17,18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip are shared by the 82562EH and 82562ET configurations.
- No stubs should be present when 82562ET is installed.
- Packages used for the dual footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22 Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e., magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component.
- Use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Traces from magnetics to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.
- Place at least bulk capacitor (4.7 µF or greater) on each side of the component.
- Place decoupling capacitors (0.1 µF) as close to the component as possible.

10.10 LPC/FWH

The following subsections provide general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS.

10.10.1 In-Circuit FWH Programming

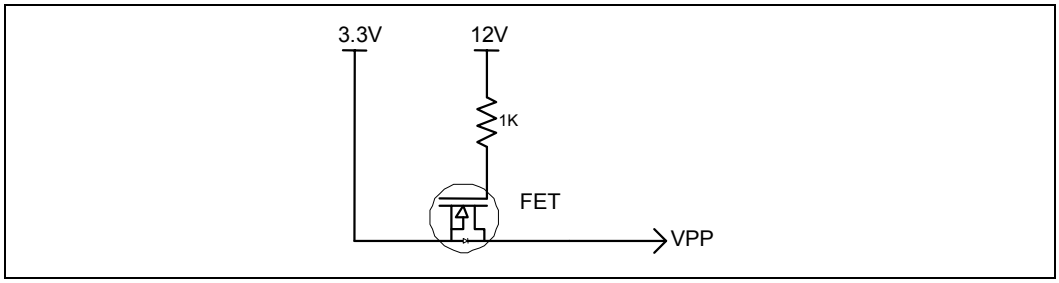
All cycles destined for the FWH will appear on the PCI. The ICH2 hub interface-to-PCI Bridge puts all processor boot cycles out on the PCI (before sending them out on the FWH interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on PCI. This enables booting from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH2 in the subtractive decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, two devices will positively decode the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind the 82380AB. Once you have booted from the PCI card, you potentially could program the FWH in circuit and program the ICH2 CMOS.

10.10.2 FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports a Vpp of 3.3 V or 12 V. If Vpp is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 Vpp for 80 hours. The 12 Vpp would be useful in a programmer environment that is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 97. FWH VPP Isolation Circuitry



10.10.3 FWH Decoupling

A 0.1 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the VCC supply pins and the VSS ground pin to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

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11 Clocking

For an 815EP universal platform, there are two clock specifications. One is for a two-DIMM solution, and the other is for a three-DIMM solution. In both specifications only single-ended clocking is supported. 815EP Universal Socket 370 platforms using a future 0.13 micron socket 370 processor cannot implement differential clocking.

11.1 2-DIMM Clocking

Table 40 shows the characteristics of the clock generator for a 2-DIMM solution.

Table 40. CK815 (2-DIMM) Clocks

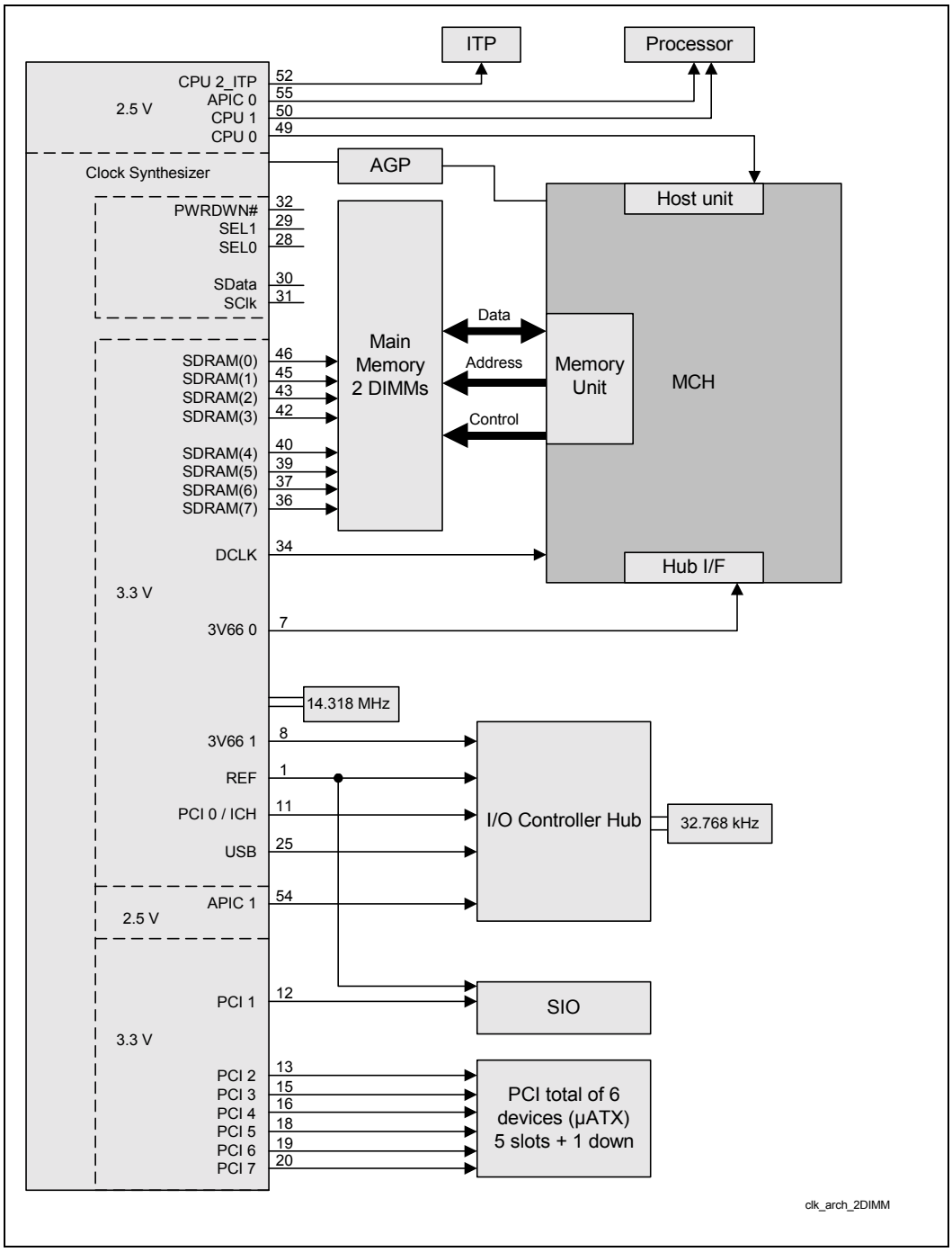
Number	Clock	Frequency
3	Processor clocks	66/100/133 MHz
9	SDRAM clocks	100/133 MHz
7	PCI clocks	33 MHz
2	APIC clocks	16.67/33 MHz
2	48 MHz clocks	48 MHz
3	3 V, 66 MHz clocks	66 MHz
1	REF clock	14.31818 MHz

The following bullets list the features of the CK-815 clock generator in a 2-DIMM solution:

- Nine copies of 100/133 MHz SDRAM clocks (3.3 V) [SDRAM0…7, DClk]
- Seven copies of PCI clock (33 MHz) (3.3 V)
- Two copies of APIC clock @ 33 MHz, synchronous to processor clock (2.5 V)
- One copy of 48 MHz USB clock (3.3 V) (non-SSC) (type 3 buffer)
- One copy of 48 MHz DOT clock (3.3 V) (non-SSC) (see DOT details)
- Three copies of 3 V, 66 MHz clock (3.3 V)
- One copy of REF clock @ 14.31818 MHz (3.3 V)
- Ref. 14.31818 MHz xtal oscillator input
- Power-down pin
- Spread-spectrum support
- I^2C support for turning off unused clocks

Figure 98 shows the 815EP chipset platform clock architecture for a 2-DIMM solution.

Figure 98. Platform Clock Architecture for a 2-DIMM Solution



11.2 3-DIMM Clocking

Table 41 shows the characteristics of the clock generator for a 3-DIMM solution.

Table 41. CK815 (3-DIMM) Clocks

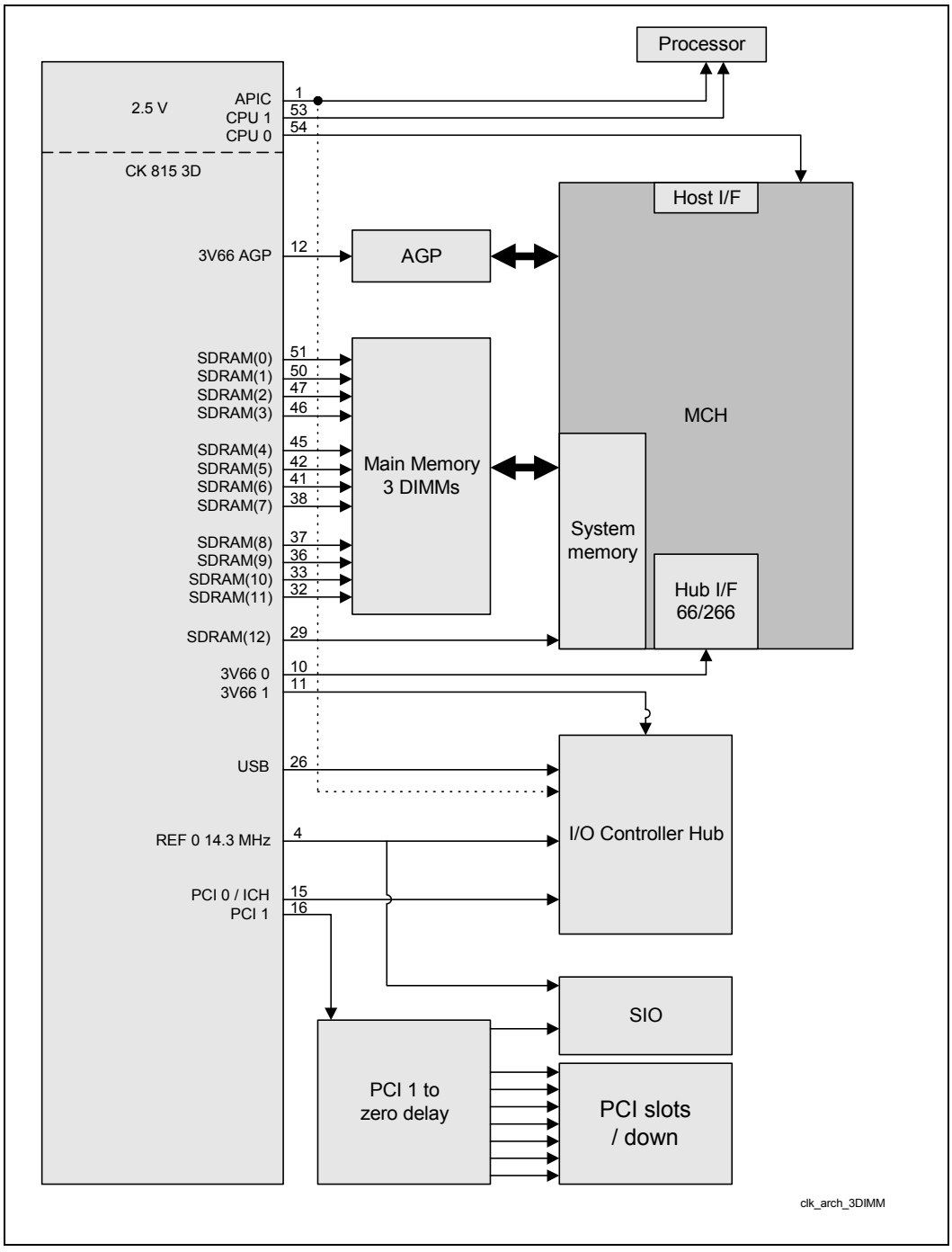
Number	Clock	Frequency
2	Processor clocks	66/100/133 MHz
13	SDRAM clocks	100/133 MHz
2	PCI clocks	33 MHz
1	APIC clocks	33 MHz
2	48 MHz clocks	48 MHz
3	3 V, 66 MHz clocks	66 MHz
1	REF clock	14.31818 MHz

The following bullets list the features of the CK-815 clock generator in a 3-DIMM solution:

- Thirteen copies of SDRAM clocks
- Two copies of PCI clock
- One copy of APIC clock
- One copy of 48 MHz USB clock (3.3 V) (non-SSC) (type 3 buffer)
- One copy of 48 MHz DOT clock (3.3 V) (non-SSC) (see DOT details)
- Three copies of 3 V, 66 MHz clock (3.3 V)
- One copy of ref. clock @ 14.31818 MHz (3.3 V)
- Ref. 14.31818 MHz xtal oscillator input
- Spread-spectrum support
- I^2C support for turning off unused clocks

Figure 99 shows the 815EP chipset platform clock architecture for a 3-DIMM solution.

Figure 99. Platform Clock Architecture for a 3-DIMM Solution



11.3 Clock Routing Guidelines

This section presents the generic clock routing guidelines for both 2-DIMM and 3-DIMM boards. For 3-DIMM boards, additional analysis must be performed by the motherboard designer to ensure that the clocks generated by the external PCI clock buffer meet the PCI specifications for clock skew at the receiver, when compared with the PCI clock at the ICH2.

Figure 100. Clock Routing Topologies

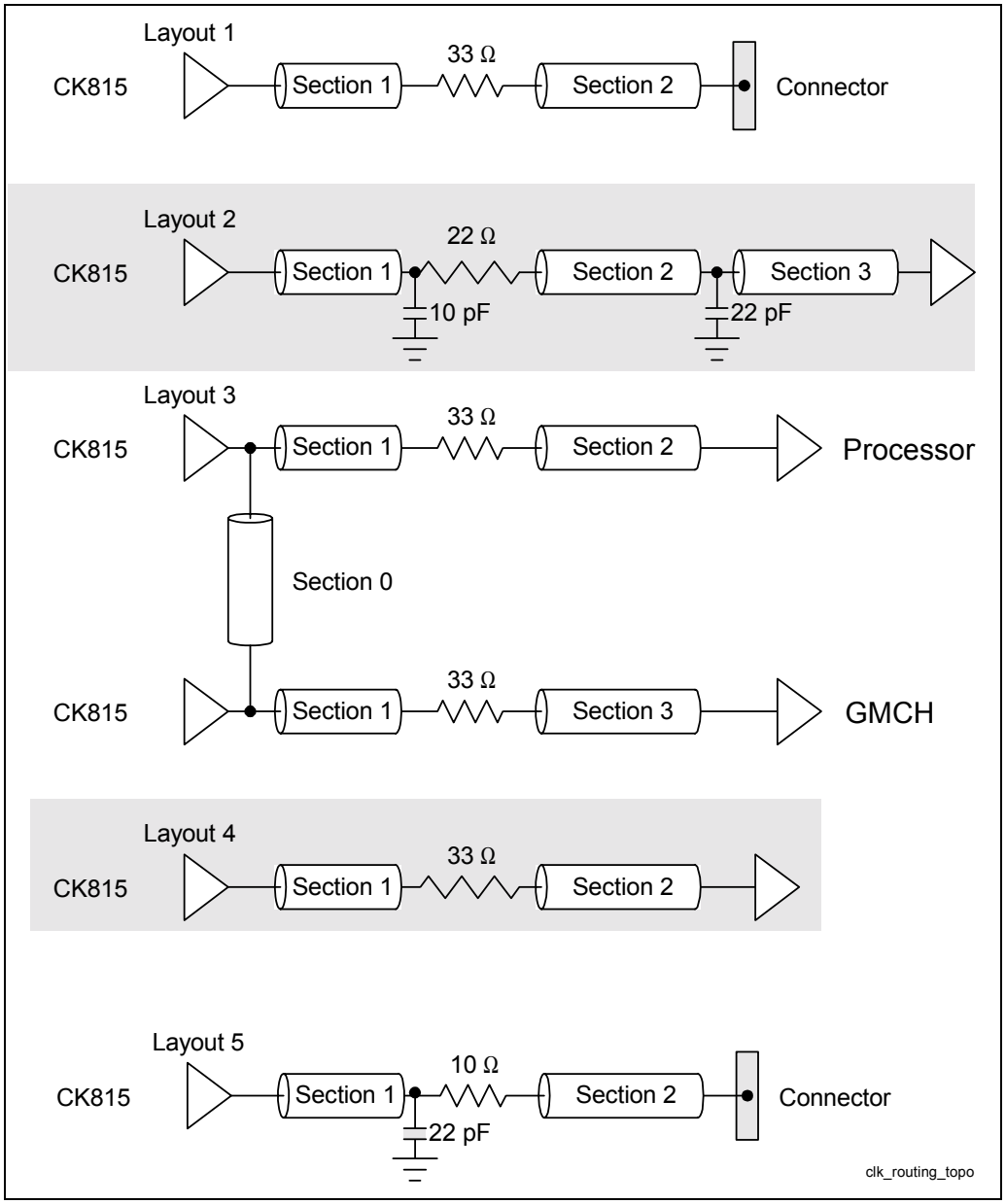


Table 42. Simulated Clock Routing Solution Space

Destination	Topology from Previous Figure	Section 0 Length	Section 1 Length	Section 2 Length	Section 3 Length
SDRAM MCLK	Layout 5	N/A	< 0.5”	A[1]	N/A
MCH SCLK[3]	Layout 2	N/A	< 0.5”=L1	A + 3.5” – L1	0.5”
Processor BCLK	Layout 3	< 0.1”	< 0.5”	A + 5.2”	A + 8”
MCH HCLK			<0.5”		
MCH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH2 HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH2 PCICLK	Layout 4	N/A	<0.5”	A + 8”	N/A
AGP CLK	Layout 4	N/A	<0.5”	A + 3" to A + 4"	N/A
PCI down[2]	Layout 4	N/A	<0.5”	A + 8.5” to A + 14”	N/A
PCI slot[2]	Layout 1	N/A	<0.5”	A + 5” to A + 11”	

NOTES:
1. Length “A” has been simulated up to 6 inches. The length must be matched between SDRAM MCLK lines by ±100 mils.
2. All PCI clocks must be within 6 inches of the ICH2 PCICLK route length. Routing on PCI add-in cards must be included in this length. In the presented solution space, ICH2 PCICLK was considered to be the shortest in the 6 inches trace routing range, and other clocks were adjusted from there. The system designer may choose to alter the relationship of PCI device and slot clocks, as long as all PCI clock lengths are within 6 inches. Note that the ICH2 PCICLK length is fixed to meet the skew requirements of ICH2 PCICLK to ICH2 HUBCLK.
3. 22 pf Load cap should be placed 0.5 inch from MCH Pin.

General Clock Layout Guidelines

- All clocks should be routed 5 mils wide with 15 mil spacing to any other signals.
- It is recommended to place capacitor sites within 0.5 inch of the receiver of all clocks. They are useful in system debug and AC tuning.
- Series resistor for clock guidelines: 22 Ω for MCH SCLK and SDRAM clocks. All other clocks use 33 Ω.
- Each DIMM clock should be matched within ±10 mils.

Clock Decoupling

Several general layout guidelines should be followed when laying out the power planes for the CK815 clock generator, as follows:

- Isolate power planes to the each of the clock groups.
- Place local decoupling as close as possible to power pins, and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to a plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14 mil finished hole with a 24 mil to 26 mil path. An example power via is an 18 mil finished hole with a 33 mil to 38 mil path. For large decoupling or power planes with large current transients, a larger power via is recommended.

11.4 Clock Driver Frequency Strapping

A CK-815-compliant clock driver device uses two of its pins to determine whether processor clock outputs should run at 133 MHz, 100 MHz or 66 MHz. The pin names are SEL0 and REF0. In addition, a third strapping pin is defined (SEL1), which must be pulled High for normal clock driver operation.

SEL0 and REF0 are driven by either the processor, which depends on the processor populated in the 370-pin socket, or pull-up resistors on the motherboard. While SEL0 is a pure input to a CK-815-compliant clock driver, REF0 is also the 14 MHz output that drives the ICH2 and other devices on the platform. In addition to sampling BSEL[1:0] at reset, CK-815-compliant clock drivers are configured by the BIOS via a two-wire interface to drive SDRAM clock outputs at either 100 MHz (default) or 133 MHz (if all system requirements are met).

11.5 Clock Skew Assumptions

The clock skew assumptions in are used in the system clock simulations.

Table 43. Simulated Clock Skew Assumptions

Skew Relationships	Target	Tolerance (±)	Notes
HCLK @ MCH to HCLK @ processor	0 ns	150 ps	Assumes ganged clock outputs will allow max of 50 ps skew
HCLK @ MCH to SCLK @ MCH	0 ns	600 ps	500 ps pin-to-pin skew 100 ps board/package skew
SCLK @ MCH to SCLK @ SDRAM	0 ns	630 ps	250 ps pin-to-pin skew 380 ps board + DIMM variation
HLCLK @ MCH to SCLK @ MCH	0 ns	900 ps	• 500 ps pin-to-pin skew • 400 ps board/package skew
HLCLK @ MCH to HCLK @ MCH	0 ns	700 ps	• 500 ps pin-to-pin skew • 200 ps board/package skew
HLCLK @ MCH to HLCLK @ ICH	0 ns	375 ps	• 175 ps pin-to-pin skew • 200 ps board/package skew
HLCLK @ ICH to PCICLK @ ICH	0 ns	900 ps	• 500ps pin-to-pin skew • 400 ps board/package skew
PCICLK @ ICH to PCICLK @ other PCI devices	0 ns	2.0-ns window	• 500 ps pin-to-pin skew • 1.5 ns board/add-in skew
HLCLK @ MCH to AGPCLK @ connector			• Total electrical length of AGP connector + add-in card is 750 ps (according to AGP2.0 spec and AGP design guide 1.0). • Motherboard clock routing must account for this additional electrical length. Therefore, AGPCLK routed to the connector must be shorter than HLCLK to the MCH, to account for this additional 750 ps.

11.6 Intel® CK-815 Power Gating on Wake Events

For systems providing functionality with the future 0.13 micron socket 370 processors, special handling of wake events is required. When a wake event is triggered, the MCH and the CK-815 must not sample BSEL[1:0] until the signal VTTPWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the CK-815-compliant clock driver until schematic signal VTTPWRGD12 is asserted.
2. Clocks to the ICH2 stabilize before the power supply asserts PWROK to the ICH2. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus it is necessary to gate PWROK to the ICH2 from the power supply while the CK-815 is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.
3. ICH2 takes the MCH out of reset.
4. MCH samples BSEL[1:0]. CK-815 will have sampled BSEL[1:0] much earlier.

Refer to Section 4.3 for full implementation details.

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12 Power Delivery

12.1 Power Delivery Guidelines

This chapter contains power delivery guidelines. Table 44 provides definitions fro power delivery terms used in this chapter.

Table 44. Power Delivery Definitions

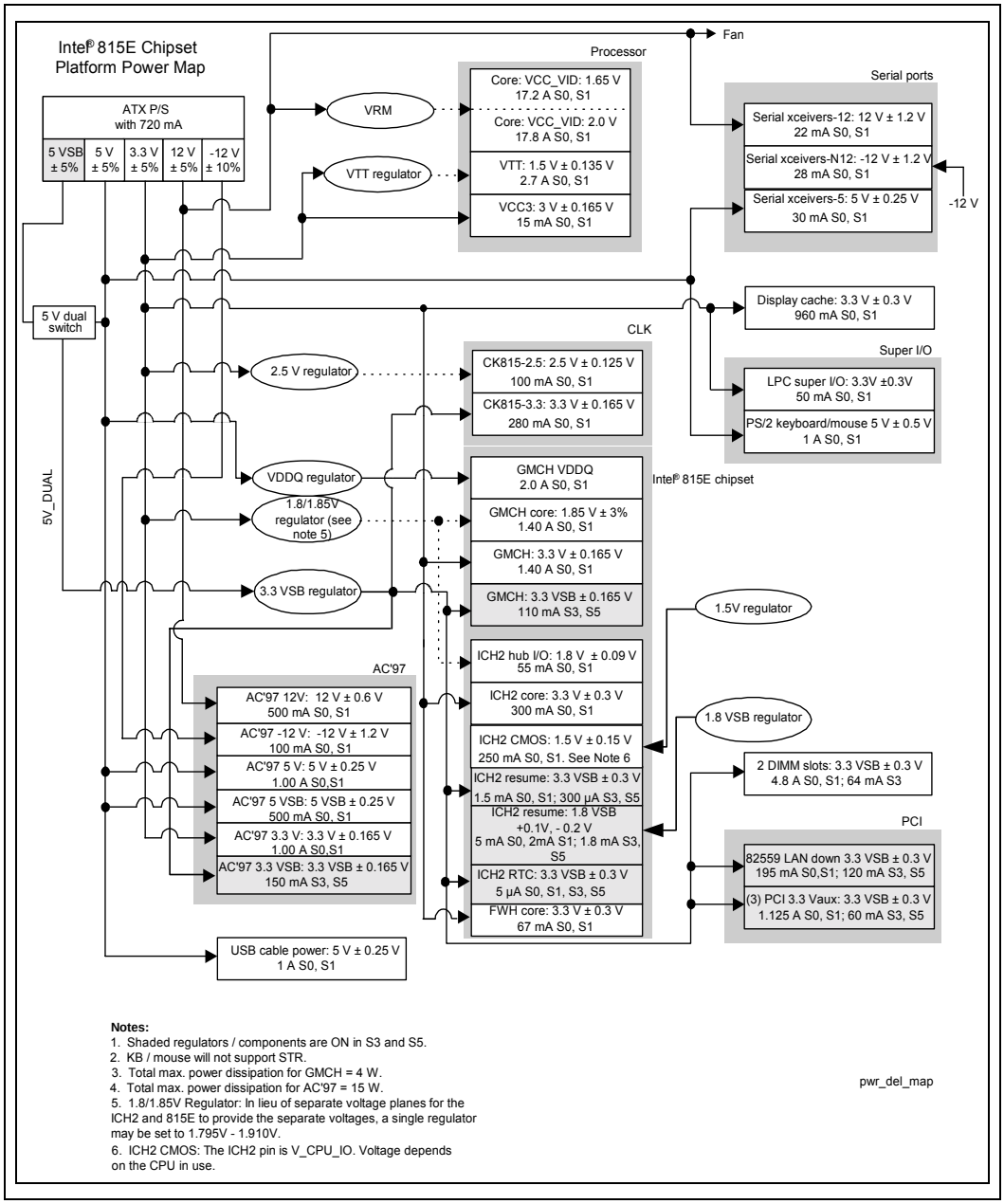
Term	Description
Suspend-To-RAM (STR):	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board (CRB) to satisfy the S3 ACPI power management state.
Full-power operation:	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (processor stop-grant state) state.
Suspend operation:	During suspend operation, power is removed from some components on the motherboard. The CRB supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Power rails:	An ATX power supply has 6 power rails: +5 V, –5 V, +12 V, –12 V, +3.3 V, 5VSB. In addition to these power rails, several other power rails are created with voltage regulators on the CRB.
Core power rail:	A power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are: ±5 V, ±12 V and +3.3 V.
Standby power rail:	A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5VSB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail:	A *derived* power rail is any power rail that is generated from another power rail. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator (on the CRB, 3.3VSB is derived from 5V_DUAL).
Dual power rail:	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

Figure 101 shows the power delivery architecture for an example system based on the 815EP platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the *suspend-to-RAM* (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH2 resume well, PCI wake devices (via 3.3 Vaux), AC ’97, and optionally USB. (USB can be powered only if sufficient standby power is

available.) To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device's power requirements, both in *suspend* and in *full-power*. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a *dual* power rail.

The solutions in this design guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 101. Power Delivery Map



In addition to the power planes provided by the ATX power supply, an *instantly available* 815EP universal platform (using *Suspend-to-RAM)* requires six power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the CRB will have a *5V Dual Switch*.

12.1.1 5V Dual Switch

This switch will power the *5V Dual plane* from the 5 V core ATX supply during *full-power* operation. During *Suspend-to-RAM,* the *5V Dual plane* will be powered from the 5 V Standby power supply.

Note: The voltage on the 5V Dual plane **is not 5 V!** There is a resistive drop through the *5V Dual Switch* that must be considered. Therefore, **no components** should be connected directly to the 5V Dual plane. On the CRB, the only devices connected to the 5V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in an 815EP universal socket 370 platform that does not support Suspend-to-RAM (STR).

12.1.2 VTT

This power plane is used to power the AGTL/AGTL+ termination resistors. Refer to the latest revisions of:

- Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) Datasheets

Note: This regulator is required in ALL designs.

12.1.3 1.85 V

The 1.85 V plane powers the MCH core and the ICH2 hub interface I/O buffers. This power plane has a total power requirement of approximately 1.7 A. The 1.85 V plane should be decoupled with a 0.1 µF and a 0.01 µF chip capacitor at *each* corner of the MCH, and with a single 1 µF and 0.1 µF capacitor at the ICH2.

Note: Note: This regulator is required in **all** designs.

12.1.4 VDDQ

The VDDQ plane is used to power the MCH AGP interface. Refer to the AGP Interface Specification Revision 2.0 (http://www.agpforum.org) and ECR#43 and ECR#44 for specific VDDQ delivery requirements.

For the consideration of component long-term reliability, the following power sequence is strongly recommended while the AGP interface of MCH is running at 3.3 V. If the AGP interface is running at 1.5 V, the following power sequence recommendation is no longer applicable. The power sequence recommendations are:

- During the power-up sequence, the 1.85 V must ramp up to 1.0 V **before** 3.3 V ramps up to 2.2 V
- During the power-down sequence, the 1.85 V **cannot** ramp below 1.0 V **before** 3.3 V ramps below 2.2 V
- The same power sequence recommendation also applies to the entrance and exit of S3 state, since MCH power is compete off during the S3 state.

Refer to Section 12.4.2 for more information on the power ramp sequence requirement between 3.3 V and 1.85 V. System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply. For further details on the voltage sequencing requirements, refer to the *Intel® 815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH) for use with the Universal Socket 370* Datasheet.

Note: This regulator is required in ALL designs (unless the design does not support 1.5 V AGP, and therefore does not support 4X AGP).

12.1.5 3.3VSB

The 3.3VSB plane powers the I/O buffers in the resume well of the ICH2 and the PCI 3.3Vaux suspend power pins. The 3.3Vaux requirement state that during suspend, the system must deliver 375 mA to each *wake-enabled* card and 20 mA to each *non wake-enabled* card. During *full-power* operation, the system must be able to supply 375 mA to *EACH* card. Therefore, the total current requirement is:

- *Full-power Operation:* 375 mA * number of PCI slots
- *Suspend Operation:* 375+20 mA* (number of PCI slots – 1)

In addition to the PCI 3.3Vaux, the ICH2 suspend well power requirements must be considered as shown in Figure 101.

Note: This regulator is required in ALL designs.

12.1.6 1.85VSB

The 1.85VSB plane powers the logic to the resume well of the ICH2. This should not be used for VCMOS.

12.1.7 VCMOS

The VCMOS plane is used to power the processor CMOS signals. In non-universal socket 370 platforms, the 1.5 V plane used by VTT also provided VCMOS. Given that VTT can be either 1.25 V or 1.5 V in a universal socket 370 platform, it is necessary to provide VCMOS as its own separate plane.

12.2 Thermal Design Power

The Thermal Design power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP of the MCH component is 5.1 W. The TDP of the ICH2 is 1.5 W ± 15%.

12.2.1 Pull-Up and Pull-Down Resistor Values

The pull-up and pull-down values are system dependent. The appropriate value for a system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, the input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high-voltage/low-voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be performed to determine the minimum/maximum values usable on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, and other considerations.

A simplistic DC calculation for a pull-up value is:

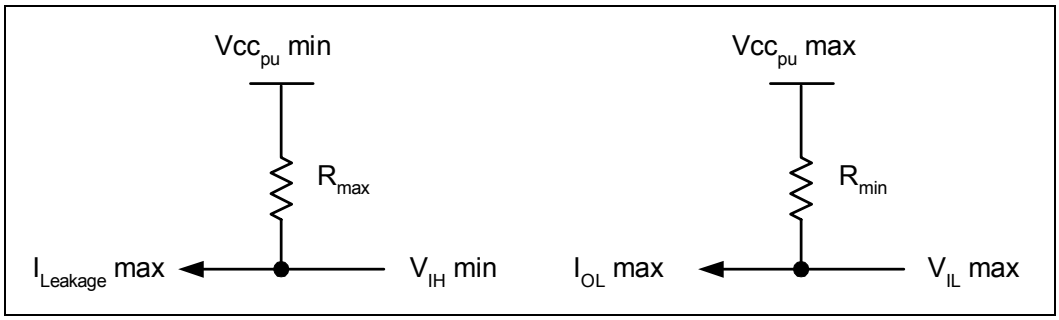
$$R_{MAX} = (VCC_{PU}\,MIN - V_{IH}\,MIN) / I_{LEAKAGE}\,MAX$$

$$R_{MIN} = (VCC_{PU}\,MAX - V_{IL}\,MAX) / I_{OL}\,MAX$$

Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} also is determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including the input capacitance of the devices to be driven, the output capacitance of the driver, and the line capacitance. This calculation yields the largest pull-up resistor allowable to meet the rise time t.

$$R_{MAX} = -t / (C * \ln(1-(V_{IH}\,MIN / VCC_{PU}\,MIN)))$$

Figure 102. Pull-Up Resistor Example



12.3 ATX Power Supply PWRGOOD Requirements

The PWROK signal must be glitch free for proper power management operation. The ICH2 sets the PWROK_FLR bit (ICH2 GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at offset A2h). If this bit is set upon resume from S3 power-down, the system will reboot and control of the system will not be given to the program running when entering the S3 state. System designers should insure that PWROK signal designs are glitch free.

12.4 Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH2 integrates 16 ms debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH2 to detect power failure.
- It is recommended that the ATXPWROK signal from the power supply connector be routed through a Schmitt trigger to square-off and maintain its signal integrity. It should not be connected directly to logic on the board.
- PWROK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, while making sure that the input to the ICH2 is at the 3 V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also ensure that voltage on RSMRST# does not exceed VCC(RTC).
- It is recommended that 3.3 V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3 V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V, using a 330 Ω resistor. It also has a 1.8 KΩ pull-down to ground.
- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH2 suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.
- SLP_S3# from the ICH2 must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is Low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

12.4.1 Power Button Implementation

The following items should be considered when implementing a power management model for a desktop system. The power states are as follows:

- S1 – Stop Grant – (processor context not lost)
- S3 - STR (Suspend to RAM)
- S4 - STD (Suspend to Disk)
- S5 - Soft-off

Note the following:

1. *Wake:* Pressing the power button wakes the computer from S1–S5.
2. *Sleep:* Pressing the power button signals software/firmware in the following manner:
   a. If SCI is enabled, the power button will generate an SCI to the OS.
      1. The OS will implement the power button policy to allow orderly shutdowns.
      2. Do not override this with additional hardware.
   b. If SCI is not enabled:
      1. Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
      2. Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
      3. Always install an SMI handler for the power button that operates until ACPI is enabled.
3. *Emergency Override:* Pressing the power button for 4 seconds goes directly to S5.
   a. This is only to be used in EMERGENCIES when system is not responding.
   b. This will cause the user data to be lost in most cases.
4. Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off. This violates ACPI.
5. To be compliant with the latest PC9x specification, machines must appear to the user to be off when in the S1–S4 sleeping states. This includes:
   a. All lights, except a power state light, must be off.
   b. The system must be inaudible: silent or stopped fan, drives off.

Note: Contact Microsoft for the latest information concerning PC9x and Microsoft Logo programs.

12.4.2 1.85 V/3.3 V Power Sequencing

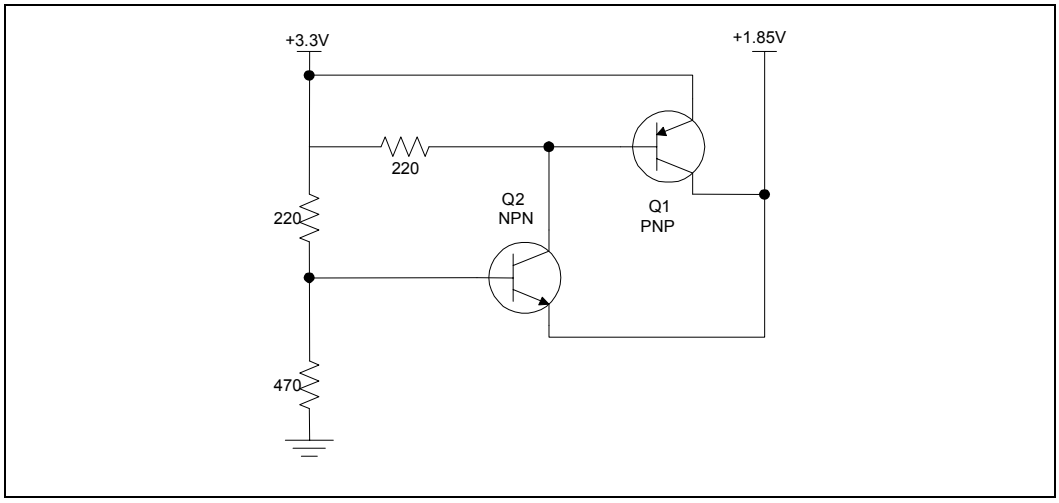
The ICH2 has two pairs of associated 1.85 V and 3.3 V supplies. These are {VCC1_85, VCC3_3} and {VCCSus1_85, VCCSus3_3}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0 V.** The 1.85 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.85 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violation of the 2 V Rule is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.85 V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.85 V logic is powered up. Some signals that are defined as “Input-only” actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.85 V supply is not.

Figure 103 shows an example power-on sequencing circuit that ensures the 2 V Rule is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.85 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.85 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.85 V plane, current will not flow from the 3.3 V supply into 1.85 V plane when the 1.85 V plane reaches 1.85 V.

Figure 103. Example 1.85 V/3.3 V Power Sequencing Circuit



When analyzing systems that may be “marginally compliant” to the 2 V Rule, pay close attention to the behavior of the ICH2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the resume wells.
- PWROK controls isolation between the resume wells and main wells

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

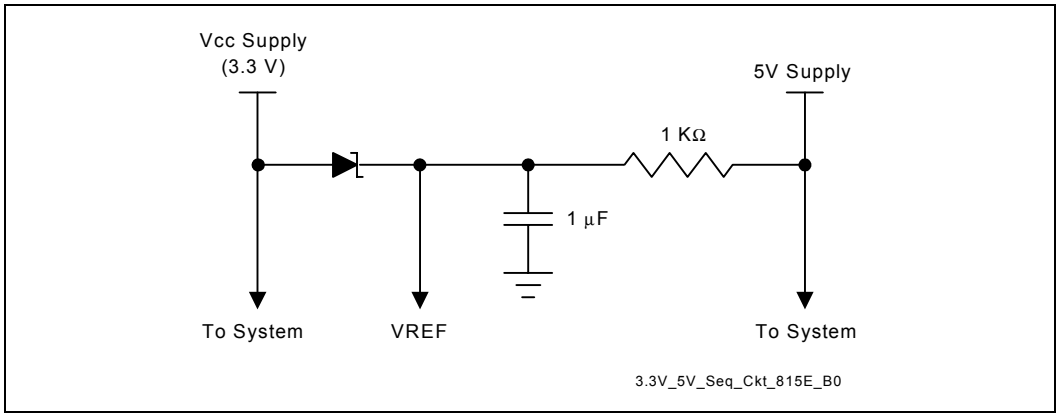
12.4.3 3.V/V5REF Sequencing

V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0 .7 V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 104 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 rail and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

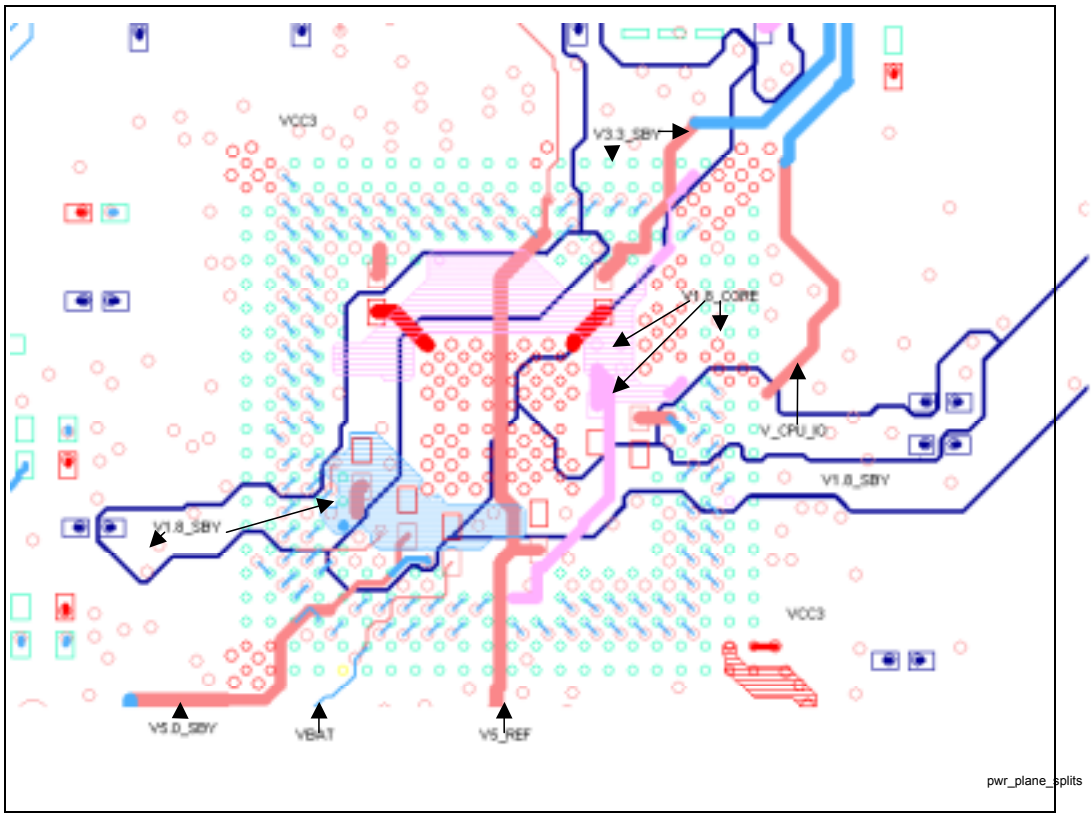
As an additional consideration, during suspend the only signals that are 5 V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX, which remains powered during S5.

Figure 104. 3.3 V/V5REF Sequencing Circuitry



12.5 Power Plane Splits

Figure 105. Power Plane Split Example



12.6 Glue Chip 3 (ICH2 Glue Chip)

To reduce the component count and BOM cost of the ICH2 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The Glue Chip 3 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- PWROK signal generation
- Control circuitry for Suspend To RAM
- Power Supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for suspend to RAM
- 5 V reference generation
- Flash FLUSH# / INIT# circuit
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for Audio MIDI signal
- Audio-disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test

More information regarding this component is available from the following vendors.

Vendor	Contact	Contact Information
Fujitsu Microelectronics	Customer Response Center	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 *phone:* 1-800-866-8600 *fax:* 1-408-922-9179 *email:* fmicrc@fmi.fujitsu.com
Mitel Semiconductor	Greg Kizik Regional Business Manager	1735 Technology Drive Suite 240 San Jose, CA 95110 *phone:* 408-451-4723 *fax*: 408-451-4710 *e-mail:* greg_kizik@mitel.com http://www.mitelsemi.com

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13 System Design Checklist

13.1 Design Review Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an 815EP chipset platform for use with the universal socket 370 platform. This is not a complete list and does not guarantee that a design will function properly.

The following set of tables provides design considerations for the various portions of a design. Each table describes one of those portions and is titled accordingly. Contact your Intel Field Representative in the event of questions or issues regarding the interpretation of the information in these tables.

13.2 Processor Checklist

13.2.1 GTL Checklist

Checklist Items	Recommendations
A[35:3]# [1]	• Connect A[31:3]# to MCH. Leave A[35:32]# as No Connect (not supported by chipset).
BNR#, BPRI#, DBSY#, DEFER#, DRDY#, D[63:0]#, HIT#, HITM#, LOCK#, REQ[4:0]#, RS[2:0]#, TRDY#	• Connect to MCH.
ADS#	• Resistor site for 56 Ω pull-up to VTT placed within 150 mils of MCH for debug purpose. Connect to MCH.
BREQ[0]# (BR0#)	• 33 Ω pull-down resistor to ground
RESET# (AH4)	• Terminate to VTT through 86 Ω resistor, decoupled through 22 Ω resistor in series with 10 pF capacitor to ground. Connect to MCH. For ITP, also connect to ITP pin 2 (RESET#) with 240 Ω series resistor.
RESET2# (X4)	• 1 kΩ series resistor to RESET#.

13.2.2 CMOS Checklist

Checklist Items	Recommendations
IERR#	• 150 Ω pull-up resistor to VCC_{CMOS} if tied to custom logic, or leave as No Connect (not used by chipset)
PREQ#	• 200–300 Ω pull-up resistor to VCC_{CMOS} / Connect to ITP or else leave as No Connect.
THERMTRIP#	• See Section 5.3.1.
A20M#, IGNNE#, INIT#, INTR, NMI, SLP#, SMI#, STPCLK#	• Connect to ICH2. External pull-ups are not needed.
FERR#	• Requires 150 Ω pull-up to VCC_{CMOS}/Connect to ICH2.
FLUSH#	• Requires 150 Ω pull-up to $VCC_{CMOS.}$ (Not used by chipset.)
PWRGOOD	• 330 Ω pull-up to VCC2_5 /1.8 kΩ pull-down resistor to ground /Connect to POWERGOOD logic.

13.2.3 TAP Checklist for 370-Pin Socket Processors

Checklist Items	Recommendations
TCK	• 39 Ω pull-down resistor to ground / Connect to ITP.
TMS	• 39 Ω pull-up resistor to VCMOS / Connect to ITP
TDI	• 200–330 Ω pull-up resistor to VCMOS / Connect to ITP.
TDO	• 150 Ω pull-up resistor to VCMOS / Connect to ITP.
TRST#	• 500-680 Ω pull-down resistor to ground / Connect to ITP.
PRDY#	• Pull-up resistor that matches GTL characteristic impedance to VTT / 240 Ω series resistor to ITP.

Note: Resistors need to be placed within 1’’ of the TAP connector.

13.2.4 Miscellaneous Checklist for 370-Pin Socket Processors

Checklist Items	Recommendations
BCLK	• Connect to clock generator. / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the MCH and processor.
BSEL0	• **Case 1 (66/100/133 MHz support):** 1 kΩ pull-up resistor to 3.3 V. Connect to CK815 SEL0 input. Connect to MCH LMD29 pin via 10 kΩ series resistor. • **Case 2 (100/133 MHz support):** 1 kΩ pull-up resistor to 3.3 V. Connect to PWRGOOD logic such that a logic Low on BSEL0 negates PWRGOOD.
BSEL1	• 1 kΩ pull-up resistor to 3.3 V. Connect to CK815 REF pin via 10 kΩ series resistor. Connect to MCH LMD13 pin via 10 kΩ series resistor.
CLKREF	• Connect to divider on VCC2.5 or VCC3.3 to create 1.25 V reference with a 4.7 µF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. Do not use VTT as source voltage for this reference!
CPUPRES#	• Tie to ground. Leave as No Connect or connect to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1 kΩ to 10 kΩ pull-up resistor to VCC_{CMOS}.
DYN_OE	• 1 kΩ pull-up resistor to VTT.
PICCLK	• See Section 10.5.
PICD[1:0]	• 150 Ω pull-up resistor to VCC_{CMOS}/Connect to ICH2.
PLL1, PLL2	• Low-pass filter on VCC_{CORE} provided on motherboard. Typically a 4.7 µH inductor in series with VCC_{CORE} is connected to PLL1, and then through a series 33 µF capacitor to PLL2.
RTTCTRL (S35)	• 56 Ω ± 1% pull-down resistor to ground.
SLEWCTRL (E27)	• 110 Ω ± 1% pull-down resistor to ground.
STPCLK# (AG35)	• Connect to ICH2.
THERMDN, THERMDP	• No Connect if not used. Otherwise, connect to thermal sensor using vendor guidelines.
VCC2.5	• No connect for Intel® Pentium® III processors
GTL_REF/ CMOSREF (AK22)	• Connect to a 1.0 V voltage divider derived from VCC_{CMOS}. See Section 4.2.7.
VCC_{CORE}	• 16 ea. (min.) 4.7 µF in 1206 package all placed within the PGA370 socket cavity. • 8 ea. (min.) 1 µF in 0612 package placed in the PGA370 socket cavity.
VID[25mV, 3:0]	• Connect to on-board VR or VRM. 25mV should connect to VID25mV. For on-board VR, 10 kΩ pull-up resistor to power solution-compatible voltage is required (usually pulled up to input voltage of the VR). Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.
VTTPWRGD	• Pull up to VTT through 1 kΩ resistor and connect to VTTPWRGD circuitry.

Checklist Items	Recommendations
VREF[6:0]	• Connect to VREF voltage divider made up of 75 Ω and 150 Ω 1% resistors connected to VTT. Processor VREF must be able to be separate from chipset VREF. • Decoupling Guidelines: • 4 ea. (min.) 0.1 µF in 0603 package placed within 500 mils of VREF pins
VTT	• Connect AH20, AK16, AL13, AL21, AN11, AN15, G35, G37, AD36, AB36, X34, AA33, AA35, AN21, E23, S33, S37, U35, and U37 to VRM regulators compliant with Intel® VRM guidelines for future 0.13 micron processors.. Provide high- and low-frequency decoupling. • Decoupling Guidelines: • 20 ea (min.) 0.1 µF in 0603 package placed as near the VTT processor pins as possible. • 4 ea (min.) 0.47 µF in 0612 package
NO CONNECTS	• The following pins must be left as no-connects: A29, A31, A33, AC37, AJ3, AK24, AK30, AL1, AL11, AM2, AN13, AN23, B36, C29, C31, C33, C35, E21, E29, E31, E35, E37, F10, G33, L33, N33, N35, Q33, Q35, Q37, R2, V4, W35, X2, Y1, Z36.
AJ3	• See Table 2 and Section 4.2.1.
EDGCTRL (AG1)	• See Table 2 Section 4.2.4
DETECT (AF36)	• See Table 2 Section 4.2.2
NCHCTRL (N37)	• 14 Ω pull-up resistor to VTT.

13.3 MCH Checklist

13.3.1 AGP Interface 1X Mode Checklist

Checklist Items	Recommendations
RBF#, WBF#, PIPE#, GREQ#, GGNT#, GPAR, GFRAME#, GIRDY#, GTRDY#, GSTOP#, GDEVSEL#, GPERR#, GSERR#, ADSTB0, ADSTB1, SBSTB	• Pull up to VDDQ through 8.2 kΩ
ADSTB0#, ADSTB1#, SBSTB#	• Pull down to ground through 8.2 kΩ
PME#	• Connect to PCI connector 0 device Ah. / Connect to PCI connector 1 device Bh. / Connect to 82559 LAN (if implemented).
TYPEDET#	• Connect to AGP voltage regulator circuitry / AGP reference circuitry.
PIRQ#A, PIRQ#B	• Pull up to 5 V through 2.7 kΩ. / Follow ref. schematics (other device connections).

13.3.2 Designs That Do Not Use the AGP Port

Any external graphics implementation not using the AGP port should terminate the MCH AGP control and strobe signals in the following way:

Table 45. Recommendations for Unused AGP Port

Signal	Pull up / Pull Down
FRAME#	Pull-up to +VDDQ
TRDY#	Pull-up to +VDDQ
IRDY#	Pull-up to +VDDQ
DEVSEL#	Pull-up to +VDDQ
STOP#	Pull-up to +VDDQ
SERR#	Pull-up to +VDDQ
PERR#	Pull-up to +VDDQ
RBF#	Pull-up to +VDDQ
WBF#	Pull-up to +VDDQ
INTA#	Pull-up to +VDDQ
INTB#	Pull-up to +VDDQ
PIPE#	Pull-up to +VDDQ
REQ#	Pull-up to +VDDQ
GNT#	Pull-up to +VDDQ
GPAR	Pull-down to Ground using a 100 kΩ resistor
AD_STB[1:0]	Pull-up to +VDDQ
SB_STB	Pull-up to +VDDQ
AD_STB[1:0]#	Pull-down to Ground
SB_STB#	Pull-down to Ground
ST[2:0]	Pull-up to +VDDQ

13.3.3 System Memory Interface Checklist

Checklist Items	Recommendations
SMAA12	• Connect MCH through 10 kΩ resistor to transistor junction as per Chapter 4 for systems supporting the *universal PGA370* design.
SMAA9	• Connect 10 kΩ to ground.

13.3.4 Hub Interface Checklist

Checklist Items	Recommendations
HUBREF	• Connect to HUBREF generation circuitry.
HL_COMP	• Pull up to VCC1.85 through 40 Ω (both MCH and ICH2 side).

13.4 Intel® ICH2 Checklist

13.4.1 PCI Interface

Checklist Items	Recommendations
All	• All inputs to the ICH2 must not be left floating. Many GPIO signals are fixed inputs that must be pulled up to different sources.
PERR#, SERR# PLOCK#, STOP# DEVSEL#, TRDY# IRDY#, FRAME# REQ[4:0] #, GPIO[1:0], THRM#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3.3 or a 2.7 kΩ pull-up resistor to VCC5. See PCI 2.2 Component Specification for pull-up recommendations for VCC3.3 and VCC5.
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal. • 33 Ω series resistor to IDE connectors.
PCIGNT#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to VCC3.3.
PME#	• No extra pull-up resistors This signal has an integrated pull-up resistor of 24 kΩ.
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to VCC3.3 is recommended.
GNT[A]#, /GPIO[16], GNT[B]/ GNT[5]#/ GPIO[17]	• No extra pull-up needed. These signals have integrated pull-ups of 24 kΩ. • GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.

13.4.2 Hub Interface

Checklist Items	Recommendations
HL11	• No pull-up resistor required. Use a no-stuff or a test point to put the ICH2 into NAND chain mode testing
HL_COMP	• Tie the COMP pin to a 40Ω 1% or 2% (or 39 Ω 1%) pull-up resistor (to VCC1.85) via a 10 mil wide, very short (~0.5 inch) trace. ZCOMP No longer supported.

13.4.3 LAN Interface

Checklist Items	Recommendations
LAN_CLK	• Connect to LAN_CLK on Platform LAN Connect Device.
LAN_RXD[2:0]	• Connect to LAN_RXD on Platform LAN Connect Device. ICH2 contains integrated 9 kΩ pull-up resistors on interface.
LAN_TXD[2:0] LAN_RSTSYNC	• Connect to LAN_TXD on Platform LAN Connect Device.

NOTES:
1. LAN connect interface can be left NC if not used. Input buffers internally terminated.
2. In the event of EMI problems during emissions testing (FCC Classifications) you may need to place a decoupling cap (~470 pF) on each of the 4 LED pins. Reduces emissions attributed to LAN subsystem.

13.4.4 EEPROM Interface

Checklist Items	Recommendations
EE_DOUT	• Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector. • Connected to EEPROM data input signal (input from EEPROM perspective and output from ICH2 perspective).
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector. ICH2 contains an integrated pull-up resistor for this signal. • Connected to EEPROM data output signal (output from EEPROM perspective and input from ICH2 perspective).

13.4.5 FWH/LPC Interface

Checklist Items	Recommendations
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	• No extra pull-ups required. ICH2 Integrates 24 kΩ pull-up resistors on these signal lines.

13.4.6 Interrupt Interface

Checklist Items	Recommendations
PIRQ#[D:A]	• These signals require a pull-up resistor. The recommendation is a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3. • In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the ICH2 datasheet. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19.

Checklist Items	Recommendations
PIRQ#[G:F]/ GPIO[4:3]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3. • In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the ICH2 datasheet. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23.
PIRQ#[H] PIRQ#[E]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3.3. • Since PIRQ[H]# and PIRQ[E]# are used internally for LAN and USB controllers, they cannot be used as GPIO(s) pin.
APIC	• If the APIC is used: — 150 Ω pull-up resistors on APICD[0:1] — Connect APICCLK to CK133 with a 20–33 Ω series termination resistor. • If the APIC is not used on UP systems: — The APICCLK can either be tied to GND or connected to CK133, but not left floating. — Pull APICD[0:1] to GND through 10 kΩ pull-down resistors. — Use pull-downs for each APIC signal. Do not share resistor to pull signals up.

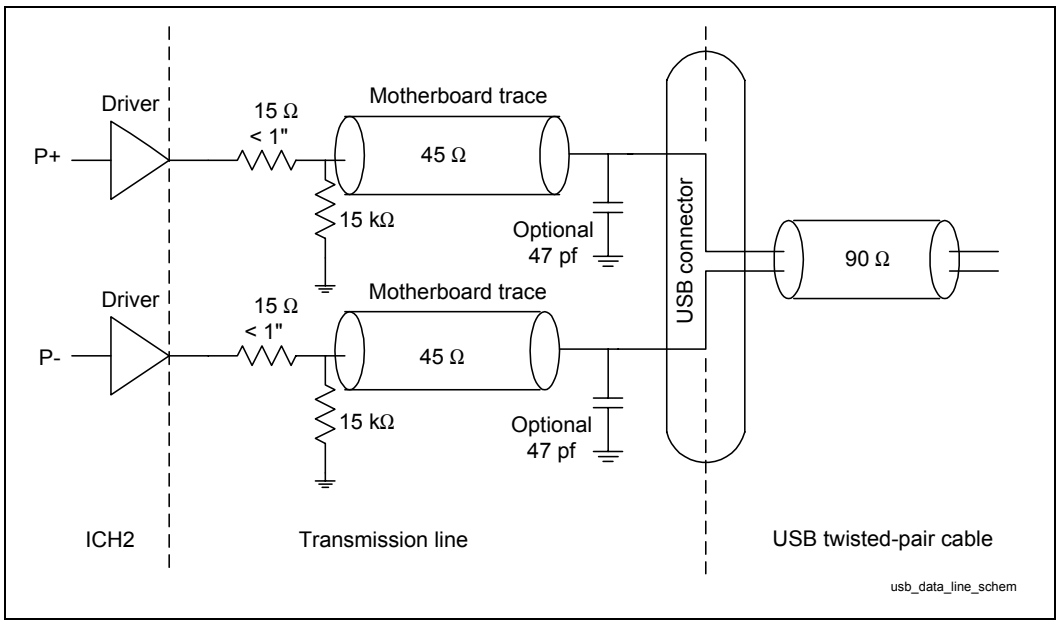
13.4.7 GPIO Checklist

Checklist Items	Recommendations
All	• Ensure ALL unconnected signals are OUTPUTS ONLY!
GPIO[7:0]	• These pins are in the main power well. Pull-ups must use the VCC3.3 plane. Unused core well inputs must either be pulled up to VCC3.3 or be pulled down. Inputs must not be allowed to float. These signals are 5 V tolerant. • GPIO[1:0] can be used as REQ[A:B]#. GPIO[1] can also be used as PCI REQ[5]#.
GPIO[8], [13:11]-	• These pins are in the resume power well. Pull-ups must use the VCCSUS3.3 plane. These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register. Unused **resume** well inputs must be pulled up to VCCSUS3.3. These signals are not 5 V tolerant. • These are the only GPIs that can be used as ACPI compliant wake events.
GPIO[23:16]	• Fixed as output only. Can be left NC. In main power well. GPIO22 is open drain.
GPIO[24,25,27,28]	• These I/O pins can be NC. These pins are in the resume power well.

13.4.8 USB

Checklist Items	Recommendations
USBP[3:0]P USBP[3:0]N	• See Figure 106 for circuitry needed on each differential Pair.
VCC USB (Cable power)	• It should be powered from the 5 V core instead of the 5 V standby, unless adequate standby power is available.
Voltage drop considerations	• The resistive component of the fuses, ferrite beads and traces must be considered when choosing components, and power and GND trace widths. Minimize the resistance between the VCC5 power supply and the USB ports to prevent voltage drop. • Sufficient bypass capacitance should be located near the USB receptacles to minimize the voltage drop that occurs during the hot plugging a new device. For more information, see the USB specification.
Fuse	• A fuse larger than 1A can be chosen to minimize the voltage drop.

Figure 106. USB Data Line Schematic



13.4.9 Power Management

Checklist Items	Recommendations
THRM#	• Connect to temperature Sensor. Pull-up if not used.
SLP_S3# SLP_S5#	• No pull-up/down resistors needed. Signals driven by ICH2.
PWROK	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and VCC1_8 have reached their nominal voltages. For systems implementing the *universal PGA370* design, this signal must be connected to the gating circuit found in Section 4.
PWRBTN#	• No extra pull-up resistors. This signal has an integrated pull-up of 24 kΩ.
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to resume well • If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCCSus3_3 and VCCSus1_8 have reached their nominal voltages. Requires a weak pull-down. Also requires well isolation control as directed in Section 10.8.6.

13.4.10 Processor Signals

Checklist Items	Recommendations
A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#	• Internal circuitry has been added to the ICH2, external pull-up resistors are not needed.
FERR#	• Requires Weak external pull-up resistor to VCC_{CMOS}.
RCIN# A20GATE	• Pull-up signals to VCC3.3 through a 10 kΩ resistor.
CPUPWRGD	• Connect to the processor's CPUPWRGD input. Requires weak external pull-up resistor.

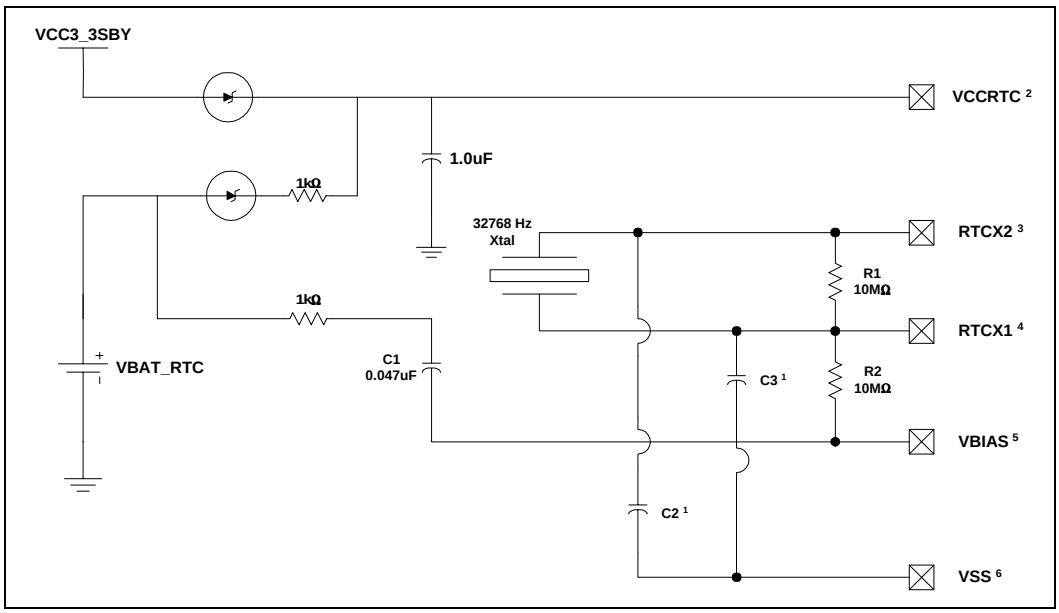
13.4.11 System Management

Checklist Items	Recommendations
SMBDATA SMBCLK	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pullup resistors. (core well, suspend well, or a combination.) • Value of pull-up resistors determined by line load. Typical value used is 8.2 kΩ.
SMBALERT#/ GPIO[11]	• See GPIO section if SMBALERT# not implemented
SMLINK[1:0]	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pullup resistors. (core well, suspend well, or a combination.) • Value of pull-up resistors determined by line load. Typical value used is 8.2 kΩ.
INTRUDER#	• Pull signal to VCCRTC (VBAT), if not needed.

13.4.12 RTC

Checklist Items	Recommendations
VBIAS	• The VBIAS pin of the ICH2 is connected to a .047 µF capacitor. See Figure 107
RTCX1 RTCX2	• Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling capacitors (assuming crystal with C_{LOAD} = 12.5 pF) at each signal. • The ICH2 implements a new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in Figure 107 below will be required to maintain the accuracy of the RTC. • The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds. • RTCX1 may optionally be driven by an external oscillator instead of a crystal. These signals are 1.85 V only, and must not be driven by a 3.3 V source.
RTCTST#	• Ensure 10–20 ms RC delay (8.2 KΩ and 2.2 µF). See Figure 81.
SUSCLK	• To assist in RTC circuit debug, route SUSCLK to a test point if it is unused.

Figure 107. Intel® ICH2 Oscillator Circuitry



NOTE: Capacitors C2 and C3 are crystal dependent

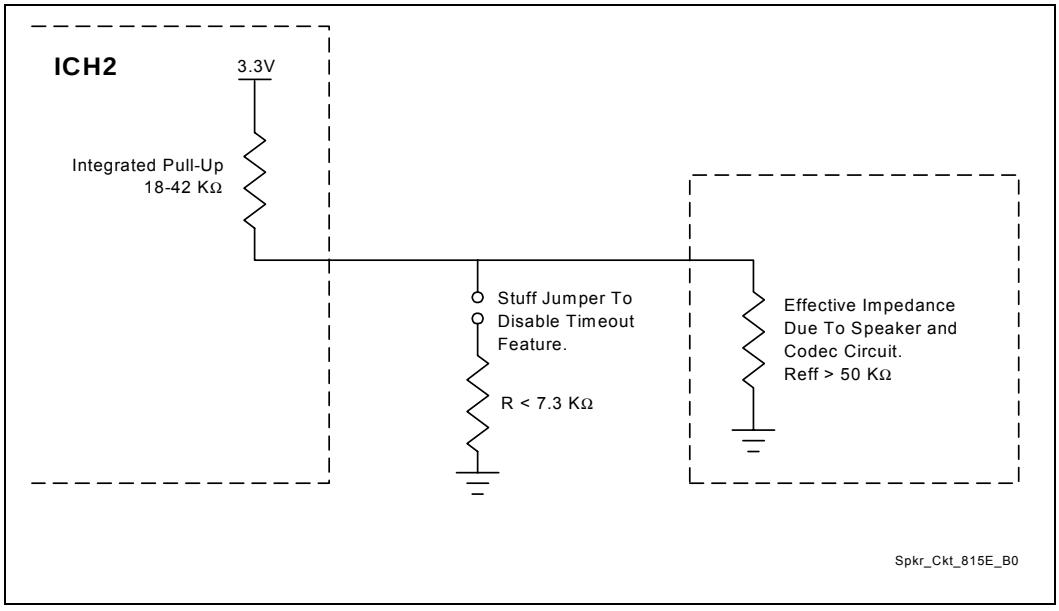
13.4.13 AC '97

Checklist Items	Recommendations
AC_BITCLK	• No extra pull-down resistors required. • When nothing is connected to the link, BIOS must set a shut off bit for the internal keeper resistors to be enabled. At that point, you do not need pull-ups/pull-downs on any of the link signals.
AC_SYNC	• No extra pull-down resistors required. Some implementations add termination for signal integrity. Platform specific.
AC_SDOUT	• Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation. • This pin has a weak internal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down.
AC_SDIN[1], AC_SDIN[0]	• Requires pads for weak 10 kΩ pull-downs. Stuff resistor for unused AC_SDIN signal or AC_SDIN signal going to the CNR connector. • AC_SDIN[1:0] are inputs to an internal OR gate. If a pin is left floating, the output of the OR gate will be erroneous. • If there is no codec on the system board, then both AC_SDIN[1:0] should be pull-down externally with resisters to ground.
CDC_DN_ENAB#	• If the primary codec is down on the motherboard, this signal must be low to indicate the motherboard codec is active and controlling the AC '97 interface.

13.4.14 Miscellaneous Signals

Checklist Items	Recommendations
SPKR	• No extra pull-up resistors. Has integrated pull-up of between 18 kΩ and 42 kΩ. The integrated pull-up is only enabled at boot/reset for strapping functions; at all other times, the pull-up is disabled. • A low effective impedance may cause the TCO Timer Reboot function to be erroneously disabled. • Effective Impedance due Speaker and Codec circuitry must be greater than 50 kΩ or a means to isolate the resistive load from the signal while PWROK is low be found. See Figure 108.
TP[0]	• Requires external pull-up resistor to VCCSUS3.3
FS[0]	• Rout to a test point. ICH2 contains an integrated pull-up for this signal. Test point used for manufacturing appears in XOR tree.

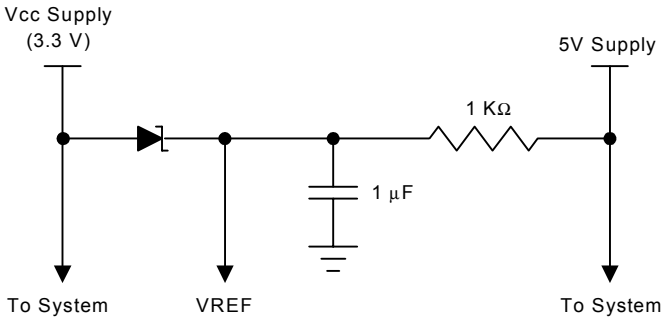
Figure 108. SPKR Circuitry



13.4.15 Power

Checklist Items	Recommendations
V_CPU_IO[1:0]	• The power pins should be connected to the proper power plane for the processor's CMOS Compatibility Signals. Use one 0.1 µF decoupling capacitor.
VCCRTC	• No clear CMOS jumper on VCCRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS
VCC3.3	• Requires six 0.1 µF decoupling capacitor
VCCSus3.3	• Requires one 0.1 µF decoupling capacitor.
VCC1.85	• Requires two 0.1 µF decoupling capacitor s.
VCCSus1.85	• Requires one 0.1 µF decoupling capacitor.
V5_REF SUS	• Requires one 0.1 µF decoupling capacitor. • V5REF_SUS affects 5V-tolerance for all USB pins and can be connected to VccSUS3_3 if ICH2 USB is not supported in the platform. If USB is supported, 5VREF_SUS must be connected to 5V_AUX, which remains powered during S5.
V5_REF	• V5REF is the reference voltage for 5 V tolerant inputs in the ICH2. Tie to pins VREF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. Refer to Figure 109 for an example circuit schematic that may be used to ensure the proper V5REF sequencing.
VCMOS	• VCMOS power source must supply 1.5 V and be generated by circuitry on the motherboard. Do not connect to VTT.

Figure 109. V5REF Circuitry



13.4.16 IDE Checklist

Checklist Items	Recommendations
PDD[15:0], SDD[15:0]	• No extra series termination resistors or other pull-ups/pull-downs are required. These signals have integrated series resistors. Note that simulation data indicates that the integrated series termination resistors can range from 31 Ω to 43 Ω. • PDD7/SDD7 does not require a 10 kΩ pull-down resistor. Refer to ATA ATAPI-4 specification.
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	• No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns. These signals have integrated series resistors. Note that simulation data indicates that the integrated series termination resistors can range from 31 Ω to 43 Ω.
PDREQ SDREQ	• No extra series termination resistors. No pull-down resistors needed. • These signals have integrated series resistors in the ICH2. These signals have integrated pull-down resistors in the ICH2.
PIORDY SIORDY	• No extra series termination resistors. These signals have integrated series resistors in the ICH2. Pull-up to VCC3.3 via a 4.7 kΩ resistor.
IRQ14, IRQ15	• Recommend 8.2 kΩ—10 kΩ pull-up resistors to VCC3.3. • No extra series termination resistors.
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.
Cable Detect:	• Host Side/Device Side Detection: — Connect IDE pin PDIAG/CBLID to an ICH2 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. • Device Side Detection: — Connect a 0.047 µF capacitor from IDE pin PDIAG/CBLID to GND. No ICH2 connection. Note that all ATA66/ATA100 drives will have the capability to detect cables

NOTE: The maximum trace length from the ICH2 to the ATA connector is 8 inches.

Figure 110. Host/Device Side Detection Circuitry

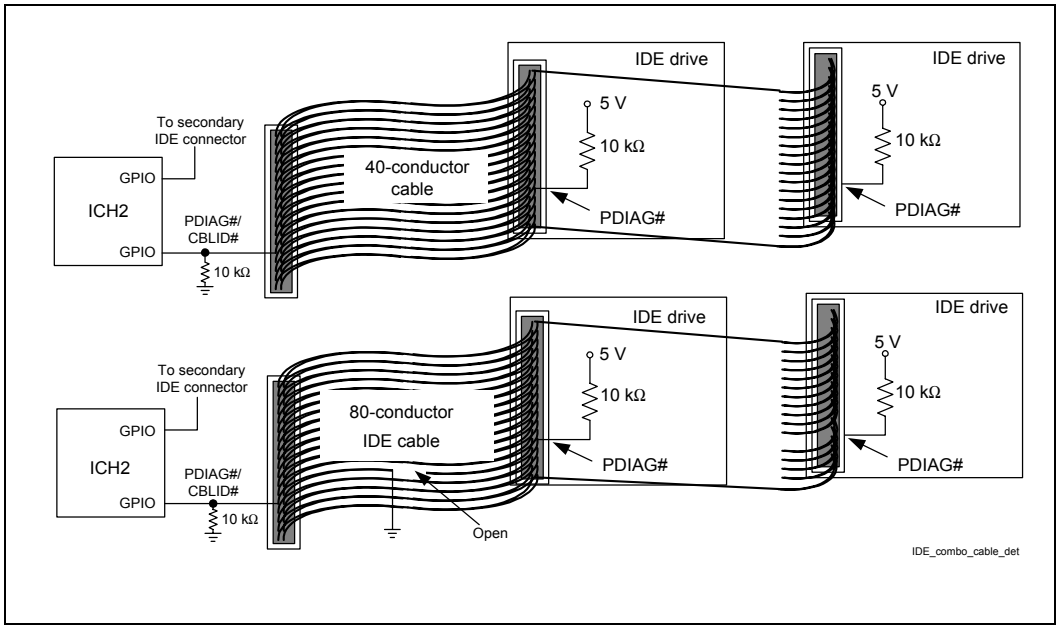
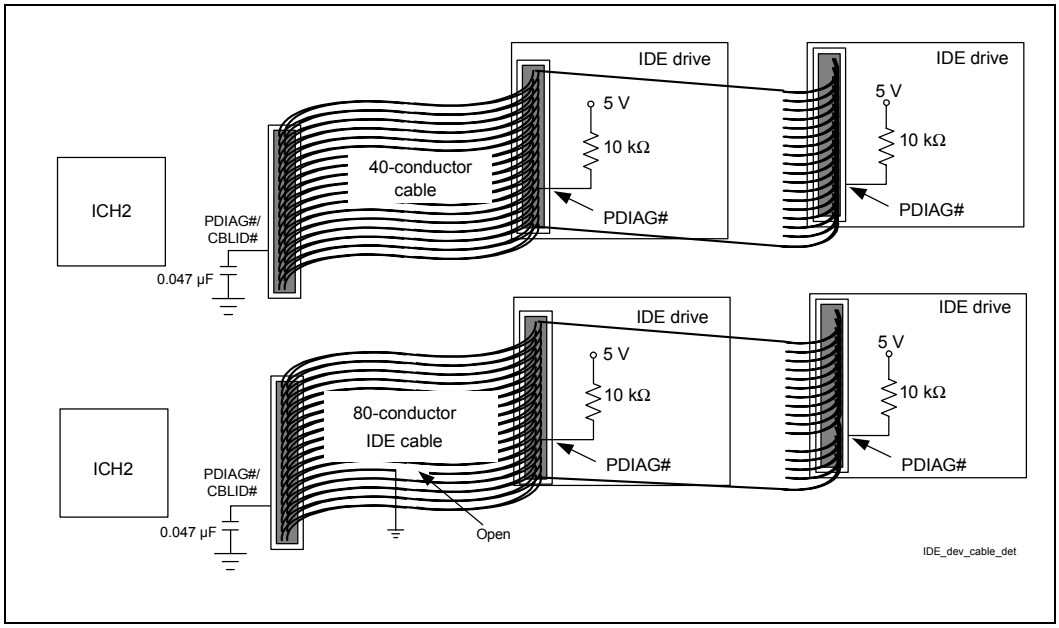


Figure 111. Device Side Only Cable Detection



13.5 LPC Checklist

Checklist Items	Recommendations
RCIN#/KBRST#	• Pull up through 8.2 kΩ resistor to VCC3_3.
LPC_PME#	• Pull up through 8.2 kΩ resistor to VCC3_3. Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH2.
J1BUTTON1, J2BUTTON2, J2BUTTON1, J2BUTTON2	• Connect through 1 kΩ series resistor / decouple through 1000 pF capacitor to GND, followed by 4.7 kΩ pull-up to VCC5 / decouple through 470 pF capacitor to GND.
JOY1X, JOY2X, JOY1Y, JOY2Y	• Connect through 1 kΩ series resistor / decouple through 22 pF capacitor to GND, followed by 4.7 kΩ pull-up to VCC5 / decouple through 470 pF capacitor to GND.
A20GATE	• Pull up through 8.2 kΩ resistor to VCC3_3.
CASEOPEN#	• Pull up through 10 MΩ resistor to VCCRTC / connect to switch to GND.
KEYLOCK#	• Pull up through 10 kΩ resistor to VCC5.
MCLK, MDAT, KCLK, KDAT	• Pull up through 4.7 kΩ resistor to VCC5_Dual.
MIDI_IN, MIDI_OUT	• Pull up through 4.7 kΩ resistor to VCC5, followed by 47 Ω series resistor / decouple through a 470 pF capacitor to GND.
RI#1, CTS#0, RXD1, RXD0, RI#0, DCD#1, DSR#1, DSR#0, DTR#1, DTR#0, DCD#0, RTS#1, RTS#0, CTS#1, TXD1, TXD0	• Decoupled using 100 pF capacitor to GND.
SERIRQ	Pull up through 8.2 kΩ resistor to VCC3_3.
LFRAME#	No required pull-up resistor
LDRQ#0	No required pull-up resistor

13.6 System Checklist

Checklist Items	Recommendations
KEYLOCK#	• Pull up through 10 kΩ resistor to VCC3_3.
PBTN_IN	• Connects to PBSwitch and PBin.
PWRLED	• Pull up through a 220 Ω resistor to VCC5.
R_IRTX	• Signal IRTX after it is pulled down through 4.7 kΩ resistor to GND and passes through 82 Ω resistor.
IRRX	• Pull up to 100 kΩ resistor to VCC3_3. • When signal is input for SI/O decouple through 470 pF capacitor to GND
IRTX	• Pull down through 4.7 kΩ to GND. • Signal passes through 82 Ω resistor. • When signal is input to SI/O decouple through 470 pF capacitor to GND
FP_PD	• Decouple through a 470 pF capacitor To GND. • Pull up 470 Ω to VCC5.
PWM1, PWM2	• Pull up through a 4.7 kΩ resistor to VCC3_3.

13.7 FWH Checklist

Checklist Items	Recommendations
No floating inputs	• Unused FGPI pins must be tied to a valid logic level.
WP#, TBL#	• Connect to ICH2.
VPP	• Pulled up to VCC3_3 and decoupled with a 0.1 µF capacitor to GND.
FGPI0, FGPI1, FGPI2, FPGI3, FPGI4, IC	• Pull down through a 8.2 kΩ resistor to GND.
INIT#	• FWH INIT# must be connected to processor INIT#.
RST#	• FWH RST# must be connected to PCIRST#.
ID[3:0]	• For a system with only one FWH device, tie ID[3:0] to ground.

NOTE: These recommendations are only valid for the Intel® firmware hub.

13.8 Clock Synthesizer Checklist

Checklist Items	Recommendations
REFCLK	• Connects to R-RefCLK, USB_CLK, SIO_CLK14, and ICHCLK14.
ICH_3V66/3V66_0, DOTCLK	• Passes through 33 Ω resistor. • When signal is input for ICH, it is pulled down through a 18 pF capacitor to GND.
DCLK/DCLK_WR	• Passes through 33 Ω resistor. • When signal is input for MCH, it is pulled down through a 22 pF capacitor to GND.
CPUHCLK/CPU_0_1	• Passes through 33 Ω resistor. • When signal is input for 370PGA, decouple through a 18 pF capacitor to GND.
R_REFCLK	• REFCLK passed through 10 kΩ resistor. • When signal is input for 370PGA, pull up through 1 kΩ resistor to VCC3_3 and pass through 10 kΩ resistor.
USB_CLK, ICH_CLK14	• REFCLK passed through 10 Ω resistor.
XTAL_IN, XTAL_OUT	• Passes through 14.318 MHz oscillator. • Pulled down through 18 pF capacitor to GND.
SEL1_PU	• Pulled up via MEMV3 circuitry through 8.2 kΩ resistor.
FREQSEL	• Connected to clock frequency selection circuitry through 10 kΩ resistor. (See CRB schematic, page 4.)
L_VCC2_5	• Connects to VDD2_5[0…1] through ferrite bead to VCC2_5.
MCHHCLK/CPU_1, ITPCLK/CPU_2, PCI_0/PCLK_OICH, PCI_1/PCLK_1, PCI_2/PCLK_2, PCI_3/PCLK_3, PCI_4/PCLK_4, PCI_5/PCLK_5, PCI_6/PCLK_6, APICCLK_CPU/APIC_0, APICCLK)ICH/APIC_1, USBCLK/USB_0, MCH_3V66/3V66_1, AGPCLK_CONN	• Passes through 33 Ω resistor.
MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7	Pass through 10 Ω resistor.
SCLK	Pass through 22 Ω resistor.
VCC3.3	Connected to VTTPWRGD gating circuit according to information in Section 4.3.1 for systems supporting the *universal PGA370* design.

13.9 System Memory Checklist

Checklist Items	Recommendations
SM_CSA#[0:3, SM_CSB#[3:0, SMAA[11:8,3:0], SM_MD[0:63], SM_CKE[0:3], S_DQM[0:7]	• Connect from MCH to DIMM0, DIMM1.
SM_MAA[7:4], SM_MAB[7:4]#	• Connect from MCH to DIMM0, DIMM1 through 10 Ω resistors.
SM_CAS#	• Connected to R_REFCLK through 10 kΩ resistor.
SM_RAS#	• Jumpered to GND through 10 kΩ resistor.
SM_WE#	• Connected to R_BSEL0# through 10 kΩ resistor.
CKE[5…0] (For 3-DIMM implementation)	• When implementing a 3-DIMM configuration, all six CKE signals on the MCH are used. (0,1 for DIMM0; 2, 3 for DIMM1; 4,5 for DIMM2)
REGE	• Connect to GND (since this Intel® 815EP chipset platform does not support registered DIMMs).
WP (Pin 81 on the DIMMS)	• Add a 4.7 kΩ pull-up resistor to 3.3 V. This recommendation write-protects the DIMMs EEPROM.
SRCOMP	• Needs a 40 Ω resistor pulled up to 3.3 V standby.

13.10 Power Delivery Checklist

Checklist Items	Recommendations
All voltage regulator components meet maximum current requirements.	• Consider all loads on a regulator, including other regulators.
All regulator components meet thermal requirements.	• Ensure the voltage regulator components and dissipate the required amount of heat.
VCC1_8 pins	• These power pins must be supplied by a 1.85 V source and be between (1.795 V to 1.905 V).
If devices are powered directly from a dual rail (i.e., not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET.	• “Dual” voltage rails may not be at the expected voltage.
Dropout voltage	• The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage.
Voltage tolerance requirements are met.	• See the individual component specifications for each voltage tolerance.

14 Third-Party Vendor Information

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the 815EP chipset platform. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

Super I/O (Vendors Contact Phone)

- SMSC — Dave Jenoff (909) 244-4937
- National Semiconductor — Robert Reneau (408) 721-2981
- ITE — Don Gardenhire (512)388-7880
- Winbond — James Chen (02) 27190505 - Taipei office

Clock Generation (Vendors Contact Phone)

- Cypress Semiconductor — John Wunner 206-821-9202 x325
- ICS — Raju Shah 408-925-9493
- IMI — Elie Ayache 408-263-6300, x235
- PERICOM — Ken Buntaran 408-435-1000

Memory Vendors

http://developer.intel.com/design/motherbd/se/se_mem.htm

Voltage Regulator Vendors (Vendors Contact Phone)

Analog Devices	Richard Carlson (408) 382-3258
On Semiconductor	Tod Shift (503) 203-7920
Semtech	Jason Bowles (408) 566-8729
Interisel	Gary Wiggins (360) 921-4421
Fairchild Semiconductor	Ron Lenk (408) 822-2546

Firmware Hub Vendors (Vendors Contact Phone)

- Silicon Storage Technology — TBD
- STMicroelectronics — TBD

GPA (a.k.a. AIMM) Card (Vendors Contact Phone)

- Kingston — JK_TSAI@kingston.com, Richard_Kanadjian@kingston.com
- Smart Modular — James.Lee@smartm.com, Arthur.SAINIO@smartm.com
- Micron Semiconductor — TBD

TMDS Transmitters

Silicon Images	John Nelson (408) 873-3111
Texas Instrument	Greg Davis [gdavis@ti.com] (214) 480-3662
Chrontel	Chi Tai Hong [cthong@chrontel.com] (408) 544-2150

TV Encoders

Chrontel	Chi Tai Hong [cthong@chrontel.com] (408)544-2150
Conexant	Eileen Carlson [eileen.carlson@conexant.com] (858) 713-3203
Focus	Bill Schillhammer [billhammer@focusinfo.com] (978) 661-0146
Philips	Marcus Rosin [marcus.rosin@philips.com]
Texas Instrument	Greg Davis[gdavis@ti.com] (214) 480-3662

Combo TMDS Transmitters/TV Encoders

Chrontel	Chi Tai Hong [cthong@chrontel.com] (408) 544-2150
Texas Instrument	Greg Davis[gdavis@ti.com] (214) 480-3662

LVDS Transmitter

National Semiconductor	387R Jason Lu [Jason.Lu@nsc.com](408) 721-7540