Intel® 815E Chipset Platform for Use with Universal Socket 370

Design Guide Update

August 2003

Notice: The Intel® 815E chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 298594-008

Contents

Revision History

Revision.	Draft/Changes	Date
-001	Initial Release	October 2001
-004	Revision Number corrected to –004 due to numbering error. Added Documentation Changes #9 - #16	January 2002
-005	Added Document Change #17, changed Section 13.3.3, 3.3V/V5REF Sequencing	March 2002
-006	Added Document Change #18-19.	April 2002
-007	Added Schematic, Layout and Routing Change #6	October 2002
-008	Deleted Documentation Change 1-17 and 19, which have been updated in the 815E DG	August 2003

Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® 815E Chipset Platform for Use with Universal Socket 370 Design Guide*, Document #298350-002, dated September 2002. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2000. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public update document when the public document is first published. This update document contains a complete list of all known information types.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 815E Chipset Platform for Use with Universal Socket 370 Design Guide, September 2002	298350-002

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 815E Chipset Platform for Use with Universal Socket 370.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc: Document change or update that will be implemented.

Shaded: This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
1	Doc	Added Support for P-MOS Kicker “ON”: SMAA[9] Is Strapped High by Internal 50 kΩ Pull-Up

NO.	Plans	SCHEMATIC, LAYOUT AND ROUTING UPDATES
1	Doc	Changed: Appendix A, Schematic Page 7 of 33, Replace PR42
2	Doc	Changed: Appendix A, Schematic Page 27 of 33, Replace R390 and R393
3	Doc	Changed: Appendix A, Schematic Page 29 of 33, Change R394 and R395 Connections
4	Doc	Changed: Appendix A, Schematic Page 26 of 33, Change VTTPWRGD Circuit
5	Doc	Changed: Appendix A, Schematic Page 7 of 33, Change SMAA[9] Circuit to Enable FSB P-MOS Kicker
6	Doc	Changed: Appendix A, Schematic Page 7 of 33, Delete SM_BS0, SM_BS1

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Added: Workaround for THERMTRIP Erratum
2	Doc	Corrected: Checklist Item Figure Number in Section 14.4.12, RTC
3	Doc	Changed: Processor Pin Names, Section 5.4
4	Doc	Changed: Processor Pin Names, Section 4.1
5	Doc	Changed: Added Information and Figure to Section 11.8.6, Power-Well Isolation Control Strap Requirements
6	Doc	Changed: Section 14.4.9, Power Management; Modified
7	Doc	Changed: Section 1.3.2.1, Intel® 82815 GMCH Features, Packaging/Power; Bullet Modified
8	Doc	Changed: Figure 100, Power Delivery Map; Replaced
9	Doc	Added Section 10.5 Power_Supply PS_ON Considerations
10	Doc	Changed Section 14.4.12, RTC, Add SUSCLK to the Checklist
11	Doc	Changed Section 14.4.15, Power, Modify Checklist Recommendations for 5V_REF_SUS
12	Doc	Changed Section 13.3.3, 3.3V/V5REF Sequencing
13	Doc	Changed Figure 86, Trace Routing, in Section 11.9.2.1, General Trace Routing Considerations

NO.	Plans	DOCUMENTATION CHANGES
14	Doc	Changed Figure 81-a, RTC Power Well Isolation Control, in Section 11.8.6, Power Well Isolation Control Strap Requirements
15	Doc	Changed Table 39, Intel® CK-815 (2-DIMM) Clocks, in Section 12.1, 2-DIMM Clocking
16	Doc	Changed Table 40, Intel® CK-815 (3-DIMM) Clocks, in Section 12.2, 3-DIMM Clocking
17	Doc	Changed Section 13.3.3, 3.3V/V5REF Sequencing
18	Doc	Changed Figure 100, Power Delivery Map, in Section 13, Power Delivery
19	Doc	Added Section 2.2, Electrostatic Discharge Platform Recommendations

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General Design Considerations

1. Added Support for P-MOS Kicker “ON”: SMAA[9] Is Strapped High by an Internal 50 kΩ Pull-Up

The PSB P-MOS Kicker circuit should be enabled (SMAA[9] is strapped high through an internal 50 kΩ pull-up resistor to enable P-MOS Kicker) on all new, future 815E Universal Socket 370 designs. Use of the P-MOS Kicker circuit improves PSB timings by improving AGTL and AGTL+ signal flight time.

Existing designs which have implemented the pull-down resistor circuit on the SMAA[9] signal as shown in the Customer Reference Board schematics and populated the resistor site to over-ride the internal pull-up resistor, may depopulate the site to enable the P-MOS Kicker circuit. This activity should be based on timing analysis of the specific platform.

P-MOS Kicker circuit “ON” is the recommended setting for 815E Universal Socket 370 designs using future 0.13 micron technology processors

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Schematic, Layout and Routing Updates

1. Changed: Appendix A, Schematic Page 7 of 33, Replace PR42

The GTLREF circuit for the GMCH does not reflect the updated recommendation in the design guide. Resistor PR42 should be replaced with a 63.4 kΩ, 1% resistor.

2. Changed: Appendix A, Schematic Page 27 of 33, Replace R390 and R393

With the change in the VRM specification for the Intel® Pentium® III processor 900 MHz, the reference schematic has been updated to meet that processor's load line requirements. Resistor R390 should be replaced with a 27.4 kΩ, 1% resistor. Resistor R393 should be replaced with a 30.1 kΩ, 1% resistor.

3. Changed: Appendix A, Schematic Page 29 of 33, Change R394 and R395 Connections

The reference schematics do not reflect the proper implementation of the BSEL signals. Resistor R394 should be connected to FMOD1 instead of FMOD0. Resistor R395 should be connected to FMOD0 instead of FMOD1.

4. Changed Appendix A, Schematic Page 26 of 33, Change VTTPWRGD Circuit

To guarantee proper operation of the comparators in the VTTPWRGD circuit, the power rail of U32 should be connected to 5-V standby instead of normal VCC5.

5. Changed Appendix A, Schematic Page 7 of 33, Change SMAA[9] Circuit to Enable FSB P-MOS Kicker

To enable the front side bus P-MOS Kicker, remove R88. The SMAA[9] signal has an internal 50 kΩ pull-up which enables the P-MOS Kicker at power-up.

6. Changed Appendix A, Schematic Page 7 of 33, Delete SM_BS0, SM_BS1

SM_BS0 and SM_BS1 are reserved pins, therefore the circuit shown on page 7 of 33 should be deleted along with the Table references to SM_BS0/SM_BS1.

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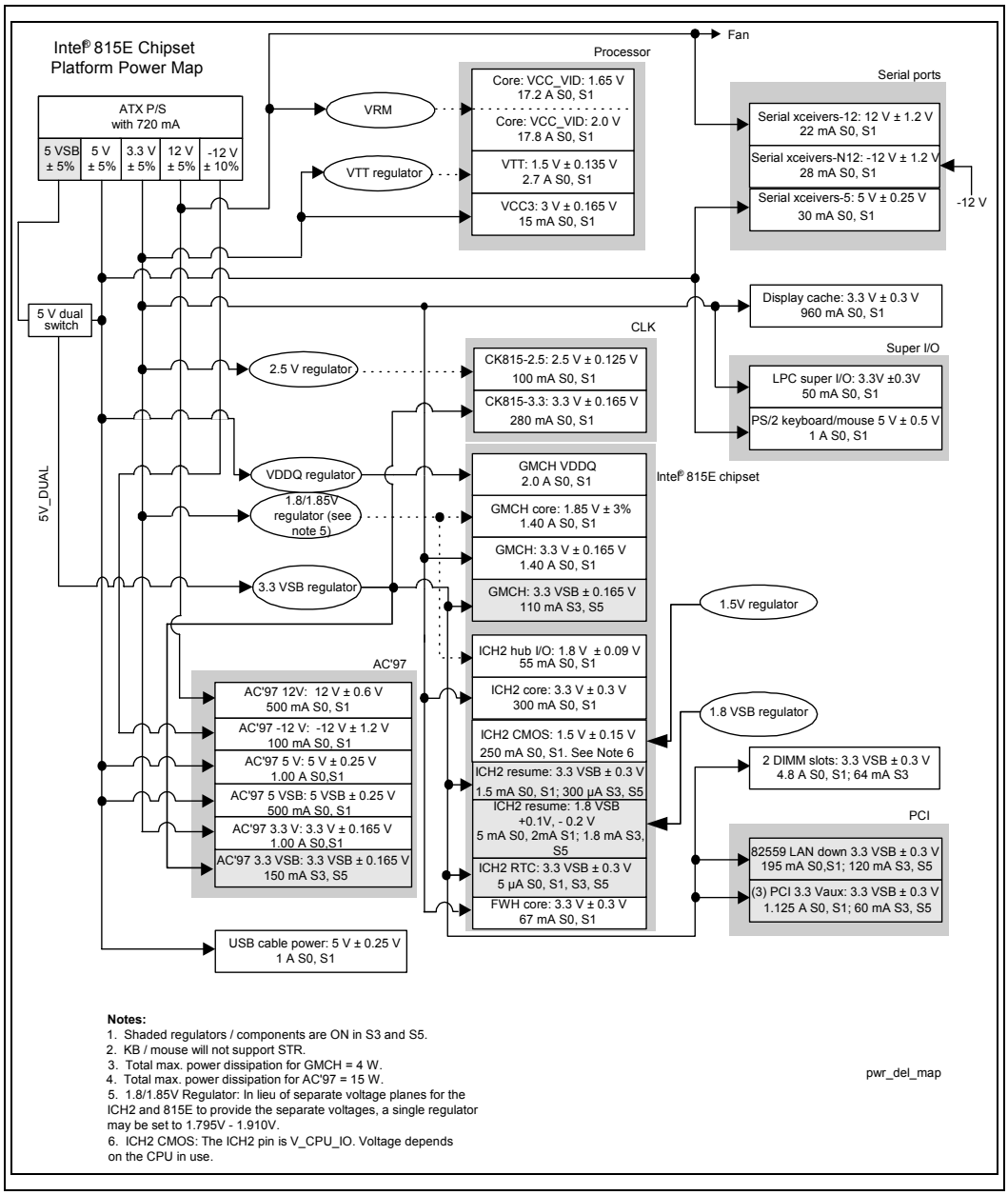
Documentation Changes

17. Changed Figure 100, *Power Delivery Map*, in Section 13, *Power Delivery*

Figure 100, *Power Delivery Map*, in Section 13, *Power Delivery*, was replaced by Document Change #8 in the public *Intel® 815E Chipset Platform Design Guide Update* 298594-005, dated March 2002. Figure 100 has two additional changes in the ICH2 section.

1. An ICH2 power plane is added to it. This added ICH2 power plane is “ICH2 CMOS”. This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.
2. An ICH2 power plane is added to it. This added ICH2 power plane is “ICH2 Resume 1.8 VSB”. This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.

Figure 100, *Power Delivery Map*, is replaced with the following:


Intel® 815E Chipset
Platform Power Map
ATX P/S
with 720 mA
5 VSB ± 5%
5 V ± 5%
3.3 V ± 5%
12 V ± 5%
-12 V ± 10%
VRM
VTT regulator
Processor
Core: VCC_VID: 1.65 V
17.2 A S0, S1
Core: VCC_VID: 2.0 V
17.8 A S0, S1
VTT: 1.5 V ± 0.135 V
2.7 A S0, S1
VCC3: 3 V ± 0.165 V
15 mA S0, S1
Fan
Serial ports
Serial xceivers-12: 12 V ± 1.2 V
22 mA S0, S1
Serial xceivers-N12: -12 V ± 1.2 V
28 mA S0, S1
Serial xceivers-5: 5 V ± 0.25 V
30 mA S0, S1
-12 V
5 V dual switch
Display cache: 3.3 V ± 0.3 V
960 mA S0, S1
CLK
2.5 V regulator
CK815-2.5: 2.5 V ± 0.125 V
100 mA S0, S1
CK815-3.3: 3.3 V ± 0.165 V
280 mA S0, S1
Super I/O
LPC super I/O: 3.3V ±0.3V
50 mA S0, S1
PS/2 keyboard/mouse 5 V ± 0.5 V
1 A S0, S1
5V_DUAL
VDDQ regulator
1.8/1.85V regulator (see note 5)
3.3 VSB regulator
GMCH VDDQ
2.0 A S0, S1
GMCH core: 1.85 V ± 3%
1.40 A S0, S1
GMCH: 3.3 V ± 0.165 V
1.40 A S0, S1
GMCH: 3.3 VSB ± 0.165 V
110 mA S3, S5
Intel® 815E chipset
1.5V regulator
ICH2 hub I/O: 1.8 V ± 0.09 V
55 mA S0, S1
ICH2 core: 3.3 V ± 0.3 V
300 mA S0, S1
1.8 VSB regulator
ICH2 CMOS: 1.5 V ± 0.15 V
250 mA S0, S1. See Note 6
ICH2 resume: 3.3 VSB ± 0.3 V
1.5 mA S0, S1; 300 µA S3, S5
ICH2 resume: 1.8 VSB
+0.1V, - 0.2 V
5 mA S0, 2mA S1; 1.8 mA S3, S5
ICH2 RTC: 3.3 VSB ± 0.3 V
5 µA S0, S1, S3, S5
FWH core: 3.3 V ± 0.3 V
67 mA S0, S1
AC'97
AC'97 12V: 12 V ± 0.6 V
500 mA S0, S1
AC'97 -12 V: -12 V ± 1.2 V
100 mA S0, S1
AC'97 5 V: 5 V ± 0.25 V
1.00 A S0,S1
AC'97 5 VSB: 5 VSB ± 0.25 V
500 mA S0, S1
AC'97 3.3 V: 3.3 V ± 0.165 V
1.00 A S0,S1
AC'97 3.3 VSB: 3.3 VSB ± 0.165 V
150 mA S3, S5
2 DIMM slots: 3.3 VSB ± 0.3 V
4.8 A S0, S1; 64 mA S3
PCI
82559 LAN down 3.3 VSB ± 0.3 V
195 mA S0,S1; 120 mA S3, S5
(3) PCI 3.3 Vaux: 3.3 VSB ± 0.3 V
1.125 A S0, S1; 60 mA S3, S5
USB cable power: 5 V ± 0.25 V
1 A S0, S1
Notes:
1. Shaded regulators / components are ON in S3 and S5.
2. KB / mouse will not support STR.
3. Total max. power dissipation for GMCH = 4 W.
4. Total max. power dissipation for AC'97 = 15 W.
5. 1.8/1.85V Regulator: In lieu of separate voltage planes for the ICH2 and 815E to provide the separate voltages, a single regulator may be set to 1.795V - 1.910V.
6. ICH2 CMOS: The ICH2 pin is V_CPU_IO. Voltage depends on the CPU in use.
pwr_del_map