Intel® 865G/865GV/865PE/865P Chipset

Platform Design Guide Update

For use with the Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and the Intel® Pentium® 4 Processor on 90 nm Process

August 2004

Notice: The Intel® 865 chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 301120-004

Contents

Revision History

Revision	Draft/Changes	Date
-001	• Initial release. • Added Documentation Change 1 and 2	February 2004
-002	Added Documentation Change 3	March 2004
-003	Added Documentation Change 4	May 2004
-004	Added Documentation Change 5 - 9	August 2004

Preface

This public Design Guide Update document is an update to the specifications and information contained in the *Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide*, Document Number 252518-004. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types.

Affected Documents

Document Title	Document Number
Intel® 865G/865GV/865PE/865P Chipset Platform Design Guide	252518-004

Related Documents

Document Title	Document Number
Intel® 82865G/82865GV Chipset: Intel® 82865G/82865GV Graphics and Memory Controller Hub (GMCH) Datasheet	252514-004
Intel® 82865P/82865PE Chipset: Intel® 82865P/82865PE Graphics and Memory Controller Hub (GMCH) Datasheet	252523-003
Intel® 82801EB I/O Controller Hub 5 (ICH5) / Intel® 82801ER I/O Controller Hub 5R (ICH5R) Datasheet	252516-001

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 865 Chipset: 82865G/82865GV/82865PE/82865P Graphics and Memory Controller Hub (GMCH).

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Consideration changes in this Design Guide Update revision.

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
		There are no Schematic, Layout, And Routing Updates changes in this Design Guide Update revision.

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Revised Checklist Item for Section 17.1.3, Processor Connector Only Items, Item VIDPWRGD
2	Doc	In Section 5.1.6.10, replace Figure 46 “Routing Illustration for BOOTSELECT”
3	Doc	Revised Section 18.1.2, Processor Connector/Intel® ICH5 Items, PWRGOOD
4	Doc	Revised Section 16.2.2, GMCH_VTT, power sequencing
5	Doc	Revise ICH5 section 16.3.5.3, 3.3V/1.5V Power Sequencing
6	Doc	Added ICH5 section 16.3.5.4, 1.5V/V_CPU_IO Power Sequencing
7	Doc	Revise ICH5 section 18.8.11, Intel® ICH5/Hub Items, add comment to HI_VSWING
8	Doc	Revise ICH5 section 11.11.5, revised Figure 135, RTCRST# External Circuit for the ICH5
9	Doc	Revise ICH5 section 11.7.1.6, Table 79: delete notation “Preliminary”

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General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

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Schematic, Layout, and Routing Updates

There are no Schematic, Layout, and Routing Updates in this design guide update revision.

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Documentation Changes

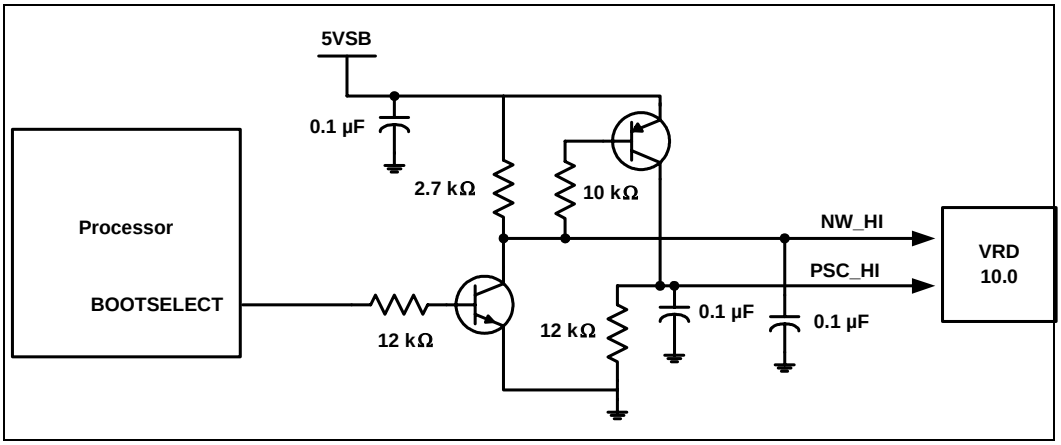
1. Revised Checklist Item for Section 17.1.3, Schematic Checklist, Processor Connector Only Items, item VIDPWRGD

Replace Section 17.1.3, Schematic Checklist, Processor Connector Only Items, item VIDPWRGD with the following:

Checklist Items	Connections/Recommendations	Reason/Impact
VIDPWRGD	Connect to power good output of the 1.2V linear supply w/ 681Ω, 1% pull-up.	

2. Replace Figure 46 "Routing Illustration for BOOTSELECT"

In Section 5.1.6.10 on page 80, replace Figure 46 "Routing Illustration for BOOTSELECT" with the following:



3. Revise Section 18.1.2, Schematic Checklist, Processor Connector/Intel® ICH5 Items, PWRGOOD

Revise Section 18.1.2, Schematic Checklist, Processor Connector/Intel® ICH5 Items, Connections/Recommendations, PWRGOOD, as follows:

Checklist Items	Connections/Recommendations
PWRGOOD	Connects to CPUPWRGD/GPO49 in ICH5. Note that a weak pullup to VCCP (V_CPU_IO) is required and that such value should not exceed ICH5s Ioh2/Iol2 specs.

4. Revise Section 16.2.2, GMCH_VTT, power sequencing

Replace the 2nd paragraph of Section 16.2.2, GMCH_VTT, with the following:

The GMCH_VTT power sequencing must meet the following two requirements:

1) GMCH_VTT must come up at the same time or after the CPU core voltage under all conditions, and 2) GMCH_VTT must come up at least 1ms before the CPU's PWRGOOD pin is asserted.

5. Revise Section 16.3.5.3, 3.3V/1.5V power sequencing

Replace Section 16.3.5.3, with the following:

16.3.5.3 3.3V/1.5V Power Sequencing

VCC1_5 should come up prior to VCC3_3 or after within 0.7V

6. Add Section 16.3.5.4, 1.5V/V_CPU_IO power sequencing

16.3.5.4 1.5V/V_CPU_IO Power Sequencing

VCC1_5 should come up prior to V_CPU_IO or after within 0.7V

7. Revise Section 18.8.11, Intel® ICH5/Hub Items

In Section 18.8.11, add the following comment to checklist item HI_VSWING:

See voltage divider recommendations in section 7.1.2

8. Revise Section 11.11.5, Figure 135, RTCRST# External Circuit for the ICH5

In Section 11.11.5, revise Figure 135 as follows:

The resistor and capacitor on RTCRST# should be changed to the following values:

R: 180k ohm to 20K ohm

C: 0.1uF to 1.0uF

9. Revise Section 11.17.1.6, Table 79, delete notation “Preliminary”

In Section 11.17.1.6, Table 79, delete the notation “Preliminary” from the table title.