Intel 100MHz Pentium(R) II processor/440GX AGPset Dual-Processor Customer Reference Schematics

Revision 1.0

**** Please note that these schematics are subject to change.**

INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: Intel 100MHz Pentium(R) II Processor/440GX AGPset Dual processor Cover Sheet		
Size: A	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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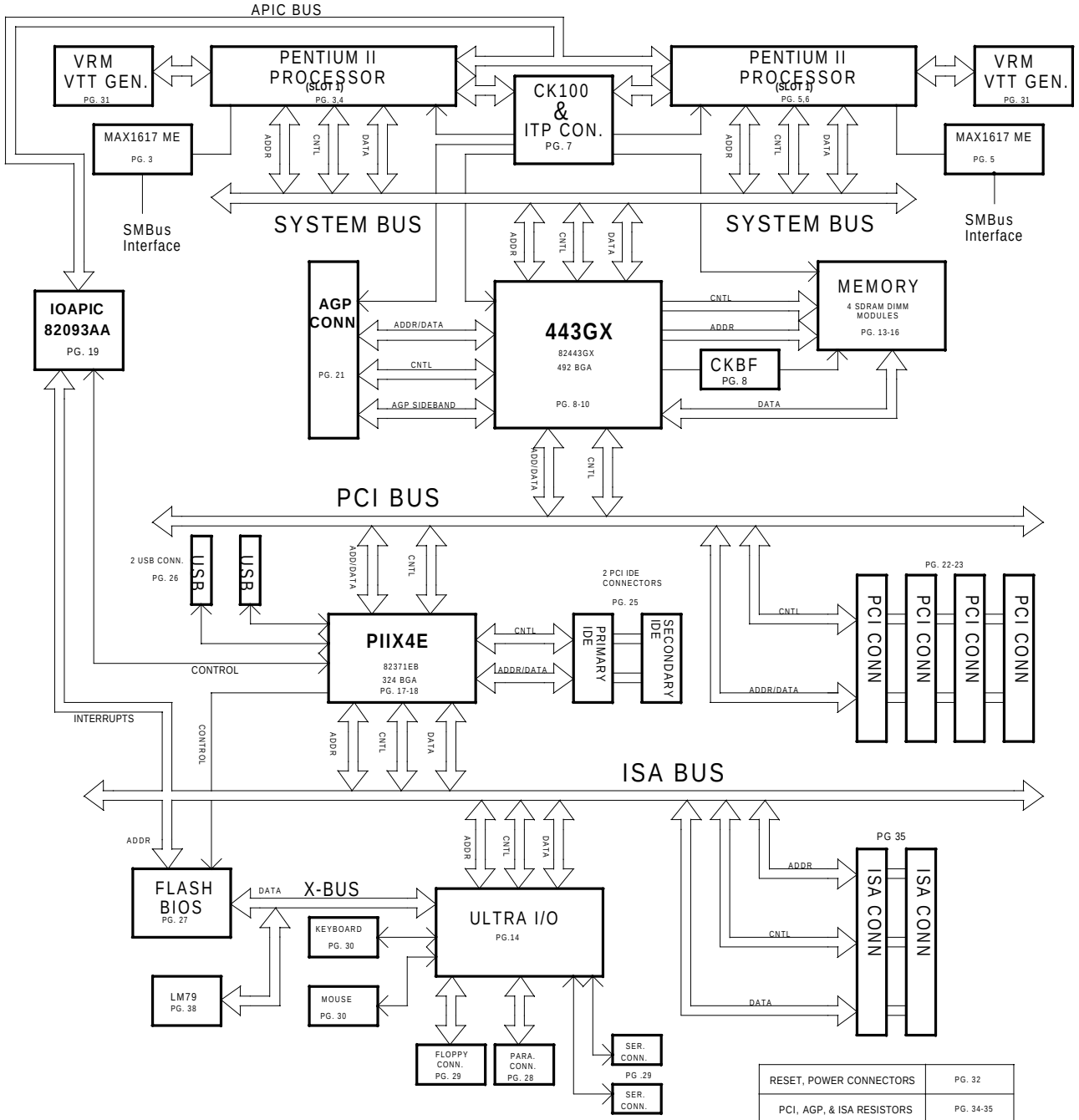

RESET, POWER CONNECTORS	PG. 32
PCI, AGP, & ISA RESISTORS	PG. 34-35
DECOUPLING CAPACITORS	PG. 36-37

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AN END USER PRODUCT. iNTEL ISNOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

DEVICE TABLE

DEVICE TYPE	REFERENCE DESIGNATOR	PAGE #
FUSES	F1,F2,F3,F4	26,30
Slot 1 Connectors	J1A,B J2A,B	3,4,5,6
ITP Connector	J3	
DIMM Sockets	J4,J5,J6,J7	13,14,15,16
AGP Connector	J8	21
PCI Connector	J9,J10,J11,J12	22,23
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IDE Connector	J15, J16	25
USB Connector	J17,J18	26
VRM8.2	J25,J26	31
BLM31A700S	L1-L13	26,30
CK100	U1	7
82443GX	U2 - 1,2,3	8,9,10
CKBF	U3	8
FET SWITCHES (74CBT16212)	U4,5,6,7,8,9	11,12
82371EB (PIIX4E)	U10A,B	17,18
74LVC14 **3VSB**	U11A,B,C,D,E,F	18, 32, 33
82093AA (IOAPIC)	U12	19
74LVC125 **3VSB**	U13A,B,C,D	19,35
FDC37C932FR (Ultra I/O)	U14	20
74AS07	U15A,B,C,D,E,F	21,35
74HCT14	U16 A,B,C,D,E,F	27,32,35
E28F002BC-T(FLASH)	U17	27
74ALS08	U20 A,B,C,D	32,35
74ALS05	U21 A,B,C,D,E,F	32,33,35
74HC10 **5VSB**	U22 A,B,C	18,32
74F07	U23A,B,C,D,E,F	32,33
74FCT3244	U24	33
LM79	U25	39
MAX 1617 ME	U28,U29	3,5
74HCT14 **5VSB**	U30	18,35
74HC112	U32	18
74F07 **5VSB**	U36A,B,C,D,E,F	18, 32, 35
LT1575	VR1	31
LT1585	VR2	31
Crystal (14.318 MHz)	Y1	7

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Title: Intel 100MHz Pentium(R) II processor/440GX AGPset Block Diagram

Size: Custom | Document Number: Intel(R) 440GX AGPset | Rev: 1.0

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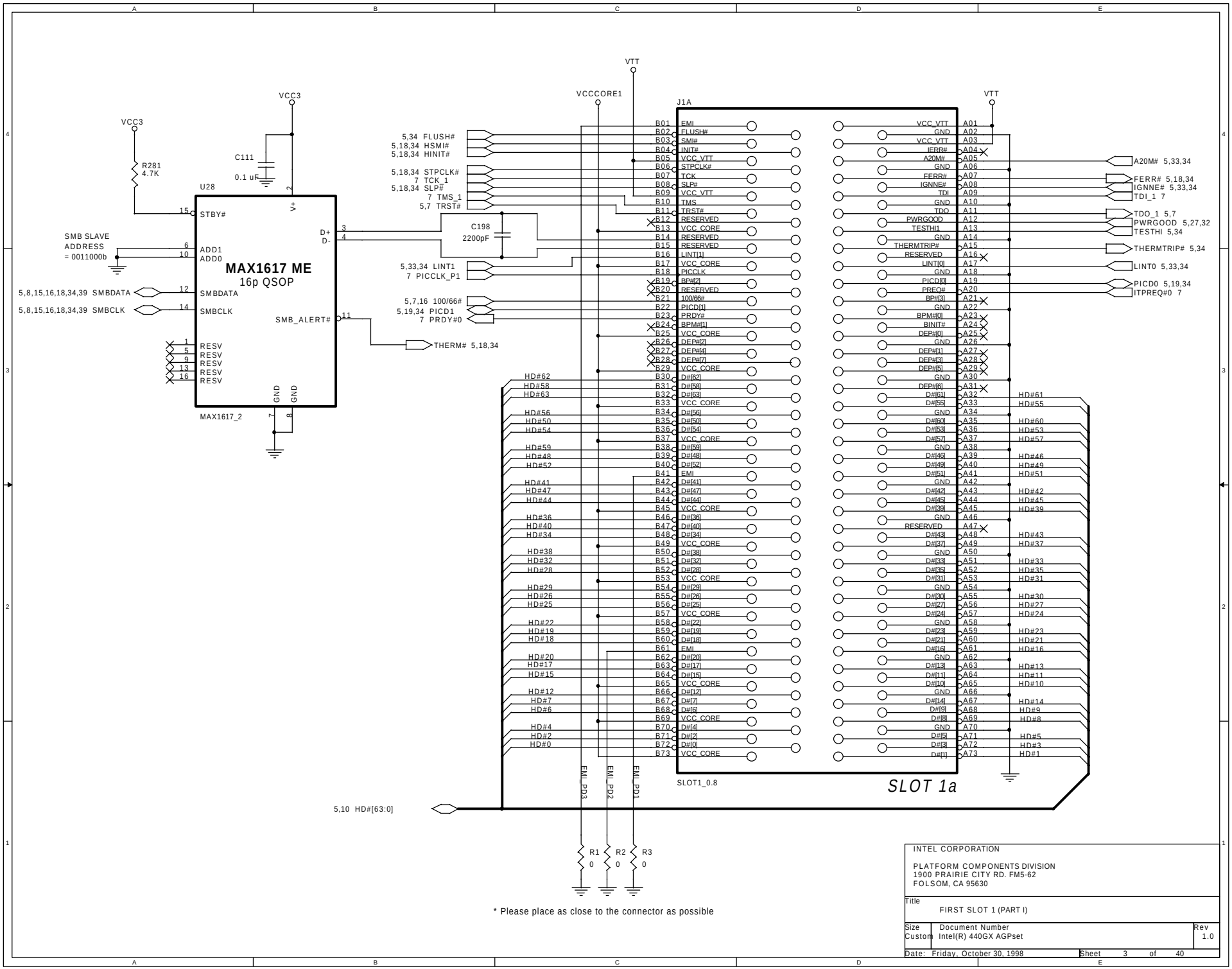

* Please place as close to the connector as possible

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Title: FIRST SLOT 1 (PART I)

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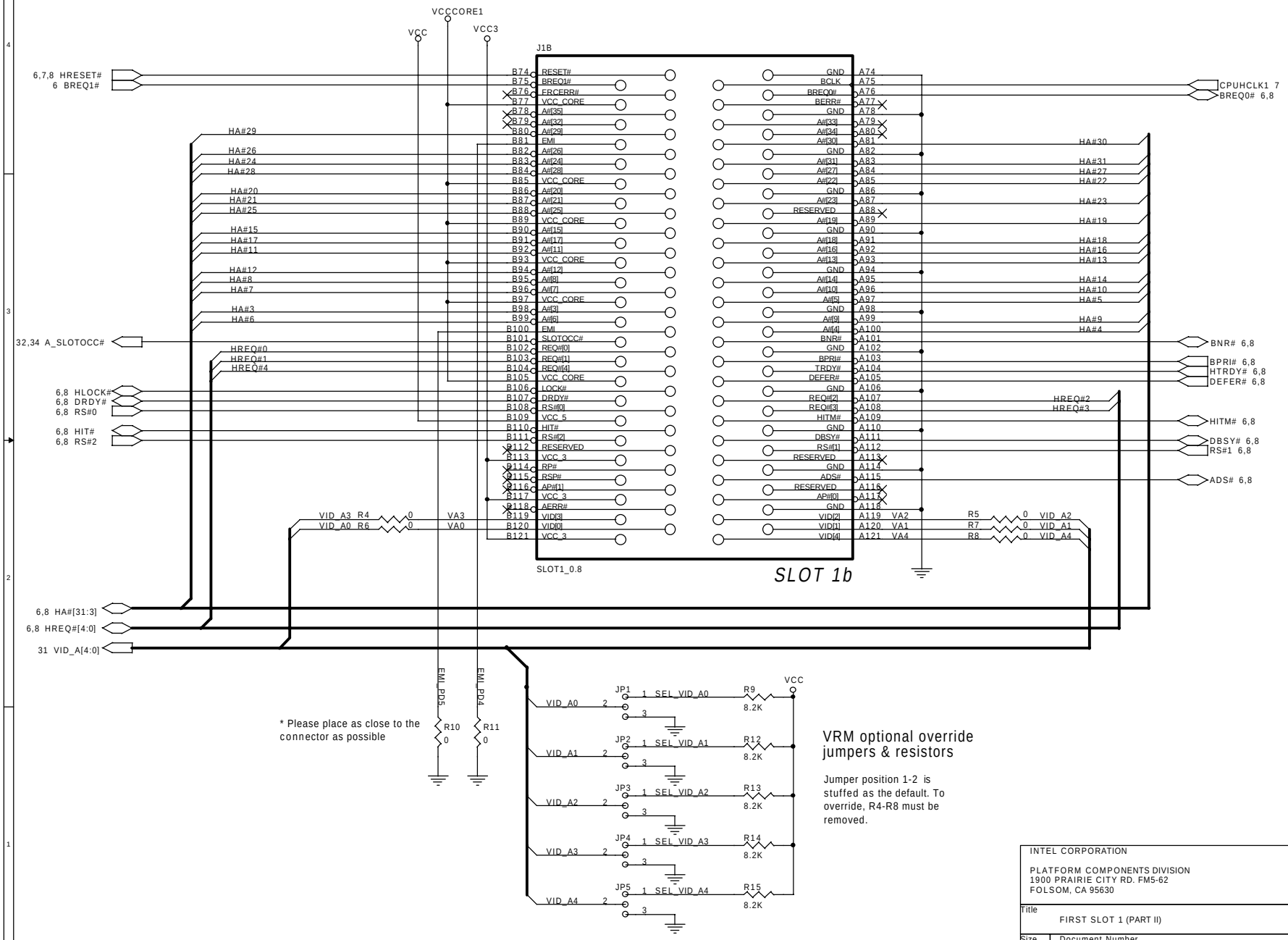
VCCCORE1
VCC
VCC3
J1B
6,7,8 HRESET#
6 BREQ1#
RESET#
BREQ1#
FRCERR#
VCC_CORE
A#[35]
A#[32]
A#[29]
EMI
A#[26]
A#[24]
A#[28]
VCC_CORE
A#[20]
A#[21]
A#[25]
VCC_CORE
A#[15]
A#[17]
A#[11]
VCC_CORE
A#[12]
A#[8]
A#[7]
VCC_CORE
A#[3]
A#[6]
EMI
SLOTOCC#
REQ#[0]
REQ#[1]
REQ#[4]
VCC_CORE
LOCK#
DRDY#
RS#[0]
VCC_5
HIT#
RS#[2]
RESERVED
VCC_3
RP#
RSP#
AP#[1]
VCC_3
AERR#
VID[3]
VID[0]
VCC_3
SLOT1_0.8
GND
BCLK
BREQ0#
BERR#
GND
A#[33]
A#[34]
A#[30]
GND
A#[31]
A#[27]
A#[22]
GND
A#[23]
RESERVED
A#[19]
GND
A#[18]
A#[16]
A#[13]
GND
A#[14]
A#[10]
A#[5]
GND
A#[9]
A#[4]
BNR#
GND
BPRI#
TRDY#
DEFER#
GND
REQ#[2]
REQ#[3]
HITM#
GND
DBSY#
RS#[1]
RESERVED
GND
ADS#
RESERVED
AP#[0]
GND
VID[2]
VID[1]
VID[4]
SLOT 1b
CPUHCLK1 7
BREQ0# 6,8
HA#30
HA#31
HA#27
HA#22
HA#23
HA#19
HA#18
HA#16
HA#13
HA#14
HA#10
HA#5
HA#9
HA#4
BNR# 6,8
BPRI# 6,8
HTRDY# 6,8
DEFER# 6,8
HREQ#2
HREQ#3
HITM# 6,8
DBSY# 6,8
RS#1 6,8
ADS# 6,8
HA#29
HA#26
HA#24
HA#28
HA#20
HA#21
HA#25
HA#15
HA#17
HA#11
HA#12
HA#8
HA#7
HA#3
HA#6
32,34 A_SLOTOCC#
HREQ#0
HREQ#1
HREQ#4
6,8 HLOCK#
6,8 DRDY#
6,8 RS#0
6,8 HIT#
6,8 RS#2
VID_A3 R4 0 VA3
VID_A0 R6 0 VA0
R5 0 VID_A2
R7 0 VID_A1
R8 0 VID_A4
6,8 HA#[31:3]
6,8 HREQ#[4:0]
31 VID_A[4:0]
EMI_PD5
EMI_PD4
R10 0
R11 0
* Please place as close to the connector as possible
VCC
JP1 1 SEL_VID_A0 R9 8.2K
VID_A0 2 3
JP2 1 SEL_VID_A1 R12 8.2K
VID_A1 2 3
JP3 1 SEL_VID_A2 R13 8.2K
VID_A2 2 3
JP4 1 SEL_VID_A3 R14 8.2K
VID_A3 2 3
JP5 1 SEL_VID_A4 R15 8.2K
VID_A4 2 3
VRM optional override jumpers & resistors
Jumper position 1-2 is stuffed as the default. To override, R4-R8 must be removed.
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FOLSOM, CA 95630
Title
FIRST SLOT 1 (PART II)
Size
Custom
Document Number
Intel(R) 440GX AGPset
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1.0
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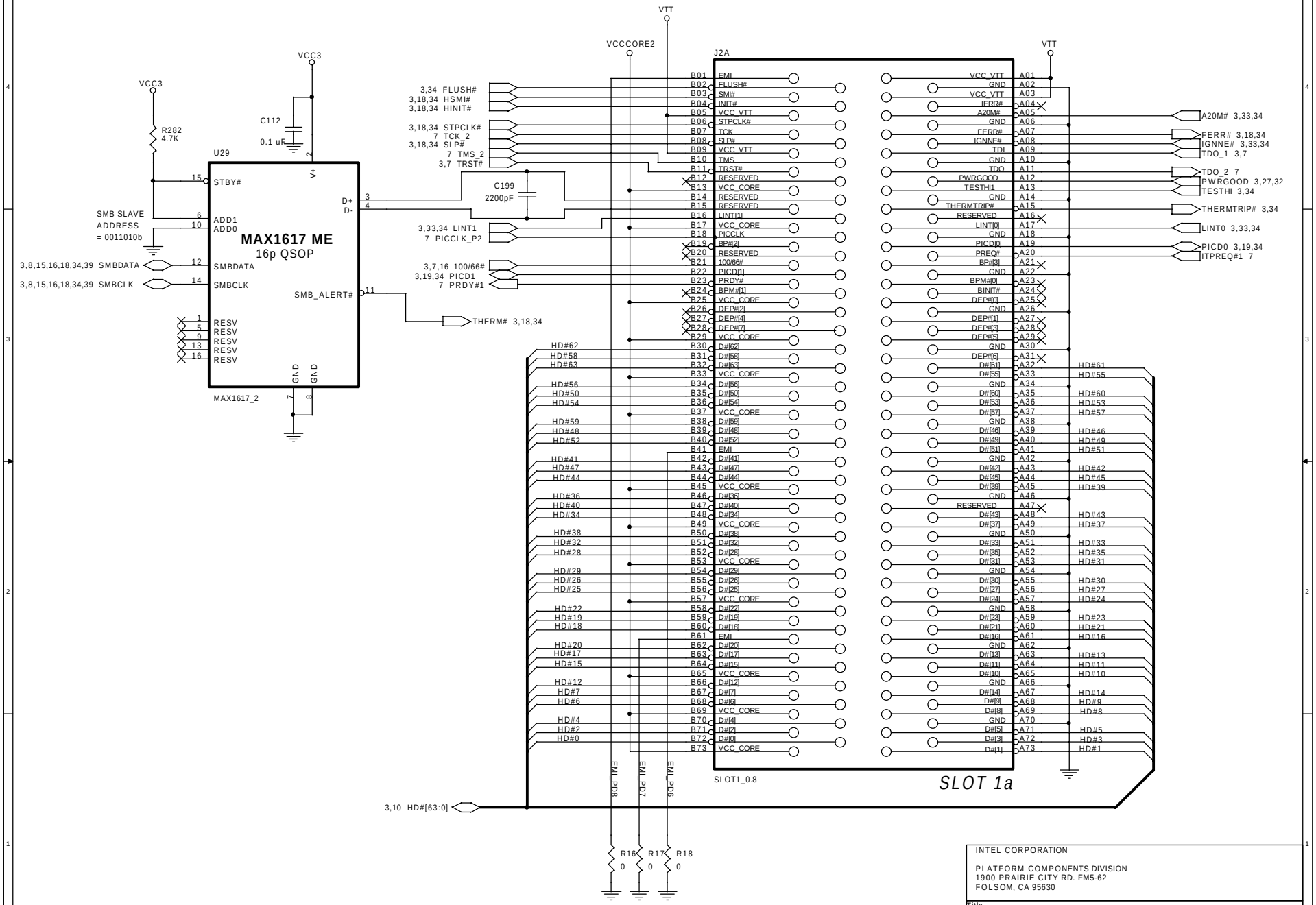

* Please place as close to the connector as possible

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Title: SECOND SLOT 1 (PART I)

Size	Document Number	Rev
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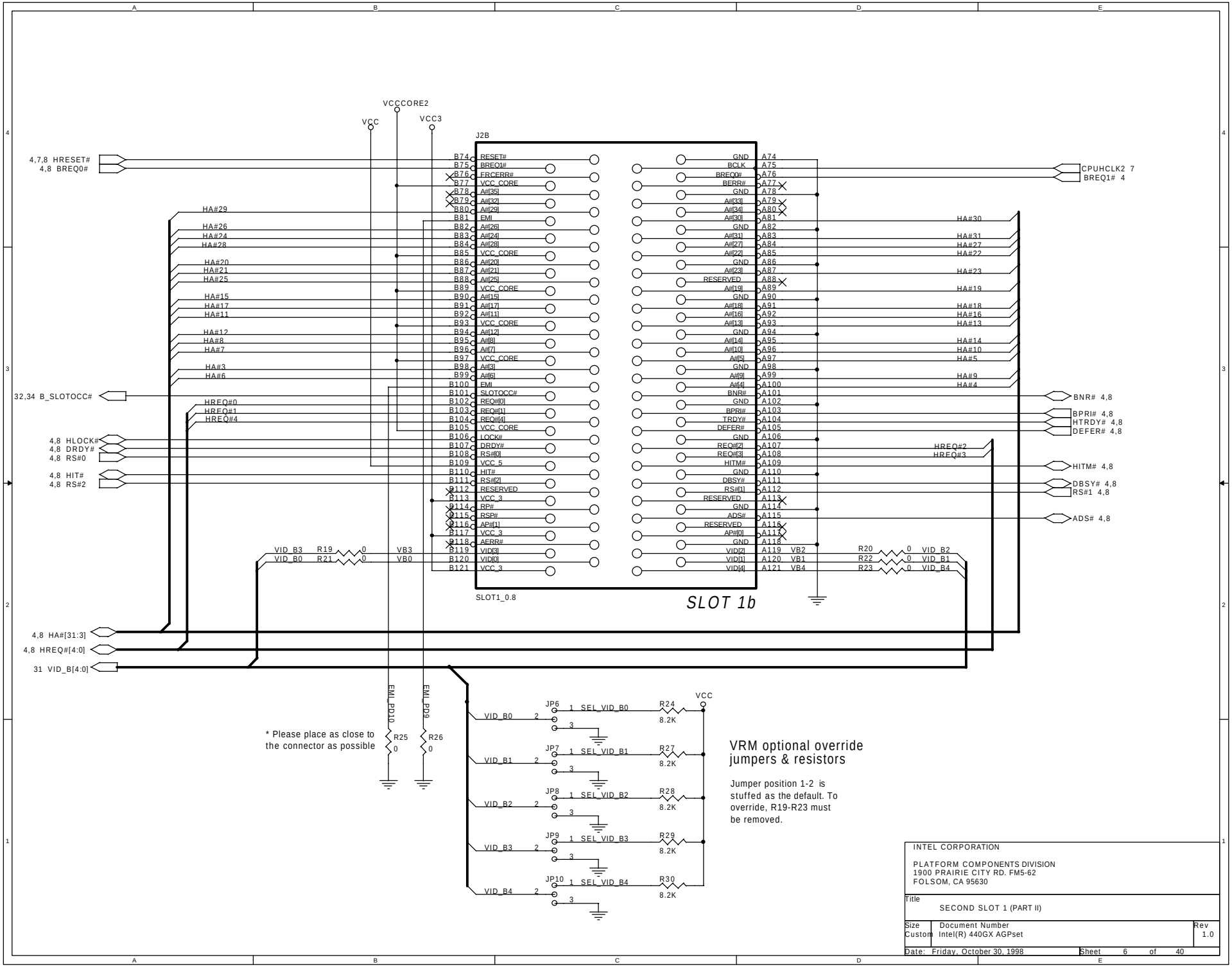
VCCCORE2
VCC
VCC3
J2B
4,7,8 HRESET#
4,8 BREQ0#
RESET#
BREQ1#
FRCERR#
VCC_CORE
A#[35]
A#[32]
A#[29]
EMI
A#[26]
A#[24]
A#[28]
VCC_CORE
A#[20]
A#[21]
A#[25]
VCC_CORE
A#[15]
A#[17]
A#[11]
VCC_CORE
A#[12]
A#[8]
A#[7]
VCC_CORE
A#[3]
A#[6]
EMI
SLOTOCC#
REQ#[0]
REQ#[1]
REQ#[4]
VCC_CORE
LOCK#
DRDY#
RS#[0]
VCC_5
HIT#
RS#[2]
RESERVED
VCC_3
RP#
RSP#
AP#[1]
VCC_3
AERR#
VID[3]
VID[0]
VCC_3
GND
BCLK
BREQ0#
BERR#
GND
A#[33]
A#[34]
A#[30]
GND
A#[31]
A#[27]
A#[22]
GND
A#[23]
RESERVED
A#[19]
GND
A#[18]
A#[16]
A#[13]
GND
A#[14]
A#[10]
A#[5]
GND
A#[9]
A#[4]
BNR#
GND
BPRI#
TRDY#
DEFER#
GND
REQ#[2]
REQ#[3]
HITM#
GND
DBSY#
RS#[1]
RESERVED
GND
ADS#
RESERVED
AP#[0]
GND
VID[2]
VID[1]
VID[4]
CPUHCLK2 7
BREQ1# 4
HA#30
HA#31
HA#27
HA#22
HA#23
HA#19
HA#18
HA#16
HA#13
HA#14
HA#10
HA#5
HA#9
HA#4
BNR# 4,8
BPRI# 4,8
HTRDY# 4,8
DEFER# 4,8
HREQ#2
HREQ#3
HITM# 4,8
DBSY# 4,8
RS#1 4,8
ADS# 4,8
VB2
VB1
VB4
SLOT1_0.8
SLOT 1b
HA#29
HA#26
HA#24
HA#28
HA#20
HA#21
HA#25
HA#15
HA#17
HA#11
HA#12
HA#8
HA#7
HA#3
HA#6
32,34 B_SLOTOCC#
HREQ#0
HREQ#1
HREQ#4
4,8 HLOCK#
4,8 DRDY#
4,8 RS#0
4,8 HIT#
4,8 RS#2
VID_B3 R19 0 VB3
VID_B0 R21 0 VB0
R20 0 VID_B2
R22 0 VID_B1
R23 0 VID_B4
4,8 HA#[31:3]
4,8 HREQ#[4:0]
31 VID_B[4:0]
EMI_PD10
EMI_PD9
R25 0
R26 0
* Please place as close to the connector as possible
VCC
JP6 1 SEL_VID_B0 R24 8.2K
JP7 1 SEL_VID_B1 R27 8.2K
JP8 1 SEL_VID_B2 R28 8.2K
JP9 1 SEL_VID_B3 R29 8.2K
JP10 1 SEL_VID_B4 R30 8.2K
VID_B0
VID_B1
VID_B2
VID_B3
VID_B4
VRM optional override jumpers & resistors
Jumper position 1-2 is stuffed as the default. To override, R19-R23 must be removed.
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Title
SECOND SLOT 1 (PART II)
Size
Custom
Document Number
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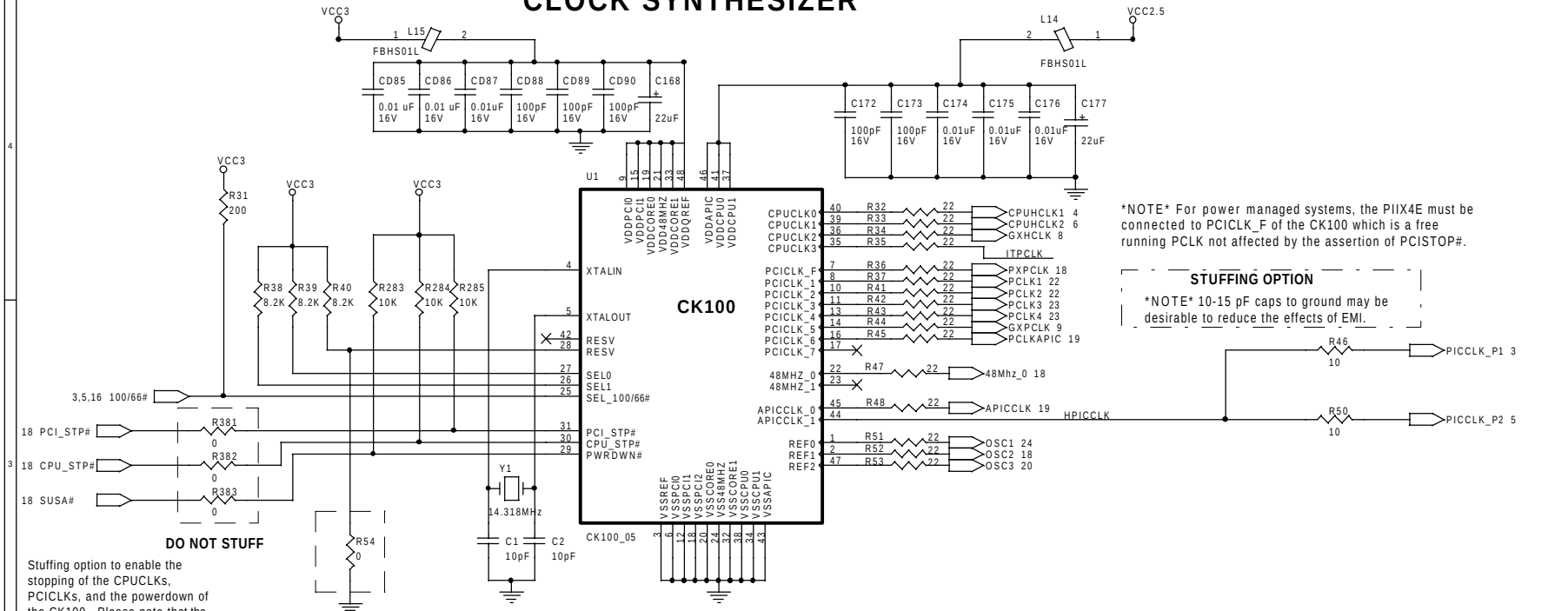
CLOCK SYNTHESIZER



NOTE For power managed systems, the PIIX4E must be connected to PCICLK_F of the CK100 which is a free running PCLK not affected by the assertion of PCISTOP#.

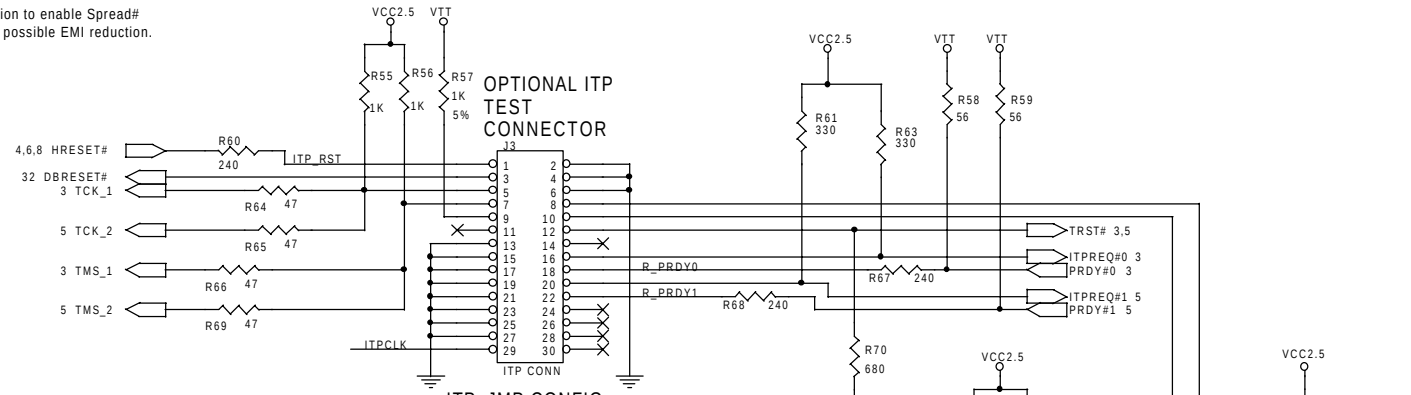
STUFFING OPTION

NOTE 10-15 pF caps to ground may be desirable to reduce the effects of EMI.

DO NOT STUFF

Stuffing option to enable the stopping of the CPUCLKs, PCICLKs, and the powerdown of the CK100. Please note that the resistors are not stuffed.

Stuffing option to enable Spread# function for possible EMI reduction.



ITP_JMP CONFIG

TDO_JMP JP12	TDI_JMP JP13	CPU CONFIG
1 - 2	1 - 2	SINGLE CPU1
2 - 3	1 - 2	DUAL CPU
2 - 3	2 - 3	SINGLE CPU2

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Title: CLOCK SYNTHESIZER

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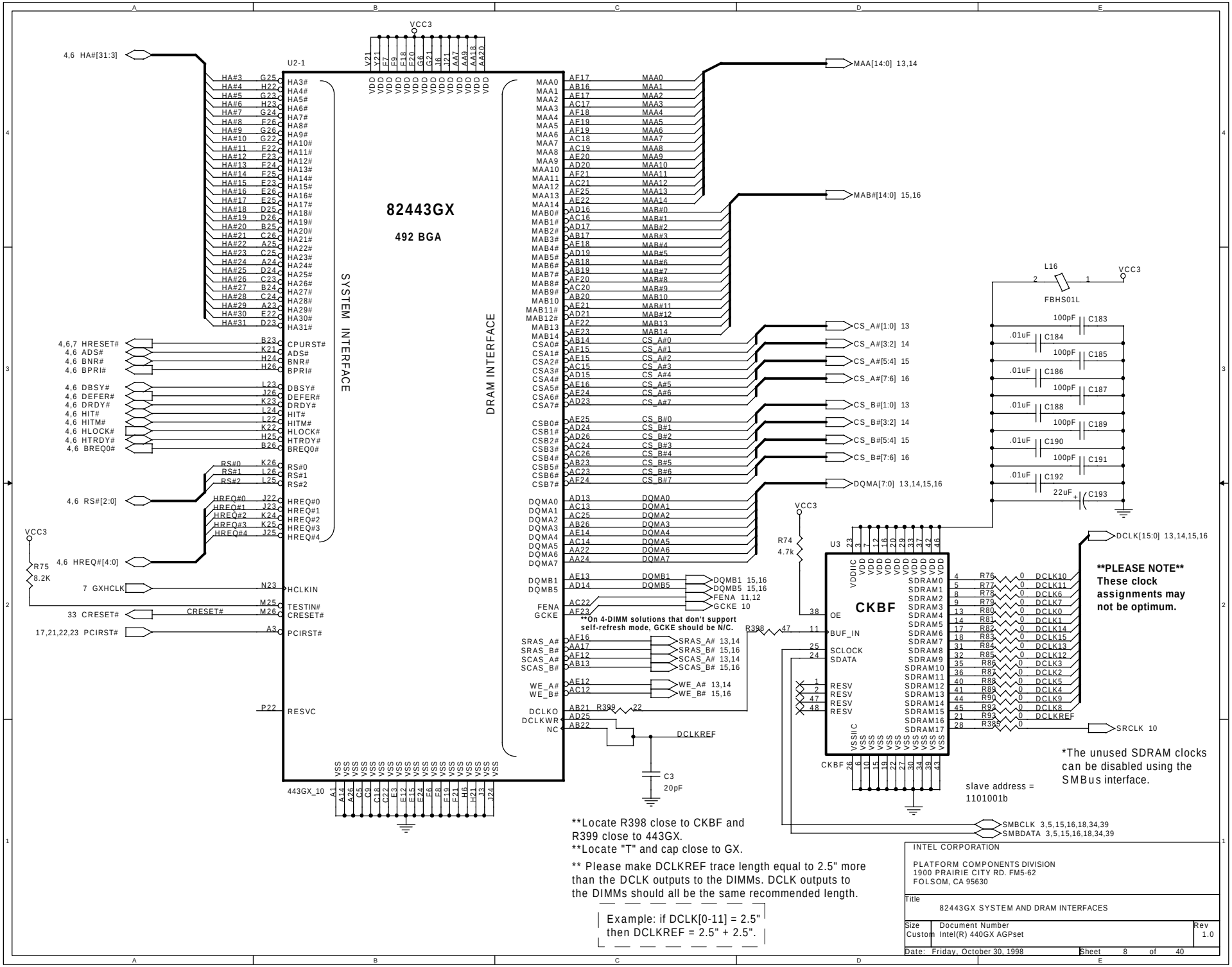

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Title: 82443GX SYSTEM AND DRAM INTERFACES		
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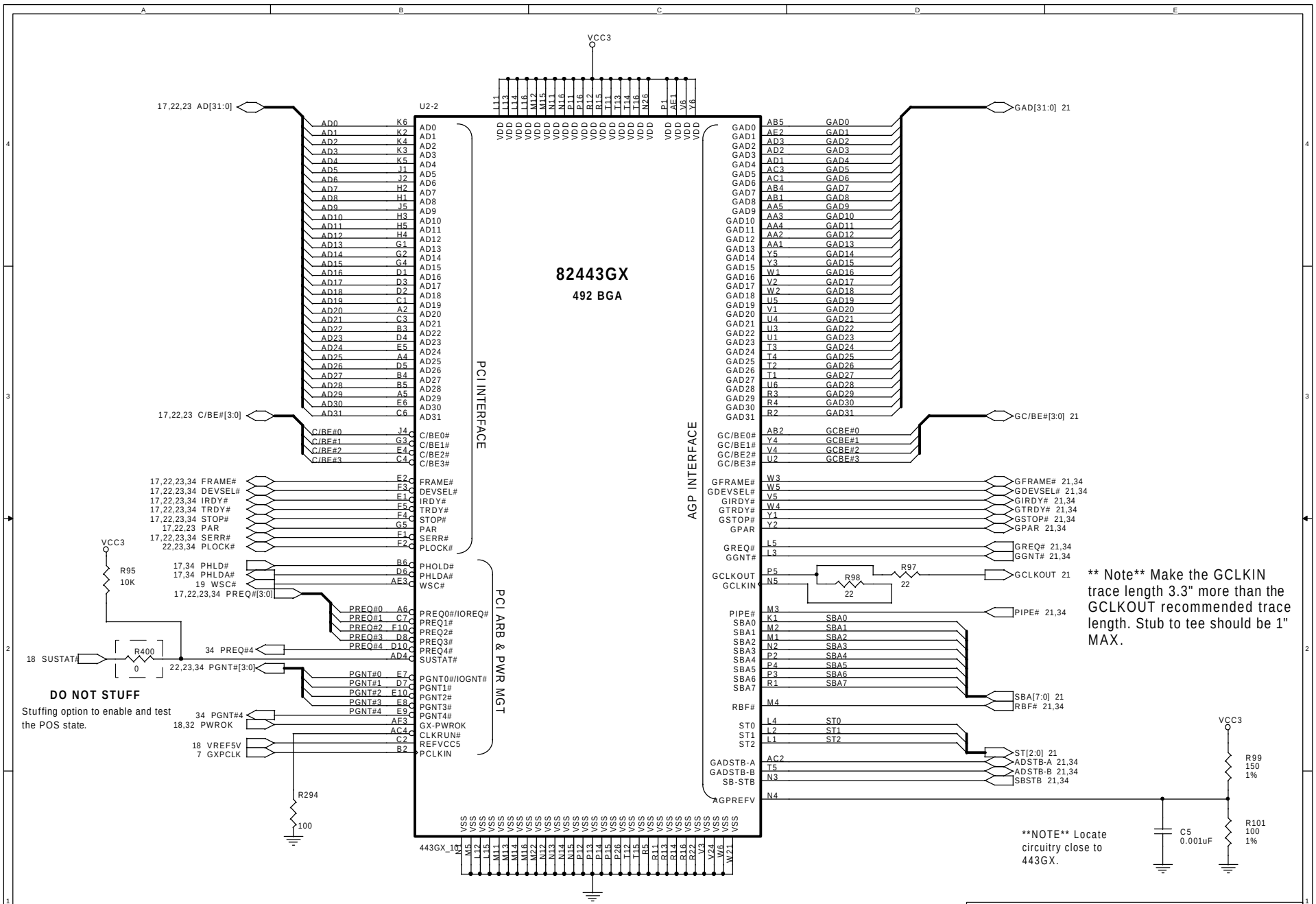

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Title: 82443GX PCI AND AGP INTERFACES		
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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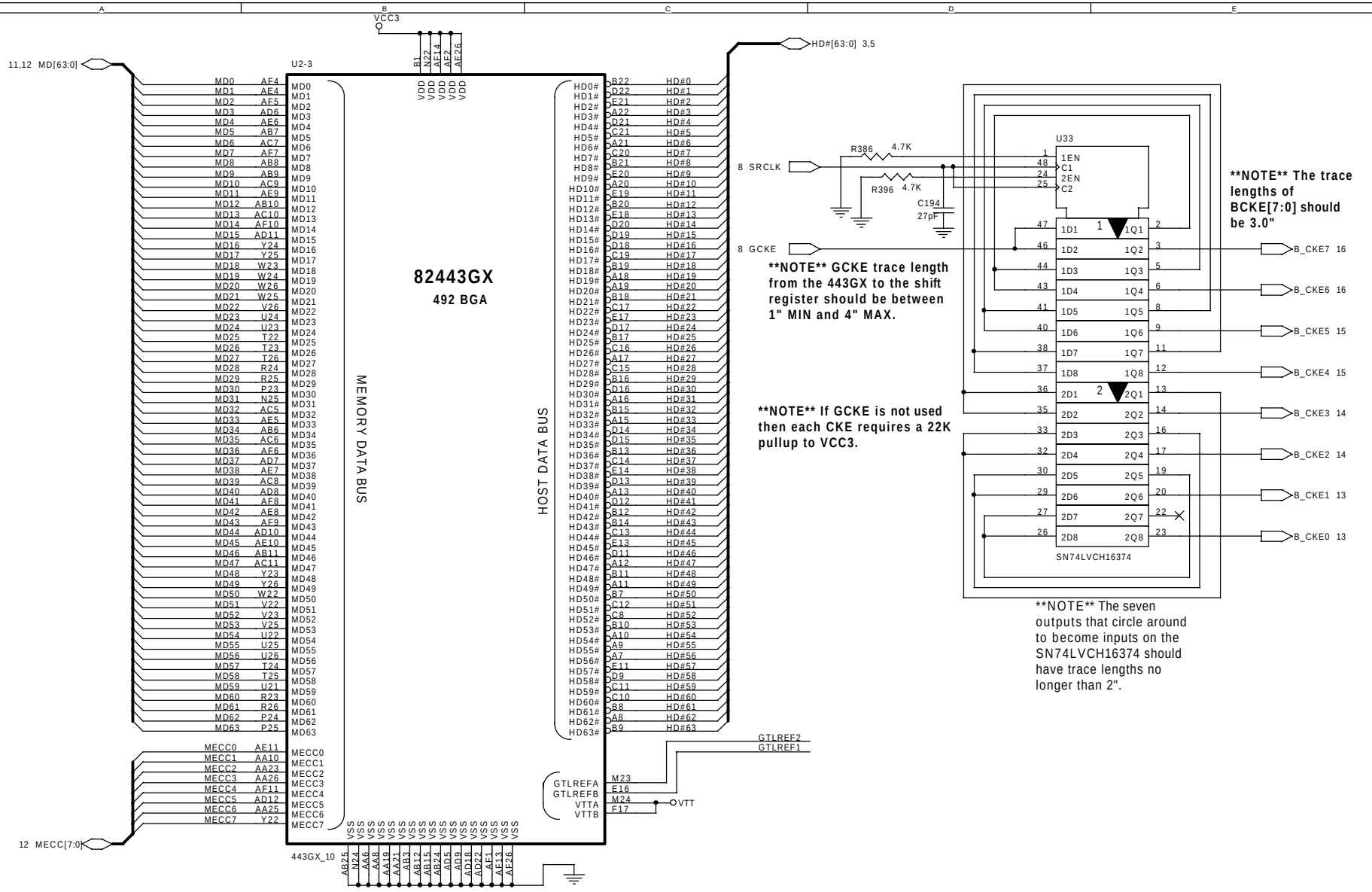

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Title: 82443GX MD/HD BUS	
Size: Custom	Document Number: Intel(R) 440GX AGPset
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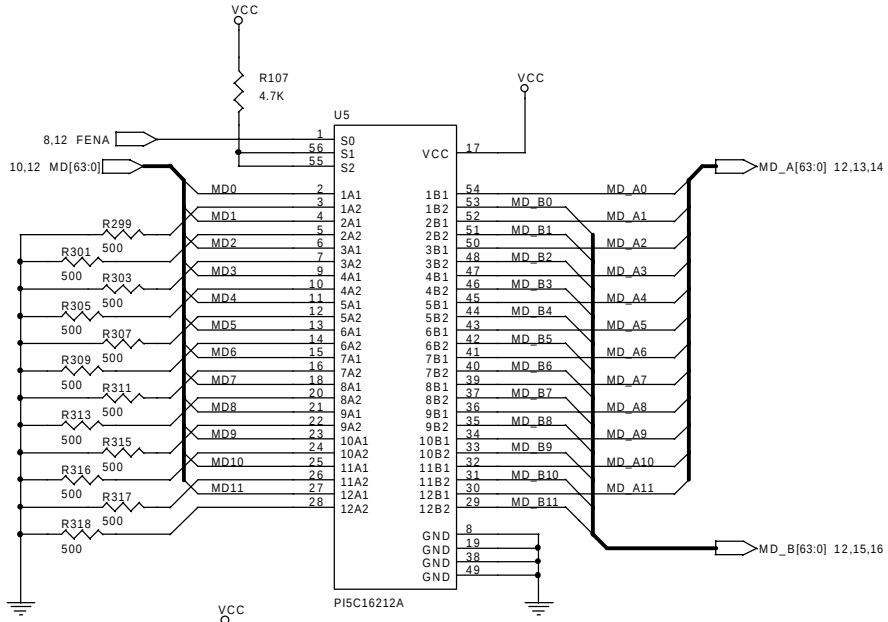
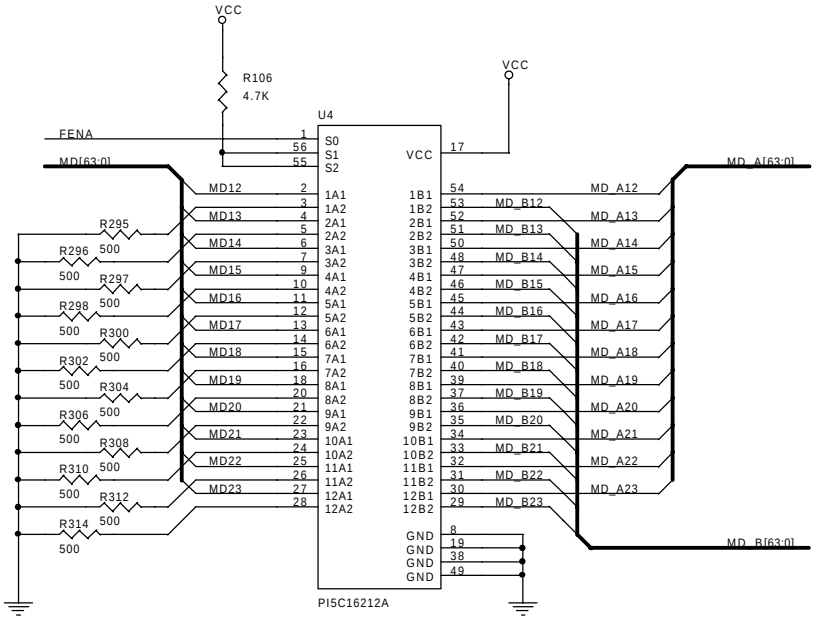
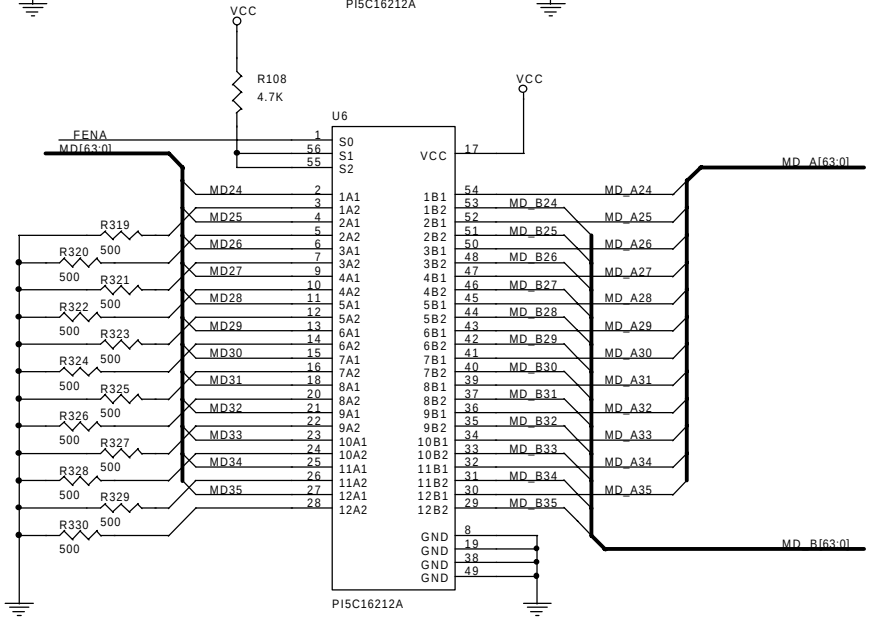
FET-SWITCHES (MEMORY DATA LINES & ECC)







FET ENABLE TRUTH TABLE

FUNCTION	S2	S1	S0 [FENA]	A1	A2
A1 TO B1, A2 TO B2	H	H	L	B1	B2
A1 TO B1, A2 TO B2	H	H	H	B2	B1

A1 = DRAM DATA LINES
A2 = GND

B1 = DIMM 0,1 DATA LINES
B2 = DIMM 2,3 DATA LINES

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Title: FET SWITCHES (DP/4 DIMM Design)

Size: Custom | Document Number: Intel(R) 440GX AGPset | Rev: 1.0

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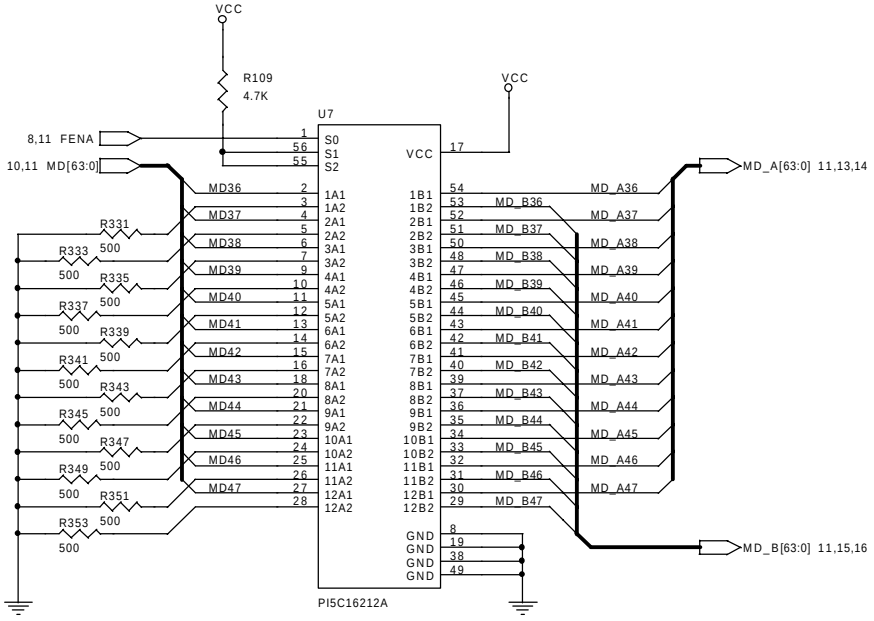
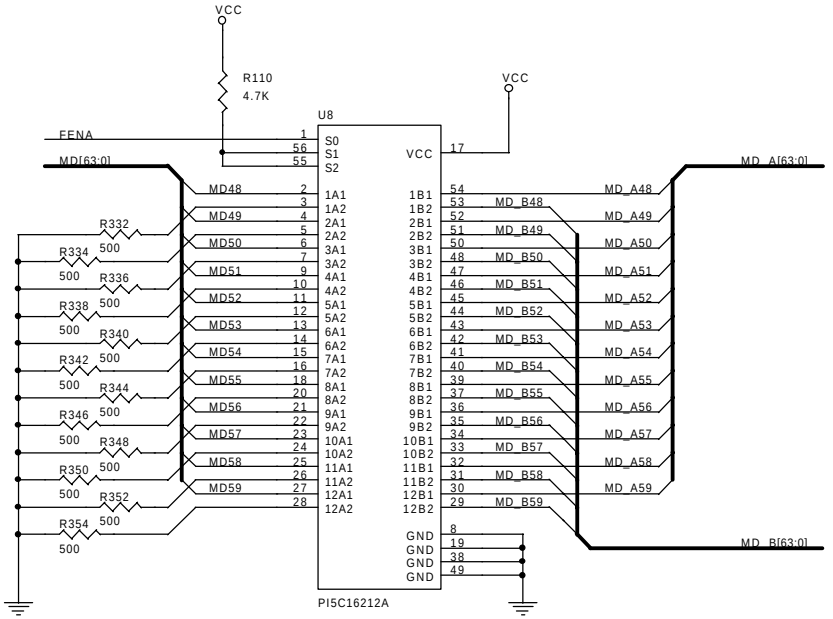
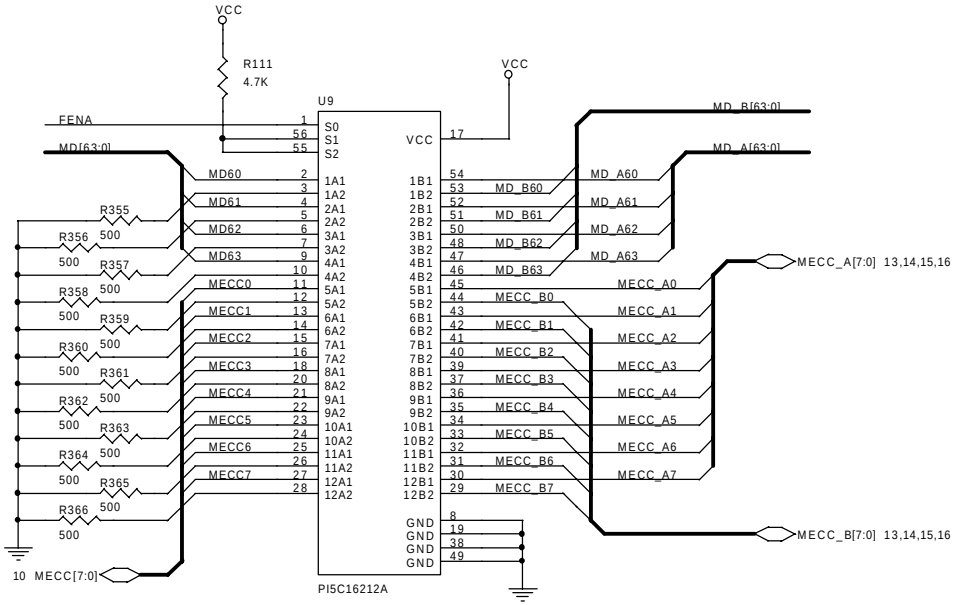
FET-SWITCHES (DRAM DATA LINES & ECC)







FET ENABLE TRUTH TABLE

FUNCTION	S2	S1	S0 [FENA]	A1	A2
A1 TO B1, A2 TO B2	H	H	L	B1	B2
A1 TO B1, A2 TO B2	H	H	H	B2	B1

A1 = DRAM DATA LINES
A2 = GND

B1 = DIMM 0,1 DATA LINES
B2 = DIMM 2,3 DATA LINES

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Title: FET SWITCHES (DP/4 DIMM Design)

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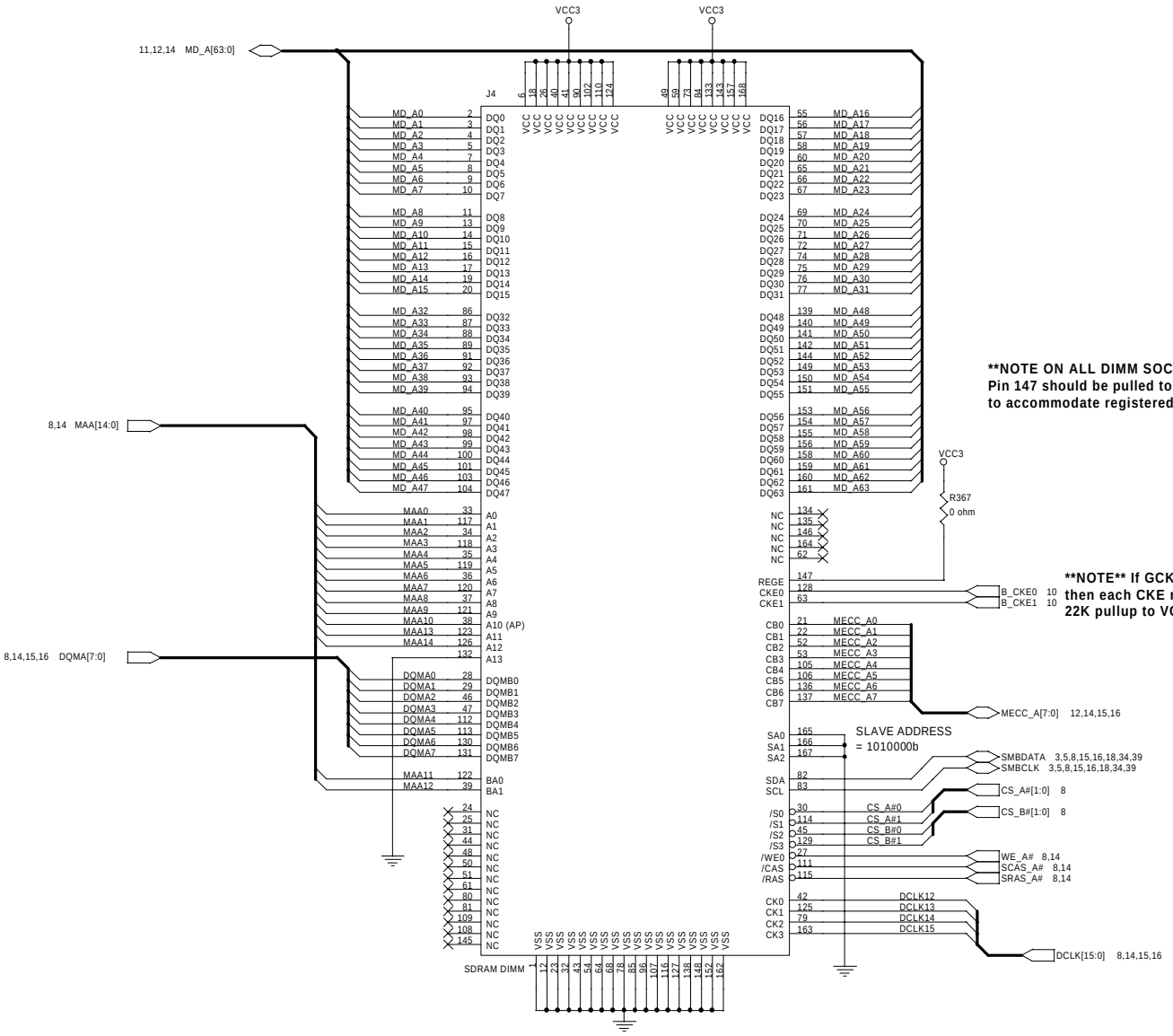
DIMM SOCKET 0



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Title	DIMM SOCKET 0
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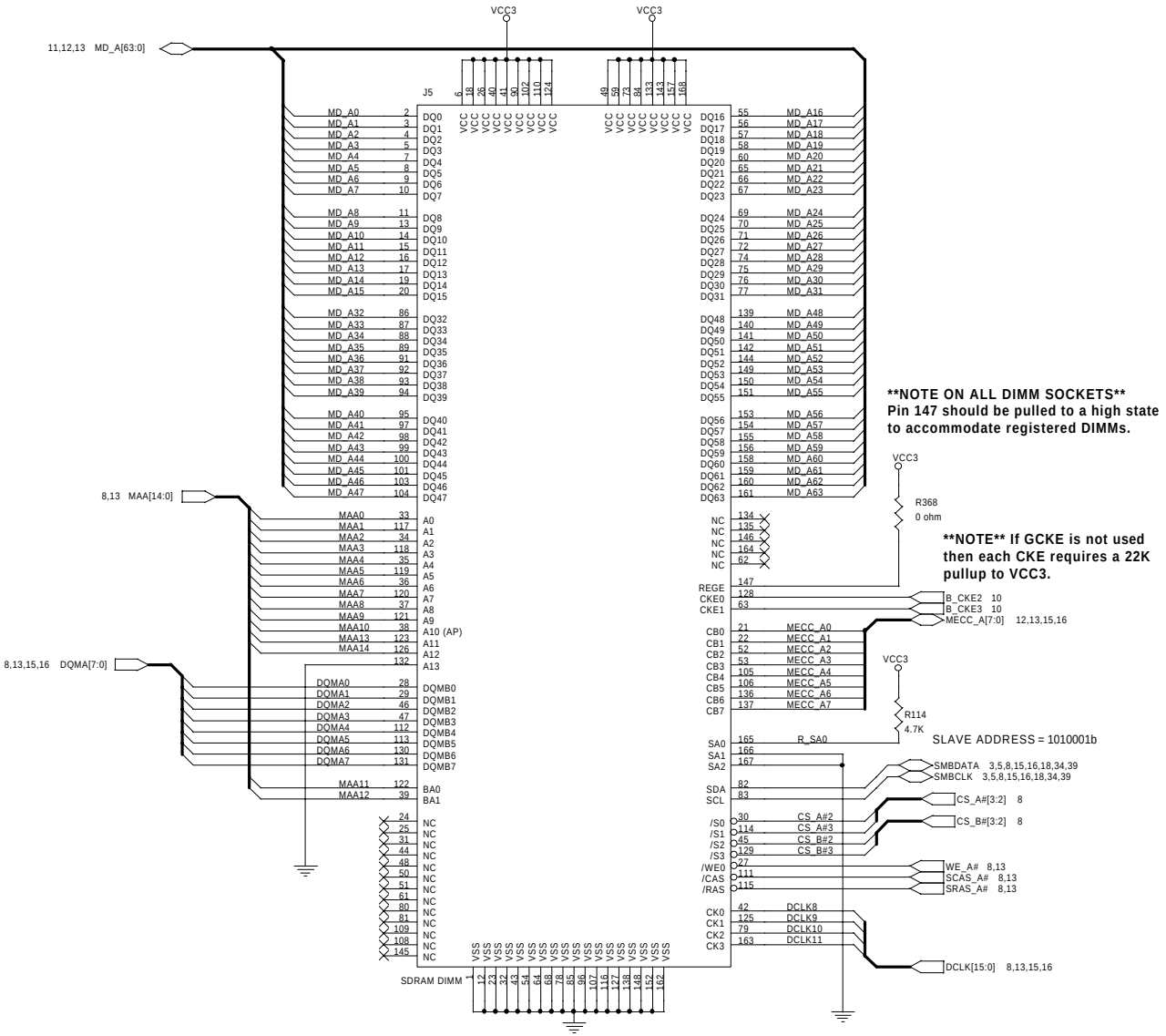
DIMM SOCKET 1



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Title: DIMM SOCKET 1

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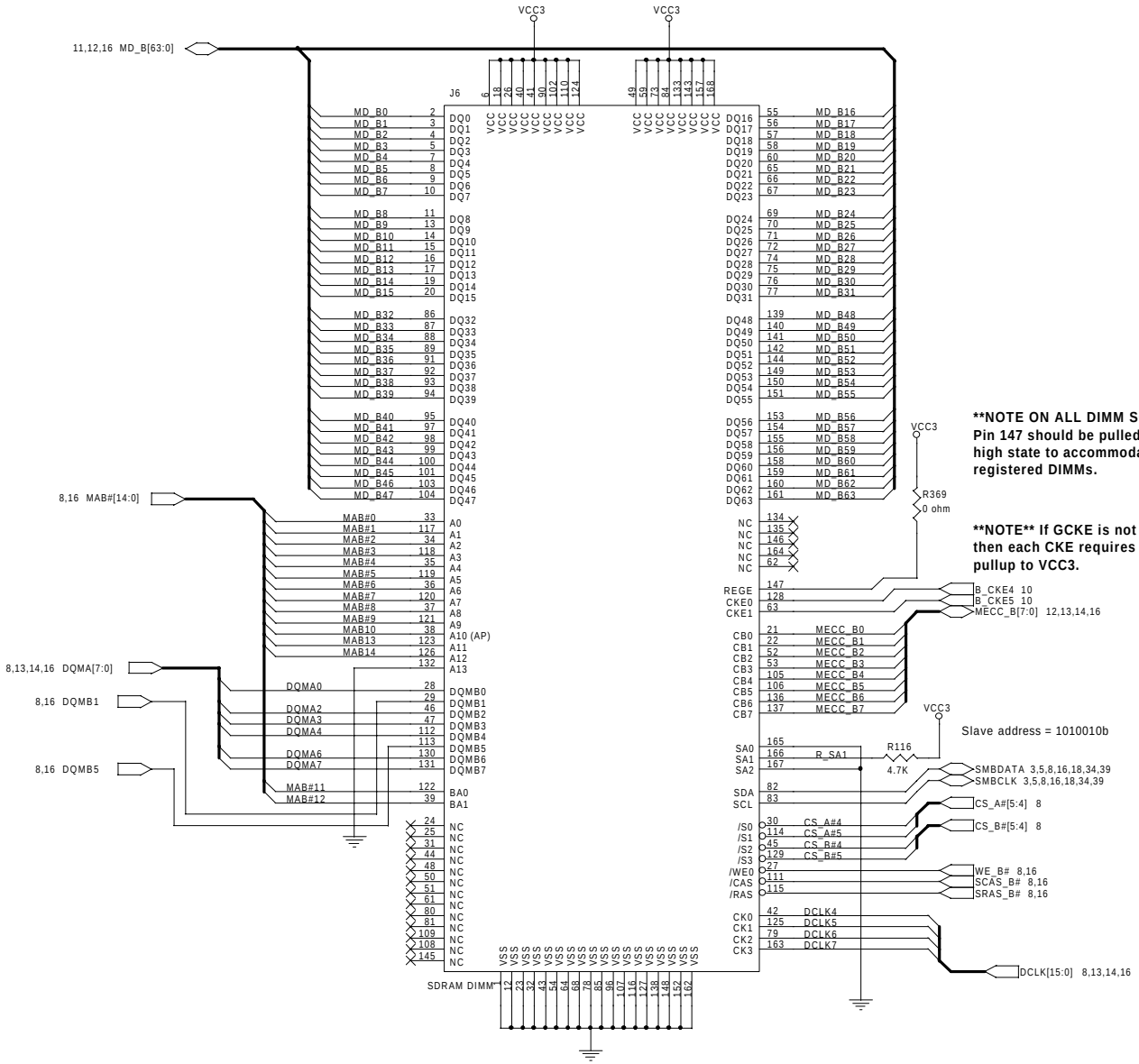
DIMM SOCKET 2



****NOTE ON ALL DIMM SOCKETS****
Pin 147 should be pulled to a high state to accommodate registered DIMMs.

****NOTE** If GCKE is not used then each CKE requires a 22K pullup to VCC3.**

Slave address = 1010010b

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Title: DIMM SOCKET 2		
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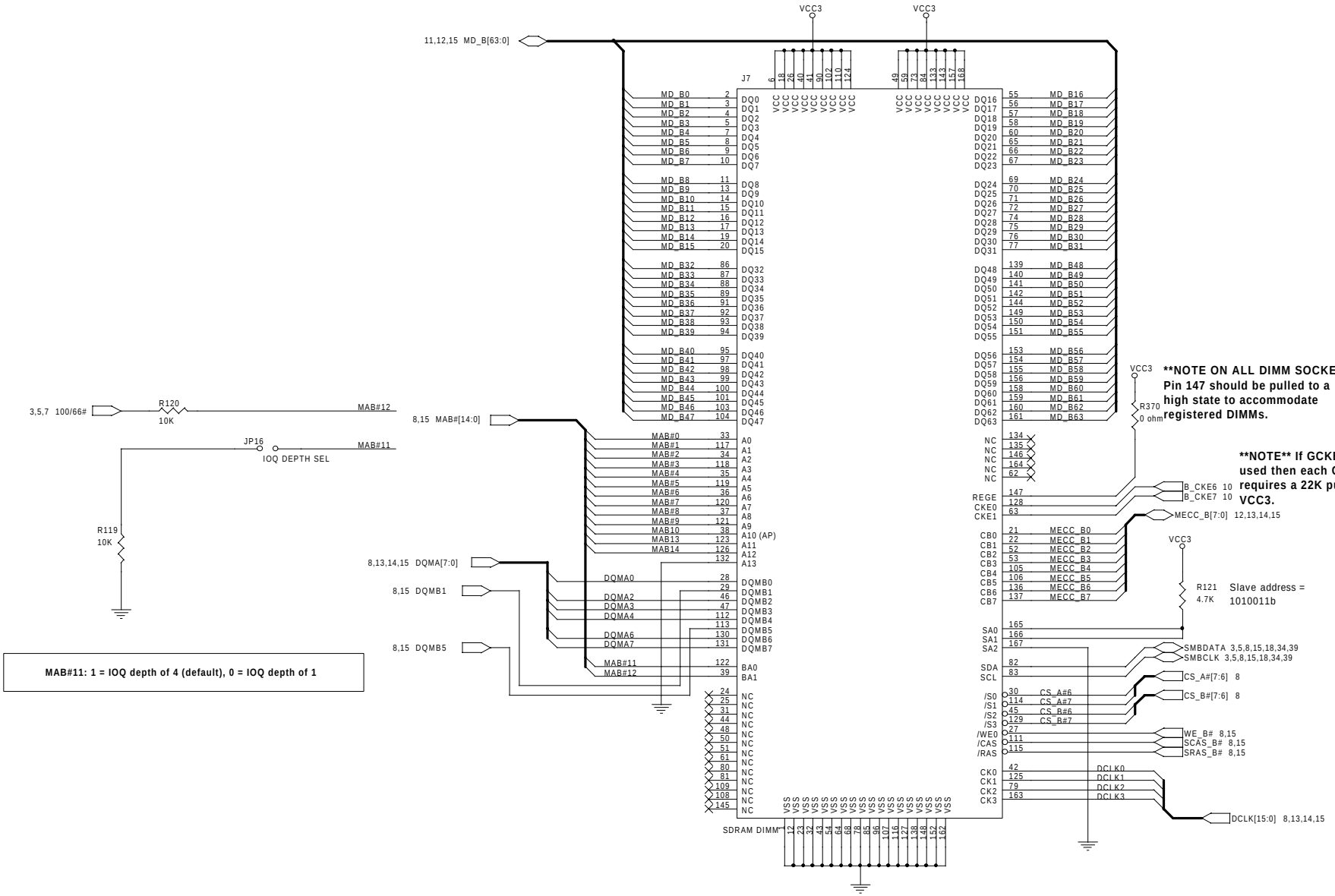
DIMM SOCKET 3



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Title	DIMM SOCKET 3	
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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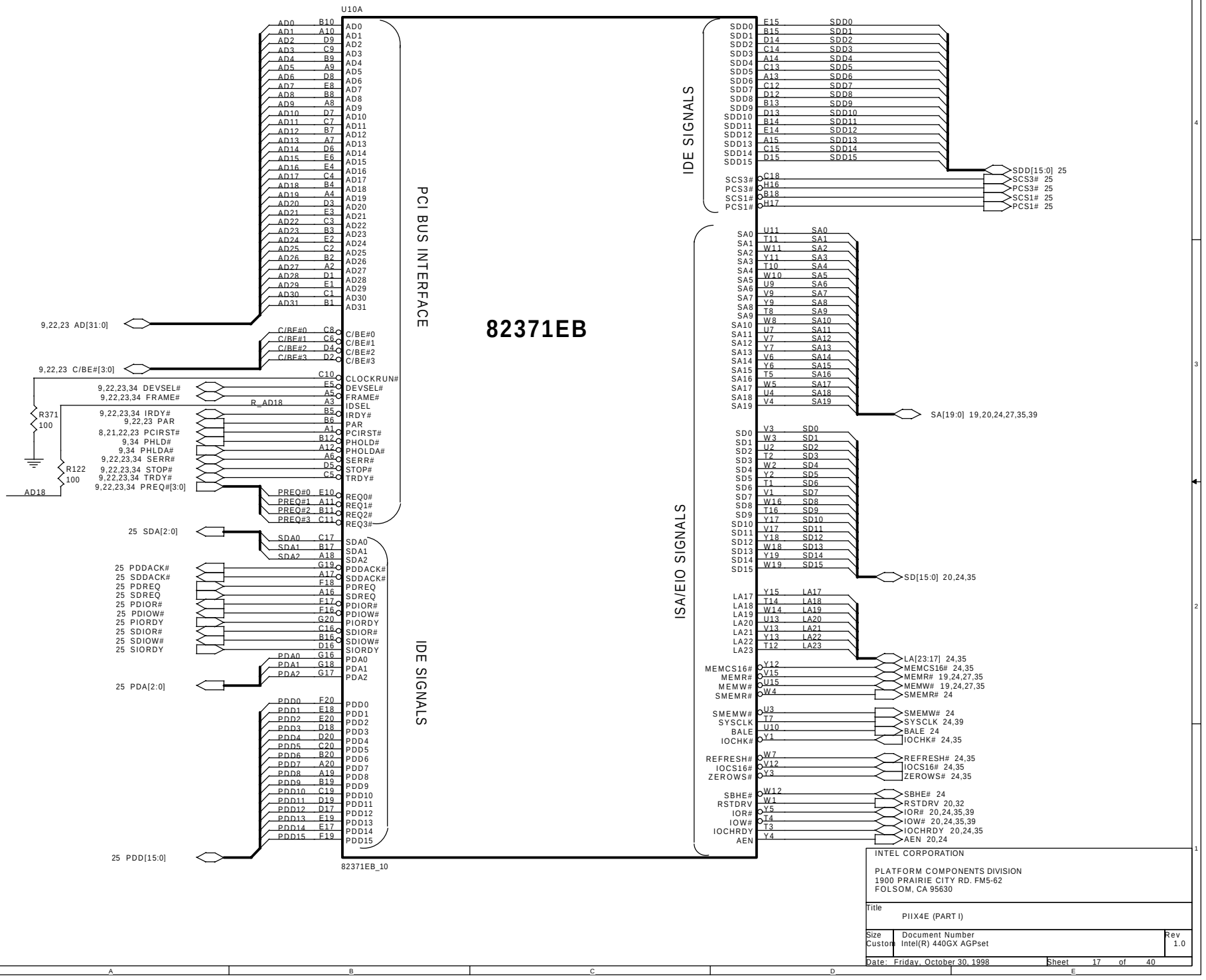

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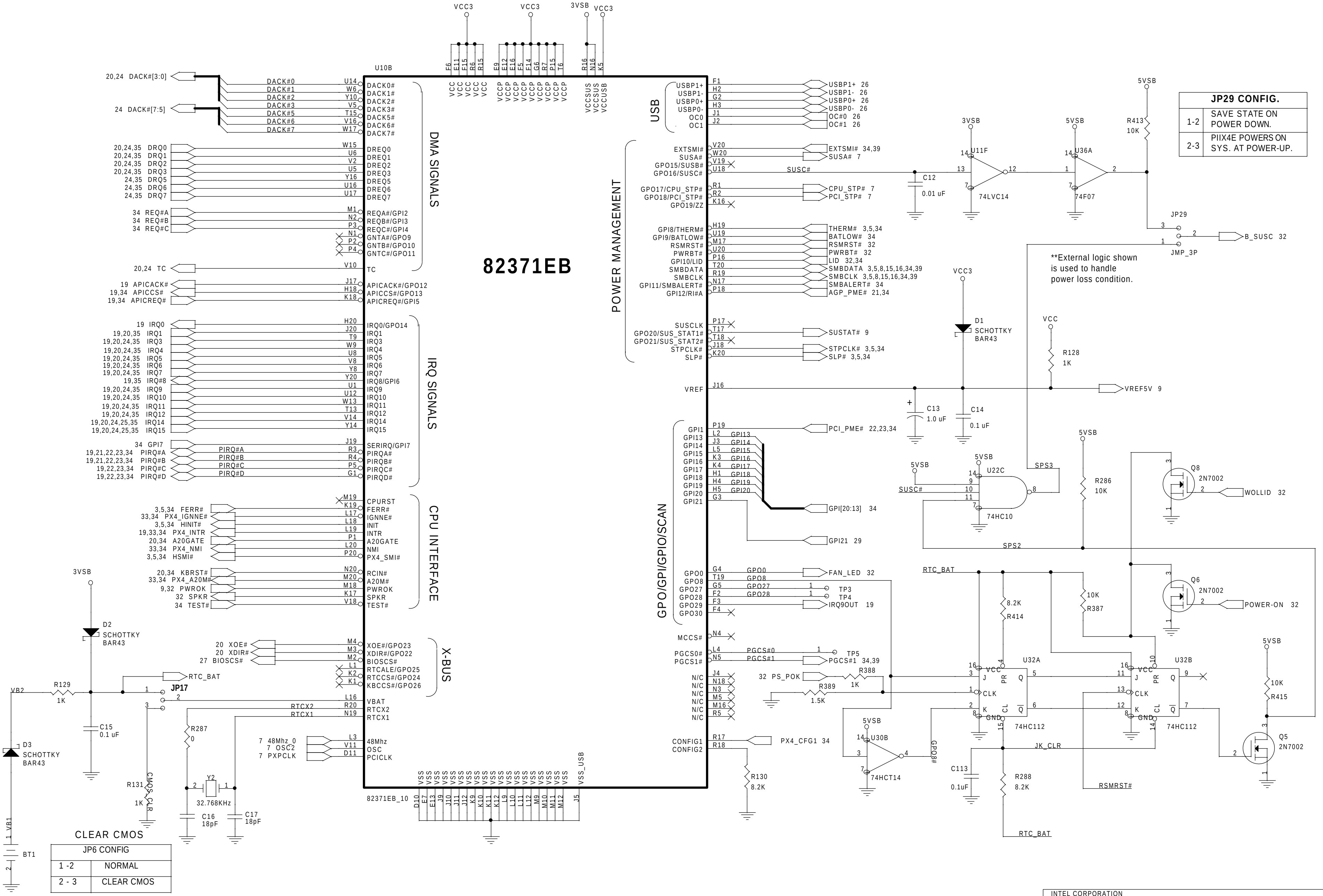
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: PIIX4E (PART I)

Size	Document Number	Rev
Custom	Intel(R) 440GX AGPset	1.0

Date: Friday, October 30, 1998 Sheet 17 of 40



82371EB
U10B
82371EB_10
DMA SIGNALS
IRQ SIGNALS
CPU INTERFACE
X-BUS
USB
POWER MANAGEMENT
GPO/GPI/GPIO/SCAN
VCC3
3VSB
5VSB
VCC
DACK#[3:0]
DACK#[7:5]
USBP1+ 26
USBP1- 26
USBP0+ 26
USBP0- 26
OC#0 26
OC#1 26
EXTSMI# 34,39
SUSA# 7
SUSC#
CPU_STP# 7
PCI_STP# 7
THERM# 3,5,34
BATLOW# 34
RSMRST# 32
PWRBT# 32
LID 32,34
SMBDATA 3,5,8,15,16,34,39
SMBCLK 3,5,8,15,16,34,39
SMBALERT# 34
AGP_PME# 21,34
SUSTAT# 9
STPCLK# 3,5,34
SLP# 3,5,34
VREF5V 9
PCI_PME# 22,23,34
GPI[20:13] 34
GPI21 29
FAN_LED 32
TP3
TP4
IRQ9OUT 19
TP5
PGCS#1 34,39
32 PS_POK
PX4_CFG1 34
U11F
74LVC14
U36A
74F07
C12
0.01 uF
R413
10K
JP29
JMP_3P
B_SUSC 32
**External logic shown
is used to handle
power loss condition.
D1
SCHOTTKY
BAR43
R128
1K
C13
1.0 uF
C14
0.1 uF
U22C
74HC10
SPS3
SPS2
R286
10K
Q8
2N7002
WOLLID 32
Q6
2N7002
POWER-ON 32
RTC_BAT
R414
8.2K
R387
10K
U32A
74HC112
U32B
74HC112
R388
1K
R389
1.5K
U30B
74HCT14
C113
0.1uF
R288
8.2K
JK_CLR
RSMRST#
R130
8.2K
R415
10K
Q5
2N7002
D2
SCHOTTKY
BAR43
R129
1K
VB2
RTC_BAT
JP17
C15
0.1 uF
D3
SCHOTTKY
BAR43
R131
1K
CMOS_CLR
R287
0
Y2
32.768KHz
C16
18pF
C17
18pF
BT1
VB1

JP29 CONFIG.

1-2	SAVE STATE ON POWER DOWN.
2-3	PIIX4E POWERS ON SYS. AT POWER-UP.

CLEAR CMOS

JP6 CONFIG	
1 -2	NORMAL
2 - 3	CLEAR CMOS

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PLATFORM COMPONENTS DIVISION
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Title	PIIX4E (PART II)	
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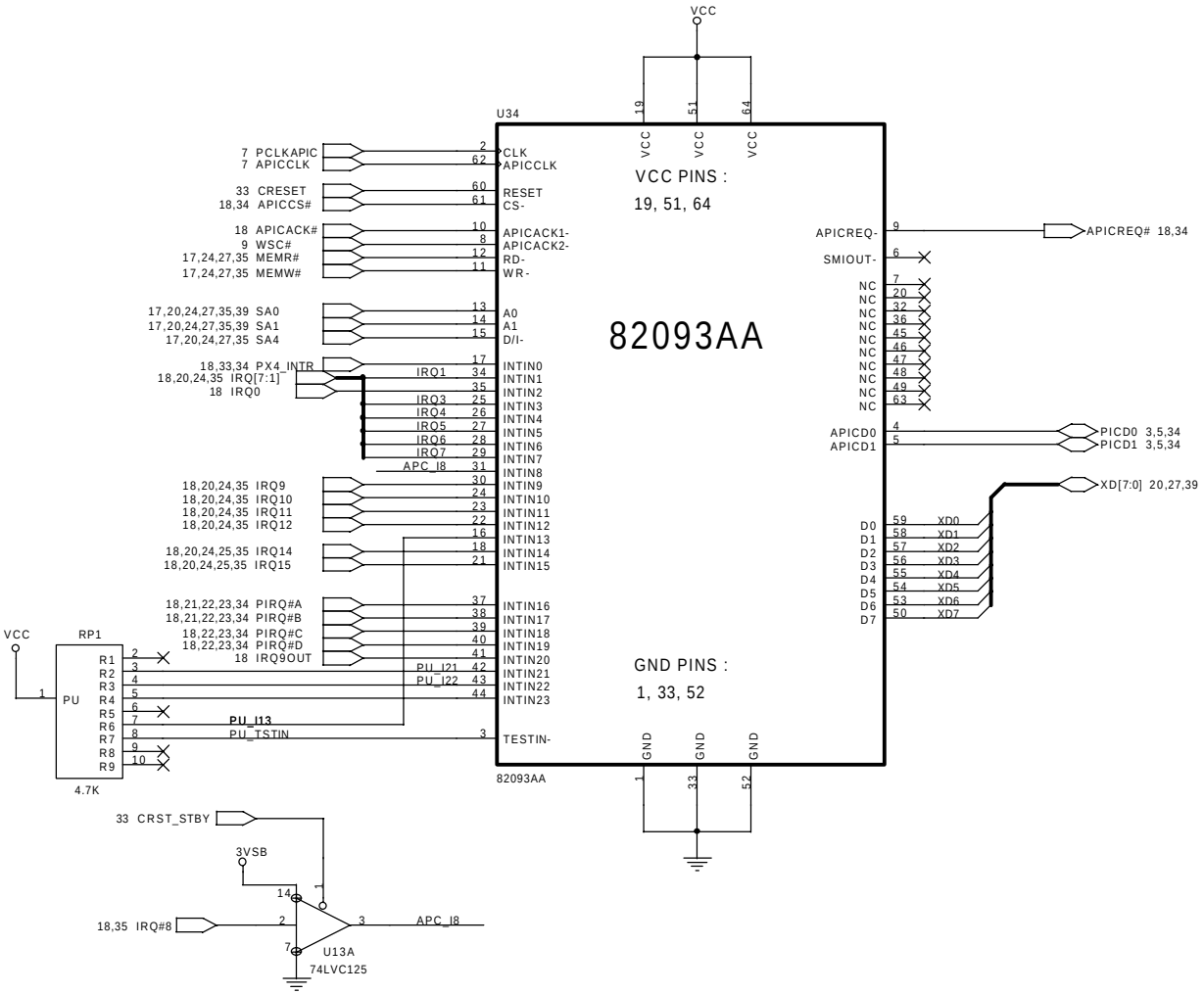
IOAPIC



INTEL CORPORATION		
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: IOAPIC		
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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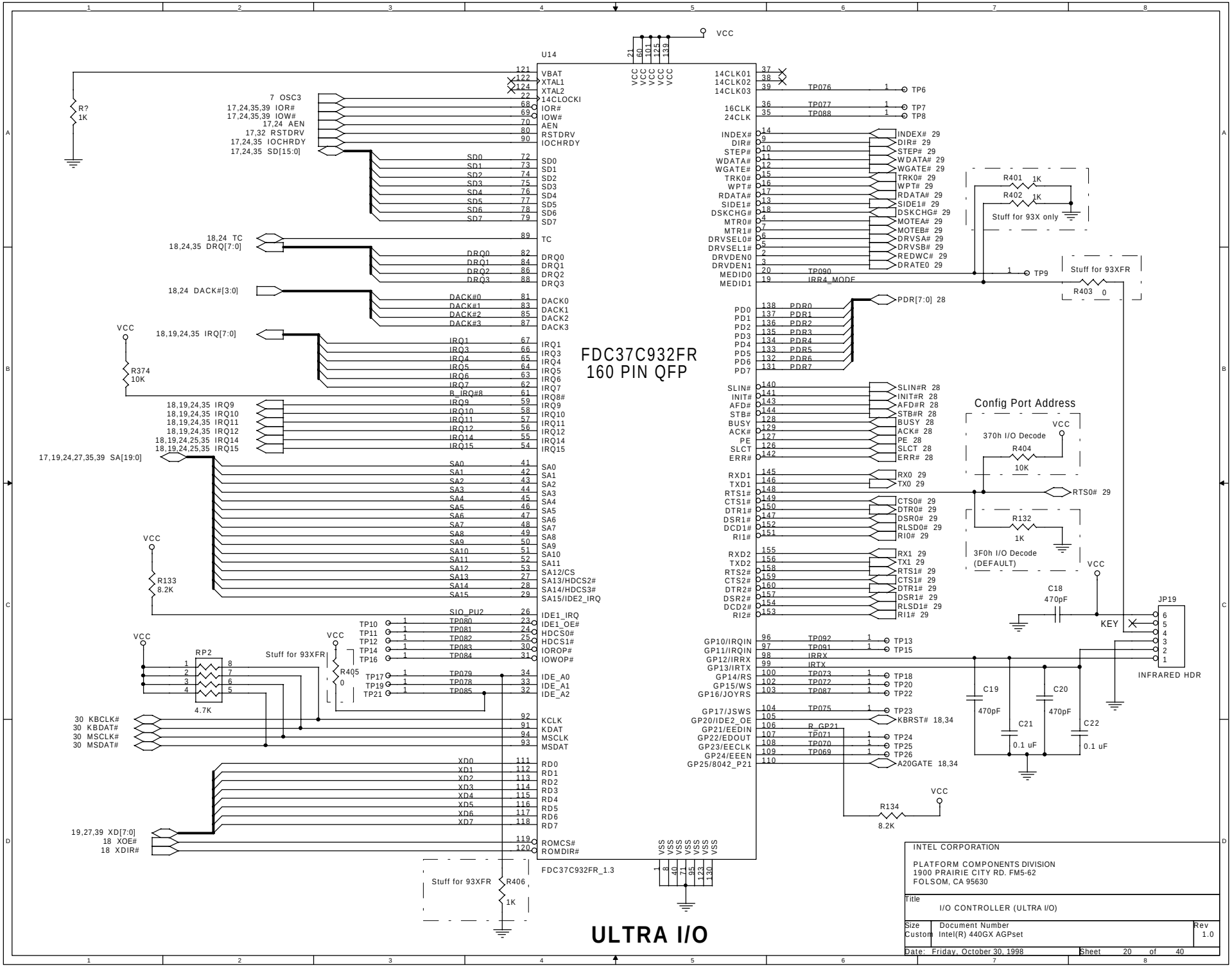
U14
FDC37C932FR
160 PIN QFP
FDC37C932FR_1.3
VCC
R?
1K
7 OSC3
17,24,35,39 IOR#
17,24,35,39 IOW#
17,24 AEN
17,32 RSTDRV
17,24,35 IOCHRDY
17,24,35 SD[15:0]
18,24 TC
18,24,35 DRQ[7:0]
18,24 DACK#[3:0]
18,19,24,35 IRQ[7:0]
R374
10K
18,19,24,35 IRQ9
18,19,24,35 IRQ10
18,19,24,35 IRQ11
18,19,24,35 IRQ12
18,19,24,25,35 IRQ14
18,19,24,25,35 IRQ15
17,19,24,27,35,39 SA[19:0]
R133
8.2K
RP2
4.7K
Stuff for 93XFR
R405
0
30 KBCLK#
30 KBDAT#
30 MSCLK#
30 MSDAT#
19,27,39 XD[7:0]
18 XOE#
18 XDIR#
Stuff for 93XFR
R406
1K
14CLK01
14CLK02
14CLK03
16CLK
24CLK
INDEX#
DIR#
STEP#
WDATA#
WGATE#
TRK0#
WPT#
RDATA#
SIDE1#
DSKCHG#
MTR0#
MTR1#
DRVSEL0#
DRVSEL1#
DRVDEN0
DRVDEN1
MEDID0
MEDID1
PDR[7:0] 28
SLIN#
INIT#
AFD#
STB#
BUSY
ACK#
PE
SLCT
ERR#
RXD1
TXD1
RTS1#
CTS1#
DTR1#
DSR1#
DCD1#
RI1#
RXD2
TXD2
RTS2#
CTS2#
DTR2#
DSR2#
DCD2#
RI2#
GP10/IRQIN
GP11/IRQIN
GP12/IRRX
GP13/IRTX
GP14/RS
GP15/WS
GP16/JOYRS
GP17/JSWS
GP20/IDE2_OE
GP21/EEDIN
GP22/EDOUT
GP23/EECLK
GP24/EEEN
GP25/8042_P21
IRR4_MODE
R_GP21
R401 1K
R402 1K
Stuff for 93X only
Stuff for 93XFR
R403 0
Config Port Address
370h I/O Decode
R404
10K
3F0h I/O Decode
(DEFAULT)
R132
1K
C18
470pF
KEY
JP19
INFRARED HDR
C19
470pF
C20
470pF
C21
0.1 uF
C22
0.1 uF
R134
8.2K
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1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
I/O CONTROLLER (ULTRA I/O)
Size
Custom
Document Number
Intel(R) 440GX AGPset
Rev
1.0
Date: Friday, October 30, 1998
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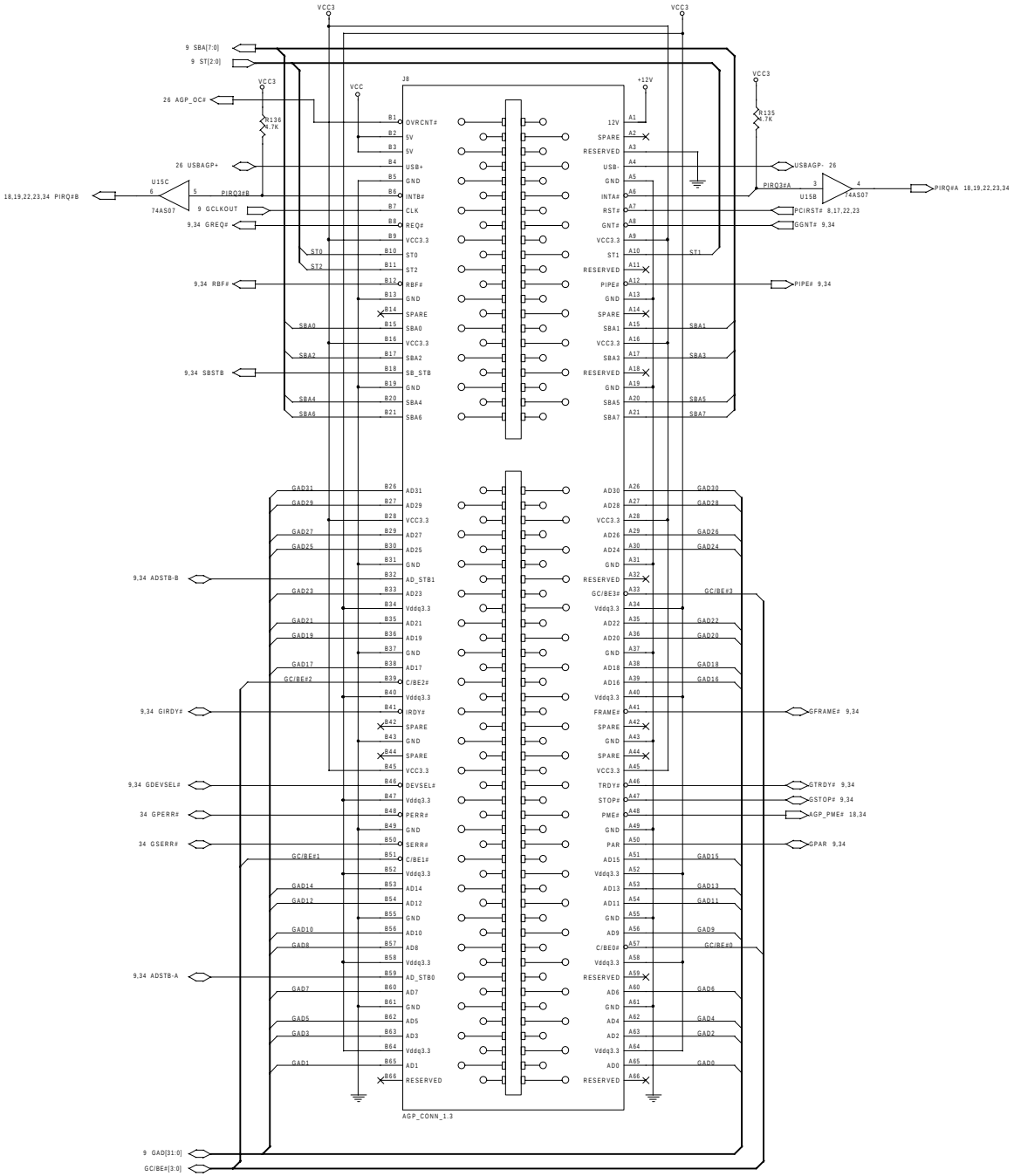
ULTRA I/O

AGP CONNECTOR



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Title: ACCELERATED GRAPHICS PORT (AGP) CONNECTOR

Size: Custom | Document Number: Intel(R) 440GX AGPset | Rev: 1.0

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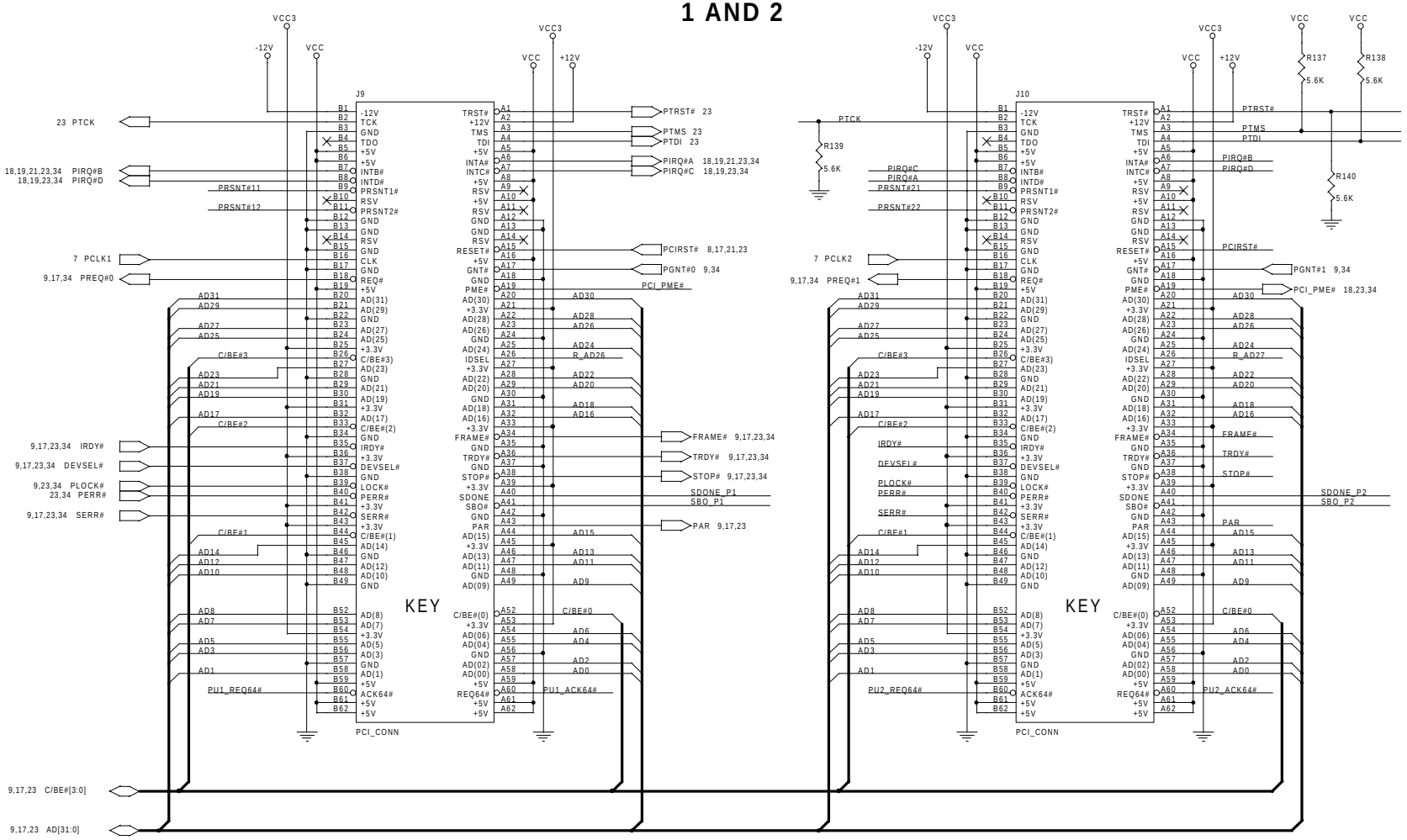
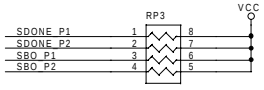
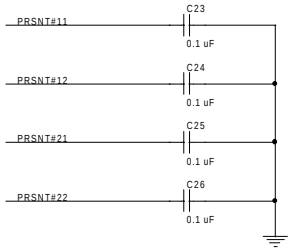
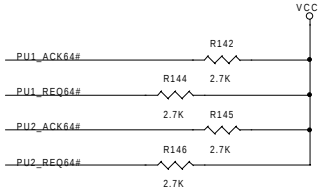
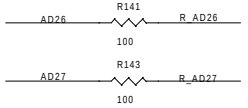
PCI CONNECTORS
1 AND 2











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PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: PCI CONNECTORS 1 & 2		
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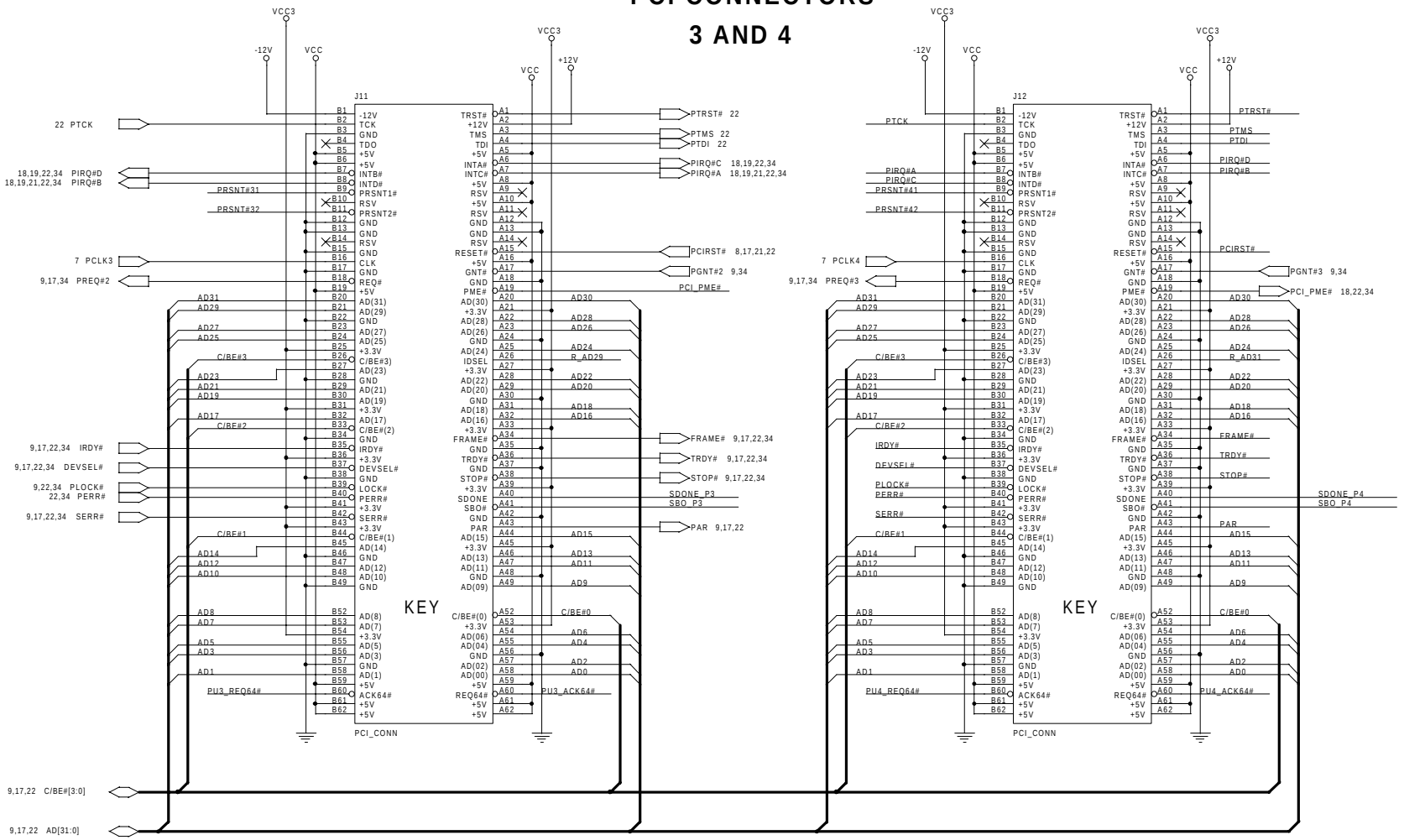
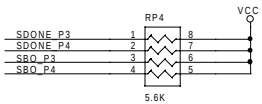
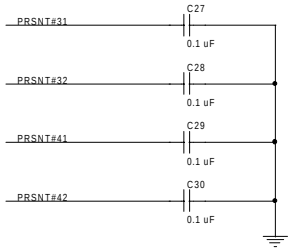
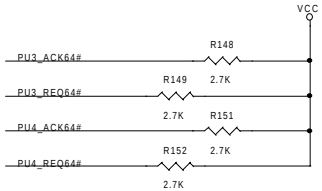
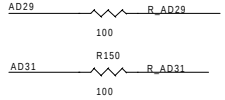
PCI CONNECTORS 3 AND 4











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1900 PRAIRIE CITY RD. FM5-62
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Title	PCI CONNECTORS 3 & 4	
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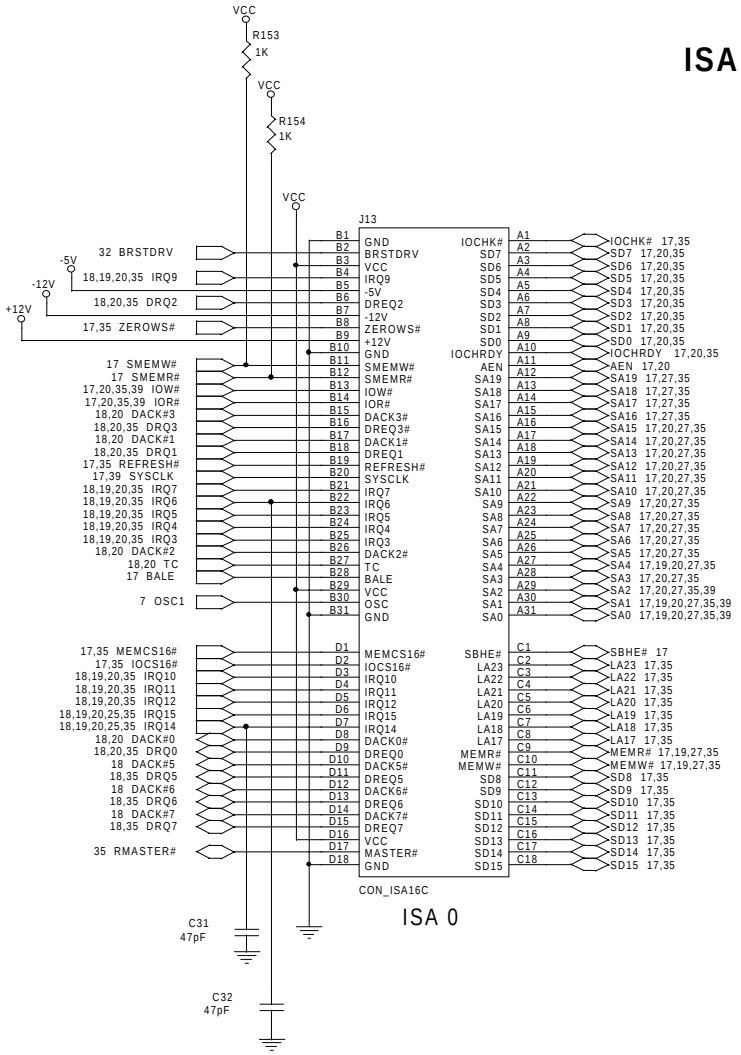
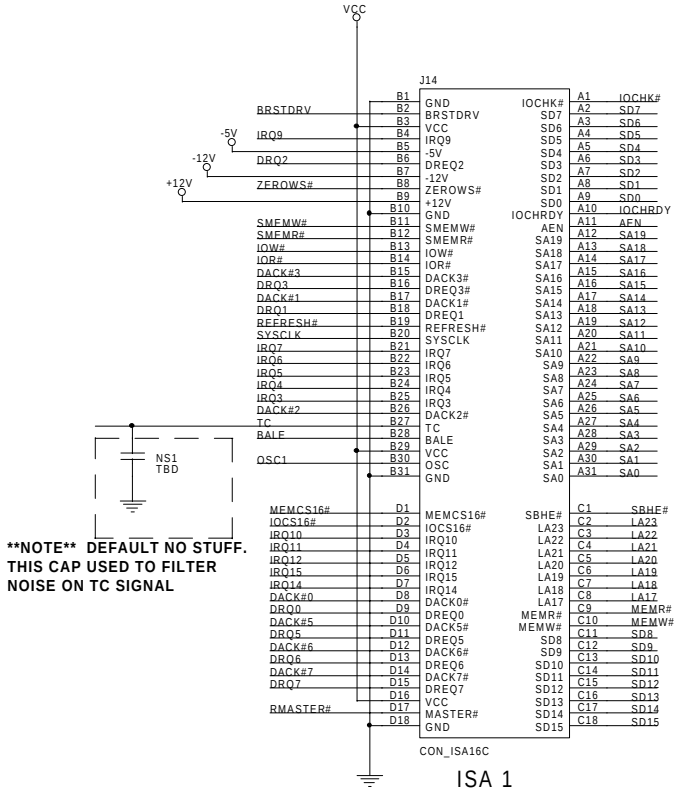
ISA SLOTS 0 & 1



ISA 0



ISA 1

****NOTE** DEFAULT NO STUFF. THIS CAP USED TO FILTER NOISE ON TC SIGNAL**

INTEL CORPORATION PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: ISA SLOTS		
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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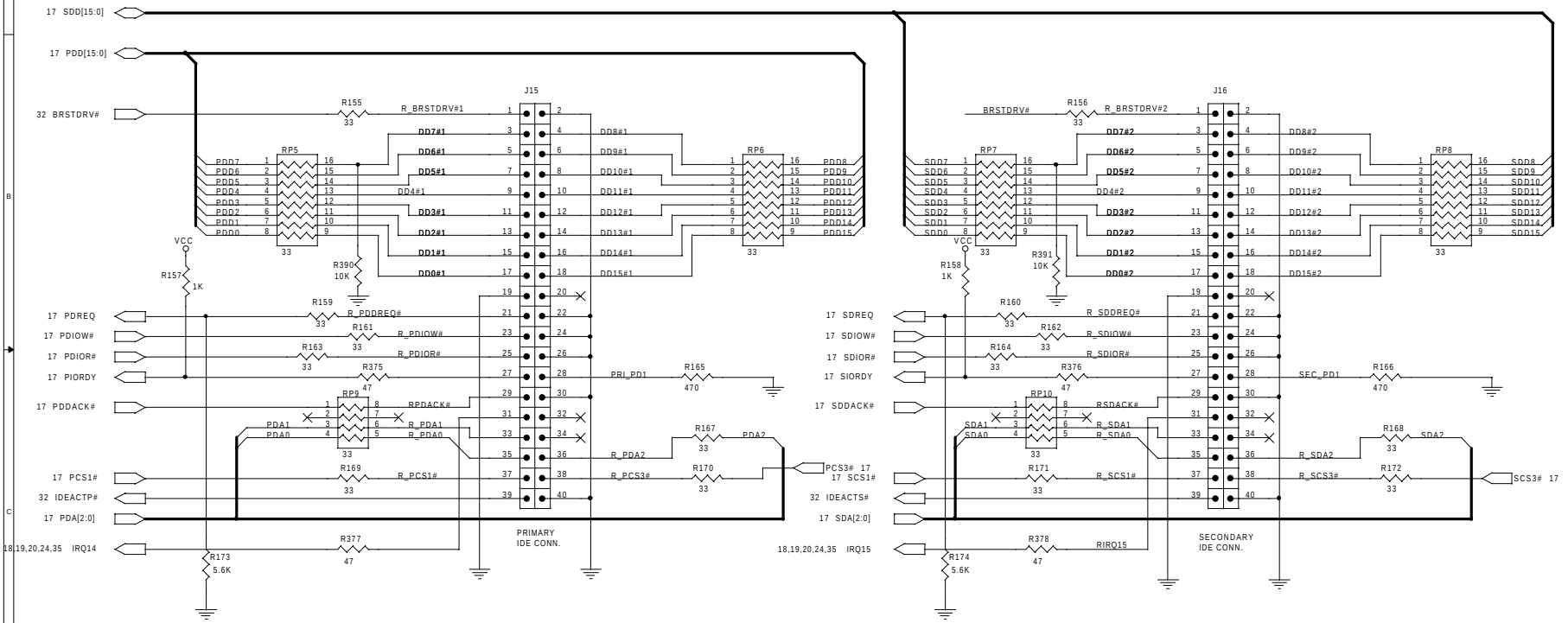
IDE CONNECTORS



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PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: PCI IDE CONNECTORS		
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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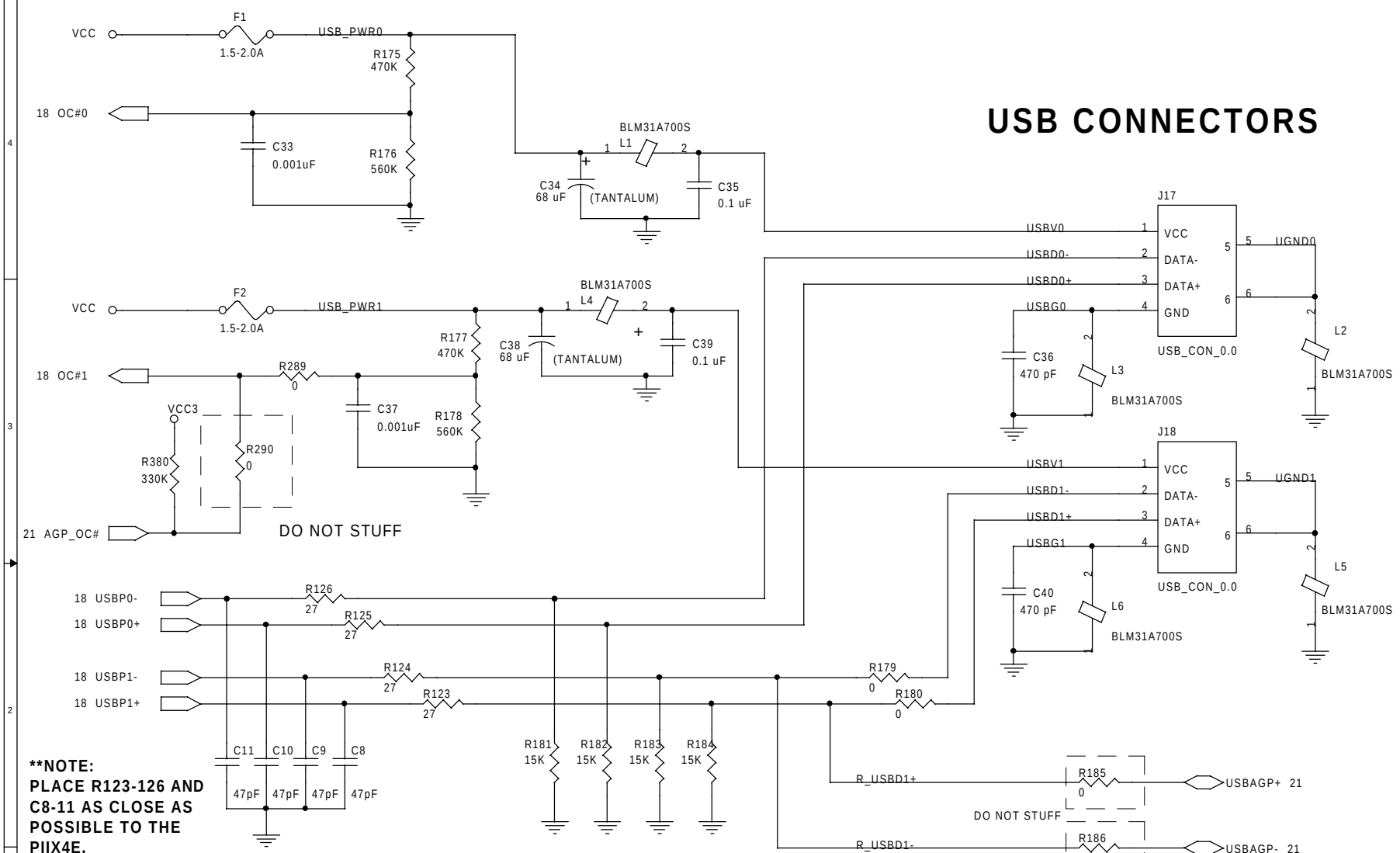
USB CONNECTORS



****NOTE:
PLACE R123-126 AND
C8-11 AS CLOSE AS
POSSIBLE TO THE
PIIX4E.**

NOTE: USE PIIX4E APPLICATION NOTE FOR LAYOUT GUIDELINES

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1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: USB HEADER

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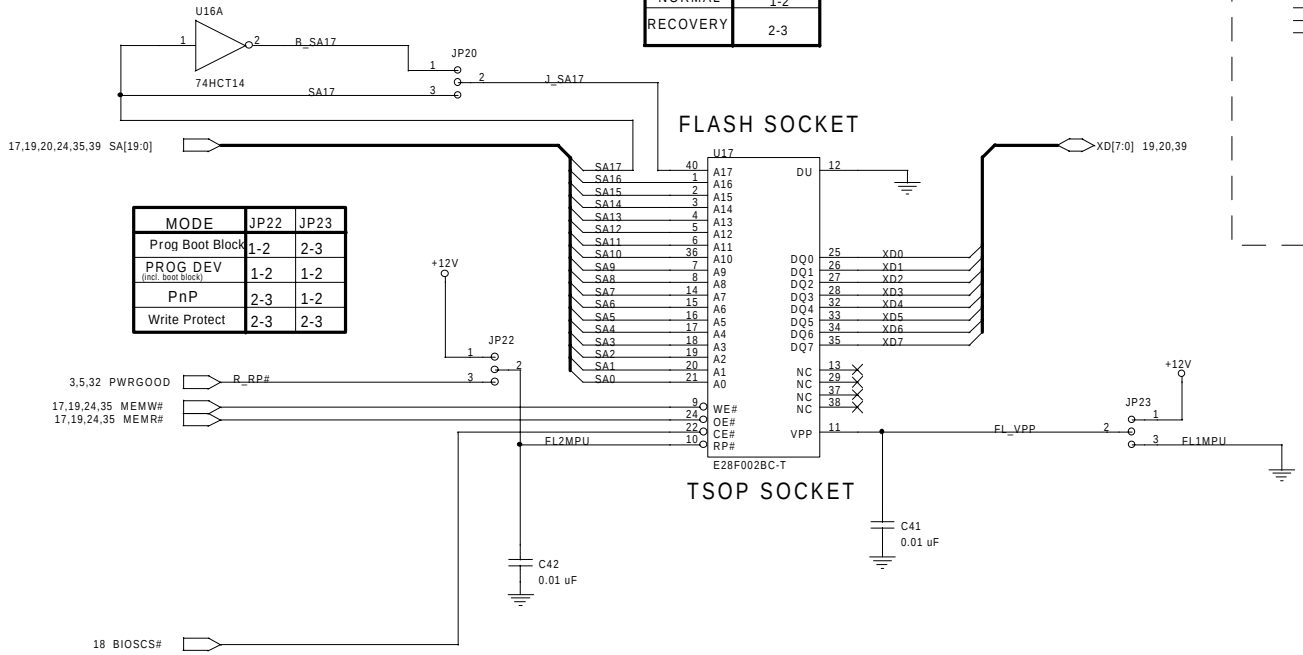
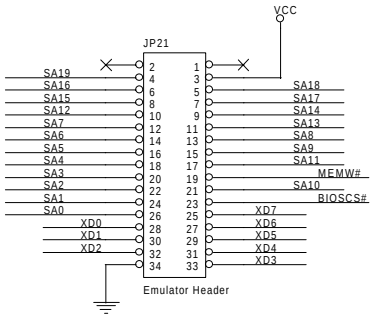
SYSTEM ROM

MODE	JP20
NORMAL	1-2
RECOVERY	2-3

MODE	JP22	JP23
Prog Boot Block	1-2	2-3
PROG DEV (incl. boot block)	1-2	1-2
PnP	2-3	1-2
Write Protect	2-3	2-3



STUFFING OPTION



* Header provided for BIOS emulation

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PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: SYSTEM ROM

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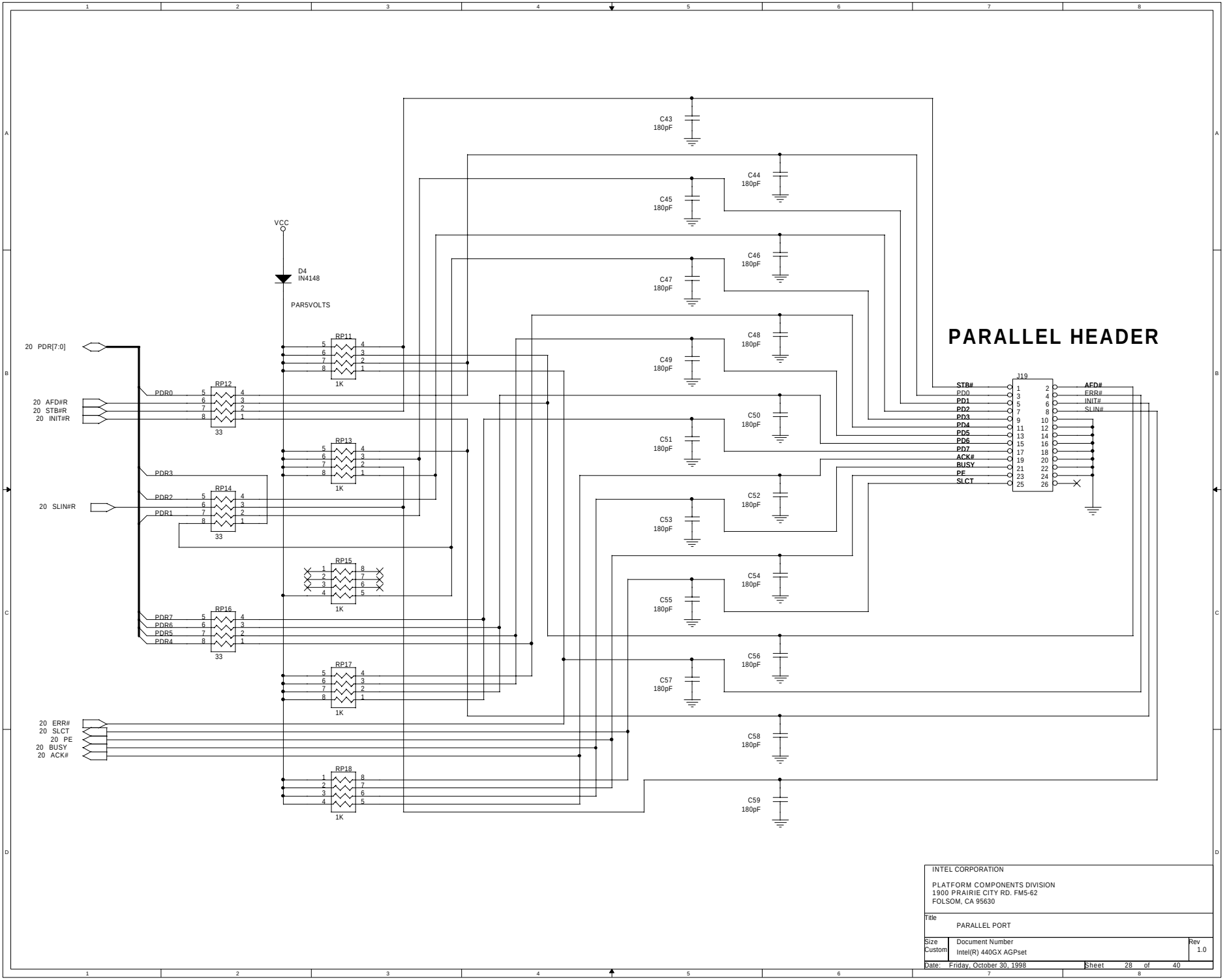

INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: PARALLEL PORT

Size	Document Number	Rev
Custom	Intel(R) 440GX AGPset	1.0

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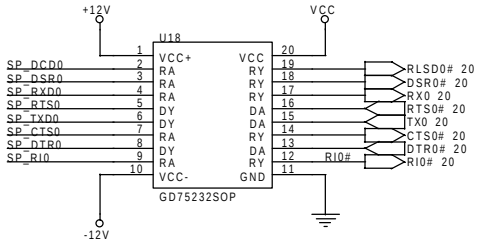
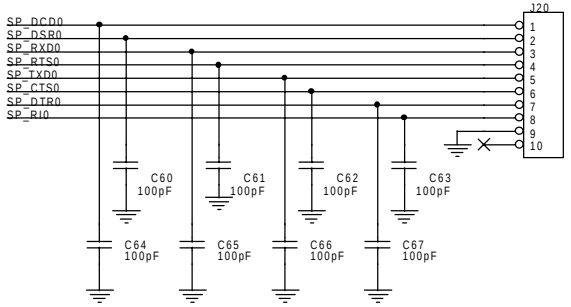
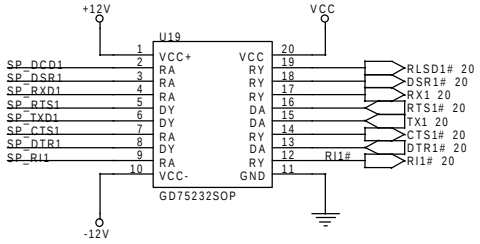
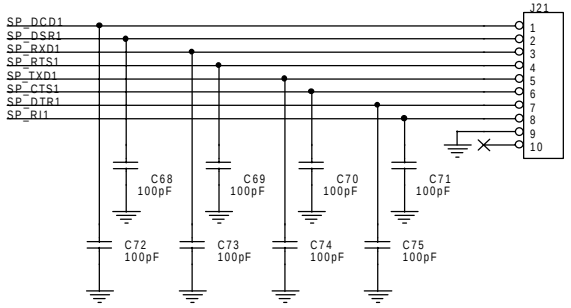


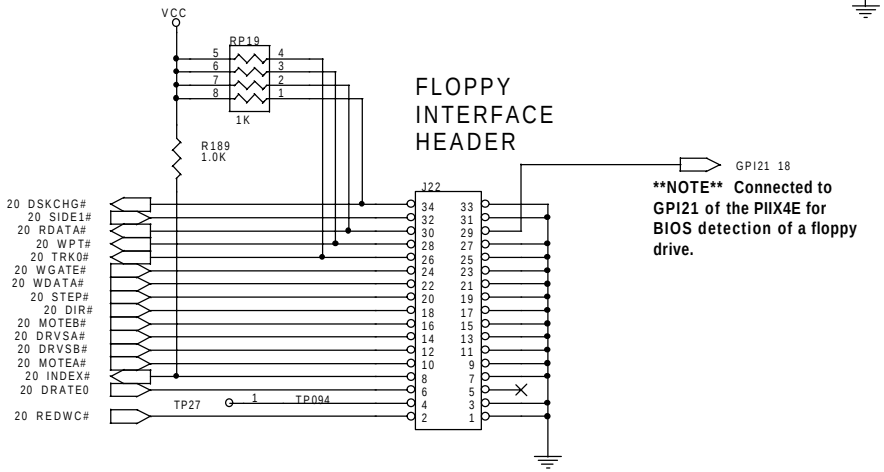


COM 0 HEADER





COM 1 HEADER



****NOTE** Connected to GPI21 of the PIIX4E for BIOS detection of a floppy drive.**

INTEL CORPORATION PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: SERIAL AND FLOPPY		
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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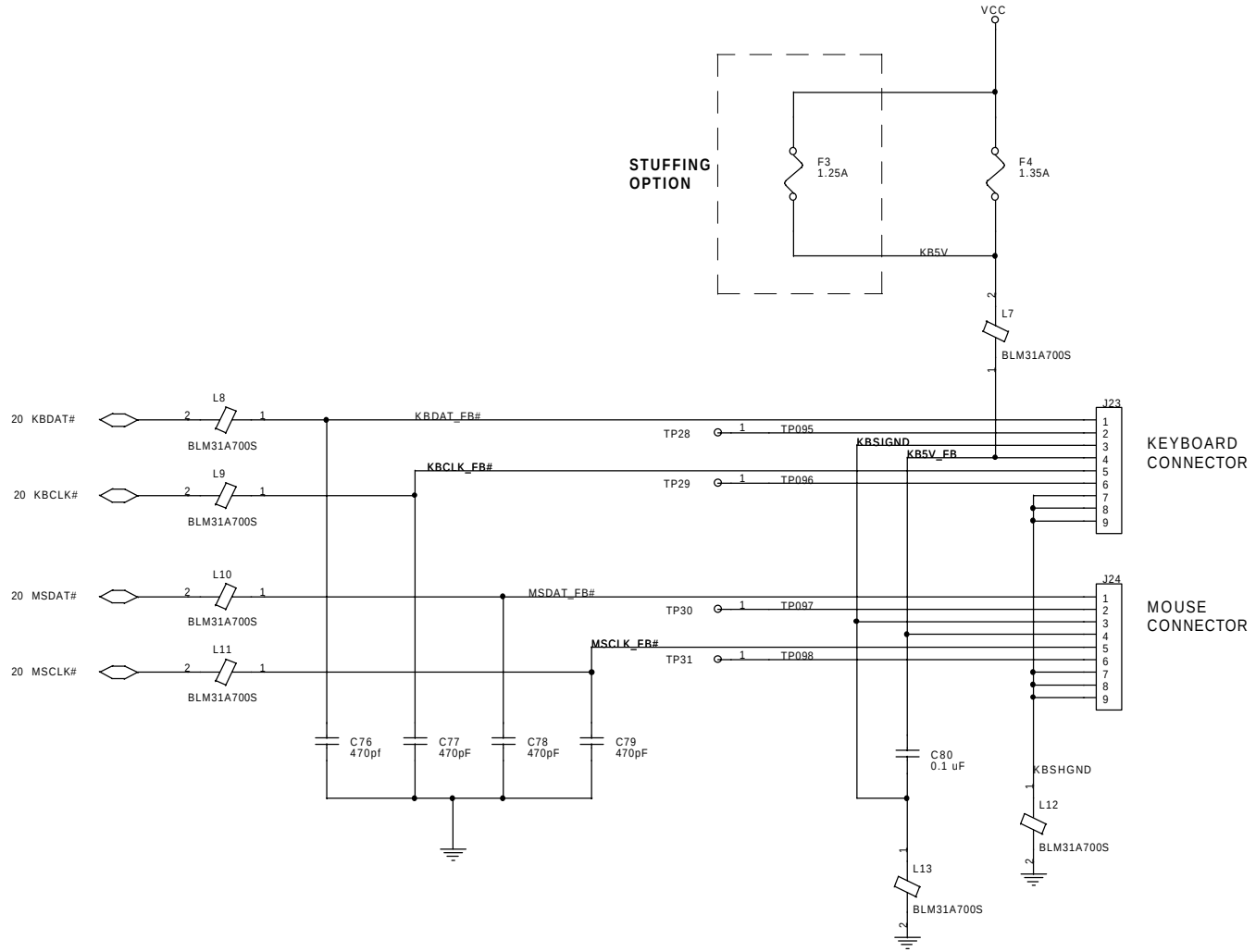
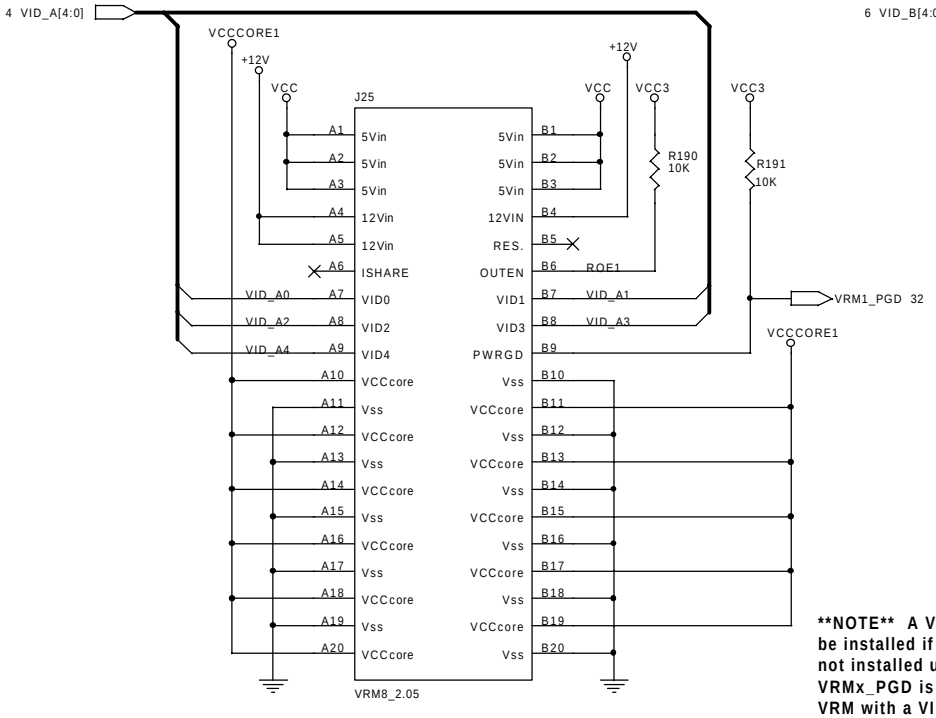
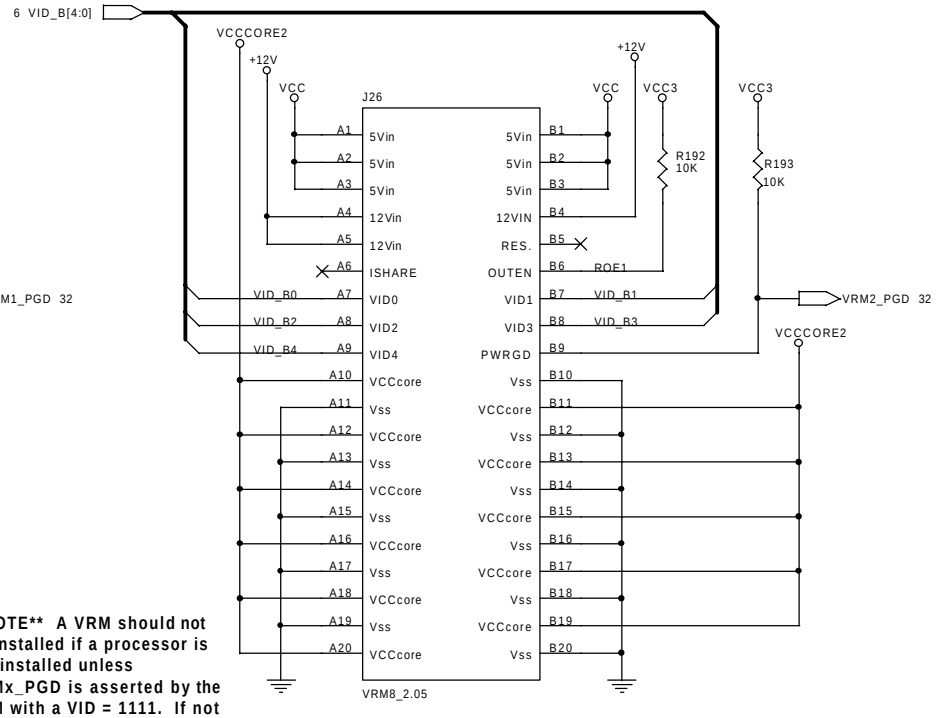
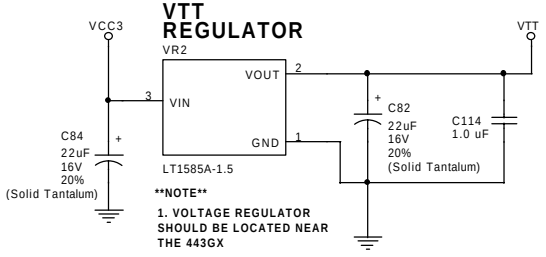


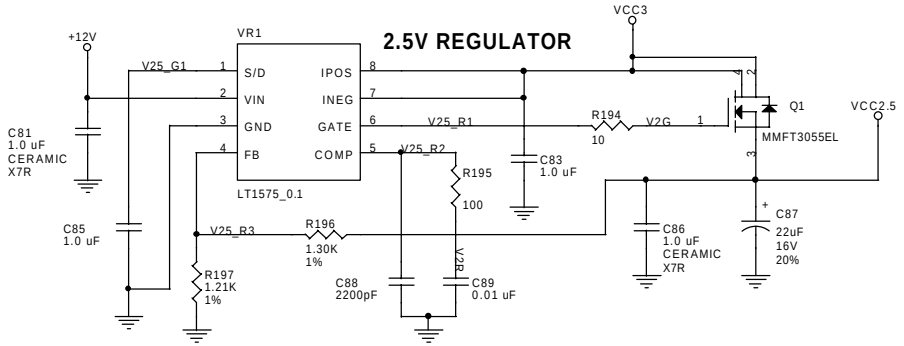
INTEL CORPORATION PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: KEYBOARD/MOUSE INTERFACE		
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
Date: Friday, October 30, 1998	Sheet 30 of 40	





****NOTE** A VRM should not be installed if a processor is not installed unless VRMx_PGD is asserted by the VRM with a VID = 1111. If not asserted by the VRM, then circuitry must be provided to the block VRMx_PGD for the unpopulated Slot 1.**





INTEL CORPORATION		
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: DC-DC CONVERTER CONNECTORS		
Size: Custom	Document Number: Intel(R) 440GX AGPset	Rev: 1.0
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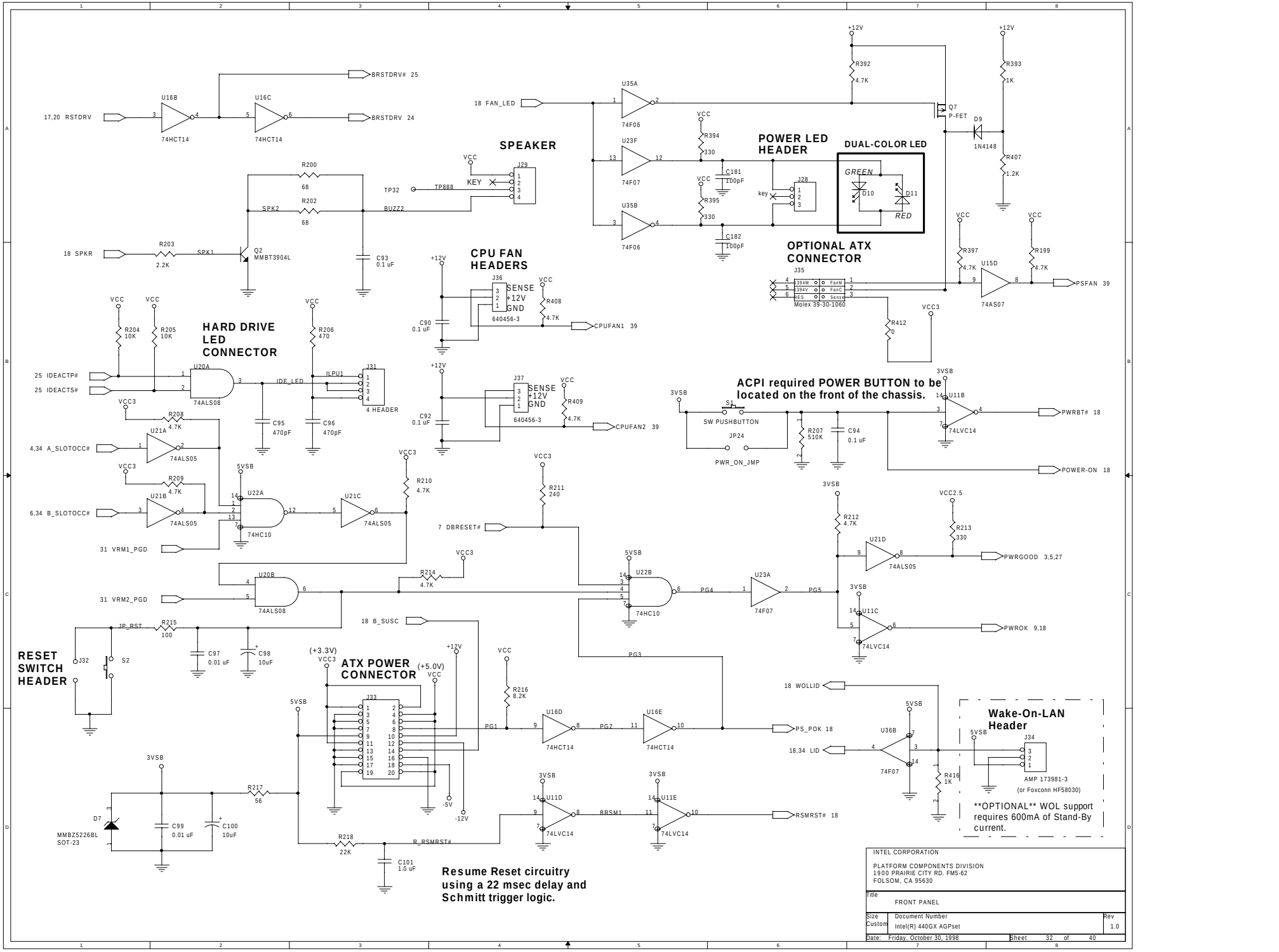
SPEAKER
POWER LED HEADER
DUAL-COLOR LED
GREEN
RED
OPTIONAL ATX CONNECTOR
CPU FAN HEADERS
HARD DRIVE LED CONNECTOR
ACPI required POWER BUTTON to be located on the front of the chassis.
SW PUSHBUTTON
PWR_ON_JMP
RESET SWITCH HEADER
ATX POWER CONNECTOR
Wake-On-LAN Header
OPTIONAL WOL support requires 600mA of Stand-By current.
Resume Reset circuitry using a 22 msec delay and Schmitt trigger logic.
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
FRONT PANEL
Intel(R) 440GX AGPset
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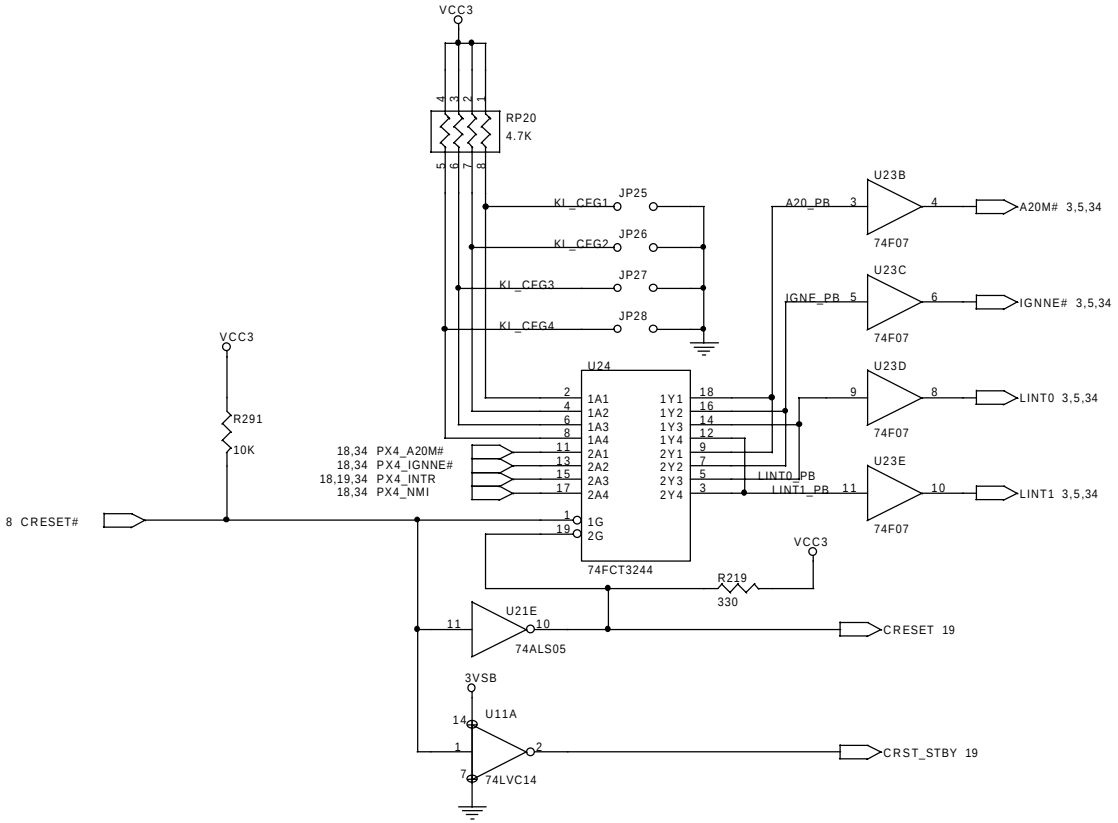
PROCESSOR BUS/CORE FREQUENCY



Processor Core Freq : System Bus Freq	LINT[1] JP28	LINT[0] JP27	IGNNE# JP26	A20M# JP25
2	L	L	L	L
3	L	L	H	L
4	L	L	L	H
5	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
Reserved	All Other Combinations, HLLL-HHHL			
2	H	H	H	H

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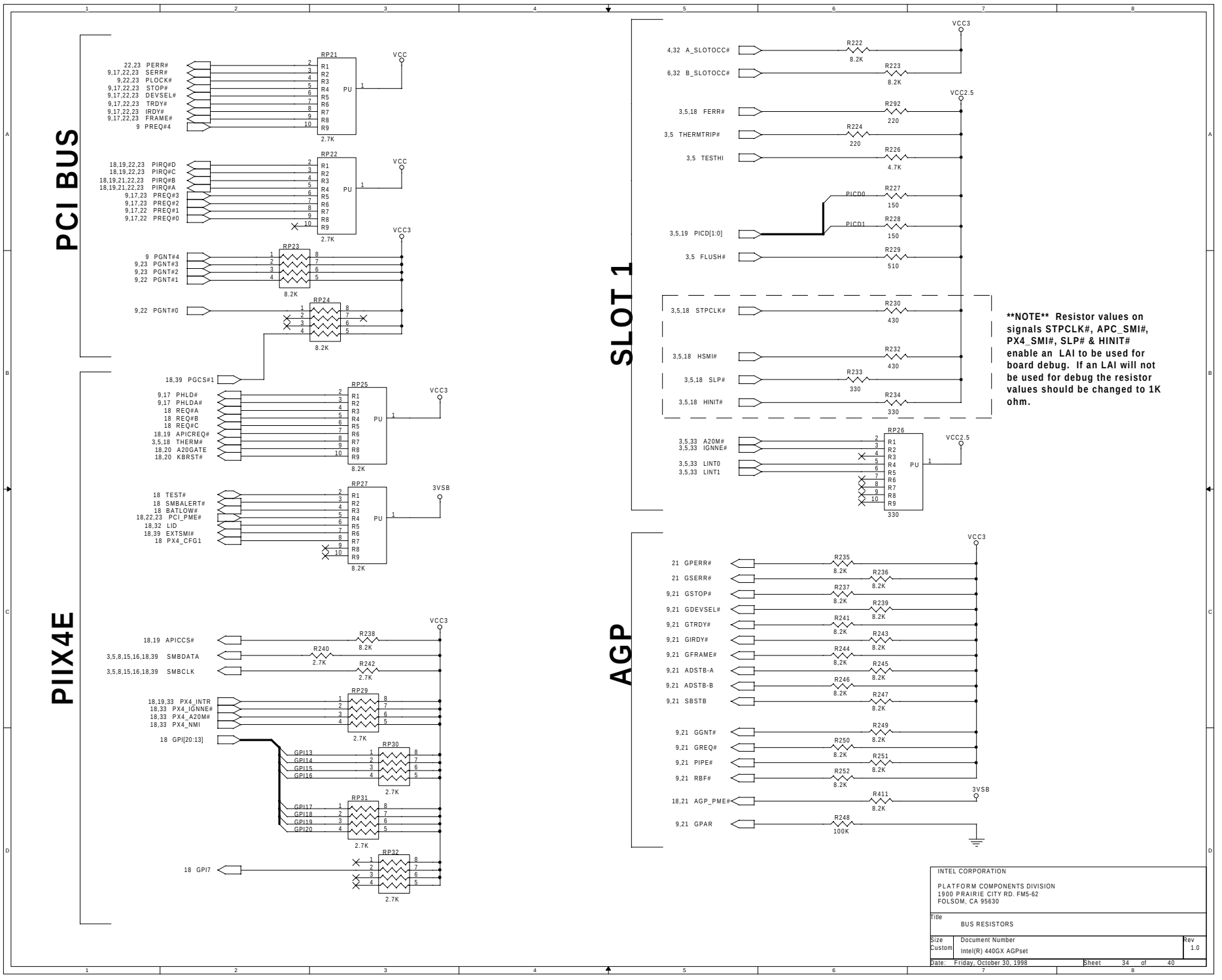
PCI BUS
PIIX4E
SLOT 1
AGP
RP21
RP22
RP23
RP24
RP25
RP26
RP27
RP29
RP30
RP31
RP32
VCC
VCC3
VCC2.5
3VSB
PU
2.7K
8.2K
22,23 PERR#
9,17,22,23 SERR#
9,22,23 PLOCK#
9,17,22,23 STOP#
9,17,22,23 DEVSEL#
9,17,22,23 TRDY#
9,17,22,23 IRDY#
9,17,22,23 FRAME#
9 PREQ#4
18,19,22,23 PIRQ#D
18,19,22,23 PIRQ#C
18,19,21,22,23 PIRQ#B
18,19,21,22,23 PIRQ#A
9,17,23 PREQ#3
9,17,23 PREQ#2
9,17,22 PREQ#1
9,17,22 PREQ#0
9 PGNT#4
9,23 PGNT#3
9,23 PGNT#2
9,22 PGNT#1
9,22 PGNT#0
18,39 PGCS#1
9,17 PHLD#
9,17 PHLDA#
18 REQ#A
18 REQ#B
18 REQ#C
18,19 APICREQ#
3,5,18 THERM#
18,20 A20GATE
18,20 KBRST#
18 TEST#
18 SMBALERT#
18 BATLOW#
18,22,23 PCI_PME#
18,32 LID
18,39 EXTSMI#
18 PX4_CFG1
18,19 APICCS#
3,5,8,15,16,18,39 SMBDATA
3,5,8,15,16,18,39 SMBCLK
18,19,33 PX4_INTR
18,33 PX4_IGNNE#
18,33 PX4_A20M#
18,33 PX4_NMI
18 GPI[20:13]
GPI13
GPI14
GPI15
GPI16
GPI17
GPI18
GPI19
GPI20
18 GPI7
R238
R240
R242
4,32 A_SLOTOCC#
6,32 B_SLOTOCC#
3,5,18 FERR#
3,5 THERMTRIP#
3,5 TESTHI
3,5,19 PICD[1:0]
3,5 FLUSH#
3,5,18 STPCLK#
3,5,18 HSMI#
3,5,18 SLP#
3,5,18 HINIT#
3,5,33 A20M#
3,5,33 IGNNE#
3,5,33 LINT0
3,5,33 LINT1
R222
R223
R292
R224
R226
PICD0
PICD1
R227
R228
R229
R230
R232
R233
R234
330
430
510
4.7K
220
150
100K
NOTE Resistor values on signals STPCLK#, APC_SMI#, PX4_SMI#, SLP# & HINIT# enable an LAI to be used for board debug. If an LAI will not be used for debug the resistor values should be changed to 1K ohm.
21 GPERR#
21 GSERR#
9,21 GSTOP#
9,21 GDEVSEL#
9,21 GTRDY#
9,21 GIRDY#
9,21 GFRAME#
9,21 ADSTB-A
9,21 ADSTB-B
9,21 SBSTB
9,21 GGNT#
9,21 GREQ#
9,21 PIPE#
9,21 RBF#
18,21 AGP_PME#
9,21 GPAR
R235
R236
R237
R239
R241
R243
R244
R245
R246
R247
R249
R250
R251
R252
R411
R248
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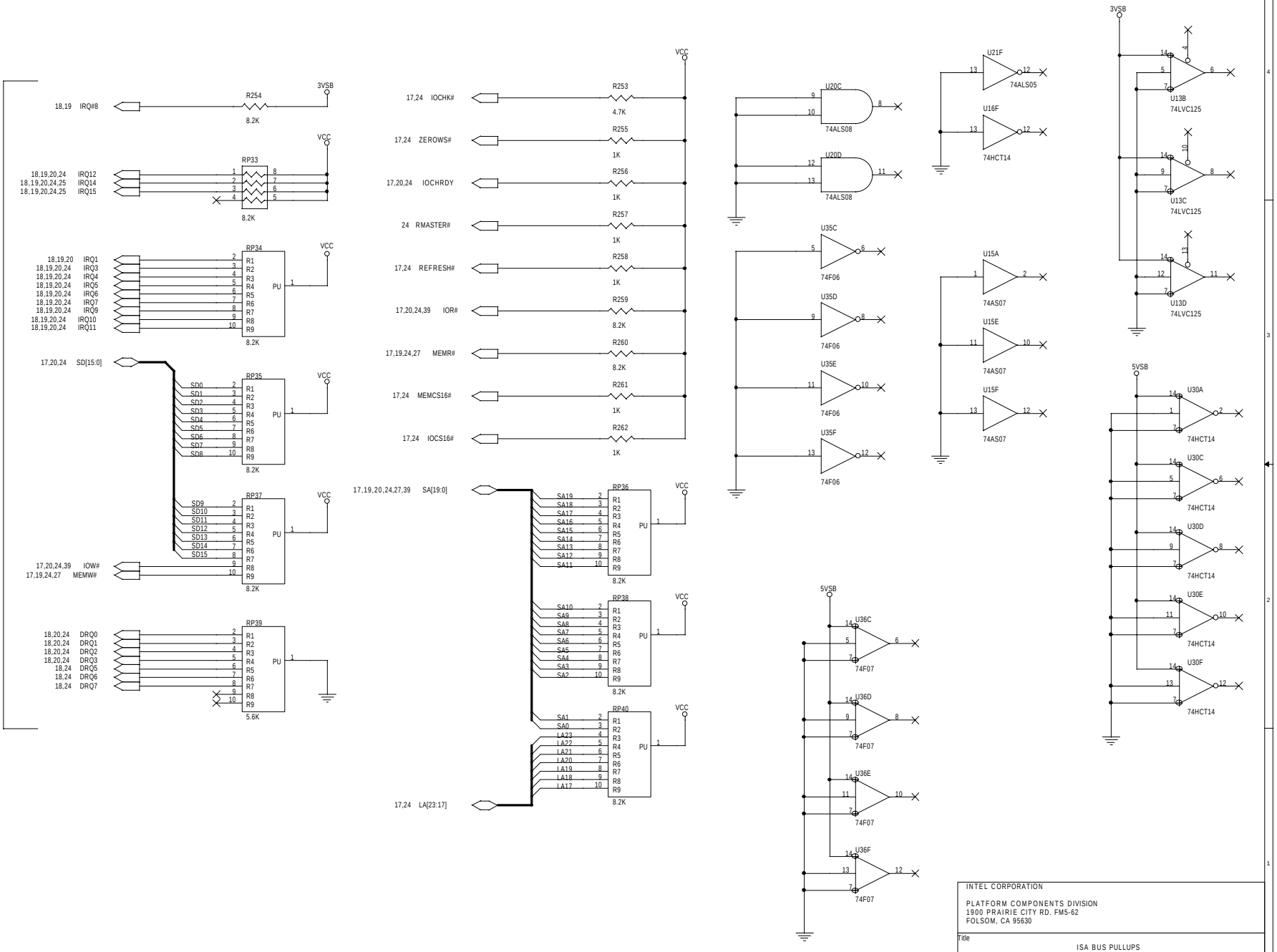
ISA BUS


UNUSED GATES
18,19 IRQ#8
R254
8.2K
3VSB
18,19,20,24 IRQ12
18,19,20,24,25 IRQ14
18,19,20,24,25 IRQ15
RP33
8.2K
VCC
18,19,20 IRQ1
18,19,20,24 IRQ3
18,19,20,24 IRQ4
18,19,20,24 IRQ5
18,19,20,24 IRQ6
18,19,20,24 IRQ7
18,19,20,24 IRQ9
18,19,20,24 IRQ10
18,19,20,24 IRQ11
RP34
8.2K
17,20,24 SD[15:0]
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
RP35
8.2K
SD9
SD10
SD11
SD12
SD13
SD14
SD15
RP37
8.2K
17,20,24,39 IOW#
17,19,24,27 MEMW#
18,20,24 DRQ0
18,20,24 DRQ1
18,20,24 DRQ2
18,20,24 DRQ3
18,24 DRQ5
18,24 DRQ6
18,24 DRQ7
RP39
5.6K
17,24 IOCHK#
R253
4.7K
17,24 ZEROWS#
R255
1K
17,20,24 IOCHRDY
R256
1K
24 RMASTER#
R257
1K
17,24 REFRESH#
R258
1K
17,20,24,39 IOR#
R259
8.2K
17,19,24,27 MEMR#
R260
8.2K
17,24 MEMCS16#
R261
1K
17,24 IOCS16#
R262
1K
17,19,20,24,27,39 SA[19:0]
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
RP36
8.2K
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
RP38
8.2K
SA1
SA0
LA23
LA22
LA21
LA20
LA19
LA18
LA17
RP40
8.2K
17,24 LA[23:17]
U20C
74ALS08
U20D
74ALS08
U35C
74F06
U35D
74F06
U35E
74F06
U35F
74F06
U21F
74ALS05
U16F
74HCT14
U15A
74AS07
U15E
74AS07
U15F
74AS07
3VSB
U13B
74LVC125
U13C
74LVC125
U13D
74LVC125
5VSB
U30A
74HCT14
U30C
74HCT14
U30D
74HCT14
U30E
74HCT14
U30F
74HCT14
5VSB
U36C
74F07
U36D
74F07
U36E
74F07
U36F
74F07
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ISA BUS PULLUPS
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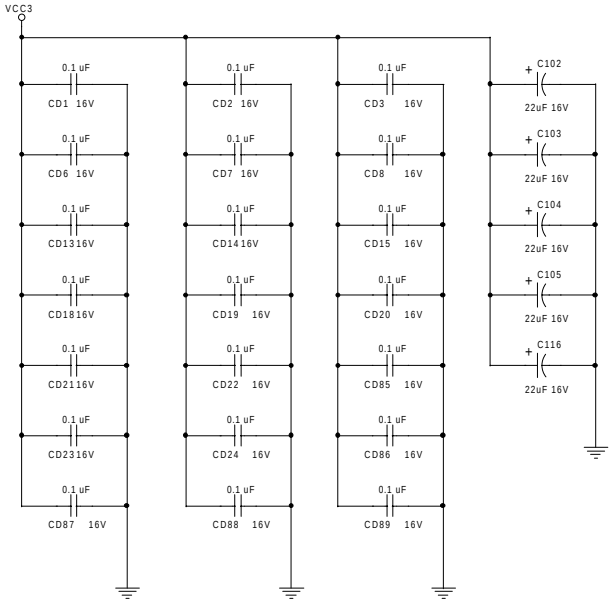
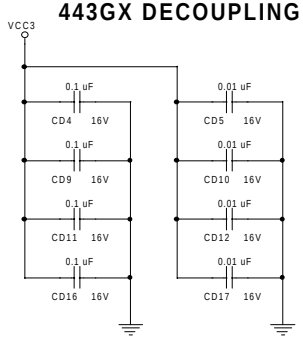
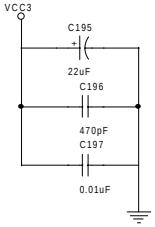
DIMM DECOUPLING



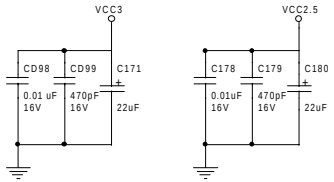
443GX DECOUPLING



CKBF DECOUPLING



CK100 DECOUPLING



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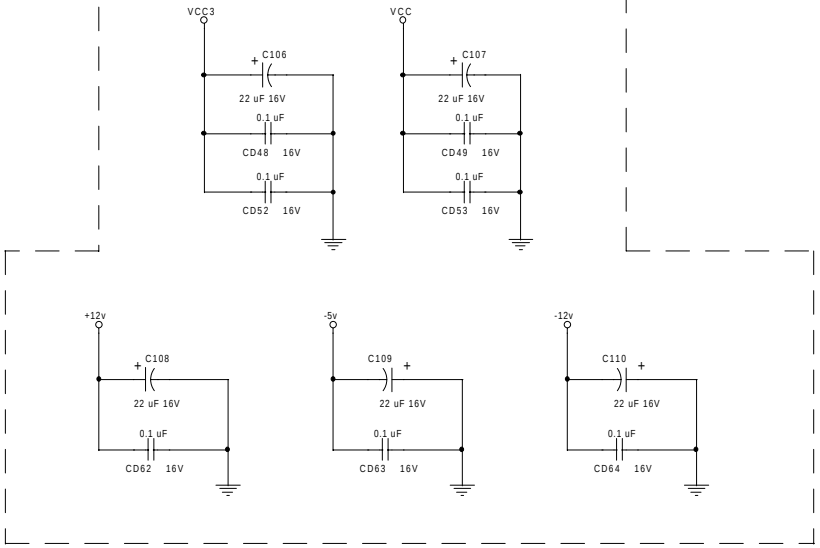
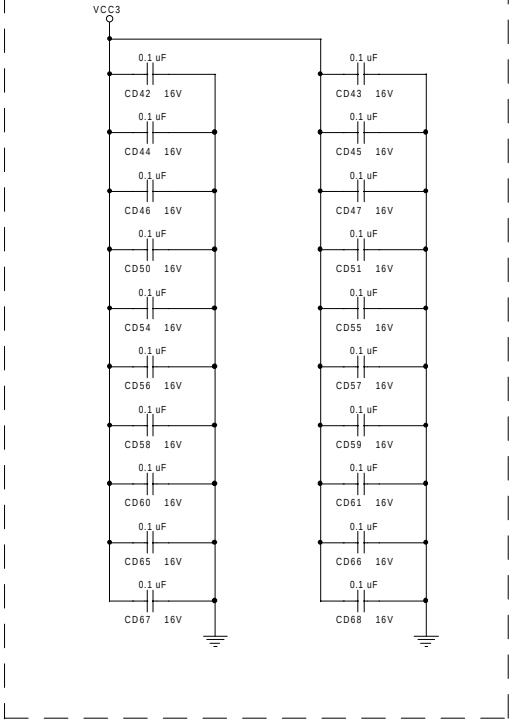
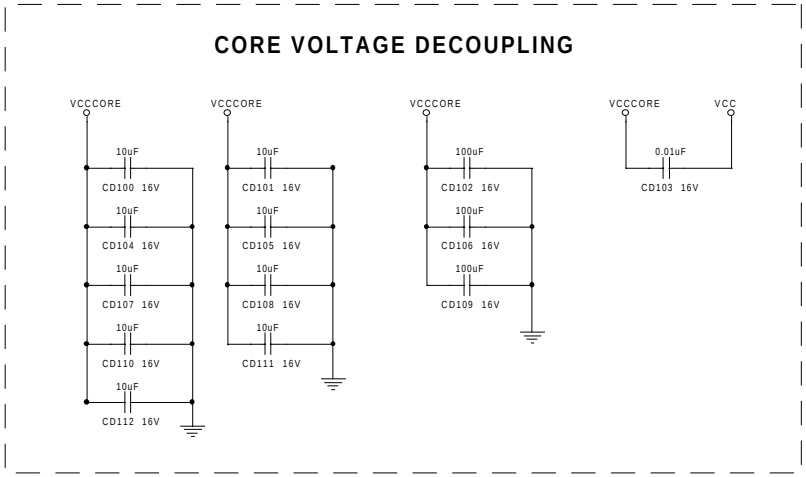
BULK POWER DECOUPLING



3 VOLT DECOUPLING



CORE VOLTAGE DECOUPLING



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Title: 3.3 VOLT AND BULK POWER DECOUPLING

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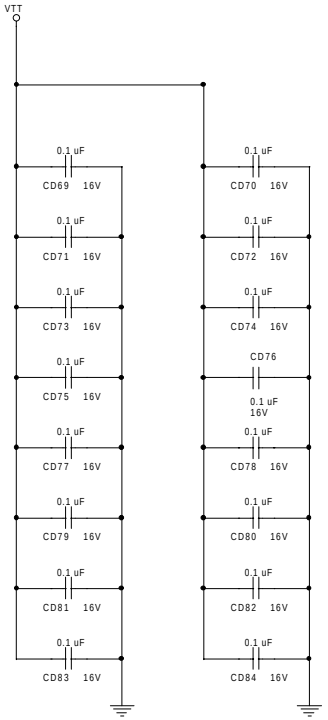
**THIS TERMINATION DECOUPLING IS OPTIONAL.

TERMINATION VOLTAGE DECOUPLING



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Title: TERMINATION DECOUPLING		
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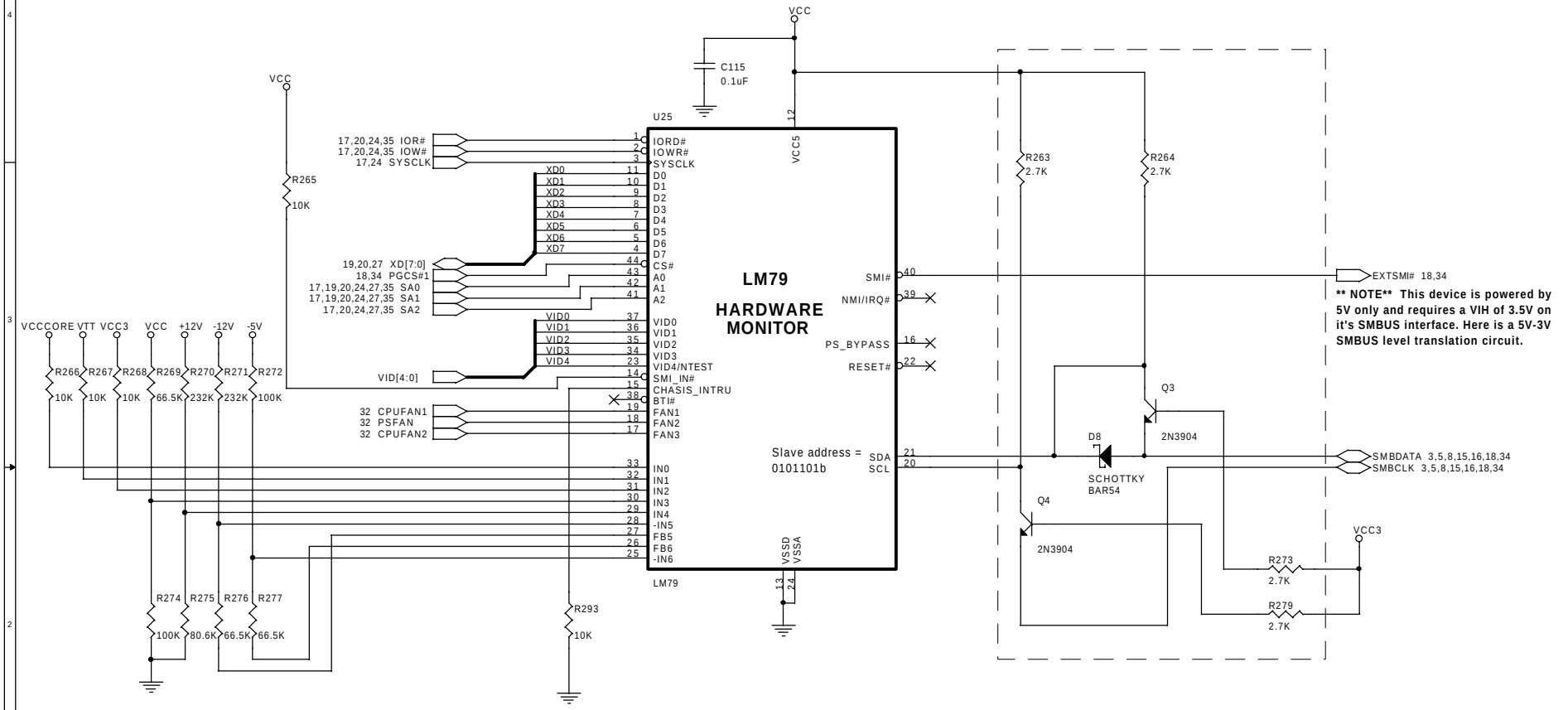

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