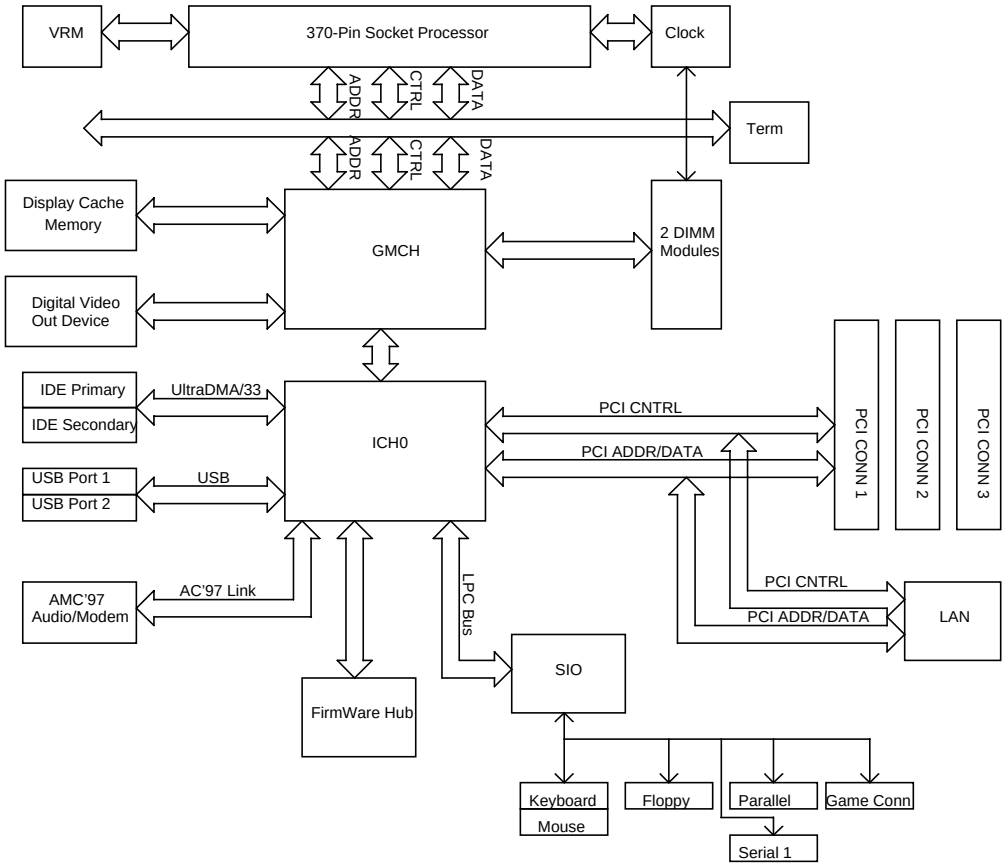
INTEL(R) CELERON(TM) PROCESSOR (PPGA)/INTEL(R) 810 CHIPSET
UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS
REVISION 1.3

** PLEASE NOTE THESE SCHEMATICS ARE SUBJECT TO CHANGE

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD COVER SHEET		REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 5-26-1999 17:09	PROJECT: INTEL(R) 810 CHIPSET SHEET: 1 OF 40

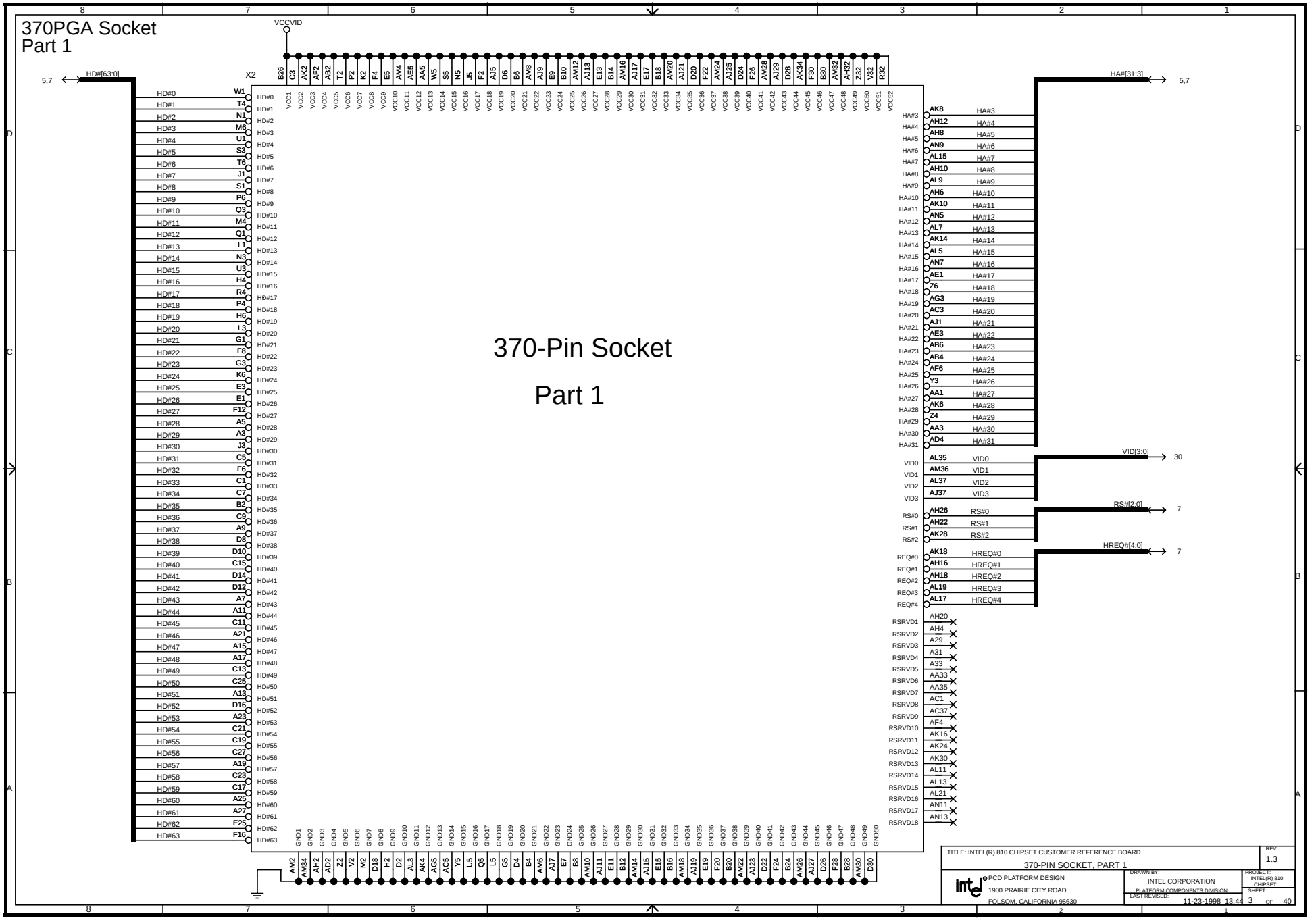
Block Diagram

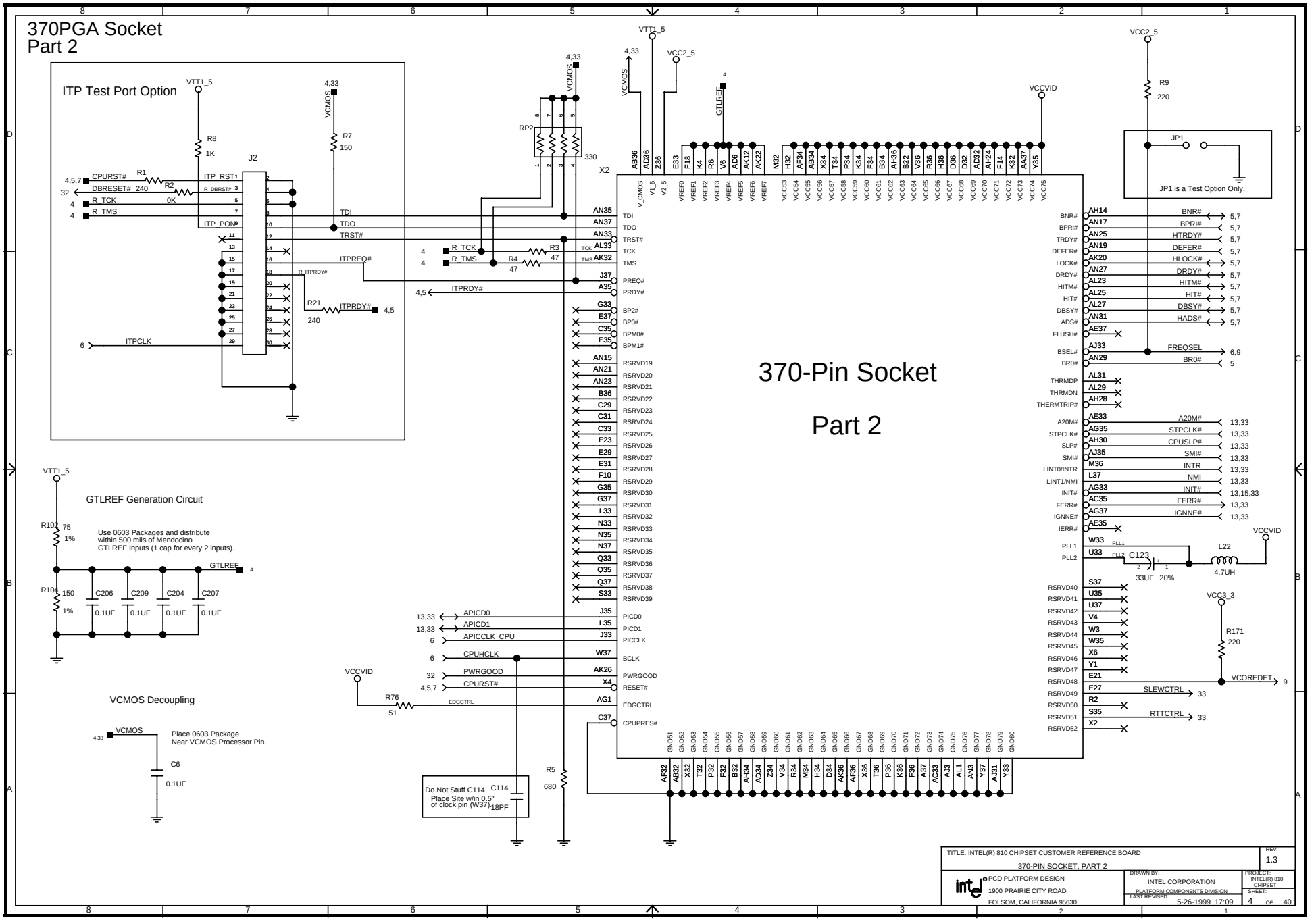


Device Table

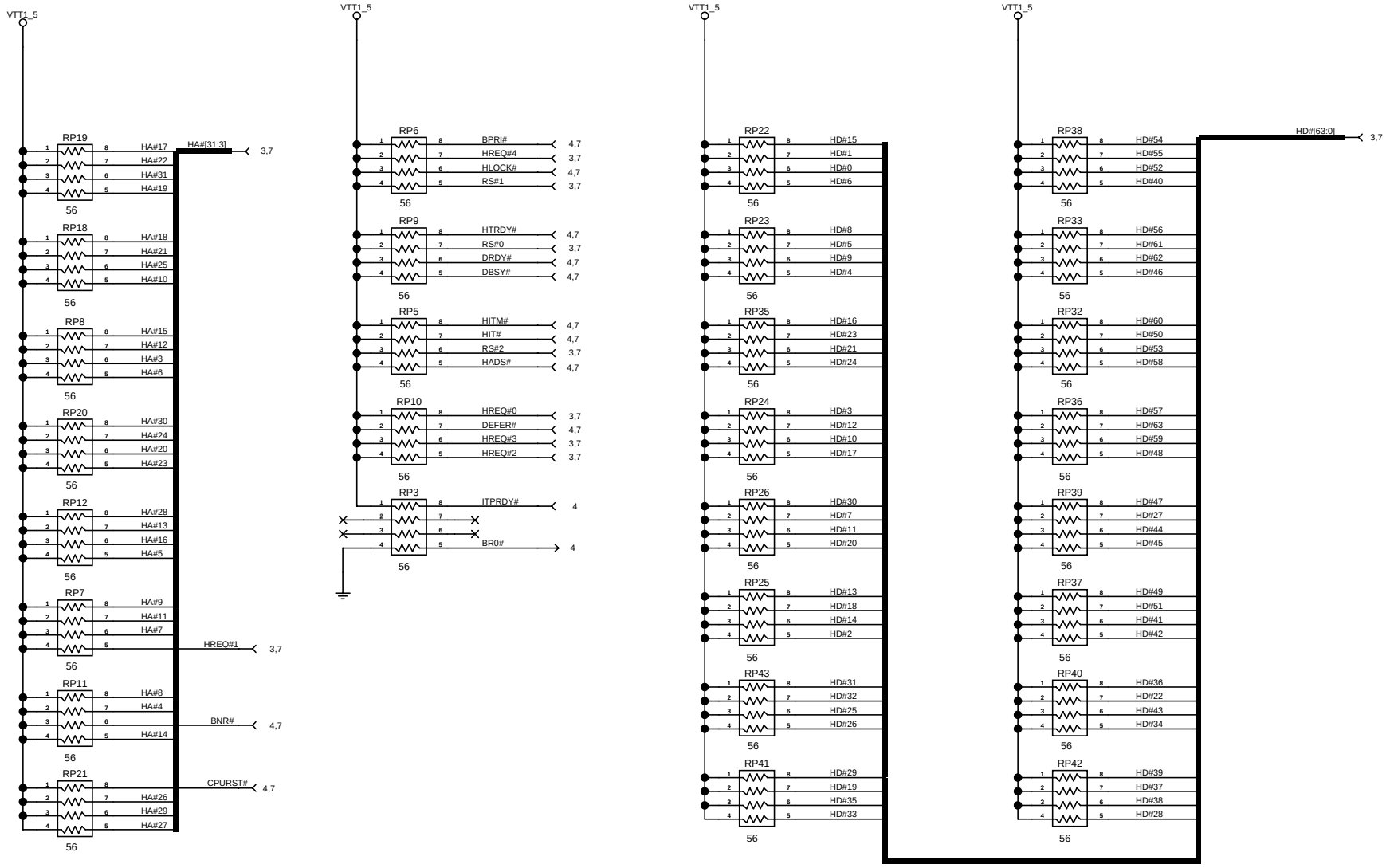
REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U12	74lvc14a	A,B,C,D	32
U16,U17	gd75232		22
U15	lpc47b27_a		16
U3	74lvc06a	A,B,C,D	29,32
U1	ck-whitney		6
U2	82810-DC100		7,8,9
U14	82801AB		13,14
U7	sii-dfp		24
U13	82559		27
U8,U9	1x16sdram		10
U10	74lvc08a	A,B	32
U6	qst3384		25
U18	93c46		27
U4	74ls132	A,B	29,32
U5	74lvc07a	A,B,C	29,31
U11	74lvc07a	A,B,C	19,31
VR2,VR3	lt1587ad		29
VR4	lt1117_3		29
VR1	ltc1753		30
VR5	lt1585ad		29

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD
BLOCK DIAGRAM
REV: 1.3
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY: INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
PROJECT: INTEL(R) 810 CHIPSET
LAST REVISED: 11-23-1998 13:43
SHEET: 2 OF 40


370PGA Socket
Part 1
370-Pin Socket
Part 1
VCCVID
X2
HD#[63:0]
HA#[31:3]
VID[3:0]
RS#[2:0]
HREQ#[4:0]
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD
370-PIN SOCKET, PART 1
REV: 1.3
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
PROJECT: INTEL(R) 810 CHIPSET
LAST REVISED: 11-23-1998 13:44
SHEET: 3 OF 40

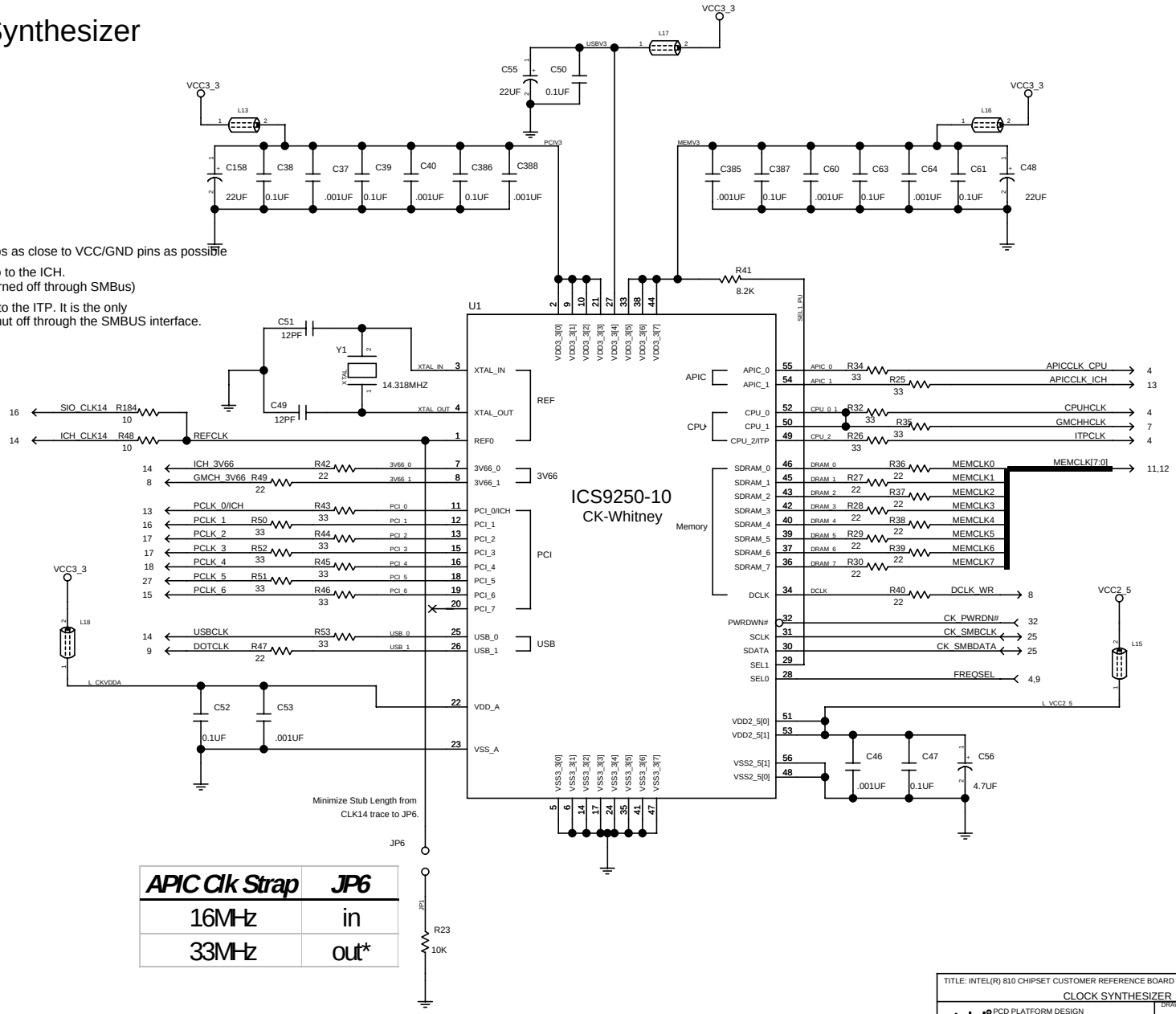

370PGA Socket
Part 2
ITP Test Port Option
VTT1_5
VCMOS
4,33
R8
1K
R7
150
J2
CPURST#
DBRESET#
R_TCK
R_TMS
ITP_PON
ITP_RST1
R_DBRST#
R1
R2
240
0K
TDI
TDO
TRST#
ITPREQ#
R_ITPRDY#
R21
240
ITPRDY#
ITPCLK
RP2
330
R_TCK
R_TMS
R3
R4
47
X2
370-Pin Socket
Part 2
V_CMOS
V1_5
V2_5
VREF0
VREF1
VREF2
VREF3
VREF4
VREF5
VREF6
VREF7
VCC53
VCC54
VCC55
VCC56
VCC57
VCC58
VCC59
VCC60
VCC61
VCC62
VCC63
VCC64
VCC65
VCC66
VCC67
VCC68
VCC69
VCC70
VCC71
VCC72
VCC73
VCC74
VCC75
TDI
TDO
TRST#
TCK
TMS
PREQ#
PRDY#
BP2#
BP3#
BPM0#
BPM1#
RSRVD19
RSRVD20
RSRVD21
RSRVD22
RSRVD23
RSRVD24
RSRVD25
RSRVD26
RSRVD27
RSRVD28
RSRVD29
RSRVD30
RSRVD31
RSRVD32
RSRVD33
RSRVD34
RSRVD35
RSRVD36
RSRVD37
RSRVD38
RSRVD39
PICD0
PICD1
PICCLK
BCLK
PWRGOOD
RESET#
EDGCTRL
CPUPRES#
GND51
GND52
GND53
GND54
GND55
GND56
GND57
GND58
GND59
GND60
GND61
GND62
GND63
GND64
GND65
GND66
GND67
GND68
GND69
GND70
GND71
GND72
GND73
GND74
GND75
GND76
GND77
GND78
GND79
GND80
BNR#
BPRI#
TRDY#
DEFER#
LOCK#
DRDY#
HITM#
HIT#
DBSY#
ADS#
FLUSH#
BSEL#
BR0#
THRMDP
THRMDN
THERMTRIP#
A20M#
STPCLK#
SLP#
SMI#
LINT0/INTR
LINT1/NMI
INIT#
FERR#
IGNNE#
IERR#
PLL1
PLL2
RSRVD40
RSRVD41
RSRVD42
RSRVD43
RSRVD44
RSRVD45
RSRVD46
RSRVD47
RSRVD48
RSRVD49
RSRVD50
RSRVD51
RSRVD52
VCCVID
VCC2_5
GTLREF
JP1
JP1 is a Test Option Only.
R9
220
FREQSEL
HTRDY#
DEFER#
HLOCK#
DRDY#
HITM#
HIT#
DBSY#
HADS#
BR0#
A20M#
STPCLK#
CPUSLP#
SMI#
INTR
NMI
INIT#
FERR#
IGNNE#
PLL1
PLL2
C123
33UF 20%
L22
4.7UH
VCC3_3
R171
220
VCOREDET
SLEWCTRL
RTTCTRL
GTLREF Generation Circuit
R102
75
1%
R101
150
1%
C206
C209
C204
C207
0.1UF
Use 0603 Packages and distribute
within 500 mils of Mendocino
GTLREF Inputs (1 cap for every 2 inputs).
VCMOS Decoupling
Place 0603 Package
Near VCMOS Processor Pin.
C6
0.1UF
APICD0
APICD1
APICCLK_CPU
CPUHCLK
PWRGOOD
CPURST#
R76
51
EDGCTRL
R5
680
Do Not Stuff C114
Place Site w/in 0.5"
of clock pin (W37)
C114
18PF
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD
370-PIN SOCKET, PART 2
REV: 1.3
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
LAST REVISED: 5-26-1999 17:09
PROJECT: INTEL(R) 810 CHIPSET
SHEET: 4 OF 40

GTL Termination



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD GTL TERMINATION		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 5 OF 38

Clock Synthesizer



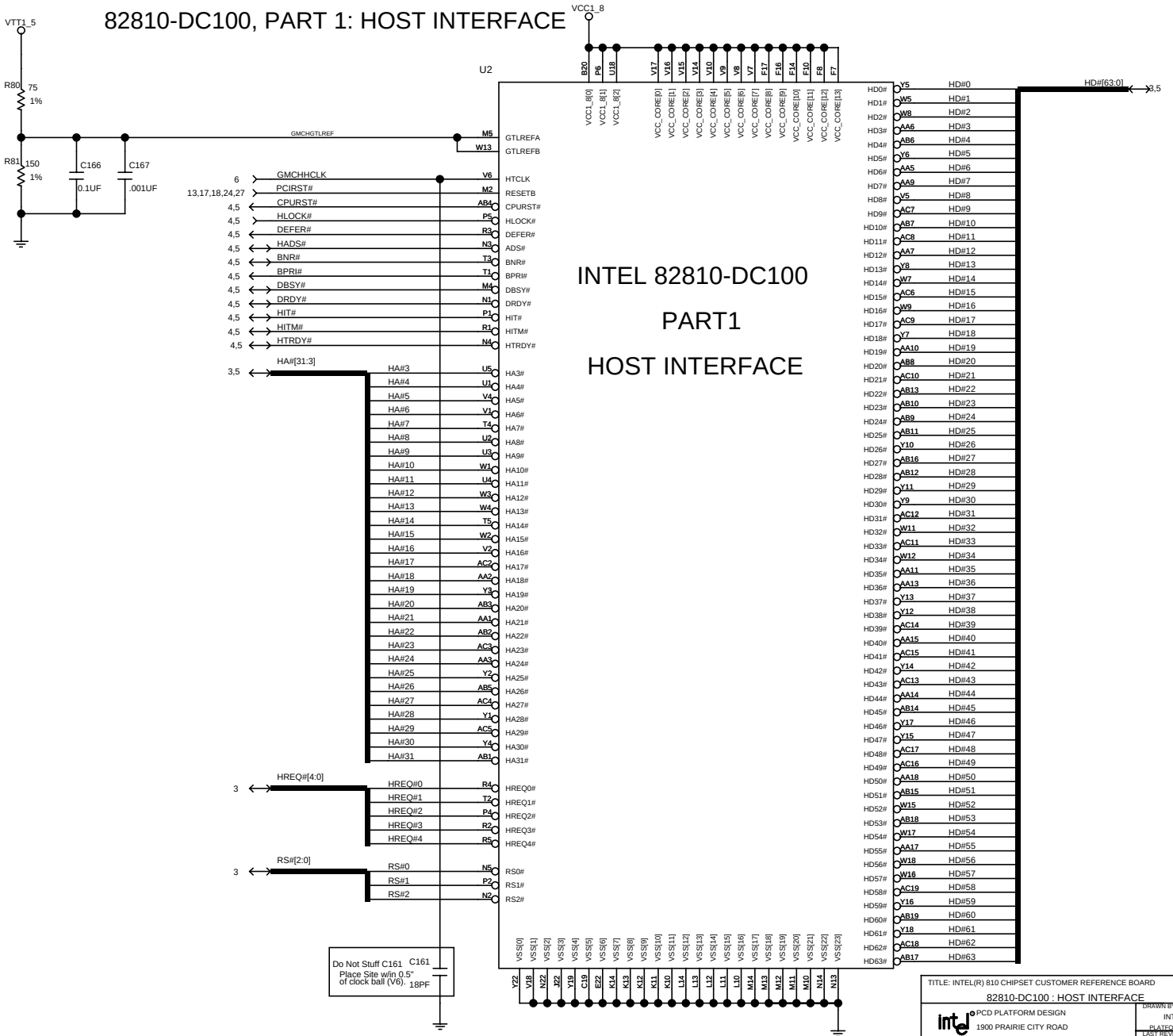
Notes:

- Place all decoupling caps as close to VCC/GND pins as possible
- PCI_0/ICH pin has to go to the ICH.
  (This clock cannot be turned off through SMBus)
- CPU_ITP pin has to go to the ITP. It is the only
  CPU CLK that can be shut off through the SMBUS interface.

APIC Clk Strap	JP6
16MHz	in
33MHz	out*

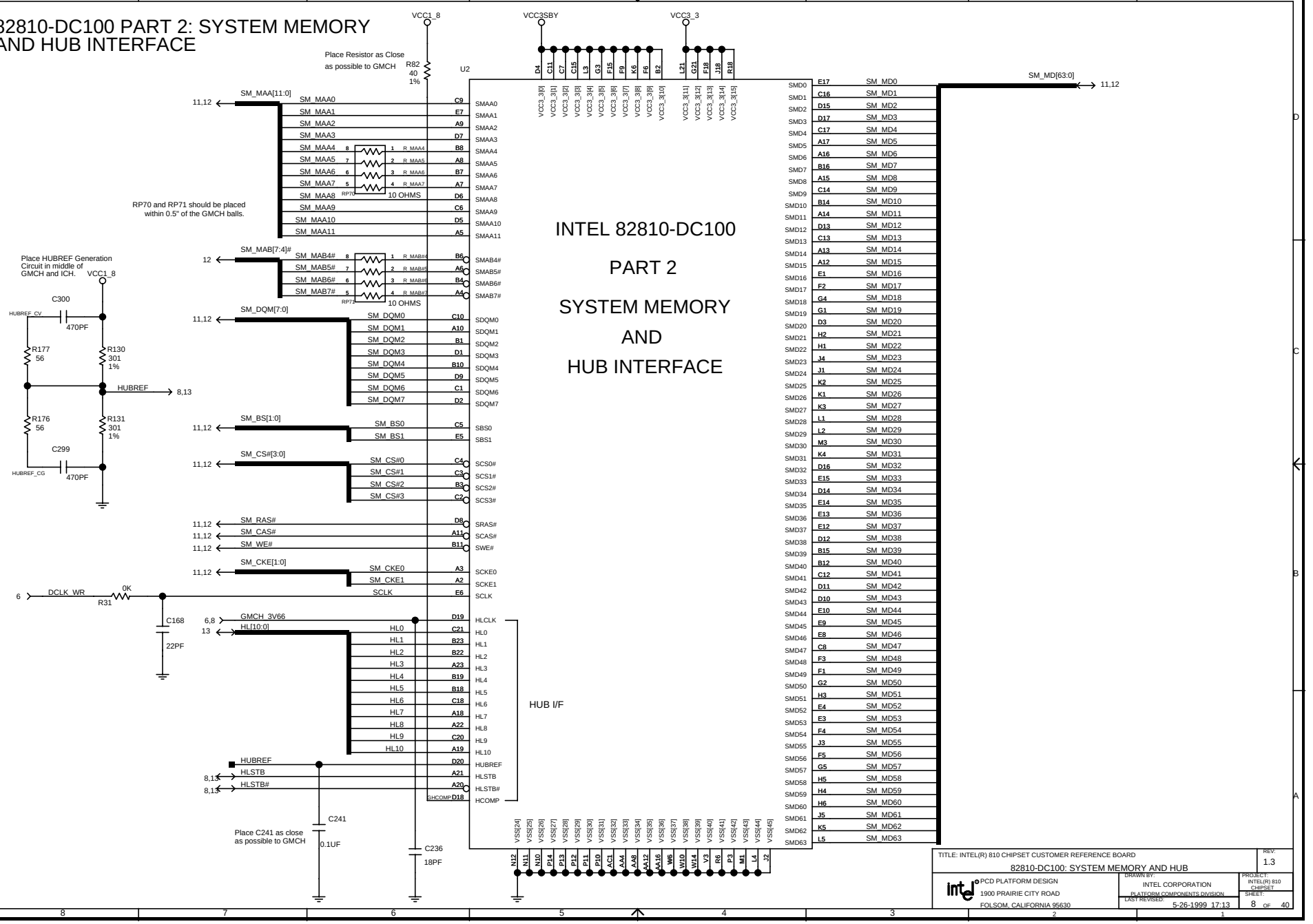
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD CLOCK SYNTHESIZER			REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 12-8-1998 13:05	PROJECT: INTEL(R) 810 CHIPSET SHEET: 6 OF 40	

82810-DC100, PART 1: HOST INTERFACE



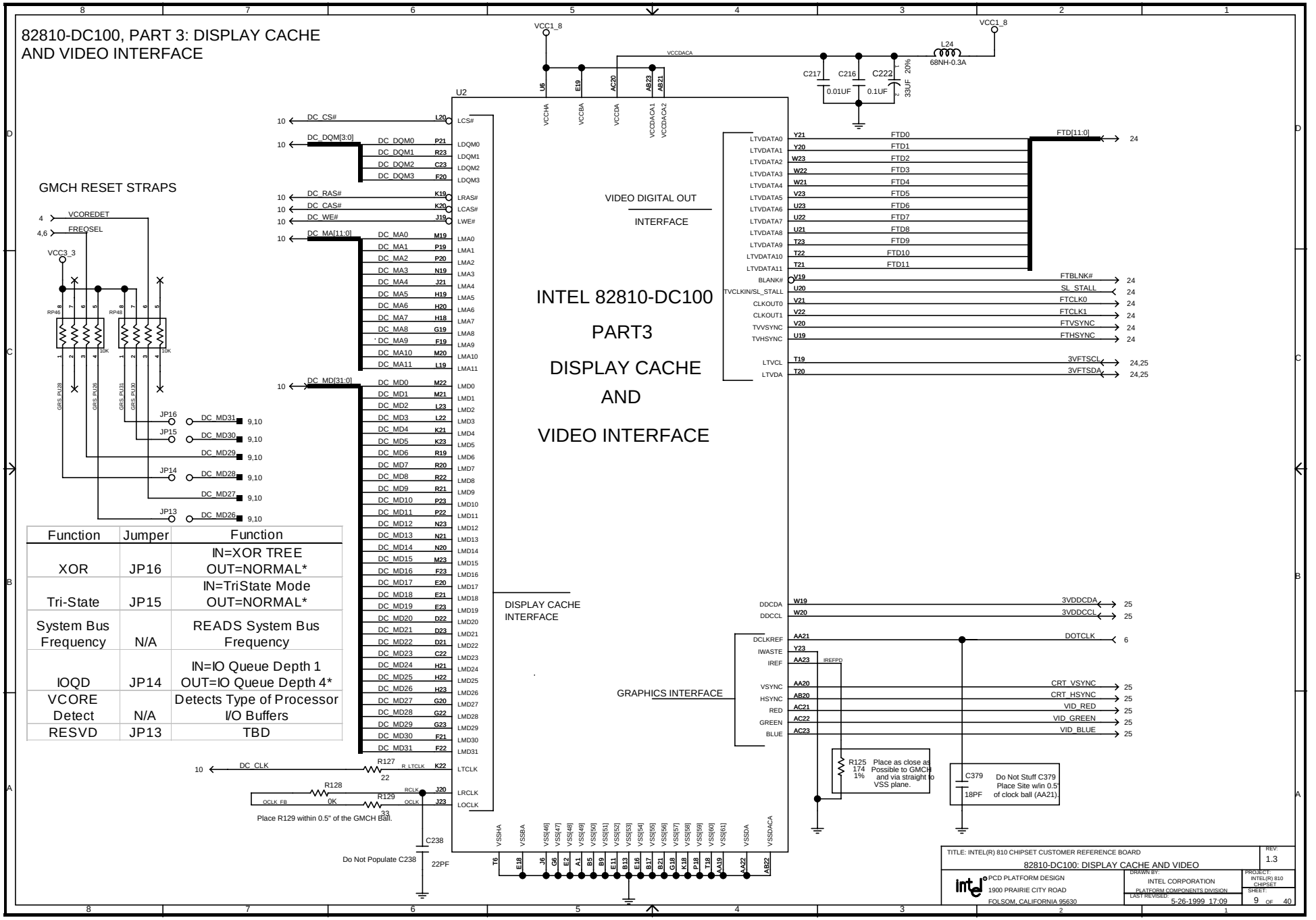
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
82810-DC100 : HOST INTERFACE	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION
LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 7 OF 40

82810-DC100 PART 2: SYSTEM MEMORY AND HUB INTERFACE



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
82810-DC100: SYSTEM MEMORY AND HUB	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION
LAST REVISED: 5-26-1999 17:13	PROJECT: INTEL(R) 810 CHIPSET SHEET: 8 OF 40

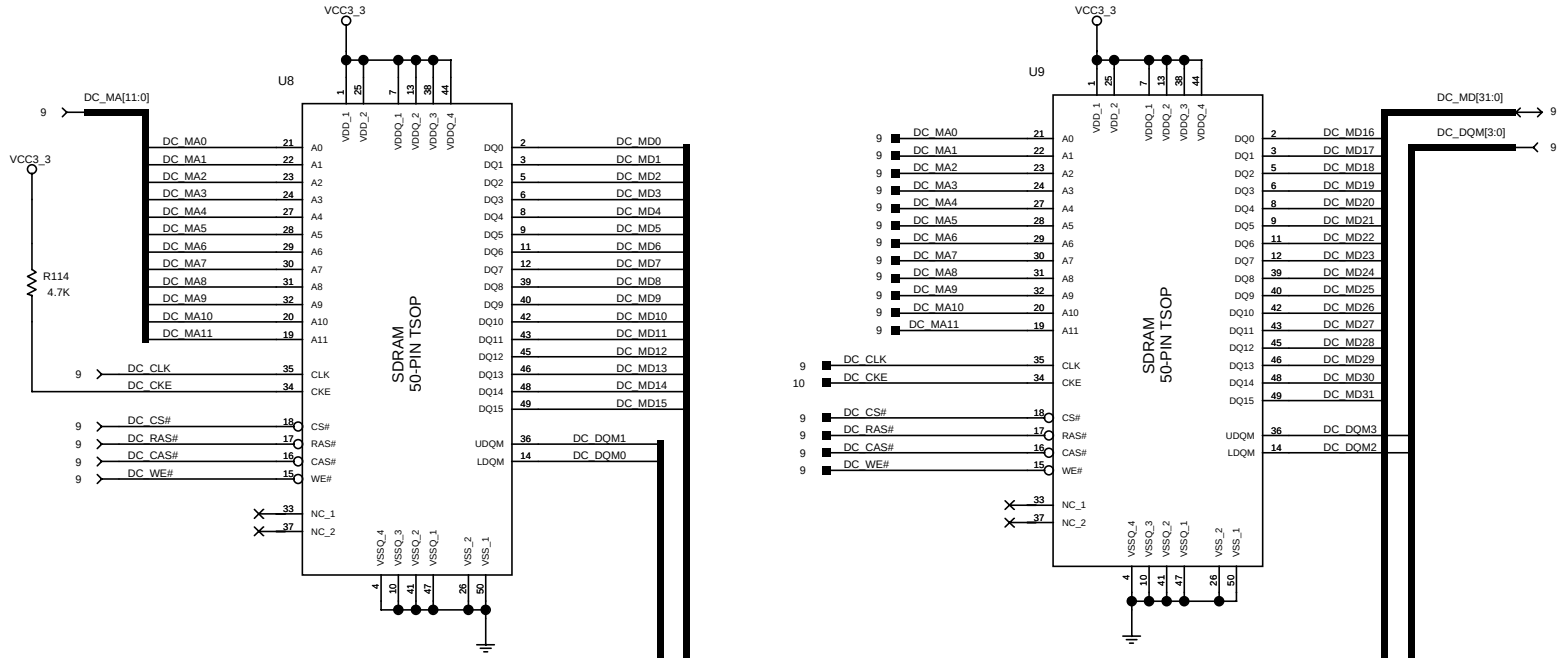
82810-DC100, PART 3: DISPLAY CACHE AND VIDEO INTERFACE



Function	Jumper	Function
XOR	JP16	IN=XOR TREE OUT=NORMAL*
Tri-State	JP15	IN=TriState Mode OUT=NORMAL*
System Bus Frequency	N/A	READS System Bus Frequency
IOQD	JP14	IN=IO Queue Depth 1 OUT=IO Queue Depth 4*
VCORE Detect	N/A	Detects Type of Processor I/O Buffers
RESVD	JP13	TBD

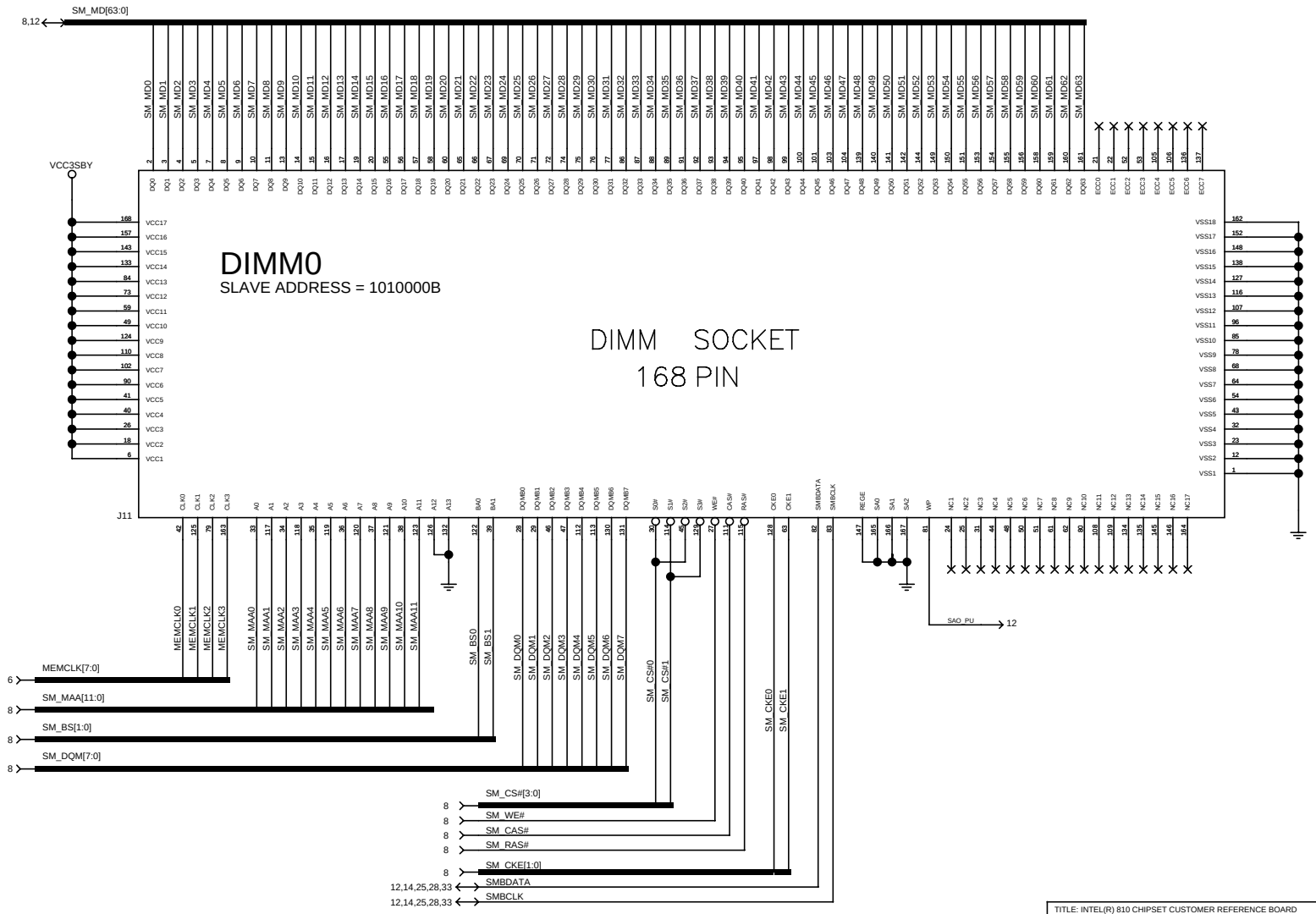
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
82810-DC100: DISPLAY CACHE AND VIDEO	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 5-26-1999 17:09
PROJECT: INTEL(R) 810 CHIPSET	SHEET: 9 OF 40

4MB Display Cache



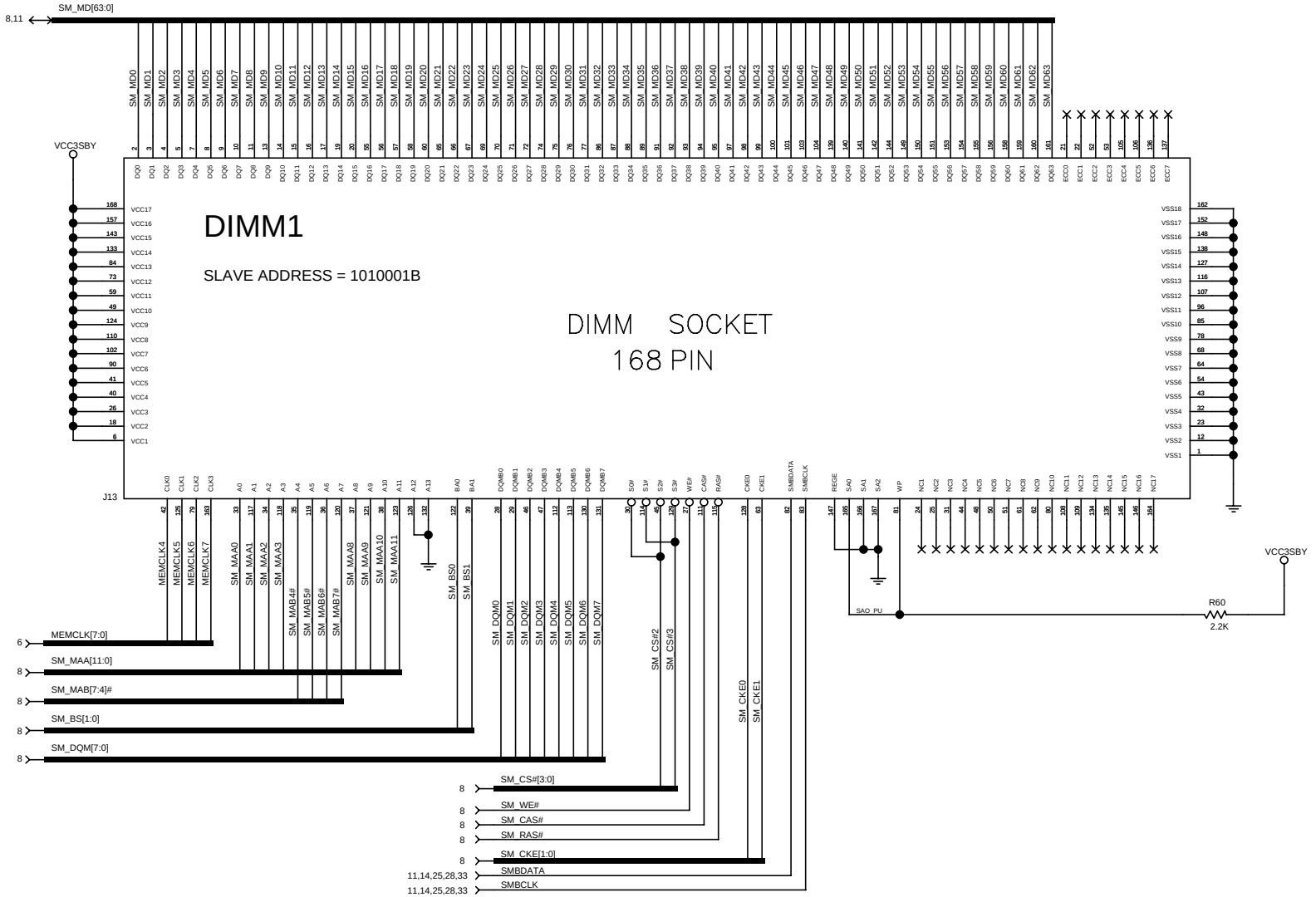
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.3
DISPLAY CACHE		
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 10 OF 40

SYSTEM MEMORY



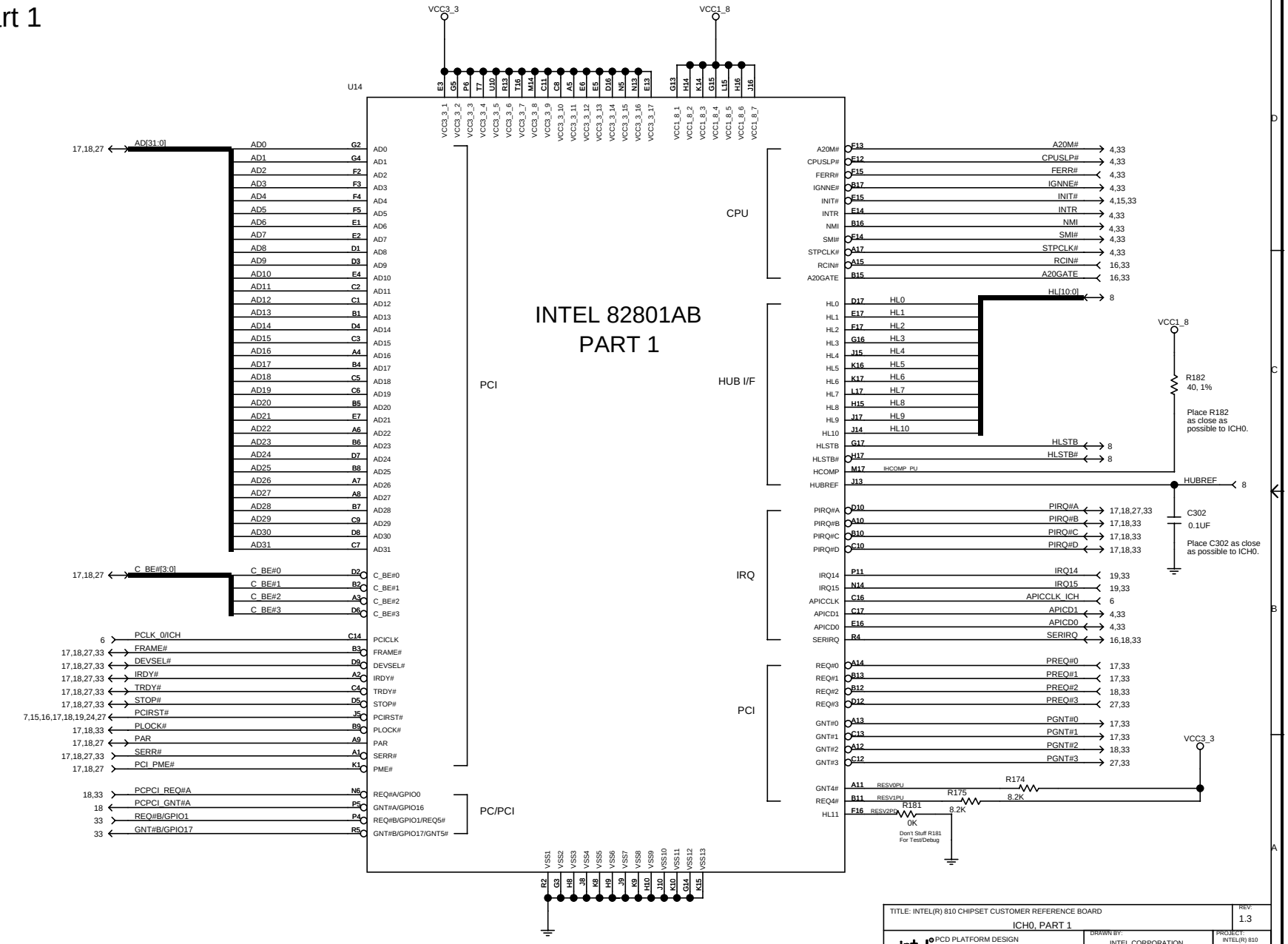
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
SYSTEM MEMORY: DIMM0	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 12-8-1998 13:14
PROJECT: INTEL(R) 810 CHIPSET	SHEET: 11 OF 40

SYSTEM MEMORY

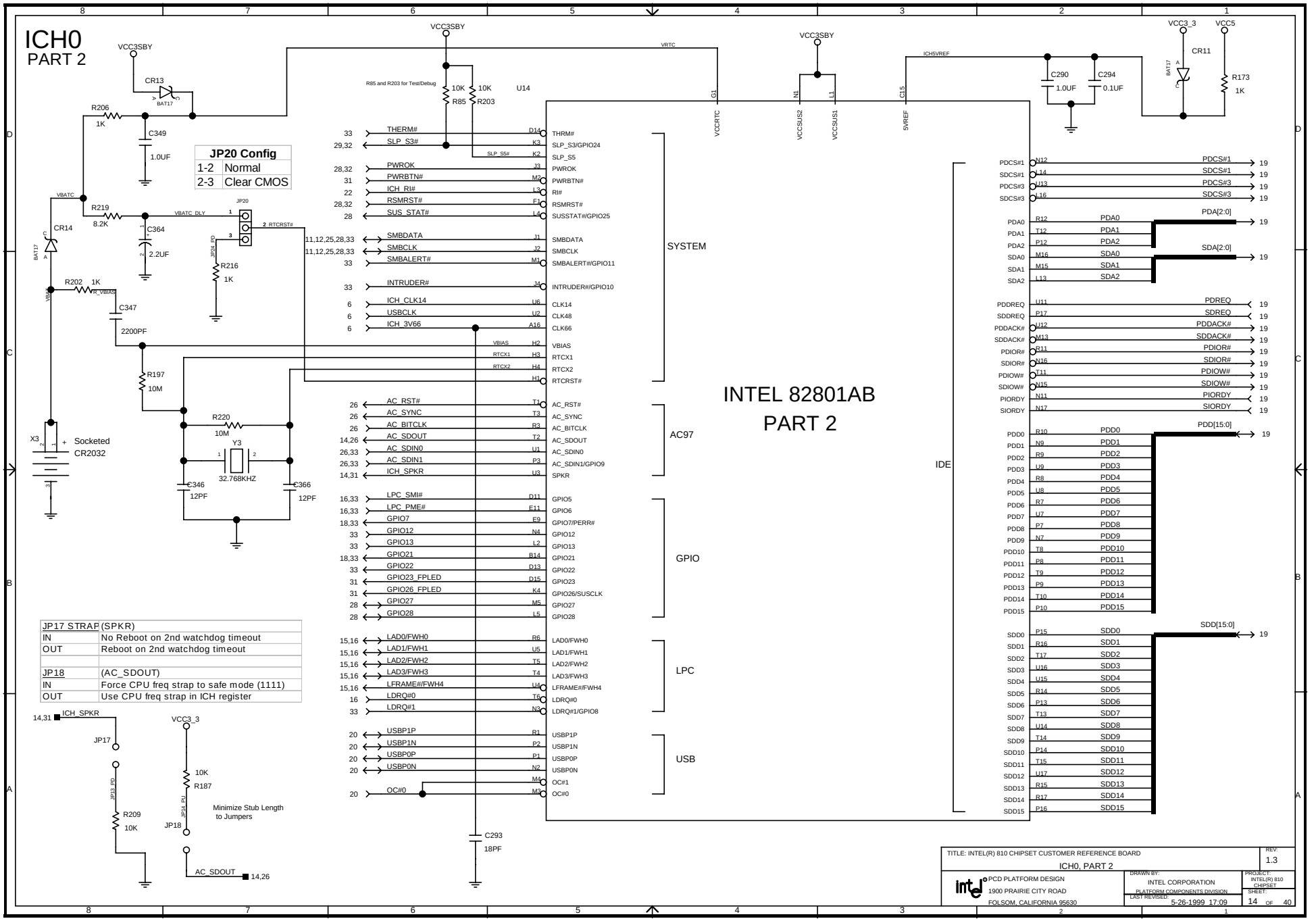


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD SYSTEM MEMORY: DIMM1		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 12-8-1998 13:14	PROJECT: INTEL(R) 810 CHIPSET SHEET: 12 OF 40

ICH0, Part 1

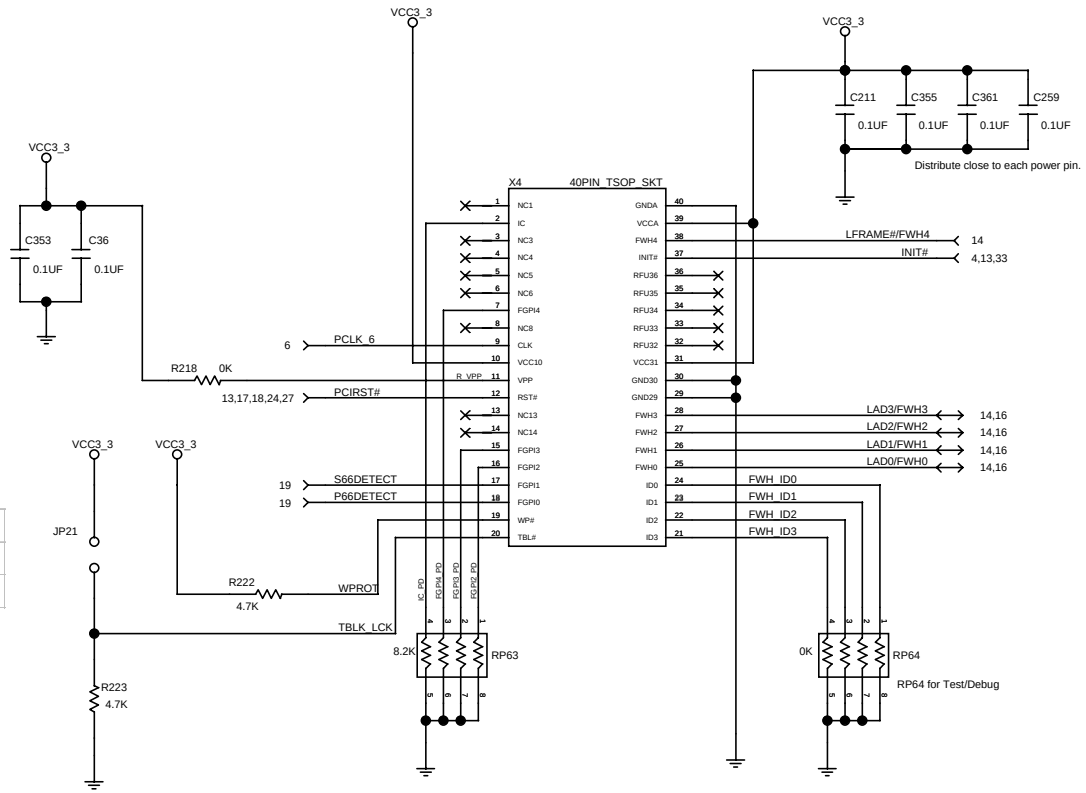


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
ICH0, PART 1	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 2-22-1999 10:37
PROJECT: INTEL(R) 810 CHIPSET SHEET: 13 OF 40	


ICH0
PART 2
INTEL 82801AB
PART 2
JP20 Config
1-2 Normal
2-3 Clear CMOS
JP17 STRAP (SPKR)
IN No Reboot on 2nd watchdog timeout
OUT Reboot on 2nd watchdog timeout
JP18 (AC_SDOUT)
IN Force CPU freq strap to safe mode (1111)
OUT Use CPU freq strap in ICH register
Minimize Stub Length to Jumpers
SYSTEM
AC97
GPIO
LPC
USB
IDE
THERM#
SLP_S3#
SLP_S5#
PWROK
PWRBTN#
ICH_RI#
RSMRST#
SUS_STAT#
SMBDATA
SMBCLK
SMBALERT#
INTRUDER#
ICH_CLK14
USBCLK
ICH_3V66
RTCRST#
AC_RST#
AC_SYNC
AC_BITCLK
AC_SDOUT
AC_SDIN0
AC_SDIN1
ICH_SPKR
LPC_SMI#
LPC_PME#
GPIO7
GPIO12
GPIO13
GPIO21
GPIO22
GPIO23_FPLED
GPIO26_FPLED
GPIO27
GPIO28
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LFRAME#/FWH4
LDRQ#0
LDRQ#1
USBP1P
USBP1N
USBP0P
USBP0N
OC#0
PDCS#1
SDCS#1
PDCS#3
SDCS#3
PDA[2:0]
SDA[2:0]
PDDREQ
SDDREQ
PDDACK#
SDDACK#
PDIOR#
SDIOR#
PDIOW#
SDIOW#
PIORDY
SIORDY
PDD[15:0]
SDD[15:0]
Socketed CR2032
32.768KHZ
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD
ICH0, PART 2
REV: 1.3
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY: INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
LAST REVISED: 5-26-1999 17:09
PROJECT: INTEL(R) 810 CHIPSET
SHEET: 14 OF 40

FirmWare Hub (FWH) Socket

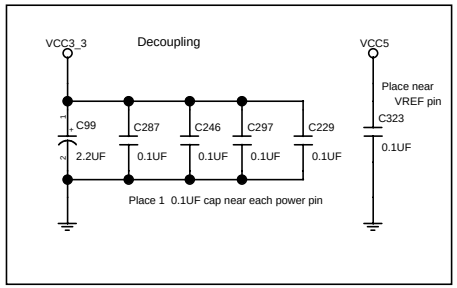
NOTE: This is a Socketed Implementation

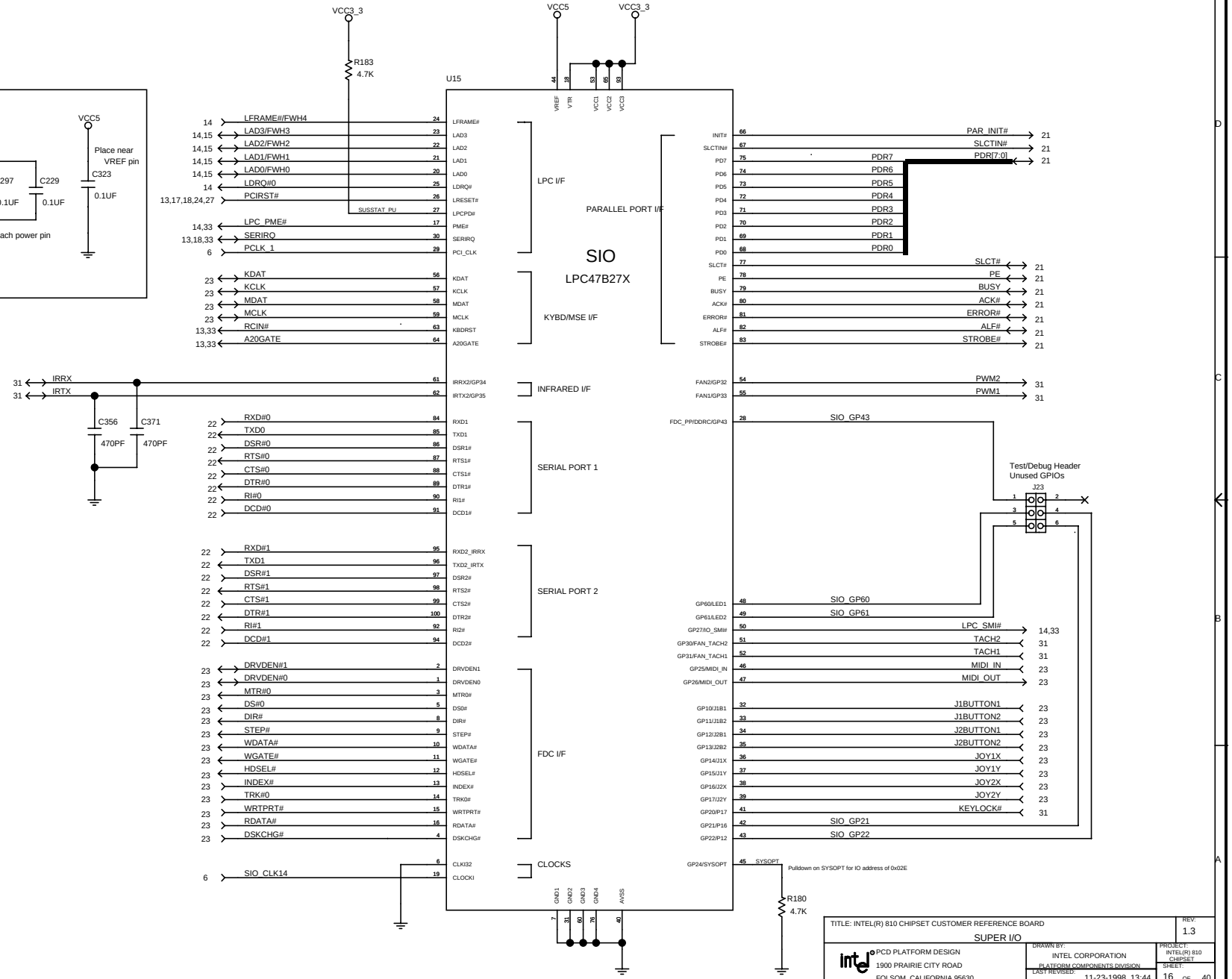


JP21 CONFIG		
IN	Unlocked	
OUT	Locked	Default

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD FIRMWARE HUB (FWH)		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 2-22-1999 10:37	PROJECT: INTEL(R) 810 CHIPSET SHEET: 15 OF 40

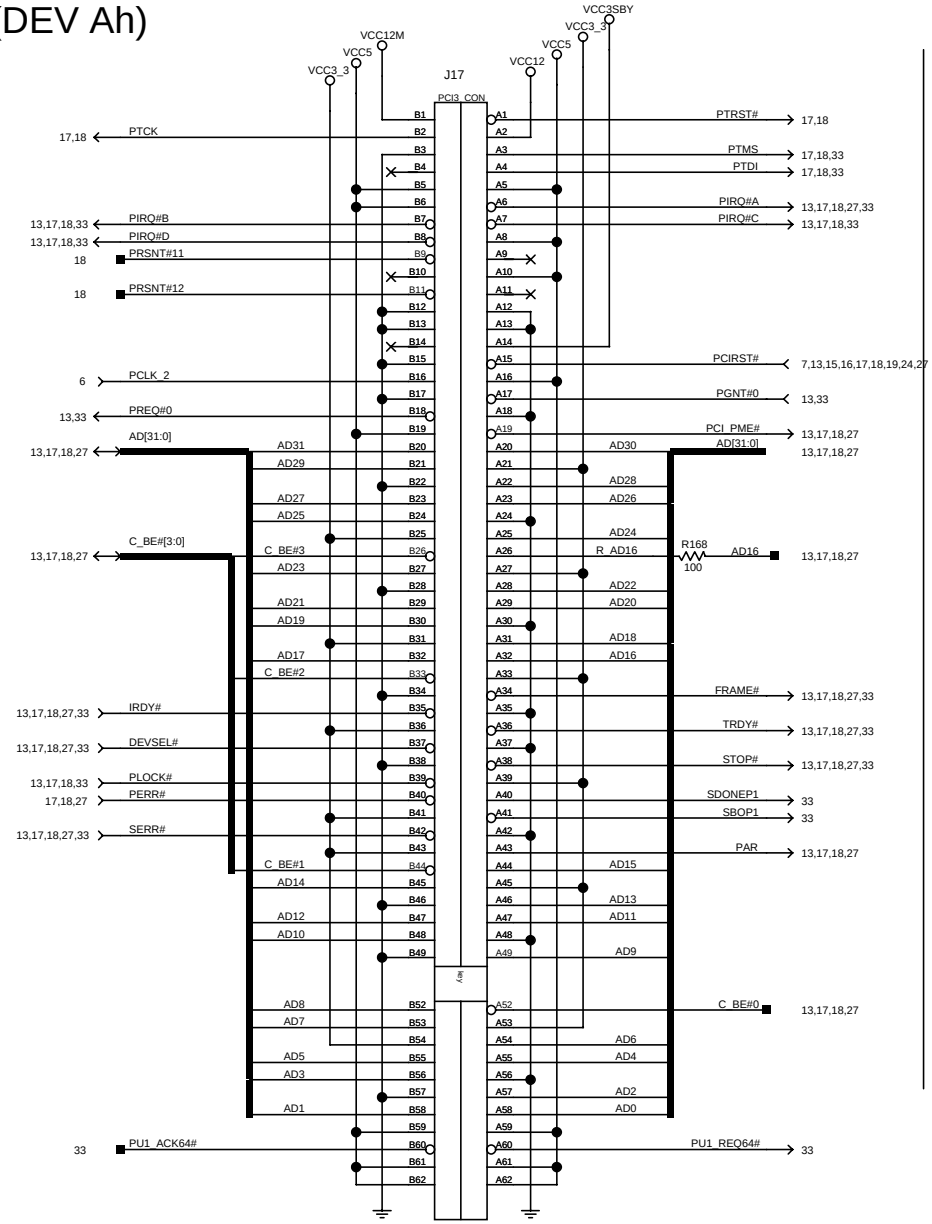
Super I/O



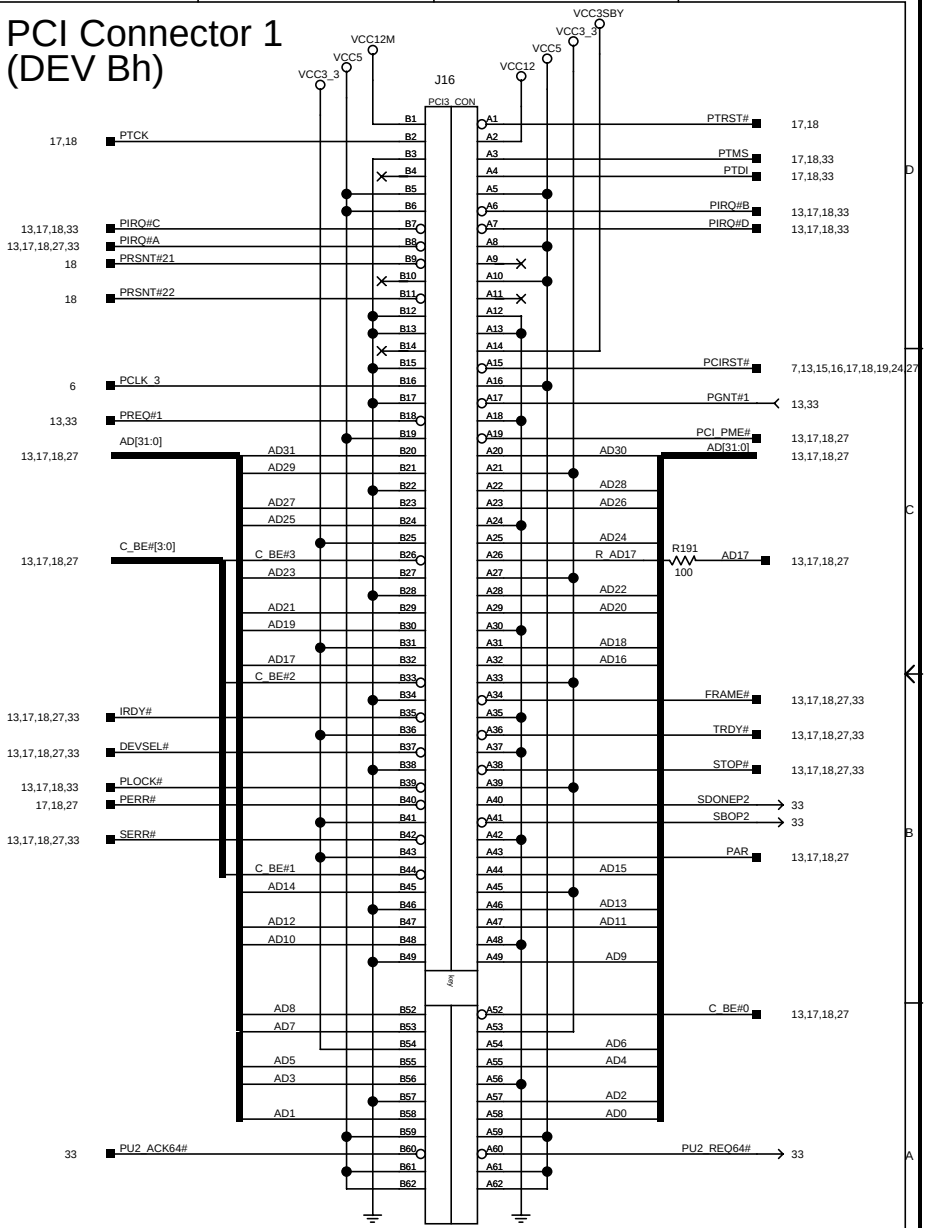


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
SUPER I/O	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION
LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 16 OF 40

PCI Connector 0 (DEV Ah)



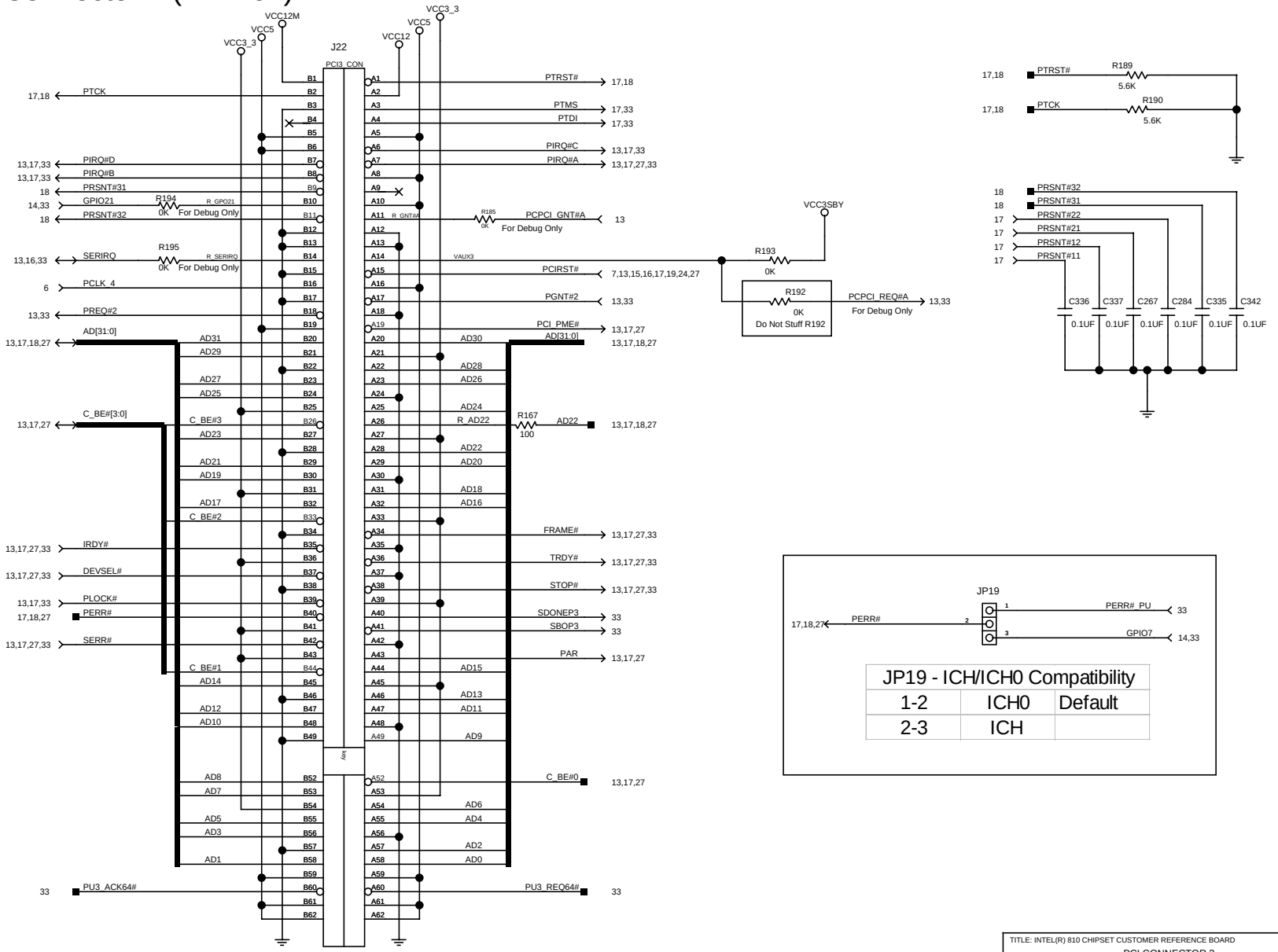
PCI Connector 1 (DEV Bh)



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD PCI CONNECTORS 1 AND 2		REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 17 OF 40

PCI Connector 2 (DEV 6h)

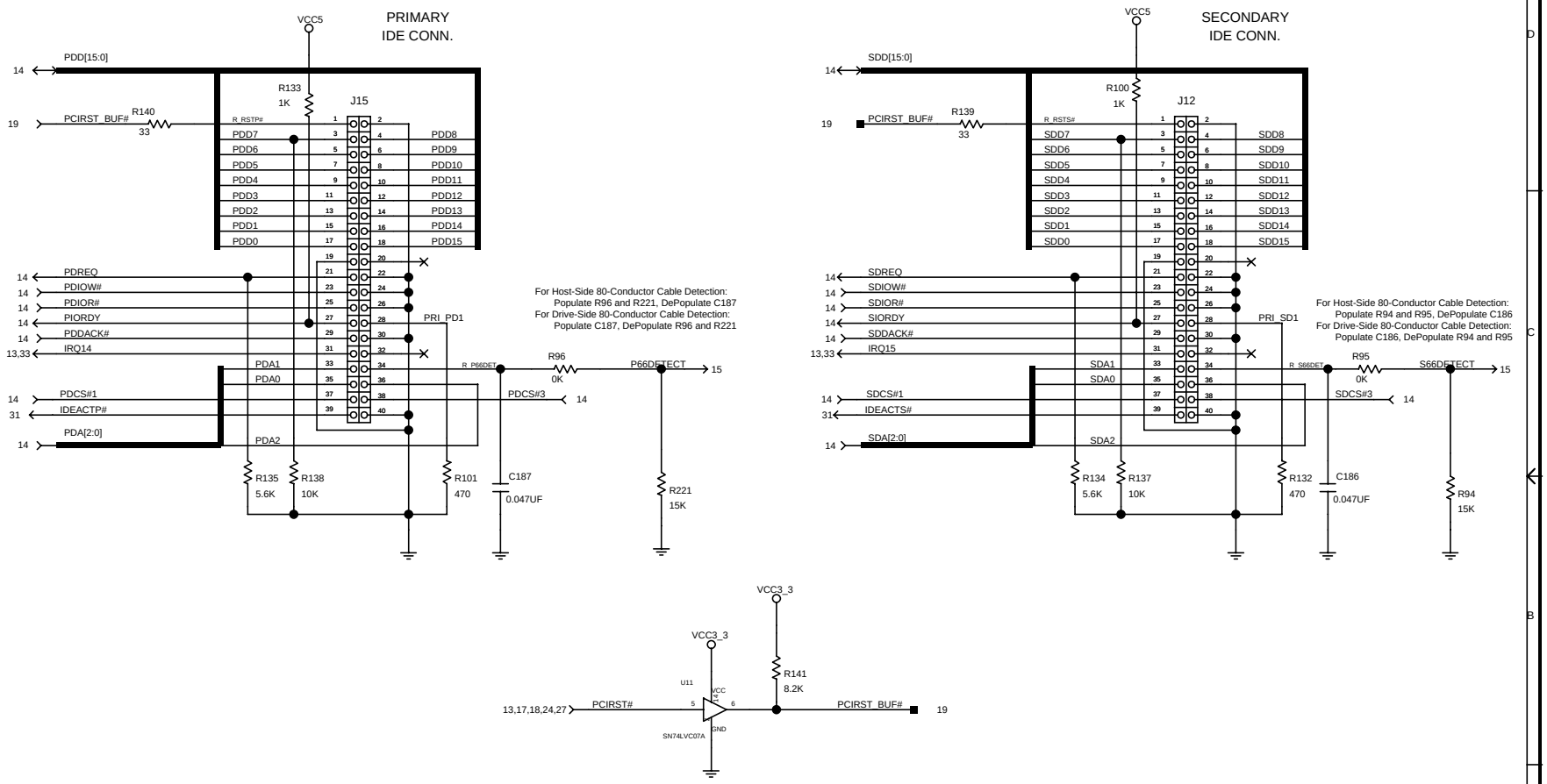
Layout Note: Should be in Slot 0 Position (Outside Edge of Board Furthest from CPU)



JP19 - ICH/ICH0 Compatibility		
1-2	ICH0	Default
2-3	ICH	

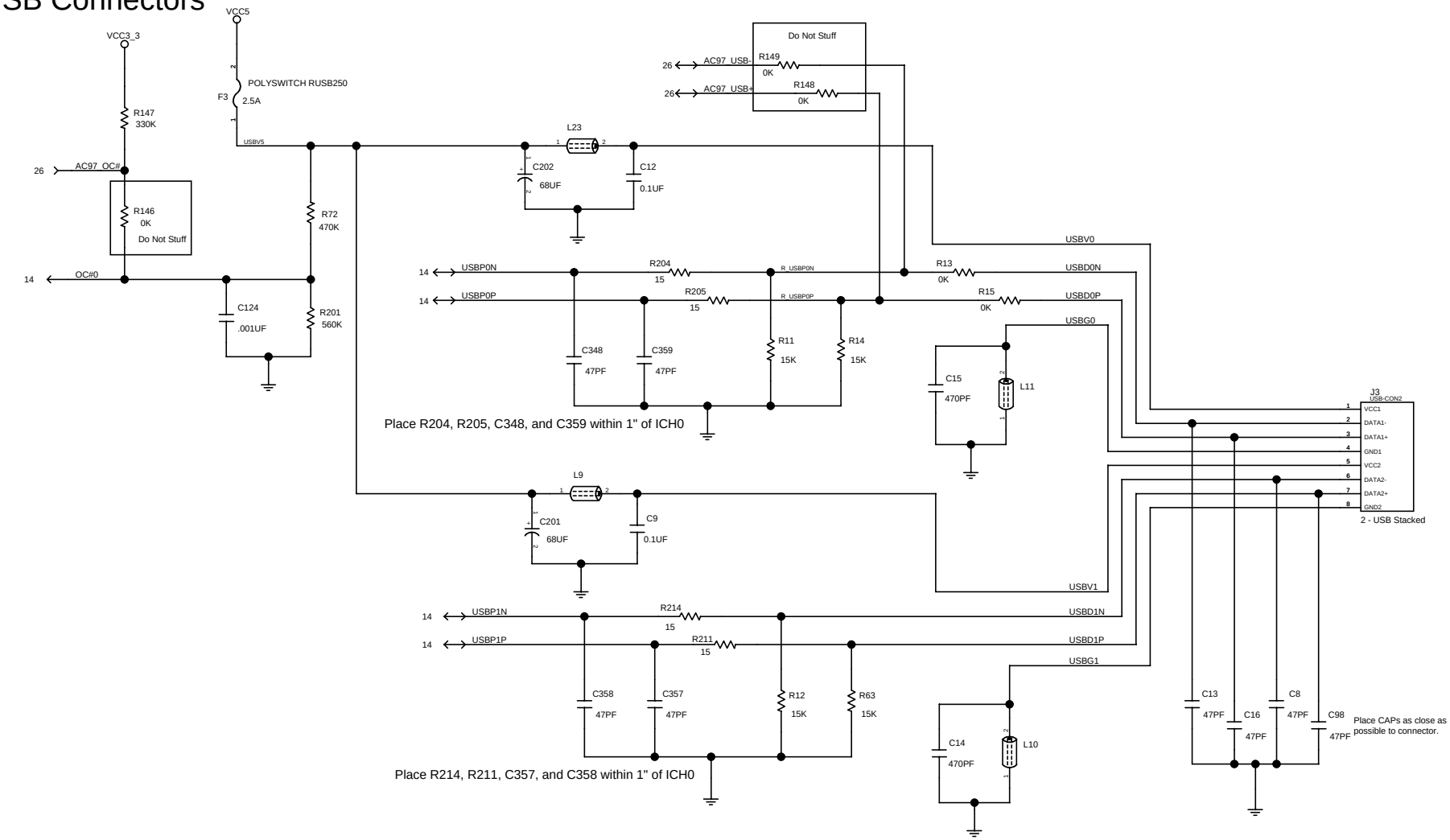
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD PCI CONNECTOR 3		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 18 OF 40

ULTRAATA/33 IDE CONNECTORS



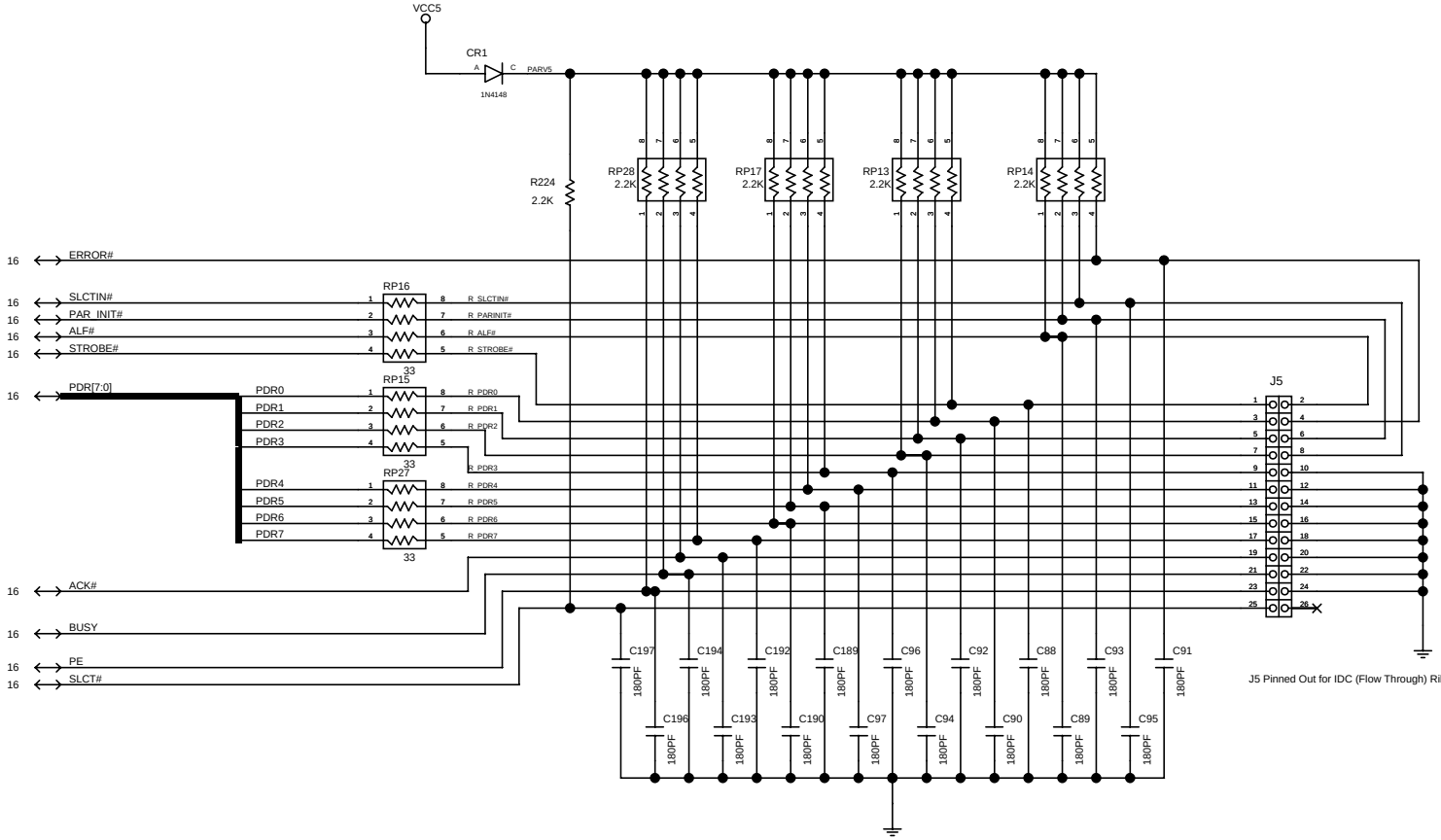
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD ULTRAATA/33 CONNECTORS		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 2-22-1999 10:37	PROJECT: INTEL(R) 810 CHIPSET SHEET: 19 OF 40

USB Connectors



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD USB CONNECTORS		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 20 OF 40

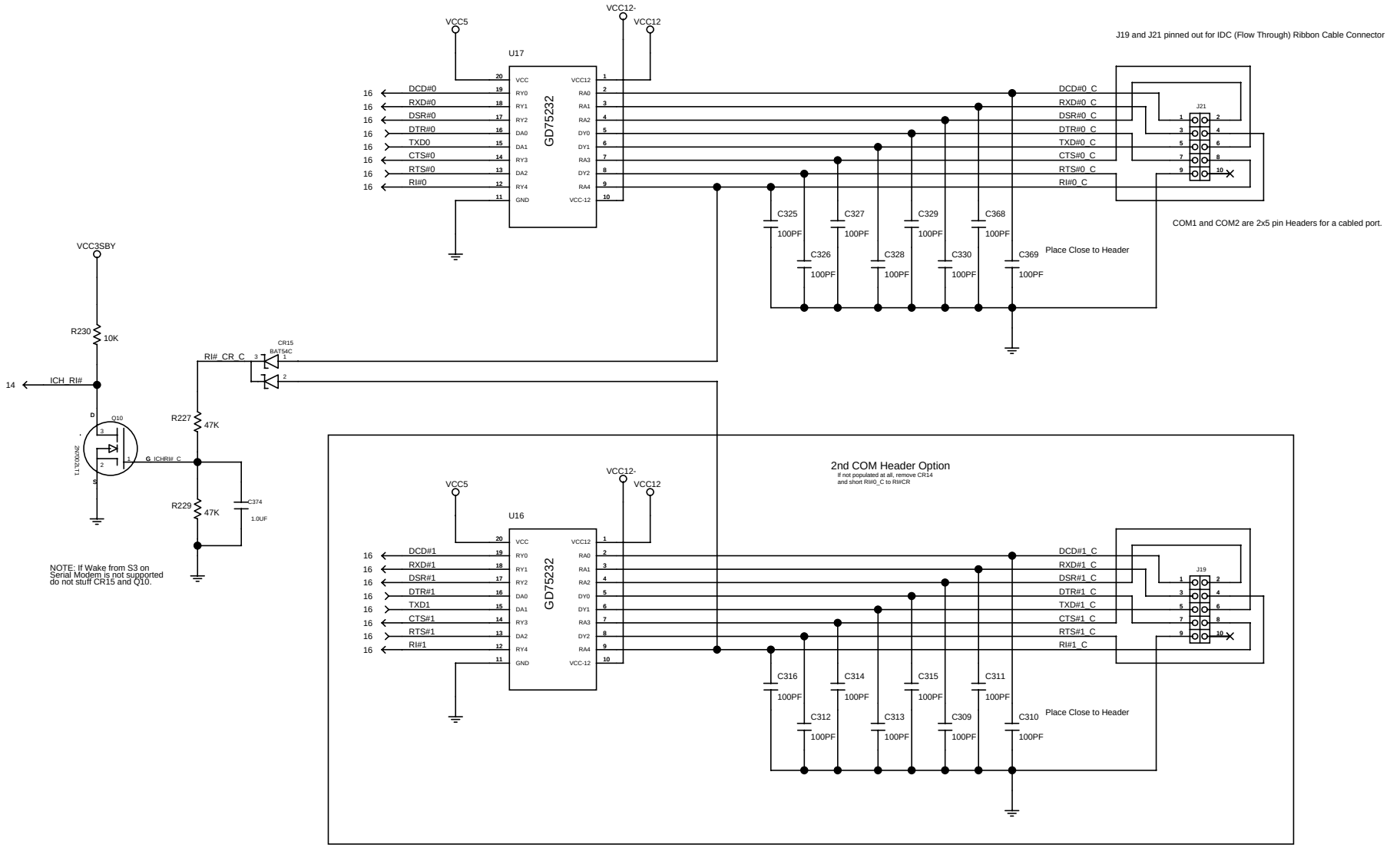
Parallel Port Header



J5 Pinned Out for IDC (Flow Through) Ribbon Cable Connector

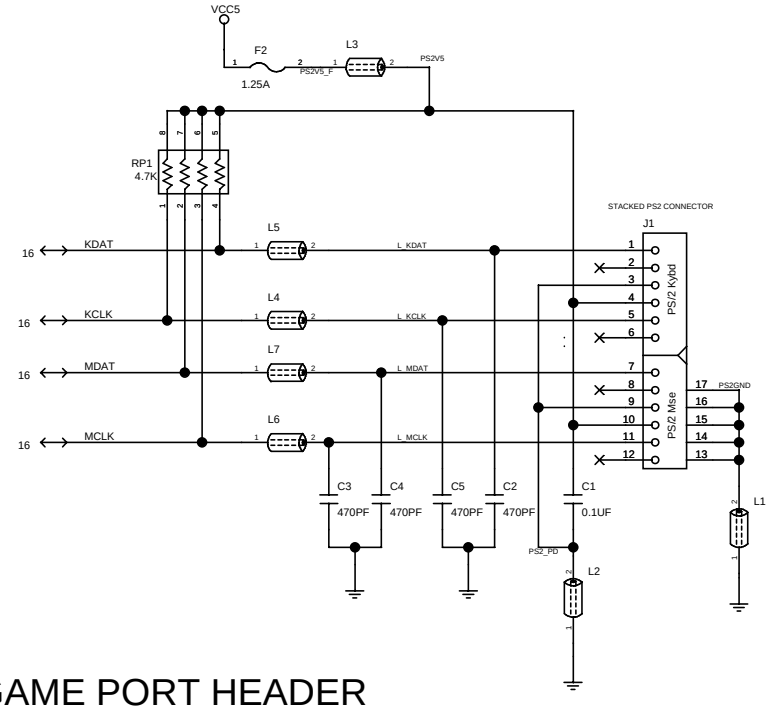
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD PARALLEL PORT		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 2-22-1999 11:02	PROJECT: INTEL(R) 810 CHIPSET SHEET: 21 OF 40

Serial Port/COM Headers

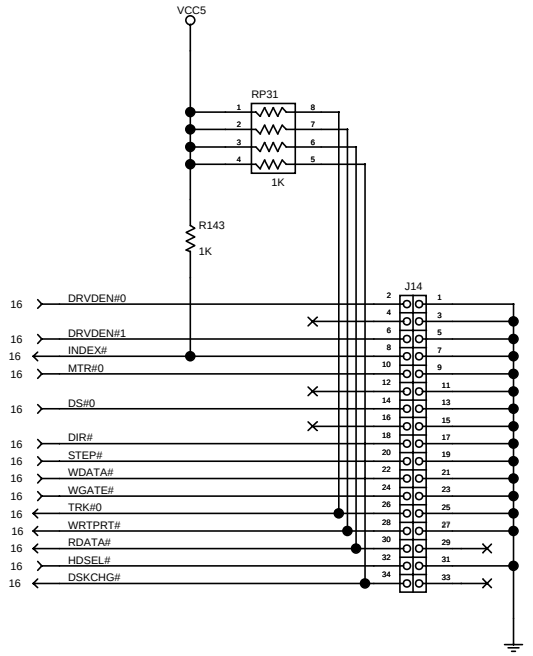


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD SERIAL AND GAME PORTS	REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION
LAST REVISED: 2-22-1999 11:02	PROJECT: INTEL(R) 810 CHIPSET SHEET: 22 OF 40

KEYBOARD/MOUSE PORTS

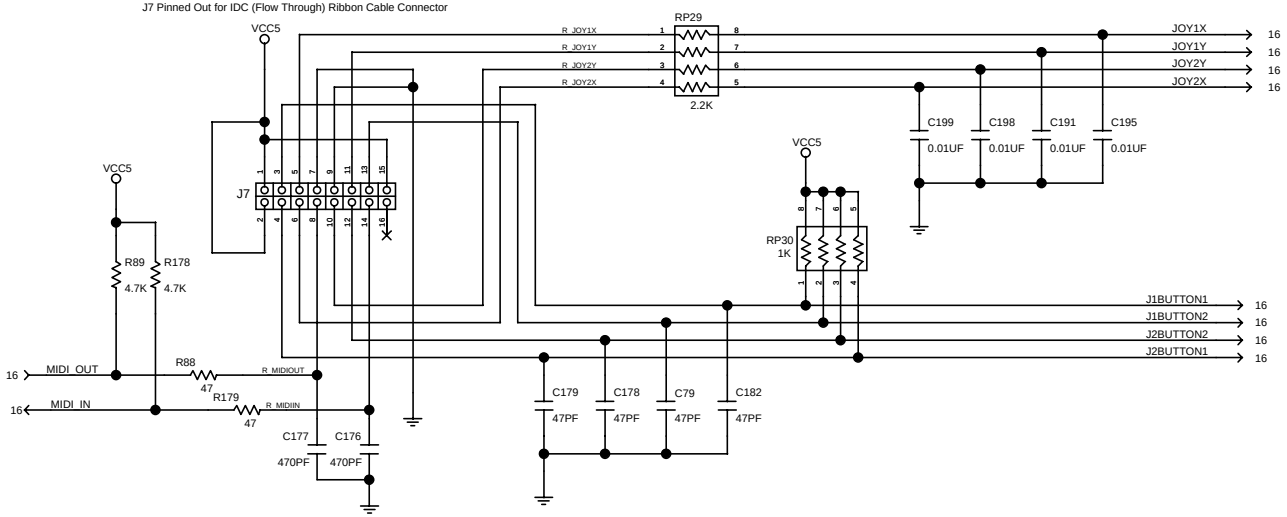


FLOPPY DISK HEADER



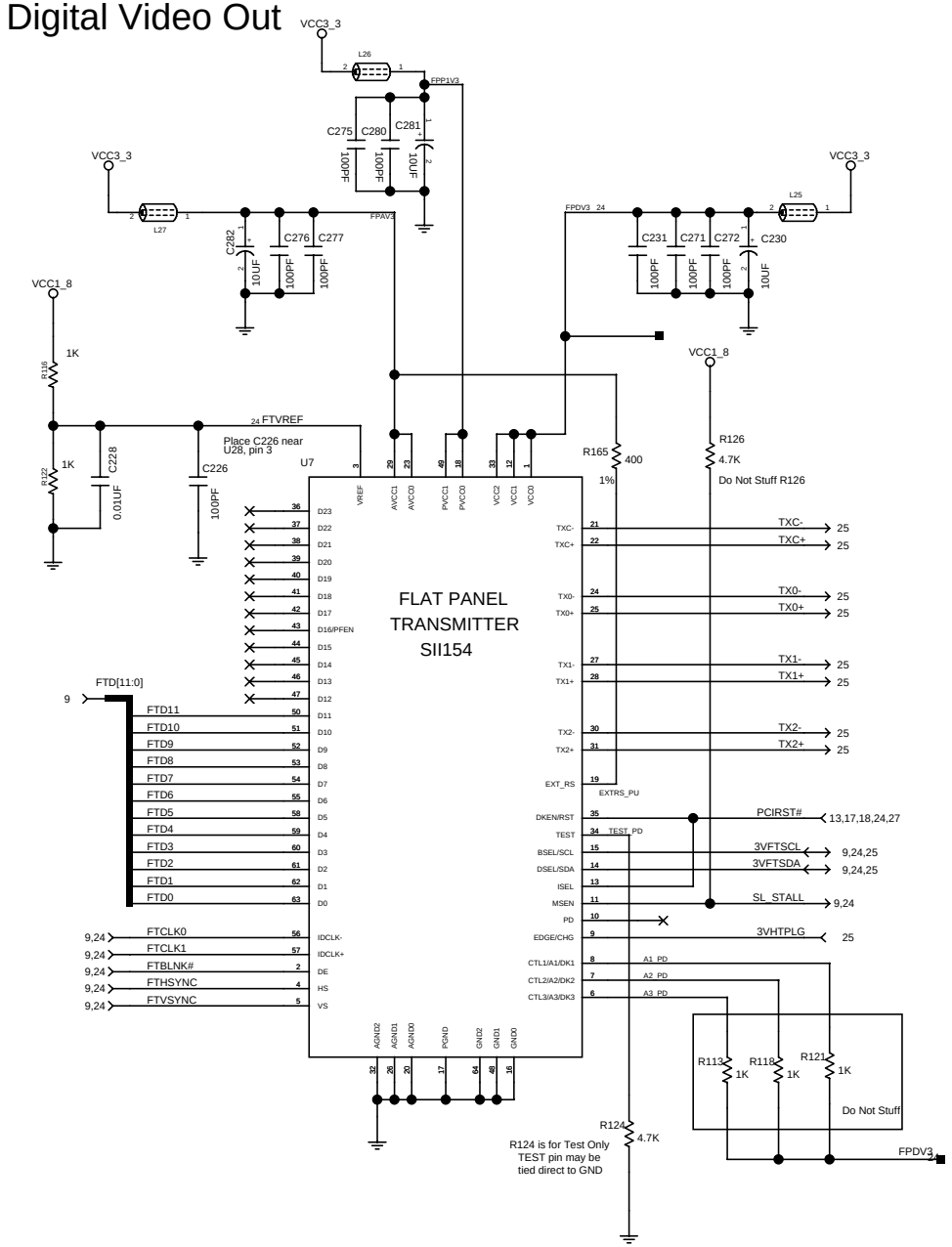
GAME PORT HEADER

J7 Pinned Out for IDC (Flow Through) Ribbon Cable Connector



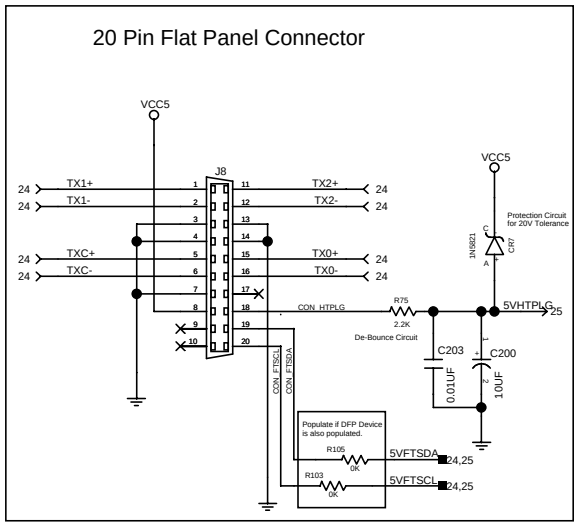
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD KEYBOARD/MOUSE/FLOPPYGAME PORTS	REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION
LAST REVISED: 2-22-1999 11:02	PROJECT: INTEL(R) 810 CHIPSET SHEET: 23 OF 40

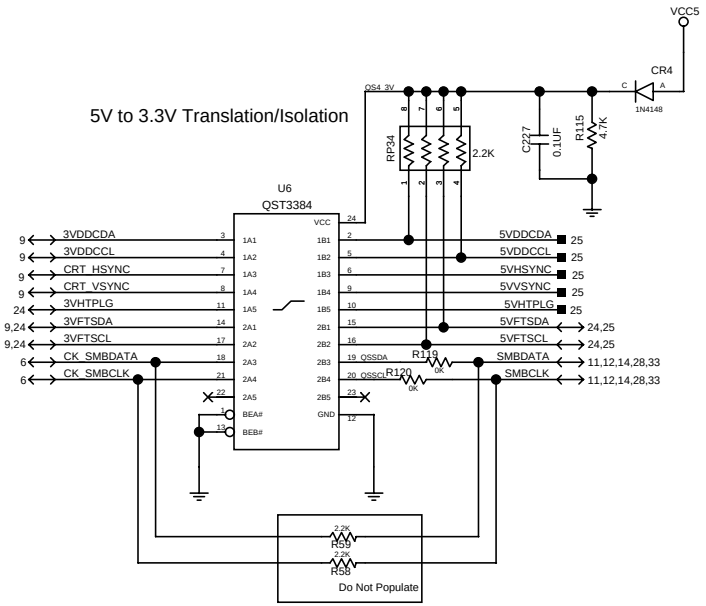
Digital Video Out

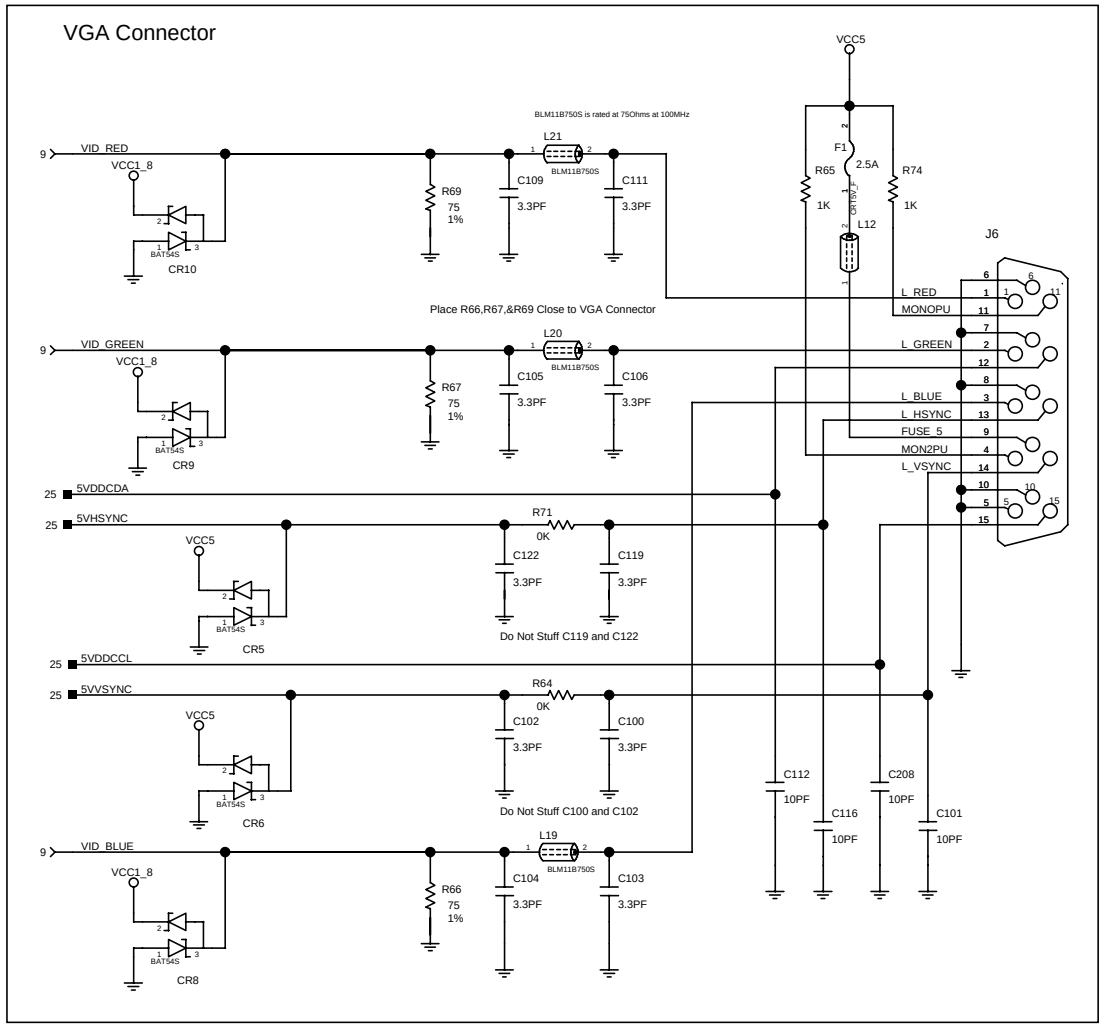


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD DIGITAL VIDEO OUT		REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 5-26-1999 17:13	PROJECT: INTEL(R) 810 CHIPSET SHEET: 24 OF 40

Video Connectors

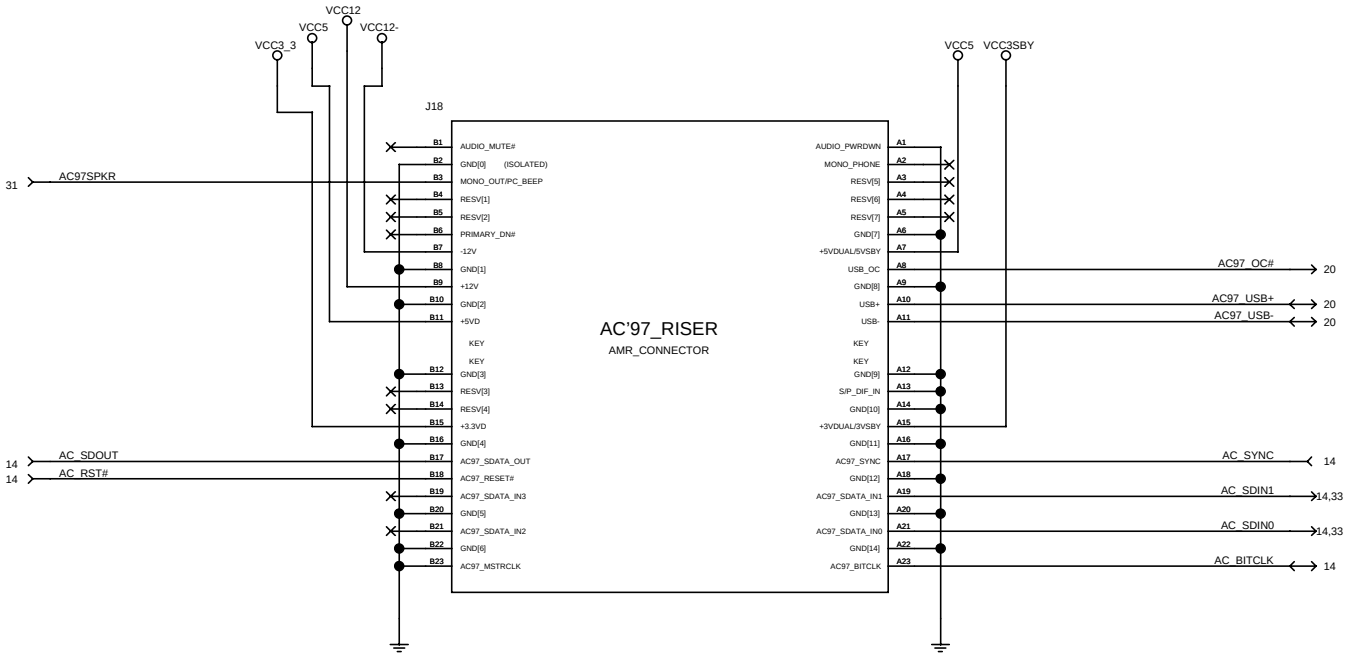




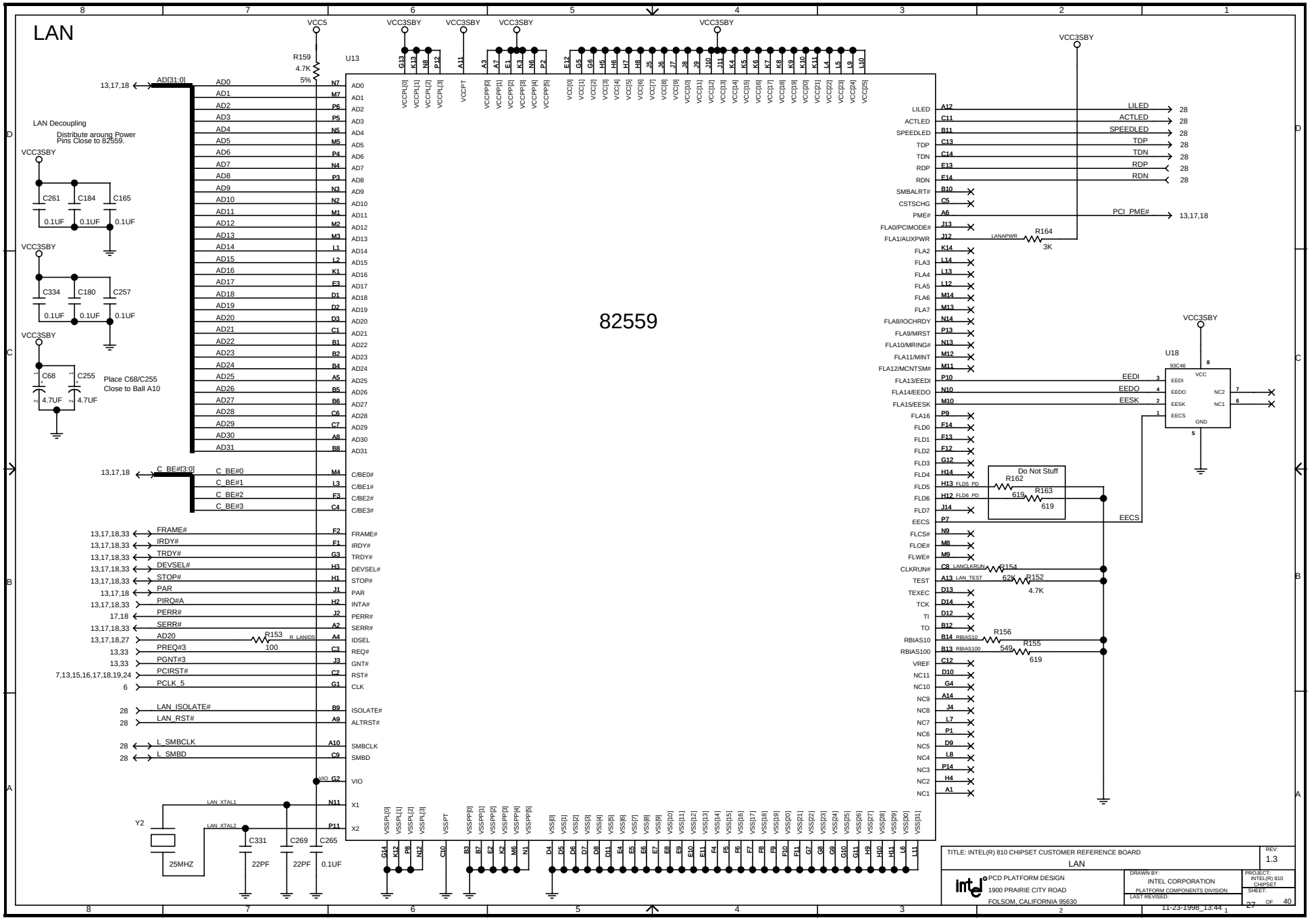


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD VIDEO CONNECTORS		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 25 OF 40

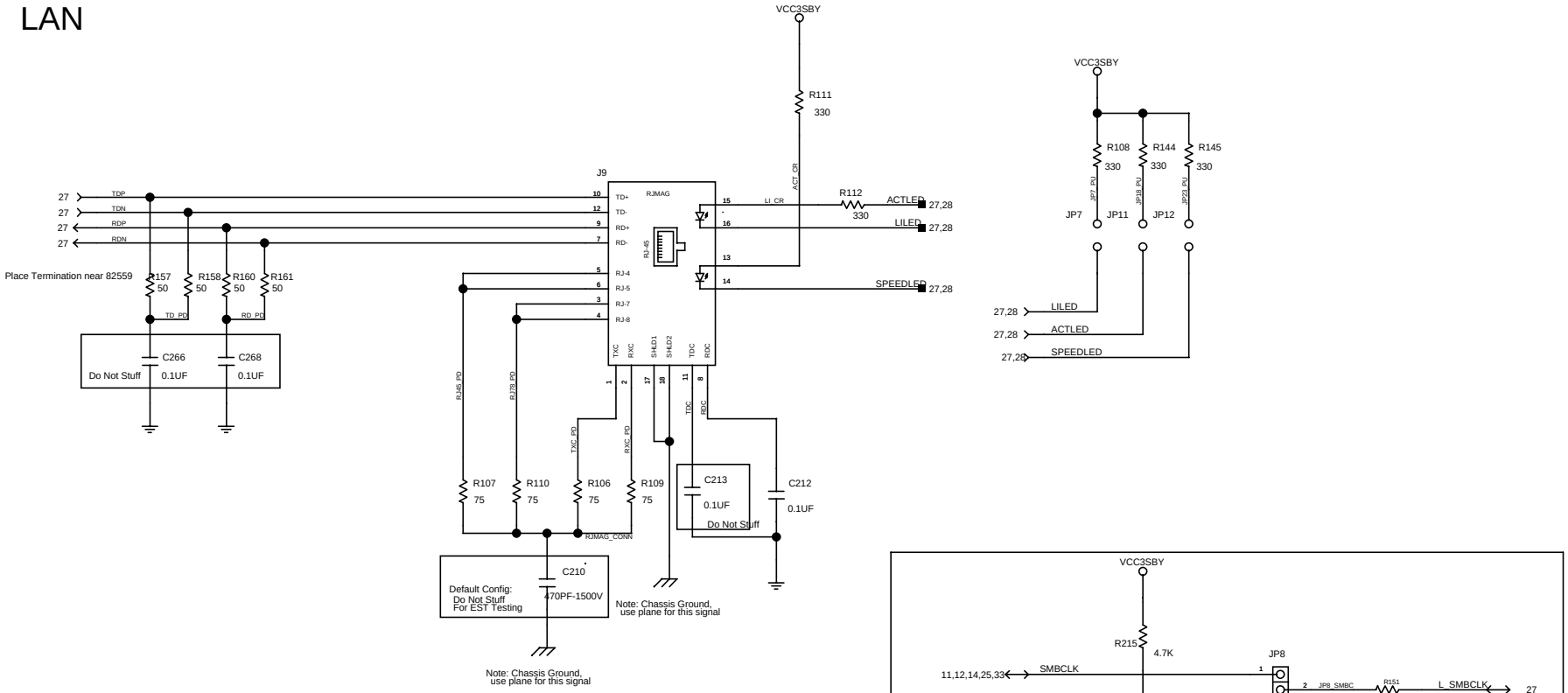
AUDIO/MODEM RISER

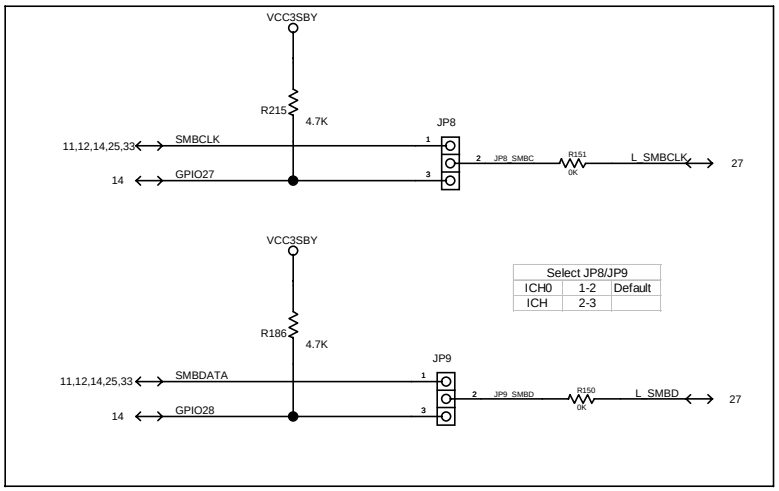


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD AUDIO/MODEM RISER		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 26 OF 40

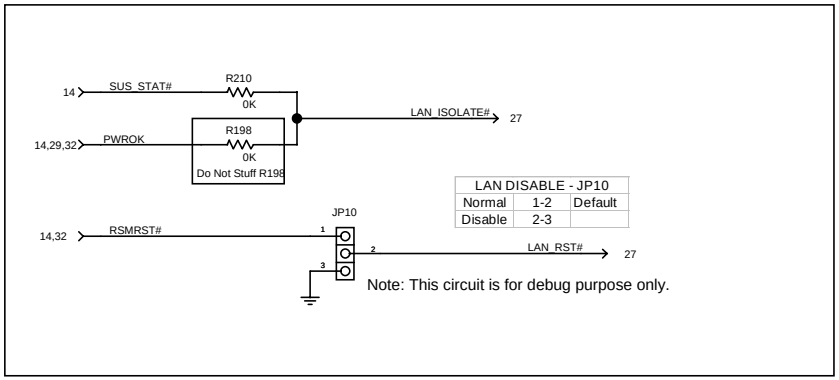

LAN
82559
U13
U18
93C46
VCC5
VCC3SBY
R159
4.7K
5%
LAN Decoupling
Distribute aroung Power
Pins Close to 82559.
C261
C184
C165
C334
C180
C257
0.1UF
C68
C255
4.7UF
Place C68/C255
Close to Ball A10
AD[31:0]
C_BE#[3:0]
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
PIRQ#A
PERR#
SERR#
AD20
R153
100
R_LANIDS
PREQ#3
PGNT#3
PCIRST#
PCLK_5
LAN_ISOLATE#
LAN_RST#
L_SMBCLK
L_SMBD
VIO
LAN_XTAL1
LAN_XTAL2
Y2
25MHZ
C331
22PF
C269
22PF
C265
0.1UF
LILED
ACTLED
SPEEDLED
TDP
TDN
RDP
RDN
SMBALRT#
CSTSCHG
PME#
PCI_PME#
FLA0/PCIMODE#
FLA1/AUXPWR
LANAPWR
R164
3K
EEDI
EEDO
EESK
EECS
Do Not Stuff
R162
619
R163
619
CLKRUN#
LANCLKRUN
R154
62K
TEST
LAN_TEST
R152
4.7K
RBIAS10
RBIAS100
R156
549
R155
619
VREF
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD
LAN
REV: 1.3
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
PROJECT: INTEL(R) 810 CHIPSET
LAST REVISED:
11-23-1998 13:44
SHEET: 27 OF 40

LAN





Select JP8/JP9		
ICH0	1-2	Default
ICH	2-3	



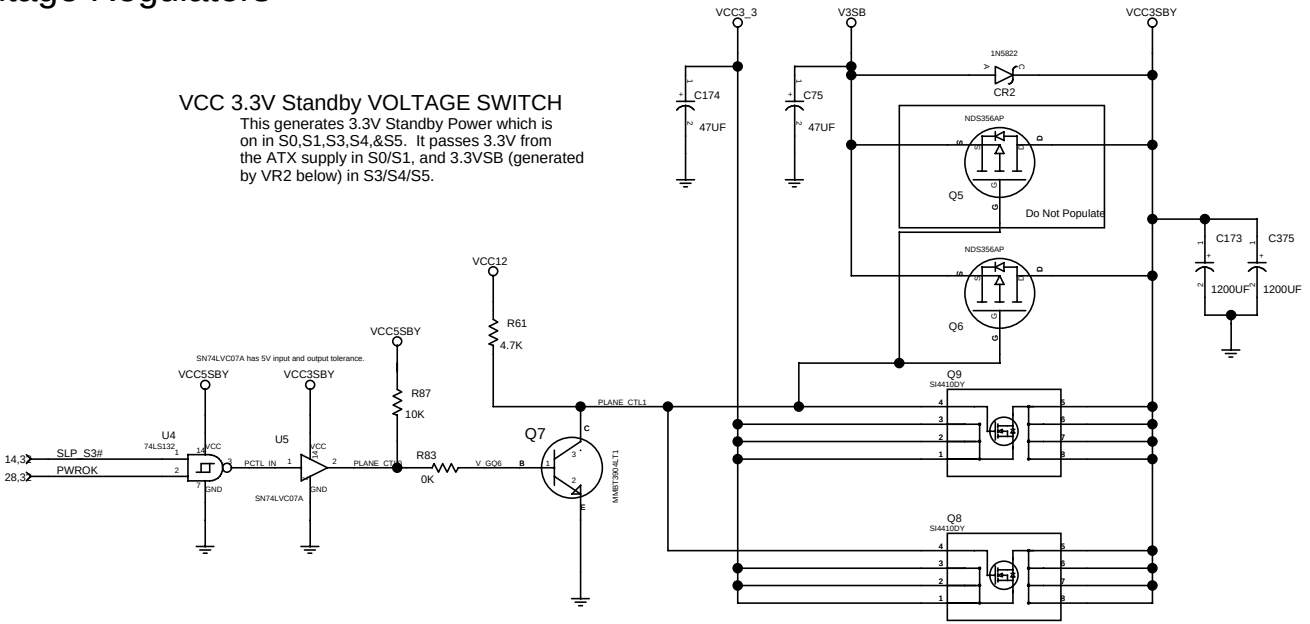
LAN DISABLE - JP10		
Normal	1-2	Default
Disable	2-3	

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD LAN		REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 28 OF 40

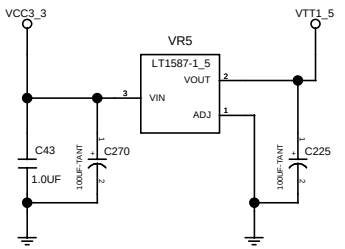
Voltage Regulators

VCC 3.3V Standby VOLTAGE SWITCH

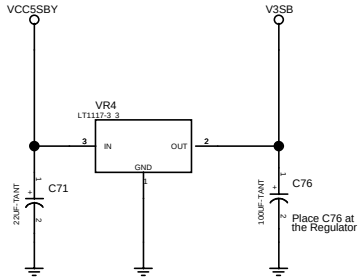
This generates 3.3V Standby Power which is on in S0,S1,S3,S4,&S5. It passes 3.3V from the ATX supply in S0/S1, and 3.3VSB (generated by VR2 below) in S3/S4/S5.



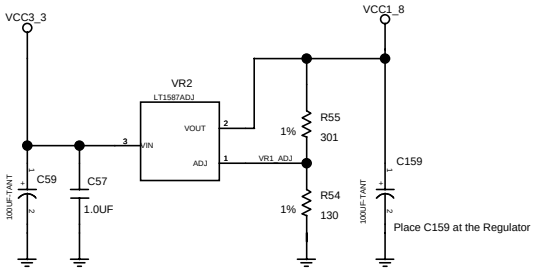
VTT 1.5V VOLTAGE REGULATOR



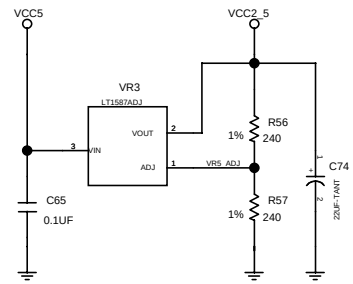
VCC 3.3VSB Regulator



VCC 1.8 VOLTAGE REGULATOR

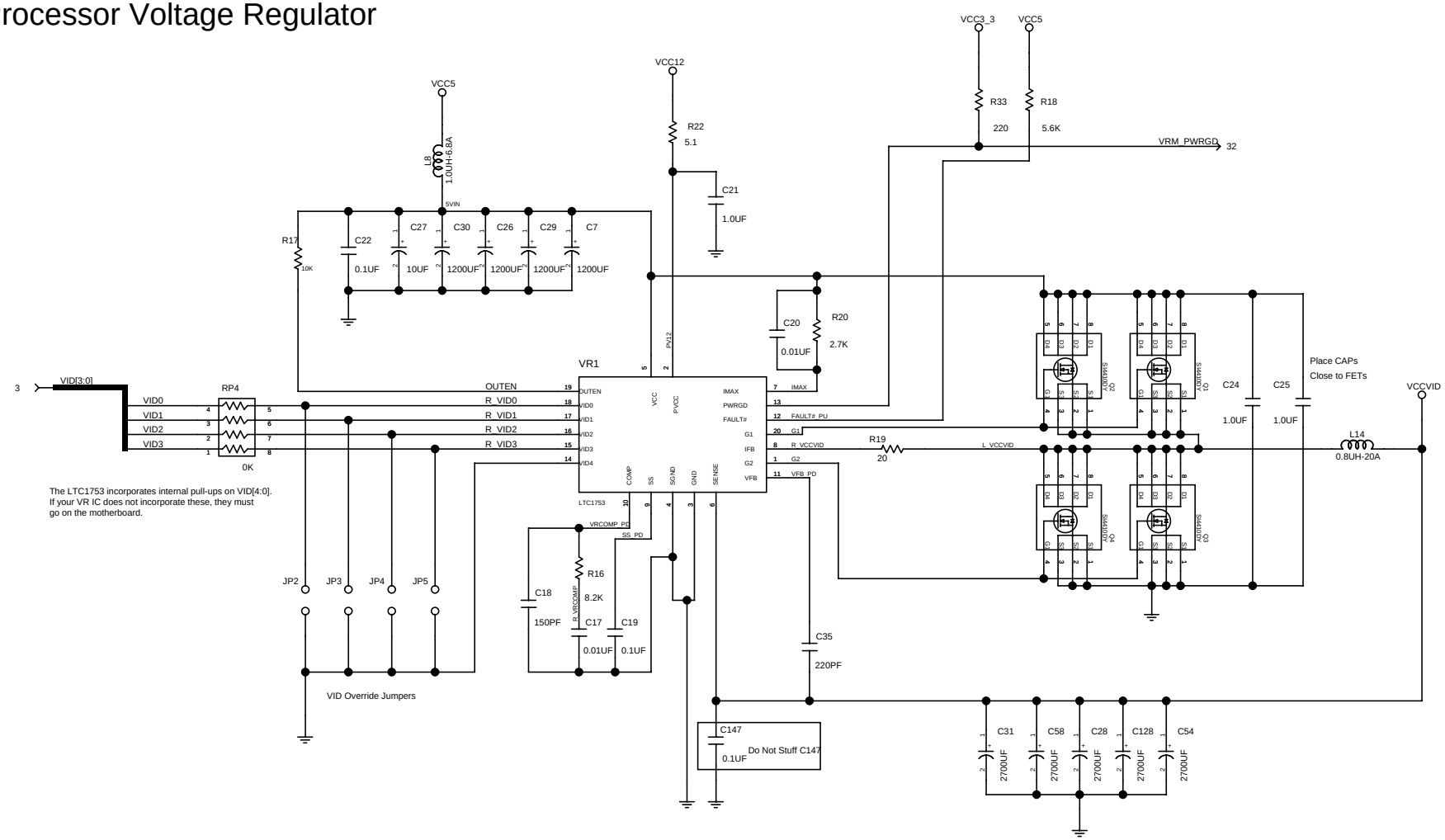


VCC 2.5 VOLTAGE REGULATOR



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD VOLTAGE REGULATORS		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44	PROJECT: INTEL(R) 810 CHIPSET SHEET: 29 OF 40

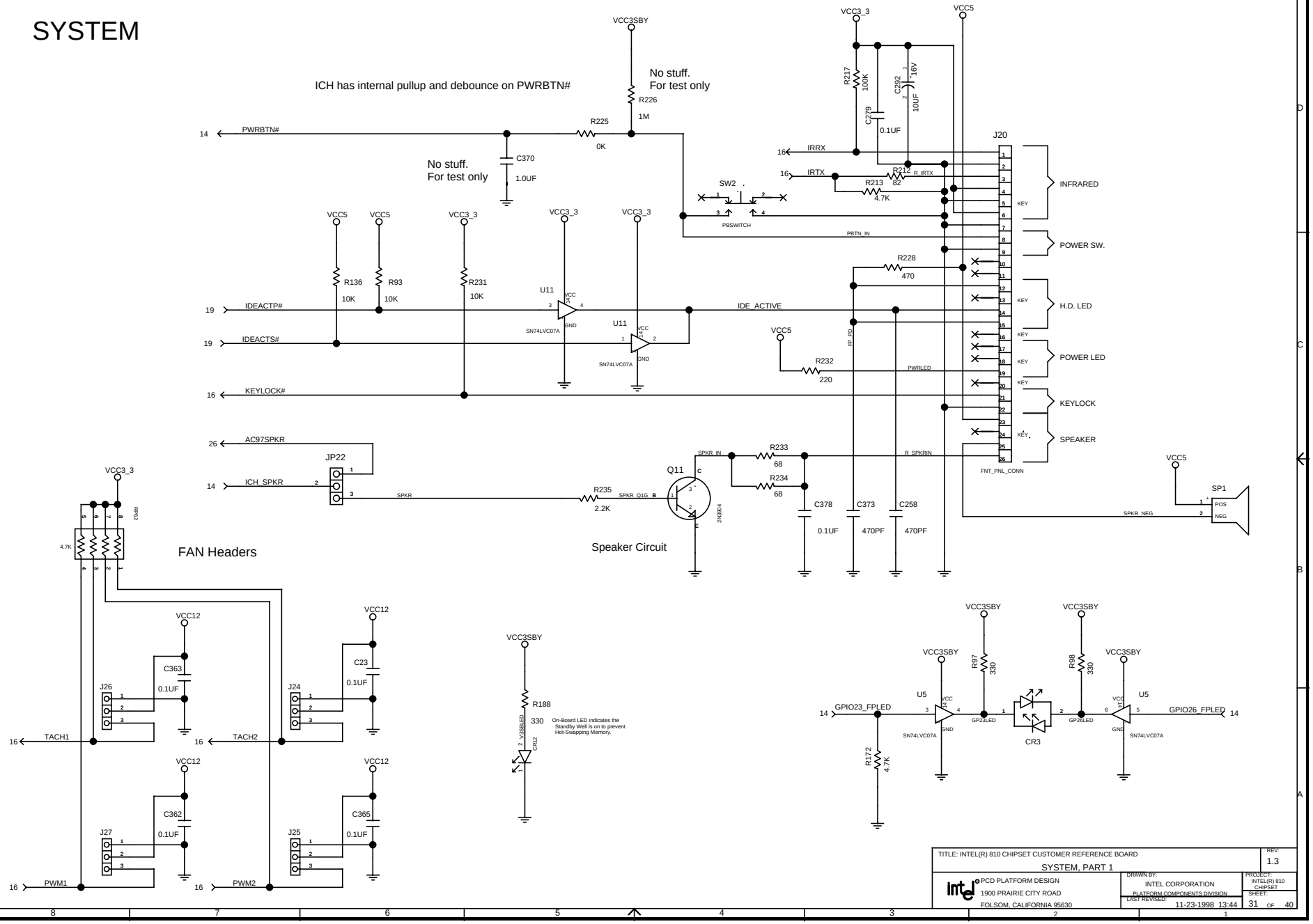
Processor Voltage Regulator



Refer to VR Supplier for Layout Guidelines

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD VRM 8.4		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 2-22-1999 11:02	PROJECT: INTEL(R) 810 CHIPSET SHEET: 30 OF 40

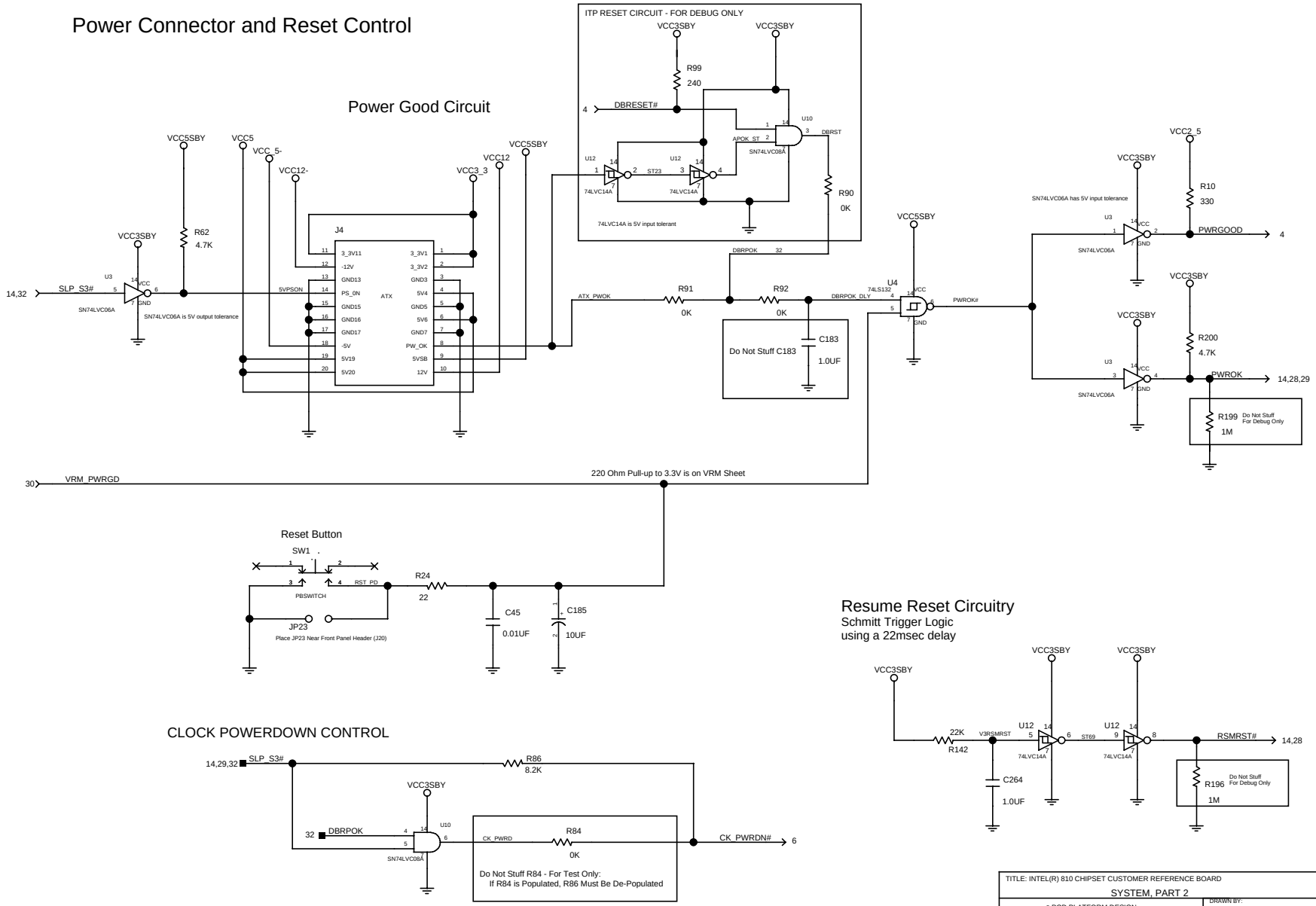
SYSTEM



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD SYSTEM, PART 1	REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44
PROJECT: INTEL(R) 810 CHIPSET SHEET: 31 OF 40	

SYSTEM

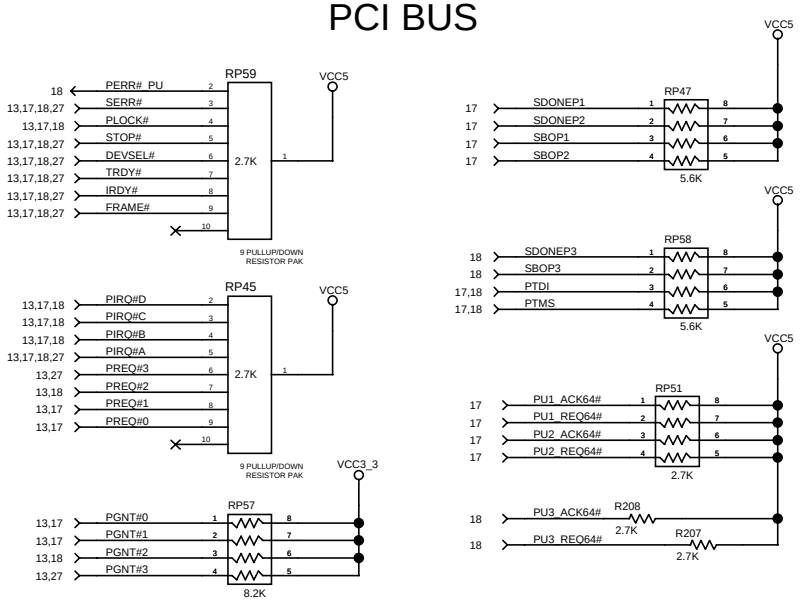
Power Connector and Reset Control



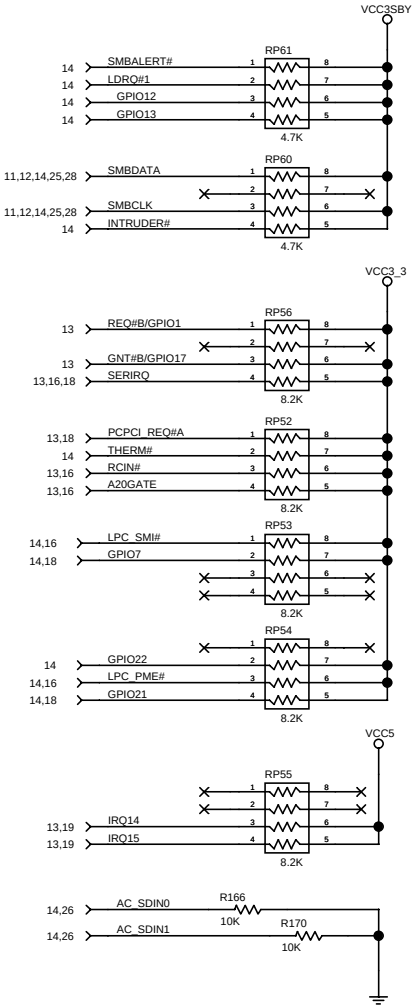
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD SYSTEM, PART 2	REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION
LAST REVISED: 12-6-1998 12:54	PROJECT: INTEL(R) 810 CHIPSET SHEET: 32 OF 40

PULL-UP RESISTORS AND UNUSED GATES

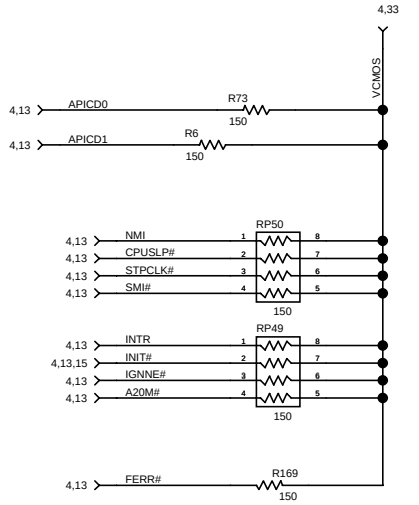
PCI BUS



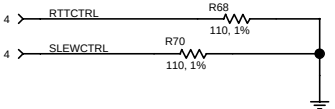
ICH0



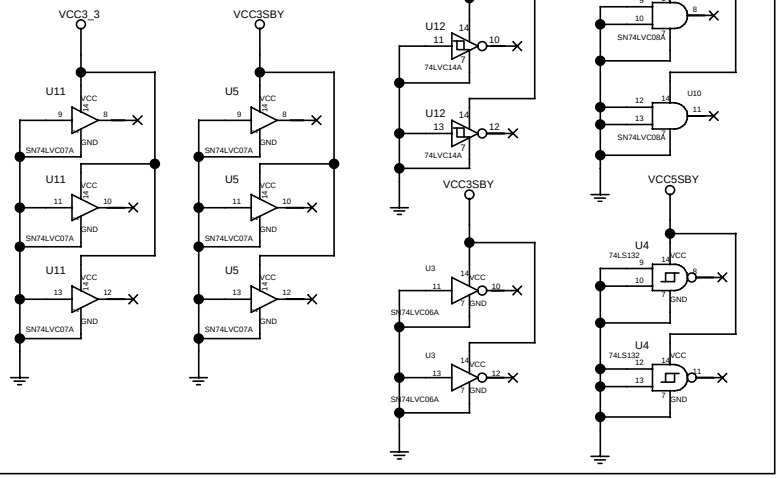
CPU



For Future Compatibility Upgrade

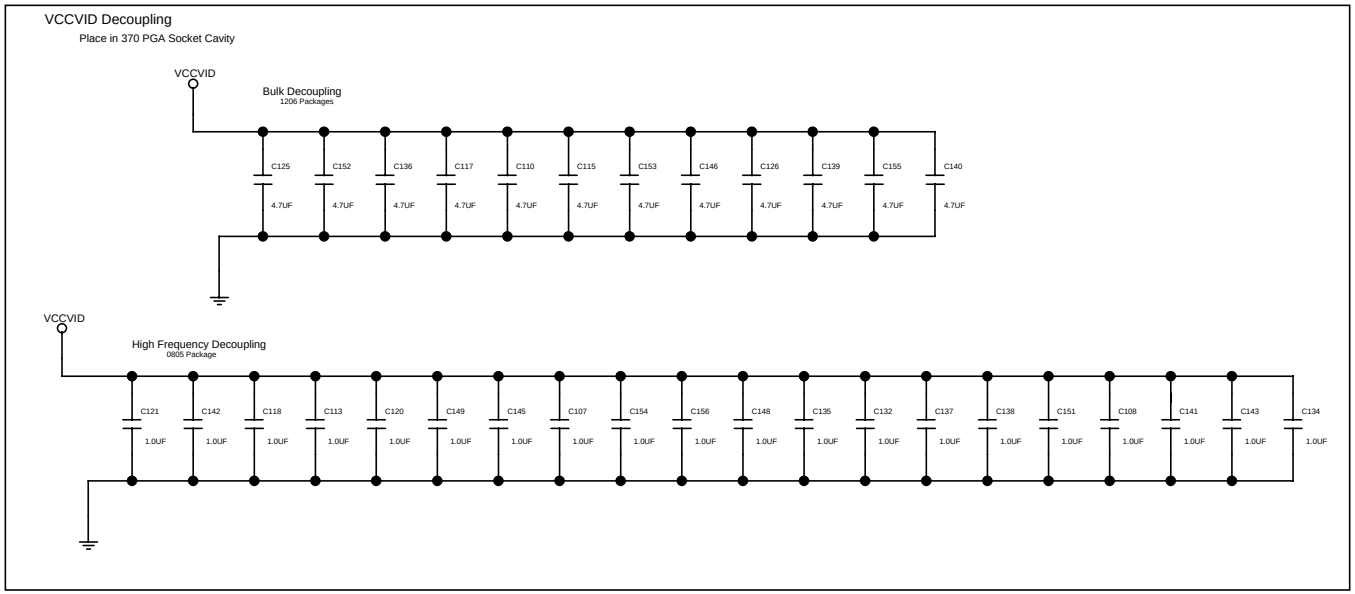


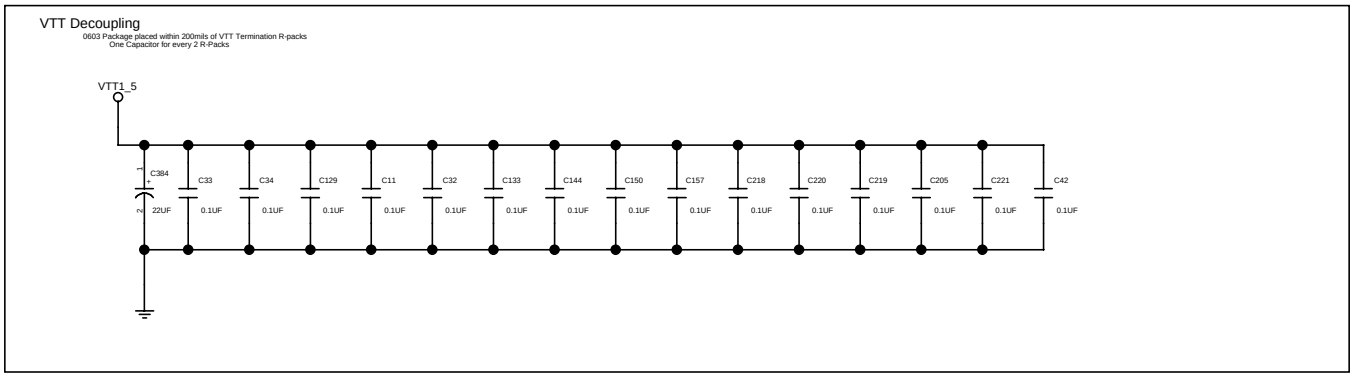
UNUSED GATES



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
PULLUP/PULLDOWN RESISTORS	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 5-26-1999 17:09
	PROJECT: INTEL(R) 810 CHIPSET SHEET: 33 OF 40

370-pin Socket Decoupling

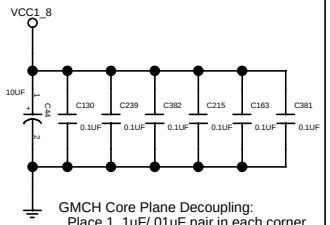




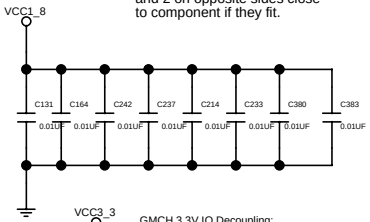
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD VRM DECOUPLING		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 12-8-1998 14:04	PROJECT: INTEL(R) 810 CHIPSET SHEET: 34 OF 40

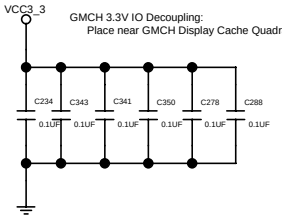
DRAM, CHIPSET, and BULK POWER DECOUPLING

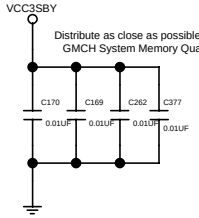
GMCH Decoupling



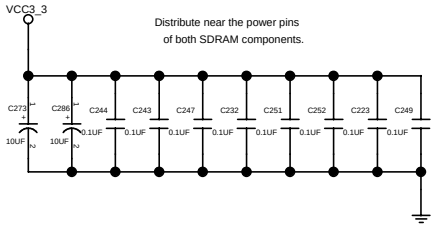
GMCH Core Plane Decoupling:
Place 1 .1uF/.01uF pair in each corner, and 2 on opposite sides close to component if they fit.



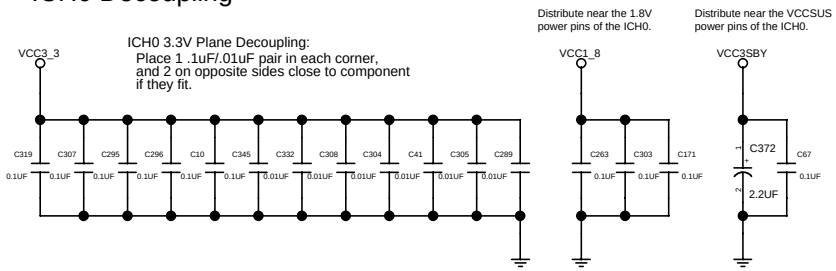




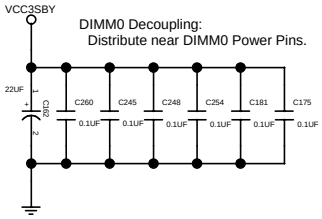
Display Cache Decoupling

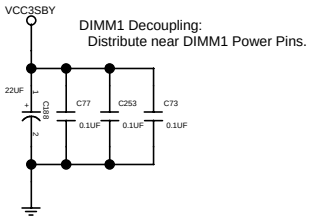


ICH0 Decoupling

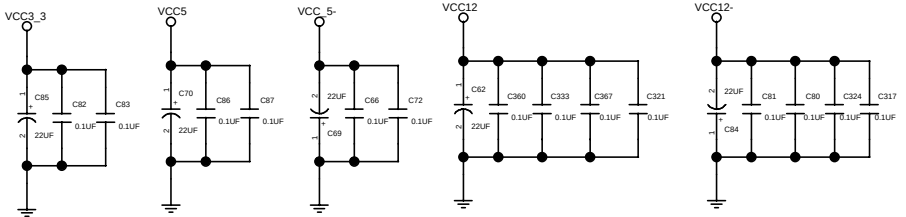


System Memory Decoupling

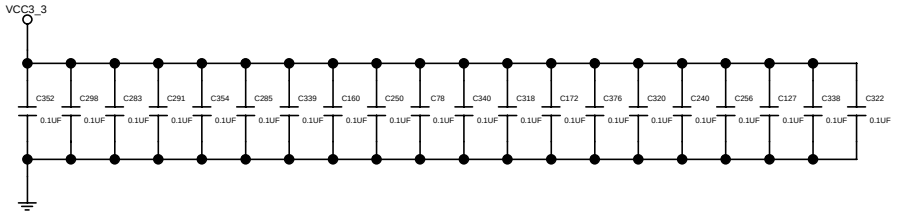




Bulk Power Decoupling



3 VOLT Decoupling



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD DRAM, ICH, AND GMCH DECOUPLING		REV: 1.3
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 5-26-1999 17:09	PROJECT: INTEL(R) 810 CHIPSET SHEET: 35 OF 40

Revision History (Changes from Rev 0.7)

Sheet	Description	Sheet	Description
ALL	Cosmetic changes to all pages (Re-names nets, re-organized symbol arrangement, etc.)	10	Ganged the tw o CKEs off of one 4.7K Pull-Up to 3.3V.
4	Changed FB1 (ferrite bead for PLL analog isolation) to Inductor L2.	11	Fixed Symbol Pinout
	Changed value of R36 to 10 ohms.	12	Fixed Symbol Pinout
	Replaced R21-R23 w ith 1K R-pack (RP50). Replaced R24-26 and R34 w ith RP44.		Removed SMBUS pullups from this page. There are pullups on page 32.
	Changed R184 value to 220 ohms		Removed Reset Straps from MD lines.
	Changed Pull-Up/Dow n Resistor Values on signals to ITP interface and grouped into Rpacks/Discretes to make true populate/de-populate Mfg. Option.	13	Updated Ballout
	Floated THERMTRIP# Signal		Changed C172 to 0.1UF Cap (HUBREF decoupling)
	Generate GTLREF w ith 1% resistors. Move from page 5 to page 4.		Added Resistor Site to Pull F16 to GND for test/debug.
	Changed BR0# Pull-Dow n to 56Ohm to use existing GTL Term Rpack Slot on sheet 5	14	Updated Ballout
	Added Jumper Test Option to GND BSEL line.		Routed PME# and SMI# to GPIO[13:12] respectively to support w ake events from S1.
	Change R35 from 51Ohm, 1% to 51Ohm, 5%		Pull RTCRST# signal from input node of first RC delay rather than output node (just other side of diode).
	Added VCMOS Decoupling		Moved Clear CMOS to RTCRST# signal and Added 1K resistor to GND on pin 3 of jumper.
6	Changed VDDA (pin22) of CK-Whitney to 3.3V Supply pet 0.5 Spec.		Change RTC Circuit to pow er Vbias straight from positive terminal of battery (BAT1). Was charged from VCCRTC input.
	Added/Modified Decoupling and Pow er Isolation		Changed AC_SYNC pull-dow n strap (CPU Safe Mode Jumper JP14) to AC_SDOUT pull-up strap.
	Ganged CPU and GMCH Clock Lines		Change C8 and C9 to 12pF caps.
	Isolated USB/DotCLK pow er (pin 27) from SDRAM pow er		Tied OC#0 and OC#1 together.
	Changed Pow erDow n control signal to NAND of SLP_S3# and PWR_OK		Add jumper straps to SPKR and AC_SYNC
	Change C146 and C147 from 10pF to 12pF		Remove Pull-up from SLP_S3# signal
7	Updated GMCH BallOut	15	Updated FWH pinout and labelled symbol as a TSOP Socket.
	Changed GTLREF divider to 1% resistors and GTLREF Decoupling to a 0.1uF (C2) and 0.001UF (C72) in parallel		Updated FWH (Socket) Symbol to include FGPI[4:0], routed ATA66 cable detect to GPI[1:0] and pulled rest dow n through 8.2K.
8	Updated GMCH BallOut		Cominbed Decoupling Caps and reduced to appropriate amount.
	HUBREF Generated from tw o 1% resistors w ith 0.1uF (C171) at GMCH HUBREF pin.		Changed JP4 to a 2 pole instead of 3 pole jumper.
	Changed C3 to 20pF Cap		Replace discrete resistors w ith R-packs. Replaced R84-87 w ith RP42.
	Decoupled System Memory 3.3V balls from Local Memory 3.3V balls. System Memory quadrant connects to 3.3Vsb plane and Local Memory connects to 3.3V plane.	16	Updated Pinout. Connected new VREF pin to 5V. Added Decoupling to IRRX/IRTX lines.
9	Updated GMCH BallOut		Routed PME# and SMI# to GPIO[13:12] respectively to support w ake events from S1.
	Connected VCCDACA and VCCDA signals to 1.8V through filtering circuitry. Connected VSSDACA and VSSDA to Digital GND.		Routed Game Port to game port header, 2nd Serial Port to serial header, PWM/Tach signals to fan headers, and unused signals to test header.
	Added Reset Strap jumpers to LMD[31:26].		Routed Unused GPIOs signals to test header.
	Added Oscillator to DotCLK for Test/Debug option		Removed JP6 and Grounded CLOCKI.
	Connected Digital Video Out signals		Connected VTR to VCC3.3 (removed from VCC3SB w ell) and added pow er decoupling.
	Changed R70 to 33Ohm and C4 to 20pF.		Pulled SYSOPT pin dow n to GND through 4.7K resistor. Moved Keylock pull-up sheet 31.

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD REVISION HISTORY, PART 1		REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:43	PROJECT: INTEL(R) 810 CHIPSET SHEET: 36 OF 40

Revision History (Changes from Rev 0.7)

Sheet	Description	Sheet	Description
17	Changed device numers (IDSEL wiring) for slots to AD16, AD17, and AD22. Routed additional signals required to AD22 slot to support ISA bridge test card.	27	Changed 93C46 Pinout.
18	Changed device numers (IDSEL wiring) for slots to AD16, AD17, and AD22. Routed additional signals through 0K resistors to AD22 slot to support ISA bridge test card.	28	Replaced RJ45 connector and discrete magnetics with integrated RJ45/magnetics part and connected accordingly.
	Added Jumper to route PERR# to ICH/ICH0 if ICH is populated.		Added LAN Disable Jumper.
19	Connected pin 34 of each connector to P66DETECT and S66DETECT(FWH_GPI0 and FWH_GPI1 respectively).		Added ICH/ICH0 scalability jumpers.
	Buffered PCIRST# signal going to pin 1 of IDE connectors to isolate cable loading.	29	Moved Power Connector to Sheet 32
	Removed Series Terminations from IRQ lines (pulled into ICH0).		Replaced old VCC5dual circuit, with VCC3Sby Circuit which generates supply for devices which must stay powered in S3. Removed LT1585-3.3 (U36 on rev0.7).
20	Isolated each VCC input to USB stacked connector through dedicated filtering circuitry.		Changed U27 from LT1585-1.5 to LT1587-1.5 and changed discretes.
	Added 47pF EMI caps on USB data lines.		Added V3SB regulator (generated V3SB from V5SB from ATX power supply).
	Connect USB through Audio/Modem Riser through 0K resistors.		Changed 1.8V Regulator design from LT1585ADJ to LT1587ADJ and changed discretes.
	Make OC detect circuitry unique to each port and update polyfuse value.		Changed 2.5V Regulator design from LT1585ADJ to LT1587ADJ and changed discretes.
21	Replaced DB25 connector with 2x13 header so we can cable out. SMB	30	Added VRM Override Jumpers to VID bus.
	Removed Series Termination Resistors from Ack# and Busy# signals.		Change VR Design to VRM8.4 compliant design. Use LTC1753 per Linear App Note.
	Changed Pull-ups to 2.2K	31	Moved Reset and Power circuitry to sheet 32
22	Added 2nd serial port and connected both through 2x5 headers to cable out (Removed 1 DB9 Connector).		Added Infrared, Power Switch, Hard Drive/Power LEDs, Keylock, and Speaker Circuitry to Common System Header.
	Added discrete solution to level translate and route Ring Indicate from Serial ports to ICH for Wake from S3 on serial modem.		Added 12V Fan Headers (2 supporting TACH outputs, and 2 support PWM inputs).
23	Added MIDI/Game Port circuitry connected through 2x8 header to cable out.		Added Debug LED to monitor 3.3VSBY Plane
	Increased Cap values on Keybd/Mouse lines from 100pF to 470pF.	32	Moved Pull-ups to sheet 33.
	Changed the keyboard and mouse symbols to a PS/2 stacked connector.	32	Updated new PWROK/PWRGOOD Generation, RESET, RSMRST# circtuitry.
25	Changed RGB PI filter caps from 22pF to 3.3pF.	33	Pulled-Up SMBUS interface to 3.3VSby instead of 3.3V.
	Added Quick Switch to level translate the CRT Sync, CRT DDC, and Flat Panel DDC Signals.		Removed R164 (FLUSH#) and R168 (THERMTRIP#) pull-ups. Removed pull-up on PWRGOOD (pulled up on sheet 32). Grouped remaining pull-ups to 1 1K Rpack.
	Isolated CK-Whitney from SMBUS in Power Down through Voltage translation Quick Switch.		Changed all PCI 3.3V pull-ups to 8.2K per PCI spec.
	Changed VGA Connector symbol.		Combined like pullups into R-packs where possible.
	Added EMI Caps on SYNC and DDC Signals.		Added 8.2K pull-ups to SERIRQ and ICH0 unused GPIOs.
26	Routed USB up the AMR Connector.		Added Pull-Up Sites for FLUSH# and 370PGA Socket Pin W35 to VCMOS for future compatibility upgrade.
	Ran 5V (instead of 5VSB) to Audio Modem Riser.	34	Updated Processor Decoupling per latest Guidelines for 370PGA socket.
	Added stuffing option AC'97 debug port	35	Added System Decoupling

Revision History (Changes from Rev0.9 to Rev0.95)

Sheet	Description	Sheet	Description
2	Changed "Video Encoder" box on Block Diagram to "Digital Video Out Device" Box.	20	Changed R117,R118,R121,R122 from 27ohm to 15ohm-1% Resistors
	Added Device Table	22	Change R207 from 47K to 10K
3	Changed Reference Designator on 370-pin Socket from J20 to X1	23	Moved RP31 from pg. 16 to pull-up Key/Mouse lines to filtered VCC5.
4	Changed Reference Designator on 370-pin Socket from J20 to X1		Added 470pF Caps on MIDI lines (C327,C328).
	Changed C1 from 22uF,30% to 47uF,10%	25	Moved R67,R68,R69 from Sheet 9.
6	Changed Series Termination Resistor Values from 22 Ohms to: R37,R38,R55,R56,R57=43ohm,2%; R39,R40,R41,R42,R43,R46,R47,R58,R59,R60,R61=33ohm,2%; R45,R48,R49,R50,R51,R52,R53,R54,R63=33ohm,5%; R44,R226=10ohm,5%		Cleaned Up VGA Connector Schematic
	T'ed REFCLK and added R226 (to separate termination to ICH and SIO). Renamed CLK14 to SIO_CLK14 and ICH_CLK14 for each new NET out of the T.		Added Provisions to add PI Filters on VSYNC and HSYNC Lines
	Changed C144 and C185 from 4.7uF to 22uF.		Changed 5V Supply to Quick Switch to pull-down on DIODE output. Also pulled DDC lines up to the same supply powering the Quick Switch.
8	Added Cap Site to GMCH Hub Clk		Change R132,R133 from 8.2K to 1K Pull-Ups
	Added 0K Resistor (R231) in series with DCLK_WR	26	Removed AC97 Debug Connector (J5)
9	Changed Reference Designator on Oscillator Socket from U34 to X2	27	Changed R4 pull-up from 62K to 4.7K and added 0.1uF Decoupling to VIO pin (C262).
	Corrected Connection of Debug Oscillator from DDCSDA to DOTCLK NET.		Added Decoupling for LAN Power (C336-C341)
	Updated Pin Numbers to match GMCH 0.7 EDS Ballout	28	Change R140/R141 to 4.7K Resistors
	Added 0K Resistor (R232) in series with LRCLK	29	Modified CK_PWRDWN# Generation Circuitry to pull off U33 NAND gate and invert through U13 to get correct logic level. Previously it was tapped off the base of BJT Q6. This would have kept CK_PWRDWN# from charging higher than 0.7V (drop across BE junctio
	Added Cap Site to ICH Hub Clk		Changed R191 to 10K, R192 to 0K, and R193 to 4.7K
	Replace Bead FB21 with Inductor (L4) - 68nH to create LC filter (<130kHz)	30	Changed Reference Designator on U15 and U25 to Q9 and Q10 respectively.
	Added LC filter to 1.8V plane connected to balls U6 and E19.		Changed Reference Designator on U8 to VR5, U11 to VR3, and U27 to VR4
	Changed Test Oscillator Circuit (U34) to remove shorted jumper and add decoupling. Changed pin names on 48MHz oscillator symbol.		Changed C268 and C259 to 1.0uF,X7R caps
	Moved R67,R68,R69 to Sheet 25.		Added 2 more Si4410DY FETs in parallel with two there (Q7/Q8)
14	Rename NET CLK14 to ICH_CLK14		Changed C160-C163 to 2700uF and added one more (C342) in parallel.
	Rename Pin L1 to VCCSUS1 and Pin N1 to VCCSUS2		Change C153 to 220pF
	Rename NET GPIO23 to GPIO23_FPLED, and NET GPIO26 to GPIO26_FPLED		Changed connections of COMP and SS to show them returning directly to SGND pin.
	Routed LPC_SMI# and LPC_PME# to GPIO[5:6] respectively from GPIO[12:13] respectively.		Added Inductor (L13) to filter 5V input to VRM
	Changed Value of C11 from 0.1uF to 1.0uF	31	Change reference designator S1 to SW1
15	Changed Reference Designator on U9 to X3		Change C79 to 1.0uF
15	Added 0K RPACK(RP68) in series to GROUND on FWH ID lines for Test/Debug.		Add Front Panel Dual LED Circuit controlled by ICH GPIOs
16	Changed Pin 87 Name from RTS1#_SYSOP to RTS1# and Pin 50 name from GP27/IO_SMI#/TEST to SP27/IO_SMI#	32	Change ATX connector Reference Designator from U6 to J29.
16	Rename NET CLK14 to SIO_CLK14		Change reference designator S2 to SW2
		33	Removed Pull-Ups from GPIO23/GPIO26
16	Moved RP31 to pg. 23 to pull-up Key/Mouse lines to filtered VCC5.		Pulled LDRQ#1 Up to 3.3VSby (instead of 3.3V).
17	Swapped ACK64# and REQ64# to route to correct pins per PCI spec.		Changed PCI Pull-Up Resistor (R99,R100,RP53,RP46,RP47) values from 8.2K to 2.7K and connected to 5V. Also connected RP40 and RP43 to 5V (from 3.3V) to maintain compatibility with more 5V PCI cards.
18	Swapped ACK64# and REQ64# to route to correct pins per PCI spec.		Removed RP49 (VID Pull-Ups) Since internal to LTC1753
	Replaced JP6 Jumper with 0K Resistor Stuffing Option (R233, R234)	35	Added additional Decoupling for Various Components (C343-C389)
19	Inserted 0K Stuffing Resistors in Series with ATA66 Cable Detect (R235,R236)		Changed C217-C220 from 0.1uF to 0.01uF
19	Swapped 74LS07 out for 74LVC07A and connected to 3.3V.	ALL	Changed Reference Designators on All Ferrite Beads from FB* to L*.

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD REVISION HISTORY, PART 3		REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:43	PROJECT: INTEL(R) 810 CHIPSET SHEET: 38 OF 40

Revision History (Changes from Rev0.95 to Rev0.99)

Sheet	Description
4	Changed C1 to 33uF and L2 to 4.7uH.
	Connected E21 to VCC_DET Pull-Up
	Added 0603 Cap Site on CPUHCLK
	Removed RP50 and routed TCK and TMS to 330ohm pull-ups in RP44.
5	Changed Rpack connections per Layout Back Annotation
6	Changed R39-R43,R46,R47,R58-R61 to 33ohm,5% (from 2%)
	Routed CK_PWRDN# to Clock Chip (SLP_S3# thru 8.2K resistor by default).
7	Added 0603 Cap Site on GMCHHCLK
8	Changed HUBREF Voltage Divider Resistor Values (R182 and R185) from 1K-1% to 301ohm-1% and added AC Decouping Discrete Sites (C394,C395,R245,R246)
9	Added 22ohm series term (R242) to LTCLK Net (U22.K22).
	Moved C323, C324 to page 34 and made C324 0.01uF.
	Removed L5 and C325. Change C5 to 33uF. Connect U22.U6 and U22.E19 direct to VCC1_8 Plane. Change U22.AB21 and U22.AB23 to connect to VCC1_8.
	Removed Series Terms on Digital Video Out Port
	Added 0K (R31) in series with Debug Oscillator
	Routed DC_MD27 (core detect Strap) to 10K to 220 pull-up on VCCDET net.
14	Changed C148 from 2.2uF Monolithic to 2.2uF Polarized
	Changed Reference Designator on BAT1 to X4 (it is a socket footprint).
16	Pulled Up SUSSTAT to 3.3V through 4.7K (R136, which was removed from LAN page) resistor and disconnected from ICH0.
19	Changes to P66DETECT and S66DETECT NETs to support both Drive and Host Sided 80 conductor cable detection: Added C392 and C393 (0.047uF, X7R, 16V, 10%) to GND, 0ohm Resistors in Series (R235,R236), and 15K Pull-downs (R243,R244) to GND.
20	Fixed Connectivity of Resistor R124. USBV5 Net now Connects directly to L26 terminal 1, and R124 disconnected from L26 terminal 1. Eliminated unwanted resistor divider on 5V power pins at USB port.
	Added Series Resistors (0K) to decouple ICH USB signals from stacked connector if routed up AMR connector.
22	Changed Net Name G_ICHRI# to ICHRI#_C

Sheet	Description
24	Change C330 to a 100pF cap and Scaled Back Decoupling on power planes to U28..
	Swapped Connectivity of FTCLK0 and FTCLK1.
25	Fixed Connectivity of CR2, CR4, CR5, CR6 and CR7. In all cases Pins 1 and 2 were swapped.
	Change L8,L9,L10 Part Number to BLM11B750S
	Changed F3 from 2.0A Fuse to 2.5A Fuse.
27	Removed Pull-up from LANTCK (U29.D14) and made No Connect. R136 moved to Sheet 16 to Pull-up LPCPD (U16.27).
	Removed C338,C339,C340,C341 and Changed C336,C337 to 4.7uF Polarized Capacitors.
	Changed INTA# (U29.H2) from PIRQ#D to PIRQ#A and Changed LAN IDSEL (R142.1) from AD19 to AD20.
28	Made C74 a 470pF-1500V cap and added "For EST Testing" Note.
	Changed J28.14 connection from ACTLED to SPEEDLED and Changed R219.1 connection from VCC3SBY to ACTLED
	Added Provision for Isolating 82559 either on SUS_STAT# or PWROK
29	Changed Reference Designator U14 to Q10 and U16 to Q11.
	Renamed NET CK_PWRD to IN_U5, and Deleted connection to U13 pin 9
	Removed CK_PWRDWN# NET, R240
30	Connected Q4.{5-8}/Q7.{5-8}, C193, R150 to Net 5VIN instead of direct to VCC5.
	Added 0K Rpack (RP69) in Series to VID[3:0] pins of VR3.
31	Changed Switch Symbol to 4-pin device to match physical device.
32	Changed RefDes U6 to J29.
	Changed Switch Symbol to 4-pin device to match physical device.
	Added provision for sending early powerok to Clock PD# pin for clean Power-up
33	Swapped SIP Rpacks on CPU and ICH pull-ups to 4-Element Rpacks per Layout Back Annotation
	Change RP48 from 1K Rpack to 330ohm Rpack, and R202, and R203 from 1K resistors to 330ohm resistors for future upgrade compatibility.
35	Added Additional Decoupling on VCC12- and VCC12

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD	REV: 1.3
REVISION HISTORY, PART 4	
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:43
PROJECT: INTEL(R) 810 CHIPSET	SHEET: 39 OF 40

Revision History:Changes from Rev0.99 and On

Changes from Rev0.99 to Rev1.0

- Back Annotated from Layout (Reference Designator Changes/Rpack Routing Swaps)
- Changed Series Term Values on CPU and APIC Clocks to 33ohm (Sheet 6)
- Changed Series Term Values on Memory, Hub, and DOT Clocks to 22ohm (Sheet 6)
- Added 10K Pull-Ups on SLP_S3# and SLP_S5# (Sheet 14)
- Added 2 1200uF Caps on VCC3_3SBY Plane (Sheet 29)

Changes from Rev1.0 to Rev1.1

- Removed X1, R77, R78, R79 (Debug Oscillator Socket) from Sheet 9
- Connected C377 to VCC3_3SBY Plane
- Corrected Pinout of 2x5 Com Port Headers (Sheet 22)
- Added 2x1 Header (JP23) to sheet 32 for Chasses Reset Button

Changes from Rev1.1 to Rev1.2

- Added RP70 and RP71 to Sheet 8 (SM_MA Series Terms)
- Removed 330Ohm Pull-Ups from FLUSH# and TestHi (W35 on 370-Pin Socket)
- Added 110Ohm, 1% Pull-Downs to pins S35 and E27 of 370-pin Socket (RTTCTRL and SLEWCTRL)
- Changed C347 from a 2200pF Cap to a 0.047uF Cap

Changes from Rev1.2 to Rev1.3

- Changed VCCDET Net name to VCOREDET
- Changed Value of R125 to 174ohm, 1% (from 178ohm, 1%)
- Changed value of C347 back to 2200pF Cap (from 0.047uF Cap)
- Designated R126 as No Stuff per SiI 154 Specification
- Removed R123 pull-up and connected SiI154 pin 13 to reset.
- Changed RP50, RP49, and R169 from 330ohm to 150ohm

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD REVISION HISTORY, PART 5		REV: 1.3
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 5-26-1999 17:09	PROJECT: INTEL(R) 810 CHIPSET SHEET: 40 OF 38