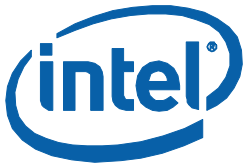

Intel® Core™ i5 Processor With Mobile Intel® QM57 Express Chipset

Development Kit User Guide

December 2009

Revision 001

Document Number: 322996

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Revision History

Document Number	Revision Number	Description	Revision Date
322996	001	Initial release.	November 2009

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1 About This Manual

This guide describes the use of the Intel® Core™ i5 Processor with Mobile Intel® QM57 Express Chipset Development Kit. This manual has been written for OEMs, system evaluators, and embedded system developers. This manual assumes basic familiarity in the fundamental concepts involved with installing and configuring hardware for a personal computer system. This document defines all jumpers, headers, LED functions, their locations on the development kit, and other subsystem features and POST codes. This manual assumes basic familiarity in the fundamental concepts involved with installing and configuring hardware for a personal computer system.

For the latest information about the Red Fort CRB and platform design collateral, please visit the Embedded Platform Code Named Calpella+ECC – including the Auburndale/Arrandale and Auburndale+ECC/Arrandale+ECC Processors and the Ibex Peak-M PCH for Embedded Applications:

http://tigris.intel.com/scripts-edk/viewer/UI_CLCatalog.asp?edkId=8381.

1.1 Content Overview

This manual is arranged into the following sections:

- About This Manual contains a description of conventions used in this manual. The last few sections explain how to obtain literature and contact customer support.
- Getting Started describes the contents of the development kit. This section explains the basics steps necessary to get the board running. This section also includes information on how to update the BIOS.
- Development Board Features describes details on the hardware features of the development board. It explains the Power Management and Testability features.
- Development Board Physical Hardware Reference provides a list of major board components and connectors. It gives a description of jumper settings and functions. The chapter also explains the use of the programming headers.
- Rework Instructions contains rework instructions for the development board and for some of the add-in cards to enable additional supported features and functionality.
- Add-in Cards contains information on add-in cards available from Intel that can be used with the development board.
- Heatsink Installation Instructions provides instructions for installing the heatsink.

1.2 Text Convention

The notations listed in Table 1 may be used throughout this manual.

Table 1. Text Conventions

Notation	Definition
#	The pound symbol (#) appended to a signal name indicates that the signal is active low. (e.g., PRSNT1#)
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either uppercase or lowercase.
Numbers	Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character H. A zero prefix is added to numbers that begin with A through F. (For example, FF is shown as 0FFH.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 is a binary number. In some cases, the letter B is added for clarity.)
Units of Measure A GByte KByte KΩ mA MByte MHz ms mW ns pF W V µA µF µs µW	The following abbreviations are used to represent units of measure: amps, amperes gigabytes kilobytes kilo-ohms milliamps, mill amperes megabytes megahertz milliseconds milliwatts nanoseconds picofarads watts volts microamps, microamperes microfarads microseconds microwatts
Signal Names	Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (n). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CSn#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Terminology

The notations listed in Table 2 may be used throughout this manual.

Table 2. Terminology

Term	Description
Aggressor	A network that transmits a coupled signal to another network.
Anti-etch	Any plane-split, void or cutout in a VCC or GND plane.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. Even Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. Odd Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Duck Bay 3	PCI Express* interposer card that provides Express-card support for CRB
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the TCO (time from clock-in to data-out) of the driver, plus any adjustments to the signal at the receiver needed to ensure the setup time of the receiver. More precisely, flight time is defined as: The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. Maximum and Minimum Flight Time - Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. Maximum flight time is the largest acceptable flight time a network will experience under all conditions. Minimum flight time is the smallest acceptable flight time a network

Term	Description
	will experience under all conditions.
Infrared Data Assoc.	The Infrared Data Association (IrDA) has outlined a specification for serial communication between two devices via a bi-directional infrared data port. The CRB has such a port and it is located on the rear of the platform between the two USB connectors.
IMVP6.5	The Intel® Mobile Voltage Positioning specification for the Arrandale Processor. It is a DC-DC converter module that supplies the required voltage and current to a single processor.
Inter-Symbol Interference	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI may impact both timing and signal integrity.
Mott Canyon IV	This Add-in Card enables Intel® High Definition Audio functionality
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pin	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings may be measured at the pin.
Power-Good	"Power-Good," "PWRGOOD," or "CPUPWRGOOD" (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active at a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Ringback	The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the processor.
Setup Window	The time between the beginning of Setup to Clock (TSU_MIN) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

Term	Description
Simultaneous Switching Output	Simultaneous Switching Output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay ("push-out") or a decrease in propagation delay ("pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end.
System Management Bus	A two-wire interface through which various system components may communicate.
Undershoot	The minimum voltage extending below VSS observed for a signal at the device pad.
VCC (CPU core)	VCC (CPU core) is the core power for the processor. The system bus is terminated to VCC (CPU core).
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

Table 3 defines the acronyms used throughout this document.

Table 3. Acronyms

Acronym	Definition
AC	Audio Codec
ACPI	Advanced Configuration and Power Interface
ADD2	Advanced Digital Display 2
ADD2N	Advanced Digital Display 2 Normal
AIC	Add-In Card
AMC	Audio/Modem Codec.
Intel® AMT	Intel® Advanced Management Technology
ASF	Alert Standard Format
AMI*	American Megatrends Inc.* (BIOS developer)
ATA	Advanced Technology Attachment (disk drive interface)
ATX	Advance Technology Extended (motherboard form factor)

Acronym	Definition
BGA	Ball Grid Array
BIOS	Basic Input/Output System
CK-SSCD	Spread Spectrum Differential Clock
CMC	Common Mode Choke
CMOS	Complementary Metal-Oxide-Semiconductor
CPU	Central Processing Unit (processor)
CRB	Customer Reference Board
DDR	Double Data Rate
DMI	Direct Memory Interface
DPST	Display Power Saving Technology
ECC	Error Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMA	Extended Media Access
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
EV	Engineering Validation
EVMC	Electrical Validation Margining Card
ERB	Early Engineering Reference Board
FCBGA	Flip Chip Ball Grid Array
FDD	Floppy Disk Drive
FIFO	First In First Out - describes a type of buffer
FIR	Fast Infrared
FS	Full-speed. Refers to USB
FSB	Front Side Bus
FWH	Firmware Hub
GMCH	Graphics Memory Controller Hub
GPIO	General Purpose IO
Intel® HDA	Intel® High Definition Audio
HDMI	High Definition Media Interface
HS	High-speed. Refers to USB
ICH	I/O Controller Hub

Acronym	Definition
IDE	Integrated Drive Electronics
Intel® MVP	Intel® Mobile Voltage Positioning
IP/IPv6	Internet Protocol/Internet Protocol version 6
IrDA	Infrared Data Association
ISI	Inter-Symbol Interference
KBC	Keyboard Controller
LAI	Logic Analyzer Interface
LAN	Local Area Network
LED	Light Emitting Diode
LOM	LAN on Motherboard
LPC	Low Pin Count (often used in reference to LPC bus)
LS	Low-speed. Refers to USB
LVDS	Low Voltage Differential Signaling
MC	Modem Codec
MDC	Mobile Daughter Card
ME	Manageability Engine
MHz	Mega-Hertz
OS	Operating System
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PCIe*	PCI Express*
PCH	Platform Controller Hub
PCM	Pulse Code Modulation
PGA	Pin Grid Array
PLC	Platform LAN Connect
PLL	Phase Locked Loop
POST	Power On Self Test
RAID	Redundant Array of Inexpensive Disks
RTC	Real Time Clock
SATA	Serial ATA
SIO	Super Input/Output
SKU	Stock Keeping Unit
SMC	System Management Controller

Acronym	Definition
SMBus	System Management Bus
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SPWG	Standard Panels Working Group - http://www.spwg.org/
SSO	Simultaneous Switching Output
STR	Suspend To RAM
TCO	Total Cost of Ownership
TCP	Transmission Control Protocol
TPM	Trusted Platform Module
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus
VGA	Video Graphics Adapter
VID	Voltage Identification
VREG or VR	Voltage Regulator
XDP	eXtended Debug Port

1.4 Reference Documents

Table 4 provides a summary of publicly available documents related to this development kit. For additional documentation, please contact your Intel Representative.

Table 4. Reference Documents

Document	Document Number
[Calpella] Platform Mobile Intel® 5 Series Chipset (formerly called Ibex Peak-M) – I/O Buffer Information Specification (IBIS) Models	384457
[Calpella] Platform, Red Fort Customer Reference Board (CRB) – Schematics / Diagrams	382504

Document	Document Number
[Calpella] Platform, Red Fort – Customer Reference Board File	392593
[Calpella] Platform – Cadence / OrCad Symbol Files	382676
[Calpella] Platform, Power Sequence – Product Specification	393353
Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification	414591
Calpella Platform, for Arrandale, Clarksfield and Mobile Intel® 5 Series Chipset – Design Guide	398905
Arrandale Processor External Design Specification - Volumes 1 and 2	416056/ 415057
[Calpella] Platform,PCIe graphics-2 Add-in-Card – User Guide	414150
[Calpella] Platform, PCI expansion card 2 Add In Card – Schematics / Diagrams	417149
Intel® 5 Series Chipset and Intel® 3400 Series Chipset – External Design Specification (EDS)	401376

1.5 Development Kit Technical Support

1.5.1 Online Support

Intel's web site (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week.

1.5.2 Additional Technical Support

If you require additional technical support, please contact your Intel Representative or local distributor.

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2 Getting Started

2.1 Development Kit

The following hardware, software and documentation are included in the kit. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

- Letter to the Customer
- Development Kit User's Manual (this document)
- Software CD-ROM, which includes (see the readme.txt file for a complete list of CD-ROM contents):
  - System BIOS
  - BIOS installation utilities
  - Chipset drivers
  - Intel Embedded Graphics Drivers
  - Intel® Active Management Technology (Intel® AMT) software installation kit
- Pre-assembled development system, which includes:
  - Red Fort motherboard
  - Chassis and mounting screws (installed)
  - Intel® Core™ i5 Processor (installed)
  - Processor thermal solution and CPU back plate
- Mobile Intel® QM57 Express Chipset (installed)
- Intel® QM57 heatsink (installed)
- One Type 2032, 3 V lithium coin cell battery (installed)
- One 1GB DDR3 SO-DIMM
- One Port 80 display card
- One Power Supply
- One 80Gb SATA Hard Disk Drive
- One SATA DVD-ROM Drive
- SATA Cabling (Data and power)
- One HDMI and Display Port add-in card
- One PCI Extension Card

Current drives required for this development are available at http://platforms.intel.com.

2.2 Additional Required Hardware Not Included In This Kit

The following additional hardware may be necessary to successfully set up and operate the motherboard:

- **VGA Monitor:** Any standard VGA or multi-resolution monitor may be used. The setup instructions in this chapter assume the use of a standard VGA monitor, TV, or flat panel monitor.
- **Keyboard**: The Development kit can support either a PS/2 or USB style keyboard.
- **Mouse:** The Development kit can support either a PS/2 or USB style mouse.
- **Hard Disk Drives (HDDs) and Optical Disc Drives (ODD):** Up to six SATA drives and two IDE devices (master and slave) may be connected to the Development kit. An optical disc drive may be used to load the OS. All these storage devices may be attached to the board simultaneously.
- **Video Adapter:** Integrated video is output from the VGA connector on the back panel of the Development kit. Alternately, an on board HDMI connector, On board DP connector or LVDS displays can be used for desired display options. Check the BIOS and the graphics driver, where appropriate, for the proper video output settings.
- **Network Adapter:** A Gigabit network interface is provided on the Development kit. The network interface will not be operational until after all the necessary drivers have been installed. A standard PCI/PCI Express* adapter may be used in conjunction with, or in place of, the onboard network adapter.

You must supply appropriate network cables to utilize the LAN connector or any other installed network cards.

- **Other Devices and Adapters:** The Development kit functions much like a standard desktop computer motherboard. Most PC-compatible peripherals can be attached and configured to work with the Development kit.

2.3 Additional Required Software Not Included In This Kit

The following additional software may be necessary to operate this system:

- **Operating System:** The user must supply any needed operating system installation files and licenses.
- **Application Software:** The user must supply any needed application software.

2.4 Workspace Preparation

The development kit is shipped as an open system to provide flexibility in changing hardware configurations and peripherals in a lab environment. Because the board is not in a protective chassis, the user is required to take the following safety precautions in handling and operating the board:

1. The power supply cord is the main disconnect device to main power (AC power). The socket outlet should be installed near the equipment and should be readily accessible.
2. To avoid shock, ensure that the power cord is connected to a properly wired and grounded receptacle.
3. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.
4. Use a flame retardant work surface and take note of closest fire extinguisher and emergency exits.
5. Ensure a static-free work environment before removing any components from their anti-static packaging. Wear an ESD wrist strap when handling the development board or other development kit components. The development board is susceptible to electrostatic discharge (ESD) damage, and such damage may cause product failure or unpredictable operation.

2.5 System Setup2.5

Please follow the steps outlined below to ensure the successful setup and operation of your development kit system.

These steps should already be completed in the kit:

1. One (or more) DDR3 SO-DIMMs in memory sockets, populating J4V1 and/or J4W1.
2. The processor in socket U7J2 is locked in place (make sure to align the chip to the pin 1 marking).
3. The (default) configuration jumpers are as shown in Table 23.
4. RTC battery is populated in BT5G1.
5. The cable from the ATX power supply is inserted into J4J1.
6. The hard disk drive (HDD) is attached with the supplied cable SATA.
7. The optical driver (ODD) is a attached with the supplied SATA cable.

The following steps need to be completed by the user:

1. Connect either a PS/2 keyboard in J1A1 (bottom) or a USB keyboard in one of the USB connectors.
2. Connect either a PS/2 mouse in J1A1 (top) or a USB mouse in one of the USB connectors.
3. If using external graphics, plug a PCI graphics card in PCIe x1 slot J6C2 or a PCI Express Graphics card in the PCIe x16 slot J5C1 and connect a monitor to the card
4. Connect an Ethernet cable (optional), one end of the cable to the motherboard, the other end to a live Ethernet hub.

5. Connect the monitor to the VGA connector. Also take care to plug the monitor's power cable into the wall.

2.6 System Power-up

Having completed the steps outlined above, you are now absolutely ready to power up the development kit:

1. Install the heatsink/fan for the processor at U7J2, and the fan-power cable must be plugged into J4C1.
2. Press the power button.
3. As the system boots, press F2 to enter the BIOS setup screen.
4. Check time, date, and configuration settings. The default settings should be sufficient for most users with the exception of Intel® SpeedStep™ Technology. This feature is disabled by default and can be enabled in setup.
5. Press F4 to save and exit the BIOS setup.
6. The system reboots and is ready for use.

The fan/heatsink installation is discussed in Heatsink Installation Instructions.

Install operating system and necessary drivers:

Depending on the operating system chosen, drivers for components included in this development kit can be found in http://platformsw.intel.com.

Note: Not all drivers are supported across all operating systems.

2.7 System Power-down

There are three options for powering-down the development kit. Those three options are:

- Use OS-controlled shutdown through the OS menu (e.g., Windows* XP: **Start → Shut Down**).
- Press the power button on the motherboard at SW1E1 to begin power-down.
- If the system hangs, it is possible to asynchronously shut the system down by holding the power button down continuously for 4 seconds.

Intel **does not** recommend powering down the board by removing power at the ATX power supply by either unplugging the power supply from the AC source/wall or by unplugging the DC power at the board.

2.8 System BIOS

A version of the AMI* BIOS is pre-loaded on the development kit board.

2.8.1 Configuring the BIOS

The default BIOS settings may need to be modified to enable or disable various features of the development board. The BIOS settings are configured through a menu-driven user interface which is accessible during the Power On Self Test (POST). Press the **F2** key or **Delete** during POST to enter the BIOS interface.

For AMI BIOS POST codes, visit: http://www.ami.com.

For BIOS updates please contact your Intel Sales Representative or visit http://platformsw.intel.com.

2.8.2 Programming BIOS Using a Bootable USB Device

The flash chips which store the BIOS and BIOS extensions on the development board are connected to the SPI bus and are soldered down with solder. One method of programming these devices is through software utilities as described below. The software files and utilities needed to program the BIOS are contained on the included CD-ROM.

Follow these steps to program the system BIOS using a bootable USB Device:

1. Prepare the workspace as outlined in Section 2.4 above.
2. Setup the system as outlined in Section 2.5 above.
3. Unplug the hard disk drive (HDD) SATA cable from the board at connector J6J3 so that the board will boot from the bootable USB key.
4. Copy the following files and utilities to a Bootable USB Device, preferably a USB flash memory stick.

   BIOS Image Files:

   a. Spifull.bin
   b. BIOS Programming Software Utilities
   c. fpt.exe (DOS SPI Flash Utility)
   d. fparts.txt (helper file)
   e. MAC Address Programming Software Utility
   f. eeupdate.exe
   g. Other helper files contained on the included CD-ROM:
5. Record the 12-digit MAC Address of the board from the sticker near the CPU.
6. Insert the Bootable USB Key into one of the USB Ports on the development board.
7. Switch on the power supply (to "1").
8. Press the Power (PWR) button on the development board.
9. Wait for the system to boot from the USB Key to a DOS prompt.

10. From the DOS prompt (C:>), Run the following:
    a. Fpt-f spifull.bin
    b. Make sure there are no warning signs or errors
11. From DOS, run the following to reprogram the MAC address:
    a. eeupdate /nic=1 /mac= xxxxxxxxxxxx
    b. Where: xxxxxxxxxxxx is the MAC address from the sticker
    c. Make sure there are no warnings or errors.
12. Power the system down by pressing the PWR button.
13. Clear the CMOS by performing the following:
    a. Shunt the CMOS CLR jumper (J5F2 – hear the on-board batter).
    b. Press the PWR button on the board. The board will not power on, but a couple of LEDs will flash.
    c. Switch the power supply off to power down the board.
    d. Remove the CMOS CLR jumper (J5F2).
14. Uplug the bootable USB key.

Verify correct BIOS installation:

1. Switch the power supply back on.
2. Press the PWR button on the board to power-up the system.
3. Boot to BIOS Configuration screen by pressing F2 at the BIOS splash screen.
4. In the BIOS Main screen, check that the "Project Version" lists the correct version of the BIOS.
5. Press the PWR key on the board to power the system back down, or you may simply exit the BIOS menu and continue booting into the operating system.

The BIOS update is now complete; the system is now ready for normal operation.

2.9 Instructions to Flash BIOS on SPI

The Intel® Core™ i5 Processor with Mobile Intel® QM57 Express Chipset Development kit requires the use of a 2-partition SPI image for SPI-0 and SPI-1 respectively. The Descriptors sit on SPI-0 while the BIOS on SPI-1.

1. Remove all the power supplies to the board.
2. Connect the Dedi-prog SF100 at J8E1.
3. Set jumpers J8D1 and J8D2 at 1-2
4. Set jumper J8D3 and J9E2 at 1-2 for SPI-0 and flash the .bin image corresponding to SPI-0.
5. Set the jumper J8D3 at 2-3 and J9E2 at 1-2 for SPI-1 and flash the .bin image corresponding to SPI-1.
6. Set the jumper J9E2 at 2-3 for SPI-1 and flash the .bin image corresponding to SPI-2.
7. Once the programming is successful on the SPI, set J8D1 and J8D2 at 1-X and J8D3 at 1-X and 3-X.
8. Remove the Dediprog connector.

9. Set the SPI.

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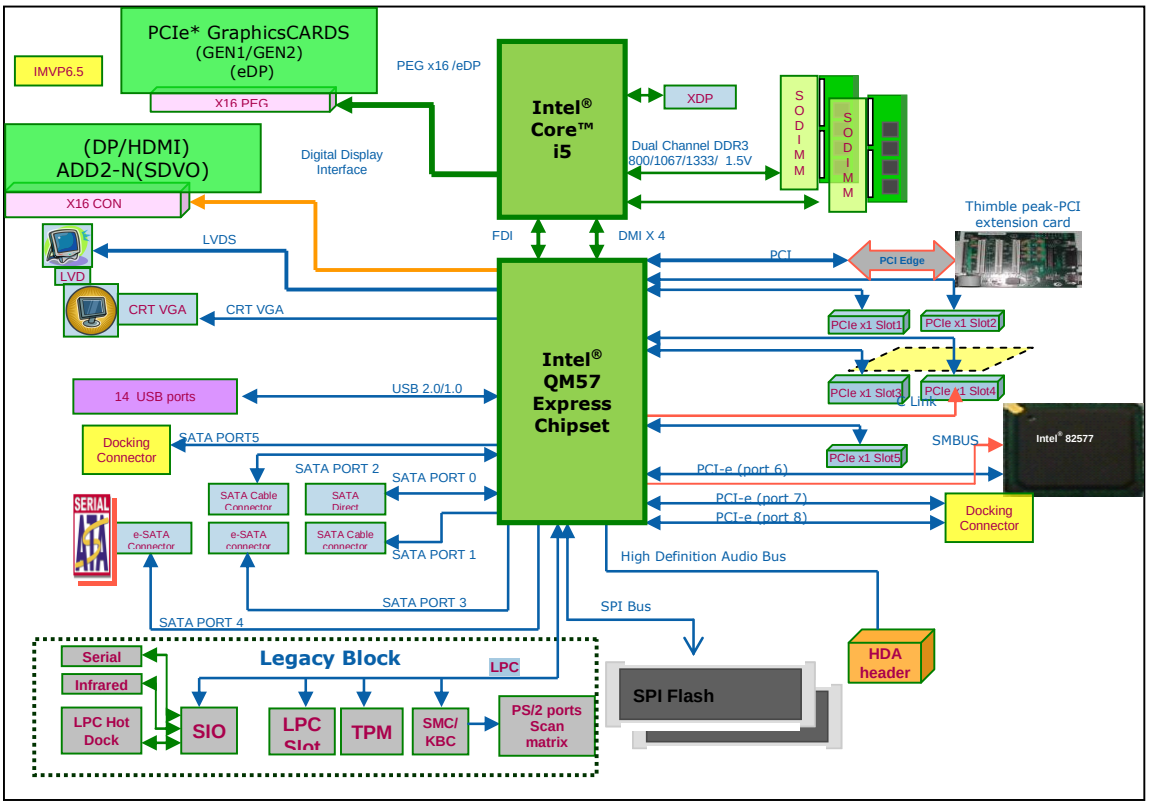
3 Development Board Features

3.1 Block Diagram

The block diagram of the Intel® Core™ i5 Processor with Mobile Intel® QM57 Express Chipset Development kit is shown in Figure 1.

Figure 1. System Block Diagram



3.2 Mechanical Form Factor

The development kit conforms to the ATX 2.2 form factor.

3.3 Development Board Key Features

Development kit features are summarized in Table 5.

Table 5. Platform Feature Summary

	Description	Comments
Processor	Intel® Core™ i5	989-pin rPGA Socket (Socket – G1) Board
Chipset	Mobile Intel® QM57 Express Chipset	1071-pin FCBGA Foot-Print
Memory	2x DDR3 SODIMM slots	Maximum 8 GB using 2-Gb technology and stacked SO-DIMMs Maximum 4 GB using 2-Gb technology and non-stacked SO-DIMMs Supports DDR3 Frequency of up to 1066 MT/s.
External Graphics	1x PCI Express* x16 Graphics Slot	One, x16 PCI graphics slot supported Embedded DisplayPort* (eDP) supported through PCIe graphics 2 add in card.
Video	1x 24-bit dual-channel LVDS Interface	Connectors and cables from previous mobile platforms can be used
Video	DisplayPort	3 – Display port Lanes on chipset: 1 On-Board DP Connector. The other two ports can be supported through PCIe graphics 2 add in card.
Video	HDMI*	1 On-Board HDMI Connector (Optional Routing through Display Port D of Chipset). Three additional HDMI ports are available through the PCIe graphics 2 external card
Video	SDVO	**Port B:** Connected to x16 connector at J8C2. Requires ADD2N add-in card
Video	CRT	1 on-board, right-angled CRT Connector Similar to the earlier platforms
PCI	No slots onboard	PCI Rev 2.3 Specifications at 33 MHz. Only one PCI gold finger on board. 3x 5-V slots supported through PCI Expansion add-in card.
PCI Express	8x PCIe x1 lanes	PCI Express 2.0 Compliance, 2.5GT/s speed. Five lanes to x1 PCIe Ports. One lane to Intel 82577 GbE Controller LAN. Two lanes to docking.

	Description	Comments
On-Board LAN	Intel® 82577 GbE Controller PHY supported	
BIOS (SPI)	2x SPI flash devices	Support for multi-vendor SPI Support multi package (SOIC-8 and SOIC-16)
Soft Audio/ Soft Modem	Intel® High Definition Audio MDC Header	Support via interposer Use Mott Canyon 4 daughter card (support via sideband cable)
ATA/Storage	6x SATA Ports	Two cable connector and one direct connect connector Two eSATA connectors and one to Docking
USB	14x USB 2.0/1.1 Ports	One Quad USB Connector One Dual USB connector on RJ45 8 ports available as FPIOs Optional routing to docking for USB Lane 4. Over current protection provided for pairs. Floater OC7# used as SMC_WAKE_SCI#
LPC	1x LPC Slot	Includes sideband headers
SMC/KBC	H8S/2117 microcontroller Two PS/2 ports One scan matrix keyboard connector	ACPI-compliant
Clocks	CK505 system clock	CRB Supports Buffered mode only
RTC	Battery-backed Real Time Clock	Implementation similar to earlier platforms
Processor Voltage Regulator	Intel® MVP-6.5	Intel MVP 6.5 compliant processor core and graphics core VRs, Manual Override Option for VIDs available on both VR controllers.
Power Supply		ATX Power Supply Support
Debug Interfaces	Processor and PCH XDP Port 80 Display	On board Processor and XDP Ports Port 80 through Add-in card. Four, 7-segment displays
Form Factor	ATX 2.2 form factor	10-layer board – 12” x 9.6”

3.4 Driver Key Features

The driver CD included in the kit contains all software drivers necessary for basic system functionality for various operating systems. The CD contains the production drivers that were released in conjunction with the launch of this platform. However, it is possible that these drivers have been updated since then. Please check for updated drivers at http://platformsw.intel.com.

Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your evaluation kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using the tools that work with Microsoft* products must license those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

3.5 BIOS Key Features

This development kit ships with AMI* BIOS pre-boot firmware from AMI* preinstalled. AMI* BIOS provides an industry-standard BIOS on which to run most standard operating systems, including Windows* XP/XP Embedded, Linux*, and others.

The following features of AMI* BIOS are enabled in the development board:

- DDR3 detection, configuration, and initialization
- Mobile Intel® QM57 Chipset configuration
- POST codes displayed to port 80h
- PCI/PCI Express* device enumeration and configuration
- Integrated video configuration and initialization
- Super I/O configuration
- Intel® Active Management Technology
- Intel® Matrix Storage Manger RAID 0/1 Support

3.6 System Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance and cause reliability problems.

The development kit is shipped with a fan/heatsink assembly thermal solution for installation on the processor. This thermal solution has been tested in an open-air environment at room temperature and is sufficient for development purposes. The

designer must ensure that adequate thermal management is provided for if the system is used in other environments or enclosures.

The fan/heatsink assembly should arrive installed on the board.

3.7 System Features and Operation

The following sections provide a detailed view of the system features and operation of the development kit. The development kit uses the Red Fort board design.

3.7.1 Processor

The development kit uses the Red Fort board design, which supports Intel® Core™ i5 processor in a 989-pin rPGA package (U3E1). This processor is a 2-die package made up of the dual core processor, graphics processor and integrate memory controller.

3.7.1.1 Processor Voltage Regulators

The development kit implements an onboard IMVP-6.5 regulator for the processor core supply, which supports PSI (Power Status Indicator). The maximum current that can be supported by the core VR is 60 Amps.

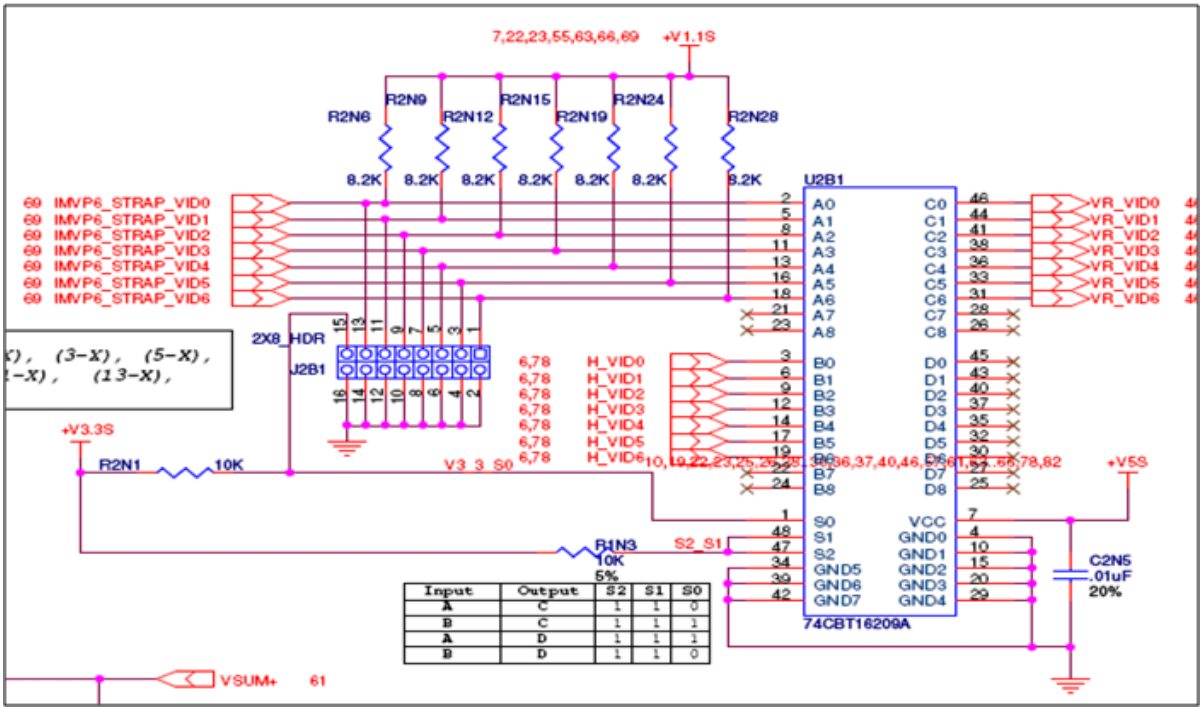
3.7.1.2 Processor Power Management

The processor supports C0, C1 C1E, C3, C6 states. All the power management handshakes occur over the DMI interface. None of the 'Power State' status signals can be observed on the board directly.

3.7.1.3 Manual VID Support for CPU VR

The development kit supports manual VID operation for processor VR. A jumper J2B1<pins 15-16> is provided to enable "VID override" to the CPU VCC core VR. The intent of this "VID override' circuit is for ease of debug and testing. The VID0-VID6 signals of CPU have been brought out from VID0-VID6 pins on the processor package.

Figure 2. VID Override Circuit



Input	Output	S2	S1	S0
A	C	1	1	0
B	C	1	1	1
A	D	1	1	1
B	D	1	1	0

3.7.1.4 Graphics Core VR

The development kit implements an onboard IMVP-6.5 compliant VR controller for the graphics core supply. The maximum current that can be supported by the core VR is 21 Amps.

3.7.1.5 Manual VID Support for Graphics VR

The development kit supports manual VID operation for graphics VR. A jumper J2C1<pins 1-2> is provided to enable "GFX VID override" to the graphics core VR. The intent of this "VID override' circuit is for ease of debug and testing. The implementation is similar to the CPU VR VID over-ride.

3.7.1.6 Memory Support

The development kit supports a dual channel DRR3 interface. There are two DDR3 SODIMM sockets (J4V1 and J4V2) on the motherboard. The memory controller supports four ranks of memory up to 1066MT/s. The maximum amount of memory supported is 8GB of DDR3 memory by utilizing 2Gb technology in stacked SO-DIMMs and 4GB of DDR3 memory by utilizing 2Gb technology in non-stacked SO-DIMMs.

Minimum capacity supported is 512 MB. On-board thermal sensor is provided for the SODIMMs. There is no ECC support on this system.

3.7.1.7 Processor PCI Express* Support (PCI Express Graphics)

The processor supports a PCI Express* port, which can be used for PCI Express Graphics or for PCI Express IO. The development kit supports external graphics through this processor PCIe graphics card slot, and supports Lane-Reversal of the PCIe graphics card lanes. However, the motherboard uses non-reversed routing.

The processor has the capability of using the PCI Express interface in two ways:

- 1x16 PCI Express IO (or PCIe graphics card)
- 2x8 PCI Express IO (or PCIe graphics card)

The 2x8 slots are supported through the Nowata Add-In Card. Embedded Display Port (eDP) is supported through the PCIe Graphics add-in card.

The usage model of the processor's PCI Express interface needs to be configured through the following hardware straps:

Table 6. Hardware Straps for PCI Express* Graphics Interface Usage

STRAP	0	1
CFG0	PCI Express Bifurcation Enabled (STUFF R2R5)	Single PCI Express (default)
CFG4	No Display Port connected to eDP (Default)	An External Display Port is connected (Short J1D1)

3.7.1.8 Embedded DisplayPort

Embedded DisplayPort (eDP) is a feature on Intel® Core™ Processor.

When eDP is enabled, we can only have 1x8 PCIe graphics card. eDP lanes are multiplexed over the PCIe graphics card 12:15 lanes from the processor.

1. Insert the PCIe graphics add-in-card in the PCIe graphics slot (J5C1), not the DDI slot.
2. To enable eDP, you need to "short" the Jumper pins of J1D1 (1-2) on CRB.
3. Connect the side-band signals on J6D1 on CRB, via a cable to J3C1 on the PCIe graphics card.
4. For the sideband signals, there exist two options.
5. Connect J6D1 (on CRB) to J3C1 (on PCIe graphics card FAB 3) through a 10-pin cable.
6. Use the BLI connector from LVDS Connector provided to connect it directly at the eDP Panel.

3.7.1.9 DMI Interface

The Development kit Supports x4 DMI bi-directional lanes between the processor and Mobile Intel® QM57 Express. The transmissions happen over DMI protocol. Max speed supported is 2.5GT/s. This protocol is different from the ones on earlier platforms, and has some instructions added.

3.7.1.10 Intel® Flexible Display Interface (Intel® FDI)

The Development kit supports a new interface: Intel® Flexible Display Interface. On this platform, the GPU is in the processor and display interfaces are supported through Mobile Intel® QM57 Express. The Intel® FDI is a dedicated link to transmit the display related pixel information over unidirectional 2x4 lane interfaces. The synchronization signals are directed from Mobile Intel® QM57 Express Chipset to processor.

3.7.1.11 Processor Thermals

The processor temperature is communicated to the Mobile Intel® QM57 Express Chipset over the PECI, a single wire interface. Some important signals are:

- **CATERR#:** Indicates (asserted low) that the system has experienced a catastrophic error and cannot continue to operate.
- **PROCHOT#:** Active (low) when the processor temperature monitoring sensor detects that the processor has exceeded the thermal specifications.
- **THERMTRIP#:** Assertion (low) indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur.

3.7.1.12 Processor Active Cooling

The development kit supports PWM-based FAN speed control. Fan circuitry is controlled by the signal CPU_PWM_FAN signal from the EC. A 4-pin header J4C1 is provided to support FAN speed output measurement for the CPU.

3.7.2 Chipset Support

The Red Fort board implements the Mobile Intel® QM57 Express Chipset which provides the interface to the processor, DMI, and a highly integrated I/O hub that provides the interface to peripherals. The following sections describe the Mobile Intel® QM57 Express Chipset features:

- 8 x PCI Express* 2.0 specification ports running at 2.5GT/s
- 1 PCI Gold-finger slot (for PCI expansion slots)
- On-board LAN
- 6 x SATA ports
- Support for CRT, LVDS, HDMI, DP and eDP (embedded DP) displays

- 14 x USB ports
- LPC interface
- Serial IrDA port
- Support for two SPI flash devices

Subsystem features described in this section refer to socket and connector locations on the motherboard. Socket and connector locations are labeled with a letter-number combination (for example, the first memory DIMM connector is located at J4V1). Please refer to the silkscreen labeling on the motherboard for socket locations.

3.7.2.1 Chipset PCI Express Support

The development kit supports five on board PCI Express (x1) slots. The Mobile Intel® QM57 Express Chipset has a total of eight PCIe ports (Base Specification, Rev 2.0); five of which are routed to x1 connectors on board; two to docking; and one to LAN. See Table 7.

Table 7. PCI Express* Ports

PCIe* Port	Default Destination	Optional Destination
1	PCIelot 1 (J6C2)	-
2	PCIeSlot 2 (J6D2) (in-line with Slot 1)	-
3	PCIe Slot 3 (J7C1)	-
4	PCIe Slot 4 (J7D2)	-
5	PCIe Slot 5 (J6C1)	-
6	LAN (EU7M1)	-
7	DOCKING (J9C2)	PCIe SLOT6 (J8C1)
8	DOCKING (J9C2)	-

3.7.2.2 PCI Slots

The Intel® Core™ i5 Processor with Mobile Intel® QM57 Express Chipset Development kit does not have any PCI slots on the motherboard. Three 5V PCI slots are supported via PCI expansion card PCI Extension Card.

3.7.2.2.1 Golden Finger

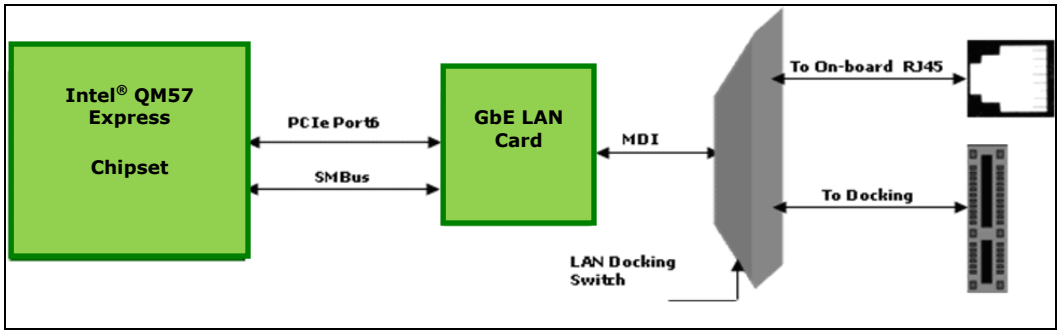
A gold-finger connector (S9B1) is also supplied on the motherboard, which allows for an external PCI expansion board, PCI expansion card. PCI expansion card has three additional PCI slots allowing the user greater expansion.

3.7.2.3 On-board LAN

The Development kit supports 10/100/1000 Mbps Intel® 82577 Gigabit Ethernet Phy (EU7M1) on board. It has a PCIe and SMBus link to the Mobile Intel® QM57 Express Chipset. Routed to Dock via the Docking Switch. Data Transfer happens over PCIe lanes. Communication between the LAN Controller and the LAN Connected Device is done through SMBus whenever the system is in a low power state (Sx). LAN is also supported over DOCKING.

A block Diagram of the implementation is given in Figure 3.

Figure 3. Block Diagram of On-bard LAN Implementation



3.7.2.4 Audio and Modem

Intel® High Definition Audio (Intel® HD Audio) functionality is enabled through the Mott Canyon 4 Daughter Card. An on-board header is provided at J9E7 and J9E4 for this purpose. No direct connection is provided for the Intel® HD Audio Card on the motherboard; the Mott Canyon 4 card is required to enable the Intel® HD Audio functionality.

The motherboard supports low voltage (LV) High definition codecs I/O. R8T2, R8T3 and R8E2, R8T1 resistors are used to select between 3.3V I/O and 1.5VI/O.

Table 8. Selection of I/O Voltage for the Intel® High Definition Audio

I/O Voltage for the Intel® High Definition Audio	STUFF	NO STUFF
3.3V (Default)	R8T2, R8E2	R8T3, R8T1

3.7.2.5 SATA Storage

These connectors mentioned in Table 9 are for the serial data signals. The motherboard has a power connector J8J1 to power the serial ATA hard disk drive. A green LED at CR7G1 indicates activity on the ATA channel.

Table 9. SATA Storage

SATA Port	Connection Type	Connector
Port 0	Direct Connect	J8J1
Port 1 and Port 2	Cable Connect	J7G2 and J7G1
Port 3 and Port 4	eSATA	J6J1 and J7J1

The motherboard shares the power connector for both SATA 1 and 2. Due to this only one of the serial ATA channel (Port1 by default) supports hot swapping capability. Hot swap on Port 1 can be used only when the Port 2 is not used. Y-Power cable needs to be connected first to the device on Port 1 before connecting the signal cable. When hot swap is not desired, both Port 1 and Port 2 can be used. A jumper J9J2 is provided to enable hot plug/removal on port-1.

The eSATA drives should be externally powered. Hence, there is no power supply support for them on the motherboard.

3.7.2.6 USB Connectors

The Mobile Intel® QM57 Express Chipset provides fourteen USB 2.0/1.1 ports:

- Ports 0, 1, 2, and 3 are routed to a four-stacked USB connector (J3A3) at the back panel.
- Two USB ports (8 and 9) are routed to RJ45 + Dual USB Connector J4A1on Back of the Chassis.
- IO headers are provided for the other 8 x USB lanes.

Over current protection has been provided for ports in pairs. Ports (0,1), (1,2)…(12,13) share the OC Indicators.

Table 10. USB Port Mapping

USB Port	Panel	Connector
Port 0	Back Panel I/O Connector	J3A3 (4 stacked USB Connector)
Port 1	Back Panel I/O Connector	J3A3 (4 stacked USB Connector)
Port 2	Back Panel I/O Connector	J3A3 (4 stacked USB Connector)
Port 3	Back Panel I/O Connector	J3A3 (4 stacked USB Connector)
Port 4	FPIO	J8H1 (2x5 Connector)
Port 5	FPIO	J8H1 (2x5 Connector)
Port 6	FPIO	J7H3 (2x5 Connector)
Port 7	FPIO	J7H3 (2x5 Connector)
Port 8	Back Panel	J4A1
Port 9	Back Panel	J4A1 (Rework Required: Stuff R8F3 and R8F5; No Stuff R8F2 and R8F4)

USB Port	Panel	Connector
Port 10	FPIO	J7H4 (2x5 Connector)
Port 11	FPIO	J7H4 (2x5 Connector)
Port 12	FPIO	J7H2 (2x5 Connector)
Port 13	FPIO	J7H2 (2x5 Connector)

3.7.2.7 LPC Super I/O (SIO)/LPC Slot

A SMSC SIO1007 serves as the SIO on the motherboard and is located at U9A1. Shunting the jumper at J8C3 to the 2-3 positions can disable the SIO by holding it in reset. This allows other SIO solutions to be tested in the LPC slot at J8F2. A sideband header is provided at J9G3 for this purpose. This sideband header also has signals for LPC power management.

3.7.2.8 Serial IrDA

The SMSC SIO incorporates a serial port, and IrDA (Infrared), as well as general purpose IOs (GPIO). The Serial Port connector is provided at J2A1, and the IrDA transceiver is located at U6A2. The IrDA transceiver on Red Fort CRB supports SIR (slow IR), FIR (Fast IR) and CIR (Consumer IR). The option to select between these is supported through software and GPIO pin (IR_MODE) on the SIO.

3.7.2.9 System Management Controller (SMC)/Keyboard Controller (KBC)

A Renesas* H8S/2117 (U9H1) serves as both SMC and KBC for the platform. The SMC/KBC controller supports two PS/2 ports, battery monitoring and charging, wake/runtime SCI events, CPU thermal monitoring/Fan control, GMCH thermal throttling support, LPC docking support and power sequencing control.

The two PS/2 ports on the motherboard are for legacy keyboard and mouse. The keyboard plugs into the bottom jack and the mouse plugs into the top jack at J1A1. Scan matrix keyboards can be supported via an optional connector at J9E3.

There is a LPC Slot (J8F2) and LPC Sideband connector (J9G2) on the motherboard to connect external EC for validation purposes. On-board EC has to be disabled by shorting pin 1 and 2 of connector J9F2 and external EC has to take care of board power sequencing and thermal management.

If the intension is to read thermal information from the Mobile Intel® QM57 Express Chipset by external EC/Fan controller, only Mobile Intel® QM57 Express Chipset SM-Bus signals (SML1_CLK and SML1_DATA) from the LPC sideband connector can be used without connecting the EC on LPC slot.

For more information on the embedded controller please refer to *Intel® Management Engine (Intel® ME) and Embedded Controller Interaction for Calpella Platform*.

3.7.2.10 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) on Mobile Intel® QM57 Express Chipset can be used to support two compatible flash devices (U8C1 and U8D1), storing Unified BIOS Code. The SOIC-8 package (U8D2 & U8C2) would support 16 Mb SPI flashes, while the SOIC-16 (U8C1 and U8D1) package will support 32Mb or higher SPI flash. One can opt to use SPI sockets, if they wish to. Socket KOZ has been taken into account in the layout. A Dedi-Prog Header (J8E1) has been provided for SPI programming.

Out of the SOIC-8 and SOIC-16 footprints supported on the board only one of these can be used at a time and on the board. Footprint is arranged one over the other. By default, U8C1 (16Mb on CS#0) and U8D1 (16Mb on CS#1) will be stuffed.

Table 11. Jumper Setting for SPI Programming

MODE	J8D1	J8D3	J8D2
Normal Operation	1-X	1-X 3-X	1-X
Programming SPI0	1-2	1-2 3-X	1-2
Programming SPI1	1-2	1-X 2-3	1-2

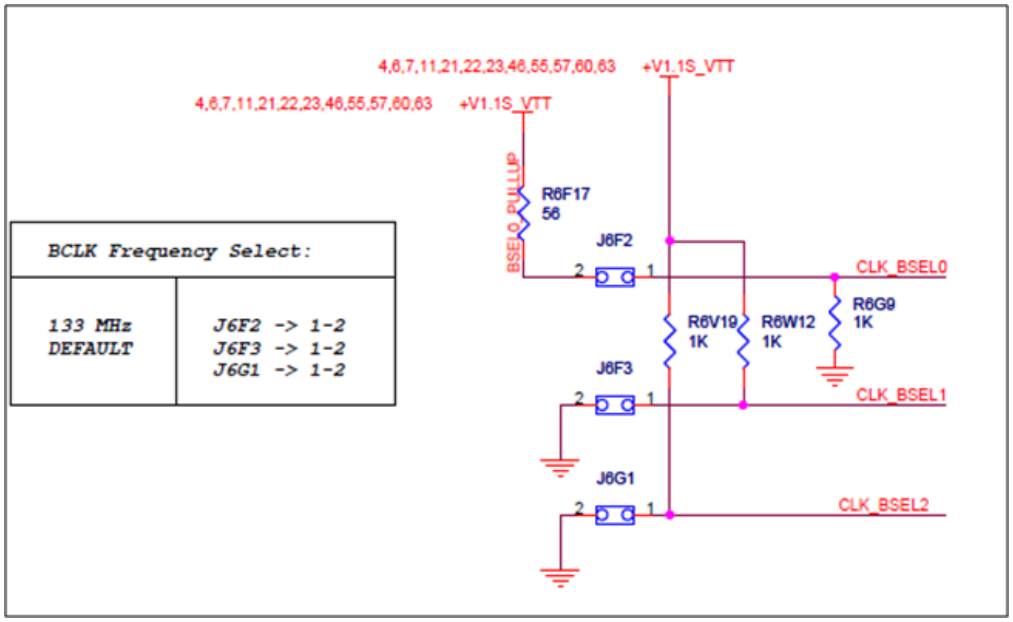
3.7.2.11 Clocks

The development kit system clocks are provided by the CK505 (EU6V1) clock synthesizer.

The BCLK frequency can be set using the BSEL Jumpers J6G1, J6F2, J6F3. Unlike previous platforms it always needs to be 133MHz.

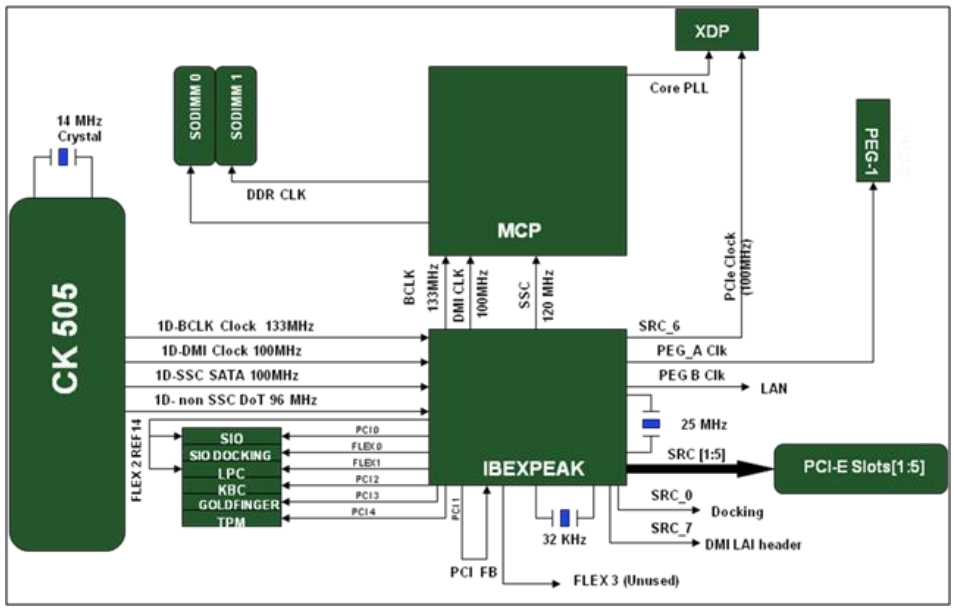
CPUSTP# is not supported as the requirement is to have this clock always running during buffered mode.

Figure 4. Jumpers for CLK_BSEL Signals



The clocks on the CRB are provided by the Mobile Intel® QM57 Express Chipset which uses four clocks from CK505 as inputs and use these as a reference to generate all the other platform clocks. A general block diagram is shown in Figure 5.

Figure 5. Platform Clocking Circuit



The development kit also supports clocks directly off the CK505, should there be a problem with the Mobile Intel® QM57 Express Chipset clock synthesizer, which can be done by changing a few resistor stuffing options. Table 12 provides the rework instructions to move from buffered or integrated clock modes to the "back-up" mode, in which CK505 sources all platform clocks.

Table 12. Rework to Move From Integrated Clock Mode to Back-up Mode

	Destination	Rework involved	
		NO STUFF	STUFF
1	PROCESSOR: BCLK	R4T7, R4T8 R6W13, R6W14	R6W16, R4T6 R6W15, R4T9
2	PROCESSOR: PCIE GRAPHICS CARD CLK	R4T2, R4T5 R6V2, R6V3	R6V4, R4T3 R6V1, R4T4
3	XDP: BCLK	R1R7, R1R14	R6W6, R6W7
4	PCIE- SLOT1	R6C5, R6C6	R6C4, R6C7 R6V12, R6V13
5	PCIE-SLOT2	R6R5, R6R6	R6R4, R6R3 R6W2, R6W3
6	PCIE-SLOT3	R7C10, R7C11	R7C8, R7C9 R6W4, R6W5

7	PCIE-SLOT4	R7R8, R7R9	R7R7, R7R6 R5V15, R5V17
8	PCIE-SLOT5	R7C4, R7C5	R7C6, R7C7 R5G13, R5G14
9	PCIE GRAPHICS CARD SLOT	R5C9, R5C10	R5C13, R5C8 R6V10, R6V11
10	PCI SIO	R7T23	R7T17, R6V9
11	PCI LPC	R7T27	R7T16, R6V8
12	PCI KBC	R7T22	R7T15, R6V20
13	PCI GOLDF	R7T19	R7T13, R6V7
14	PCI TPM	R7T24	R7T18, R6V6
15	REF14 SIO	R7E6	R7E3, R6W1

3.7.2.12 Real Time Clocks (RTC)

An on-board battery at BT5G1 maintains power to the real time clock (RTC) when in a mechanical off state. A CR2032 battery is installed on the motherboard.

3.7.3 Displays

The development kit supports the following displays:

- **CRT:** A right-angled CRT connector is provided on-board (J1A2). Optional routing to the docking connector is supported through a CRT dock switch (U6C1).
- **LVDS:** LVDS support is very similar to that used on earlier platforms. Connector is at J7D3.
- **HDMI:** An HDMI connector (J3A2) is added on-board for the first time. HDMI connectors are also available on PCIe graphics 2 Add-In Card.
- **DP:** A DP connector (J5A1) has been added on board for the first time. DisplayPort connectors are also available on PCIe graphics 2 Add-In Card.
- **eDP (Embedded DP):** eDP is available on the PCIe graphics 2 Fab 3 Add-In Card. When used for eDP, this card needs to be inserted in the PCIE GRAPHICS CARD Slot (J5C1) and not in the DDI Slot (J8C2). A 2x5 header (J6D1) is provided for the side-band signals (backlight related information and SMBus access).
- **SDVO:** SDVO can be configured only on Port B.
  - A maximum of two displays can be active at a time.
  - Display connectors DP/HDMI are on Port D of the Mobile Intel® QM57 Express Chipset, Port B and C can be used through PCIe graphics 2 FAB 3 Add-In Card.

One DP and one HDMI Connector have been provided on board on the Red Fort CRB.

1. Port D of Digital Display Interface on PCH is mapped to on board DP and HDMI connectors.
2. DP is the default configuration. To select HDMI rework is required on the CRBs.
3. For HDMI:
   a. No stuff – C5A1, C5A2, C5A13, C5A14, C5A5, C5A6, C5A9, C5A10
   b. Stuff – C5A3, C5A4, C5A15, C5A16, C5A7, C5A8, C5A11, C5A12 with 0402 0.1 µF capacitor
   c. The same capacitors no stuffed in Step A can be used in Step B
      i. R2M2 and R2M5 are the 2.2k pull-ups on SMBus. These should be changed to 4.4 k.
      ii. For HPD: Stuff R5A1 with 0 or HPD: Stuff R5A1.

3.7.3.1 Digital Display Interface Configuration Modes

- 3x DisplayPorts
- 3x HDMI/DVI Ports
- 2x DP + 1x SDVO
- 2x DP + 1x HDMI/DVI
- 2x HDMI/DVI + 1x SDVO
- 2x HDMI/DVI + 1x DP
- 1x DP + 1x HDMI/DVI + 1x SDVO

3.7.4 Debugging Interfaces

3.7.4.1 Processor Debug

An XDP (Extended Debug Port) connector is provided at J1D3 for processor run control debug support. An additional MANARA Connector is also provided for processor debug.

A port 80-83 display add-in card can also be used for debug. The port 80-83 add in card could be used on the TPM header located at J9A1.

3.7.4.2 Chipset Debug

An XDP Connector is provided at J8H3, for Mobile Intel® QM57 Express Chipset Debug support.

3.7.5 Power Management

3.7.5.1 Power Management States

Table 13 lists the power management states. The Controller Link (CL) operates at various power levels, called M-states. M0 is the highest power state, followed by M1 and M-off.

Table 13. Power Management States

State	Description
G0/S0/C0	Full on
G0/S0/C3	Deep Sleep: CPUSTP# signal active
G1/S3	Suspend To RAM (all switched rails are turned off)
G1/S4	Suspend To Disk
G2/S5	Soft Off
G3	Mechanical Off

3.7.6 Power Measurement Support

Power measurement resistors are provided on the platform to measure the power of most subsystems. All power measurement resistors have a tolerance of 1%. The value of these power measurement resistors are 2mOhm by default. Power on a particular subsystem is calculated using the following formula:

Equation 1. Power Calculation

$$P = \frac{V^2}{R}$$

R = value of the sense resistor (typically 0.002Ω)

V = the voltage difference measured across the sense resistor.

It is recommended that the user use a high precision digital multimeter tool such as the Agilent* 34401A digital multi-meter. Refer to Table 14 for a comparison of a high precision digital multimeter (Agilent 34401A) versus a standard precision digital multi-meter (Fluke* 79).

Table 14. Digital Multimeter

EXAMPLE SYSTEM			
Sense Resistor Value:		0.002Ω	
Voltage Difference Across Resistor:		1.492mV (746mA)	
Calculated Power:		1.113mW	
Agilent* 34401A (6.5-digit display)		Fluke* 79 (3-digit display)	
Specification:	(±0.0030% of reading) + (±0.0030% of range)	Specification:	±0.09% ±2 digits
Min Voltage Displayed: Calculated Power:	1.49193mV 1.1129mW	Min Voltage Displayed: Calculated Power:	1.47mV 1.08mW
Max Voltage Displayed: Calculated Power:	1.49206mV 1.1131mW	Max Voltage Displayed: Calculated Power:	1.51mV 1.14mW
Error in Power:	**±0.009%**	**Error in Power:**	**±0.3%**

Table 14 shows the precision achieved by using a high precision digital multimeter versus a standard digital multimeter is ~33 times more accurate.

The Power Measurement resistors provided for the various rails are in Table 15.

Table 15. Power Measurement Resistor for Power Rails

Voltage Rail Name	REFDES of the Power Measurement Resistor
GVR_VBAT	R1E2
+VGFX_CORE	R2D11
+VDC_PHASE	R3B23
+V1.1S_PCH_VCC	R6U15
MAX8792_V1.1SVTT_LX_L	R4F1
MAX8792_V1.1M_LX_L	R6E8
+V5S_HDMID_OB	R2A2
1.5_VIN	R3W26
+V1.1S_VCCTTA_QPI	R3T2
+V1.5_DIMM1	R3G2
+V1.5_DIMM0	R3G1

Voltage Rail Name	REFDES of the Power Measurement Resistor
+V3.3S_DP_OB	R5N1
+VBATA	R3W23
+V1.5_VCCDDQ	R3U2
+V1.1S_VCCTTA_DDR	R3T4
+V5A_USBPWR_IN	R3A1
+V1.5_L_R	R4G8
+V1.1S_VCC_SA	R4R7
+V3.3A_MBL	R4H1
+V1.8S_VCCSFR	R4R2
MAX8792_V1.1SVTT_VIN	R4G1
+V1.1S_VCCTT	R4T1
-V12A	R4H7
+V1.1S_VCC_FDI	R4R3
+V5SB_ATXA	R4H8
+V1.1S_VCC_PCIE GRAPHICS CARD_DMI	R4R4
+V1.8S	R5E1
+V12S_PCIE GRAPHICS CARD	R5N2
+V3.3S_PCIE GRAPHICS CARD	R5C2
62290_VIN	R5E5
+V12S_SATA_P1	R5W9
+V3.3S_PCIESLOT2	R6P1
+V3.3S_PCIESLOT1	R6B5
+V12S_PCIESLOT1	R6B2
+V12S_PCIESLOT5	R6N1
MAX8792_V1.1M_VIN	R6T4
+V5S_LVDS_BKLT	R7D11
+V3.3_PCIESLOT3	R7C1
+V3.3_PCIESLOT4	R7R2
+V12S_PCIESLOT3	R7N1
+V3.3S_PCIESLOT5	R7B6
+V3.3M_LAN	R7A1

Voltage Rail Name	REFDES of the Power Measurement Resistor
+V3.3S_LVDS_DDC	R7R12
+V12S_PCIESLOT4	R7P5
+V5S_SATA_P1	R7W1
+V1.1M_VCCEPW	R7T26
+VDD_VDL	R7D3
+V3.3S_1.5S_HDA_IO	R8R9
+VCC_LVDS_BKLT	R8D1
+V3.3S_PCIESLOT6	R8C1
+V12S_PCIESLOT6	R8B1
+V5_LPCSLOT	R8T8
+V5_PS2	R8N1
+V3.3_LPCSLOT	R8U1
+V3.3A_1.5A_HDA_IO	R8R11
+V3.3A_KBC	R8H13
+V3.3S_VCCPPCI	R8U3
+V3.3M_SPI	R8R5
+V3.3S_IR	R8M4
+V3.3S_DPS	R8B4
+V12S_DPS	R8N4
+V5S_SATA_P0	R8H15
+V12S_SATA_P0	R8W23
+V3.3S_SATA_P0	R8Y1
+V12S_PCI	R9N1
+V3.3S_PCI	R9E1
+V5S_PCI	R9B5
+V5_R1_TPM	R9M6
+V3.3S_R1_TPM	R9M8
+V3.3A_R1_TPM	R9M9
+V0.75S_R	R3W19
51125_V3.3A_VBATA	R4V11
+VDDIO_CLK	R5H1
51125_V5A_VBATA	R5W1

Voltage Rail Name	REFDES of the Power Measurement Resistor
+V5A_MBL	R5H4
+V12S_PCIESLOT2	R6C14
+V3.3S_NVRAM	R6V18
+VDD_CK505	R6W17
+V3.3S_SATA_P1	R6W18
+V1.1S_VCC_SATA	R7V2
+V3.3S_SIO	R9M10
+V3.3_KBCS	R9E6
51125_VIN	R5G6
+V5S_IMVP6	R3B20
+V3.3S_DIMM1	R2G15
+V3.3S_DIMM0	R2G4
+V1.1S_VCC_DMI	R6U19
+VCCAPLL_FDI_L	R6F20
+VCCA_DPLL_L	R6E9
+V3.3S_VCCA3GBG	R6U10
+V3.3S_CRT_VCCA_DAC	R7E15
+V3.3M_VCCPEP	R7U17
+V_NVRAM_VCCPNAND	R7V1
+V1.0M_LAN	R7A8
+V3.3A_VCCPUSB	R7F3
+V1.1S_VCCA_CLK_R	R7E9
+V1.5S_1.8S_VCCADMI_VRM	R6U11
+VCCAFDI_VRM	R6U13
+VCCPLLVRM	R6U14
+V1.1S_VCCAPLL_L	R6G5
+V1.1S_PCH_VCCDPLL_EXP	R6U16
+V1.1S_VCCPCPU	R6U17
+V1.1S_VCCDPLL_FDI	R6F14
+V3.3M_LAN_OUT_R	R7A10
+V1.1S_VCCUSBCORE	R7F4

Voltage Rail Name	REFDES of the Power Measurement Resistor
+V1.8S_VCCTX_LVD	R7T33
+V3.3S_VCCA_LVD	R7U1
+V3.3S_VCC_GIO	R7U2
+V1.1S_SSCVCC	R7T14
+V3.3A_1.5A_VCCPAZSUS	R7U8
+V1.1M_VCCAUX	R7U9
+V3.3S_VCCPCORE	R7U11
+V3.3A_VCCPSUS	R8F12

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4 Development Board Physical Hardware Reference

This section provides reference information on the physical hardware, including component's locations, connector pinout information and jumper settings.

4.1 Primary Features

Figure 6 and Figure 7 show the components on the motherboard, top and bottom views, respectively. Table 16 gives a brief description of each component.

Figure 6. Top View: Component Locations

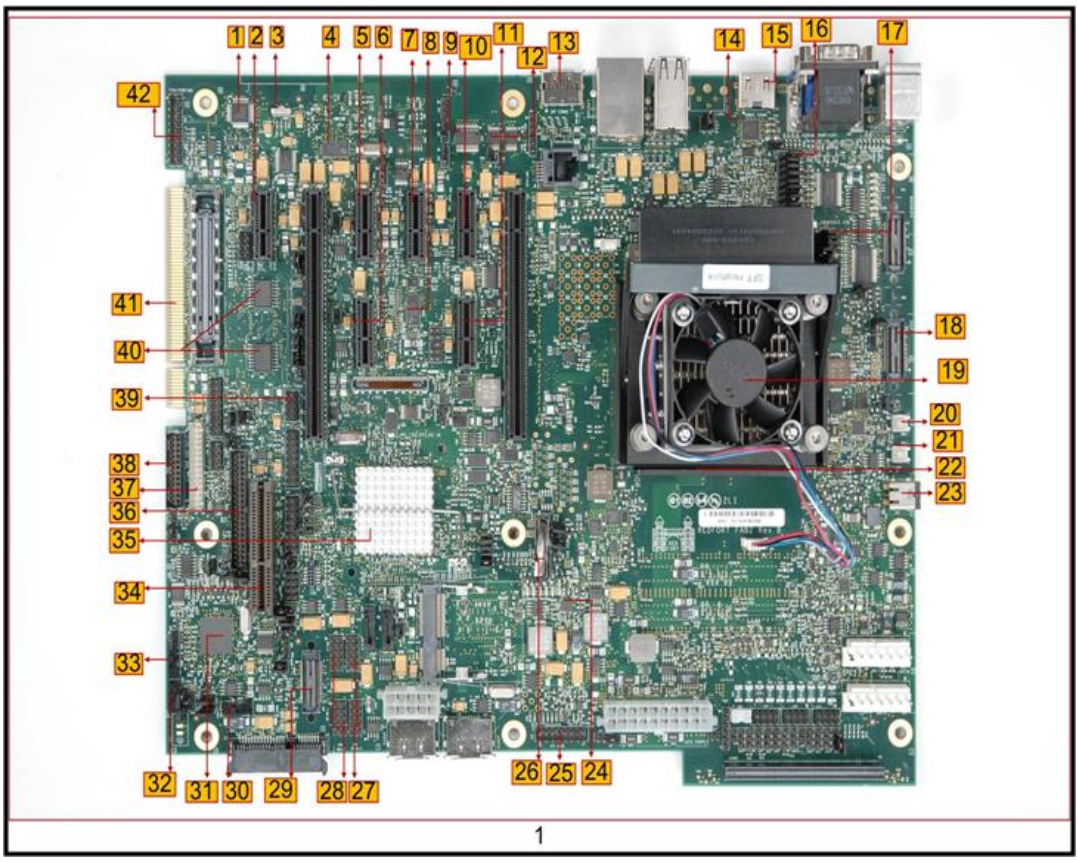

Figure 7. Bottom View: Component Locations

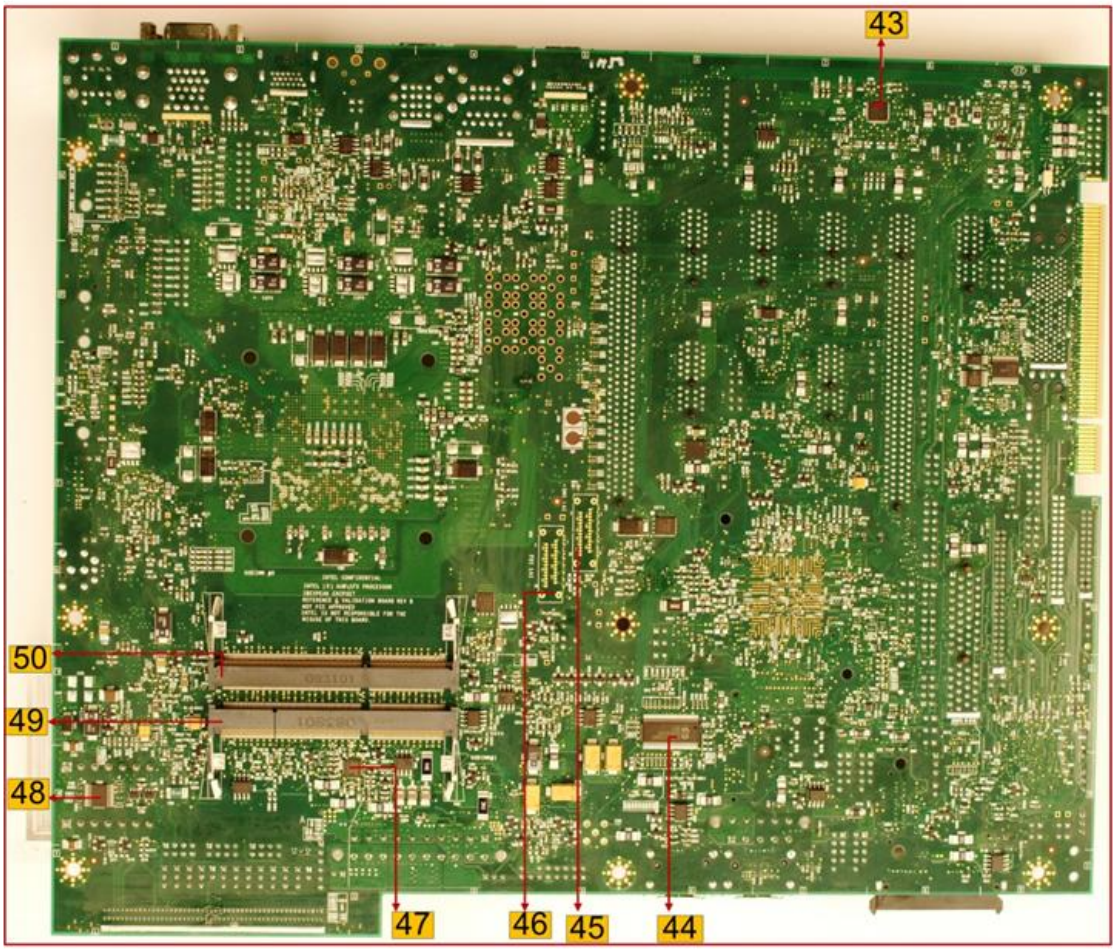

Table 16. Component Location

Ref. No.	Description
1	SMSC IO
2	PCI-e* Slot 6 (No_Stuff)
3	Infra red port
4	LAN Docking switch
5	PCI-e Slot3
6	PCI-e Slot 4
7	PCI-e Slot 5
8	DP Docking Switch

Ref. No.	Description
9	RS232 Transceiver
10	PCI-e Slot 1
11	PCI-e Slot 2
12	Intel 5 Series Chipset JTAG Buffers
13	Onboard display port
14	HDMI LVL translator
15	Onboard HDMI port
16	CPU core VID Override jumper
17	GFx core VID Override jumper
18	Arrandale XDP
19	CPU heatsink on top of Arrandale
20	Power Button
21	Reset button
22	Arrandale
23	AC Jack
24	System VR
25	Front Panel Header
26	RTC Battery holder
27	USB FPIOs
28	USB FPIOs
29	Mobile Intel® QM57 Express Chipset XDP
30	Virtual Battery Switch
31	EC/KSC
32	Lid Switch
33	Virtual docking Switch
34	LPC Slot
35	Mobile Intel® QM57 Express Chipset
36	LPC side band
37	Scan Matrix
38	LPC Hot Dock
39	SPI Programming Header
40	SPI Devices

Ref. No.	Description
41	PCI gold finger
42	TPM Header
43	Hanksville LAN Phy
44	CK 505
45	DMI LAI
46	FDI LAI
47	DDR3 VR
48	I2C Port Hub
49	DDR Channel 1
50	DDR Channel 0

4.2 Connectors

Many of the connectors provide operating voltage (+5 V DC and +12 V DC, for example) to devices inside the computer chassis, such as fans and internal peripherals. Most of these connectors are not over-current protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves. This section describes the board's connectors.

Table 17 lists the connectors on the motherboard.

Table 17. Connectors on Red Fort CRB

#	Reference Designator	Description
1	J8C2	Mobile Intel® QM57 Express Chipset DDI port x16 connector
2	J5C1	PCIE GRAPHICS CARD connector
3	J5B1	Mobile Intel® QM57 Express Chipset JTAG Header
4	J4A1B	RJ45 USB connector
4	J3A3	Quad USB connector
6	J1A1	PS/2 Keyboard/mouse connector
7	J1H1	Battery A connector
8	J1H2	Battery B connector
9	J3J1/J2J1	12C Connectors
10	J4H1	ATX Power Supply connector
11	J6J1	eSATA connector 1

12	J7J1	eSATA connector 2
13	J8J1	SATA Direct connect
14	J7D3	LVDS connector
15	J9E4/ J8F1	HAD connector
16	J9C2	Docking connector
17	J9C1	UPEK FPS header
18	U3E1C	DDR Channel 1
19	U3E1D	DDR Channel 2

Figure 8 . Back Panel Connector Locations

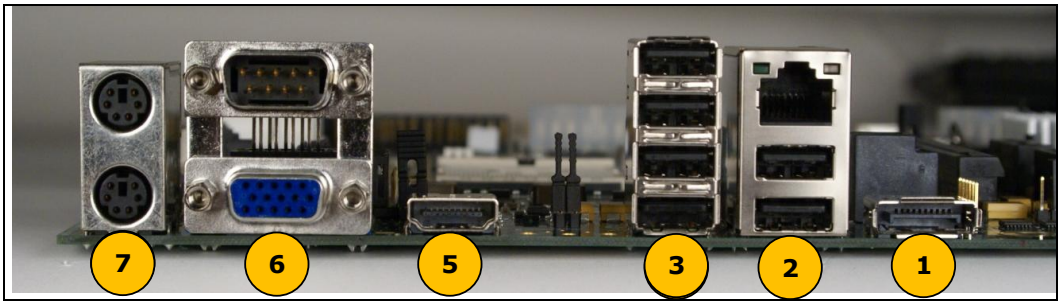

Table 18. Back Panel Connector Locations

Item	Description	Ref Des
1	Display Port	J5A1
2	RJ-45 (top) & 2 USB	J4A1
3	Quad-stack USB	J3A3
4	DP Connector	J3A1
5	HDMI Connector	J3A2
6	RS-232 (top) & CRT	J2A1
7	PS2 (mouse on top)	J1A1

4.3 Configuration Settings

Warning: Do not move jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumper settings. It may damage the board.

Table 19. Configuration Jumper/Switches Settings

#	Reference Designator	Description	Default Setting
1	J4B1	ON BOARD DDR3 THERMAL SENSOR	(1-2)
2	J4B2	ON BOARD DDR3 THERMAL SENSOR	(1-2)
3	J1D1	DISPLAY PORT PRESENT	(1-X)
4	J1J2	PM_EXTTS CONTROLLER	(2-3)
5	J5F2	CMOS SETTING	(1-X)
6	J5F1	TPM SETTING	(1-X)
7	J9E1	TPM FUNCTION	(1-X)
8	J9G4	NO REBOOT	(1-X)
9	J6B1	PCH_JTAG_RST#	(1-X)
10	J6E1	MPC Switch Control	(1-X)
11	J9E6	BBS Strap	(1-X)
12	J8F3	Configurable CPU Output Buffer	(1-X)
13	J8F7	CRB/SV DETECT	(1-X)
14	J8G1	BIOS RECOVERY	(1-X)
15	J2A1	HDMI LEVEL SHIFTER ENABLE	(1-2)
16	J7B2	PCIE SLOT 3 POWER CONTROL	(2-3)
17	J7D1	PCIE SLOT 4 POWER CONTROL	(2-3)
18	J9H5	SATA DEVICE STATUS	(1-2)
19	J9G3	PLL ON DIE VOLATAGE REGULATOR ENABLE	(1-X)
20	J7H1	SATA HOT PLUG REMOVAL DEFAULT SUPPORTED	(1-2)
21	J9H3	SATA DEVICE STATUS	(1-2)
22	J8D1	SPI PROGRAMMING (REFER SCHEMATIC FOR OTHER OPTIONS)	(1-X)
23	J8D3	SPI PROGRAMMING (REFER SCHEMATIC FOR OTHER OPTIONS)	(1-X)
24	J8D2	SPI PROGRAMMING (REFER SCHEMATIC FOR OTHER OPTIONS)	(1-X)
25	J9E2	SPI PROGRAMMING (REFER SCHEMATIC FOR OTHER OPTIONS)	(1-2)
26	J6F2	FSB FREQUENCY SELECTION	(1-2)
27	J6F3	FSB FREQUENCY SELECTION	(1-2)
28	J6G1	FSB FREQUENCY SELECTION	(1-2)

#	Reference Designator	Description	Default Setting
29	J8C3	SIO RESET	(1-2)
30	J7B1	RS232 PORT FOR EC FIRMWARE DEBUG	(1-X)
31	J6A3	IN CKT H8 PROGRAMMING	(1-2)
32	J6A2	IN CKT H8 PROGRAMMING	(1-2)
33	J8G5	H8 MODE SELECTION	(1-2)
34	J8G4	H8 MODE SELECTION	(1-X)
35	J9F2	SMC/KSC	(1-X)
36	J8G6	KBC CORE DEBUG	(1-X)
37	J9F1	THERM STRAP	(1-X)
38	J9H1	SWITCHABLE GFX	(1-2)
39	J9H4	SMC LID	(1-X)
40	J9H2	VIRTUAL BATTERY	(1-X)
41	J9G1	BOOT BLOCK PROGRAMING	(1-2)
42	J1C2	GFX VR ENABLE	(1-X)
43	J4J1	G3 SUPPORT	(1-X)
44	J1F1	FORCE POWER UP VBAT	(1-X)
45	J1E1	FORCE SHUT DOWN	(1-X)
46	J1D2	DFT STRAP ENABLE	(1-X)
47	J8H4	SATA OB ANALYSIS	(1-X)

A jumper consists of two or more pins mounted on the motherboard. When a jumper cap is placed over two pins, it is designated as 1-2. When there are more than two pins on the jumper, the pins to be shorted are indicated as 1-2 (to short pin 1 to pin 2), or 2-3 (to short pin 2 to pin 3). When no jumper cap is to be placed on the jumper, it is designated as 1-X.

4.4 Power On and Reset Push Buttons

The motherboard board has two push-buttons, POWER and RESET. The POWER button releases power to the entire board causing the board to boot. The RESET button forces all systems to warm reset. The two buttons are located near the CPU (Marked as #3 in Table 20) close to the East-edge of the board. The POWER button is located at SW1E1 (Marked as #1 in Table 20) and the RESET button is located at SW1E2 (Marked as #2 in Table 20).

Table 20. Power On and Reset Push Buttons

Item	Description	Ref Des
1	Power Button	SW1E1
2	Reset Button	SW1E2
3	CPU	U3E1

4.5 LEDs

The following LEDs in Table 21 provide status of various functions:

Table 21. Development Kit LEDs Description

Function	Reference Designator	Page# on the Schematics for reference
SATA ACTIVITY	CR7G1	16
MPC ON/OFF Indicator	CR6D1	18
BRAIDWOOD R/B#	CR7G2	27
VID0	CR1B1	46
VID1	CR1B2	46
VID2	CR1B3	46
VID3	CR1B4	46
VID4	CR1B5	46
VID5	CR1B6	46
VID6	CR1B7	46
NUM LOCK	CR9G2	47
CAPS LOCK	CR9G3	47
SCROLL LOCK	CR9G1	47
S4	CR5G6	65
S5	CR5G7	65
M0/M3	CR5G3	65
S3 COLD	CR5G5	65
S0	CR5G4	65
DSW	CR5G2	65
SYSTEM POWER GOOD	CR5G8	65

Note: Some LED Silk screens may not be correct

4.6 Other Headers

4.6.1 H8 Programming Header

The microcontroller firmware for system management/keyboard/mouse control can be upgraded in two ways. The user can either use a special DOS* utility (in-circuit) or use an external computer connected (remote) to the system via the serial port on the board.

If the user chooses to use an external computer connected to the system via the serial port, there are four jumpers that must be set correctly first. Please refer to Table 10 for a summary of these jumpers.

Required Hardware: one Null Modem Cable and a Host Unit with a serial COM port (System used to flash the SUT)

Here is the sequence of events necessary to program the H8:

1. Extract all files (keep them in the same folder) to a single directory of your choice on the host machine or on a floppy disk (recommended).
2. Connect a NULL modem cable to the serial ports of each platform (host and unit to be flashed).
3. Boot host in DOS mode.
4. Set the jumpers on the motherboard as in Table 13.
5. Power on the motherboard and press the PWR button.
6. From the host directory where you extracted the files, run the following command line:
   ```
   KSCFLAxx ksc.bin / Remote
   ```
   Where xx refers to the KSC flash utility version number.
7. This file will program ksc.bin to the KSC flash memory through the remote (Null modem cable).
8. Follow the instructions the flash utility provides.
9. After successful programming of the KSC, switch-off the system power and move all three jumpers back to their default setting. The program assumes the host computer is using serial port 1.

Make sure the board is not powered on, and the power supply is disconnected before moving any of the jumpers.

Table 22. H8 Programming Jumpers

Signals	SMC_INITCLK (H8 NMI)	Serial Port (TXD)	Serial Port (RXD)
Jumper setting	Open (Default: 1-2)	Short pin 2 and 3 (Default: 1-2)	Short pin 2 and 3 (Default: 1-2)
Red Fort CRB	J7B1	J6A2	J6A3

4.7 Default Jumper Configuration

The jumper pins that need to be shorted by default are listed in Table 23.

Table 23. Default Jumper Configuration

#	Reference Designator	Description	Default Setting
1	J4B1	ON BOARD DDR3 THERMAL SENSOR	(1-2)
2	J4B2	ON BOARD DDR3 THERMAL SENSOR	(1-2)
3	J1J2	PM_EXTTS CONTROLLER	(2-3)
4	J2A1	HDMI LEVEL SHIFTER ENABLE	(1-2)
5	J7B2	PCIE SLOT 3 POWER CONTROL	(2-3)
6	J7D1	PCIE SLOT 4 POWER CONTROL	(2-3)
7	J9H5	SATA DEVICE STATUS	(1-2)
8	J7H1	SATA HOT PLUG REMOVAL DEFAULT SUPPORTED	(1-2)
9	J9H3	SATA DEVICE STATUS	(1-2)
10	J9E2	SPI PROGRAMMING (REFER SCHEMATIC FOR OTHER OPTIONS)	(1-2)
11	J6F2	FSB FREQUENCY SELECTION	(1-2)
12	J6F3	FSB FREQUENCY SELECTION	(1-2)
13	J6G1	FSB FREQUENCY SELECTION	(1-2)
14	J8C3	SIO RESET	(1-2)
15	J6A3	IN CKT H8 PROGRAMMING	(1-2)
16	J6A2	IN CKT H8 PROGRAMMING	(1-2)
17	J8G5	H8 MODE SELECTION	(1-2)
18	J9H1	SWITCHABLE GFX	(1-2)
19	J9G1	BOOT BLOCK PROGRAMING	(1-2)

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5 Rework Instructions

The sections below list the re-works needed for the development kit's Red Fort motherboard.

5.1 Simultaneous M1 and M3 VREF

Rework the instructions for supporting M1 and M3 VREF options simultaneously.

5.1.1 DDR3 Channel 0 Reworks

1. NO_STUFF R2F6
2. NO_STUFF R5H12
3. Change R2F5 to 0 Ω (RESD, 0402, 5%, 1/16 W,0)
4. Change R2F7 to 1-kΩ (RESD, 0402, 1%, 1/16 W,1 kΩ)
5. Change R2F10 to 0 Ω (RESD, 0603, 5%, 1/16 W,0)
6. Change R2G21 to 0 Ω (RESD, 0603, 5%, 1/16 W, 0)
7. Change C2F6 to 1-kΩ resistor (RESD,0402,1%,1/16 W,1 kΩ)

5.1.2 DDR3 Channel 1 Reworks

1. NO_STUFF R2U13
2. NO_STUFF R5W3
3. Change R2U12 to 0 Ω (RESD, 0402, 5%, 1/16 W, 0)
4. Change R2U14 to 1-kΩ (RESD, 0402, 1%, 1/16 W, 1 kΩ)
5. Change R2U17 to 0 Ω (RESD, 0603, 5%, 1/16W, 0)
6. Change R2G22 to 0 Ω (RESD, 0603, 5%, 1/16W, 0)
7. Change C2U9 to 1-kΩ resistor (RESD, 0402, 1%, 1/16 W, 1 kΩ)

Rework locations for the top and bottom views of the Red Fort CRB are shown in Figure 9 and Figure 10.

Figure 9. Red Fort Motherboard: Top View

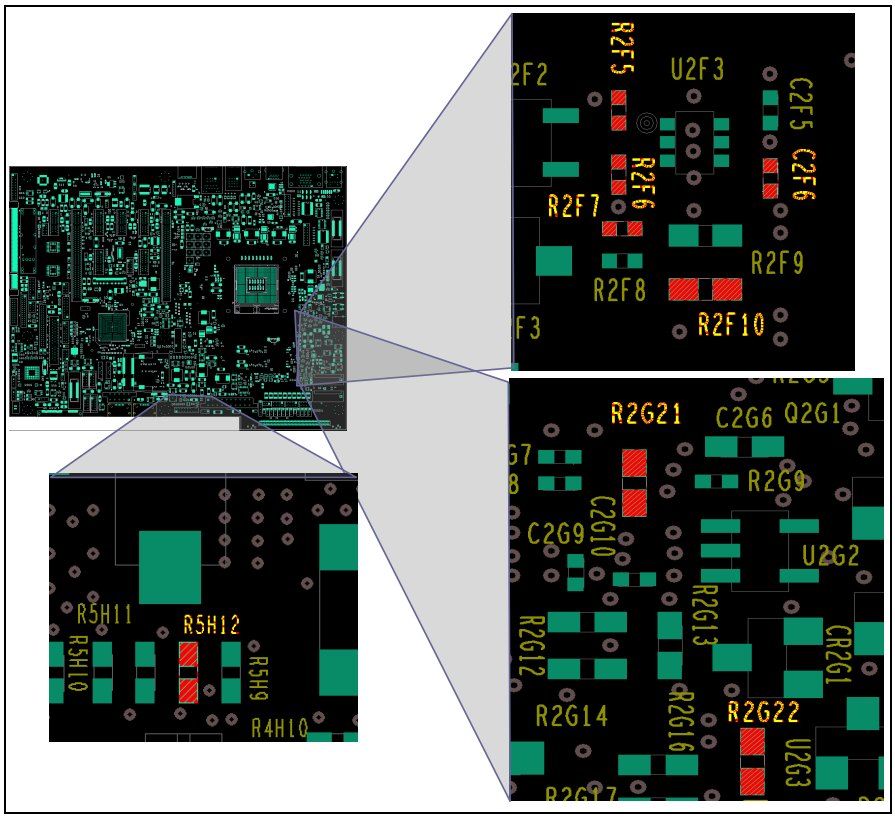
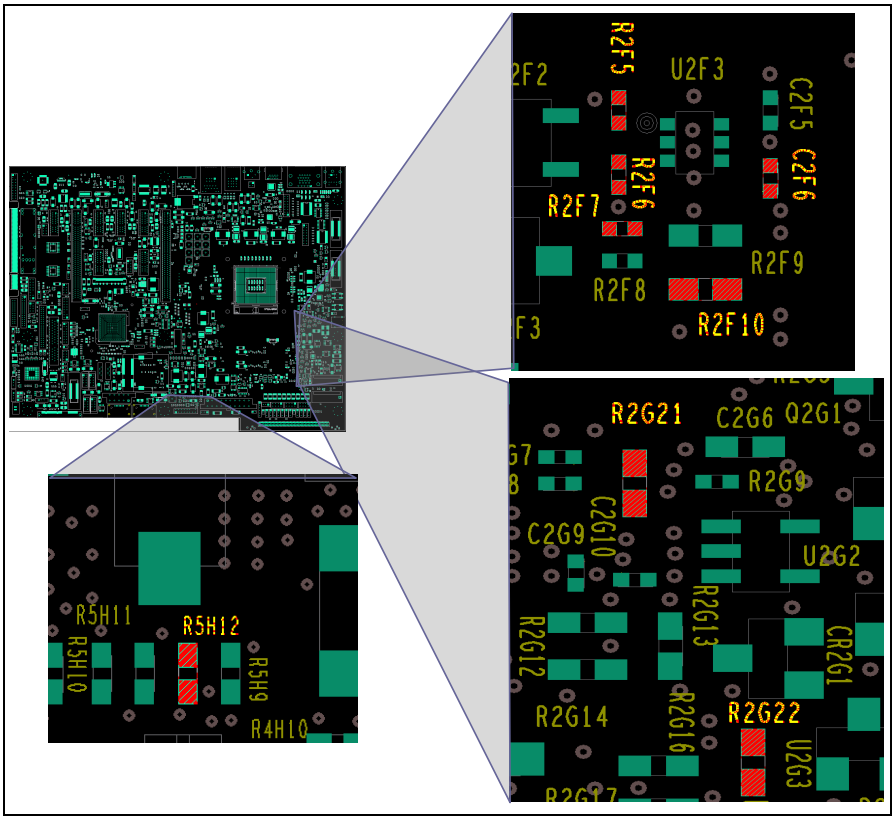


Figure 10. Red Fort Motherboard: Bottom View



5.1.3 SM_DRAM_PWROK

- **Impacted CRBs:** Red Fort ES2 CRBs (E32054-301 GM) and (E32053-301 MPI). Not needed on Red Fort QS1 and later CRBs.
- **Re-work:** Replace R2E1 to 3.01 kΩ and R2E2 to 1.1 kΩ
- **Reason:** These reduced resistor values allow the processor VIHMIN signal level to account for the processor input leakage current, while still allowing the Mobile Intel® Series 5 Chipset to actively drive a low level signal to meet the processor VILMAX specification.

5.1.4 PCH_JATG_RST# Jumper J6B1

- **Impacted CRBs:** Red Fort ES2 CRBs (E32054-301 GM) and (E32053-301 MPI). Not needed on Red Fort QS1 and later CRBs.
- **Re-work:** Short J6B1 1-2

- **Reason:** Currently PCH_JTAT_RST# is pulled up through 20 kΩ to +V3.3A while it is 1.1-V logic signal on the Mobile Intel® Series 5 Chipset ES2 silicon. This requires 10 kΩ pull-down to make the PU to +V1.1A rail.

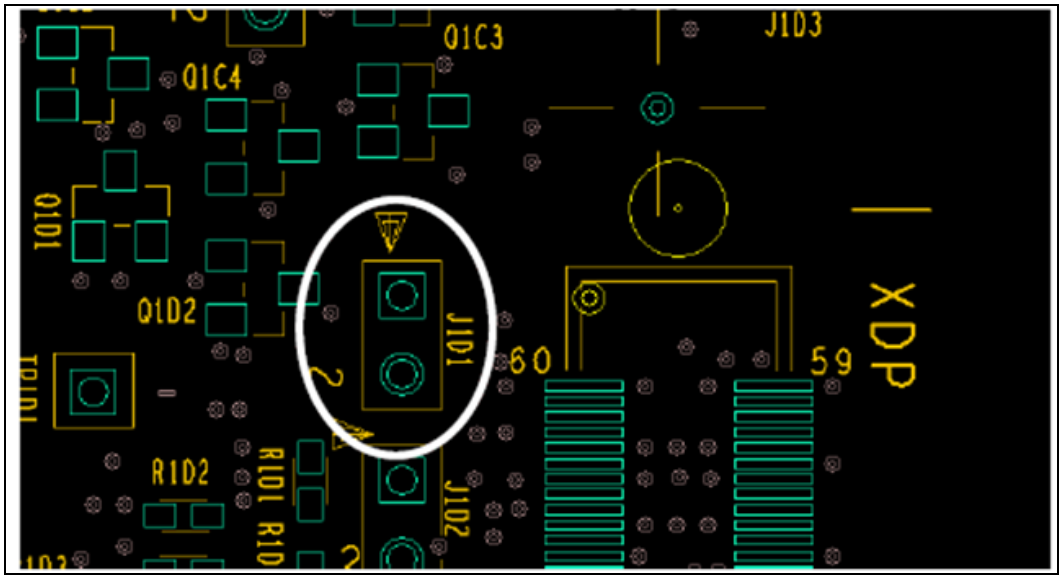
5.2 eDP

The following sections describe the rework necessary to enable eDP.

5.2.1 eDP Rework

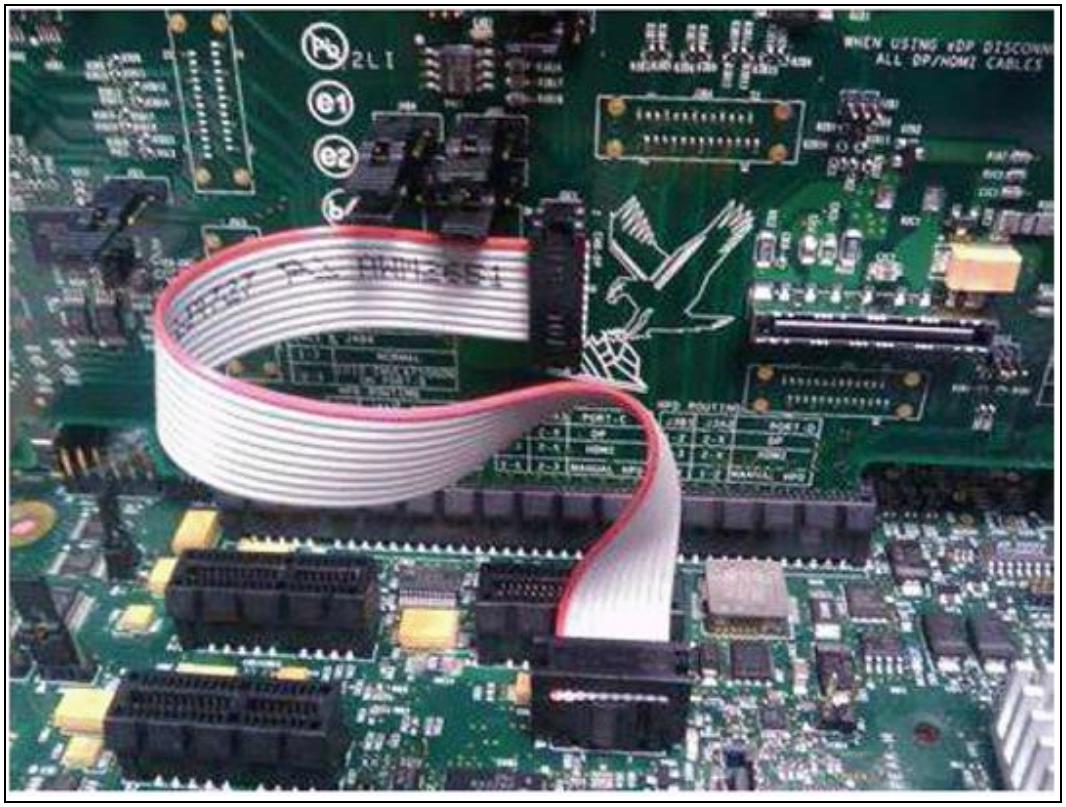
1. Short jumper J1D1 to 1-2 on the motherboard to enable eDP (Figure 11).

Figure 11. Jumper J1D1 Rework



2. Insert the PCIe graphics Fab3 Add-in-Card in the PCIE GRAPHICS CARD slot (J5C1) on the motherboard.
3. Remove R1C2 and stuff R2C1 on the PCIe graphics2 add-in card (to have the panel voltage controlled by PCH (L_VDD_EN)).
4. Connect a 10-pin flat-ribbon cable from J6D1 on CRB to J3C1 on PCIe graphics for backlight signals OR instead use the externally powered BLI panels (ensure that pin1 at both connectors is aligned) (see Figure 12).

Figure 12. Connecting the 10-pin Jumper Cable



Note: The eDP panel connector is not a standard connector, hence the PCIe graphics supports only IPEX 20455C4-based eDP panels.

Note: Refer to the eDP Spec (www.displayport.org) for more details.

Note: For BIOS setup options, please refer to *[Calpella] Platform, Enabling Embedded DisplayPort* (eDP) – Reference Guide*.

5.2.2 eDP Panel and Cables Supported

The following, and other equivalent eDP panels, are supported (using the EM2 eDP cable) in the Intel® Core™ i5 Processor with Mobile Intel® QM57 Express Chipset Development kit.

Table 24. eDP Panel Vendor/Part Number

Name	Model Number	Vendor	Resolution	Backlight	Interface Spec	Connector Type
eDP panel 15.6”W	N156B6-D7	CMO	1366 x 768	LED	eDP Version 1 (Table 5-3)	IPEX 20455C4
eDP panel 14.0”W	N1406-D03	CMO	1600 x 900			
eDP panel 14.0”W	140WD12	CPT	1366 x 768			

The following eDP cables are supported (using the EM2 eDP cable) on the Intel® Core™ i5 Processor with Mobile Intel® QM57 Express Chipset Development kit.

Table 25. eDP Cable Vendor and Part Numbers

Vendor	Part Number
ICT*	LA10MC007-A
ICT	LA10FC001-A (With Backlight Support)

5.2.3 Enabling eDP Support on Intel® 5 Series Chipset Port D

Table 26. eDP Port Information

	CFG4	LVDS_DDC_DATA	DPD_CTRL_DATA
eDP on Port D	NC	NC	2.2-k pull-up to +V3.3S
eDP on Port A	3-k pull-down to GND	NC	X (Don’t Care State)

- LVDS and eDP port A “port_detect” straps should be disabled
- ElkCreek3 (EC3) is used for eDP on port D testing
  - Fab3 requires EC3 and motherboard rework
- Panel Power sequencing and BLI control signals from Intel 5 Series Chipset
  - LVDS 50-pin CRB to EC3 cable still required
- DP port D is routed from CRB’s on-board DP connector to EC3 using a customized DP-DP cable
  - DP-DP cable: non-standard source-source cable

5.2.3.1 Rework for Enabling eDP on Port D

After implementing this rework, LVDS is totally disabled and cannot be tested. Need to reverse all the rework mentioned here for testing LVDS on the same board.

Figure 13. NO_STUFF R7R10

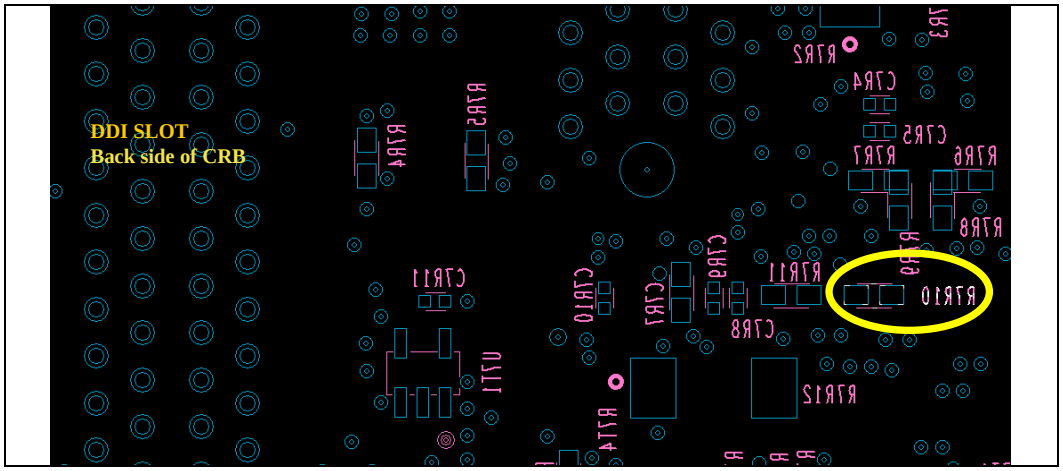
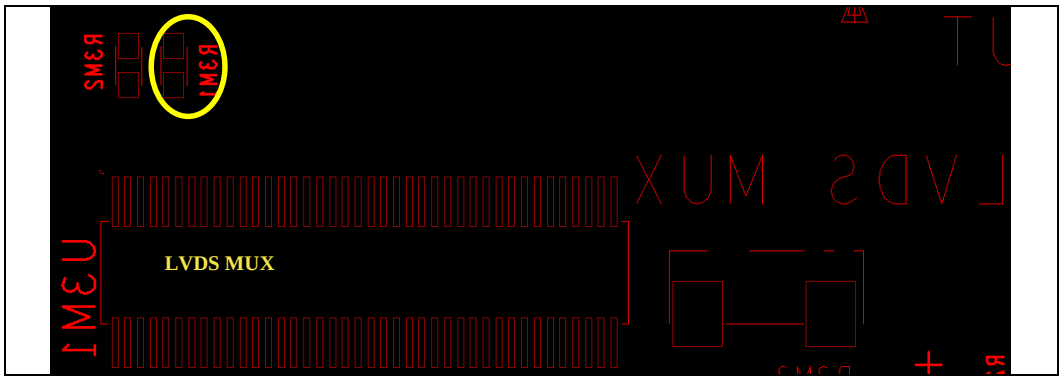


Figure 14. NO_STUFF R3M1 on ELK-CREEK3 AIC



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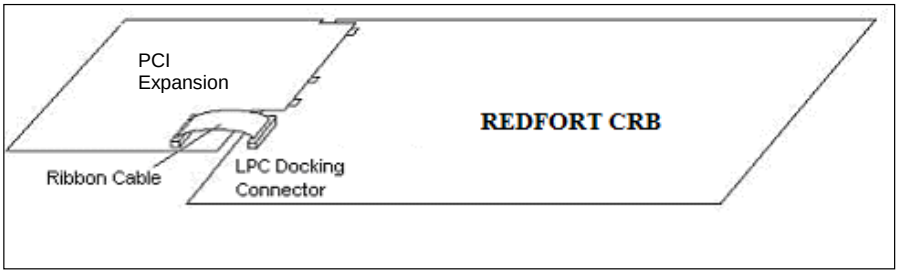
6 Add-in Cards

6.1 PCI Expansion Card

The PCI Expansion Card is provided to offer three PCI slots and one Goldfinger PCI slot on the evaluation board. PCI expansion card also contains a floppy disk drive connector, parallel port connector, and a serial port connector. To connect PCI expansion card slide the horizontal PCI connector on PCI expansion card onto the gold-fingers on the evaluation board. To connect the LPC bus to enable the floppy disk drive connector, parallel port connector, and a serial port connector, connect the ribbon cable as depicted in Figure 15. CLKRUN protocol is supported on PCI expansion card board for only those PCI cards which support CLKRUN#; otherwise CLKRUN# should be disabled in BIOS.

Upon boot up, the system BIOS on the evaluation board automatically detects that PCI expansion card is present and connected to the system. The system BIOS then performs all needed initialization to fully configure PCI expansion card. For additional information see the LPC docking connector on the evaluation board schematics. No SIO docking support on PCI expansion card.

Figure 15. PCI Expansion Card



6.2 Port 80-83 Add-in Card

Figure 16. Port 80-83 Interposer Card

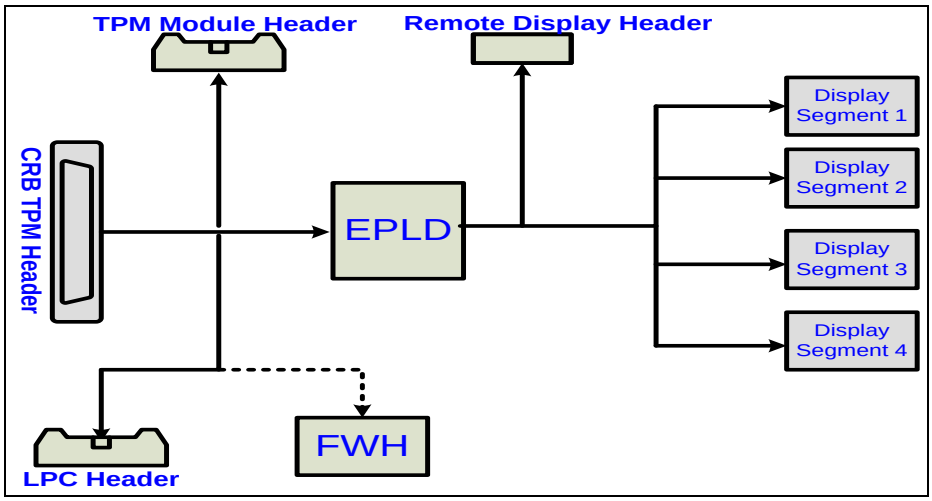
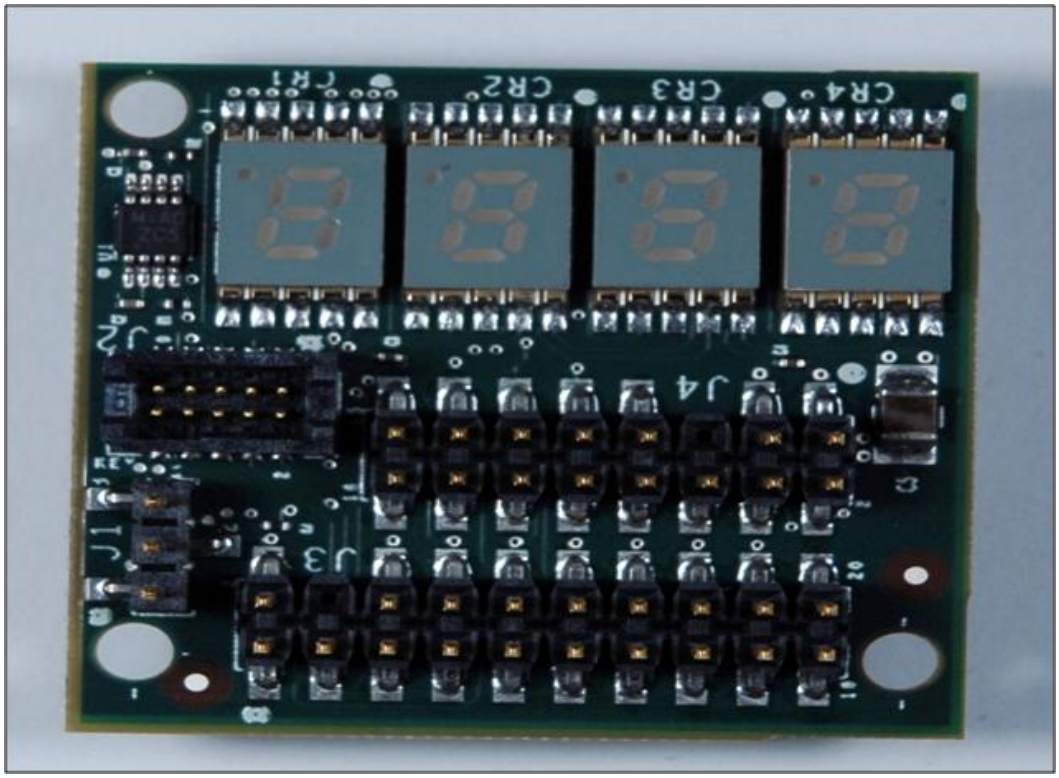


Figure 17. Port 80 Add-in Card



Jumper J1 is used for the configurations as listed in Table 27:

Table 27. Jumper Settings for Port 80-83 Card

Jumper J1	Description
Open (None)	• AIC FWH Disabled • Display Ports 81-80
1-2	• AIC FWH enabled • Display Ports 81-80
2-3	• AIC FWH Disabled • Display Ports 83-82

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7 Heatsink Installation Instructions

It is necessary for the processor to have a thermal solution attached to it in order to keep it within its operating temperatures.

Warning: An ESD wrist strap must be used when handling the board and installing the fan/heatsink assembly.

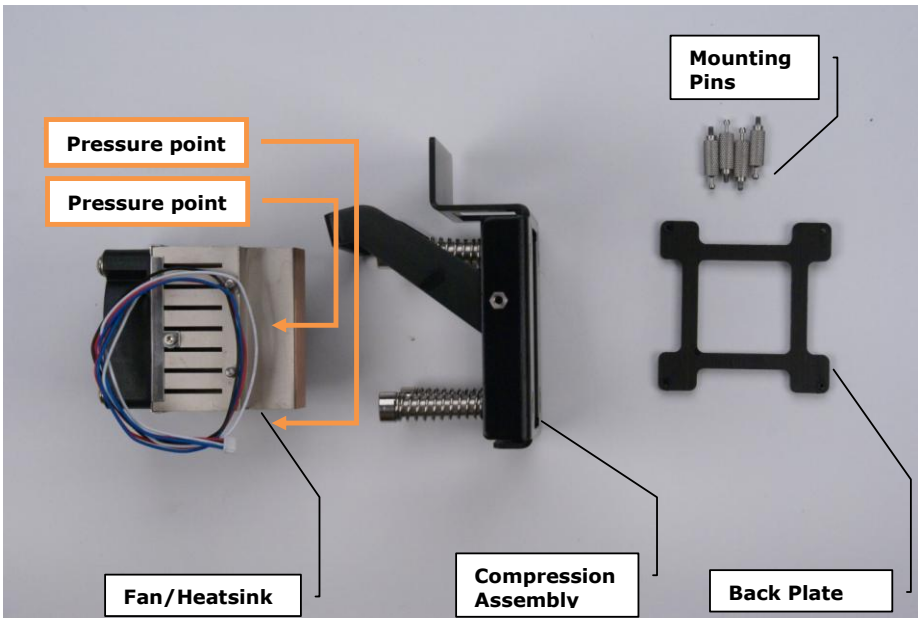
A fan/heatsink assembly is included in the kit. It comes in assembled, but will require the user to disassemble into its primary components so that it may be installed onto the CRB. Those four primary components are (see Figure 18):

- Fan/heatsink
- Compression assembly
- Backplate
- Mounting Pins

To disassemble the primary components:

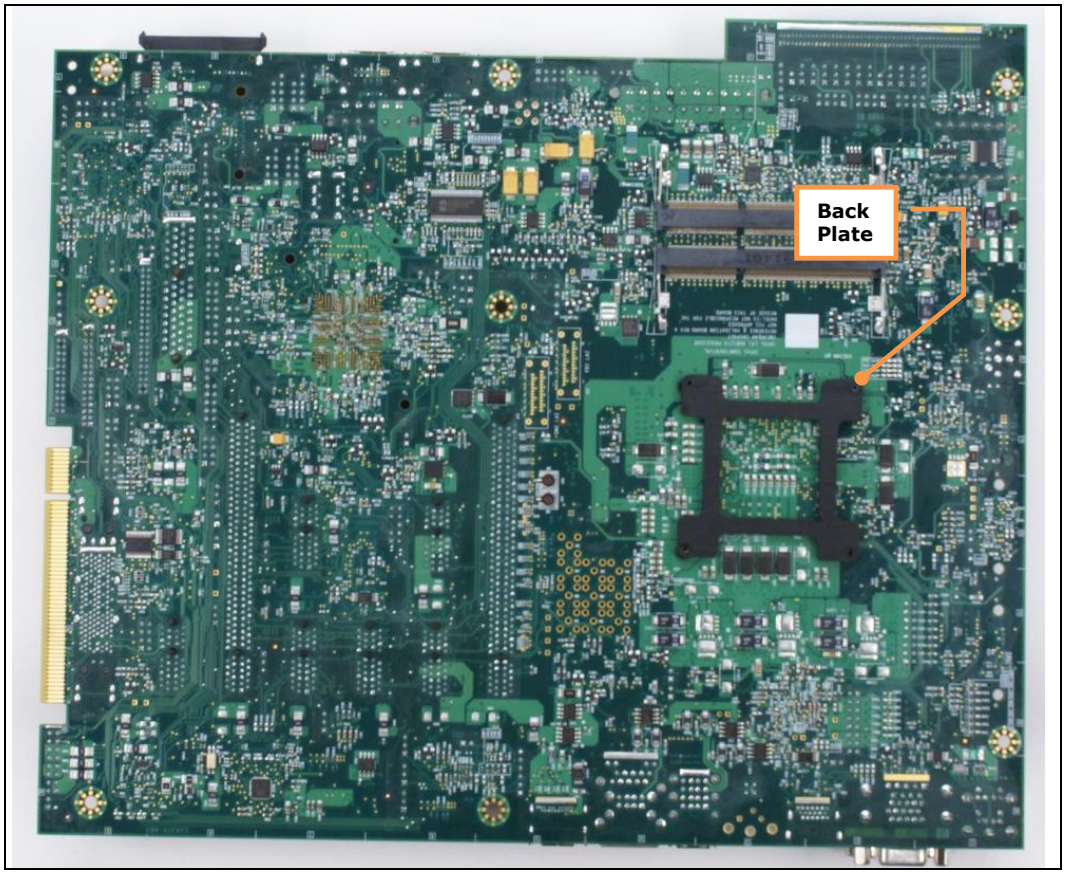
1. Remove the fan/heatsink assembly from its package. Separate into its four primary components. This will require you to unscrew the pins from the backplate. You will also have to remove the fan/heatsink from compression assembly. Set these components aside as shown in Figure 18.

Figure 18. Disassembled Fan/Heatsink Assembly



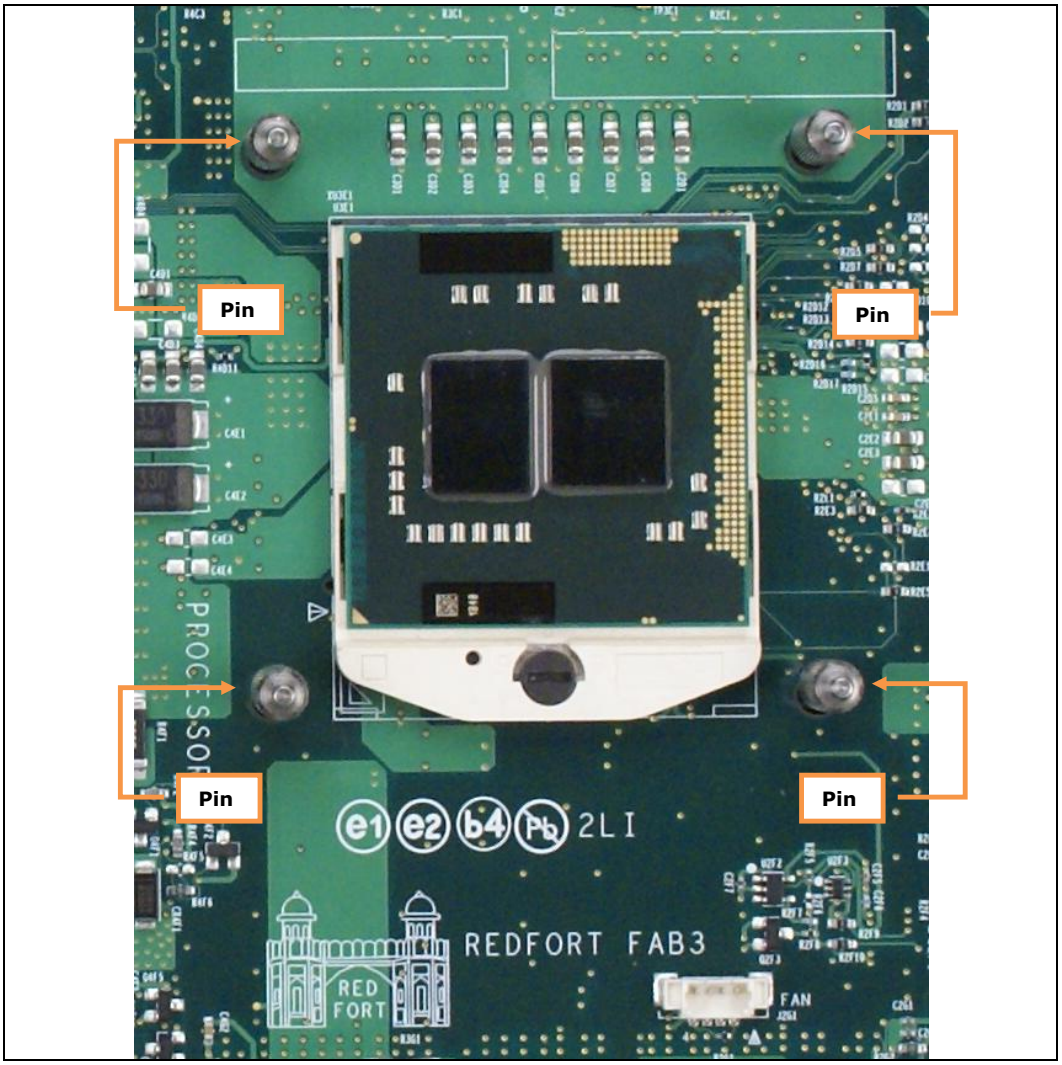
2. Examine the base of the fan/heatsink. This is the area where contact with the Processor die is made. This surface should be clean of all materials and greases. Wipe the bottom surface clean with isopropyl alcohol.
3. Place the backplate on the underside of the board as shown in Figure 19. The screw holes in the backplate should align to the holes in the CRB.

Figure 19. CRB With Backplate in Place: Bottom View



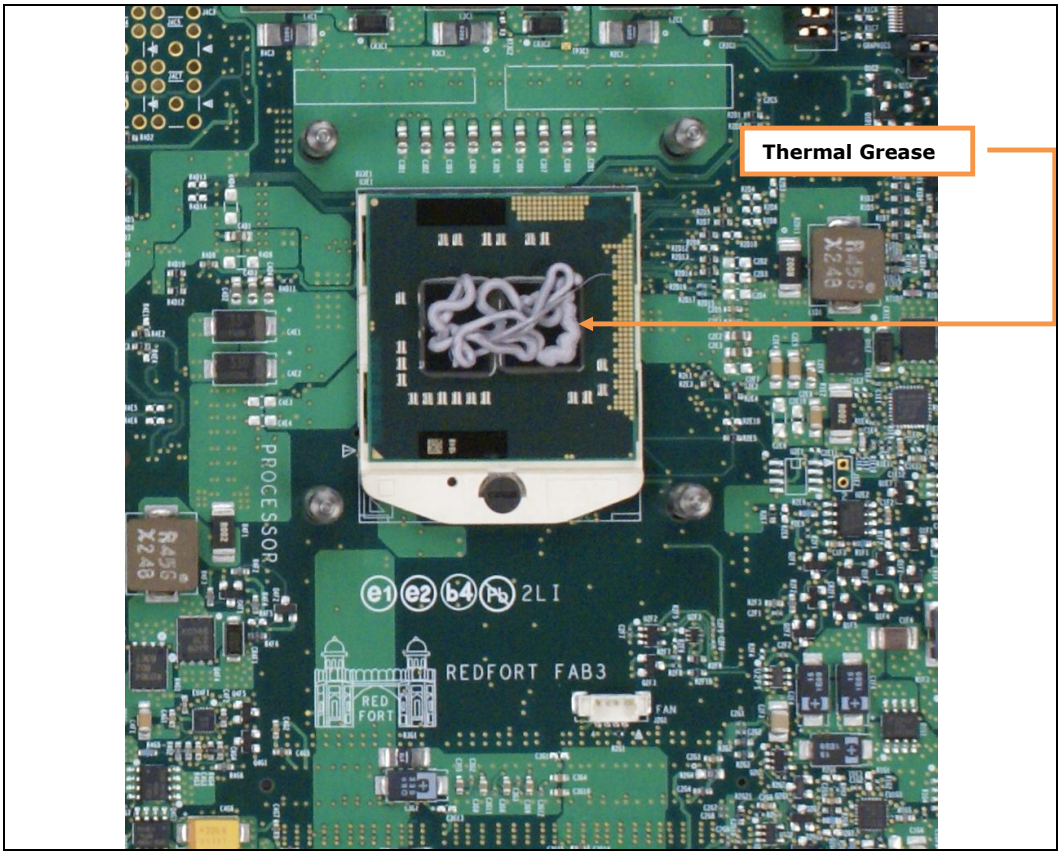
4. Holding the backplate place, turn the board over and screw the pins into the backplate, through the holes in the board. See Figure 20.

Figure 20. Board Top View With Pins Installed Through Board and Into Backplate (Backplate Not Visible)



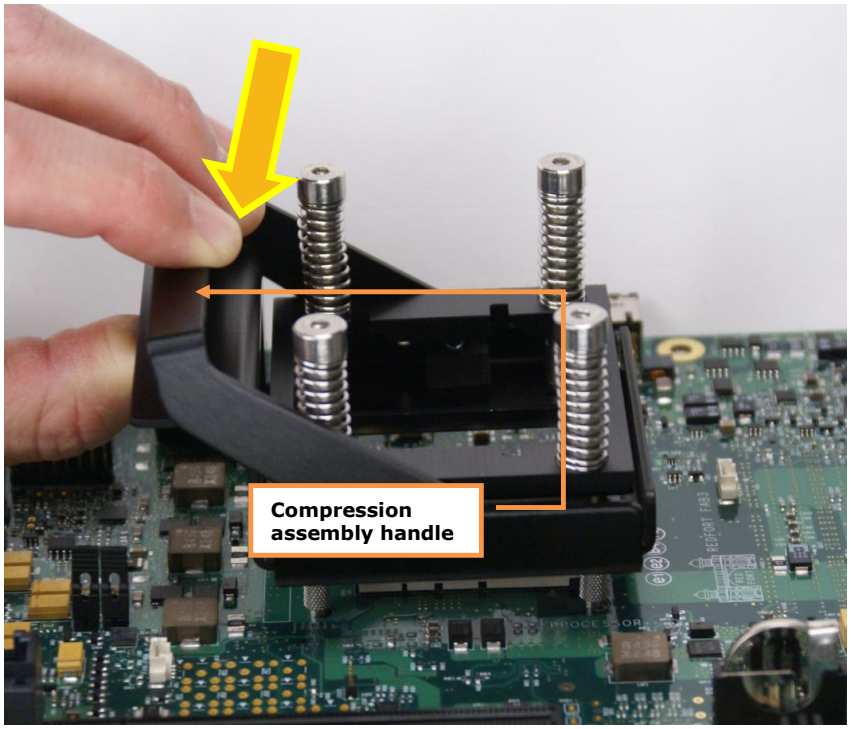
5. Clean the die of the processor with isopropyl alcohol before the fan/heatsink is installed onto the board. This will ensure that the surface of the die is clean. Remove the tube of thermal grease from the package and use it to coat the exposed die of the CPU with the thermal grease. See Figure 21.

Figure 21. Applying Thermal Grease to the Top of the Processor Package



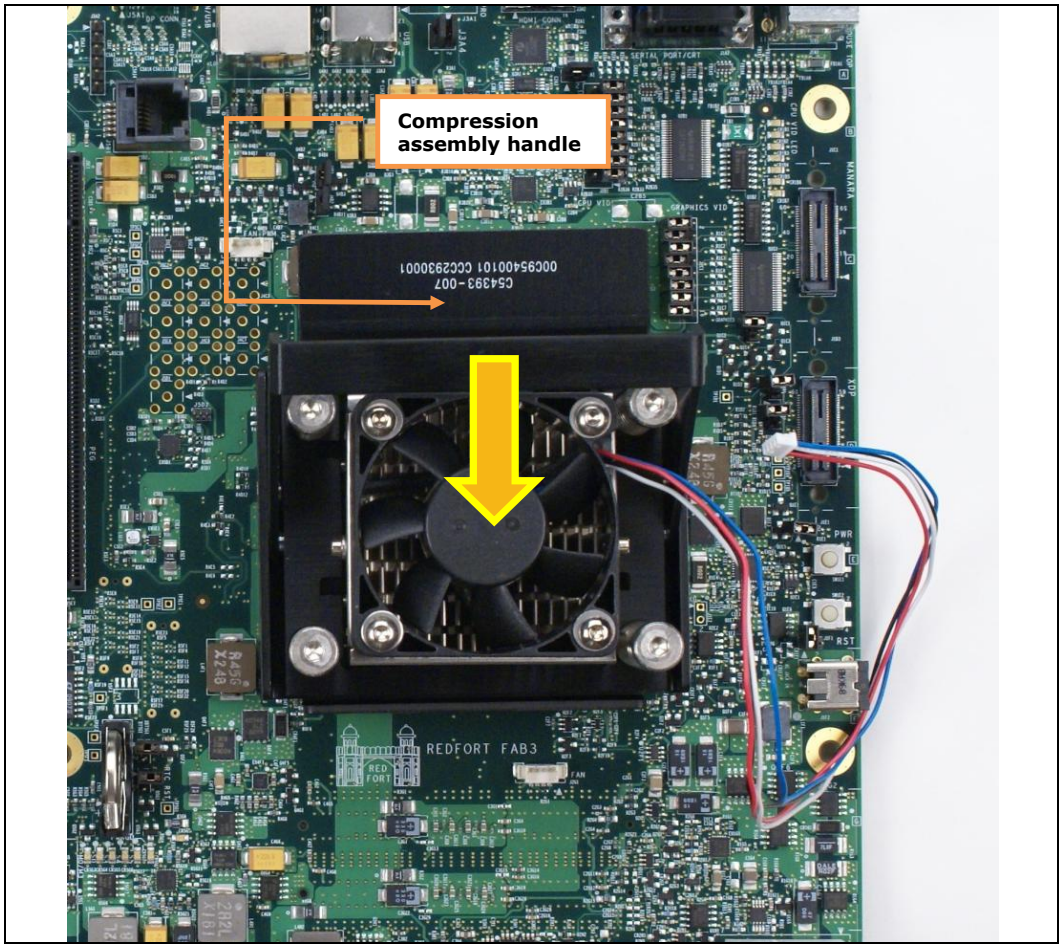
6. Pick up the compression assembly and install it onto the board by lowering the compression assembly onto the pins (installed on the board) such that the pins insert into the bottom of the compression assembly. Then slide the compression assembly forward to lock the pins in place.

Figure 22. Squeeze Activation Arm Downward, Toward the Board



7. Squeeze the activation arm of the compression assembly as shown in Figure 22, which will cause the springs on the compression assembly to compress. While keeping the activation arm compressed, insert the fan/heatsink through the top of the compression assembly such that it rests gently on the Processor. Slide the fan/heatsink away from handle as shown in Figure 23. This will ensure the compression assembly will properly engage the four contact points on the fan/assembly.
8. Now, slowly release the activation arm being certain that the compression assembly comes into contact with the four fan/heatsink contact points. Once the activation arm has been fully released, and the compression assembly should be securely holding the fan/assembly to the Processor. The fan/assembly is now mounted to the board.

Figure 23. Installing Fan/Heatsink (Slide the fan/heatsink away from compression assembly handle.)



9. Finally, plug the fan connector for the fan/heatsink onto the CPU fan header on the motherboard. You have now successfully mounted the fan/heatsink assembly to the motherboard.
10. The CPU fan header is a 4-pin connector. This is a change from the previous chipset development kit which has a 3-pin CPU fan header. As a result, it is not possible to use the heatsink from the previous chipset development.

Figure 24. Fan/Heatsink Power Plugged into Board

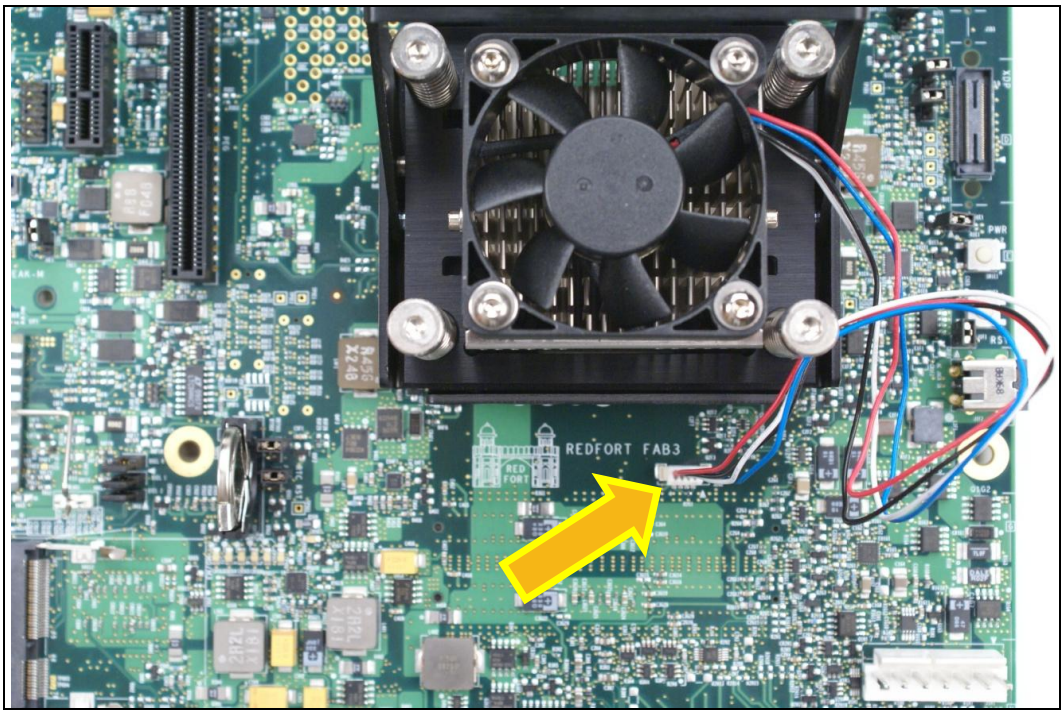


Figure 25. Completed Red Fort CRB with Fan/Heatsink Assembly Installed