REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

PAGE #	COMENT/FUNCTION
1	COVER PAGE.
2	TABLES: BLOCK DIAGRAM
3	CORE: CK_409 (MAIN CLOCK GENERATOR)
4	CORE: CPU SOCKET 1 OF 2
5	CORE: CPU SOCKET 2 OF 2
6	CORE: CPU: PULL-UPS, TJPRO CONN
7	CORE: GMCH: DDR, HOST, HI INTERFACES
8	CORE: GMCH VIDEO AND MISC INTERFACES
9	CORE: GMCH POWER AND GND
10	CORE: GMCH CIRCUITRY
11	CORE: GMCH PLL, STRAPS & MISC CLOCK DRIVERS
12	CORE: DDR SERIES TERMINATION
13	CORE: DIMM CONNECTORS
14	CORE: DDR PARALLEL TERM (STROBES, CNTL)
15	CORE: DDR VTERM CAPS
16	CORE: AGP DIGITAL DISPLAY CONNECTOR
17	CORE: VGA CONNECTOR
18-19	CORE: LVDS CONNECTOR
20	ICH: PCI & IDE INTERFACES
21	ICH: CPU, PM, SATA, USB & HI INTERFACES
22	ICH: PCI-X, AUDIO & SERIAL PORT INTERFACES
23	ICH: ICH PULL-UP/PULL-DOWNS, BATTERY
25	ICH: IDE PRIMARY & SECONDARY
26	ICH: USB BACK PANEL CONNECTORS AND POWER
27	ICH: USB FRONT PANEL CONNECTOR AND POWER
28	ICH: PCI SLOTS 2 - 1
29	ICH: PCI TERMINATION
30	ICH: PCI-X SLOTS 2 - 1
31	ICH: PCI-X TERMINATION
32-33	ICH: SMBUS ISOLATION
34	ICH: SERIAL ATA CONNECTORS
35-36	AUDIO: CODEC
37	AUDIO: CD-IN, LINE-IN
38	AUDIO: MIC-IN, LINE-OUT
39	AUDIO: VREG
40	SIO: LPC47M102
41	SIO: FLOPPY
42	SIO: KEYBOARD & MOUSE PORTS (PS/2)
43	SIO: PARALLEL PORT
44	SIO: COM1-COM3
45	FWH: MFG MODE AND RECOVERY JUMPERS

PAGE #	COMPONENT/FUNCTION
46	GLUE4
47	PC SPEAKER
48	FRONT PANEL HEADER
49	LABELS / MOUNTING HOLES
50	FAN: FAN HEADERS (3)
51	VREG: 2.5V MEMORY, STANDBY-MEMORY
52	VREG: 1.25V MEMORY VTT
53	VREG: ATX POWER CONNECTOR 2X10
54	VREG: PCI VAUX, USB_NCH & USB_PCH
55	VREG: 1.5V STBY & 3.3V STBY
56	VREG: BULK DECOUPLING
57	VREG: 2.5V STR DECOUPLING
58	VREG: CORE 1.5V & 1.8V
59	VREG: CPU MAIN REGULATOR (CPU_CORE)
60	VREG: CPU DECOUPLING, CPU VREG DECOUPLING
61	VREG: GMCH CORE REGULATOR & VCCP REGULATOR
62	DEBUG: TITLE PAGE
63	DEBUG: ITP PORT AND PULL-UPS
64	DEBUG: CPU STATUS LEDS
65	DEBUG: SYSTEM LEDS, PWR & RESET BUTTONS
66	DEBUG: PORT 80 DECODER
67	DEBUG: VID JUMPERS, SMBUS HEADER, HUBLINK PROBE
68	DEBUG: SMA CONNECTORS, SMI/STPCLK INJECTION
69	REVISION HISTORY

855GMEFB

FAB C
REV 2

PBA: C32583-300
PB: C32583-003

POWER SYMBOLS USED:

VCC3
VCC
VCCP
+12V
-12V

NOTES:

3. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.
4. VCCP = +1.05 VOLTS UNLESS OTHERWISE SPECIFIED.

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

INTEL(R) PENTIUM(R) M PROCESSOR
INTEL(R) 82855GME GMCH
INTEL(R) FWE6300ESB I/O CONTROLLER HUB

DRAWING
855GMEFB.SCH.1.1
Mon Apr 19 13:30:43 2004

BOM RELEASE DATE		PB NUMBER C32583-301	
SIGNATURE	DATE	intel	5000 W. CHANDLER BLVD CHANDLER, AZ 85044
DRN BY			
CHK BY		TITLE SCH, PBA, 855GMEFB	
ENGR APVD			
APVD		INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601 / PAGE 1/69 / REV C2
APVD			

~TO ENABLE AGP ADD A JUMPER ACCROSS J5E4 (PAGE 11)

UPGA478 SOCKET

PSB

ICS91718

ADD CONN
DVO B & C
OR
AGP 4X~

LVDS CONN

DAC

BACKLIGHT CONNECTOR

SM BUS

855GME
GMCH

SM BUS

CK_409 CLOCK
(SEE PG 4 FOR CLOCK MAP)

SM BUS
DOUBLE DATA RATE SDRAM
(2-DDR SDRAM DIMMS)

DIMM 0:1

HUB INTERFACE

IDE CONN
PRI & SEC

SERIAL ATA
PORT 0
PORT 1

6300ESB: I/O
CONTROLLER HUB

SM BUS

PCI (33MHZ)

PCI SLOTS 1
PCI SLOTS 2

PCI-X (66MHZ)

PCI-X SLOTS 1
PCI-X SLOTS 2

SERIAL PORT 1
SERIAL PORT 2

BACK PANEL
USB PORT 0
USB PORT 1

FRONT PANEL
USB PORT 2
USB PORT 3

LPC BUS

PORT80

AC LINK

SMSC I/O

FWH: FIRMWARE HUB

AC '97
AUDIO CODEC
REV 2.2

AMP

STEREO LINE OUT
STEREO LINE OUT

MIC IN
AUX CD/AUDIO IN
STEREO LINE IN

PS2 MOUSE &
KEYBOARD

PARALLEL (1)
SERIAL (1)

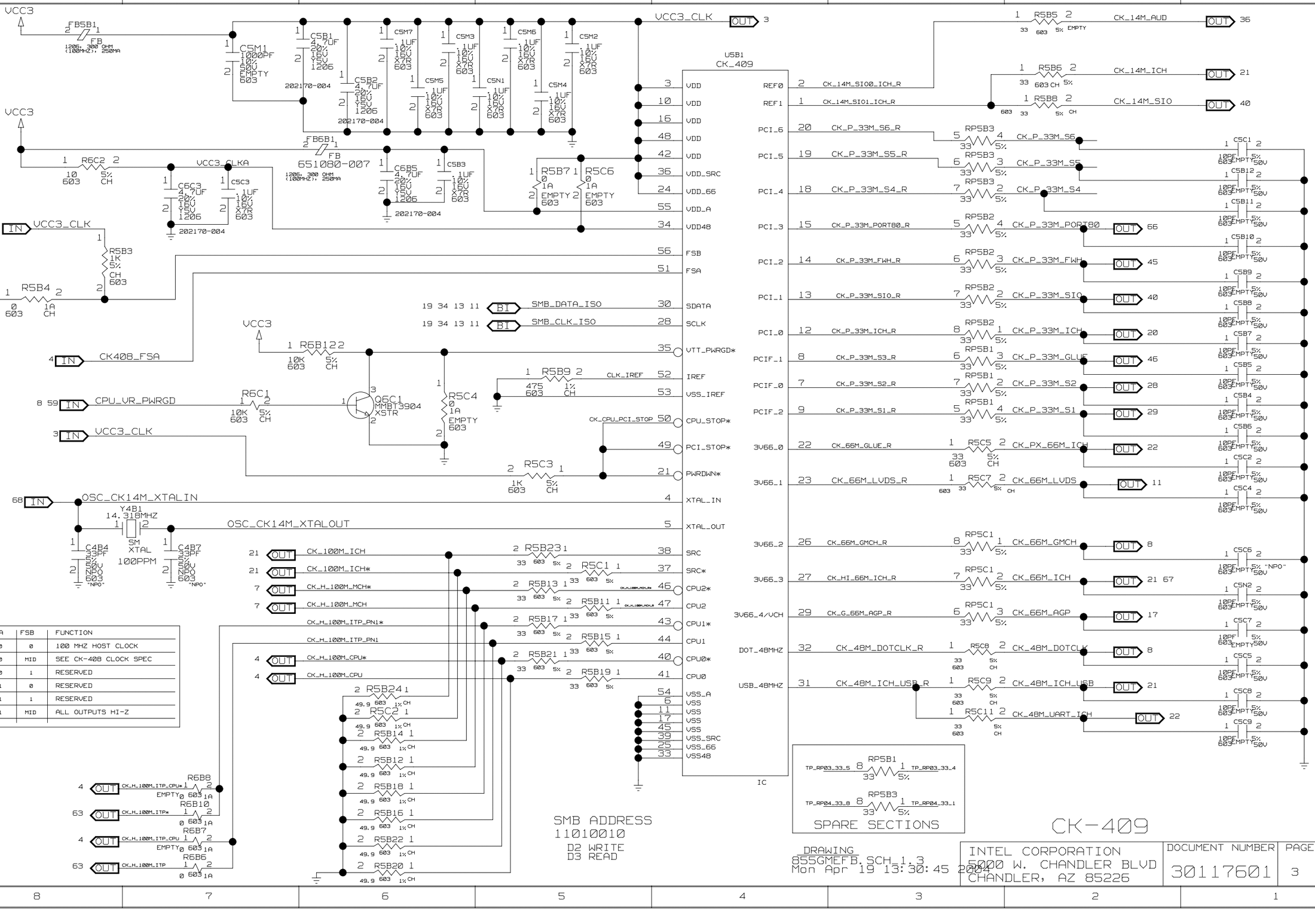
FLOPPY DISK
DRIVE CONN

[PAGE_TITLE=BLOCK DIAGRAM]

DRAWING
855GMEFB.SCH_1.2
Tue May 18 15:33:12 2004

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	2	C2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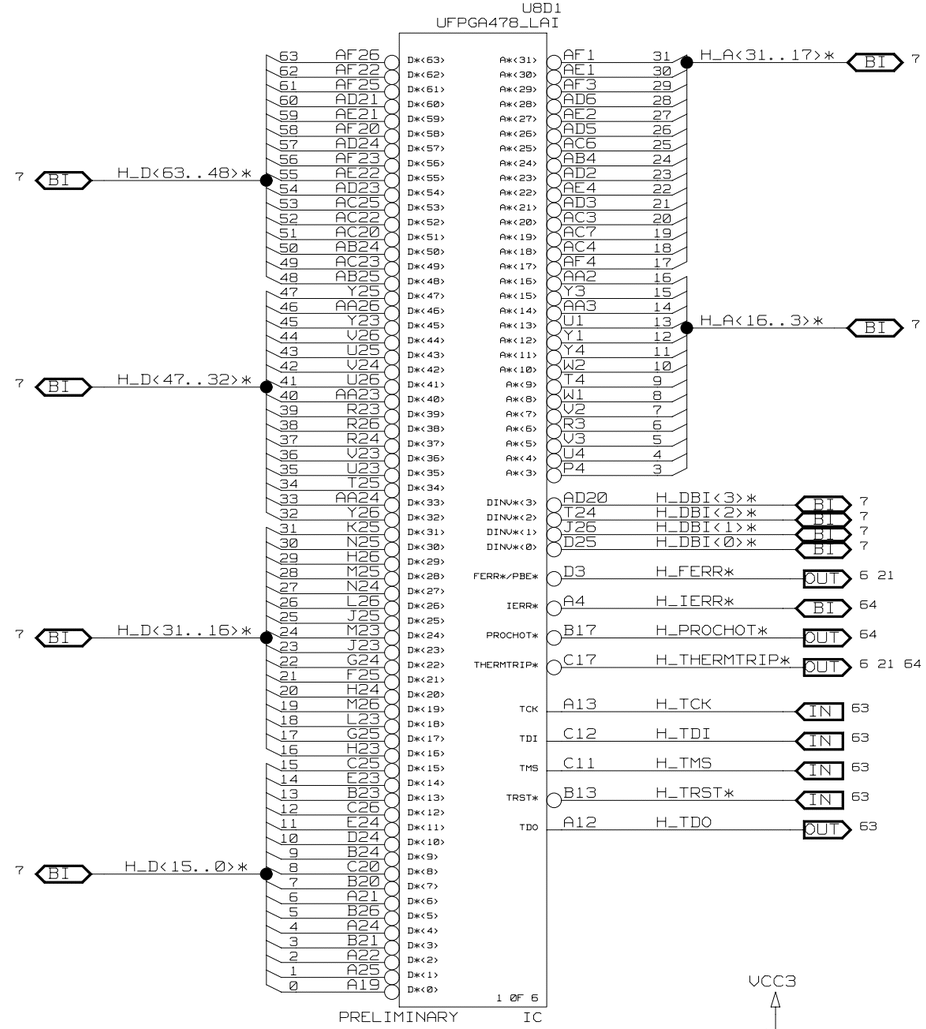
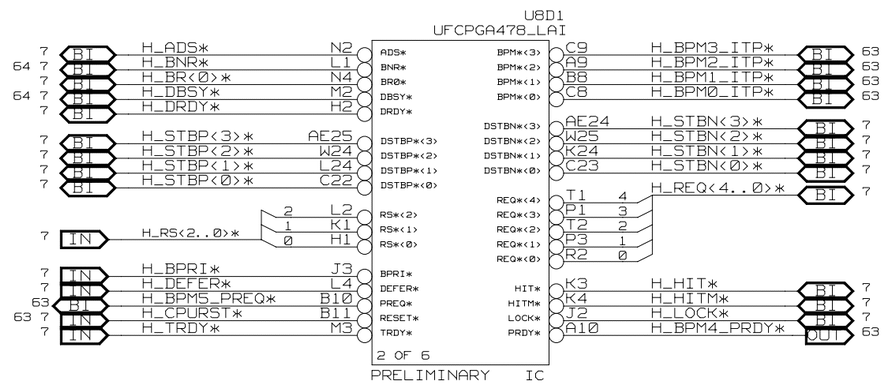
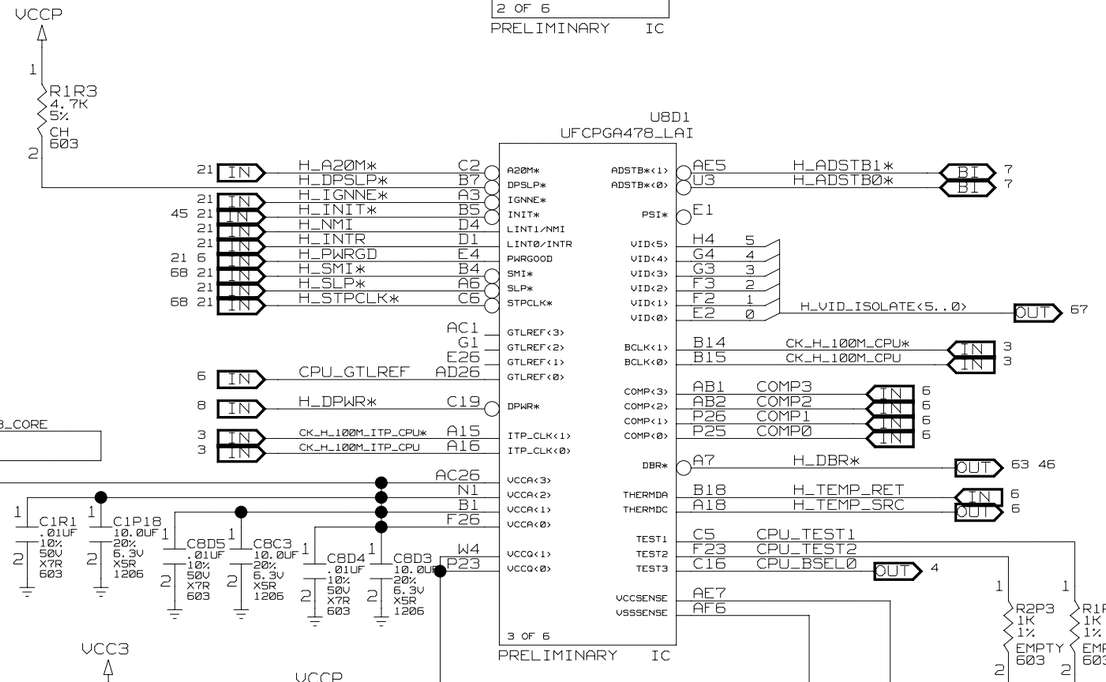
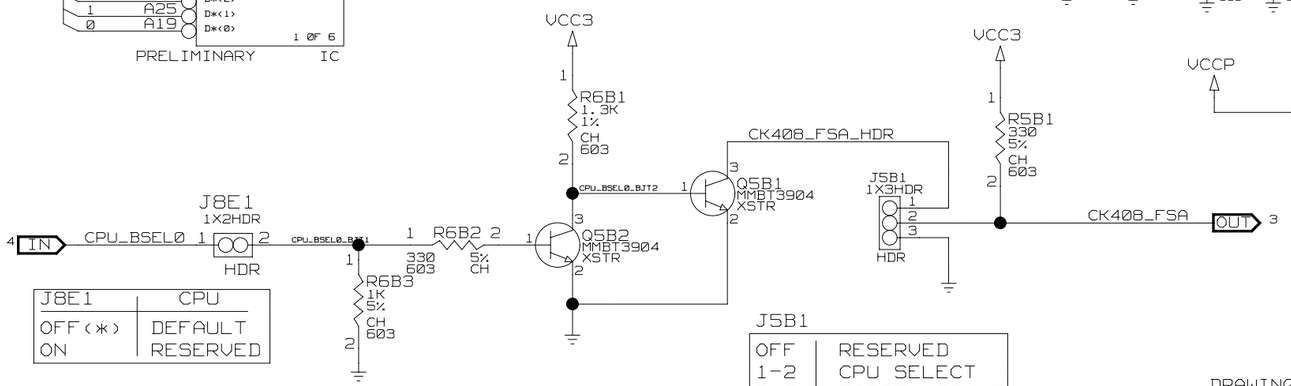
CK_409
VCC3_CLK
OUT 3
VDD 3
VDD 10
VDD 16
VDD 48
VDD 42
VDD_SRC 36
VDD_66 24
VDD_A 55
VDD48 34
FSB 56
FSA 51
SDATA 30
SCLK 28
VTT_PWRGD* 35
IREF 52
VSS_IREF 53
CPU_STOP* 50
PCI_STOP* 49
PWRDWN* 21
XTAL_IN 4
XTAL_OUT 5
SRC 38
SRC* 37
CPU2* 46
CPU2 47
CPU1* 43
CPU1 44
CPU0* 40
CPU0 41
VSS_A 54
VSS 6
VSS 11
VSS 17
VSS 45
VSS_SRC 39
VSS_66 25
VSS48 33
IC
REF0 2 CK_14M_SIO0_ICH_R
REF1 1 CK_14M_SIO1_ICH_R
PCI_6 20 CK_P_33M_S6_R
PCI_5 19 CK_P_33M_S5_R
PCI_4 18 CK_P_33M_S4_R
PCI_3 15 CK_P_33M_PORT80_R
PCI_2 14 CK_P_33M_FWH_R
PCI_1 13 CK_P_33M_SIO_R
PCI_0 12 CK_P_33M_ICH_R
PCIF_1 8 CK_P_33M_S3_R
PCIF_0 7 CK_P_33M_S2_R
PCIF_2 9 CK_P_33M_S1_R
3V66_0 22 CK_66M_GLUE_R
3V66_1 23 CK_66M_LVDS_R
3V66_2 26 CK_66M_GMCH_R
3V66_3 27 CK_HI_66M_ICH_R
3V66_4/VCH 29 CK_G_66M_AGP_R
DOT_48MHZ 32 CK_48M_DOTCLK_R
USB_48MHZ 31 CK_48M_ICH_USB_R
R5B5 CK_14M_AUD OUT 36
R5B6 CK_14M_ICH OUT 21
R5B8 CK_14M_SIO OUT 40
RP5B3 CK_P_33M_S6
RP5B3 CK_P_33M_S5
RP5B3 CK_P_33M_S4
RP5B2 CK_P_33M_PORT80 OUT 66
RP5B2 CK_P_33M_FWH OUT 45
RP5B2 CK_P_33M_SIO OUT 40
RP5B2 CK_P_33M_ICH OUT 20
RP5B1 CK_P_33M_GLUE OUT 46
RP5B1 CK_P_33M_S2 OUT 28
RP5B1 CK_P_33M_S1 OUT 29
R5C5 CK_PX_66M_ICH OUT 22
R5C7 CK_66M_LVDS OUT 11
RP5C1 CK_66M_GMCH OUT 8
RP5C1 CK_66M_ICH OUT 21 67
RP5C1 CK_66M_AGP OUT 17
R5C8 CK_48M_DOTCLK OUT 8
R5C9 CK_48M_ICH_USB OUT 21
R5C11 CK_48M_UART_ICH OUT 22
C5C1 C5B12 C5B11 C5B10 C5B9 C5B8 C5B7 C5B5 C5B4 C5B6 C5C2 C5C4 C5C6 C5N2 C5C7 C5C5 C5C8 C5C9
10PF 603 EMPTY 5% 50V
C5M1 1000PF 10% 50V EMPTY 603
C5B1 4.7UF 20% 16V Y5V 1206 202170-004
C5B2 4.7UF 20% 16V Y5V 1206 202170-004
C5M7 C5M3 C5M6 C5M2 C5M5 C5N1 C5M4 .1UF 10% 16V X7R 603
FB5B1 FB 1206, 300 OHM (100MHZ), 250MA
FB6B1 FB 651080-007 1206, 300 OHM (100MHZ), 250MA
C6B5 4.7UF 20% 16V Y5V 1206 202170-004
C5B3 .1UF 10% 16V X7R 603
C6C3 4.7UF 20% 16V Y5V 1206 202170-004
C5C3 .1UF 10% 16V X7R 603
R6C2 10 603 5% CH
R5B7 0 1A EMPTY 603
R5C6 0 1A EMPTY 603
R5B3 1K 5% CH 603
R5B4 0 603 1A CH
R6B122 10K 603 5% CH
R5B9 475 603 1% CH
R6C1 10K 603 5% CH
Q6C1 MMBT3904 XSTR
R5C4 0 1A EMPTY 603
R5C3 1K 603 5% CH
Y4B1 14.318MHZ SM XTAL 100PPM
C4B4 C4B7 33PF 50V NPO 603 "NPO"
R5B23 R5C1 R5B13 R5B11 R5B17 R5B15 R5B21 R5B19 33 603 5%
R5B24 R5C2 R5B14 R5B12 R5B18 R5B16 R5B22 R5B20 49.9 603 1% CH
R6B8 R6B10 R6B7 R6B6 0 603 1A EMPTY
CK_100M_ICH
CK_100M_ICH*
CK_H_100M_MCH*
CK_H_100M_MCH
CK_H_100M_ITP_PN1*
CK_H_100M_ITP_PN1
CK_H_100M_CPU*
CK_H_100M_CPU
CK_H_100M_ITP_CPU*
CK_H_100M_ITP*
CK_H_100M_ITP_CPU
CK_H_100M_ITP
SMB_DATA_ISO
SMB_CLK_ISO
CK408_FSA
CPU_VR_PWRGD
CK_CPU_PCI_STOP
OSC_CK14M_XTALIN
OSC_CK14M_XTALOUT
VCC3_CLKA
RP5B1 TP_RP03_33_5 TP_RP03_33_4
RP5B3 TP_RP04_33_8 TP_RP04_33_1
SPARE SECTIONS
FSA FSB FUNCTION
0 0 100 MHZ HOST CLOCK
0 MID SEE CK-408 CLOCK SPEC
0 1 RESERVED
1 0 RESERVED
1 1 RESERVED
1 MID ALL OUTPUTS HI-Z
SMB ADDRESS
11010010
D2 WRITE
D3 READ
CK-409
DRAWING
855GMEFB.SCH_1.3
Mon Apr 19 13:30:45 2004
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
DOCUMENT NUMBER 30117601
PAGE 3
REV C2



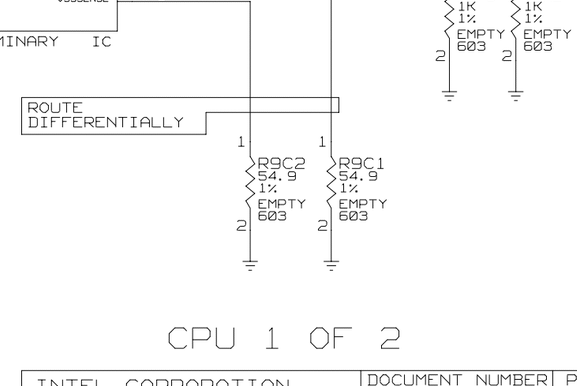






J8E1	CPU
OFF(*)	DEFAULT
ON	RESERVED

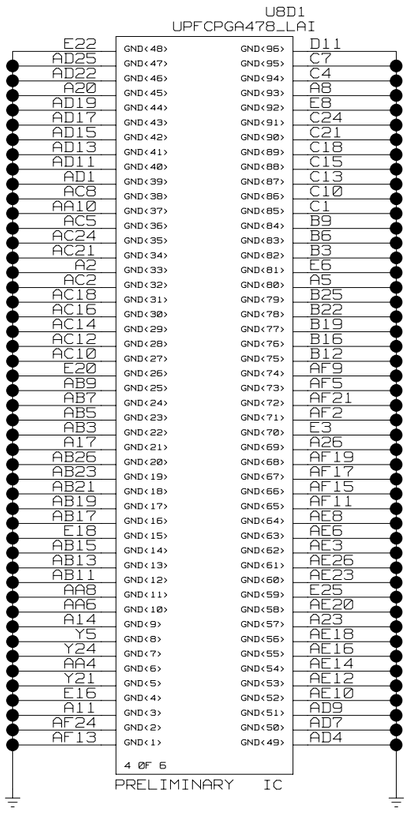
J5B1	
OFF	RESERVED
1-2	CPU SELECT
2-3	FORCE 100MHZ

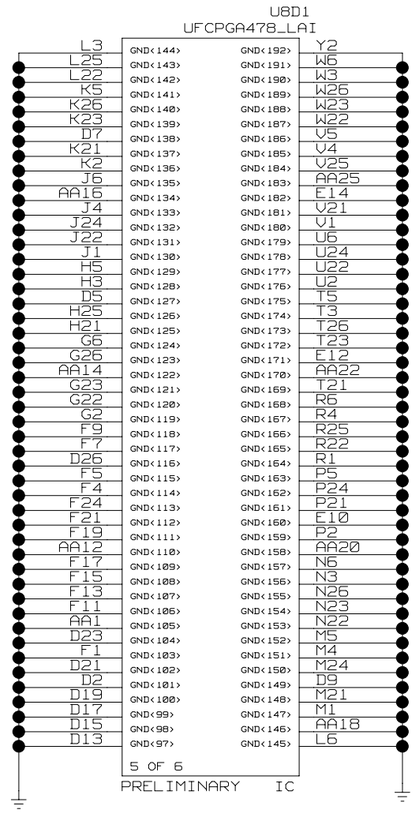


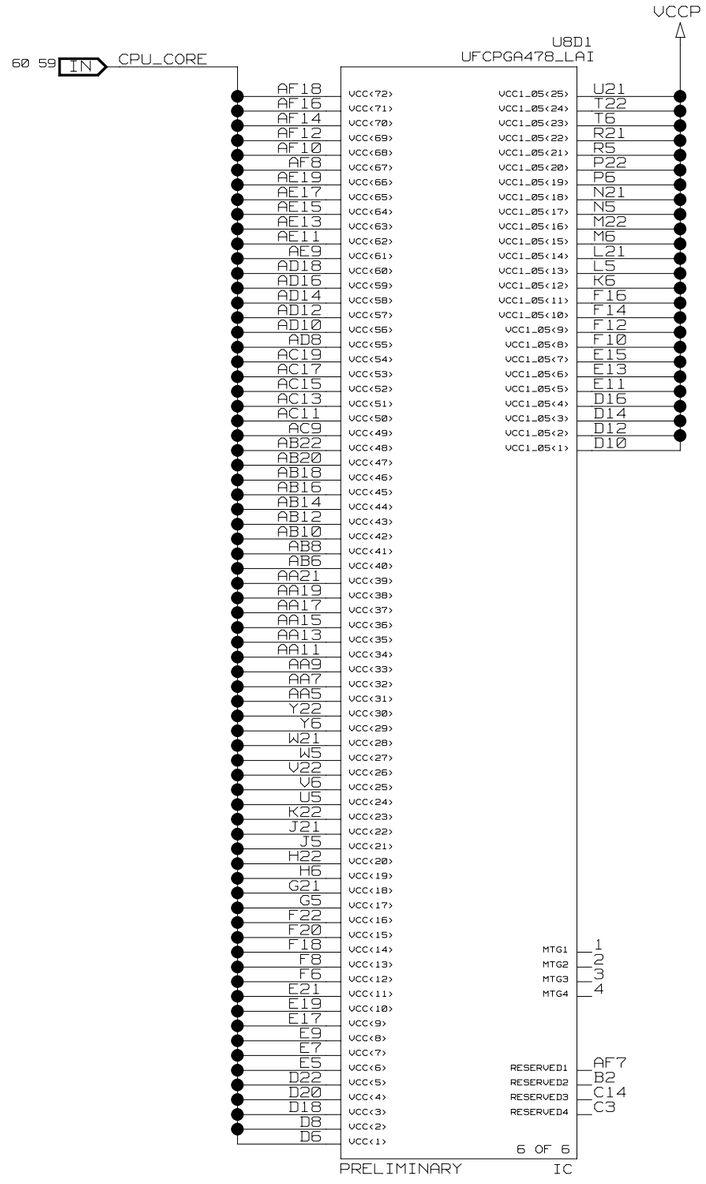
CPU 1 OF 2

DRAWING
855GMEFB.SCH_1.4
Tue May 18 15:33:16 2004

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	4	C2





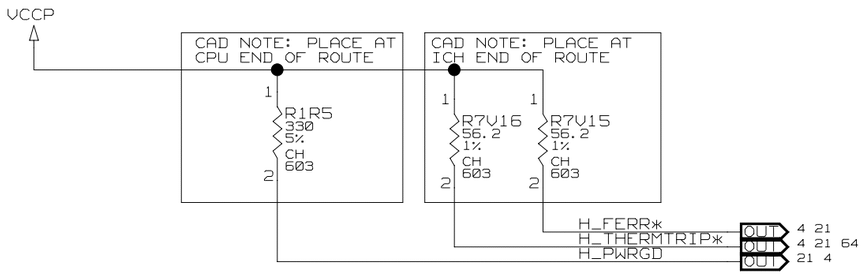


CPU 2 OF 2

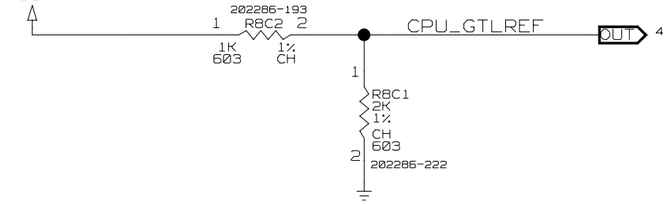
DRAWING
855GMEFB.SCH_1.5
Mon Apr 19 13:30:46 2004

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	5	C2

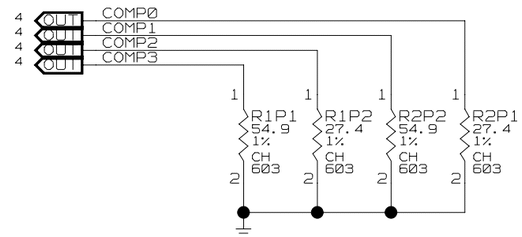
CPU SIGNAL TERMINATION



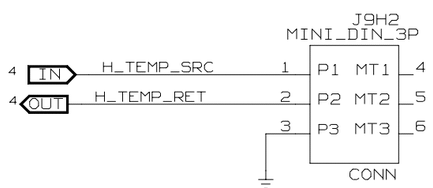
VCCP GTLREF GENERATION CIRCUIT



CPU COMP RESISTORS

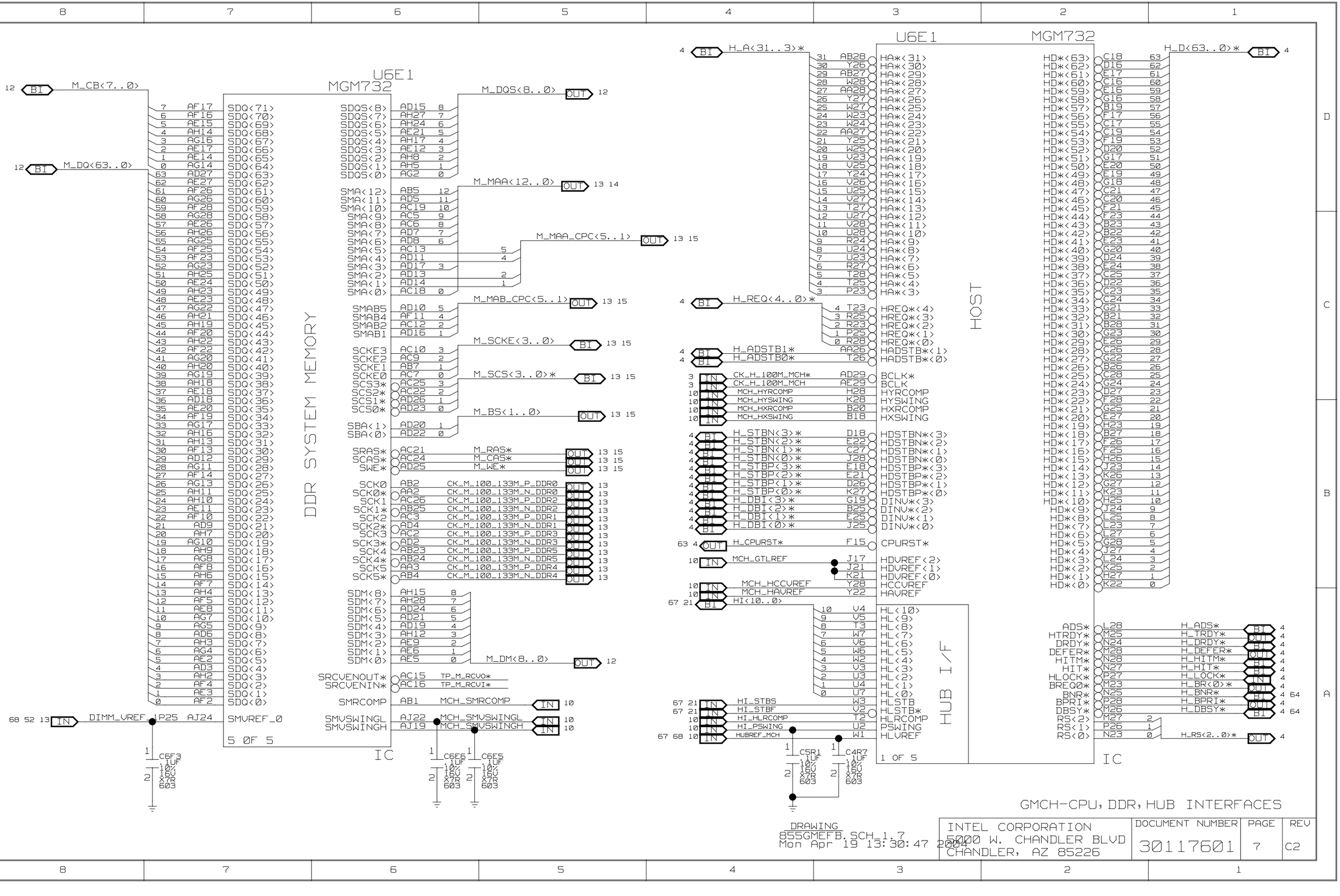


MINIDIN3 FOR CPU THERMAL DIODE MONITORING



CPU CIRCUITS

DRAWING		DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.6 Mon Apr 19 13:30:46 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	6	C2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M_MAB_CPC<5..1>
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CK_M_100_133M_N_DDR0
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CK_M_100_133M_P_DDR5
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SRCVENIN*
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TP_M_RCV1*
SMRCOMP
MCH_SMRCOMP
SMVSWINGL
SMVSWINGH
MCH_SMVSWINGL
MCH_SMVSWINGH
C6E6 .1UF 10% 16V X7R 603
C6E5 1UF 10% 16V X7R 603
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H_REQ<4..0>*
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H_ADSTB0*
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MCH_HYSWING
MCH_HXRCOMP
MCH_HXSWING
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H_DBI<2>*
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MCH_HCCVREF
MCH_HAVREF
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HI_STBF
HI_HLRCOMP
HI_PSWING
HUBREF_MCH
C5R1 1UF 10% 16V X7R 603
C4R7 1UF 10% 16V X7R 603
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BCLK
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HXRCOMP
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DINV*<2>
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DINV*<0>
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HAVREF
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HL<9>
HL<8>
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HL<4>
HL<3>
HL<2>
HL<1>
HL<0>
HLSTB
HLSTB*
HLRCOMP
PSWING
HLVREF
1 OF 5
HUB I/F
HOST
HD*<63>
HD*<62>
HD*<61>
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HD*<4>
HD*<3>
HD*<2>
HD*<1>
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ADS*
HTRDY*
DRDY*
DEFER*
HITM*
HIT*
HLOCK*
BREQ0*
BNR*
BPRI*
DBSY*
RS<2>
RS<1>
RS<0>
H_ADS*
H_TRDY*
H_DRDY*
H_DEFER*
H_HITM*
H_HIT*
H_LOCK*
H_BR<0>*
H_BNR*
H_BPRI*
H_DBSY*
H_RS<2..0>*
GMCH-CPU, DDR, HUB INTERFACES
DRAWING
855GMEFB.SCH_1.7
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CHANDLER, AZ 85226
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U6E1
MGM732

DAC
BLUE C9 VGA_BLUE OUT 8 18
BLUE* D9
GREEN C8 VGA_GREEN OUT 8 18
GREEN* D8
RED A7 VGA_RED OUT 8 18
RED* A8
HSYNC H10 VGA_HSYNC OUT 18
VSYNC J9 VGA_VSYNC OUT 18
REFSET E8 VGA_REFSET IN 10
DDCACLK B6 GLUE4_DDCSCL_3V BI 46
DDCADATA G9 GLUE4_DDCSDA_3V BI 46

LVDS
IYAM<3> C13 3
IYAM<2> C15 2
IYAM<1> E15 1
IYAM<0> G14 0
IYAP<3> B13 3
IYAP<2> C14 2
IYAP<1> E14 1
IYAP<0> F14 0
IYBM<3> G11 3
IYBM<2> C12 2
IYBM<1> E12 1
IYBM<0> H12 0
IYBP<3> G10 3
IYBP<2> C11 2
IYBP<1> E11 1
IYBP<0> G12 0
LVDS_YAM<3..0> OUT 19
LVDS_YAP<3..0> OUT 19
LVDS_YBM<3..0> OUT 19
LVDS_YBP<3..0> OUT 19
ICLKAM D14 LVDS_CLKAM OUT 19
ICLKAP E13 LVDS_CLKAP OUT 19
ICLKBM E10 LVDS_CLKBM OUT 19
ICLKBP F10 LVDS_CLKBP OUT 19
DDCPCLK B4 LVDS_DDCPCLK BI 19
DDCPDATA C5 LVDS_DDCPDATA BI 19
PANELBKLTCTL G8 LVDS_BKLTCTL OUT 19
PANELBKLTEN F8 LVDS_BKLTEN OUT 19
PANELVDDEN A5 LVDS_VDDEN OUT 19
LIBG A10 LVDS_LIBG

CLKS
DREFCLK B7 CK_48M_DOTCLK IN 3
DREFSSCLK B17 CK_66M_LVDS_SS IN 11
LCLKCTLA H9 LCLKCTLA BI 11 19
LCLKCTLB C6 LCLKCTLB BI 11 19

MISC
DPWR* AA22 H_DPWR* OUT 4
DPSLP* Y23 MCH_DPSLP*
RSTIN* AD28 P_PCIRST* IN 24 11 40 45 46 65 66
PWROK J11
EXTTS_0 D6

NC
N/C1 A2
N/C2 A28
N/C3 A29
N/C4 AA9
N/C5 AH1
N/C6 AH29
N/C7 AJ2
N/C8 AJ28
N/C9 AJ29
N/C10 AJ4
N/C11 B1
N/C12 B29

2 OF 5

DVO
DVOBD<11..0> BI 17
DVOBD<11> M5
DVOBD<10> M1
DVOBD<9> N3
DVOBD<8> N2
DVOBD<7> P2
DVOBD<6> N5
DVOBD<5> P5
DVOBD<4> P6
DVOBD<3> R4
DVOBD<2> R6
DVOBD<1> R5
DVOBD<0> R3
DVOBCLK BI 17 P3
DVOBCLK* BI 17 P4
DVOBHSYNC BI 17 T6
DVOBVSYNC BI 17 T5
DVOBBLANK* BI 17 L2
DVOBFLDSTL BI 17 M2
DVOBCINTRB G2
DVOBCCLKINT BI 17 M3
DVOCD<11..0> BI 17
DVOCD<11> G3
DVOCD<10> H6
DVOCD<9> H4
DVOCD<8> H3
DVOCD<7> H1
DVOCD<6> H2
DVOCD<5> J5
DVOCD<4> J6
DVOCD<3> K2
DVOCD<2> K3
DVOCD<1> K1
DVOCD<0> K5
DVOCCLK BI 17 J3
DVOCCLK* BI 17 J2
DVOCHSYNC BI 17 K6
DVOCVSYNC BI 17 L5
DVOCBLANK* BI 17 L3
DVOCFLDSTL BI 17 H5
MI2CCLK BI 17 K7
MI2CDATA BI 17 N6
MDVICLK BI 17 N7
MDVIDATA BI 17 M6
MDDCCLK BI 17 P7
MDDCDATA BI 17 T7
ADDID<7..0> BI 17
ADDID<7> F6
ADDID<6> G6
ADDID<5> F4
ADDID<4> G5
ADDID<3> E2
ADDID<2> E3
ADDID<1> F5
ADDID<0> E5
DVODETECT BI 17 11 L7
DPMS_CLK BI 17 D5
GVREF F1
AGPBUSY* F7
MCH_DVORCOMP BI 10 D1
CK_66M_GMCH BI 3 Y3
GCLKIN
RSVD1 AA5
RSVD2 B12
ADD_RSVD_A8 BI 17 B2
ADD_RSVD_B8 BI 17 B3
AGP_ST2 BI 17 11 C2
RSVD6 D12
ADD_RSVD_A14 BI 17 D2
ADD_RSVD_B12 BI 17 D3
RSVD9 D7
RSVD10 F12
ADD_RSVD_B18 BI 17 F2
ADD_RSVD_A18 BI 17 F3
ADD_RSVD_B39 BI 17 L4
AGP_ST1 BI 17 11 C3
AGP_ST0 BI 17 11 C4

V_1P5_CORE IN 17 11 9 8 58 68 67 56 24 23
R4P6 100K 1% CH 603
R3E4 100K 1% CH 603
R4E3 100K 1% CH 603
R4D5 100K 1% CH 603
C4P3 .1UF 10% 16V X7R 603
VCC3
R4P5 8.2K 5% CH 603
AGP_BUSY*
VCCP
R6D2 1.5K 1% CH 603
R3R2 1K 5% CH 603
R4P9 0 603 1A CH
CPU_VR_PWRGD IN 59 3
MCH_EXTTS IN 11

VGA_BLUE IN 18 8
VGA_GREEN IN 18 8
VGA_RED IN 18 8
MMBD7000LT1
Q5C1 GP SOT23S DIO
Q5D2 GP SOT23S DIO
Q5D1 GP SOT23S DIO
V_1P5_CORE IN 23 17 11 9 8 58 68 67 56 24
C5D1 .1UF 5% 16V X7R 603
C5D3 .1UF 5% 16V X7R 603
C5D2 .1UF 5% 16V X7R 603
VGA CLAMPING DIODES

GMCH-VIDEO, CLKS, CTRL, POWER, GND

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
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GND
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IC

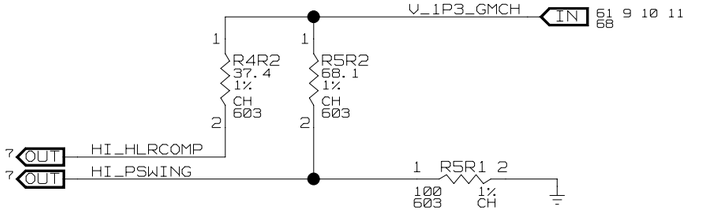
POWER
4 OF 5
IC

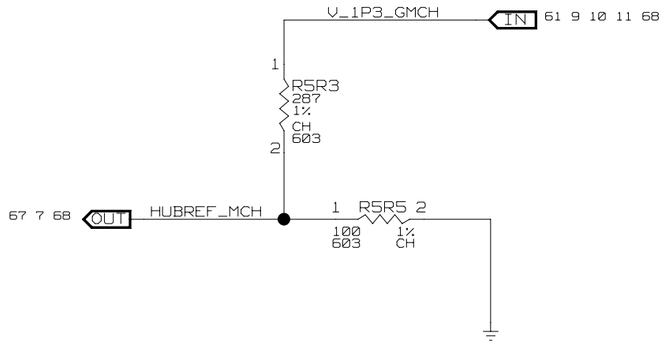
V_1P3_GMCH
V_1P5_GMCH_DPLLA
V_1P5_GMCH_DPLLB
V_1P5_CORE
V_2P5_CORE
V_2P5_SM
VCC3
VCCP

GMCH-POWER AND GROUNDS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.9 Mon Apr 19 13:30:48 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	9	C2

HUBLINK



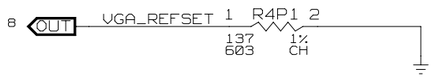


GMCH CORE VOLTAGE TABLE

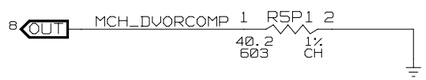
RESISTOR	1.2V	1.35V
R6R3	243, 1%	287, 1%
R5R3	27.4, 1%	37.4, 1%
R6R2	49.9, 1%	68.1, 1%

NOTE: SEE PG61 FOR RELATED STUFFING OPTIONS

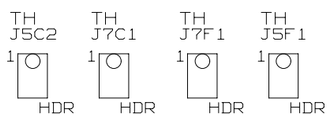
DAC



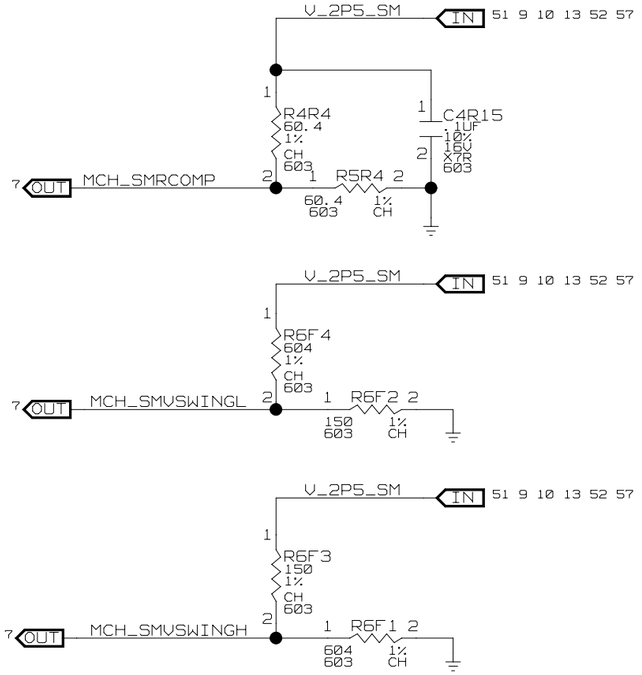
DVO



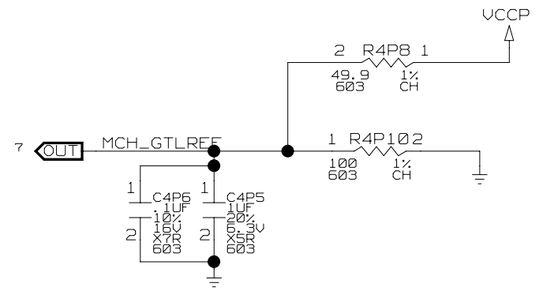
HEATSINK RETENTION CLIPS: QTY(4)



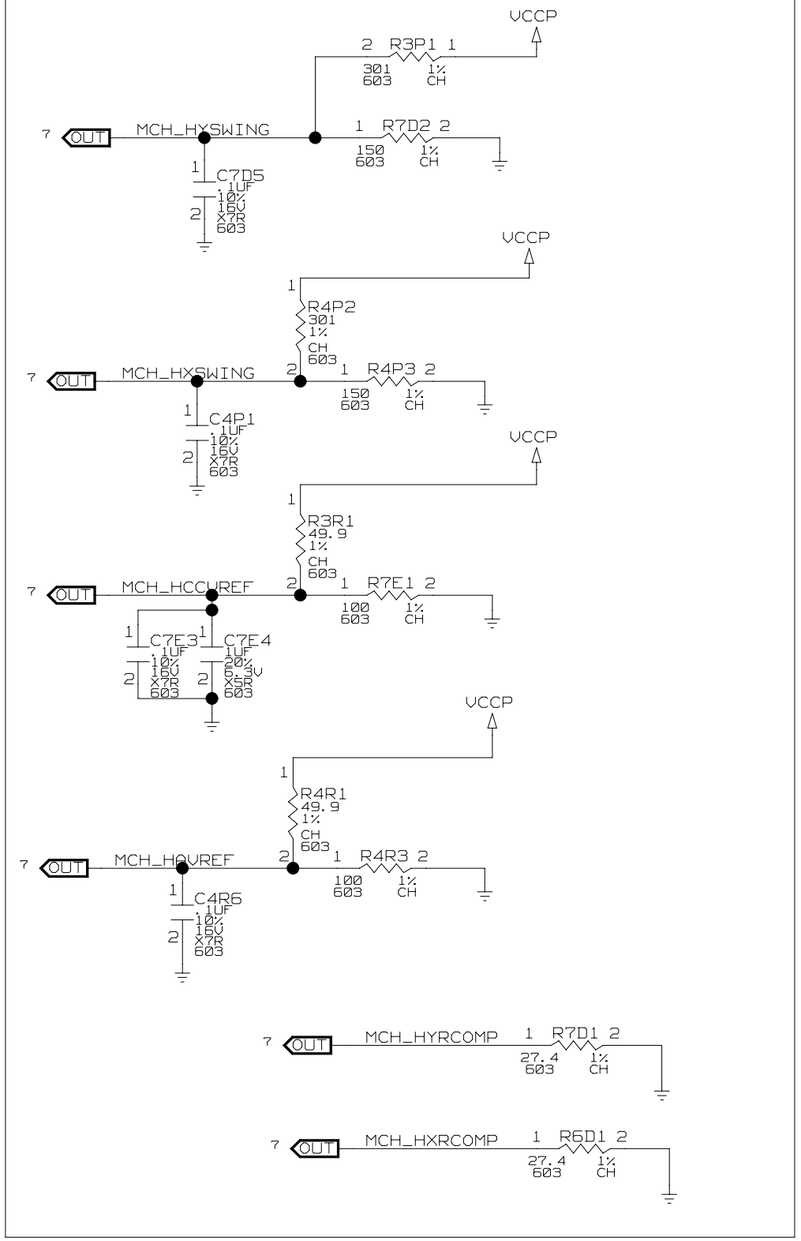
MEMORY



GTL



MCH COMPENSATION & REFERENCE VOLTAGE



GMCH-CIRCUITRY

DRAWING
855GMEFB.SCH_1.10
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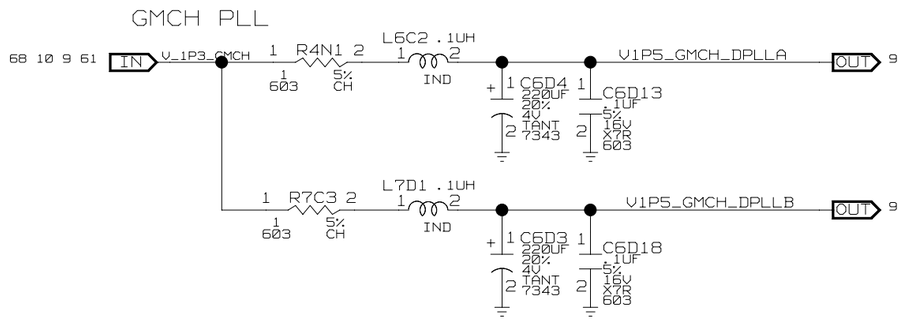
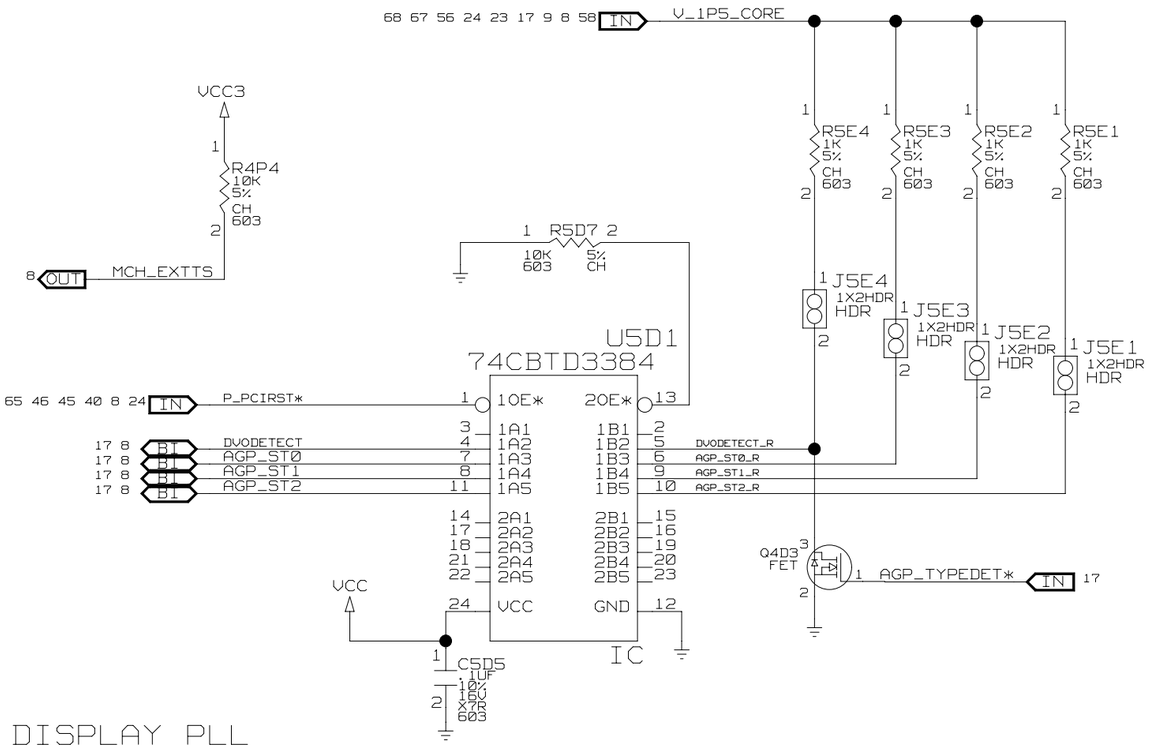
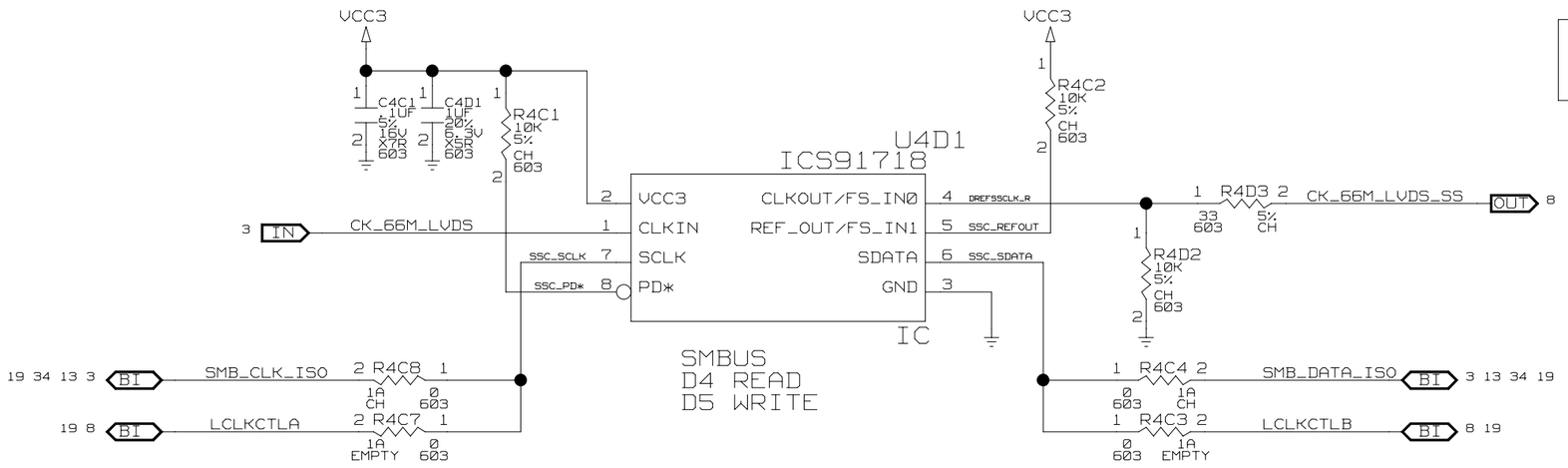
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	10	C2







GMCH STRAPPING OPTIONS

	FUNCTION	BOARD DEFAULT	OPTION OVERRIDE
J5E4	DVO/AGP STRAP	NO SHUNT FOR DVO	SHUNT FOR AGP 4X

J5E1	J5E2	J5E3	PSB FREQ	SM FREQ	GFX FREQ
0	0	0	400	266	200
0	0	1	400	200	200
0	1	0	400	200	133
1*	1*	1*	400	333	250

0 = NO SHUNT, 1 = SHUNT
* = DEFAULT

GMCH PLL, STRAPS & MISC CLKS

DRAWING
855GMEFB.SCH_1.11
Tue May 18 15:33:14 2004

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
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ROOM=DCL_DDR_CORE

M_CB_RS<7..0> BI 13 15

M_DQS_RS<8..0> OUT 13 14

M_DM_RS<8..0> BI 13 14

M_DQ_RS<63..0> BI 13 14

7 BI M_CB<7..0>

7 IN M_DQS<8..0>

7 BI M_DM<8..0>

7 BI M_DQ<63..0>

RP6F4 10 SM 5% IC
RP6F4 10 SM 5% IC
RP6F3 10 SM 5% IC
RP6F3 10 SM 5% IC
RP6F4 10 SM 5% IC
RP6F4 10 SM 5% IC
RP6F3 10 SM 5% IC
RP6F3 10 SM 5% IC

R6F6 10 603 5% CH
R8F8 10 5% CH
R7F6 10 5% CH
R7F4 10 5% CH
R7F1 10 5% CH
R6F8 10 5% CH
R5F5 10 5% CH
R5F3 10 5% CH
R5F2 10 5% CH

R6F7 10 603 5% CH
R8F7 10 5% CH
R7F5 10 5% CH
R7F3 10 5% CH
R7F2 10 5% CH
R6F9 10 5% CH
R5F6 10 5% CH
R5F4 10 5% CH
R5F1 10 5% CH

RP8F2 10 5% IC
RP8F2 10 5% IC
RP8F1 10 5% IC
RP8F1 10 5% IC
RP8F2 10 5% IC
RP8F2 10 5% IC
RP8F1 10 5% IC
RP8F1 10 5% IC
RP7F6 10 5% IC
RP7F5 10 5% IC
RP7F6 10 5% IC
RP7F6 10 5% IC
RP7F5 10 5% IC
RP7F5 10 5% IC
RP7F5 10 5% IC
RP7F5 10 5% IC

RP7F4 10 5% IC
RP7F4 10 5% IC
RP7F3 10 5% IC
RP7F3 10 5% IC
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RP7F4 10 5% IC
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RP7F3 10 5% IC
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RP7F1 10 5% IC
RP7F1 10 5% IC
RP7F1 10 5% IC
RP7F1 10 5% IC

RP6F2 10 5% IC
RP6F2 10 5% IC
RP6F1 10 5% IC
RP6F1 10 5% IC
RP6F2 10 5% IC
RP6F2 10 5% IC
RP6F1 10 5% IC
RP6F1 10 5% IC
RP5F5 10 5% IC
RP5F4 10 5% IC
RP5F5 10 5% IC
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RP5F3 10 5% IC
RP5F2 10 5% IC
RP5F2 10 5% IC
RP5F1 10 5% IC
RP4F1 10 5% IC
RP5F1 10 5% IC
RP5F1 10 5% IC
RP4F1 10 5% IC
RP4F1 10 5% IC
RP4F1 10 5% IC
RP4F1 10 5% IC

DDR SERIES RESISTORS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.12 Mon Apr 19 13:30:49 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	12	C2

ROOM=DCL_DDR_CORE

DDR DIMM 0

PRIMARY A13373-002
ALTERNATE A13373-001

J4G1
DIMM2P_184_CK

14 13 12 BI M_DQ_RS<63..0>

CK_M_100_133M_P_DDR0 IN 7
CK_M_100_133M_N_DDR0 IN 7
CK_M_100_133M_P_DDR1 IN 7
CK_M_100_133M_N_DDR1 IN 7
CK_M_100_133M_P_DDR2 IN 7
CK_M_100_133M_N_DDR2 IN 7

CONN

15 13 7 IN M_WE*
15 13 7 IN M_RAS*
15 13 7 IN M_CAS*
14 13 7 BI M_MAA<12..0>
15 7 BI M_MAA_CPC<5..1>
14 13 12 BI M_DM_RS<8..0>
14 13 12 BI M_DQS_RS<8..0>
15 13 12 BI M_CB_RS<7..0>
15 13 7 IN M_SCS<3..0>*
15 13 7 IN M_SCKE<3..0>
15 13 7 IN M_BS<1..0>

19 34 13 11 3 BI SMB_DATA_ISO
19 34 13 11 3 BI SMB_CLK_ISO

V_2P5_SM IN 51 9 10 13 52 57

V_2P5_CORE IN 51 9 13 68
DIMM_VREF_1P25 IN 13 52 68 7

PLACE RES DIVIDER NEAR DIMMS
R6U1 49.9 1% CH 603
R6U2 49.9 1% CH 603
DIMM_VREF_1P25 OUT 52 68 7 13

C4G1 .1UF 10% 16V X7R 603 NEAR DIMM PIN

DDR DIMM 1

PRIMARY A13373-002
ALTERNATE A13373-001

J4G2
DIMM2P_184_CK

14 13 12 BI M_DQ_RS<63..0>

CK_M_100_133M_P_DDR3 IN 7
CK_M_100_133M_N_DDR3 IN 7
CK_M_100_133M_P_DDR4 IN 7
CK_M_100_133M_N_DDR4 IN 7
CK_M_100_133M_P_DDR5 IN 7
CK_M_100_133M_N_DDR5 IN 7

CONN

15 13 7 IN M_WE*
15 13 7 IN M_RAS*
15 13 7 IN M_CAS*
14 13 7 BI M_MAA<12..0>
15 7 BI M_MAB_CPC<5..1>
14 13 12 BI M_DM_RS<8..0>
14 13 12 BI M_DQS_RS<8..0>
15 13 12 BI M_CB_RS<7..0>
15 13 7 IN M_SCS<3..0>*
15 13 7 IN M_SCKE<3..0>
15 13 7 IN M_BS<1..0>
57 52 13 10 9 51 IN V_2P5_SM

V_2P5_SM IN 57 51 13 9 10 52

V_2P5_CORE IN 51 9 13 68
DIMM_VREF_1P25 IN 13 52 68 7

C6U2 .1UF 10% 16V X7R 603 NEAR DIMM PIN

SMB_CLK_ISO BI 3 11 13 34 19
SMB_DATA_ISO BI 3 11 13 34 19

DDR DIMMS

DRAWING 855GMEFB.SCH_1.13
Mon Apr 19 13:30:50 2004

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
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ROOM=DCL_DDR_CORE

16 15 52 IN V_1P25_MEMVTT

13 12 IN M_DQS_RS<8..0>

13 12 BI M_DM_RS<8..0>

13 12 BI M_DQ_RS<63..0>

13 7 BI M_MAA<12..0>

R4U6 2 — 56 603 5% CH

RP8G2 — 56 SM — 5% .063W IC

RP7G8 — 56 SM — 5% .063W IC

R3U1 2 — 56 603 5% CH

R3U5 2 — 56 603 5% CH

RP6G3 — 56 SM — 5% .063W IC

RP5G7 — 56 SM — 5% .063W IC

RP5G3 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP8G3 — 56 SM — 5% .063W IC

RP8G2 — 56 SM — 5% .063W IC

RP8G1 — 56 SM — 5% .063W IC

RP8G3 — 56 SM — 5% .063W IC

RP8G2 — 56 SM — 5% .063W IC

RP8G1 — 56 SM — 5% .063W IC

RP7G8 — 56 SM — 5% .063W IC

RP7G8 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP8G1 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP7G7 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

RP7G3 — 56 SM — 5% .063W IC

RP7G3 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

RP7G6 — 56 SM — 5% .063W IC

R3U2 2 — 56 603 5% CH

RP7G3 — 56 SM — 5% .063W IC

RP7G2 — 56 SM — 5% .063W IC

RP7G2 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP7G3 — 56 SM — 5% .063W IC

RP7G2 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP7G1 — 56 SM — 5% .063W IC

RP6G4 — 56 SM — 5% .063W IC

RP6G4 — 56 SM — 5% .063W IC

RP6G3 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G4 — 56 SM — 5% .063W IC

RP6G4 — 56 SM — 5% .063W IC

RP6G3 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP5G6 — 56 SM — 5% .063W IC

RP6G2 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP5G6 — 56 SM — 5% .063W IC

RP5G6 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G3 — 56 SM — 5% .063W IC

RP5G3 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G4 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

RP5G2 — 56 SM — 5% .063W IC

RP5G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

RP4G1 — 56 SM — 5% .063W IC

R5U2 2 — 56 603 5% CH

RP5G7 — 56 SM — 5% .063W IC

RP6G6 — 56 SM — 5% .063W IC

RP5G7 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

RP6G1 — 56 SM — 5% .063W IC

R4U3 2 — 56 603 5% CH

R4U1 2 — 56 603 5% CH

RP6G6 — 56 SM — 5% .063W IC

DDR TERMINATION RESISTORS

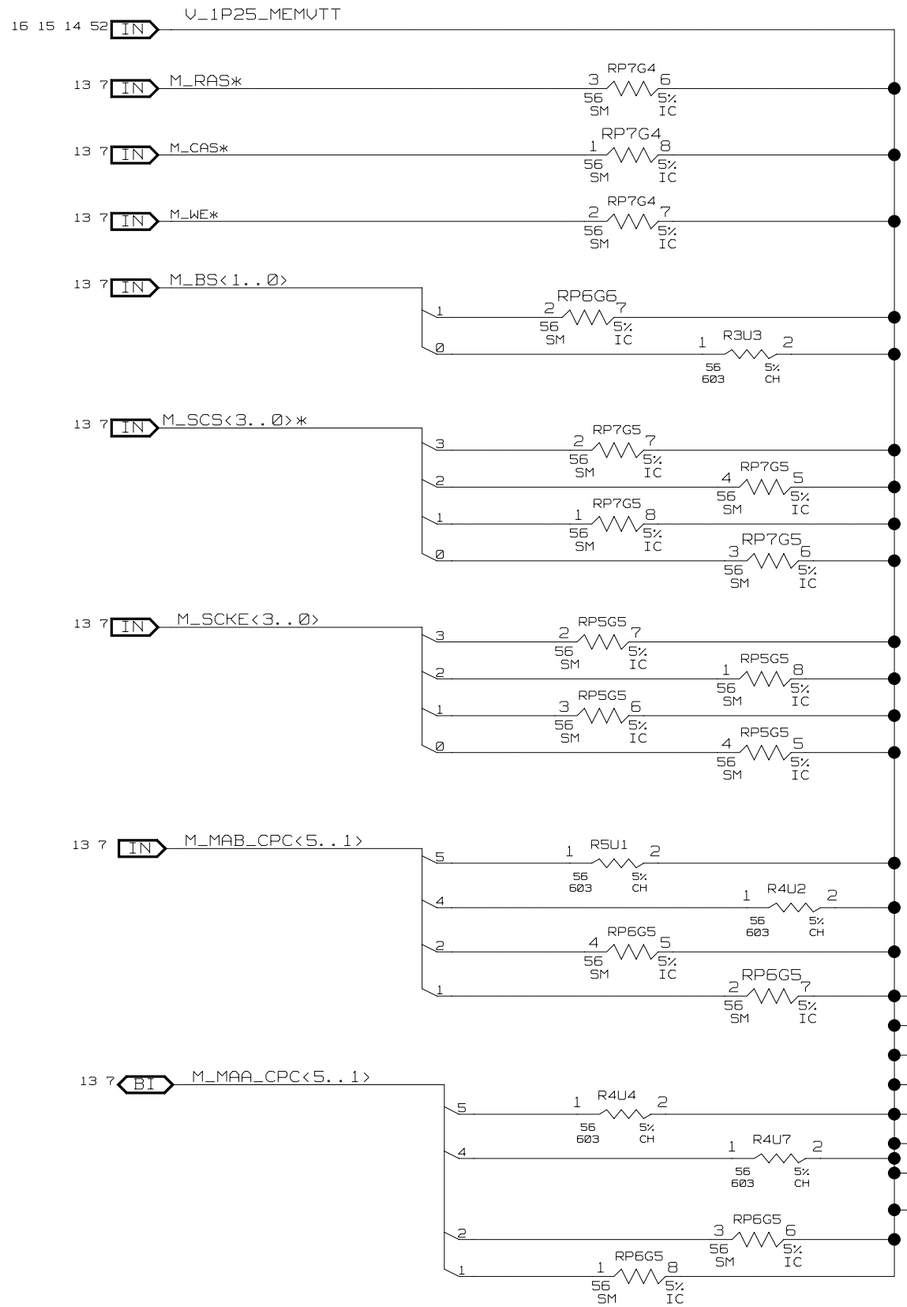
DRAWING
855GMEFB.SCH_1.14
Mon Apr 19 13:30:50 2004

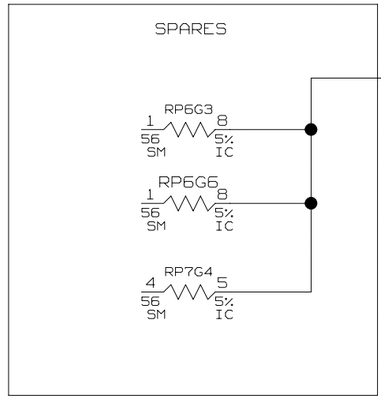
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	14	C2

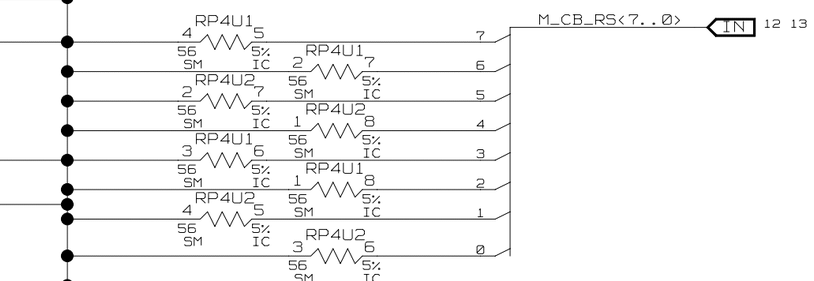
NOTE:

CS SIGNALS MUST HAVE IT'S OWN RES/RPACK
CKE SIGNALS MUST HAVE IT'S OWN RES/RPACK
CPC SIGNALS MUST HAVE IT'S OWN RES/RPACK

ROOM=DCL_DDR_CORE

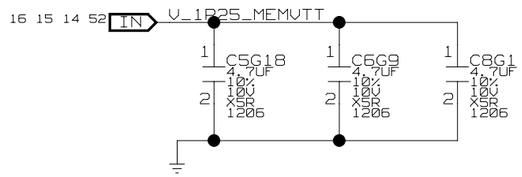




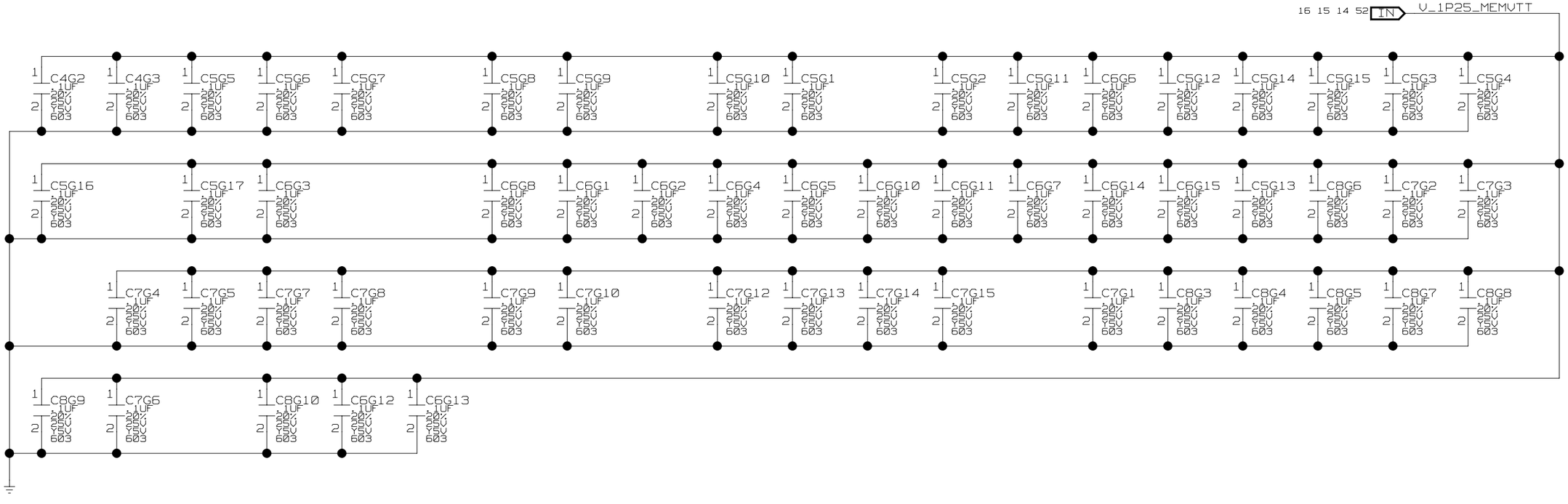


DDR TERMINATION RESISTORS

DRAWING				
855GMEFB.SCH_1.15 Mon Apr 19 13:30:50 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 15	REV C2



PLACED AT LEFT, CENTER AND RIGHT
OF VTT ISLAND



DDR DECOUPLING CAPACITORS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.16 Mon Apr 19 13:30:51 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	16	C2

ROOM=DCL_CORE_AGP

J4C2
1.5V CONAGP

11 8	BI	AGP_ST2	B11	ST2			
11 8	BI	AGP_ST1	A10	ST1			
11 8	BI	AGP_ST0	B10	ST0			
8	BI	DVOCFLDSTL	B26	GAD31			
8	BI	DVOBCINTRB	A26	GAD30			
		10	B27	GAD29			
		11	A27	GAD28			
		8	B29	GAD27			
		9	A29	GAD26			
		6	B30	GAD25			
		7	A30	GAD24			
		4	B33	GAD23			
		3	A35	GAD22			
		2	B35	GAD21			
		1	A36	GAD20			
17 8	BI	DVOCD<11..0>	0	B36	GAD19		
8	BI	DVOCBLANK*		A38	GAD18		
8	BI	DVOCHSYNC		B38	GAD17		
8	BI	DVOCVSYNC		A39	GAD16		
8	BI	MDDCDATA		A51	GAD15		
8	BI	DVOBFLDSTL		B53	GAD14		
8	BI	DVOBCCLKINT		A53	GAD13		
		10	B54	GAD12			
		11	A54	GAD11			
		8	B56	GAD10			
		9	A56	GAD9			
		6	B57	GAD8			
		4	B60	GAD7			
		5	A60	GAD6			
		2	B62	GAD5			
		3	A62	GAD4			
17 8	BI	DVOBD<11..0>	0	B63	GAD3		
			1	A63	GAD2		
8	BI	DVOBVSYNC		B65	GAD1		
8	BI	DVOBHSYNC		A65	GAD0		
8	BI	DVOBCLK		B59	GAD_STB0		
8	BI	DVOCCLK		B32	GAD_STB1		
8	BI	DVOBCLK*		A59	GAD_STB0		
8	BI	DVOCCLK*		A32	GAD_STB1		
8	BI	ADD_RSVD_B18		B18	SB_STB		
8	BI	ADD_RSVD_A18		A18	SB_STB		
17 8	BI	DVOCD<5>		A33	GC_BE3		
8	BI	ADD_RSVD_B39		B39	GC_BE2		
8	BI	DVOBBLANK*		B51	GC_BE1		
17 8	BI	DVOBD<7>		A57	GC_BE0		
				B4	USB+		
				A4	USB-		
20 30	BI	P_INTA*		A6	INTA		
20 30	BI	P_INTB*		B6	INTB		
3	IN	CK_66M_AGP		B7	AGPCLK		
32 31 29 28 46	IN	P_RST_SLOTS*		A7	PCIRST		
				B1	OVRCNT		
17 11	OUT	AGP_TYPEDET*		A2	TYPEDET		
20 29 28	BI	P_PME*		A48	PME		

GDEVSEL	B46	MI2CDATA	BI	8	
GTRDY	A46	MDVICLK	BI	8	
GIRDY	B41	MI2CCLK	BI	8	
GFRAME	A41	MDVIDATA	BI	8	
GSTOP	A47	MDDCCLK	BI	8	
GPERR	B48	ADD_PERR*			
GSERR	B50	ADD_SERR*			
GPAR	A50	DVODETECT	BI	8 11	
WBF	A14	ADD_RSVD_A14	BI	8	
GREQ	B8	ADD_RSVD_B8	BI	8	
GGNT	A8	ADD_RSVD_A8	BI	8	
RBF	B12	ADD_RSVD_B12	BI	8	
PIPE	A12	DPMS_CLK	IN	8 17	
12V	A1				
VCC	B2				
VCC	B3				
VCC3	A9				
VCC3	B9				
VCC3	A16				
VCC3	B16				
VCC3	A28				
VCC3	B28				
VCC3	A25				
VCC3	B25				
VDDQ	A34				
VDDQ	B34				
VDDQ	A40				
VDDQ	B40				
VDDQ	B47				
VDDQ	A52				
VDDQ	B52				
VDDQ	A58				
VDDQ	B58				
VDDQ	A64				
VDDQ	B64				
SBA7	A21	7			
SBA6	B21	6			
SBA5	A20	5			
SBA4	B20	4			
SBA3	A17	3			
SBA2	B17	2			
SBA1	A15	1			
SBA0	B15	0			
3.3VAUX	B24	V_3P3_PCIVAUX	IN	54 28 29 31 32 65	
VREFGC	A66				
VREFCG	B66				
RSVD	A3				
RSVD	A11				
RSVD	B14				
RSVD	A22				
RSVD	B22				
RSVD	A24				

ADDID<7..0> IN 8

NC=1, 2, 3
GND=A5, B5, A13, B13, A19, B19, A23, B23, A31, B31, A37, B37, A49, B49, A55, B55, A61, B61

V_1P5_CORE IN 58 8 9 11 17 23 24 56 67 68

R3E1 8.2K 1% CH 603
R3E2 8.2K 1% CH 603

V_1P5_CORE IN 58 8 9 11 17 23 24 56 67 68

VCC3

V_1P5_CORE IN 58 8 9 11 17 23 24 56 67 68

R4E7 1K 1% CH 603

DVO_VREF OUT 8

R4P7 1K 1% CH 603

C4E5 .1UF 10% 16V X7R 603 PLACE NEAR ADD SLOT

68 67 56 24 23 17 11 9 8 58 IN V_1P5_CORE

MDDCDATA	R4E2	2.2K 603 5% CH
MI2CDATA	R6R1	2.2K 603 5% CH
MDVIDATA	R6P1	2.2K 603 5% CH
MI2CCLK	R4D6	2.2K 603 5% CH
MDVICLK	R6R2	2.2K 603 5% CH
MDDCCLK	R4E1	2.2K 603 5% CH

AGP CONNECTOR DECOUPLING

68 58 5 8 9 11 17 23 24 56 67 V_1P5_CORE IN

C4E3 150UF 20% 10V TANT 7343 EMPTY
C4E2 150UF 20% 10V TANT 7343 EMPTY
C4E1 100UF 20% 10V TANT 7343
C4D4 22UF 20% 10V TANT 3528

C6P3 .1UF 5% 16V X7R 603
C6P2 .1UF 5% 16V X7R 603
C3D7 .1UF 5% 16V X7R 603
C3D10 .1UF 5% 16V X7R 603
C3E6 .1UF 5% 16V X7R 603
C6R2 .1UF 5% 16V X7R 603
C6R1 .1UF 5% 16V X7R 603

VCC

C3C6 22UF 20% 10V TANT 3528
C3C5 .1UF 5% 16V X7R 603
C7N1 .1UF 5% 16V X7R 603

VCC3

C4C2 100UF 20% 10V TANT 7343
C4D3 22UF 20% 10V TANT 3528
C3C9 22UF 20% 10V TANT 3528
C3D5 .1UF 5% 16V X7R 603
C3D1 .1UF 5% 16V X7R 603
C6P1 .1UF 5% 16V X7R 603

CAD NOTE: PLACE NEAR AGP CONNECTOR

68 67 56 24 23 17 11 9 8 58 IN V_1P5_CORE

R8W1 1K 603 5% CH

DPMS_CLK_R

Q4D1 FET
Q4D2 FET

DPMS_CLK OUT 8 17

Q2J1 FET

40 21 IN SUSCLK

+12V

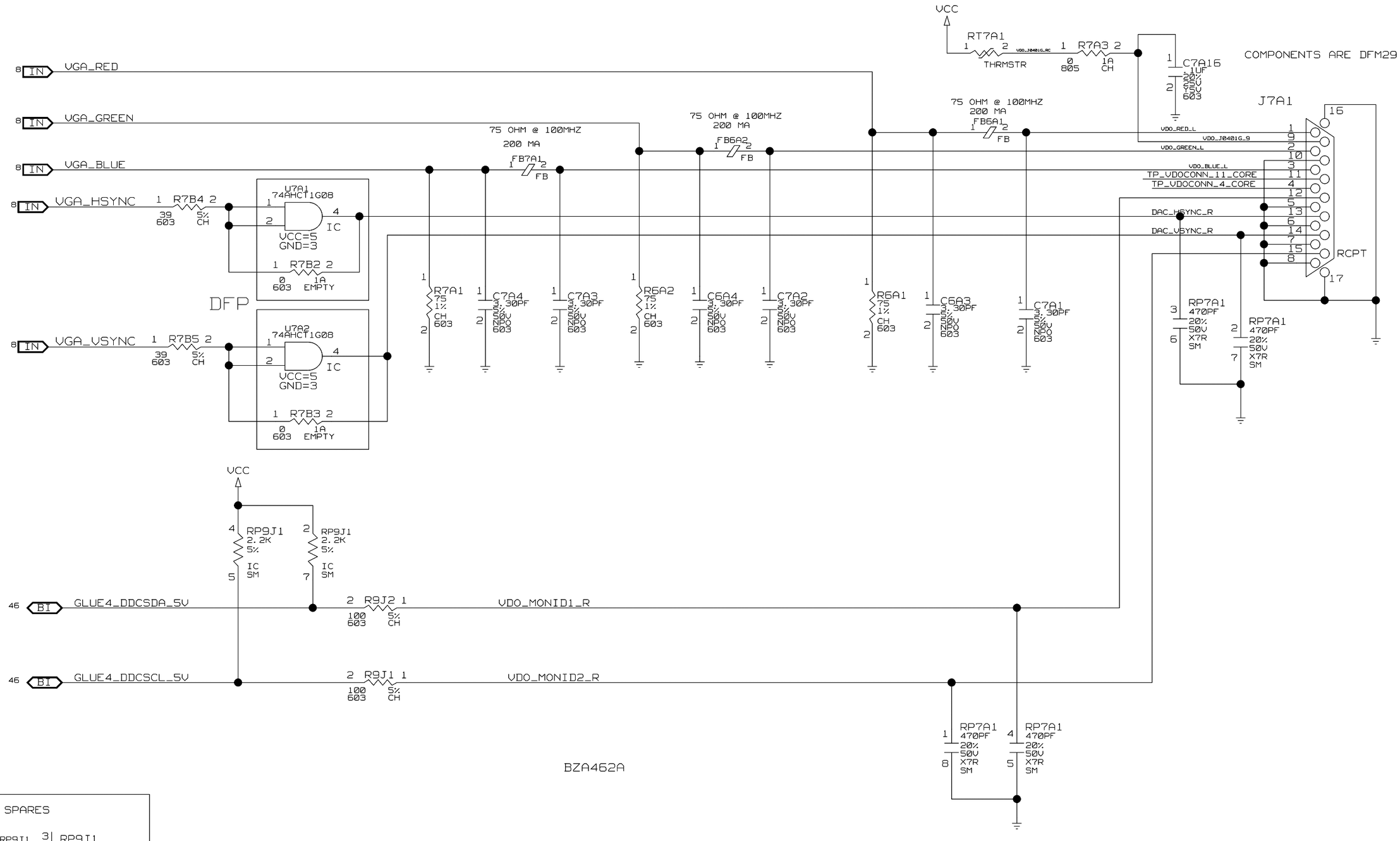
R4D4 100K 603 5% CH

11 17 IN AGP_TYPEDET*

AGP DIGITAL DISPLAY

DRAWING
855GMEFB.SCH.1.17
Mon Apr 19 13:30:51 2004

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 17	REV C2

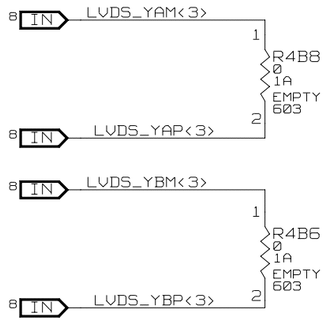


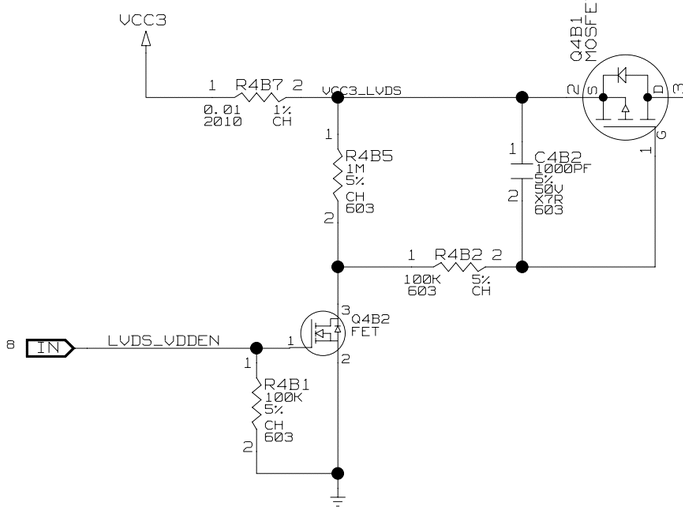
DRAWING
855GMEFB.SCH_1.18
Mon Apr 19 13:30:51 2004

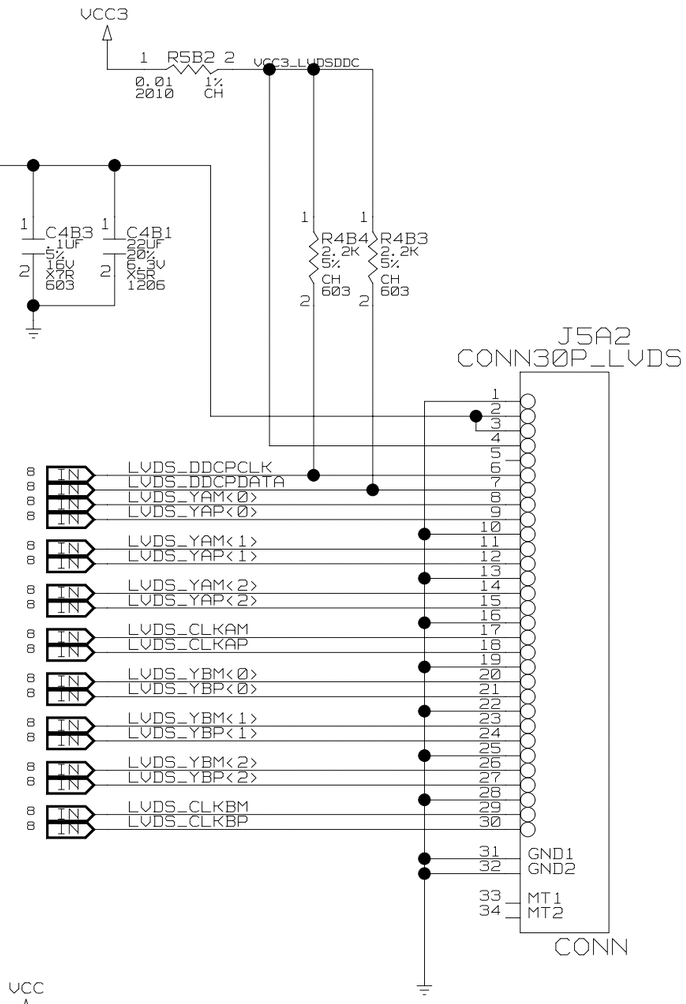
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

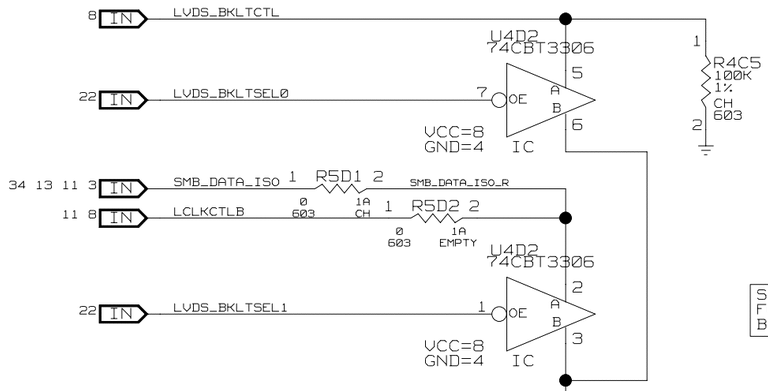
DOCUMENT NUMBER	PAGE	REV
30117601	18	C2

VGA CONNECTOR

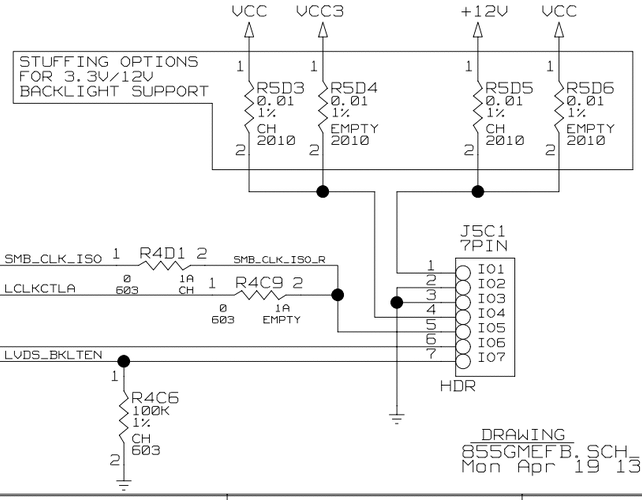








LVDS PANEL BACKLIGHT



BIOS NOTE:
DISABLE BOTH BKLTSEL
LINES BEFORE ENABLING ONE

DRAWING
855GMEFB.SCH_1.19
Mon Apr 19 13:30:52 2004

LVDS CONNECTOR

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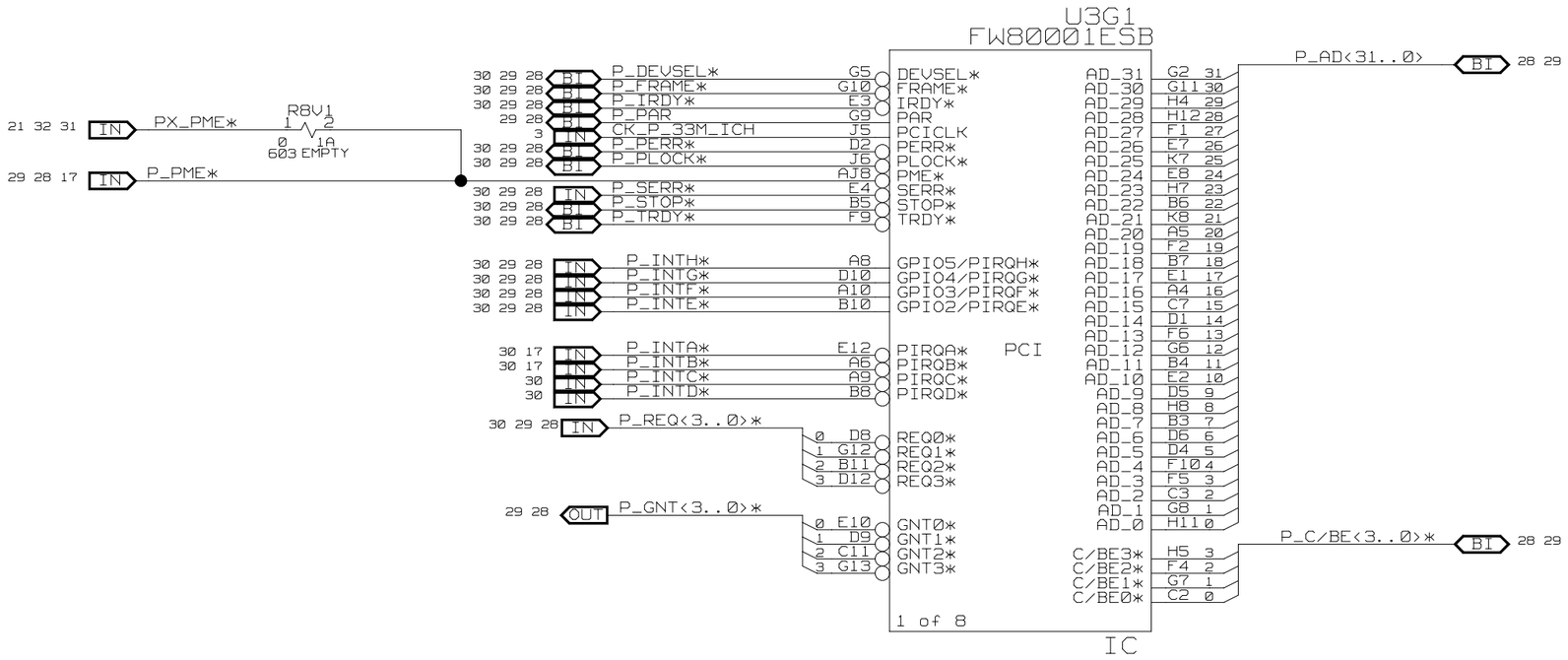
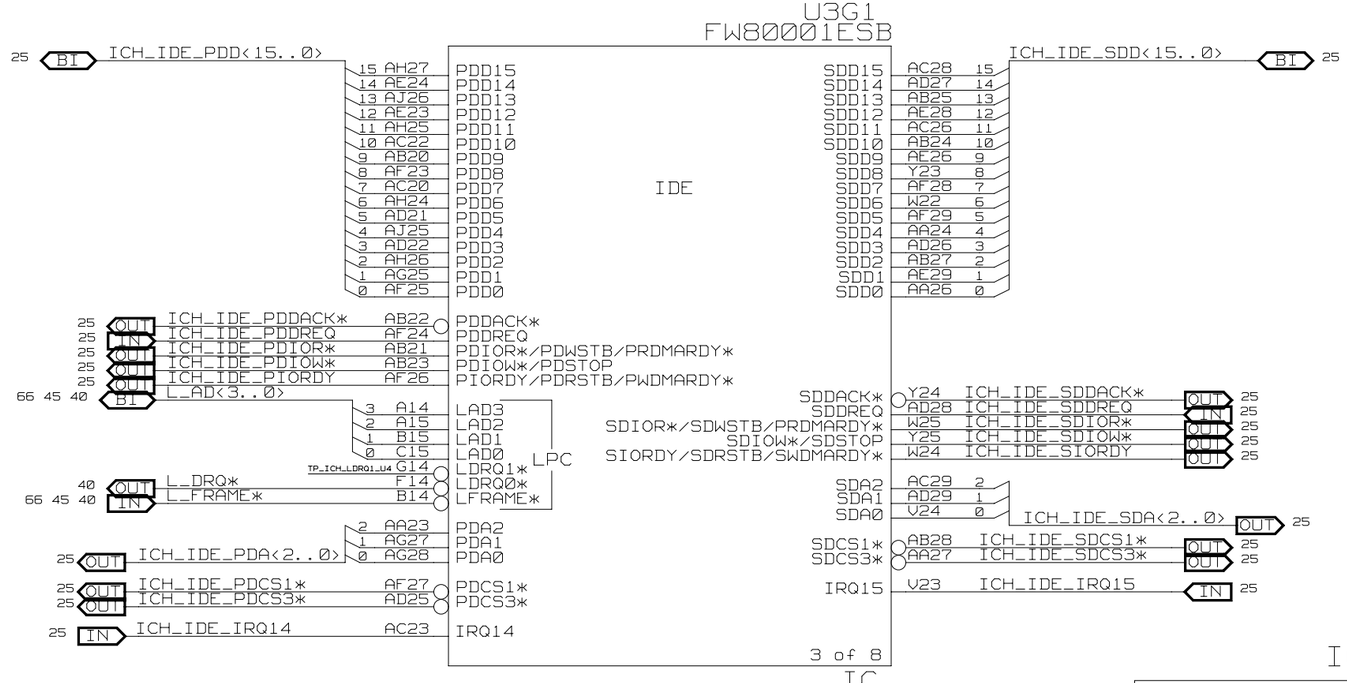
	30117601	19	C2

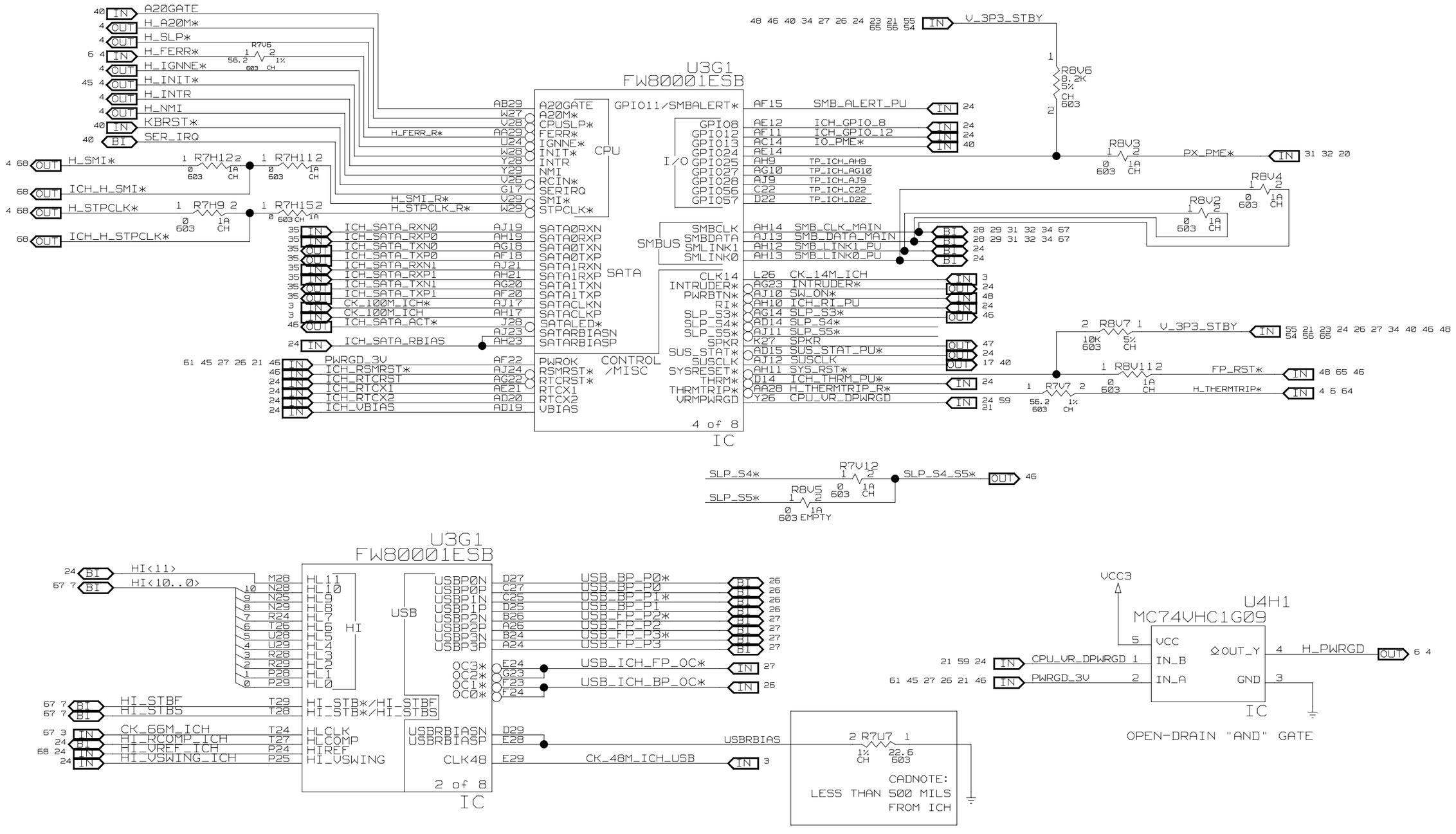




ICH PCI, IDE

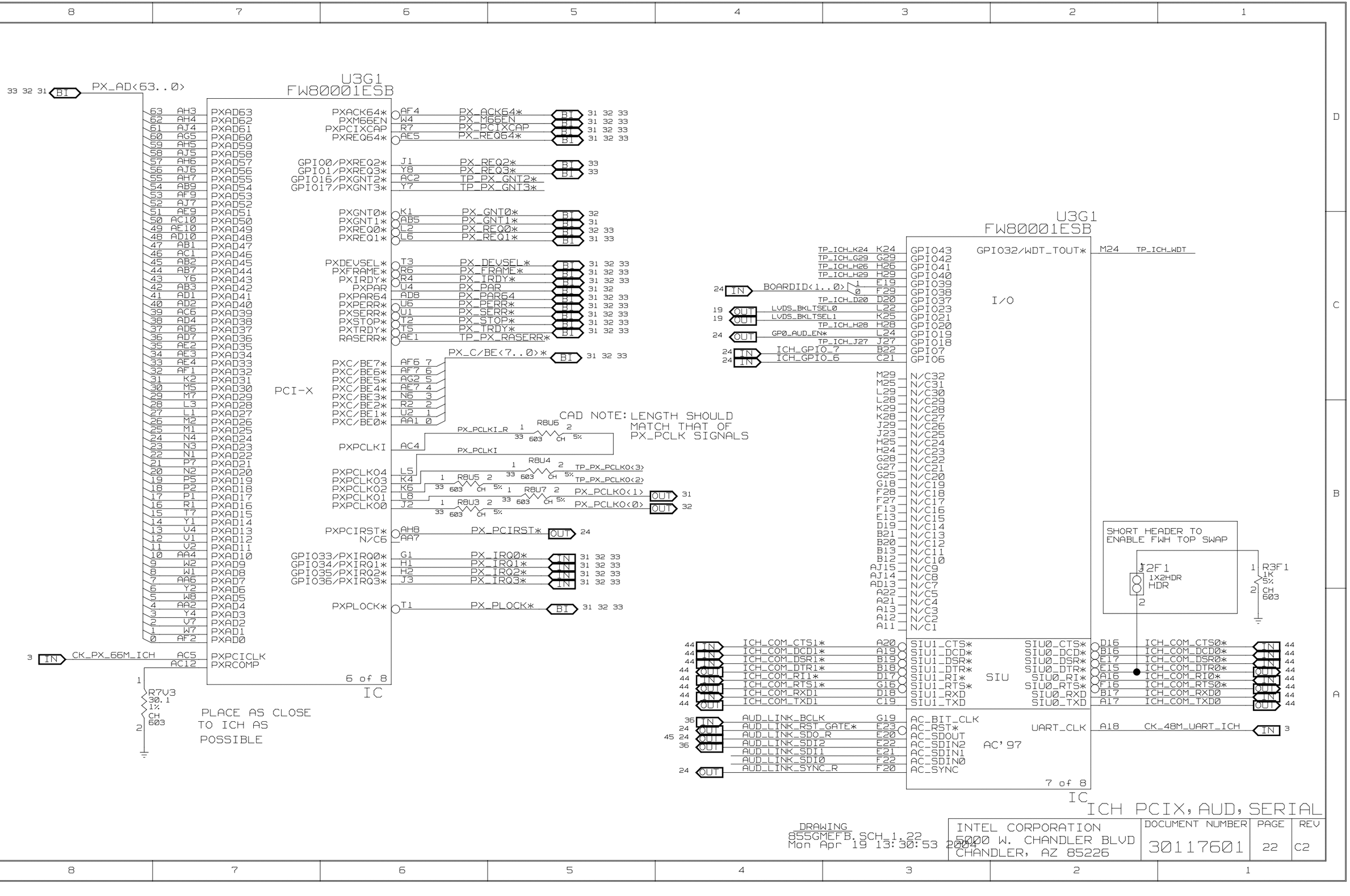
DRAWING
855GMEFB.SCH_1.20
Mon Apr 19 13:30:52 2004

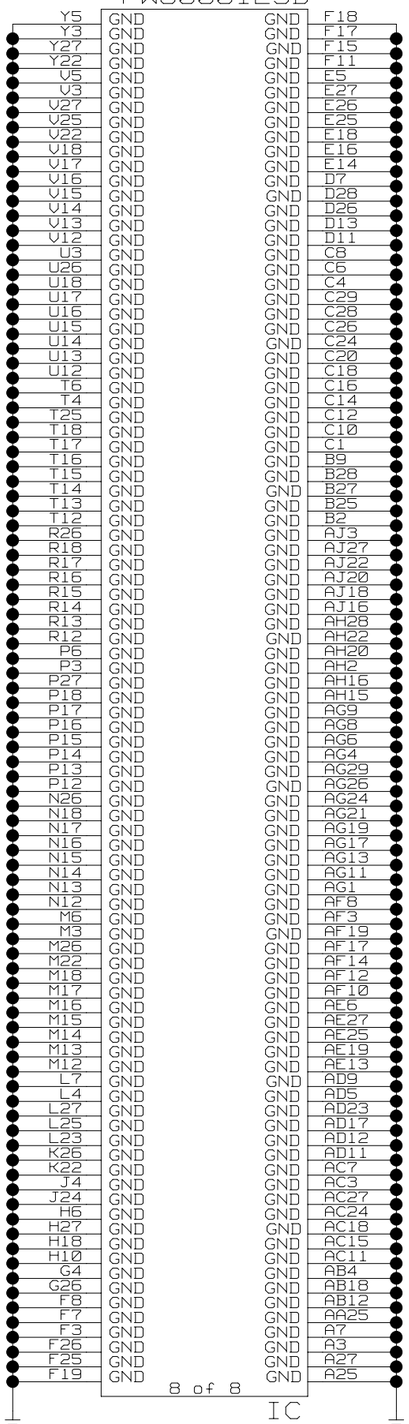
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	20	C2



ICH CPU, PM, SATA, USB, HI

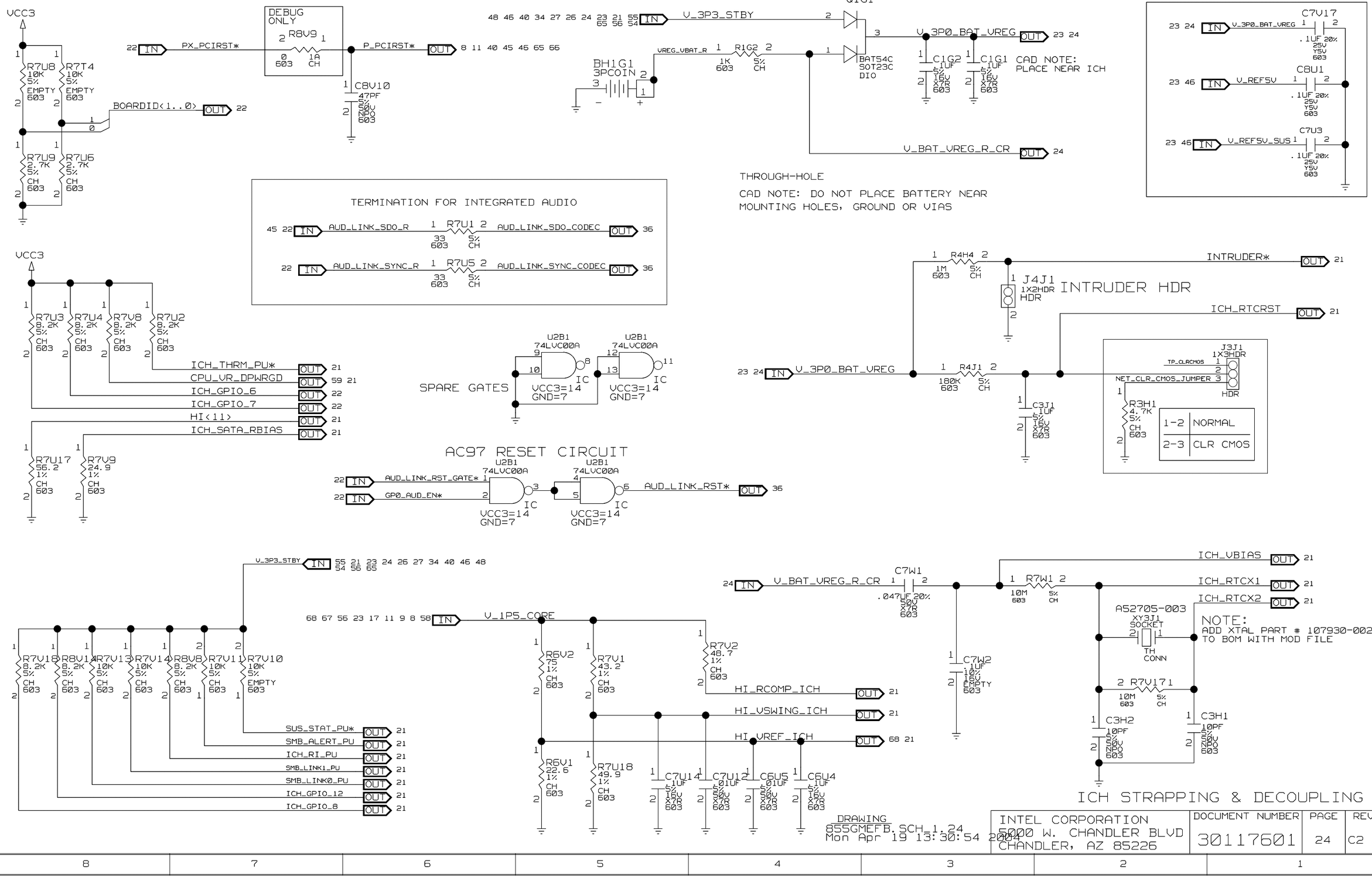
DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.21 Mon Apr 19 13:30:53 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	21	C2


U3G1
FW80001ESB
PCI-X
6 of 8
IC
PXAD63 PXAD62 PXAD61 PXAD60 PXAD59 PXAD58 PXAD57 PXAD56 PXAD55 PXAD54 PXAD53 PXAD52 PXAD51 PXAD50 PXAD49 PXAD48 PXAD47 PXAD46 PXAD45 PXAD44 PXAD43 PXAD42 PXAD41 PXAD40 PXAD39 PXAD38 PXAD37 PXAD36 PXAD35 PXAD34 PXAD33 PXAD32 PXAD31 PXAD30 PXAD29 PXAD28 PXAD27 PXAD26 PXAD25 PXAD24 PXAD23 PXAD22 PXAD21 PXAD20 PXAD19 PXAD18 PXAD17 PXAD16 PXAD15 PXAD14 PXAD13 PXAD12 PXAD11 PXAD10 PXAD9 PXAD8 PXAD7 PXAD6 PXAD5 PXAD4 PXAD3 PXAD2 PXAD1 PXAD0
PXPCICLK
PXRCOMP
CK_PX_66M_ICH
R7V3 30.1 1% CH 603
PLACE AS CLOSE TO ICH AS POSSIBLE
PXACK64* PXM66EN PXPCIXCAP PXREQ64*
PX_ACK64* PX_M66EN PX_PCIXCAP PX_REQ64*
GPI00/PXREQ2* GPI01/PXREQ3* GPI016/PXGNT2* GPI017/PXGNT3*
PX_REQ2* PX_REQ3* TP_PX_GNT2* TP_PX_GNT3*
PXGNT0* PXGNT1* PXREQ0* PXREQ1*
PX_GNT0* PX_GNT1* PX_REQ0* PX_REQ1*
PXDEVSEL* PXFRAME* PXIRDY* PXPAR PXPAR64 PXPERR* PXSERR* PXSTOP* PXTRDY* RASERR*
PX_DEVSEL* PX_FRAME* PX_IRDY* PX_PAR PX_PAR64 PX_PERR* PX_SERR* PX_STOP* PX_TRDY* TP_PX_RASERR*
PX_C/BE<7..0>*
PXC/BE7* PXC/BE6* PXC/BE5* PXC/BE4* PXC/BE3* PXC/BE2* PXC/BE1* PXC/BE0*
PXPCLKI
PX_PCLKI_R
PX_PCLKI
R8U6 33 603 CH 5%
R8U4 R8U5 R8U7 R8U3
PXPCLKO4 PXPCLKO3 PXPCLKO2 PXPCLKO1 PXPCLKO0
TP_PX_PCLKO<3> TP_PX_PCLKO<2> PX_PCLKO<1> PX_PCLKO<0>
PXPCIRST* N/C5
PX_PCIRST*
GPI033/PXIRQ0* GPI034/PXIRQ1* GPI035/PXIRQ2* GPI036/PXIRQ3*
PX_IRQ0* PX_IRQ1* PX_IRQ2* PX_IRQ3*
PXPLOCK*
PX_PLOCK*
CAD NOTE: LENGTH SHOULD MATCH THAT OF PX_PCLK SIGNALS
U3G1
FW80001ESB
I/O
GPIO43 GPIO42 GPIO41 GPIO40 GPIO39 GPIO38 GPIO37 GPIO23 GPIO21 GPIO20 GPIO19 GPIO18 GPIO7 GPIO6
GPIO32/WDT_TOUT*
TP_ICH_WDT
BOARDID<1..0>
LVDS_BKLTSEL0 LVDS_BKLTSEL1 GP0_AUD_EN* ICH_GPIO_7 ICH_GPIO_6
TP_ICH_K24 TP_ICH_G29 TP_ICH_H26 TP_ICH_H29 TP_ICH_D20 TP_ICH_H28 TP_ICH_J27
N/C32 N/C31 N/C30 N/C29 N/C28 N/C27 N/C26 N/C25 N/C24 N/C23 N/C22 N/C21 N/C20 N/C19 N/C18 N/C17 N/C16 N/C15 N/C14 N/C13 N/C12 N/C11 N/C10 N/C9 N/C8 N/C7 N/C5 N/C4 N/C3 N/C2 N/C1
SHORT HEADER TO ENABLE FWH TOP SWAP
J2F1 1X2HDR HDR
R3F1 1K 5% CH 603
SIU
SIU1_CTS* SIU1_DCD* SIU1_DSR* SIU1_DTR* SIU1_RI* SIU1_RTS* SIU1_RXD SIU1_TXD
SIU0_CTS* SIU0_DCD* SIU0_DSR* SIU0_DTR* SIU0_RI* SIU0_RTS* SIU0_RXD SIU0_TXD
ICH_COM_CTS1* ICH_COM_DCD1* ICH_COM_DSR1* ICH_COM_DTR1* ICH_COM_RI1* ICH_COM_RTS1* ICH_COM_RXD1 ICH_COM_TXD1
ICH_COM_CTS0* ICH_COM_DCD0* ICH_COM_DSR0* ICH_COM_DTR0* ICH_COM_RI0* ICH_COM_RTS0* ICH_COM_RXD0 ICH_COM_TXD0
AC'97
AC_BIT_CLK AC_RST* AC_SDOUT AC_SDIN2 AC_SDIN1 AC_SDIN0 AC_SYNC
AUD_LINK_BCLK AUD_LINK_RST_GATE* AUD_LINK_SDO_R AUD_LINK_SDI2 AUD_LINK_SDI1 AUD_LINK_SDI0 AUD_LINK_SYNC_R
UART_CLK
CK_48M_UART_ICH
7 of 8
IC
ICH PCIX, AUD, SERIAL
DRAWING 855GMEFB.SCH_1.22 Mon Apr 19 13:30:53 2004
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226
DOCUMENT NUMBER 30117601
PAGE 22
REV C2



ICH POWER, GND

DRAWING				
855GMEFB.SCH.1.23 Mon Apr 19 13:30:53 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 23	REV C2


VCC3
R7U8 10K 5% EMPTY 603
R7T4 10K 5% EMPTY 603
R7U9 2.7K 5% CH 603
R7U6 2.7K 5% CH 603
BOARDID<1..0>
OUT 22
DEBUG ONLY
R8U9 0 603 1A CH
IN 22 PX_PCIRST*
P_PCIRST*
OUT 8 11 40 45 46 65 66
C8U10 47PF 5% 50V NP0 603
48 46 40 34 27 26 24 23 21 55 65 56 54
IN V_3P3_STBY
Q1G1
BAT54C SOT23C DIO
VREG_VBAT_R
R1G2 1K 603 5% CH
BH1G1 3PCOIN
V_3P0_BAT_VREG
OUT 23 24
C1G2 1UF 5% 16V X7R 603
C1G1 1UF 5% 16V X7R 603
CAD NOTE: PLACE NEAR ICH
V_BAT_VREG_R_CR
OUT 24
THROUGH-HOLE
CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS
ATTRIBUTES:
C7V17 .1UF 20% 25V Y5V 603
C8U1 .1UF 20% 25V Y5V 603
C7U3 .1UF 20% 25V Y5V 603
TERMINATION FOR INTEGRATED AUDIO
45 22 IN AUD_LINK_SDO_R
R7U1 33 603 5% CH
AUD_LINK_SDO_CODEC OUT 36
22 IN AUD_LINK_SYNC_R
R7U5 33 603 5% CH
AUD_LINK_SYNC_CODEC OUT 36
VCC3
R7U3 8.2K 5% CH 603
R7U4 8.2K 5% CH 603
R7U8 8.2K 5% CH 603
R7U2 8.2K 5% CH 603
ICH_THRM_PU* OUT 21
CPU_VR_DPWRGD OUT 59 21
ICH_GPIO_6 OUT 22
ICH_GPIO_7 OUT 22
HI<11> OUT 21
ICH_SATA_RBIAS OUT 21
R7U17 56.2 1% CH 603
R7U9 24.9 1% CH 603
SPARE GATES
U2B1 74LVC00A IC VCC3=14 GND=7
U2B1 74LVC00A IC VCC3=14 GND=7
AC97 RESET CIRCUIT
22 IN AUD_LINK_RST_GATE*
22 IN GP0_AUD_EN*
U2B1 74LVC00A IC VCC3=14 GND=7
U2B1 74LVC00A IC VCC3=14 GND=7
AUD_LINK_RST* OUT 36
R4H4 1M 603 5% CH
INTRUDER* OUT 21
J4J1 1X2HDR HDR
INTRUDER HDR
ICH_RTCRST OUT 21
23 24 IN V_3P0_BAT_VREG
R4J1 180K 603 5% CH
C3J1 1UF 5% 16V X7R 603
J3J1 1X3HDR HDR
TP_CLRCMOS
NET_CLR_CMOS_JUMPER
R3H1 4.7K 5% CH 603
1-2 NORMAL
2-3 CLR CMOS
V_3P3_STBY IN 55 21 23 24 26 27 34 40 46 48
68 67 56 23 17 11 9 8 58 IN V_1P5_CORE
R7U18 8.2K 5% CH 603
R8U14 8.2K 5% CH 603
R7U13 10K 5% CH 603
R7U14 10K 5% CH 603
R8U8 8.2K 5% CH 603
R7U11 10K 5% CH 603
R7U10 10K 5% EMPTY 603
SUS_STAT_PU* OUT 21
SMB_ALERT_PU OUT 21
ICH_RI_PU OUT 21
SMB_LINK1_PU OUT 21
SMB_LINK0_PU OUT 21
ICH_GPIO_12 OUT 21
ICH_GPIO_8 OUT 21
R6V2 75 1% CH 603
R7V1 43.2 1% CH 603
R7V2 48.7 1% CH 603
R6V1 22.6 1% CH 603
R7U18 49.9 1% CH 603
HI_RCOMP_ICH OUT 21
HI_VSWING_ICH OUT 21
HI_VREF_ICH OUT 68 21
C7U14 .1UF 5% 16V X7R 603
C7U12 .01UF 5% 50V X7R 603
C6U5 .01UF 5% 50V X7R 603
C6U4 .1UF 5% 16V X7R 603
24 IN V_BAT_VREG_R_CR
C7W1 .047UF 20% 50V X7R 603
C7W2 1UF 10% 16V EMPTY 603
ICH_VBIAS OUT 21
R7W1 10M 603 5% CH
ICH_RTCX1 OUT 21
ICH_RTCX2 OUT 21
AS2705-003
XY3J1 SOCKET TH CONN
NOTE: ADD XTAL PART # 107930-002 TO BOM WITH MOD FILE
R7V171 10M 603 5% CH
C3H2 10PF 5% 50V NP0 603
C3H1 10PF 5% 50V NP0 603
ICH STRAPPING & DECOUPLING
DRAWING 855GMEFB.SCH_1.24
Mon Apr 19 13:30:54 2004
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
DOCUMENT NUMBER 30117601
PAGE 24
REV C2

DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS

20 IN ICH_IDE_SDD<15..0>
20 IN ICH_IDE_PDD<15..0>

VCC3

2 R5V4 1
4.7K 5% 603 CH

46 IN IDE_RST*

2 R4H3 1
33 5% 603 CH

J4H2
2X20HDR_20

PRIMARY IDE CONNECTOR

20 OUT ICH_IDE_PDDREQ
20 IN ICH_IDE_PDIOW*
20 IN ICH_IDE_PDIOR*
20 OUT ICH_IDE_PIORDY
20 IN ICH_IDE_PDDACK*
20 OUT ICH_IDE_IRQ14
20 IN ICH_IDE_PDA<1>
20 IN ICH_IDE_PDA<0>
20 IN ICH_IDE_PDCS1*
20 IN ICH_IDE_PDCS3*
20 IN ICH_IDE_PDA<2>

2 R5V3 1
8.2K 5% 603 CH

IDE_PRI_RST_R

TP_IDE_PRI_32

HDR

GPIO_DMA66_DETECT_PRI OUT 45

IDE_PRI_ACT* OUT 46

2 R4V2 1
15K 5% 603 CH

1 C5V2
.047UF 20% 50V EMPTY 603
2
"X7R" (+/- 10%)

CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

VCC3

2 R5V2 1
4.7K 5% 603 CH

2 R4H2 1
33 5% 603 CH

J4H1
2X20HDR_20

IDE_SEC_RST_R

SECONDARY IDE CONNECTOR

20 OUT ICH_IDE_SDDREQ
20 IN ICH_IDE_SDIOW*
20 IN ICH_IDE_SDIOR*
20 OUT ICH_IDE_SIORDY
20 IN ICH_IDE_SDDACK*
20 OUT ICH_IDE_IRQ15
20 IN ICH_IDE_SDA<1>
20 IN ICH_IDE_SDA<0>
20 IN ICH_IDE_SDCS1*
20 IN ICH_IDE_SDCS3*
20 IN ICH_IDE_SDA<2>

2 R5V1 1
8.2K 5% 603 CH

TP_IDE_SEC_32

HDR

GPIO_DMA66_DETECT_SEC OUT 45

IDE_SEC_ACT* OUT 46

2 R4V1 1
15K 5% 603 CH

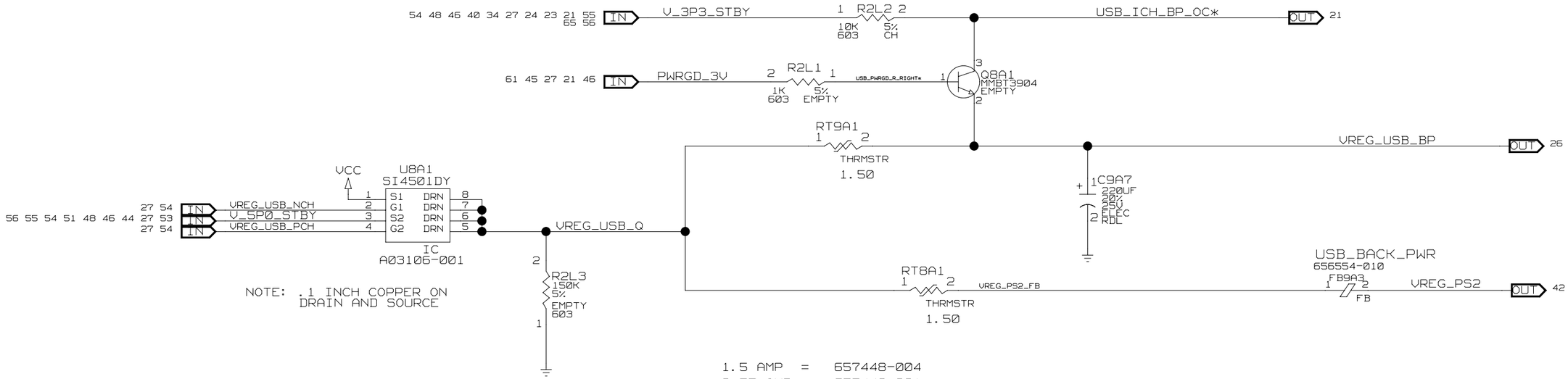
1 C5V1
.047UF 20% 50V EMPTY 603
2
"X7R" (+/- 10%)

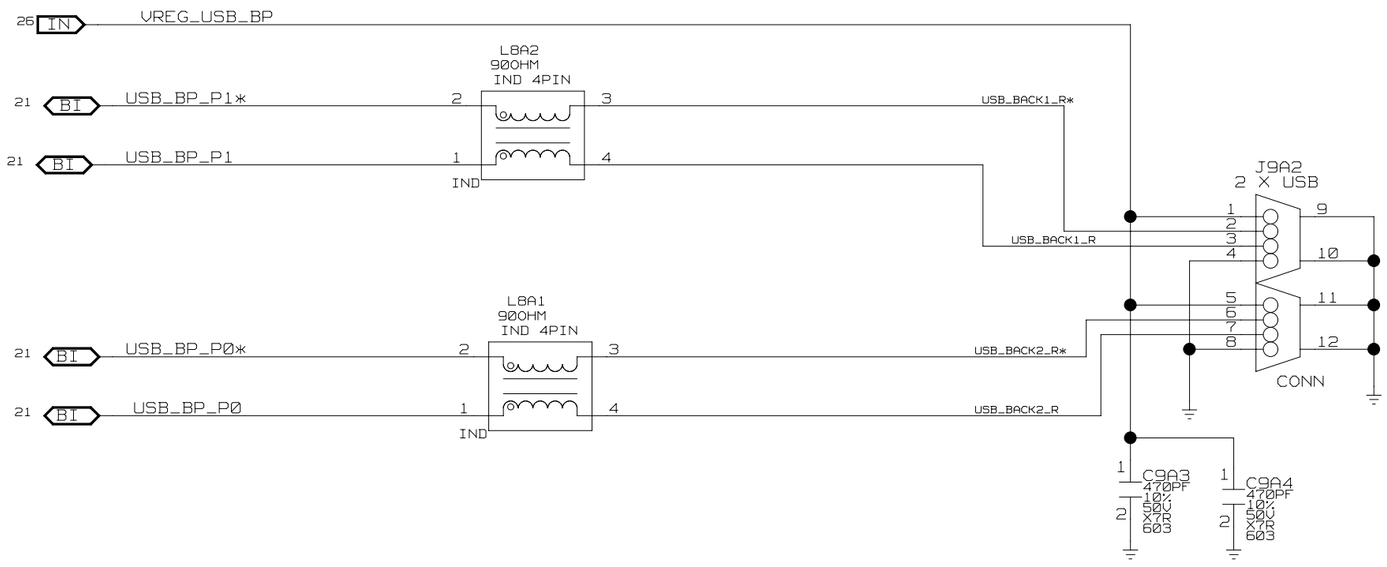
CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

IDE CONNECTORS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.25 Mon Apr 19 13:30:54 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	25	C2





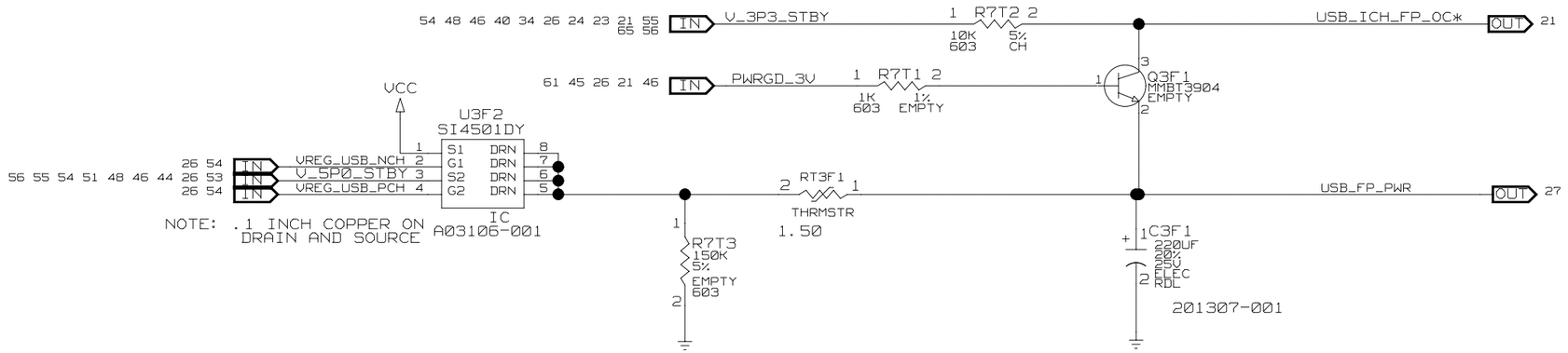
CAD NOTE:
PLACE NEAR USB CONN

USB BACK PANEL & PS/2

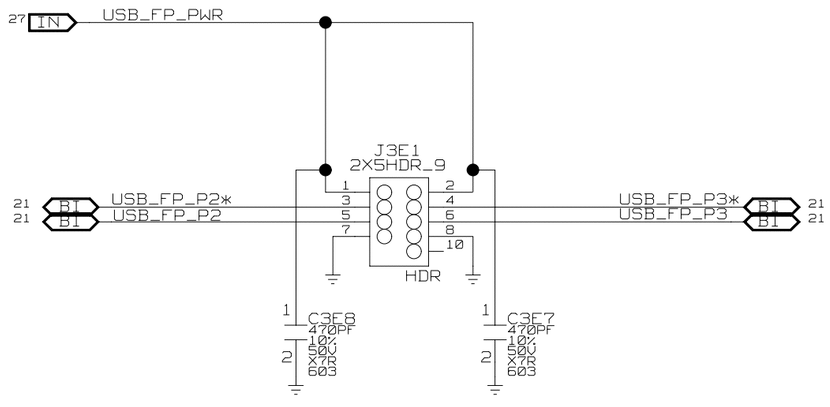
DRAWING
855GMEFB.SCH_1.26
Mon Apr 19 13:30:55 2004

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	26	C2

FRONT PANEL USB POWER

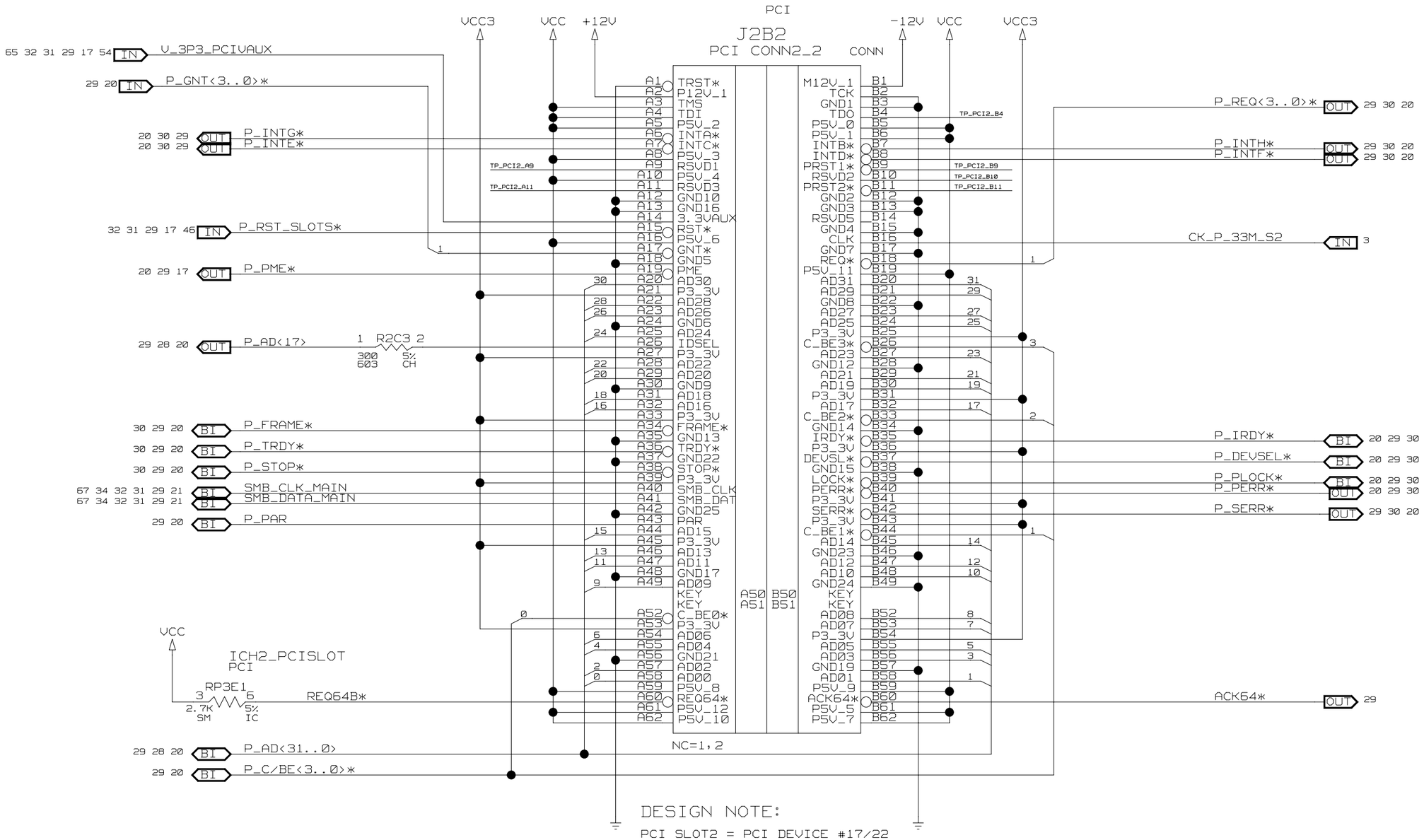


CAD NOTE;
TRACE ROUTING IS 7.5 MIL, 7.5 MIL SPACING



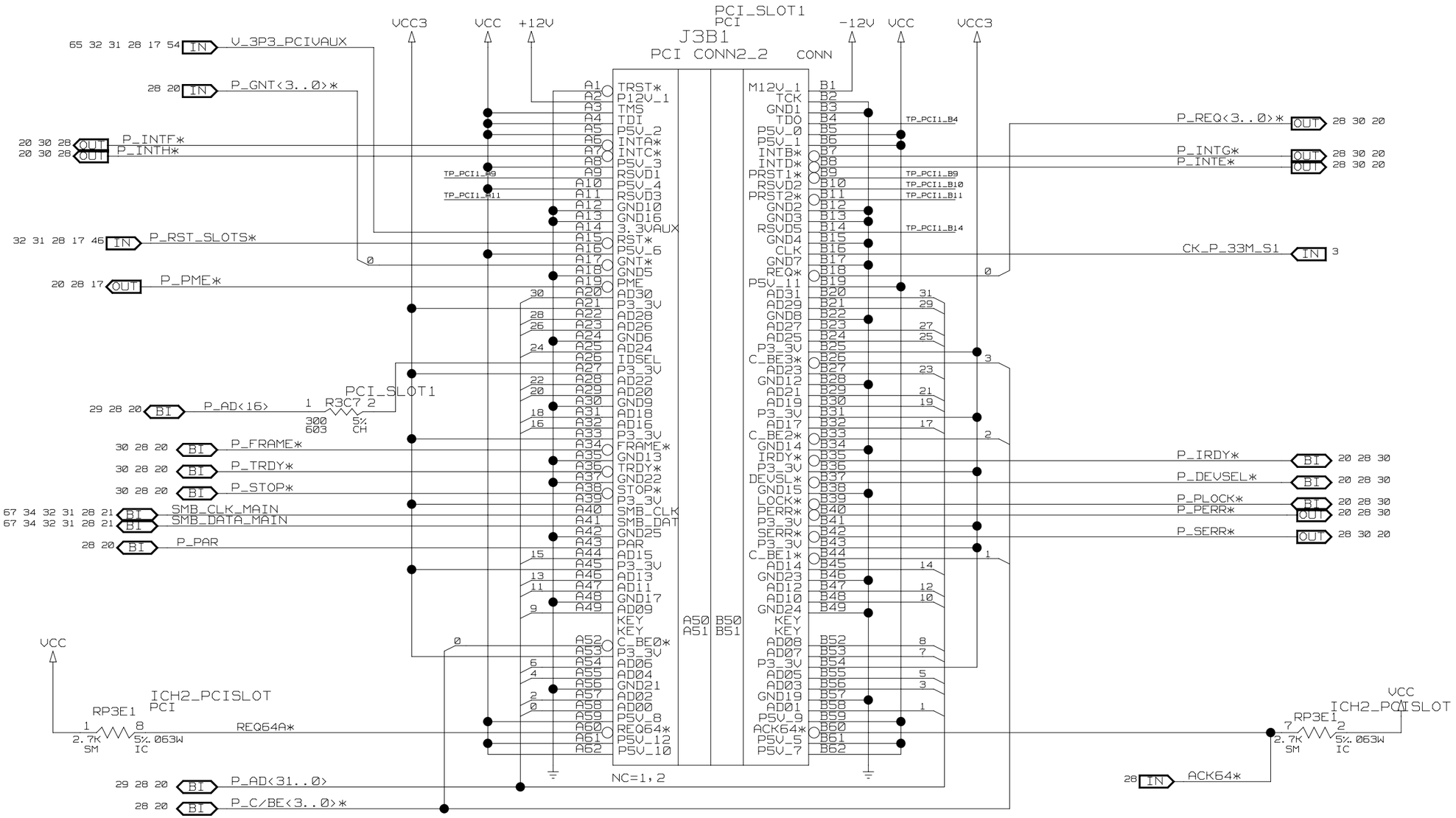
USB FRONT PANEL

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.27 Mon Apr 19 13:30:55 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	27	C2



PCI SLOT 2

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.28 Mon Apr 19 13:30:55 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	28	C2



DESIGN NOTE:

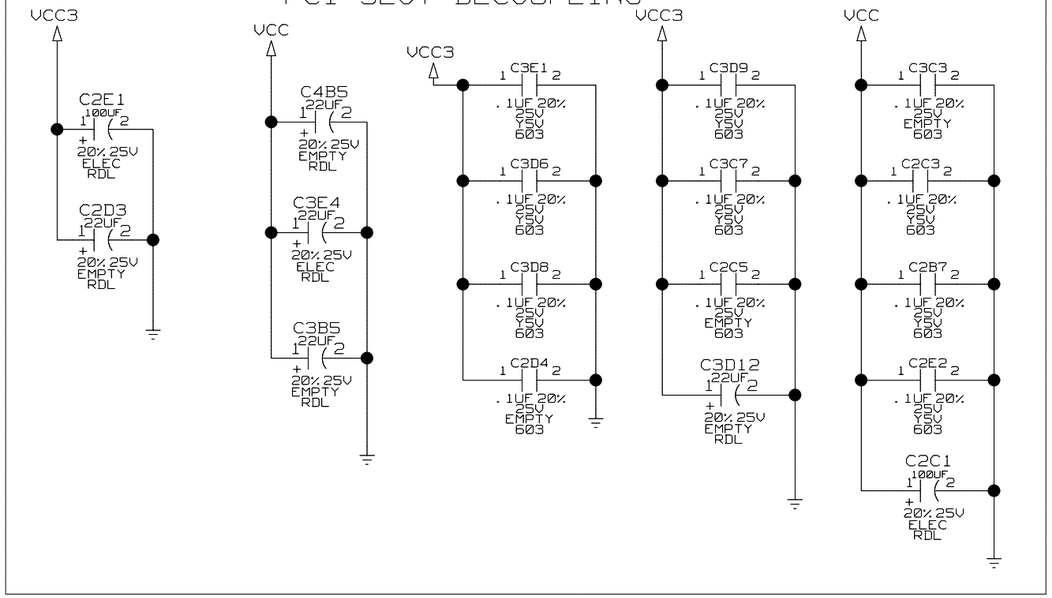
PCI SLOT1 = PCI DEVICE #16
REQ/GNT PAIR = #0
IRQ MAP A : B : C : D
F : G : H : E

CLOSEST TO AGP

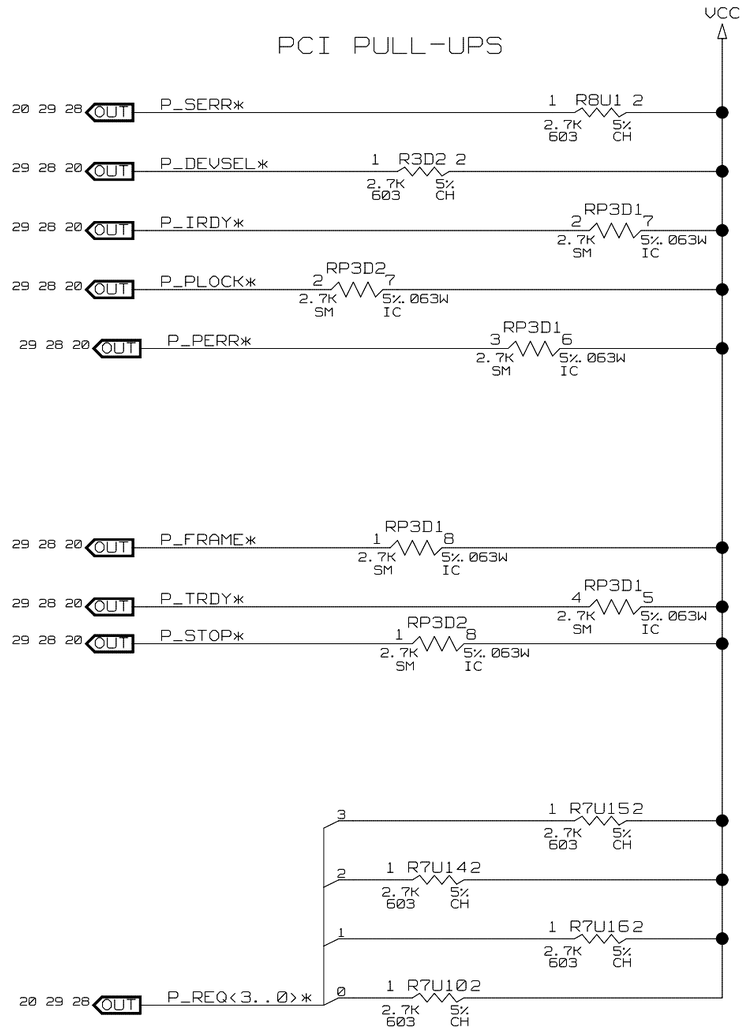
PCI SLOT 1

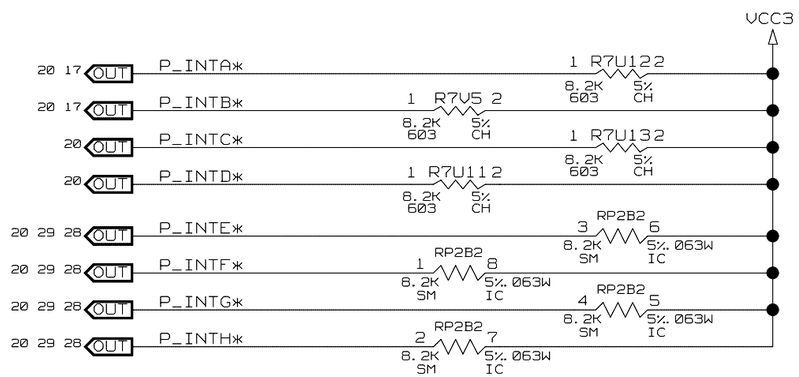
DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.29 Mon Apr 19 13:30:55 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	29	C2

PCI SLOT DECOUPLING

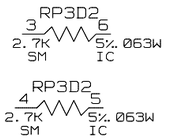


PCI PULL-UPS





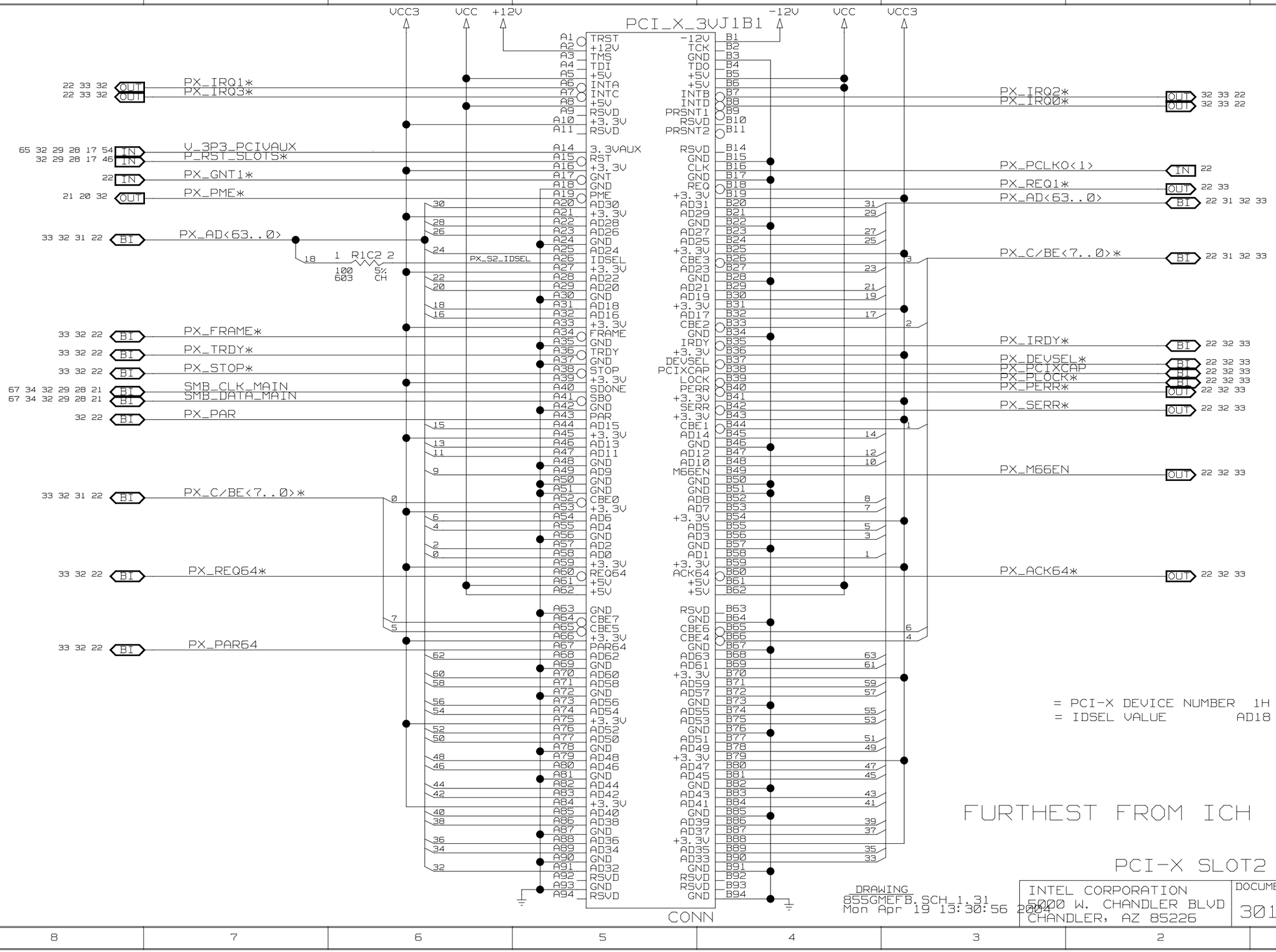
SPARE SECTIONS

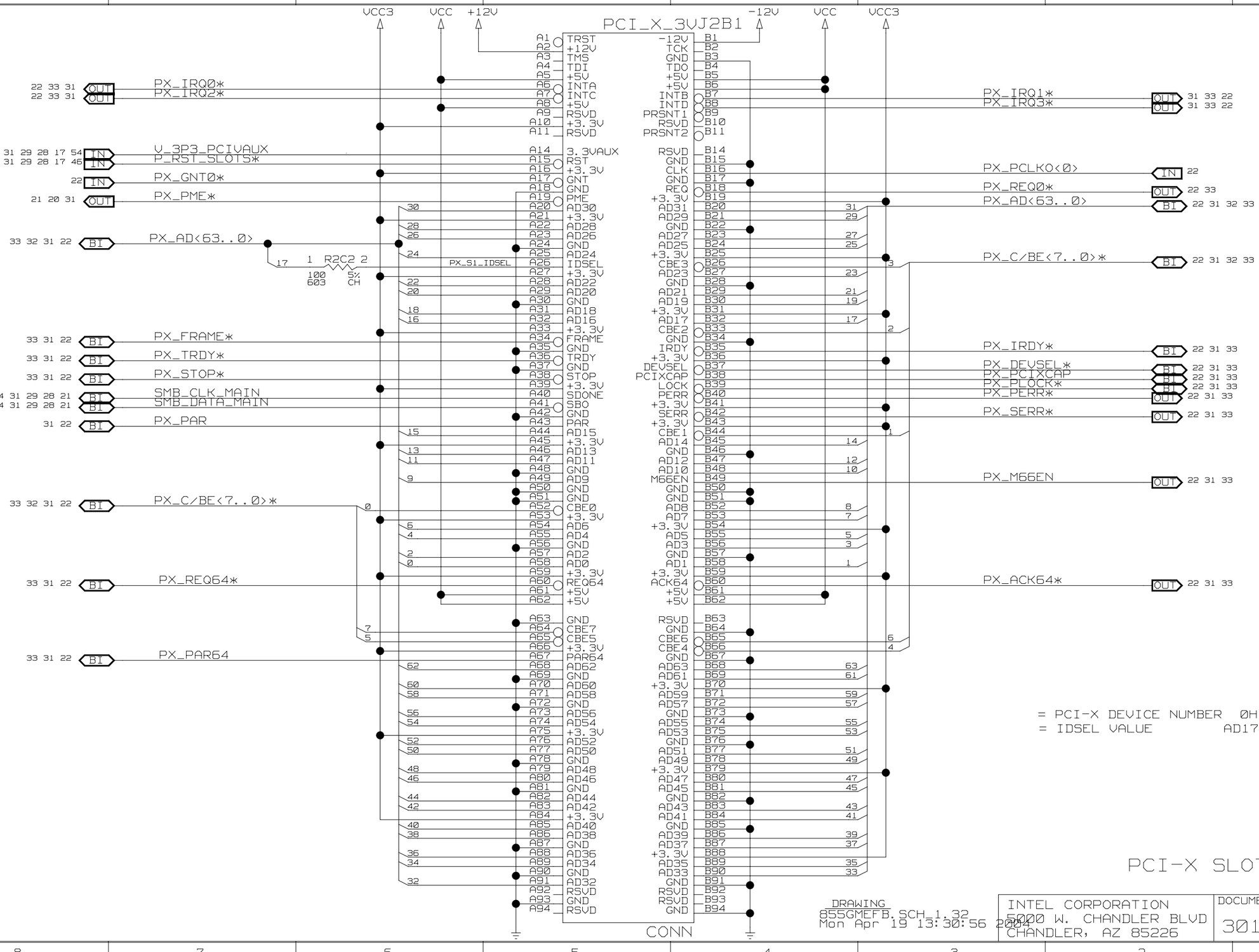


PCI TERMINATION AND DECOUPLING

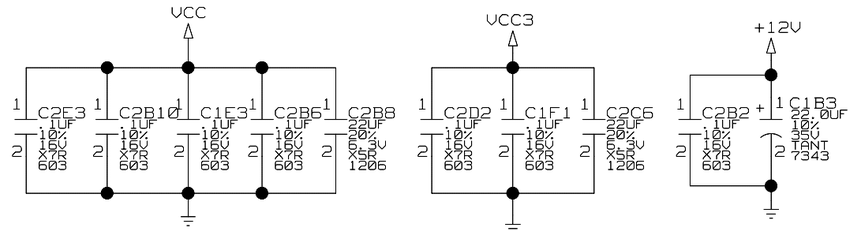
DRAWING
855GMEFB.SCH_1.30
Mon Apr 19 13:30:56 2004

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	30	C2

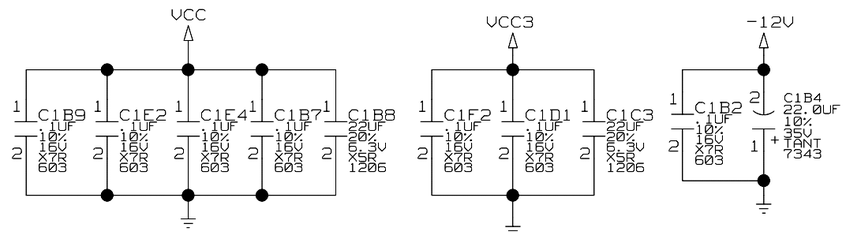

PCI_X_3VJ1B1
VCC3
VCC
+12V
-12V
PX_IRQ1*
PX_IRQ3*
V_3P3_PCIVAUX
P_RST_SLOTS*
PX_GNT1*
PX_PME*
PX_AD<63..0>
PX_FRAME*
PX_TRDY*
PX_STOP*
SMB_CLK_MAIN
SMB_DATA_MAIN
PX_PAR
PX_C/BE<7..0>*
PX_REQ64*
PX_PAR64
PX_S2_IDSEL
R1C2 2
100
603
5%
CH
PX_IRQ2*
PX_IRQ0*
PX_PCLKO<1>
PX_REQ1*
PX_AD<63..0>
PX_C/BE<7..0>*
PX_IRDY*
PX_DEVSEL*
PX_PCIXCAP
PX_PLOCK*
PX_PERR*
PX_SERR*
PX_M66EN
PX_ACK64*
= PCI-X DEVICE NUMBER 1H
= IDSEL VALUE AD18
FURTHEST FROM ICH
PCI-X SLOT2
CONN
DRAWING
855GMEFB.SCH_1.31
Mon Apr 19 13:30:56 2004
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
DOCUMENT NUMBER
30117601
PAGE
31
REV
C2


PCI_X_3VJ2B1
VCC3
VCC
+12V
-12V
PX_IRQ0*
PX_IRQ2*
V_3P3_PCIVAUX
P_RST_SLOTS*
PX_GNT0*
PX_PME*
PX_AD<63..0>
R2C2
100
603
5%
CH
PX_S1_IDSEL
PX_FRAME*
PX_TRDY*
PX_STOP*
SMB_CLK_MAIN
SMB_DATA_MAIN
PX_PAR
PX_C/BE<7..0>*
PX_REQ64*
PX_PAR64
PX_IRQ1*
PX_IRQ3*
PX_PCLKO<0>
PX_REQ0*
PX_AD<63..0>
PX_C/BE<7..0>*
PX_IRDY*
PX_DEVSEL*
PX_PCIXCAP
PX_PLOCK*
PX_PERR*
PX_SERR*
PX_M66EN
PX_ACK64*
CONN
= PCI-X DEVICE NUMBER 0H
= IDSEL VALUE AD17
PCI-X SLOT1
DRAWING
855GMEFB.SCH_1.32
Mon Apr 19 13:30:56 2004
INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226
DOCUMENT NUMBER
30117601
PAGE
32
REV
C2

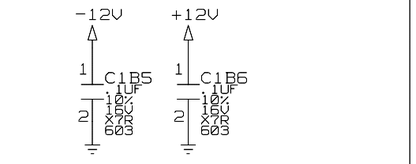
PCI-X SLOT 1 DECOUPLING

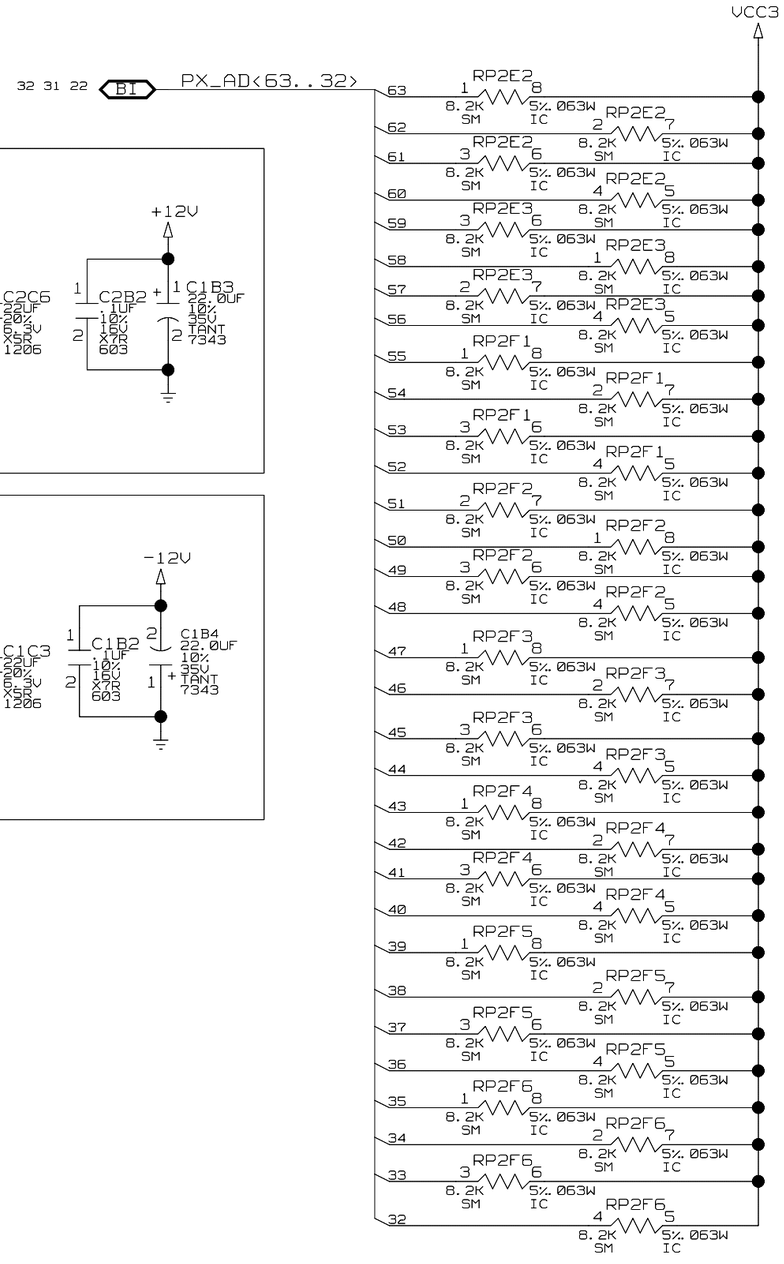


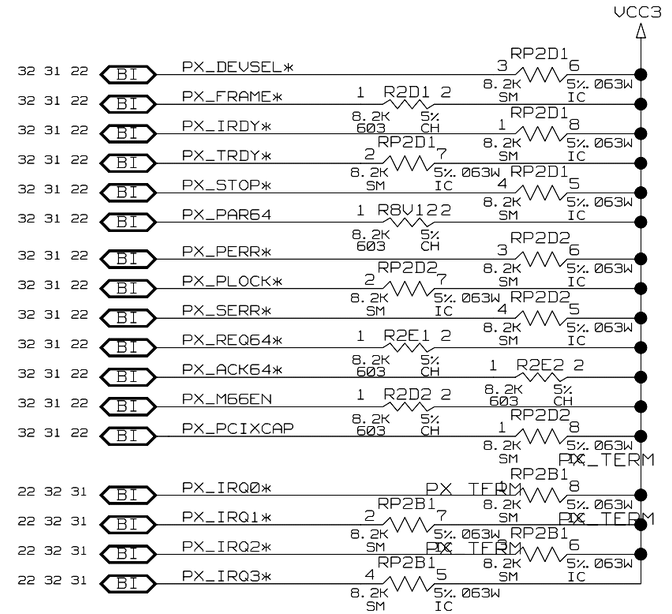
PCI-X SLOT 2 DECOUPLING

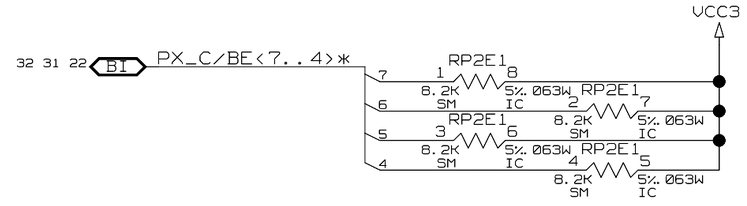


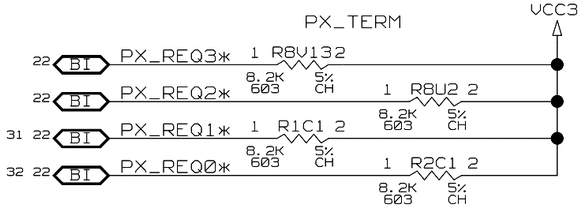
PCI-X SHARED DECOUPLING





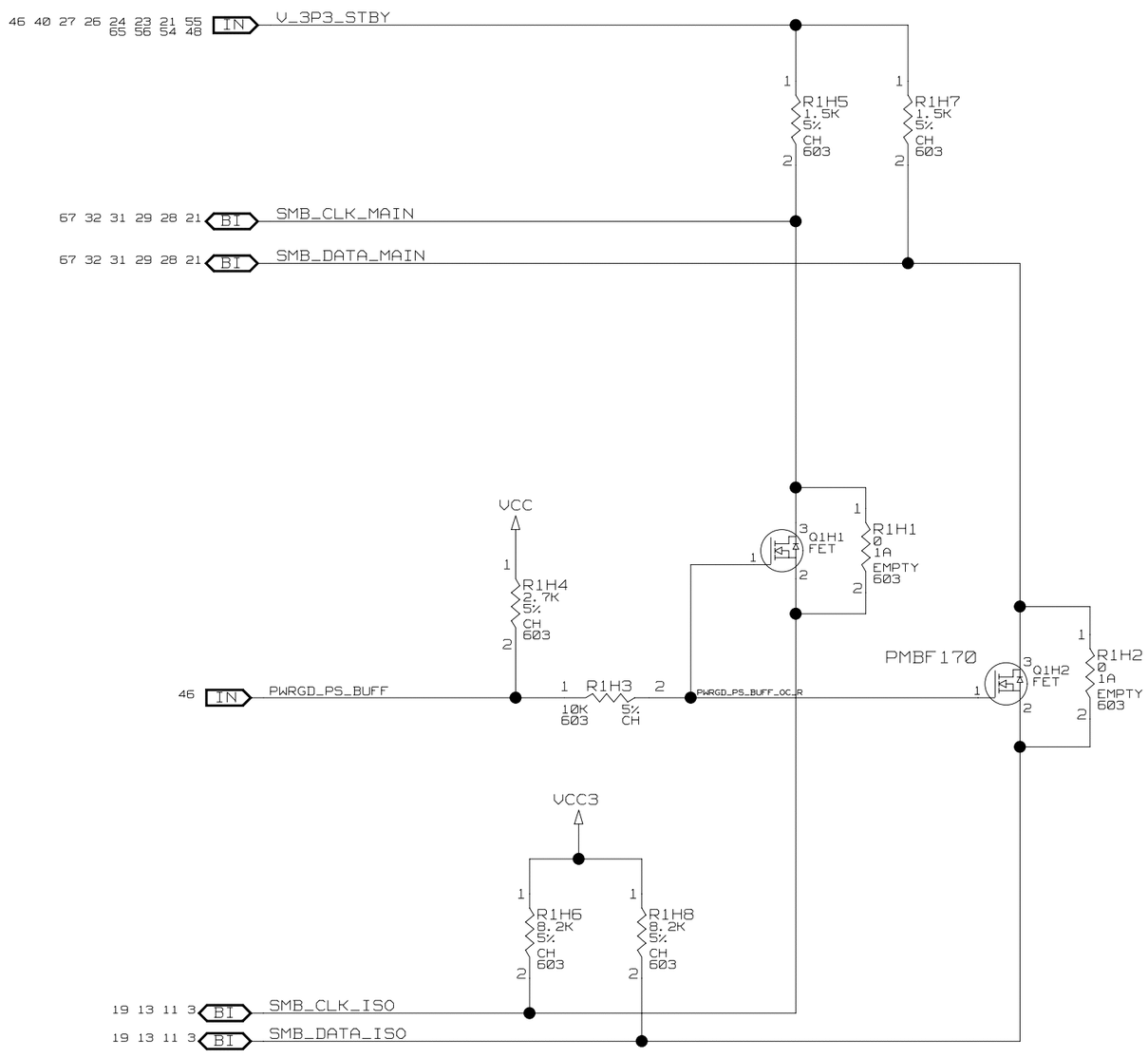


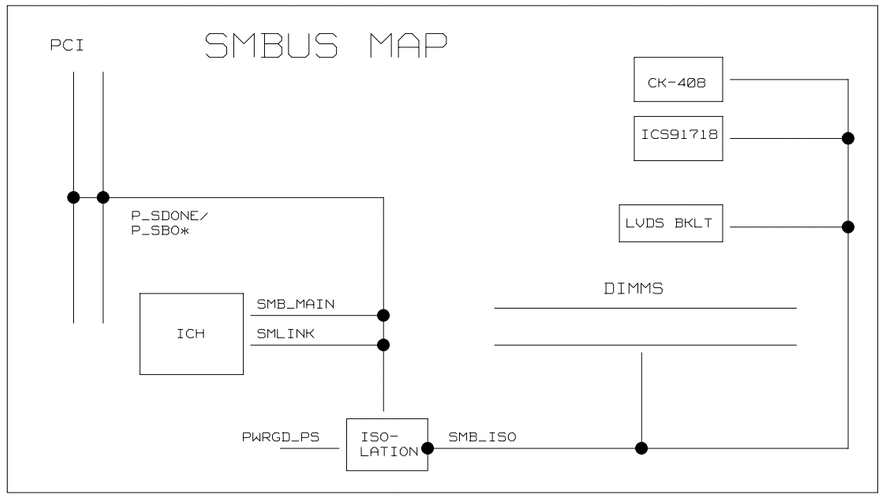




PCI-X TERMINATION

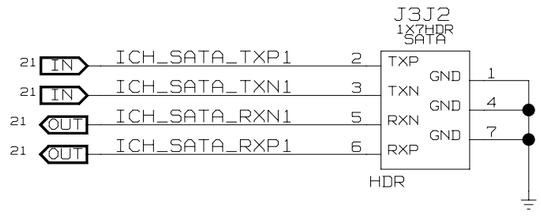
DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.33 Mon Apr 19 13:30:57 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	33	C2





SMBUS ISOLATION CIRCUIT

DRAWING				
855GMEFB.SCH.1.34 Mon Apr 19 13:30:57 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 34	REV C2

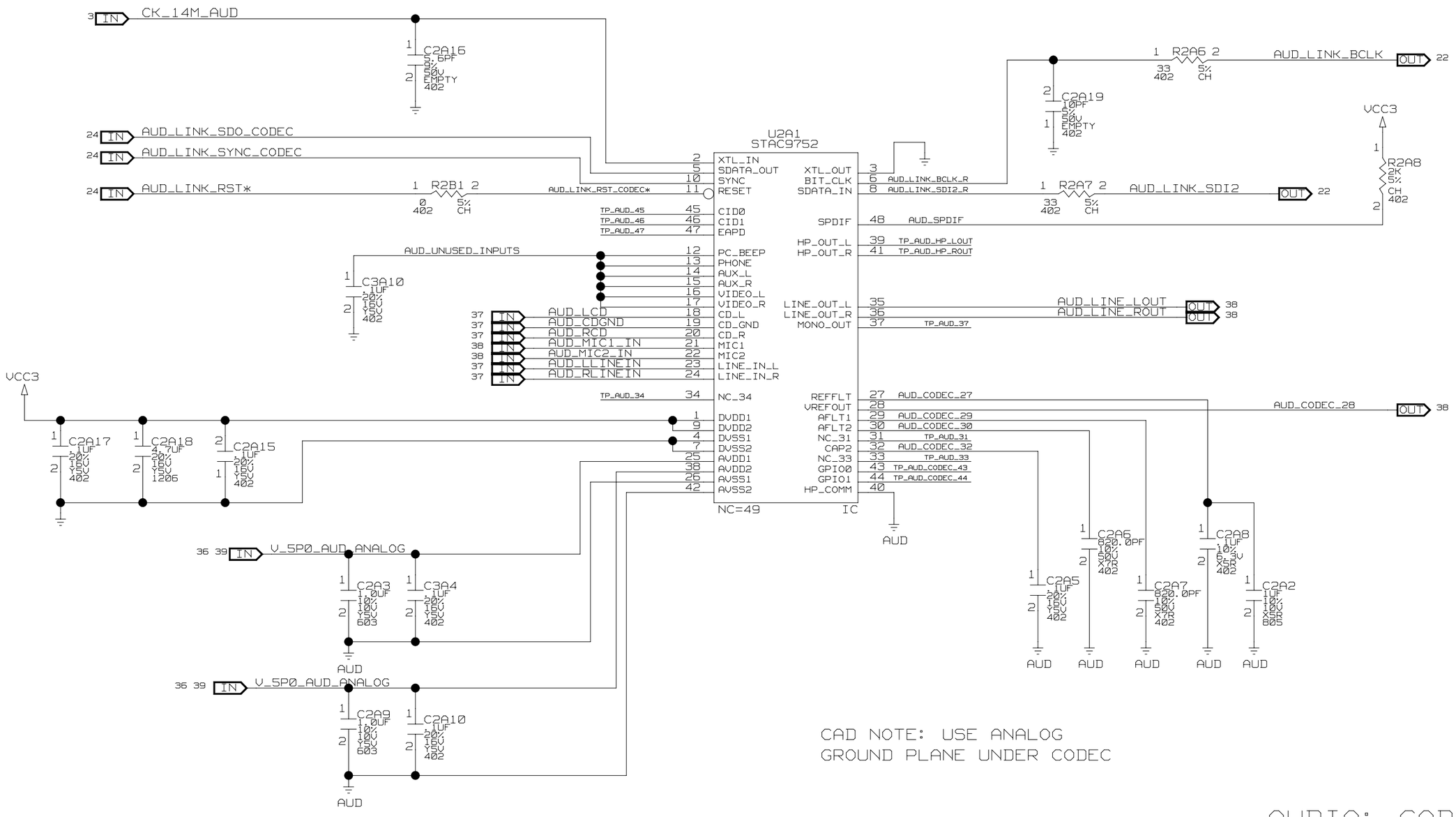


SERIAL ATA CONNECTORS.

DRAWING
855GMEFB.SCH_1.35
Mon Apr 19 13:30:57 2004

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	35	C2

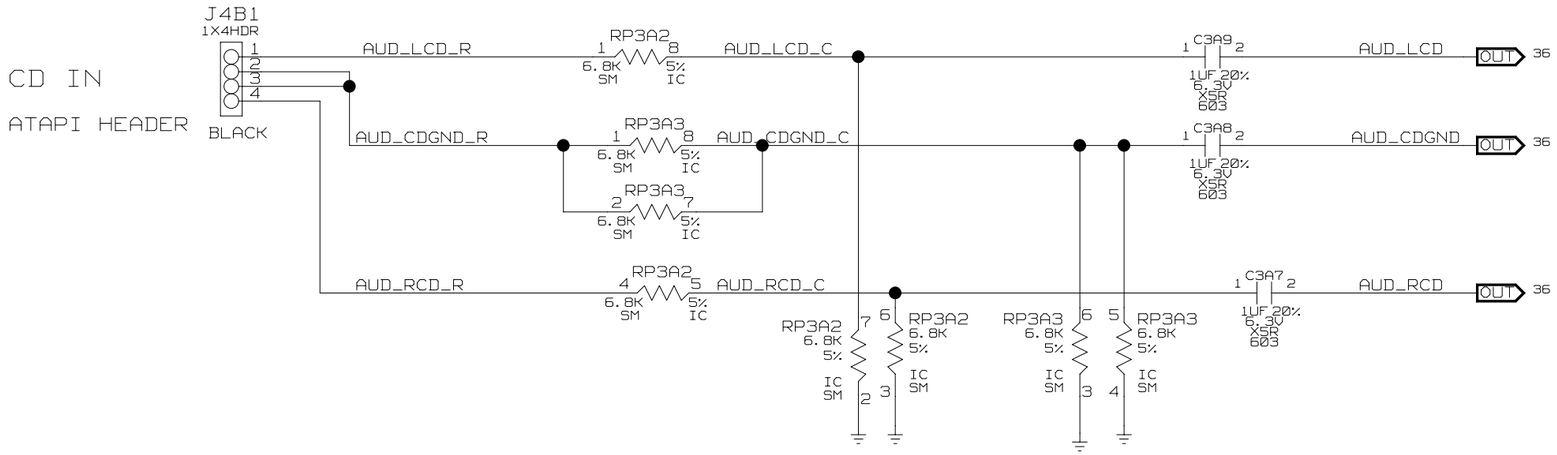


AUDIO: CODEC

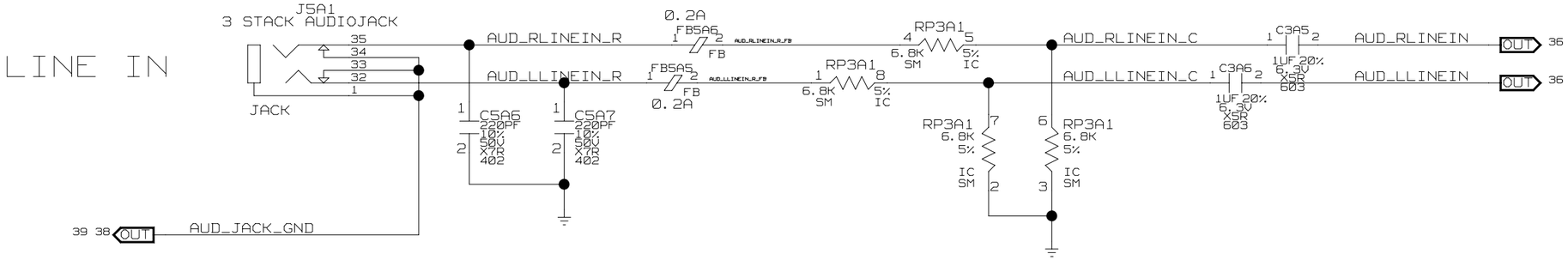
DRAWING		DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.36 Mon Apr 19 13:30:58 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	36	C2

CD IN

ATAPI HEADER

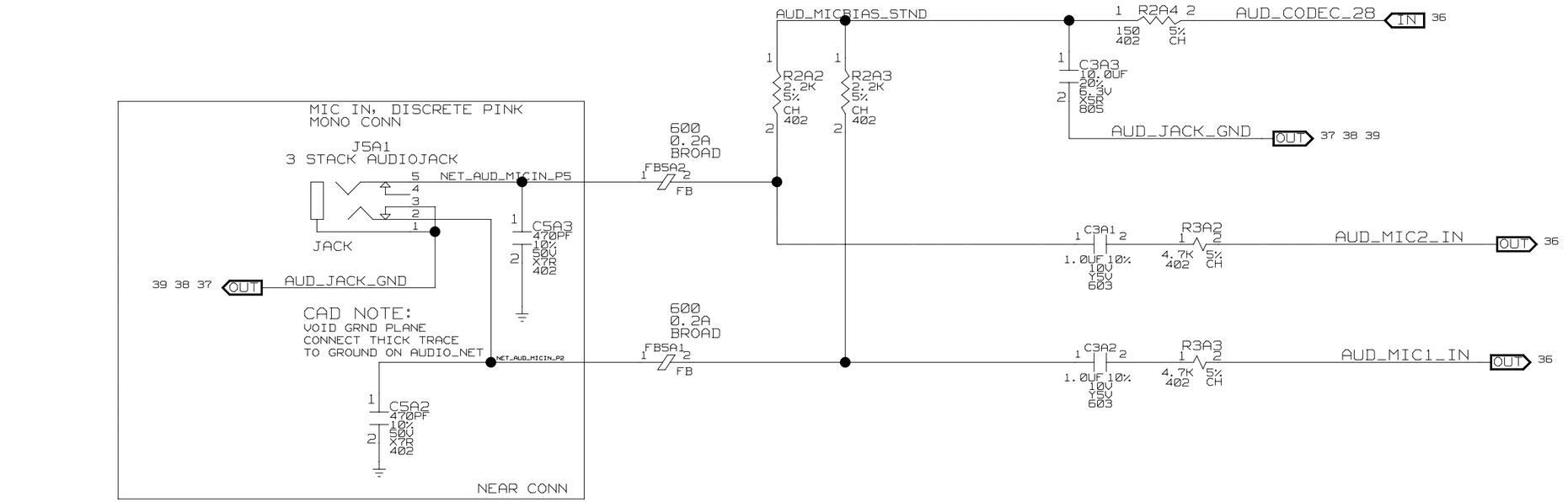


LINE IN



AUDIO: CD IN, LINE IN

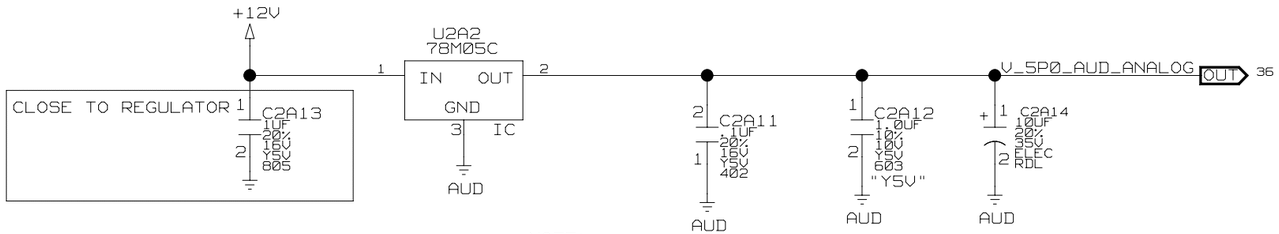
DRAWING				
855GMEFB.SCH_1.37 Mon Apr 19 13:30:58 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 37	REV C2



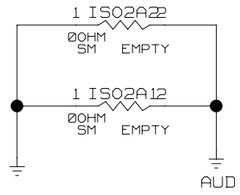
AUDIO: MIC IN, LINEOUT

DRAWING				
855GMEFB.SCH_1.38 Mon Apr 19 13:30:58 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 38	REV C2

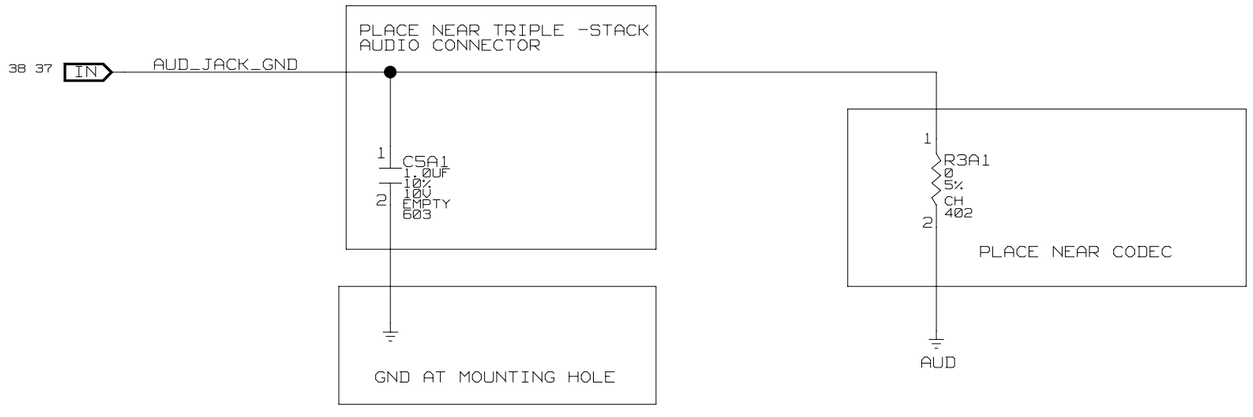
REGULATOR THERMAL TAB SHOULD BE SOLDERED
TO A COPPER PAD THAT IS LARGE ENOUGH
TO ALLOW 5 TO 10 GROUND VIAS AROUND
THE COMPONENT FOR COOLING



NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO
CAPS AND THEN THROUGH SEVERAL
VIAS TO V_5P0_AUD_ANALOG



OVERLAPPING PADS
GROUND ISOLATION SYMBOL



AUDIO: VREG

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.39 Mon Apr 19 13:30:58 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	39	C2

U8H1
LPC47M102

FLOPPY
SIO_FDD_DRVDEN0 1 DRVDEN0/GP40
SIO_FDD_DRVDEN1 2 DRVDEN1/GP41
SIO_FDD_MTR0* 3 MTR0
SIO_FDD_DS0* 5 DS0
SIO_FDD_DIR* 8 DIR
SIO_FDD_STEP* 9 STEP
SIO_FDD_WDATA* 10 WDATA
SIO_FDD_WGATE* 11 WGATE
SIO_FDD_HDSEL* 12 HDSEL
SIO_FDD_INDEX* 13 INDEX
SIO_FDD_TRK0* 14 TRK0
SIO_FDD_WRTPRT* 15 WRTPRT
SIO_FDD_RDATA* 16 RDATA
SIO_FDD_DSKCHG* 4 DSKCHG

LPC
IO_PME* 17 IOPME*/GP42
L_AD<3..0> AD0 20, AD1 21, AD2 22, AD3 23
L_FRAME_SIO* 24 FRAME
L_DRQ* 25 DRQ
SIO_PCI_RST* 26 PCI_RESET
L_PD* 27 PD
CK_P_33M_SIO 29 PCI_CLK
SER_IRQ 30 SER_IRQ

SERIAL 1
SIO_COM_RXD1 84 RXD1
SIO_COM_TXD1 85 TXD1
SIO_COM_DSR1* 86 DSR1
SIO_COM_RTS1* 87 RTS1
SIO_COM_CTS1* 88 CTS1
SIO_COM_DTR1* 89 DTR1
SIO_COM_RI1* 90 RI1
SIO_COM_DCD1* 91 DCD1

SERIAL 2 /GPIO
TP_SIO_COM_R12* 92 GP50/R12*
TP_SIO_COM_RXFD2* 94 GP51/DCD2*
TP_SIO_COM_RXD2 95 GP52/RXD2/IRRX
TP_SIO_COM_TXD2 96 GP53/TXD2/IRTX
TP_SIO_COM_DSR2* 97 GP54/DSR2*
TP_SIO_COM_RTS2* 98 GP55/RTS2*
TP_SIO_COM_CTS2* 99 GP56/CTS2*
TP_SIO_COM_DTR2* 100 GP57/DTR2*

VREF 44
VTR 18 (V_3P3_STBY)
AVSS 40

JOY
GP10/J1B1 32 TP_SIO_GAME_J1B1
GP11/J1B2 33 TP_SIO_GAME_J1B2
GP12/J2B1 34 TP_SIO_GAME_J2B1
GP13/J2B2 35 TP_SIO_GAME_J2B2
GP14/J1X 36 TP_SIO_GAME_J1X
GP15/J1Y 37 TP_SIO_GAME_J1Y
GP16/J2X 38 TP_SIO_GAME_J2X
GP17/J2Y 39 TP_SIO_39
GP25/MIDI_IN 46 TP_SIO_46
GP26/MIDI_OUT 47 TP_SIO_GP26
1

GPIO
P17/GP20 41 GP20_STRAP (IN 68)
P16/GP21 42 GP21_STRAP (IN 68)
P12/GP22 43 TP_SIO_GP22
SYSOPT/GP24 45 SIO_GP24
LED1/GP60 48 GPIO_GRN_BLNK (OUT 46)
LED2/GP61 49 GPIO_YLW_BLNK (OUT 46)
IOSMI*/GP27 50 TP_SIO_GP43
FDC_PP/DDRC/GP43 28 TP_SIO_GP43
1

KEY/MOUSE
KDAT 56 SIO_KBDATA (BI 42)
KCLK 57 SIO_KBCLOCK (BI 42)
MDAT 58 SIO_MSDATA (BI 42)
MCLK 59 SIO_MSCLOCK (BI 42)
GP36/KBDRST 63 KBRST*
GP37/A20M 64 A20GATE

PARALLEL
INIT 66 SIO_LPT_INIT* (BI 43)
SLCTIN 67 SIO_LPT_SLCTIN* (OUT 43)
PD0 68 0
PD1 69 1
PD2 70 2
PD3 71 3
PD4 72 4
PD5 73 5
PD6 74 6
PD7 75 7
SIO_LPT_PD<7..0> (BI 43)
SLCT 77 SIO_LPT_SLCT (IN 43)
PE 78 SIO_LPT_PE (IN 43)
BUSY 79 SIO_LPT_BUSY (IN 43)
ACK 80 SIO_LPT_ACK* (IN 43)
ERR 81 SIO_LPT_ERR* (IN 43)
ALF 82 SIO_LPT_ALF* (OUT 43)
STROBE 83 SIO_LPT_STROBE* (OUT 43)

IR
IRRX2/GP34 61 SIO_IRRX2 (IN 48)
IRTX2/GP35 62 SIO_IRTX2 (OUT 48)

FAN
GP32/FAN2 54 TP_SIO_FAN2_PWM
GP33/FAN1 55 FAN1_PWM
FAN_TACH2/GP30 51 FRONT_FAN_TACH (IN 50)
FAN_TACH1/GP31 52 REAR_FAN_TACH (IN 50)
R8H1 0 603 1A CH: FNT_REAR_FAN_PWM3 (OUT 50)

CLOCK
CLOCKI 19 CK_14M_SIO (IN 3)
CLKI32 6 SUSCLK (IN 21 17)

IC
VCC3=53, 65, 93
GND=7, 31, 60, 76

BIOS DETECTS ADDRESS WITHOUT STUFFING
VCC3
R9H7 4.7K 5% EMPTY 603
R8H2 4.7K 5% CH 603

VCC3
RP2V1 8.2K 5% .063W IC SM
RP2V1 8.2K 5% .063W IC SM
R2V1 8.2K 5% CH 603
R2V2 8.2K 5% CH 603
R8H4 0 603 1A CH
P_PCIRST* (IN)
SER_IRQ (BI)
L_DRQ* (OUT)
V_3P3_STBY (IN)

VCC3
RP2V1 8.2K 5% .063W IC SM
RP2V1 8.2K 5% .063W IC SM
OUT 21
OUT 21

NOTE: #1
BIOS TO PROGRAM THESE GPIO'S AS OUTPUTS

NOTE:
BIOS TO PROGRAM AS OUTPUTS
1

VCC
C8H3 1UF 20% 25VC Y5VC 603 (V_3P3_STBY)

VCC3
C8H5 1UF 20% 25VC Y5VC 603
C8H2 1UF 20% 25VC Y5VC 603
C8H4 1UF 20% 25VC Y5VC 603
C8H1 1UF 20% 25VC Y5VC 603
V_3P3_STBY (IN)
PLACE NEAR SMC DEVICE PINS 56, 65, 93, 125

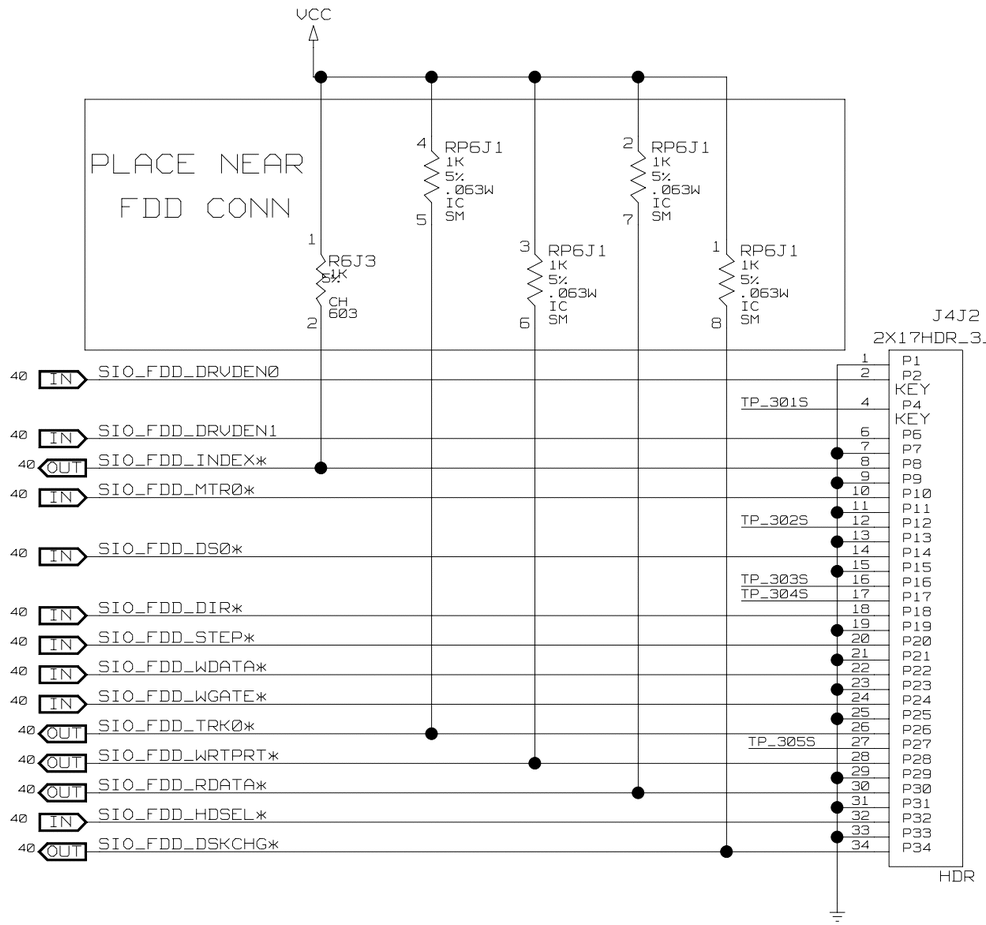
J14
1-2	NORMAL
2-3	DISABLE SIO

L_FRAME* (IN)
J8J1 1X3HDR
L_FRAME_SIO* (OUT 40)
HDR

DRAWING
855GMEFB.SCH_1.40
Mon Apr 19 13:30:59 2004

SUPER I/O

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 40	REV C2



FLOPPY CONNECTOR

DRAWING
855GMEFB.SCH.1.41
Mon Apr 19 13:30:59 2004

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
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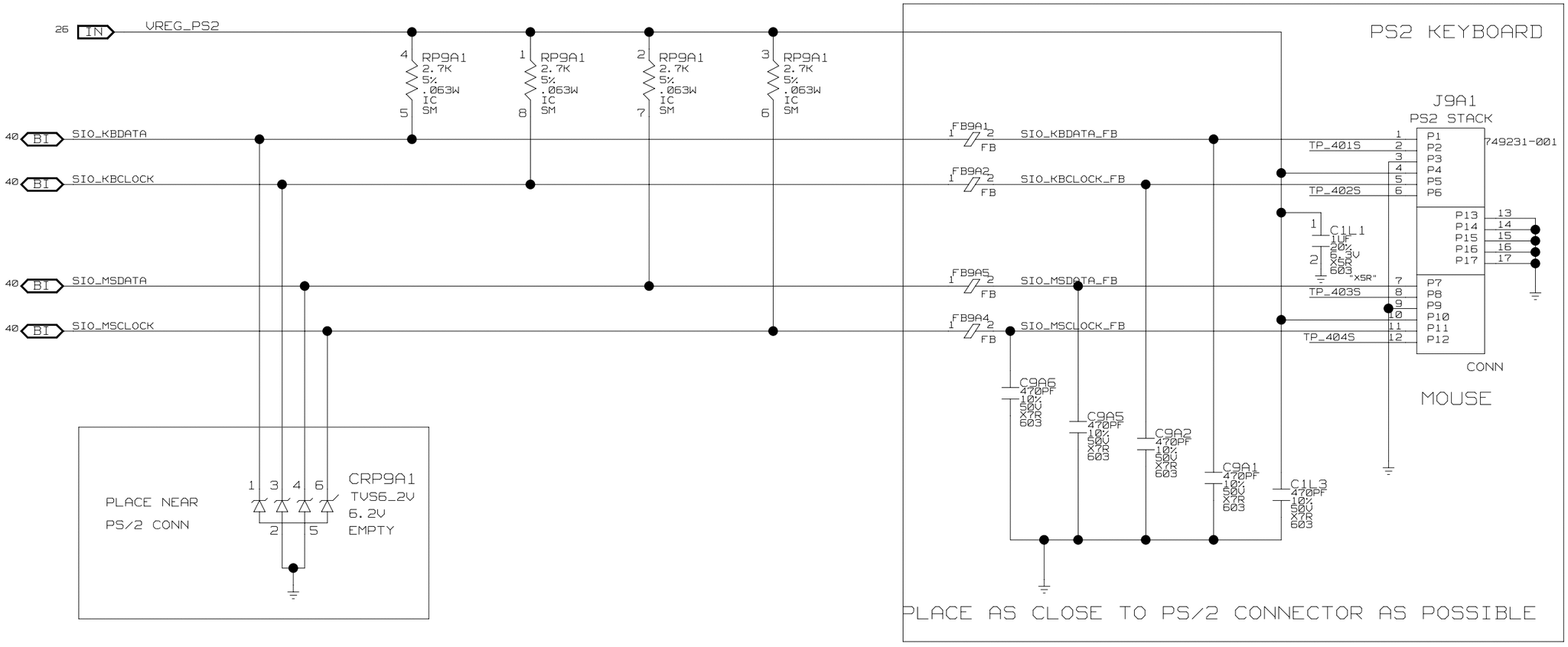
COMPONENTS ARE DFM29



ATX DOUBLE-STACKED

PS/2 STACK

DRAWING		DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.42 Mon Apr 19 13:31:00 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	42	C2

COMPONENTS ARE DFM29

40 IN SIO_LPT_PD<7..0>

RP7A3 6 SIO_LPT_PD6_R
RP7A3 5 SIO_LPT_PD7_R
RP7A2 7 SIO_LPT_PD0_R
RP7A2 8 SIO_LPT_PD1_R
RP7A2 5 SIO_LPT_PD2_R
RP7A2 6 SIO_LPT_PD3_R
RP7A3 7 SIO_LPT_PD4_R
RP7A3 8 SIO_LPT_PD5_R

33 SM, 5%.063W IC

VCC

RP7A4 2.7K 5% .063W IC SM

40 IN SIO_LPT_STROBE* — RP7A5 7 SIO_LPT_STROBE_R*
40 IN SIO_LPT_ALF* — RP7A5 8 SIO_LPT_ALF_R*
40 IN SIO_LPT_INIT* — RP7A5 5 SIO_LPT_INIT_R*
40 IN SIO_LPT_SLCTIN* — RP7A5 6 SIO_LPT_SLCTIN_R*

VCC

RP8A1 10K 5% .063W IC SM
R7A2 10K 5% CH 603

40 OUT SIO_LPT_ACK*
40 OUT SIO_LPT_BUSY
40 OUT SIO_LPT_PE
40 OUT SIO_LPT_SLCT
40 OUT SIO_LPT_ERR*

C8A3 C8A4 C8A5 C8A1 C8A2 C7A14 C7A15 C7A13 C7A8 C7A12 C7A9 C7A6 C7A11 C7A5 C7A10 C7A7
220PF 10% 50V X7R 603

J7A2
TALL DSUB 25
749179-001
DSUB
GND=26, 27, 28

PLACE NEAR
LPT CONN

PARALLEL PORT

DRAWING
855GMEFB.SCH_1.43
Mon Apr 19 13:31:00 2004

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
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DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N

SERIAL PORT A

U6B1
GD75232S

SIO_COM_DCD1* (OUT) 19 RY1 — RA1 2 → SIO_COM_DCD1_232
SIO_COM_DSR1* (OUT) 18 RY2 — RA2 3 → SIO_COM_RXD1_232*
SIO_COM_RXD1 (OUT) 17 RY3 — RA3 4 → SIO_COM_TXD1_232*
SIO_COM_CTS1* (OUT) 14 RY4 — RA4 7 → SIO_COM_DTR1_232
SIO_COM_RI1* (OUT) 12 RY5 — RA5 9 → SIO_COM_RI1_232
SIO_COM_RTS1* (IN) 16 DA1 — DY1 5 → SIO_COM_DSR1_232
SIO_COM_TXD1 (IN) 15 DA2 — DY2 6 → SIO_COM_RTS1_232
SIO_COM_DTR1* (IN) 13 DA3 — DY3 8 → SIO_COM_CTS1_232
1 VDD+ — VDD- 10

NOTE DIRECTION IC

+12V
VCC=20
GND=11
-12V
VCC=VCC

C6B4 470PF 10% 50V X7R 603
C6A10 470PF 10% 50V X7R 603
C6B3 470PF 10% 50V X7R 603
C6A8 470PF 10% 50V X7R 603
C6A7 470PF 10% 50V X7R 603
C6A9 470PF 10% 50V X7R 603
C6B2 470PF 10% 50V X7R 603
C6B1 470PF 10% 50V X7R 603

J6B1
SERIAL PORT
2X5HDR_10

SIO_COM_DCD1_232 1 P1
SIO_COM_RXD1_232* 2 P2
SIO_COM_TXD1_232* 3 P3
SIO_COM_DTR1_232 4 P4
5 P5
SIO_COM_DSR1_232 6 P6
SIO_COM_RTS1_232 7 P7
SIO_COM_CTS1_232 8 P8
SIO_COM_RI1_232 9 P9
KEY

HDR

SERIAL PORT B

U8A2
GD75232S

ICH_COM_DCD0* (OUT) 19 RY1 — RA1 2 → ICH_COM_DCD0_232
ICH_COM_DSR0* (OUT) 18 RY2 — RA2 3 → ICH_COM_DSR0_232
ICH_COM_RXD0 (OUT) 17 RY3 — RA3 4 → ICH_COM_RXD0_232*
ICH_COM_CTS0* (OUT) 14 RY4 — RA4 7 → ICH_COM_RTS0_232
ICH_COM_RI0* (OUT) 12 RY5 — RA5 9 → ICH_COM_TXD0_232*
ICH_COM_RTS0* (IN) 16 DA1 — DY1 5 → ICH_COM_CTS0_232
ICH_COM_TXD0 (IN) 15 DA2 — DY2 6 → ICH_COM_DTR0_232
ICH_COM_DTR0* (IN) 13 DA3 — DY3 8 → ICH_COM_RI0_232
1 VDD+ — VDD- 10

NOTE DIRECTION IC

+12V
VCC=20
GND=11
-12V

C2L1 470PF 10% 50V X7R 603
C2L2 470PF 10% 50V X7R 603
C2L3 470PF 10% 50V X7R 603
C2L6 470PF 10% 50V X7R 603
C3L1 470PF 10% 50V X7R 603
C2L4 470PF 10% 50V X7R 603
C2L5 470PF 10% 50V X7R 603
C2L7 470PF 10% 50V X7R 603

J8A1
2 ROW
DSUB
10
11

ICH_COM_DCD0_232 1
ICH_COM_DSR0_232 6
ICH_COM_RXD0_232* 2
ICH_COM_RTS0_232 7
ICH_COM_TXD0_232* 3
ICH_COM_CTS0_232 8
ICH_COM_DTR0_232 4
ICH_COM_RI0_232 9
5

U6A1
GD75232S

ICH_COM_DCD1* (OUT) 19 RY1 — RA1 2 → ICH_COM_DCD1_232
ICH_COM_DSR1* (OUT) 18 RY2 — RA2 3 → ICH_COM_DSR1_232
ICH_COM_RXD1 (OUT) 17 RY3 — RA3 4 → ICH_COM_RXD1_232*
ICH_COM_CTS1* (OUT) 14 RY4 — RA4 7 → ICH_COM_RTS1_232
ICH_COM_RI1* (OUT) 12 RY5 — RA5 9 → ICH_COM_TXD1_232*
ICH_COM_RTS1* (IN) 16 DA1 — DY1 5 → ICH_COM_CTS1_232
ICH_COM_TXD1 (IN) 15 DA2 — DY2 6 → ICH_COM_DTR1_232
ICH_COM_DTR1* (IN) 13 DA3 — DY3 8 → ICH_COM_RI1_232
1 VDD+ — VDD- 10

NOTE DIRECTION IC

+12V
VCC=20
GND=11
-12V

C4L1 470PF 10% 50V X7R 603
C4L2 470PF 10% 50V X7R 603
C4L3 470PF 10% 50V X7R 603
C4L6 470PF 10% 50V X7R 603
C4L8 470PF 10% 50V X7R 603
C4L4 470PF 10% 50V X7R 603
C4L5 470PF 10% 50V X7R 603
C4L7 470PF 10% 50V X7R 603

J6A1
2 ROW
DSUB
10
11

ICH_COM_DCD1_232 1
ICH_COM_DSR1_232 6
ICH_COM_RXD1_232* 2
ICH_COM_RTS1_232 7
ICH_COM_TXD1_232* 3
ICH_COM_CTS1_232 8
ICH_COM_DTR1_232 4
ICH_COM_RI1_232 9
5

+12V
C4M1 1UF 20% 25V X5R 603
C6A2 1UF 20% 25V X5R 603
C2M2 1UF 20% 25V X5R 603

-12V
C4L9 1UF 20% 25V X5R 603
C6A1 1UF 20% 25V X5R 603
C2M1 1UF 20% 25V X5R 603

V_5P0_STBY (IN) 53 26 27 46 48 51 54 55 56
C4M2 1UF 20% 25V X5R 603

VCC
C6A5 1UF 20% 25V X5R 603
C2M3 1UF 20% 25V X5R 603

PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY

SERIAL PORTS

DRAWING
855GMEFB.SCH_1.44
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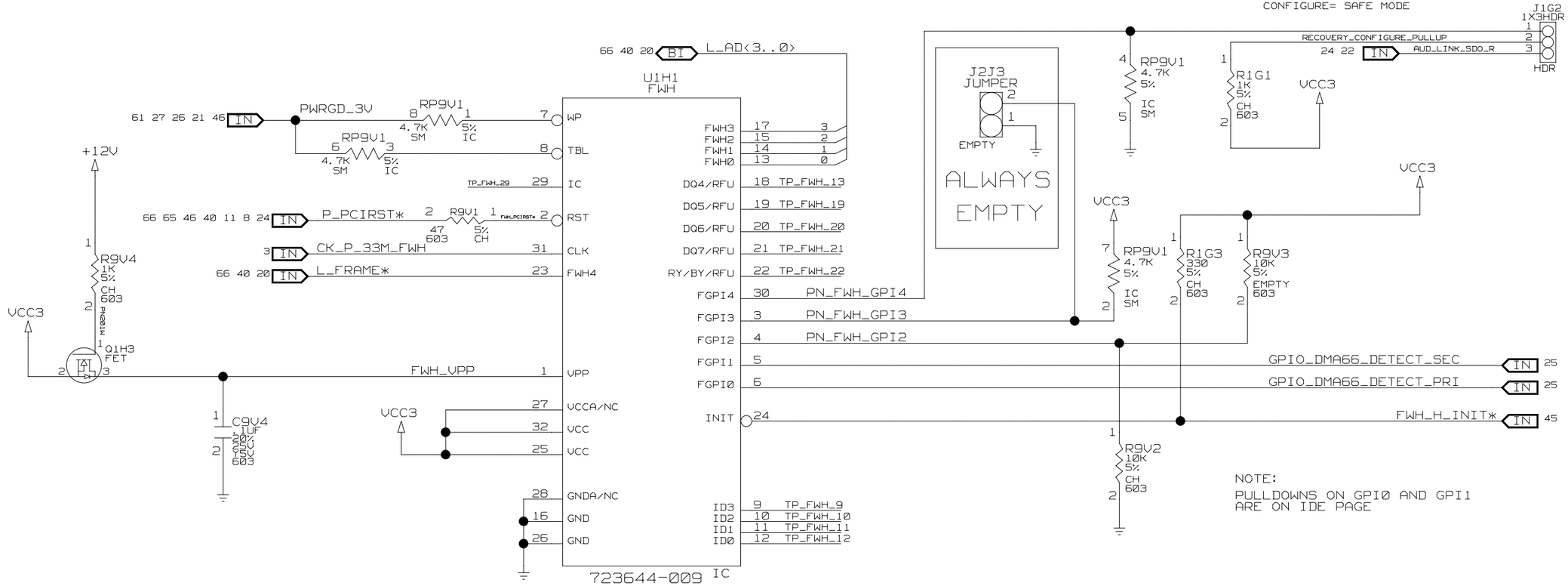
RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

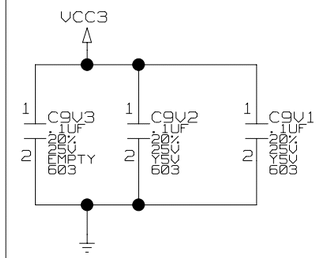


NOTE:
PULLDOWNS ON GPI0 AND GPI1 ARE ON IDE PAGE

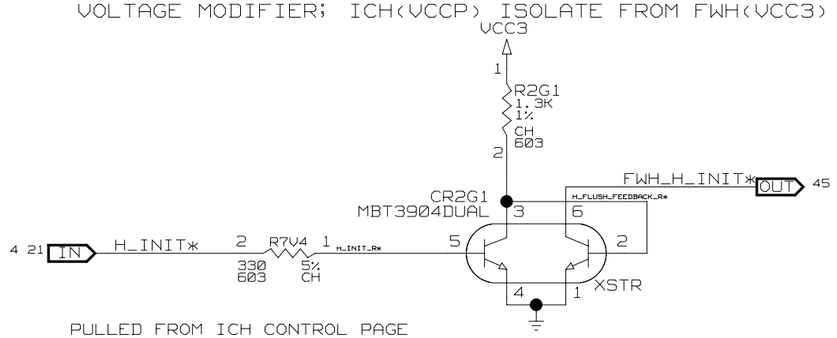
FWH SOCKET - INTEL P/N: 201138-032, AMP P/N: 822475-1

PLCC EXTRACTION TOOL
AMP: 821980-1 OR
AMP: 822476-1

FIRMWARE HUB DECOUPLING



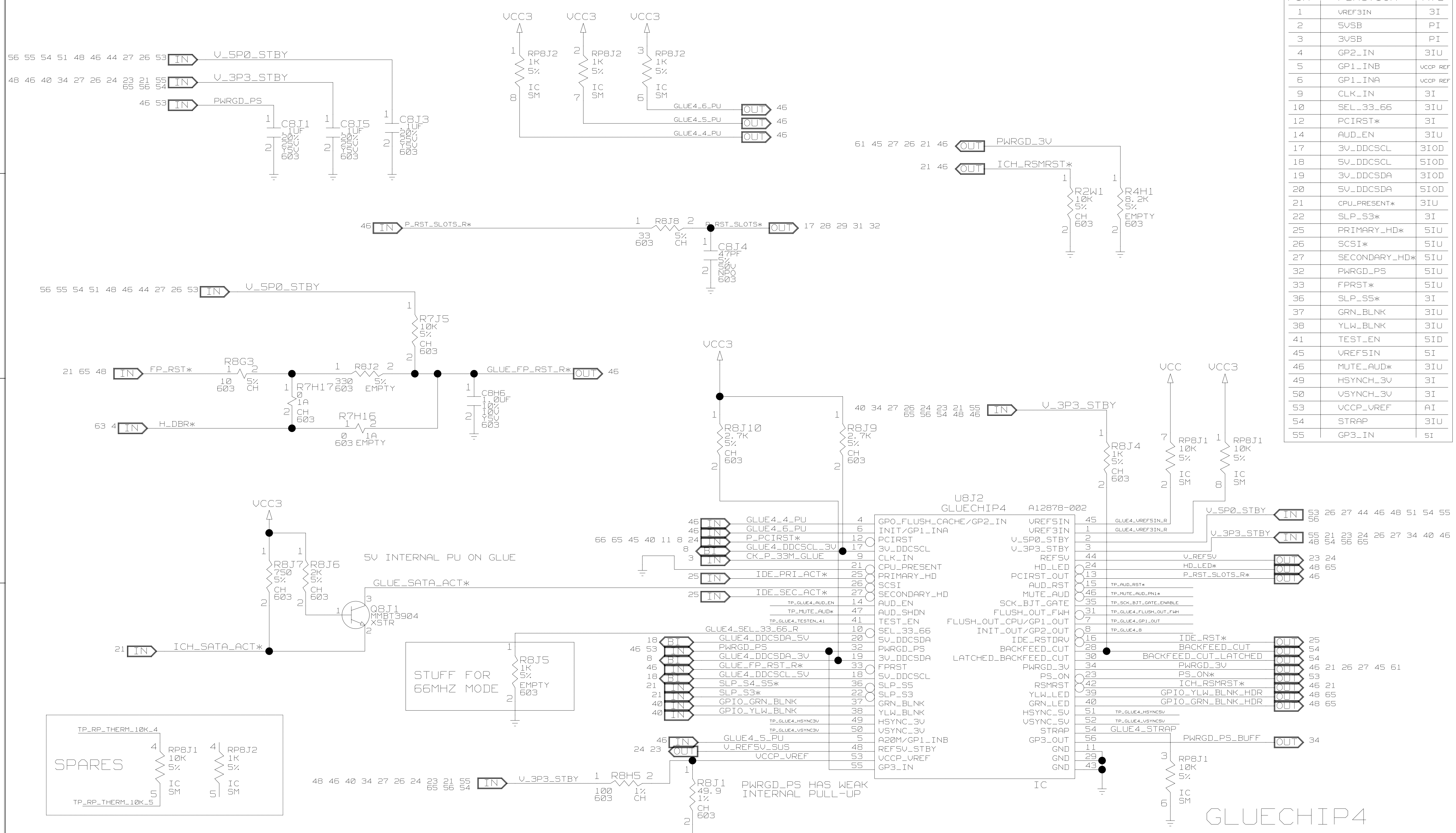
VOLTAGE MODIFIER; ICH(VCCP) ISOLATE FROM FWH(VCC3)



PULLED FROM ICH CONTROL PAGE

FIRMWARE HUB

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.45 Mon Apr 19 13:31:01 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	45	C2



GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	VCCP REF
6	GP1_INA	VCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	5IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	5IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HD*	5IU
26	SCSI*	5IU
27	SECONDARY_HD*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	VCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I

DRAWING
855GMEFB.SCH_1.46
Mon Apr 19 13:31:01 2004

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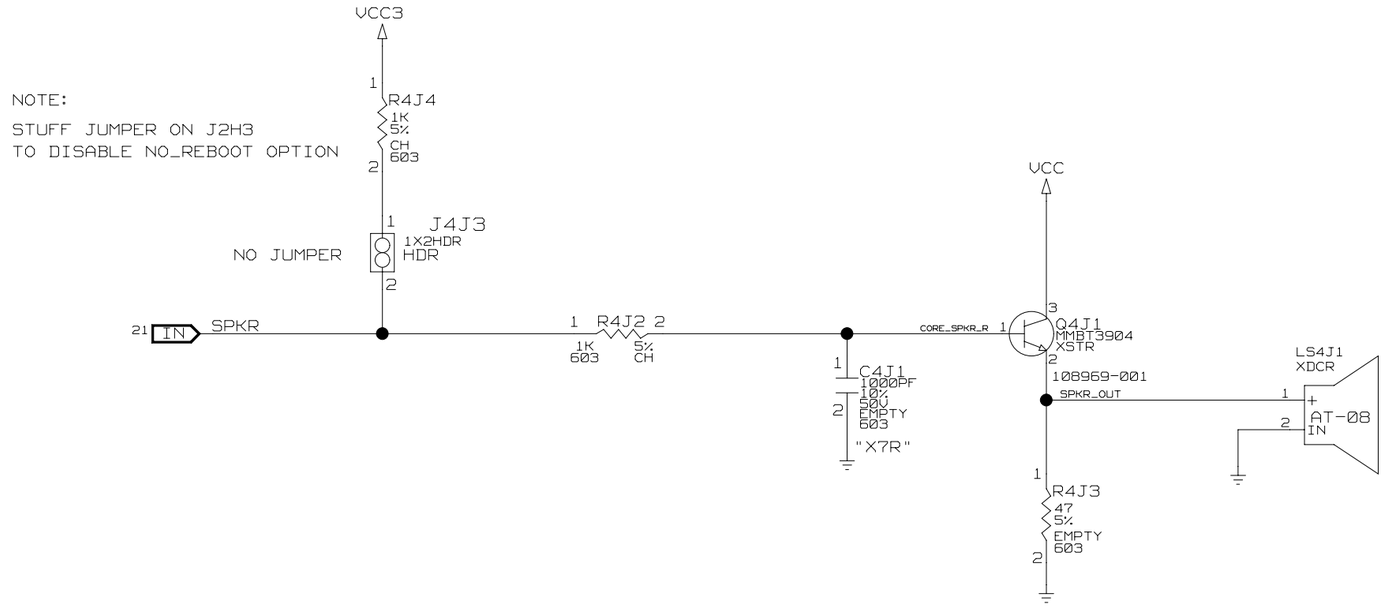
	30117601	46	C2

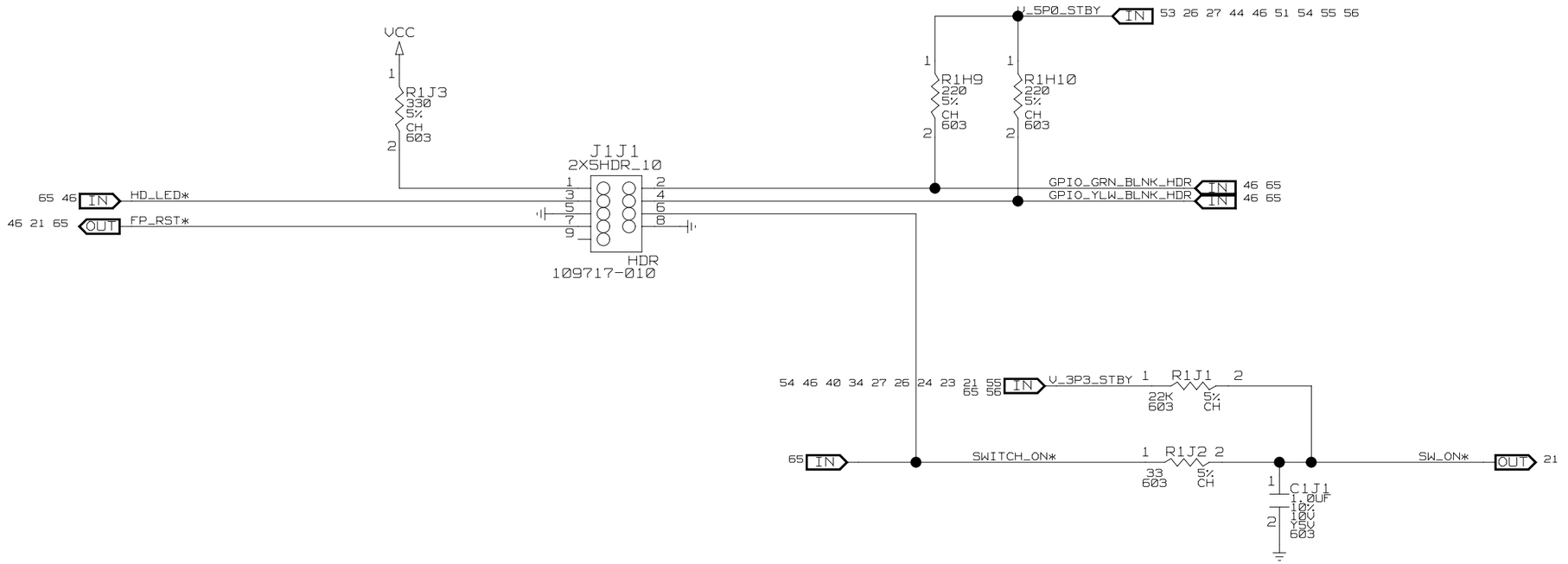
NOTE:

STUFF JUMPER ON J2H3
TO DISABLE NO_REBOOT OPTION



SPEAKER

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.47 Mon Apr 19 13:31:01 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	47	C2



FRONT PANEL HEADER
IR HEADER

DRAWING				
855GMEFB.SCH_1.48 Mon Apr 19 13:31:01 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 48	REV C2

MTG1A1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG5A1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG9B1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG1J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG9G1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG5J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

MTG9J1 DEBUG
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

CONNECTOR LOCATION

	X	Y
PS/2	8525	6210
USB/LAN	7965	5927
COM	6940	6115
PAR	5362	5843
VGA	5136	6190
DIAGLED	4636	6045
USB	4151	6026
AUD	3291	6218

LABELS

DEBUG
U3B1
SILK
1
INTELtm
'INTEL' LOGO SILKSCREEN
2.0 X 0.250
MAKE EMPTY ON BOM

LB9J1
LABEL
A19177-001
1375X250_TARGET

MOUNTING HOLES & LABELS

DRAWING
855GMEFB.SCH_1.49
Mon Apr 19 13:31:02 2004

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER 30117601
PAGE 49
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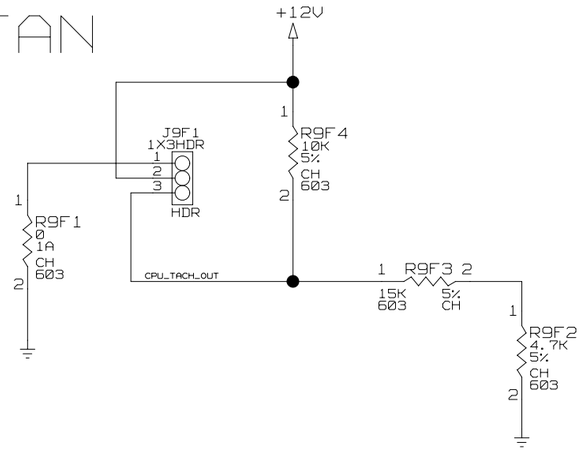
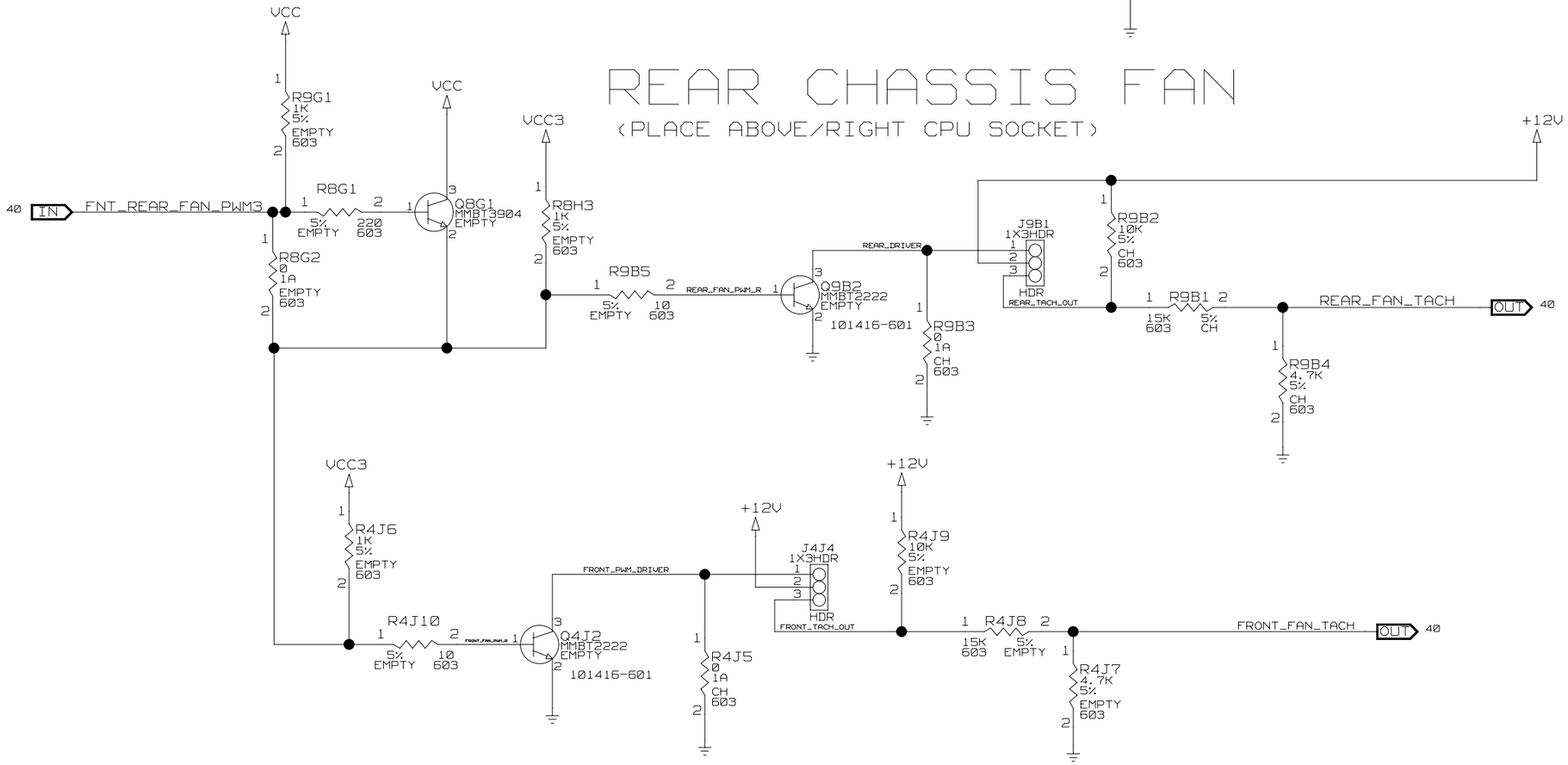
CPU ALWAYS-ON FAN

(PLACE BELOW/RIGHT CPU SOCKET)



REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)



CPU & CHASSIS FANS

ROOM=DCL_DDR_VR

STUFFING OPTIONS DEPENDING ON CONTROLLER

LOCATION	NCP1570	TPPM0115
C5J1	STUFF 0.01UF	EMPTY
C5H5	STUFF 0.1UF	EMPTY
R5H3	EMPTY	STUFF 0-OHM

+12V
R6J6 2.2 5% CH 805
C6J6 1UF 20% 16V X5R 805
VREG_TPPM0115_VCC_PU
U6J1 TPPM0115 IC
VCC DRVH PWRGD PHASE TEST DRVL SEN GND
TP_PWRGD_V2P5
TEST_PIN3
VREG_FETGATE_MEM_PN2
VREG_2P5_PN1
VREG_2P5_MEM_PN1
C6J5 1UF 10% 16V EMPTY 603
C5J1 .01UF 10% 50V EMPTY 603
VCC
L6J1 1.7UH IND
V_5P0_FILTER_2P5SM
C6H4 4.7UF 20% 10V Y5V 1206
C7H8 4.7UF 20% 10V Y5V 1206
C6H3 .1UF 10% 16V X7R 603
C7H4 2200UF 20% 16.0V ALUMINUM RDL
C6H1 2200UF 20% 16.0V ALUMINUM RDL
PHD55N03LT Q6H1 740985-001 FET
R6H1 0 805 1A CH
R6H3 0 603 1A CH
PHD55N03LT Q6H2 740985-001 FET
R6H4 0 805 1A CH
L6H1 4UH IND
R6H2 2.2 5% CH 805
C6H2 4700PF 20% 50V X7R 603
C5H1 1500UF 20% 6.3V ALUM RDL
C5G20 4.7UF 10% 10V X5R 1206
V_2P5_CORE OUT 9 13 68
68 IN VMARG_2P5_MEM
R6J2 1.5K 1% 603 CH
R6J5 1.5K 1% 603 EMPTY
R6J4 1K 1% CH 603
54 IN VREG_USB_NCH_L
54 IN VREG_USB_PCH_L
U5H1 FET
Q5G1 MOSFET
V_2P5_SM OUT 9 10 13 52 57
C5H2 1500UF 20% 6.3V ALUM RDL
C5G19 4.7UF 10% 10V X5R 1206
C5H3 1UF 10% 10V X5R 603

2.5VSTBY REGULATOR

ADJ Q4G1 MC33269
46 44 27 26 53 56 55 54 48 IN V_5P0_STBY
IN OUT ADJ SM
V_2P5_SM_SRC
C4H2 1UF 20% 25V Y5V 603
C5J2 330UF 20% 2.5V POLYMER RDL
C4H1 1UF 20% 25V Y5V 603
R4G2 453 1% CH 603
R4G1 453 603 1% CH
C4G5 .1UF 20% 25V Y5V 603
C5G21 100UF 20% 6.3V X5R 1812

2.5V DDR REGULATOR

DRAWING
855GMEFB.SCH_1.51
Mon Apr 19 13:31:02 2004

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	51	C2

ROOM=DCL_DDR_VR

57 13 10 9 51 IN

V_2P5_SM

+12V

R7H7 10 5% CH 603

C7H5 1UF 10% 10V X7R 603

INV_A_PIN8

U7H1 LM358 IC

INV_A_OUT

INV_A_PIN4

R7H3 10 5% CH 603

+12V

C7H2 1UF 10% 10V X7R 603

BAT54C SOT23C DIO

Q7H1

U7G1 FET MTD3302

R7G1 1K 5% 603 CH

R7H1 49.9 1% CH 603

INV_A_UTT

R7H4 0 603 1A CH

R7H2 49.9 1% CH 603

C7H3 1.0UF 10% 10V Y5V 603

R7H6 0 1A EMPTY 603

U7H1 LM358 IC

R7H5 0 603 1A EMPTY

DIMM_VREF_1P25

OUT 13 68 7

V_1P25_MEMUTT

OUT 14 15 16

U7G2 MOSFET A61801-001

C7G17 470UF 20% 10V ALUM RDL

C8G2 470UF 20% 10V ALUM RDL

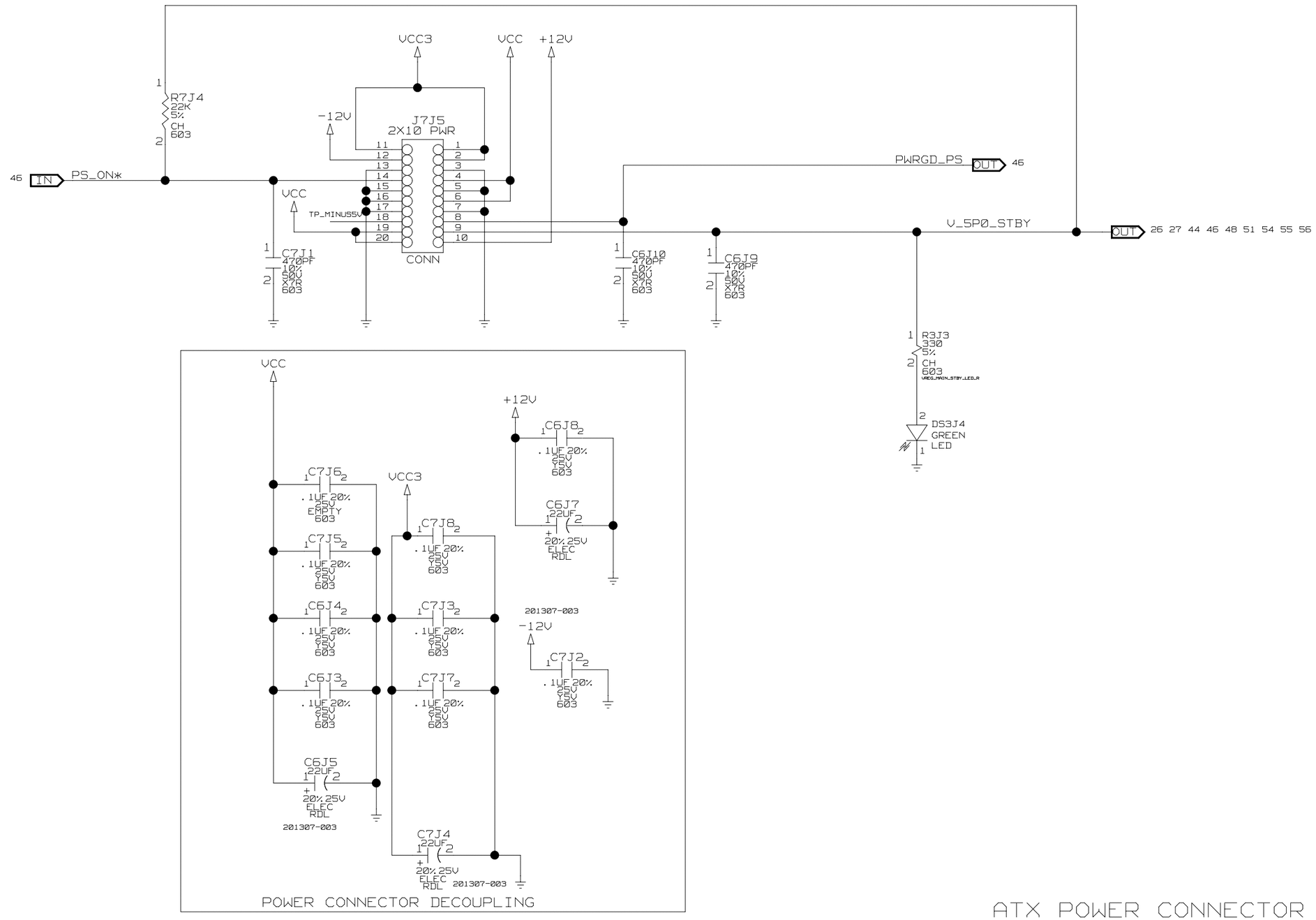
C7G11 .1UF 10% 16V X7R 603

C8G12 470UF 20% 10V ALUM RDL

C7G16 470UF 20% 10V ALUM RDL

1.25V DDR REGULATOR

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.52 Mon Apr 19 13:31:03 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	52	C2

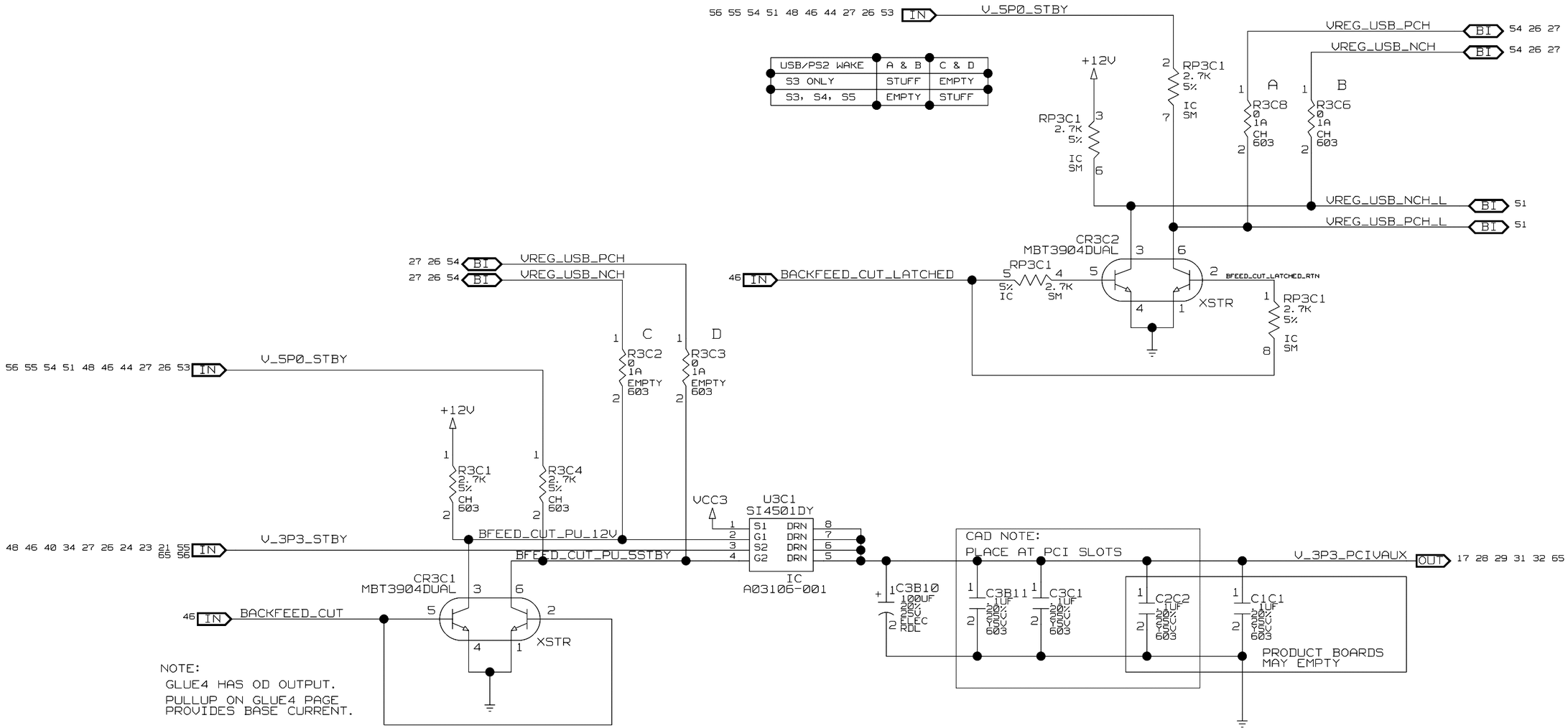


POWER CONNECTOR DECOUPLING

ATX POWER CONNECTOR

DRAWING
855GMEFB.SCH_1.53
Mon Apr 19 13:31:03 2004

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	53	C2

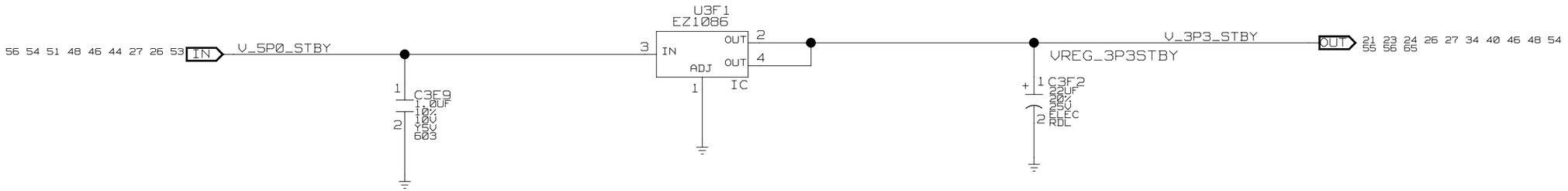


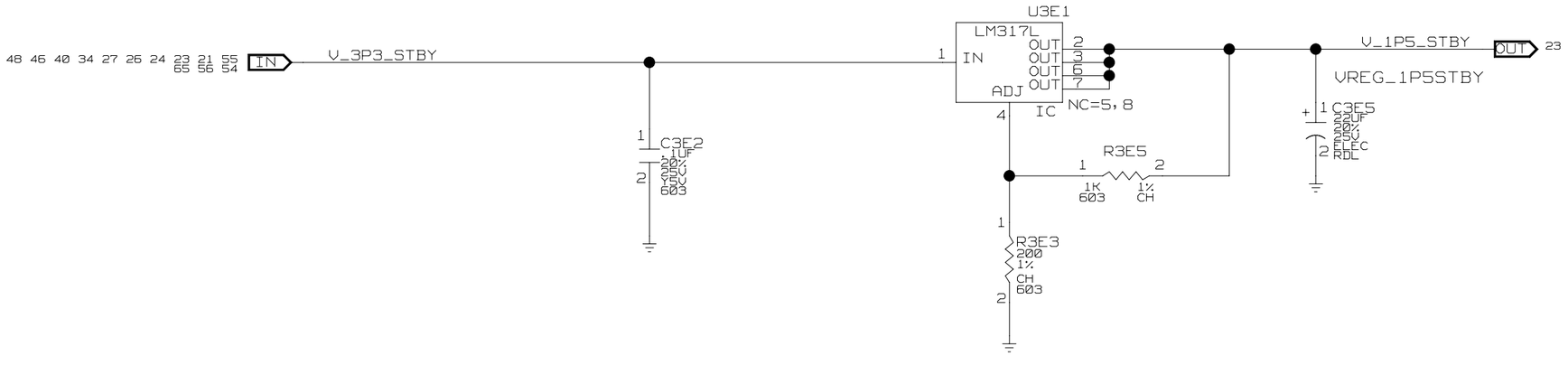
PCI VAUX

DRAWING
855GMEFB.SCH_1.54
Mon Apr 19 13:31:03 2004

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

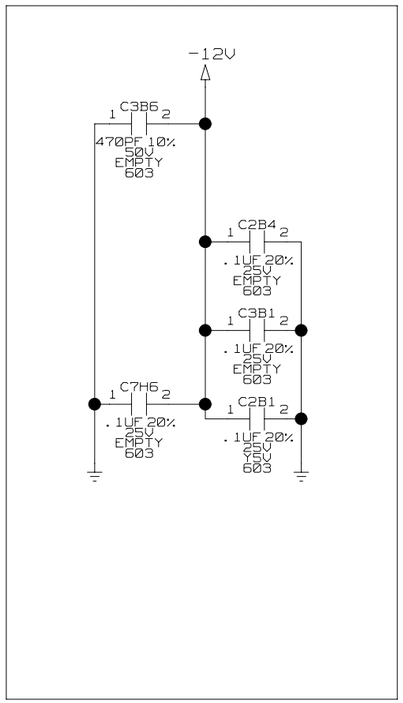
DOCUMENT NUMBER	PAGE	REV
30117601	54	C2

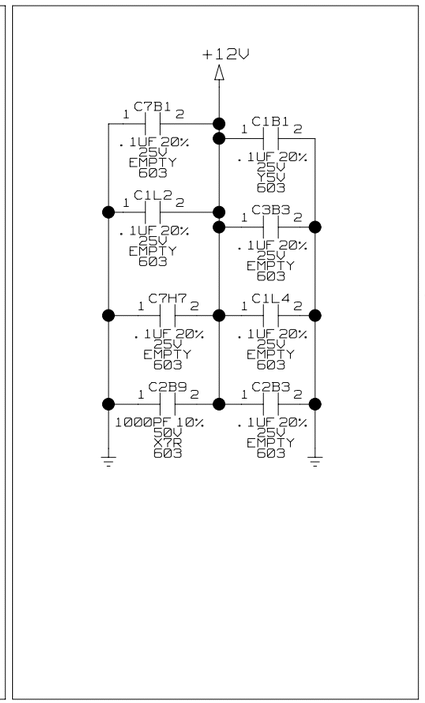


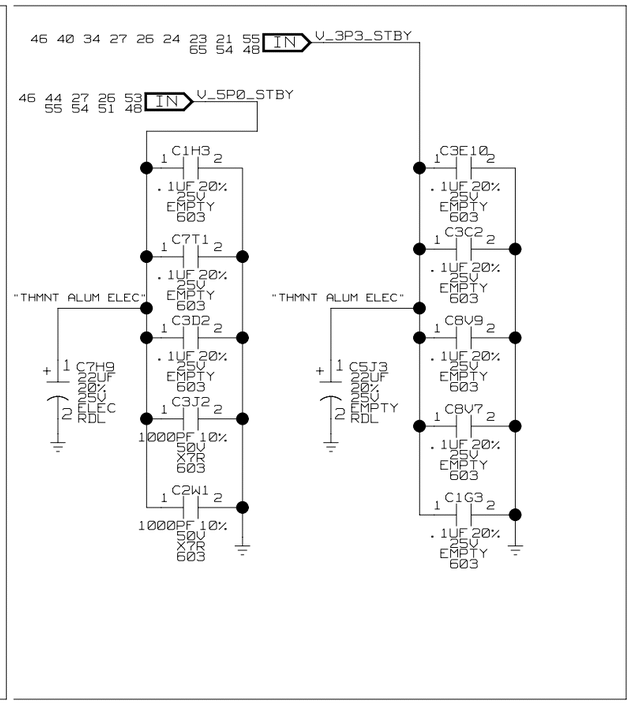


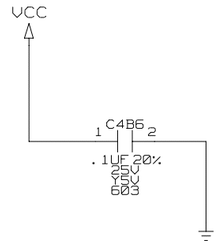
3.3V/1.5V STANDBY

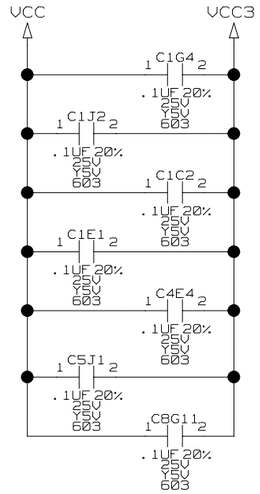
DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.55 Mon Apr 19 13:31:03 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	55	C2

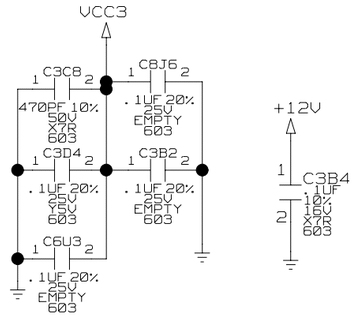


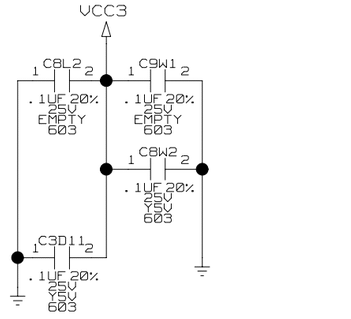


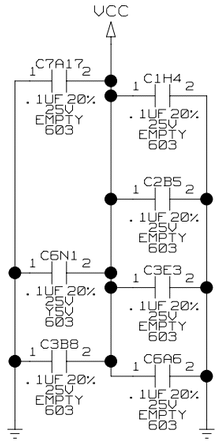


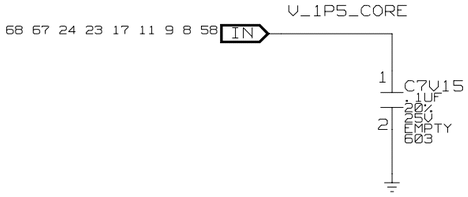


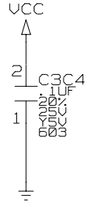


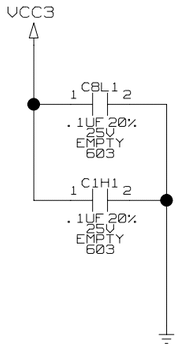


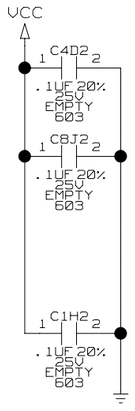


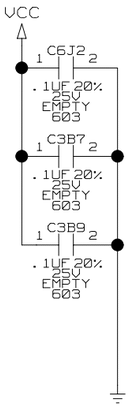


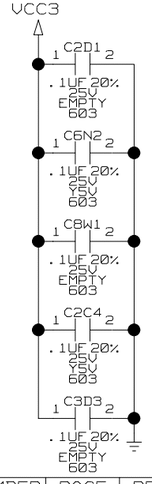








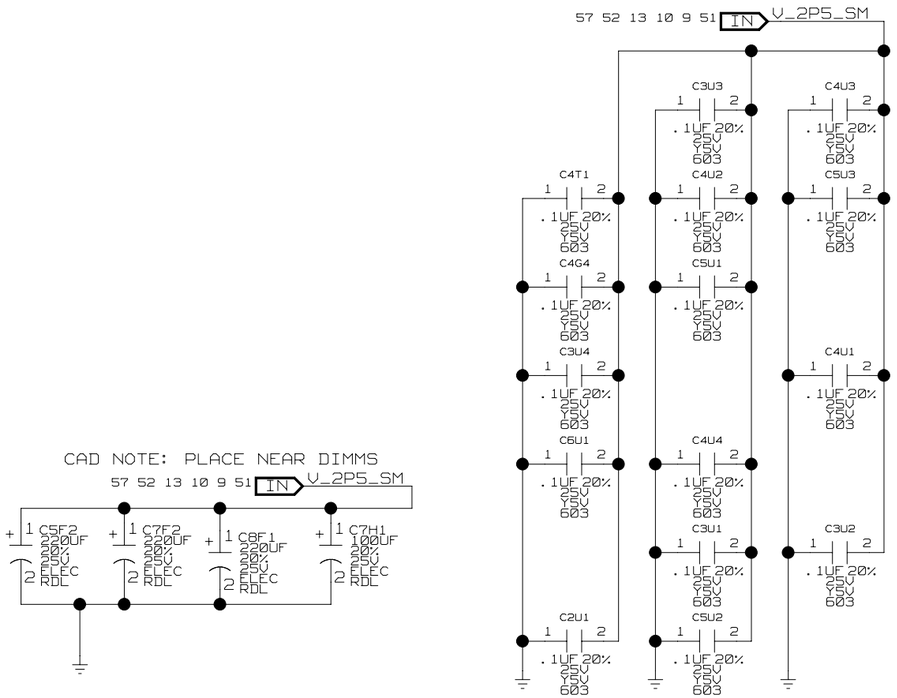




BULK DECOUPLING

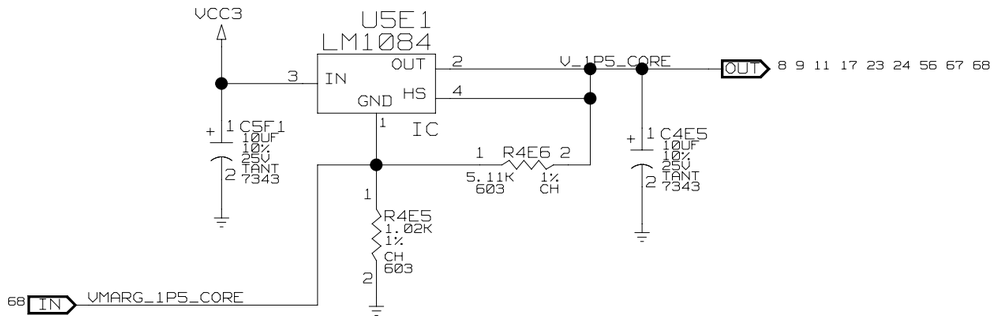
DRAWING
855GMEFB.SCH_1.56
Mon Apr 19 13:31:04 2004

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	56	C2

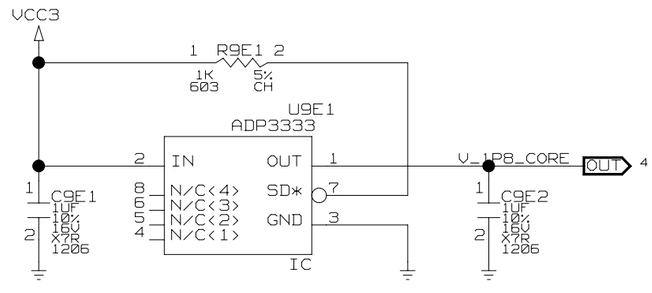


DDR 2P5_SM DECOUPLING

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH_1.57 Mon Apr 19 13:31:04 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	57	C2



CPU PLL POWER SUPPLY



1.5V & 1.8V REGULATOR

DRAWING				
855GMEFB.SCH.1.58 Mon Apr 19 13:31:04 2004	INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 30117601	PAGE 58	REV C2

VCC3 VCC +12V

60 IN VDC_PHASE1

67 60 IN H_VID<5..0> 5 4 3 2 1 0

60 IN VDC_PHASE2

GMCH_VR_PWRGD IN 61

CPU_VR_PWRGD OUT 3 8

CPU_VR_DPWRGD OUT 24 21

CPU_CORE OUT 5 60

CPU_CORE OUT 5 60

1 R8B1 2
0 1A
805 CH

CPU CORE REGULATOR

DRAWING
855GMEFB.SCH_1.59
Mon Apr 19 13:35:42 2004

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	59	C2

ROOM = DCL_CORE_CPU_VREG

MID FREQUENCY CPU DECOUPLING

5 59 IN CPU_CORE

C2P4 10.0UF 20% 6.3V X5R 0805
C2P3 10.0UF 20% 6.3V X5R 0805
C2P2 10.0UF 20% 6.3V X5R 0805
C2P1 10.0UF 20% 6.3V X5R 0805
C1P5 10.0UF 20% 6.3V X5R 0805
C1P4 10.0UF 20% 6.3V X5R 0805
C1P3 10.0UF 20% 6.3V X5R 0805
C1P2 10.0UF 20% 6.3V X5R 0805
C2N1 10.0UF 20% 6.3V X5R 0805
C1P6 10.0UF 20% 6.3V X5R 0805
C2P17 10.0UF 20% 6.3V X5R 0805
C2P16 10.0UF 20% 6.3V X5R 0805
C2P15 10.0UF 20% 6.3V X5R 0805
C2P14 10.0UF 20% 6.3V X5R 0805
C2P13 10.0UF 20% 6.3V X5R 0805

C1P15 10.0UF 20% 6.3V X5R 0805
C1P14 10.0UF 20% 6.3V X5R 0805
C1P13 10.0UF 20% 6.3V X5R 0805
C2N10 10.0UF 20% 6.3V X5R 0805
C2P12 10.0UF 20% 6.3V X5R 0805
C2P6 10.0UF 20% 6.3V X5R 0805
C1P12 10.0UF 20% 6.3V X5R 0805
C2P9 10.0UF 20% 6.3V X5R 0805
C1P9 10.0UF 20% 6.3V X5R 0805
C2N11 10.0UF 20% 6.3V X5R 0805
C1N1 10.0UF 20% 6.3V X5R 0805
C2N8 10.0UF 20% 6.3V X5R 0805
C2N7 10.0UF 20% 6.3V X5R 0805
C2N5 10.0UF 20% 6.3V X5R 0805
C2N4 10.0UF 20% 6.3V X5R 0805
C2N5 10.0UF 20% 6.3V X5R 0805
C2N3 10.0UF 20% 6.3V X5R 0805
C2N2 10.0UF 20% 6.3V X5R 0805
C1N2 10.0UF 20% 6.3V X5R 0805
C2N9 10.0UF 20% 6.3V X5R 0805

BULK CPU DECOUPLING

C8C2 220UF 20% 2.5V TANT 7343
C7C4 220UF 20% 2.5V TANT 7343
C8C1 220UF 20% 2.5V TANT 7343
C9C3 220UF 20% 2.5V TANT 7343

VCCP

VCCP CPU DECOUPLING

C2P5 1UF 5% 16V X7R 603
C2P8 1UF 5% 16V X7R 603
C2P7 1UF 5% 16V X7R 603
C2P11 1UF 5% 16V X7R 603
C2P10 1UF 5% 16V X7R 603
C1P10 1UF 5% 16V X7R 603
C1P7 1UF 5% 16V X7R 603
C1P1 1UF 5% 16V X7R 603
C1P8 1UF 5% 16V X7R 603
C1P11 1UF 5% 16V X7R 603
C8D1 150UF 20% 4V POSCAP 7343
C8D2 150UF 20% 4V EMPTY 7343

PLACE ON BOTTOM OF CPU UNDER BANIAS SOCKET CAVITY

VCCP

59 67 OUT H_VID<0> R8E6 1K 603 5% CH
59 67 OUT H_VID<1> R8E5 1K 603 5% CH
59 67 OUT H_VID<2> R8E4 1K 603 5% CH
59 67 OUT H_VID<3> R8E3 1K 603 5% CH
59 67 OUT H_VID<4> R8E2 1K 603 5% CH
59 67 OUT H_VID<5> R8E1 1K 603 5% CH

CPU VR FET DRAIN VOLTAGE

+12V
R9B6 0.002 2512 5%
VDC_PHASE1 OUT 59
C9B3 10UF 20% 25V X5R 1210
C9B4 10UF 20% 25V X5R 1210
C9C1 10UF 20% 25V X5R 1210
C9B5 10UF 20% 25V X5R 1210
C9C2 10UF 20% 25V X5R 1210

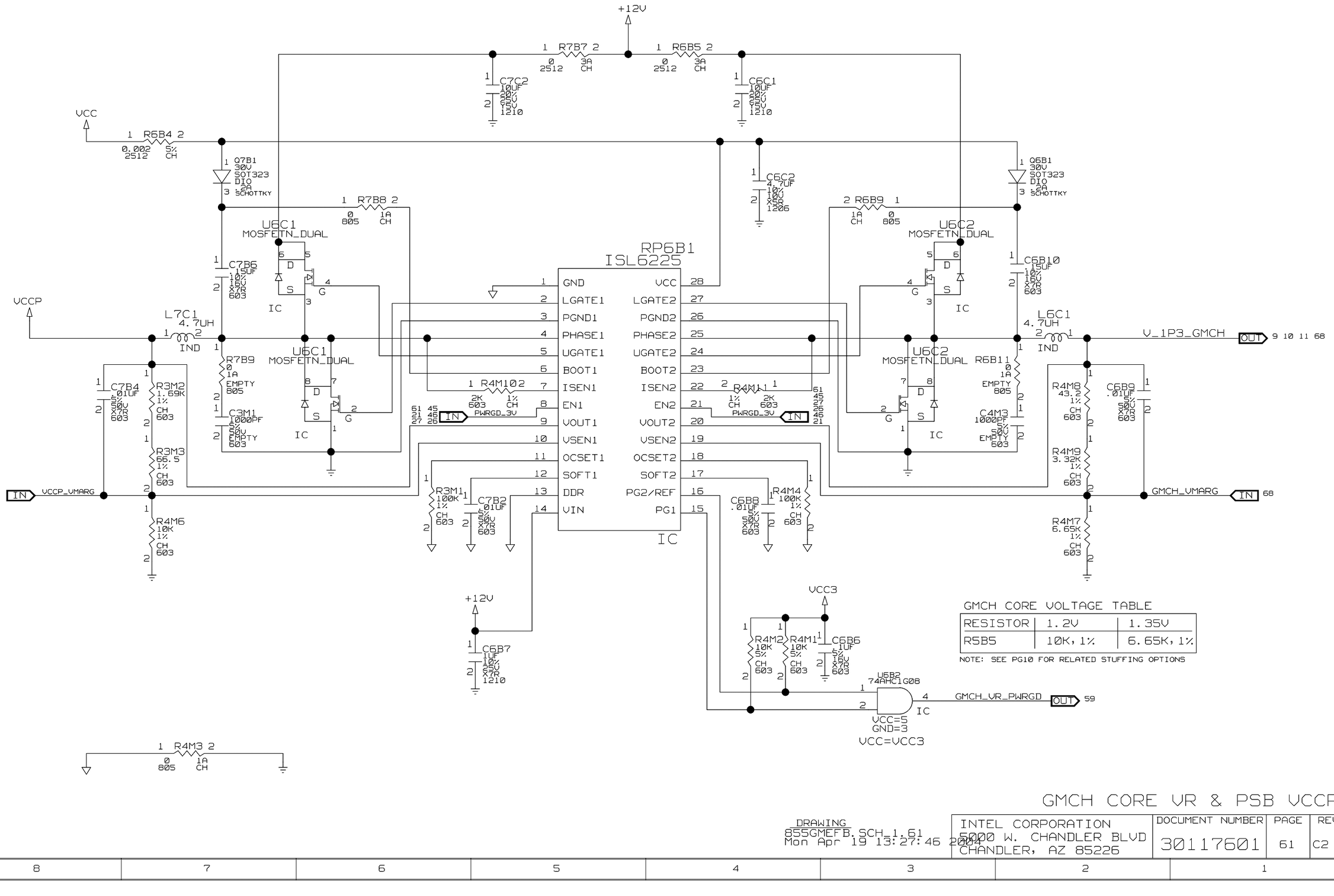
+12V
R7B6 0.002 2512 5%
VDC_PHASE2 OUT 59
C7B5 10UF 20% 25V X5R 1210
C7B3 10UF 20% 25V X5R 1210
C7C1 10UF 20% 25V X5R 1210
C7B7 10UF 20% 25V X5R 1210
C7C3 10UF 20% 25V X5R 1210

CPU DECOUPLING

DRAWING
855GMEFB.SCH_1.60
Mon Apr 19 13:27:47 2004

INTEL CORPORATION
5000 W. CHANDLER BLVD
CHANDLER, AZ 85226

DOCUMENT NUMBER	PAGE	REV
30117601	60	C2



GMCH CORE VOLTAGE TABLE

RESISTOR	1.2V	1.35V
R5B5	10K, 1%	6.65K, 1%

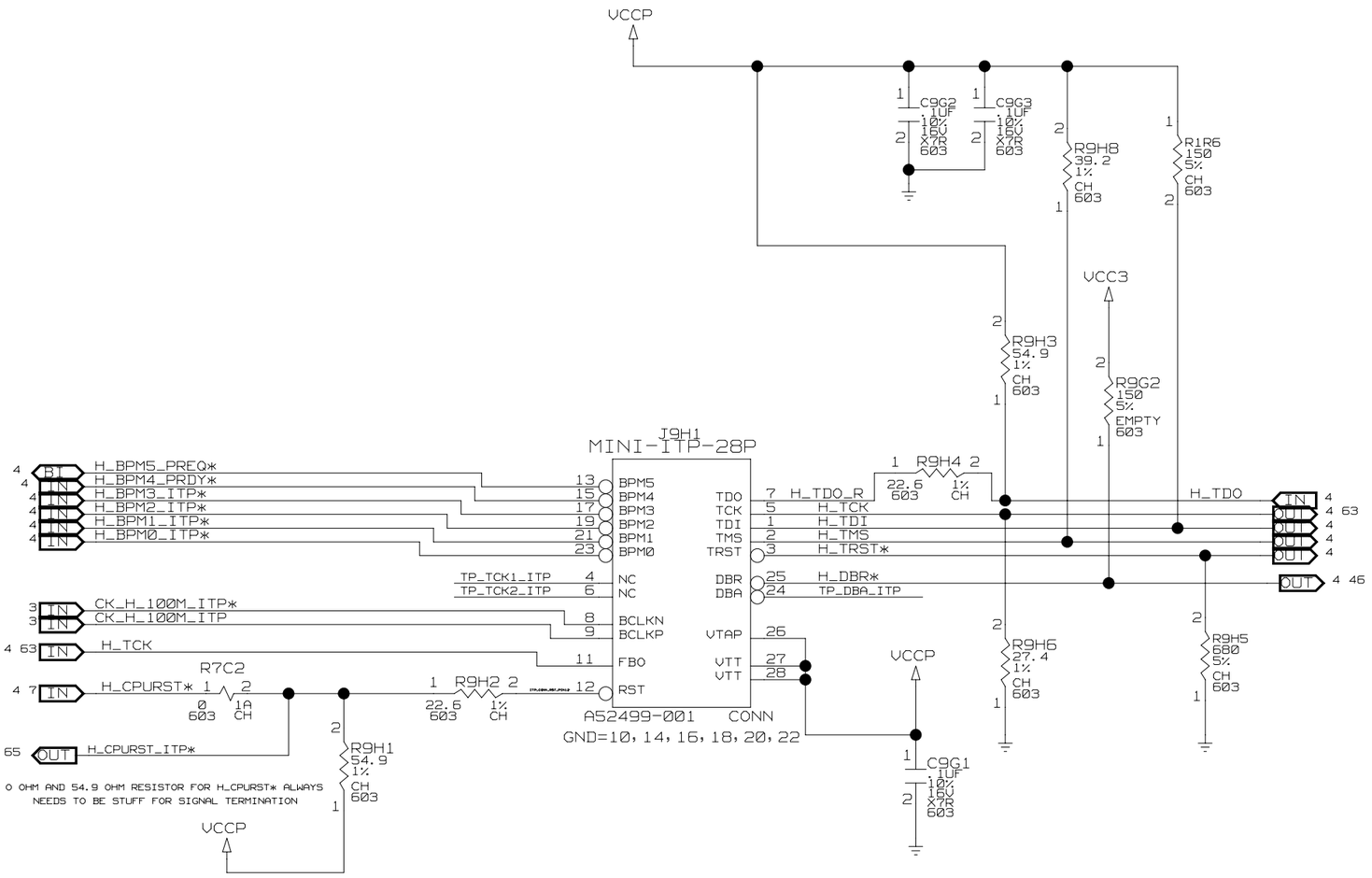
NOTE: SEE PG10 FOR RELATED STUFFING OPTIONS

GMCH CORE VR & PSB VCCP

DRAWING
855GMEFB.SCH_1.61
Mon Apr 19 13:27:46 2004

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	61	C2

DEBUG PAGES



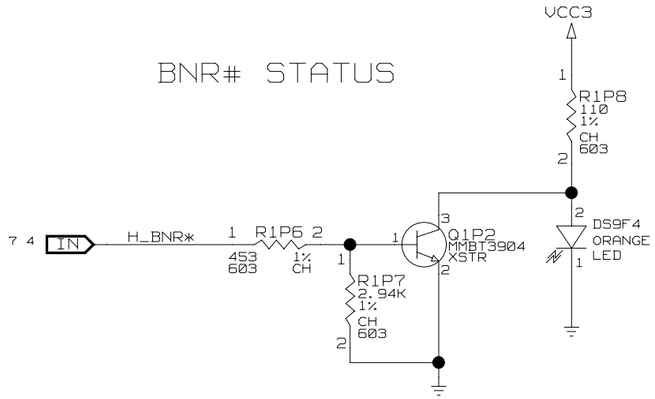
CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU.

SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

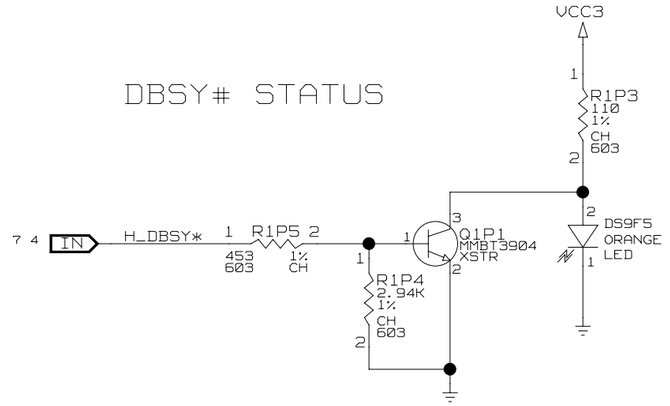
ITP 700FLEX CONNECTOR

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.63 Mon Apr 19 13:27:46 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	63	C2

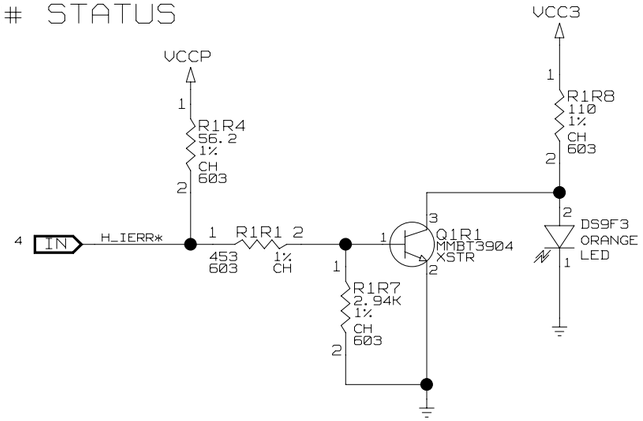
BNR# STATUS



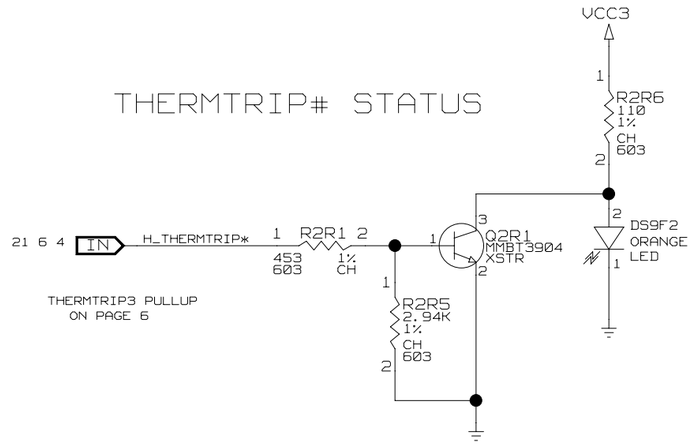
DBSY# STATUS



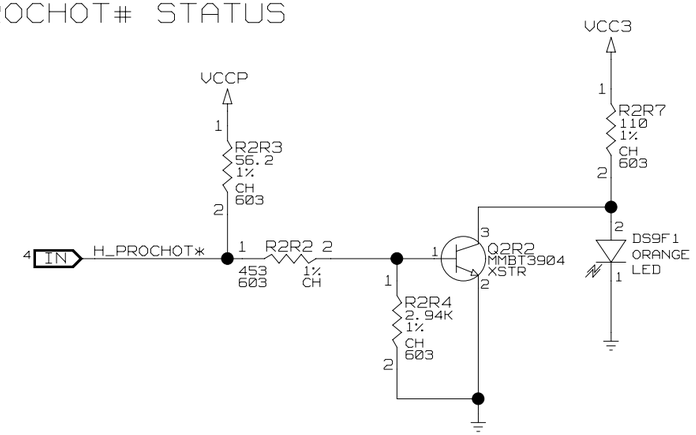
IERR# STATUS



THERMTRIP# STATUS



PROCHOT# STATUS

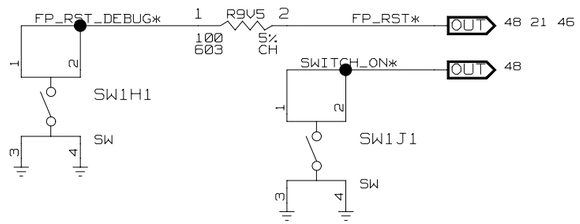


CPU STATUS LEDS

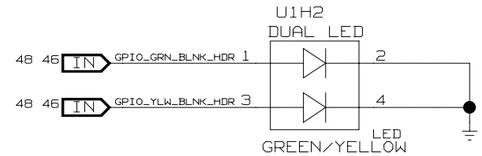
DRAWING
855GMEFB.SCH_1.64
Mon Apr 19 13:27:45 2004

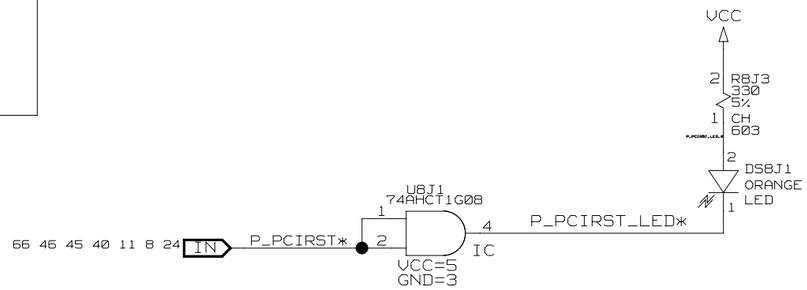
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER	PAGE	REV
	30117601	64	C2

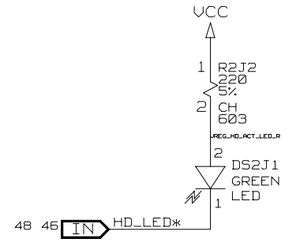
DEBUG/EV FEATURE: FRONT PANEL SWITCHES



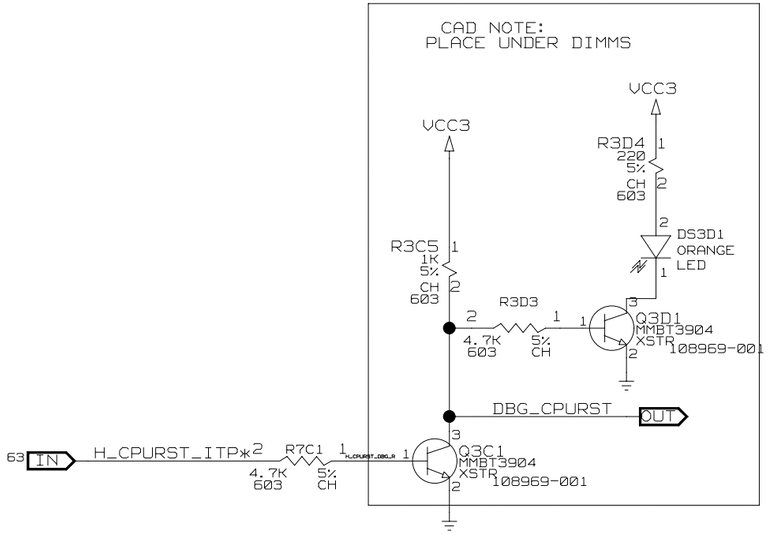
PRODUCT FEATURE: STATUS LED'S



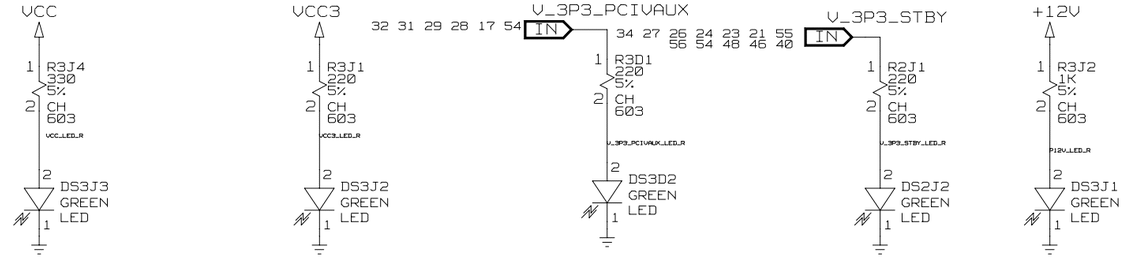




DEBUG/EV FEATURE: INVERTING LEVEL SHIFTERS ON FSB SIGNALS FOR DIAG LED'S



DEBUG/EV FEATURE: POWER RAIL STATUS LED'S

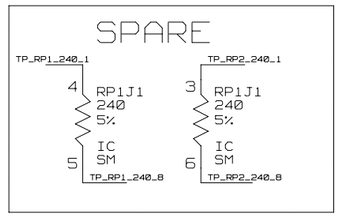


DEBUG STUFFING OPTIONS: BOM=VREG_LED_DEBUG

DEBUG LEDS, PWR/RST BTNS

DRAWING	INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
855GMEFB.SCH.1.65 Mon Apr 19 13:27:45 2004	5000 W. CHANDLER BLVD CHANDLER, AZ 85226	30117601	65	C2

SPARE

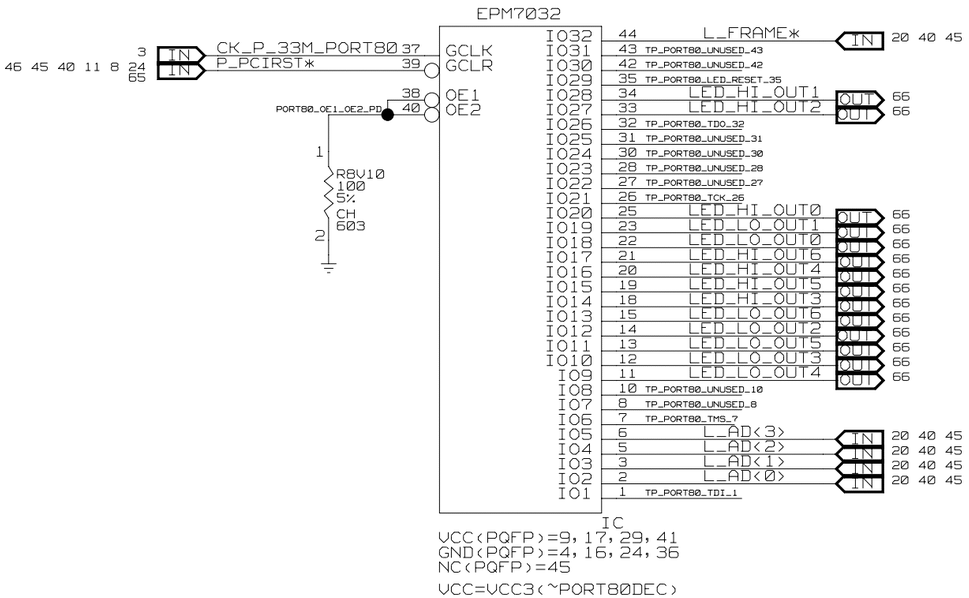


EPM7032AETC44-10

44 PIN TQFP

U2J1

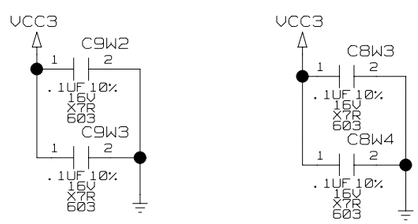
EPM7032



VCC(PQFP)=9,17,29,41
GND(PQFP)=4,16,24,36
NC(PQFP)=45

VCC=VCC3(~PORT80DEC)

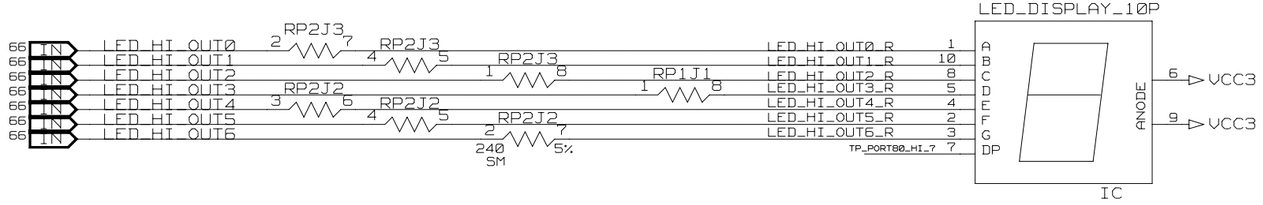
CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY



CAD NOTE: ORIENT TO LEFT

CR1J1

LED_DISPLAY_10P

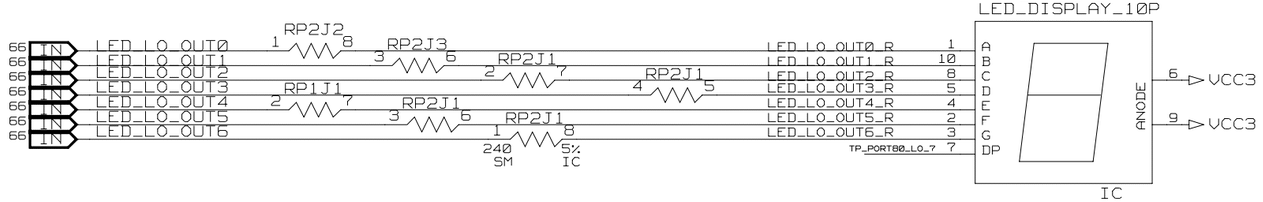


ALL RPACKS 240 OHMS

CAD NOTE: ORIENT TO RIGHT

CR2J1

LED_DISPLAY_10P



PORT 80 DECODER

DRAWING
855GMEFB.SCH_1.66
Mon Apr 19 13:27:45 2004

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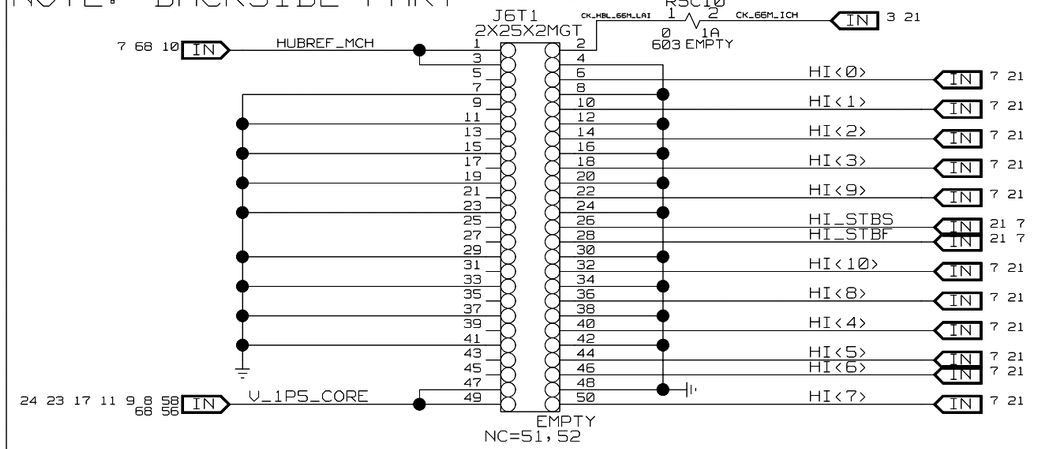
	30117601	66	C2

DEBUG/EV FEATURE: HUBLINK LAI HEADER

NOTE: BACKSIDE PART 700000-450

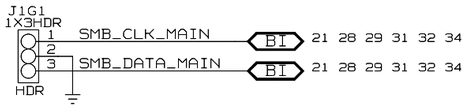
PLACE AT MIDPOINT OF HUBLINK ROUTING



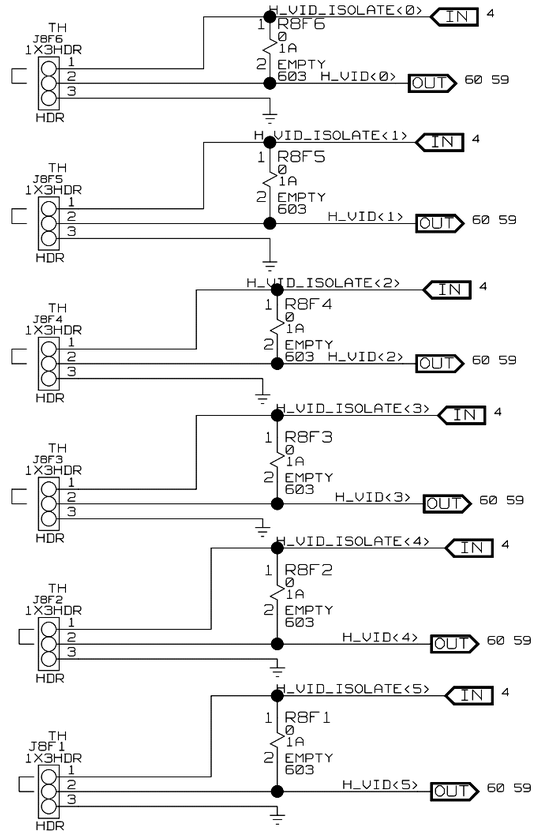
SOLDER MASK PADS: 5, 9, 13, 17, 21, 25, 27, 31, 35, 39, 43, 45

PINS ARE NOT ASSIGNED TP SIGNAL NAMES (PREVENTS TRACE CONNECTION)

DEBUG/EV FEATURE: SMBUS LAI HEADER

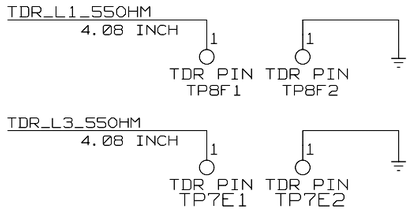


DEBUG/EV FEATURE: VID JUMPERS



VID 5	4	3	2	1	0	VCORE	VID 5	4	3	2	1	0	VCORE
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

DEBUG/EV FEATURE: TDR COUPONS



HI PROBE, SMB/VID JUMPERS, TDR

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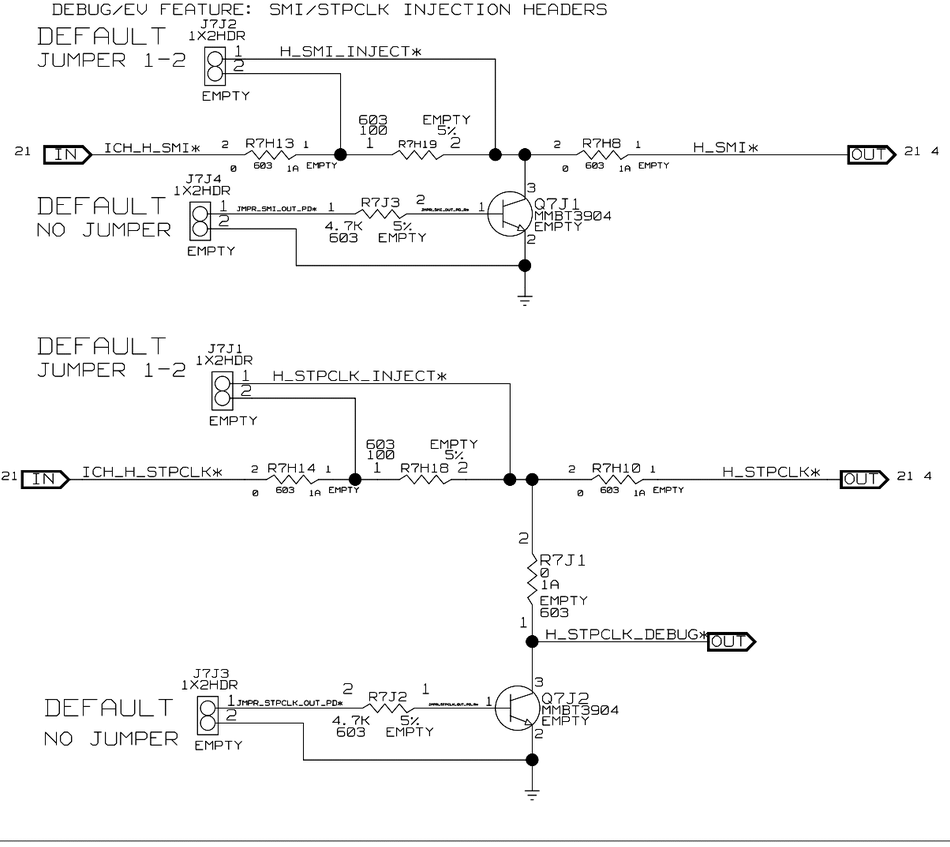
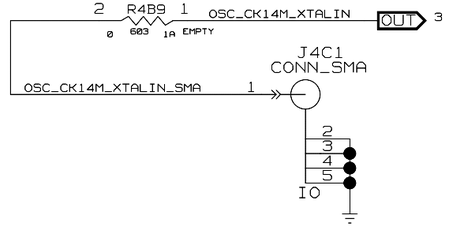
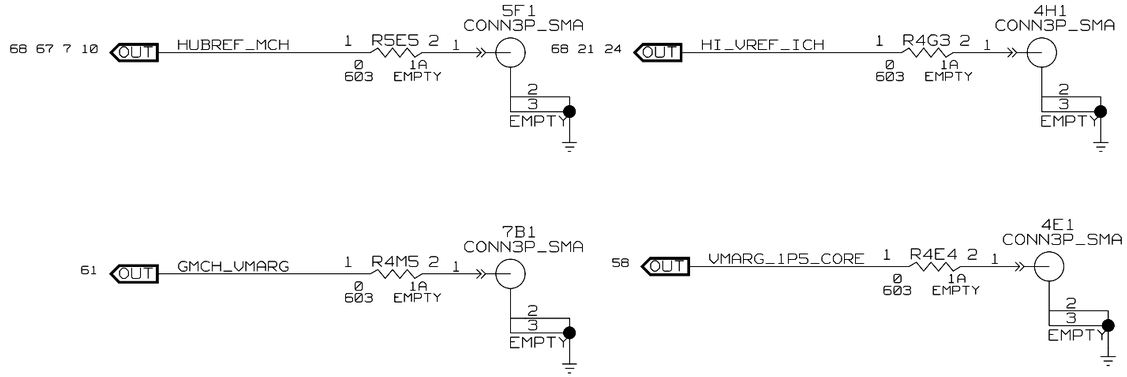
DEBUG/EV FEATURE: SMI/STPCLK INJECTION HEADERS

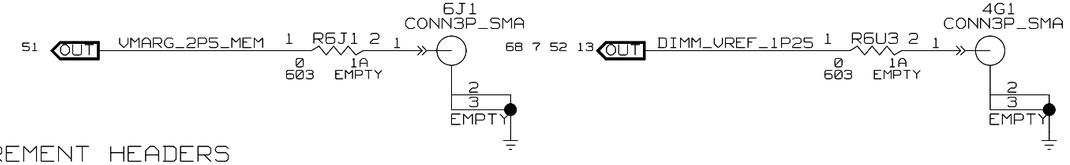


DEBUG FEATURE

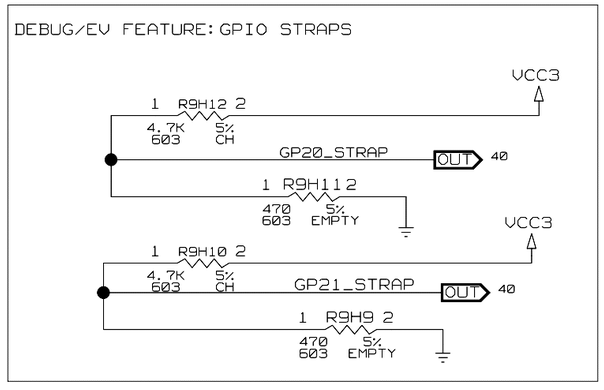


DEBUG/EV FEATURE: SMA MARGINING CONNECTORS

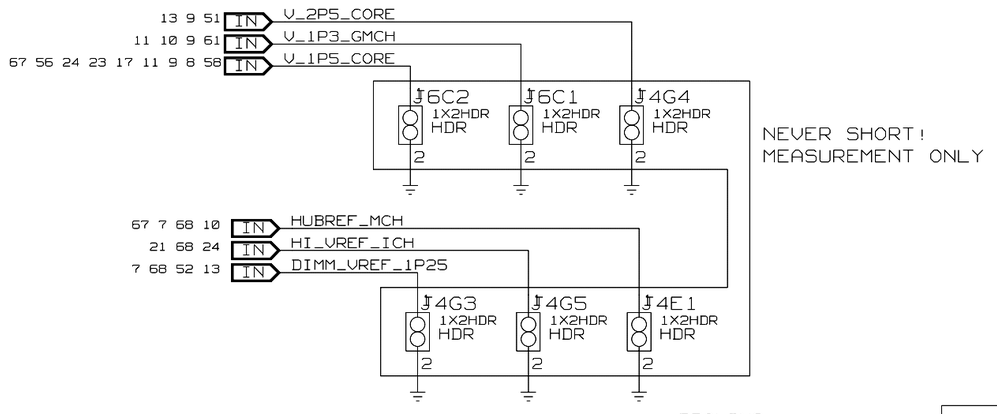




DEBUG/EV FEATURE: GPIO STRAPS



DEBUG/EV FEATURE: MEASUREMENT HEADERS



SMI/STPCLK INJECTION SMA CONNECTORS

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REVISION HISTORY

REV C0

MADE PUBLIC VERSION
CHANGED TO BPAGE PUBLIC

REV C1

REMOVED OLD DOC NO.

REV C2

P24 CHANGED R7V8 FROM EMPTY 10K TO POPULATED 8.2K
PAGE 2 ADDED AGP 4X TO DVO BLOCK
PAGE 4 REMOVED NS NOTE
PAGE 11 UPDATED STRAPPING TABLE

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