Intel® High Definition Audio Specification

Document Change Notification

Date: June 6, 2009
Company: Intel Corporation
Address: 1900 Prairie City Rd.
City: Folsom State: CA
Country: USA Zip: 95630
Phone:

Change Identification: **DCN No: HDA015-B**
Document Revision: Intel® High Definition Audio 1.0

Title: Low Power Capabilities Clarifications and Enhancements

Brief description of the functional changes:

This change of the specification will allow the power to be reduced when devices or the "codec" as a whole is not active. The challenges with the current version of the Intel High Definition Specification include:

1) Inability to put the codec into low power state as the ability to report jack presence state changes is not clearly called out and is thus not implemented in typical codecs today
2) Clarity for how to use low power states was missing, regarding the reporting of Unsolicited Responses and the ability to wake the system if in low power system states did not exist
3) Requirements on what is expected, such as no audio artifacts, and ability to go into low power states was not specified and thus most codecs did not implement sufficient capabilities for states below D0 to be used. As a result, codec low power states were typically not used (were disabled) in the past.
4) Lack of clarity on what happens to settings that have been changed across power states and resets.

This set of changes provides a clarification to controlling power at the widget level, adds a requirement to not pop or click when changing power states and also provides for an override function for nodes that support power state controls, but not the Supported Power States parameter.

This set of changes also clarifies the required operation for Jack presence detection and audio streams not coming from or going to the HD Audio link behave during power states other than fully on and during transitions.

In general this set of changes will allow lower power operation to be used by systems and codecs that implement these recommended changes. The changes specified are:

1) Codec does not generate spurious sound output on analog outputs such as headphone and speaker jacks during any power state changes.
2) Jack Presence state change reporting to operate in all D states except D3cold state of the Pin Widget, Codec in general and the Link power state.
3) System wake and reporting of presence, even if the Link clock is not running (Controller low power state)

4) Granular power management
5) Time required to exit D3 state back to fully on D0 state set to 10 milliseconds
6) Supported Power States command (Verb) is required for all widgets that report PowerCntrl bit set to 1 in their Audio Widget Capabilities response.
7) Reduction of D1 and D2 exit times to 1 and 2 milliseconds respectively.
8) Inclusion of the ability to reject D3 transition request if not able to due to loop through or other similar activity that the host software is not aware of
9) Inclusion of the ability to operate while the clock is stopped and to report that dynamically so that D3 can be used even if there is a chance that prior to stopping the clock, loops through or some other dependency removes the ability. Requires software poll state prior to stopping the clock.
10) Clearly state what settable values are reset by POR, Link and Function group resets. Clearly state what settings are persisted across Dx state transitions and Resets. Reporting of any of the settings changes across Dx state through a new status bit also included.
11) A new "Double" Function Group capability has been added to guarantee a full initialization of all settings as the settings are no longer initialized for simple Link and Function Group Resets.
12) Addition of a new power state that allows the codec to power gate most functionality for the lowest power consumption, thus removing the need for external power FETS for power gating the codec.

Current Definitions:

3.3.16 Offset 30h: Wall Clock Counter

The 32-bit monotonic counter provides a "wall clock" that can be used by system software to synchronize independent audio controllers. The counter must be implemented.

Length: 4 bytes

Table 16. Wall Clock Counter

Bit	Type	Reset	Description
31:0	RO	0000_0000h	**Wall Clock Counter (Counter):** 32 bit counter that is incremented at the link bit clock rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to 0 with a period of approximately 179 seconds with the nominal 24-MHz bit clock rate. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. The counter will be reset on controller reset.

• • •

5.5.2 Codec Function Group Reset

A codec function group reset allows software to initialize/reset a specific Codec function group without affecting or interrupting the operation of the Link. A codec function group reset is initiated via the Function RESET command verb, as described in Section 7.3.3.33, and results in all logic within the targeted function group being driven to its default or reset state.

5.5.3 Codec Initialization

Immediately following the completion of any reset sequence, all affected Codecs proceed through a codec initialization sequence as described in this section and shown in Figure 30. The purpose of this initialization sequence is to provide each

codec with a unique address by which it can thereafter be referenced with Commands on the **SDO** (broadcast) signal. During this sequence, the Controller provides each requesting codec with a unique address using its attached **SDI** signal(s). Controllers are required to support independent (simultaneous) initialization on all **SDI** signals. Independent initialization allows for codecs to be connected to the interface, be hard reset, and assigned an address even when the link is in normal running state which is required for hot docking.

5.6 Power Management

The High Definition Audio Architecture is designed to support all relevant power management features. In most cases, all power management state changes are driven by software, either through controller control registers or Command verbs to codecs. The exception to this is when a codec is put into a low power mode awaiting an external wake up event, such as a ring indication on a modem. In this case, the external wake event results in a power state change request on the Link as described below.

Whenever the Link is commanded to enter a low power state, it enters the link-reset state, as described in Section 5.5.1. This state is only exited in response to a software command and follows all link rules for exiting the link reset state.

Codecs, when put into a lower power state awaiting an external event, will post the occurrence of a wake event and request a power state change by signaling a power state change request and initialization request as described in Section 5.5.3.1. If **BCLK** and **SYNC** are running at the time of the event, the codec will signal an unsolicited response as described in Section 5.5.3. If **BCLK** and **SYNC** are not running at the time, the codec will signal the power state change request and initialization request asynchronously by asserting **SDI** continuously until it detects the de-assertion of **RST#**, as shown in Figure 33.

7.3.3.10 Power State

The **Power State** control determines the power state of the node to which it refers. There is no required power saving or maximum allowed power in any of the low power states; rather these states allow the vendor to reduce power by as much or as little as desired to meet their customer needs. However, power must never be reduced to a given circuit in a manner that would be inconsistent with the specified power recovery requirements of that power state.

Command Options:

Table 78 Power State

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F05h	0	Bits 31:8 are 0 PS-Act is in bits 7:4 PS-Set is in bits 3:0
Set	705h	PS-Set in bits 0:3 bits 4:7 are 0	0

PS-Set is a Power State field which defines the current power setting of the referenced node. If the referenced node is of any type other than a Function Group node, the actual power state is a function of both this setting and the Power State setting of the Function Group node under which the currently referenced node was enumerated (is controlled).

PS-Act is a Power State field which indicates the actual power state of the referenced node. Within a Function Group type node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within any other type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Function Group node under which the currently referenced node was enumerated (is controlled).

All Power State fields are defined as follows:

Power State[1:0]:
00: Node Power state (D0) is fully on.
01: Node Power state (D1) allows for (does not require) the lowest possible power consuming state from which it can return to the "fully on" state (D0) within 10 ms, excepting analog pass through circuits (e.g., CD analog playback) which must remain fully on.
10: Node Power state (D2) allows for (does not require) the lowest possible power consuming state from which it can return to the "fully on" state (D0) within 10 ms. For modems, this is the "wake on ring" power state.
11: Node Power state (D3) allows for (does not require) lowest possible power consuming state under software control. Note that any low power state set by software must retain sufficient operational capability to properly respond to subsequent software Power State command.
PowerState[3:2]: *Reserved*, always 0.

While Function Group nodes (Audio Function, Modem Function, etc.) and Power Widget nodes must support this control, other widget nodes may optionally implement this control to provide more fine-grained power management of the codec. For Audio Widgets, such as Input Converter or Output Converter Widgets, the Audio Widget Capabilities parameter (see Section 7.3.4.6) will define whether this control is supported.

Applies to:

(a) Audio Function Group
(b) Modem Function Group
(c) Other Function Group
(d) Power Widget
(e) Input Converter (Optional)
(f) Output Converter (Optional)
(g) Selector Widget (Optional)
(h) Mixer Widget (Optional)
(i) Pin Complex (Optional)

• • •

7.3.3.13 Pin Widget Control

Pin Widget Control controls several aspects of the Pin Widget.

Command Options:

Table 1. Enable VRef

	Verb ID	**Payload (8 Bits)**	**Response (32 Bits)**
Get	F07h	0	Bits 31:8 are 0 Bits 7:0 are PinCntl
Set	707h	Bits 7:0 are PinCntl	0

PinCntl format:

7	**6**	**5**	**4:3**	**2:0**
H-Phn Enable	Out Enable	In Enable	Rsvd	VRefEn

Figure 1. PinCntl Format

H-Phn Enable disables/enables a low impedance amplifier associated with the output. The value 1 enables the amp. Enabling a non-existent amp is ignored.

Out Enable allows the output path of the Pin Widget to be shut off. The value 1 enables the path. Enabling a non-existent amp is ignored.

In Enable allows the input path of the Pin Widget to be shut off. The value 1 enables the path.

VRefEn: Voltage Reference Enable controls the VRef signal(s) associated with the Pin Widget. If more than one of the bits in the VRef[7:0] field of the Pin Capabilities parameter (Section 7.3.4.9) are non-zero, then this control allows the signal level to be selected.

The VRefEn field encoding selects one of the possible states for the VRef signal(s). If the value written to this control does not correspond to a supported value as defined in the Pin Capabilities parameter, the control must either retain the previous value or take the value of 000, which will put the control in a Hi-Z state and prevent damage to any attached components. Table 2 enumerates the possible values for VRefEn which correlate to the values identified in the Pin Capabilities parameter (see Figure 77).

Table 2. VRefEn Values

VRefEn Encoding	VREF Signal Level
000b	Hi-Z
001b	50%
010b	Ground (0 V)
011b	*Reserved*
100b	80%
101b	100%
110b-111b	*Reserved*

Applies to:

- Pin Complex

• • •

7.3.3.9 Digital Converter Control

The **Digital Converter Controls 1** and **2** operate together to provide a set of bits to control the various aspects of the digital portion of the Converter Widget. The S/PDIF IEC Control (SIC) bits are supported in one of two ways.
In the first case referred to as “Codec Formatted SPDIF,” if a PCM bit stream of less than 32 bits is specified in the Converter Format control, then the S/PDIF Control bits, including the “V,” “PRE,” “/AUDIO,” and other such bits are embedded in the stream by the codec using the values (SIC bits) from the Digital Converter Control 1 and 2. On an input PCM stream of less than 32 bits, the codec strips off these SIC bits before transferring the samples to the system and places them in the Digital Converter Control 1 and 2 for later software access.
In the second case referred to as “Software Formatted (or Raw) SPDIF,” if a 32-bit stream is specified in the Converter Format control, the S/PDIF IEC Control (SIC) bits are assumed to be embedded in the stream by software, and the raw 32-bit stream is transferred on the link with no modification by the codec. Similarly, on a 32-bit input stream, the entire stream is transferred into the system without the codec stripping any bits. However, the codec must properly interpret the Sync Preamble bits of the stream and then send the appropriately coded preamble. The IEC60958 specification, Section 4.3, “Preambles,” defines the preambles and the coding to be used. Software will specify the “B,” “M,” or “W” (also known as

"X," "Y," or "Z") preambles by encoding the last four bits of the preamble into the Sync Preamble section (bits 0-3) of the frame. The codec must examine the bits specified and encode the proper preamble based on the previous state. The previous state is to be maintained by the codec hardware. For more information on Preamble Coding, consult Section 4.3 of the IEC 60958 specification.

Table 3. SPDIF Sync Preamble Bits

Preamble Bits Set by Software (Bits 3:0 of Frame)	Preamble Coding	
	Previous State = 0	Previous State = 1
1000b ("B" or "Z")	11101000	00010111
0010b ("M" or "X")	11100010	00011101
0100b ("W" or "Y")	11100100	00011011

Command Options:

Table 4. S/PDIF Converter Control 1 and 2

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F0Dh[1]	0	Bits 31:16 are 0 Bits 15:0 are SIC bits
Set 1	70Dh	SIC bits [7:0]	0
Set 2	70Eh	SIC bits [15:8]	0

15	14:8	7	6	5	4	3	2	1	0
Rsvd	CC[6:0]	L	PRO	/AUDIO	COPY	PRE	VCFG	V	DigEn

Figure 2. S/PDIF IEC Control (SIC) Bits

CC[6:0] (Category Code): Programmed according to IEC standards, or as appropriate.
L (Generation Level): Programmed according to IEC standards, or as appropriate.
PRO (Professional): 1 indicates Professional use of channel status; 0 indicates Consumer.
/AUDIO (Non-Audio): 1 indicates data is non-PCM format; 0 indicates data is PCM.
COPY (Copyright): 1 indicates copyright is asserted; 0 indicates copyright is not asserted.
PRE (Preemphasis): 1 indicates filter preemphasis is 50/15 µs; 0 preemphasis is none.
VCFG (Validity Config.): Determines S/PDIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the de-assertion of the S/PDIF "Validity" flag, which is bit 28 transmitted in each S/PDIF subframe. This bit is only defined for Output Converters and is defined as Reserved, with a Read Only value of 0 for Input Converters.

If "V" = 0 and "VCFG"=0, then for each S/PDIF subframe (Left and Right) bit[28] "Validity" flag reflects whether or not an internal codec error has occurred (specifically whether the S/PDIF interface received and transmitted a valid sample from the High Definition Audio Link). If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be 0 for that subframe. Otherwise, the "Validity" flag for that subframe should be transmitted as "1."

If "V" = 0 and "VCFG" = 1, then for each S/PDIF subframe (Left and Right), bit[28] "Validity" flag reflects whether or not an internal codec transmission error has occurred. Specifically, an internal codec error should result in the "Validity" flag being set to 1. In the case where the S/PDIF transmitter is not receiving a sample or does not receive a valid sample from the High Definition Audio Controller (Left or Right), the S/PDIF transmitter should set the S/PDIF "Validity" flag to 0 and pad each of the S/PDIF "Audio Sample Word" in question with 0's for the subframe in question.

[1] The Verb Code F0Eh is reserved for S/PDIF Converter Control 2 and may never be reassigned to anything else. However, it need not be implemented since standard software drivers must never use it. If a codec elects respond to this code, the response must be identical in all respects to the response to Verb Code F0Dh.

If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be 0 for that subframe.

If "V" = 1 and "VCFG" = 0, then each S/PDIF subframe (Left and Right) should have bit[28] "Validity" flag = 1. This tags all S/PDIF subframes as invalid.

"V" = 1 and "VCFG" = 1 state is reserved for future use.

Default state, coming out of reset, for "V" and "VCFG" should be 0 and 0 respectively.

V (Validity): This bit affects the "Validity flag," bit[28] transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. The behavior of the S/PDIF transmitter with respect to this bit depends on the value of the "VCFG" bit.

DigEn (Digital Enable): Enables or disables digital transmission through this node. A 1 indicates that the digital data can pass through the node. A 0 indicates that the digital data is blocked from passing through the node, regardless of the state.

Applies to:

Input Converter

Output Converter

7.3.3.29 Volume Knob

Volume Knob provides the controls for an optional external hardware volume control.

Command Options:

Table 5. Volume Knob Control

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F0Fh	0	Bit 7 is Direct Bits 6:0 is Volume
Set	70Fh	Bit 7 is Direct Bits 6:0 is Volume	0

Direct causes the Volume Control Widget to directly control the hardware volume of the slave amplifiers. If "Direct" is set to a 0, the volume control will not directly affect the volume of the slaves amplifiers; rather, the software receives an unsolicited response, reads the volume control, and then programs the appropriate amplifiers correctly.

Volume is specified in steps, as is amplifier gain. If two amplifiers slaved to the Volume Knob control have different "StepSize" parameters, they are both adjusted by the same number of steps, implying a differing total dB treatment. If the Volume Knob control has more steps than a slave amplifier is capable of supporting (as indicated in the Volume Knob Capabilities parameter), the amplifier remains at its limiting value.

Applies to:

- Volume Knob Widget

• • •

7.3.3.33 Function Reset

The **Function Reset** command causes the functional unit, and all widgets associated with the functional unit, to return to their power-on reset values. Note that some controls such as the Configuration Default controls should not be reset with this command. It is also possible that certain other controls, such as Caller-ID, should not be reset.

This command does not affect the Link interface logic, which must be reset with the link **RST#** signal. Therefore, a codec must not initiate a Status Change request on the link.

When a codec receives the Function reset verb, the expected behavior is that the codec will issue a response to the verb to acknowledge receipt, and then reset the affected Function Group controls. The codec must be ready to respond to the verbs on the Link frame after the frame on which it returns its response to the Reset command.

Command Options:

Table108. Function Reset

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Execute	7FFh	0	0

Applies to:

(a) Audio Function Group
(b) Modem Function Group
(c) Other Function Group

• • •

7.3.4.12 Supported Power States

Returns a bit field describing the power states supported by the functional unit and widgets.
Parameter ID: 0Fh
Response Format:

31:8	3	2	1	0
Reserved	D3Sup	D2Sup	D1Sup	D0Sup

Figure80. Supported Power States Response Format

Applies to:

(a) Audio Function
(b) Modem Function
(c) Other Functions
(d) Power Widget
(e) Other Widgets (optional)

New Definition:

3.3.16 Offset 30h: Wall Clock Counter

The 32-bit monotonic counter provides a "wall clock" that can be used by system software to synchronize independent audio controllers. The counter must be implemented.

Length: 4 bytes

Table 16 Wall Clock Counter

Bit	Type	Reset	Description
31:0	RO	0000_0000h	**Wall Clock Counter (Counter):** 32 bit counter that is incremented at the link bit clock rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to 0 with a period of approximately 179 seconds with the nominal 24-MHz bit clock rate. This counter will only operate (count) while the BitClk on the link for this controller is running. During low power states of the controller the clock may not be running and thus software should not assume that the counter continued to increment across Dx states and re-synchronize once the controller returns to the D0 state. Software uses this counter to synchronize between multiple controllers. The counter will be reset by controller reset.

• • •

5.5.2 Codec Function Group Reset

A codec function group reset allows software to initialize/reset a specific Codec function group without affecting or interrupting the operation of the Link. A codec function group reset is initiated via the Function RESET command verb, as described in Section 7.3.3.33, and results in all logic within the targeted function group being driven to its default or reset state. For codecs that report Extended Power States Supported of one (1) this Function Reset does not initialize some of the settings that are programmable by host software. Which settings are persisted is defined in Table T2. Host software may send two Function Resets (possibly separated by an undefined number of idle frames, but no other valid commands) , which shall cause a full reset of all settings. For more information, see Section 7.3.3.33.

A single or double Function Group reset does not cause the codec to perform the "Codec Initialization request" sequence defined in section 5.5.3.

5.5.3 Codec Initialization

Immediately following the completion of Link Reset sequence or when requesting a power state change when the link is in a low power state, all affected Codecs proceed through a codec initialization sequence as described in this section and shown in Figure 30. The purpose of this initialization sequence is to provide each codec with a unique address by which it can thereafter be referenced with Commands on the **SDO** (broadcast) signal. During this sequence, the Controller provides each requesting codec with a unique address using its attached **SDI** signal(s). Controllers are required to support independent (simultaneous) initialization on all **SDI** signals. Independent initialization allows for codecs to be connected to the interface, be hard reset, and assigned an address even when the link is in normal running state which is required for hot docking. A codec in a low power state (D1 through D3 and D3cold) retains its address while in that low power state. If the link is in reset and the codec requests a power state change back to fully powered (D0), it is required for the codec to reestablish the connection with the controller by performing a "Codec Initialization request" as specified in this section. During link initialization, the controller shall assign to the codec the same address that the codec had prior to the link being reset, as long as the codec remains on the same SDI line.

• • •

5.6 Power Management

The High Definition Audio Architecture is designed to support all relevant power management features. In most cases, all power management state changes are driven by software, either through controller control registers or Command verbs to codecs. The exception to this is when a codec (Function Group) is put into a low power mode either waiting for an external wake up event, such as a ring indication on a modem or a state change that requires that the codec be placed into D0 (Fully powered) such as Jack Presence Detection change for an Audio Codec's attached device or a Modem Codec's ring detection. In this case, the external event results in a power state change request on the Link as described below.

Whenever the Link is commanded to enter a low power state, it enters the link-reset state, as described in Section 5.5.1. This state is only exited in response to a software command and follows all link rules for exiting the link reset state.

Codec's Function Group, when put into a lower power state where the Function Group may need to return to D0 (Fully Powered), will post the occurrence of a wake event and request a power state change by signaling a power state change request and if necessary, based on link power state, an initialization request as described in Section5.5.3.1. If **BCLK** and **SYNC** are running at the time of the event, the codec will signal an unsolicited response. If **BCLK** and **SYNC** are not running at the time, the codec will signal the power state change request and initialization request asynchronously by asserting **SDI** continuously until it detects the de-assertion of **RST#**, as shown in Figure 33.

• • •

7.3.3.9 Digital Converter Control

The **Digital Converter Controls 1, 2, 3 and 4** operate together to provide a set of bits to control the various aspects of the digital portion of the Converter Widget. The S/PDIF IEC Control (SIC) bits are supported in one of two ways.
In the first case referred to as "Codec Formatted SPDIF," if a PCM bit stream of less than 32 bits is specified in the Converter Format control, then the S/PDIF Control bits, including the "V," "PRE," "/AUDIO," and other such bits are embedded in the stream by the codec using the values (SIC bits) from the Digital Converter Control 1 and 2. On an input PCM stream of less than 32 bits, the codec strips off these SIC bits before transferring the samples to the system and places them in the Digital Converter Control 1 and 2 for later software access.
In the second case referred to as "Software Formatted (or Raw) SPDIF," if a 32-bit stream is specified in the Converter Format control, the S/PDIF IEC Control (SIC) bits are assumed to be embedded in the stream by software, and the raw 32-bit stream is transferred on the link with no modification by the codec. Similarly, on a 32-bit input stream, the entire stream is transferred into the system without the codec stripping any bits. However, the codec must properly interpret the Sync Preamble bits of the stream and then send the appropriately coded preamble. The IEC60958 specification, Section 4.3, "Preambles," defines the preambles and the coding to be used. Software will specify the "B," "M," or "W" (also known as "X," "Y," or "Z") preambles by encoding the last four bits of the preamble into the Sync Preamble section (bits 0-3) of the frame. The codec must examine the bits specified and encode the proper preamble based on the previous state. The previous state is to be maintained by the codec hardware. For more information on Preamble Coding, consult Section 4.3 of the IEC 60958 specification.

Table 6. SPDIF Sync Preamble Bits

Preamble Bits Set by Software (Bits 3:0 of Frame)	Preamble Coding	
	Previous State = 0	Previous State = 1
1000b ("B" or "Z")	11101000	00010111
0010b ("M" or "X")	11100010	00011101
0100b ("W" or "Y")	11100100	00011011

Command Options:

Table 7. S/PDIF Converter Control 1, 2, 3 and 4

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F0Dh[2]	0	Bits 31:24, 22:20, 15 are 0 Bits 31:0 are SIC bits
Set 1	70Dh	SIC bits [7:0]	0
Set 2	70Eh	SIC bits [15:8]	0
Set 3	73Eh	SIC bits [23:16]	0
Set 4	73Fh	SIC bits [31:24]	Rsvd 0

31:24	23	22:20	19:16	15	14:8	7	6	5	4	3	2	1	0
Rsvd	*Keep Alive Enable*	*Rsvd*	*IEC Coding Type*	*Rsvd*	CC[6:0]	L	PRO	/AUDIO	COPY	PRE	VCFG	V	DigEn

Figure 3. S/PDIF IEC Control (SIC) Bits

KeepAlive (Keep Alive Enable): this bit is applicable only to digital converter widget that is associated (selected by) an Output Digital Pin Widget. This bit allows for software programmed control of S/P-DIF, HDMI and Display Port interfaces to continue to provide clocking information to an attached device. Many such digitally connected audio devices can take more than one second to start playing audio after the clock has stopped, which occurs for example when the Converter and/or Digital Pin Widget is placed into a low power state or even just when a stream is stopped for S/P-DIF. Although this capability is more closely associated with the output port and thus the converter widget, the generation of a valid digital stream and clock is normally provided by the Converter Widget and thus this functionality is included here. Support for the **KeepAlive Enable** is mandatory after July 1st 2011, if EPSS is reported set to 1. When **KeepAlive Enable** is set to 1 the output will supply a continuous clock, and a valid but 'silent' data stream, even when no stream is selected by this Converter Widget and while the Digital Converter and/or Digital Pin Widget connected to this Converter Widget is in D0-D3[3]. If D3cold state is supported, then the "Keep Alive" shall not be operational while in the D3cold state.

When the output from the Pin Widget connected to this Converter Widget is connected to a combination electrical and optical (TOSLINK) jack, the jack-detection capability of the electrical 3.5mm jack must also be used to report Presence Detection in the Digital Pin Widget associated with this Digital Converter's S/P-DIF output, and must also support an unsolicited response generation when the jack state changes. It is recommended that driver software disable the keep alive bit when the output port is not connected and enable it when the output port is connected to reduce the power consumed during idle. It is also recommended that driver software disable the keep alive bit when the associated output port is connected but when the Optical S/P-DIF output is not the default output device.

As mentioned above, the Keep Alive Enable bit is not applicable to input converters of digital ports. In the case of an input port, the driver software should periodically (e.g. every few seconds) wake up the Function Group out of D3 state and poll the port to see if it has locked to an input stream. If the input port is connected to a combo jack, jack-detection capability must be supported and an unsolicited response must be generated when the jack state changes. In that case, software will have to periodically poll for lock status only when it knows that the port is connected to an external transmitter.

[2] The Verb Code F0Eh is reserved for S/PDIF Converter Control 2 and may never be reassigned to anything else. However, it need not be implemented since standard software drivers must never use it. If a codec elects respond to this code, the response must be identical in all respects to the response to Verb Code F0Dh.

[3] It is likely that an output s/pdif data stream cannot be generated, unless the HD Audio link clock is running. In that case, if the s/pdif output ports must be kept alive in D3 state, the bus link clock will have to not be allowed to turn off when in the CODEC is placed in D3 state

IEC Coding Type [3:0] (IEC Coding Type): Programmed according to IEC standards to enable stream types for High Bit Rate Encoding. This is valid only for HDMI and Display port digital Pin Widgets.

CC[6:0] (Category Code): Programmed according to IEC standards, or as appropriate.
L (Generation Level): Programmed according to IEC standards, or as appropriate.
PRO (Professional): 1 indicates Professional use of channel status; 0 indicates Consumer.
/AUDIO (Non-Audio): 1 indicates data is non-PCM format; 0 indicates data is PCM.
COPY (Copyright): 1 indicates copyright is asserted; 0 indicates copyright is not asserted.
PRE (Preemphasis): 1 indicates filter preemphasis is 50/15 µs; 0 preemphasis is none.
VCFG (Validity Config.): Determines S/PDIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the de-assertion of the S/PDIF "Validity" flag, which is bit 28 transmitted in each S/PDIF subframe. This bit is only defined for Output Converters and is defined as Reserved, with a Read Only value of 0 for Input Converters.

If "V" = 0 and "VCFG"=0, then for each S/PDIF subframe (Left and Right) bit[28] "Validity" flag reflects whether or not an internal codec error has occurred (specifically whether the S/PDIF interface received and transmitted a valid sample from the High Definition Audio Link). If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be 0 for that subframe. Otherwise, the "Validity" flag for that subframe should be transmitted as "1."

If "V" = 0 and "VCFG" = 1, then for each S/PDIF subframe (Left and Right), bit[28] "Validity" flag reflects whether or not an internal codec transmission error has occurred. Specifically, an internal codec error should result in the "Validity" flag being set to 1. In the case where the S/PDIF transmitter is not receiving a sample or does not receive a valid sample from the High Definition Audio Controller (Left or Right), the S/PDIF transmitter should set the S/PDIF "Validity" flag to 0 and pad each of the S/PDIF "Audio Sample Word" in question with 0's for the subframe in question. If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be 0 for that subframe.

If "V" = 1 and "VCFG" = 0, then each S/PDIF subframe (Left and Right) should have bit[28] "Validity" flag = 1. This tags all S/PDIF subframes as invalid.

"V" = 1 and "VCFG" = 1 state is reserved for future use.

Default state, coming out of reset, for "V" and "VCFG" should be 0 and 0 respectively.

V (Validity): This bit affects the "Validity flag," bit[28] transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. The behavior of the S/PDIF transmitter with respect to this bit depends on the value of the "VCFG" bit.
DigEn (Digital Enable): Enables or disables digital transmission through this node. A 1 indicates that the digital data can pass through the node. A 0 indicates that the digital data is blocked from passing through the node, regardless of the state.
Applies to:

Input Converter
Output Converter

7.3.3.10 Power State

The **Power State** control determines the power state of the node to which it refers. There is no required power saving or maximum allowed power in any of the low power states; rather these states allow the vendor to reduce power by as much or as little as desired to meet their customer needs. However, power must never be reduced to a given circuit in a manner that would be inconsistent with the specified power recovery requirements of that power state.

It is required that no anomalous sounds be generated by any node while it is transitioning between power states. For example no Pop or Clicks should be generated on an output port during D0 to D3 or other states and visa versa. If Pops or Clicks are produced during power state transitions, then the codec must suppress these without any software directed action, other than the power state control change. This applies to audio or modem codecs or other codecs which generate analog audio output.

Command Options:

Table 78 Power State

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F05h	0	Bits 31:11 are 0 and reserved PS-SettingsReset is in bit 10 PS-ClkStopOk is in bit 9 PS-Error is in bit 8 PS-Act is in bits 7:4 PS-Set is in bits 3:0
Set	705h	PS-Set in bits 0:3 bits 4:7 are Reserved and 0	0

PS-Set is a Power State field which defines the current power setting of the referenced node. If the referenced node is of any type other than a Function Group node, the actual power state is a function of both this setting and the Power State setting of the Function Group node under which the currently referenced node was enumerated (is controlled).

PS-Act is a Power State field which indicates the actual power state of the referenced node. Within a Function Group type node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition, if currently in transition from a lower to higher power consuming state or from a higher power consuming state to D3cold). Within any other type of node, this field will be the lower power consuming state of either the currently referenced node or the Function Group node under which the currently referenced node was enumerated (is controlled).

PS-Error is reported as set to 1, when the power state requested by the host is not possible at this time. This may occur if there are dependencies between nodes that require both to be in D0 for proper operation or in cases where some operation that the host is unaware of, prohibits entering the D3 state. If the node responds to a Set Power State verb by setting the PS-Error bit to '1', then the node will remain in its previous power state at least until it receives the next Set Power State verb. If the node is going to remain in its previous power state, it shall set the PS-Error bit immediately, so it can be read by software in the next frame. If the node does not set the PS-Error bit after it receives a Set Power State verb, then it will transition to the commanded state (even though it may or may not allow for the link clock to turn off, as explained below). In all cases the reported states for Active and Set states will report both the requested and the actual power state. Note, however, that the latency from receiving the Set Power State verb to PS-Act getting updated to reflect the new state depends on the hardware implementation, so testing whether PS-Act is equal to PS-Set is not a safe way to determine whether the node was able to transition to the commanded power state or not. PS-Error should be used for that.

If a widget is commanded to a power state that it can not transition to and the widget responds by setting PS-Error, this will not affect the PS-Error bit of the Function Group that the widget belongs to. If, however, a widget is indirectly requested to transition to a lower power dissipating state because its Function Group has been commanded to that state and the widget can not transition to that state, then the PS-Error bit of both the widget and the Function Group will be set and the power state of both will not change.

PS- ClkStopOk is reported when the codec is capable of continuing proper operation even when the clock has been stopped. This bit is applicable at the Function Group level and is reserved at the widget-level. It is required for the codec to support the Get Power State commands after being commanded to enter the D3 state and report the ability for operation with the clock stopped. Reporting this while in other Dx states is optional.
The bus clock should not stop at a time when ClkStopOk is reported as '0'. However, if the bus clock does stop, then a full reset shall be performed.

Strategies for using PS-Error and PS-ClkStopOk:

> There are some cases where there are power dependencies that are not understood by the host software. This occurs for example if there is some pass through operation while the system is in low power states. There are several strategies that may be used.
>
> The first strategy allows the codec to reject power state transition requests (reporting PS-Error set) thus inhibiting the codec or just that specific widget from going into D3 when there is a dependency that the host software is not

aware of. In that case, s/w will have to re-issue a Set Power State verb to have to codec (or widget) transition in to D3 state at a later time and check the PS-Error bit again at that time. This does not ease the software burden as it does not provide knowledge as to how long this condition will remain. Thus there is a requirement for software to repeatedly attempt to command the codec in to D3, until it succeeds.

The preferred strategy is for the codec or widget to accept the D3 transition request and transition into D3 state, assuming that it is capable of servicing targeted pass-through operations while in D3 state. Servicing a pass through loop may require that certain logic in the codec remain powered up and functional in D3 state, at least for certain periods of time. This logic must operate independently of the HD Audio bus or controller, may be dynamically power managed (e.g. powered on or off) transparently to the HD Audio bus (e.g. based on activity on the loop through), and must not require any interaction with system software. The only exception to that may be the HD Audio bus clock (BCLK): if the codec requires BCLK to be available in D3 state, while a pass through loop is active, then it must indicate so by clearing the PS-ClkStopOk bit before entering D3 state, otherwise it must set that bit. Note, there is a requirement for the host software to check the state of ClkStopOk just prior to actually stopping the clock. This creates a small window, but which is handled by the codec not starting any non host software aware operation within 200ms after reporting that it is ok to stop the clock

All Power State (PS) fields are defined as follows:

Value		General Definition	Active State (PS-Act)	Set State (PS-Set)
Bit 3 *Reserved*	**Bits 2:0**			
Reserved, always 0	**000**	**D0** fully on	Reports the actual power state of the node and must be the lower power state of the Function Group power state and this node's power state. Nodes that support power states not supported by the Function Group must go to the next lower power consuming state supported by the Function Group. During transition from a lower power to a higher power consuming state this field reports the lower power consuming state.	Always the value set in the last Power State command or if no Power State command has been received since Power On or a Function Group Reset will be the default power state, which may be any power state supported by the node, other than D3cold. There is no requirement to be Fully on after reset.
	001	**D1** allowing for some reduction but must return to D0 (Fully on) within 1 millisecond. Analog pass through circuits (e.g. CD analog playback) must remain fully on while in D1.		
	010	**D2** allows for (does not require) the lowest possible power consuming state from which it can return to the "fully on" state (D0) within 2 milliseconds. For modems, this is the "wake on ring" power state.		
	011	**D3 (**or **D3hot)** allows for (does not require) lowest possible power consuming state under software control, in which EPSS requirements can be met, if EPSS is supported. Note that any low power state set by software must retain sufficient operational capability to properly respond to subsequent software Power State commands. For any widgets that report EPSS of 1, they shall transition from D3 state to D0 state in less than 10 milliseconds. This is measured from the response to the Set Power State verb that caused the transition from D3 back to fully operational D0 state. This requirement must be met even if the Function Group or widget is in the process of transitioning in to a low power state, when it receives the Set Power State verb which commands it to transition back to D0 state. It is permissible for the audio fidelity for analog outputs to be slightly degraded if audio rendering begins immediately once the fully operational state is entered. However, audio fidelity must not be degraded 75ms after the transitioning to D0 state Note, if EPSS is not supported, then D3 state could potentially be identical to D3cold state		
	100	**D3cold** is an optional state which allows for (does not require) lowest possible power consuming state under software control. A Function Group shall complete its transition to D3cold within 200ms from being commanded in to D3cold, with the exception of the link interface which shall remain alive, to allow the Function Group to receive a Get Power State verb and report D3cold as the Active state. When all Function Groups have reported transitioning in to D3cold state, the codec link interface shall power down, the codec will no longer respond to further	D3cold is different than all other power states, in that while the codec (all Function Groups) is in D3cold, no further commands to the codec are	

Value		General Definition	Active State (PS-Act)	Set State (PS-Set)
Bit 3 *Reserved*	**Bits 2:0**			
		commands and power can be removed from the codec. No functionality (e.g. jack-detection) is required to be supported in this power state. A Function Group can NOT be commanded out of D3cold state with a Set Power State verb. An exit from D3cold state occurs in the following conditions: • Power On Reset • De-assertion of link reset (synchronous with a link clock transition). • A Function Group can be taken out of D3cold with a double Function Group reset. Note that a Function Group can be taken in to and out of D3cold even when no link reset or Power On reset occurs. Transition from this state back to D0 state must be complete within 200ms. Pops and clicks must be suppressed at -65dBFS or better on every transition to or from this state. D3cold state can only be commanded to the Function Group. Behavior of this command to nodes other than the Function group, to enter D3cold state, is vendor unique and not specified by this specification.	possible. The codec will enter D3cold state only after s/w has polled the last Function Group which was commanded into D3cold and it has reported that it has entered D3cold state.	

Table T1. Power State Field Definition

PS-SettingsReset is reported as set to one (1) when, during any low power state, the settings that were changed from the defaults have been reset to their default state. When settings have not been reset, this is reported as zero (0). The conditions that may reset settings to their defaults are:

1) Power On; always sets the PS-SettingsReset to one (1) for all widgets that report EPSS set to one (1) and that have host programmable settings and reset all settings.
2) Single Function Group Reset; sets PS-SettingsReset to one (1) for any widget that reports EPSS set to one (1) only if that widget's settings that should have been persisted were reset (changed) and follows Table T2.
3) Double Function Group Reset: sets PS-SettingsReset for all widgets that report EPSS set to one (1) and that have host programmable settings and resets all settings.
4) Link Reset; sets PS-SettingsReset to one (1) for any widget that reports EPSS set to one (1) only if that widget's settings that should have been persisted were reset (changed) and follows Table T2.
5) Clock stopped, causing dynamic logic to lose state, sets PS-SettingsReset to one (1) for any widget that reports EPSS set to one (1) for any setting that was changed.
6) Exit from D3cold always sets the PS-SettingsRest to one (1) for all widgets that report EPSS set to one (1) and that have host programmable settings, as power should have been removed to all these widgets by the codec logic.

The PS-SettingsReset bit for individual widgets, will be cleared to zero (0) on receipt of any "Set" verb to that widget; or After responding to a get Power State verb, to that widget, with the response containing PS-SettingsReset set to one (1).

The PS-SettingsReset bit for the Function Group is handled differently than at the widget level. For the Function Group the PS-SettingsReset is set to one (1) when any widget sets its PS-SettingsReset to one (1). The Function Group PS-SettingsReset bit is thus the logical "or" of all the EPSS bits, but is latched so that it can be reset independently and not require that all EPSS bits be reset.

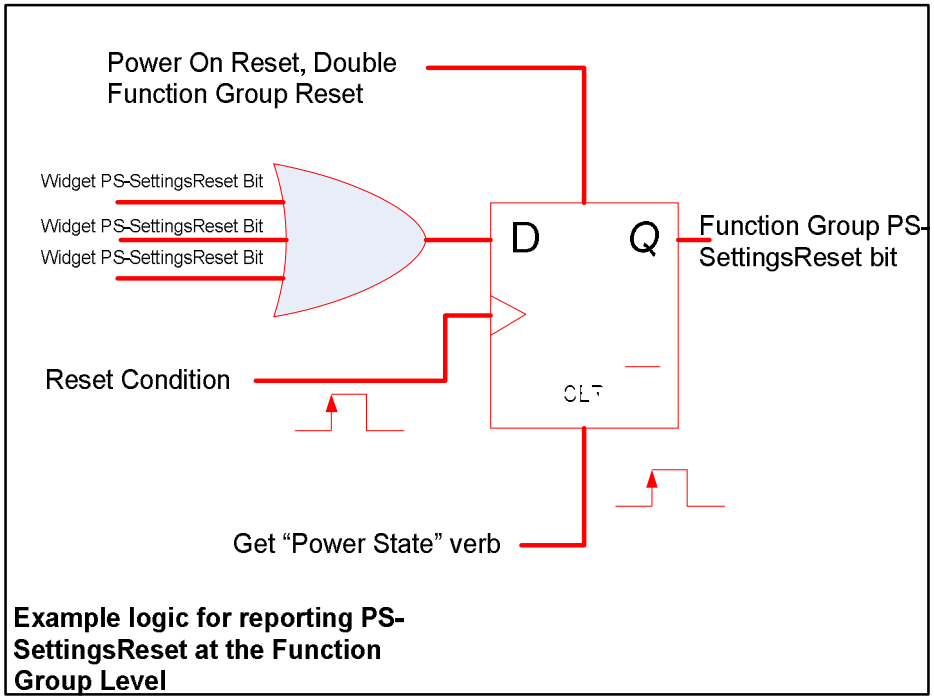


Figure F1. Power State Field Definition

The PS-SettingsReset bit is 'sticky'. Once set, it will retain its value until it's cleared by a 'Get' verb, regardless of other single or double Function Group resets, Dx state transitions etc that may occur in the meantime.

It is strongly desired that settings that host software has changed from defaults not change across any Dx state transition, function group and link resets. Although there is no requirement to persist settings across power state transitions, and resets, re-populating these values, may add undue latency to restarting audio streams after low power state exits and resets[4].

The following table outlines how the handling of setting persistence should be performed across Dx states, clock stopping and resets. For codecs (function group) and widgets that do not reported EPSS set (1) compliance to this table is not required. When EPSS is reported, the use of PS-SettingsReset to report that settings have been reset (changed) is required.

Whenever the following table refers to 'Function Group Reset' or 'Function Group Resets' it means 'single Function Group reset/resets', unless it explicitly states 'double Function Group reset/resets'.

Setting	Action across Dx state transitions or clock stopped	Action with Link or Function Group reset	Codec, Function Group or Widgets that it applies to
Codec physical address (SDI)	Persist across Dx states, unless the link has been reset, in which case the codec shall initiate a Codec Initialization sequence to acquire an address when the link re-initializes. Note that unless the codec has been moved to a different SDI line the	Persist across Single and double FG reset but Link Reset will initiate a Codec Initialization to acquire an address from the controller.	Codec

[4] Also note that, even though persisting codec parameters across power state transitions and resets is not a requirement of this specification, it is possible that some operating system vendors may require static register behavior and may not support the PS-SettingsReset bit

Setting	Action across Dx state transitions or clock stopped	Action with Link or Function Group reset	Codec, Function Group or Widgets that it applies to
	controller shall supply the same address.		
Converter Format; All bits [15:0] e.g. Type, Base, Mult, Div, Bits Chan fields	Persist across Dx states	Reset by POR, persist across Link & FG resets	Input & Output Converters, Digital Converter
Converter Stream & Channel settings, all bits [7:0] e.g. Stream number in bits [7:4] and Lowest Channel number in bits [3:0]	Reset to Default; must not assume same stream is in operation across Dx state transitions and could cause spurious audio to be played if not reset.	Reset to default by all resets and does not set PS-SettingsReset to one (1)	Input & Output Converter, Digital Converter
Digital Converter Controls 1 &2, all bits	Persist across Dx states	Reset by POR, persist across Link & FG resets	Digital Converter
Connection Select Index values, all bits [7:0]	Persist across Dx states	Reset by POR, persist across Link & FG resets	Input converter, Selector and Pin Complex
Coefficients	Vendor defined, but if reset, must report PS-SettingsReset set to 1	Vendor defined but if reset, must report PS-SettingsReset set to 1	All
Coefficient Index	Reset to default	Reset to default	Input Converter, Output Converter, Selector Widget, Pin Complex Widget, Other Widgets that have loadable processing coefficients
Proc State	Persist across Dx states	Reset by POR, persist across Link & FG resets	Input Converter, Output Converter, Selector Widget, Pin Complex Widget, Other Widgets
Amplifier Gain / Mute; “Amplifier Mute” and “Amplifier Gain” bits	Persist Index, Mute and Gain settings across Dx	Reset by POR, persist across Link & FG resets	All
Pin Widget Controls; enables, vRef and for digital Pin Widgets the Encoded stream type; “H-Phn Enable”, “Out Enable”, “In Enable”, and “VRefEn” bits	Persist across Dx states	Reset by POR, persist across Link & FG resets	Pin Complex
SDI Select, ” SDI-Select” bits	Persist across Dx states	Reset by POR, persist across Link & FG resets	Input Converters
Unsolicited Response control; Enable and Tag; “Enable” and “Tag” bits	Persist across Dx states	Reset to disabled by Power-On reset but persists across Link and FG resets	All capable of generating Unsolicited Responses
EAPD and BTL enable; LRSwap, EAPD & BTL	Persist across Dx states	Reset by POR, persist across Link & FG resets	Pin Complex
GPI/GPO Data, Enable Masks, Unsolicited Enable Masks, Sticky Masks, Direction, Wake Enable Masks	Vendor defined, but if reset must report PS-SettingsReset set to 1	Vendor defined and does not set PS-SettingsReset to 1 if settings are reset	Audio Function Group
Volume Knob widget’s volume register	Persist across Dx states, if volume control is relative	Reset by POR, persist across Link & FG resets if volume control is relative	Volume Knob
Volume knob direct bit	Persist across Dx states; a value of 0 is an	Reset by POR, persist across Link & FG resets	Volume Knob

Setting	Action across Dx state transitions or clock stopped	Action with Link or Function Group reset	Codec, Function Group or Widgets that it applies to
	unsolicited response enable and should generate unsolicited responses when the volume register changes, even while in D3 state		
Sub-System ID	Persist across Dx states	Reset by POR, persist across Link & FG resets. Note, this setting also persists across double FG resets	All Function Groups
Configuration Default; all 32 bits	Persist across Dx states	Reset by POR, persist across Link & FG resets. Note, this setting also persists across double FG resets	Pin Complex
Stripe Control	Persist across Dx states	Reset by POR, persist across Link & FG resets	Output converter, Digital Converter
Channel Converter Count; channels and the channel multiplier	Persist across Dx states	Reset by POR, persist across Link & FG resets	Digital Converters
Pin Sense	Update to reflect proper state after transition back to full operation (D0)	Update to reflect proper state and save any Unsolicited Response that has not been sent and sent it after first verb is received	Pin Complex
HDMI ELD Data (specifically the memory contents)	Vendor defined and does not cause PS-SettingsReset to be set to 1	Reset by POR, persist across Link & FG resets	HDMI Pin Complex
HDMI DIP Size	Persist across Dx states	Reset by POR, persist across Link & FG resets	HDMI Pin Complex
HDMI DIP Index	Persist across Dx states	Reset by POR, persist across Link & FG resets	HDMI Pin Complex
HDMI DIP Data	Persist across Dx states	Reset by POR, persist across Link & FG resets	HDMI Pin Complex
HDMI DIP XmitCtrl	Persist across Dx states; Causes Info Frames to be transmitted, if enabled, immediately upon returning to D0	Reset by POR, persist across Link & FG resets	HDMI Pin Complex
All sub-tags for Unsolicited Response enables; includes Content Protection Control & SLIC off hook wake	Persist across Dx states	Reset to default state by all resets; any responses that have not been sent shall not be lost and sent after the first verb received.	HDMI Pin Complex
Channel to Converter Channel mapping	Persist across Dx states	Reset by POR, persist across Link & FG resets	Digital Pin Complexes
Power State for the function group and individual widgets	The PS-Set field of the power state should persist across Dx states, except for the node which was specifically commanded to a new power state	Vendor defined; preference is for POR to go to D3 and for Link and Function Group resets not to change the power state	Function Group and Widgets capable of granular power management

Table T2. Persisted Settings across Resets and power states

The PS-SettingsReset bit must be set to one (1) if any of the settings that "should be persisted" listed in table T2 are reset. For settings not listed, the action is vendor defined and should be assumed by host software that the settings have been changed.

The PS-SettingsReset can be reported at the individual widget level or at the Function group level, depending on whether EPSS is supported at the widget level or the Function Group level. When it is reported at the Function Group level, PS-SettingsReset must be the "or" of all individual widget's PS-SettingsReset state. This allows a simple poll by the host software to detect when some settings have been reset/changed.

While Function Group nodes (Audio Function, Modem Function, etc.) and Power Widget nodes must support this control, other widget nodes may optionally implement this control to provide more fine-grained power management of the codec. If the control is supported, the node must report this by returning a 1 for the Power Cntrl (Bit 10) in the Audio Widget Capabilities response data (see Section 7.3.4.6).

Power state changes at the Function Group and Pin Widgets have some special hardware and software requirements when Extended Power States Support is reported:

(a) Pin Complex Widgets that are programmed to generate Unsolicited Responses for Presence Detection, on/off-hook state change or ring detection must continue to function in all power states. Thus when an unsolicited response is required as a result of a plug or an on/off-hook event, the codec must request a power state change, which may include performing a Codec Initialization (as defined in 5.5.3) to bring the link out of a low power state. The software must recognize the unsolicited response for the event, when the codec was in a low power state as a power state change request and immediately send a command to return the codec to Fully Powered (D0).

(b) When generating an Unsolicited Response for a plug or on/off-hook or ring detection event when the link is in a low power state (clock is not running) sending of the Unsolicited Response must wait until after the first verb is received to prevent the response from being lost due to software transition to active power state.

(c) Function groups that have the capability to pass input stream directly to an output (aka monitoring) must not interrupt that stream when entering into low power states.

Applies to:

(a) Audio Function Group or Widgets in the Function Group, if EPSS (Extended Power States Support) is reported in the Supported Power States response for the Function Group or its Widgets. Note, if EPSS is supported at the Audio Function Group level, widgets in the Function Group are not required to report the PS-SettingsReset, PS-ClockStopOk and PS-Error bits in their response to a Get Power State verb

(b) Modem Function Group

(c) Other Function Group

(d) Power Widget

(e) Input Converter, Conditional based on Audio Widget Capability (Power Cntrl) reported, and required if EPSS (Extended Power State Support) is reported in the Supported Power States response.

(f) Output Converter, Conditional based on Audio Widget Capability (Power Cntrl) reported, and required if EPSS (Extended Power State Support) is reported in the Supported Power States response.

(g) Selector Widget, Conditional based on Audio Widget Capability (Power Cntrl) reported, and required if EPSS (Extended Power State Support) is reported in the Supported Power States response.

(h) Mixer Widget, Conditional based on Audio Widget Capability (Power Cntrl) reported, and required if EPSS (Extended Power State Support) is reported in the Supported Power States response.

(i) Pin Complex, Conditional based on Audio Widget Capability (Power Cntrl) reported, and required if EPSS (Extended Power State Support) is reported in the Supported Power States response.

(j) Digital Pin Widgets such as for HDMI, Conditional based on Audio Widget Capability (Power Cntrl) reported

• • •

7.3.3.13 Pin Widget Control

Pin Widget Control controls several aspects of the Pin Widget.

Command Options:

Table 8. Enable VRef

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F07h	0	Bits 31:8 are 0 Bits 7:0 are PinCntl
Set	707h	Bits 7:0 are PinCntl	0

PinCntl format:

7	6	5	4:3	2:0
H-Phn Enable	Out Enable	In Enable	Rsvd	VRefEn

Figure 4. PinCntl Format

H-Phn Enable disables/enables a low impedance amplifier associated with the output. The value 1 enables the amp. Enabling a non-existent amp is ignored.

Out Enable allows the output path of the Pin Widget to be shut off. The value 1 enables the path. Enabling a non-existent amp is ignored. Although the Output enable could be used to lower the power usage of the output, this is not the intent. The use of Widget or Function Group power states must be the only method for lowering the power use. Once setting Out Enable to one (1) the output must instantaneously be able to produce full scale and fidelity output. In addition all power state transition timing that requires outputs to be at full fidelity within 75 milliseconds, shall not be required if Out Enable is not set to one (1) prior to the low power transition command. Timing for full scale and fidelity output if the Out Enable is changed from a zero (0) to a one (1) within the 85 millisecond time window after the widget or function group has been commanded to return to full power (D0) is vendor specified and indeterminate.

The output being enabled is also required for looping functionality such as PC Beep to operate and produce sound on the output of the Pin Widget. If the output is not enabled, then PC Beep and other looping operations will not produce any output. Thus the Out Enable must be set to one (1) when the widget or function group is commanded into a lower power state to allow the output to pop up to a higher power state and produce output.

In Enable allows the input path of the Pin Widget to be shut off. The value 1 enables the path.

VRefEn: Voltage Reference Enable controls the VRef signal(s) associated with the Pin Widget. If more than one of the bits in the VRef[7:0] field of the Pin Capabilities parameter (Section 7.3.4.9) are non-zero, then this control allows the signal level to be selected.

The VRefEn field encoding selects one of the possible states for the VRef signal(s). If the value written to this control does not correspond to a supported value as defined in the Pin Capabilities parameter, the control must either retain the previous value or take the value of 000, which will put the control in a Hi-Z state and prevent damage to any attached components. Table 2 enumerates the possible values for VRefEn which correlate to the values identified in the Pin Capabilities parameter (see Figure 77).

Table 9. VRefEn Values

VRefEn Encoding	VREF Signal Level
000b	Hi-Z
001b	50%
010b	Ground (0 V)
011b	*Reserved*
100b	80%
101b	100%
110b-111b	*Reserved*

Applies to:

- Pin Complex

• • •

7.3.3.16 EAPD/BTL Enable

EAPD/BTL Enable controls the EAPD pin and configures Pin Widgets into balanced output mode, when these features are supported. It also configures any widget to swap L and R channels when this feature is supported. When this control is referenced to a non-Pin Widget, bits 1 and 0 are not valid, and are considered reserved.

Command Options:

Table 10. EAPD/BTL Enable

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F0Ch	0	bits 31:3 are *Reserved* bit 2 = L-R Swap bit 1 = EAPD bit 0 = BTL
Set	70Ch	bits 7:3 are *Reserved* bit 2 = L-R Swap bit 1 is EAPD bit 0 is BTL	0

L-R Swap causes the left and right channels of the Widget to be swapped for both input and output paths if they exist. The value 1 enables swapping.

EAPD value is reflected on the EAPD hardware signal / pin that is used to control an amplifier. This amplifier may exist either external to a codec or can be integrated; writing a 1 to the EAPD bit causes the amplifier to power up, and a writing a 0 causes it to power down. The EAPD bit is the equivalent of a power state control for the amplifier but that allows for only D0 and D3 power states. The EAPD register bit value of 0 is equivalent to D3 and a value of 1 is equivalent to D0. Just like the function group and widget power states, the amplifier power state (level of EAPD Hardware signal / pin) should generally be the lower of the Function Group power state, Widget power state and the value specified by EAPD. Thus when the EAPD register bit value is 1, the EAPD hardware signal / pin would be placed in a state appropriate to the current power state of the associated Pin Widget. The external amplifier would be powered down whenever the associated Pin Widget is put into D3, even though the EAPD register bit value would remain set to 1.

As it is expected that the codec would normally rest in a low power state a challenge arises for looping functionality, such as for PC Beep if the amplifier is also placed into a low power state. The preferred methodology is that the EAPD hardware signal be set to an appropriate level to power down the amplifier when the function group or widget is placed in a low power state and that the level of the hardware signal / pin change dynamically to allow the amplifier to be powered up while the looping function is in effect. This is a dynamic or temporary pop-up of the amplifier power state.

The time required to pop-up the amplifier to an operating state shall not cause the starting portion of looping audio (e.g. PC Beep) to be lost, either by delaying the looping audio signal or by bringing the amplifier up quickly. Although this specification does not specify the maximum time, it is recommended that no more than 85 milliseconds is used to bring the amplifier up and reach 100 % fidelity on the audio output or for delaying the looping audio.

An alternate permissible, but non-preferred solution would be that the EAPD hardware signal remains set at a level where the amplifier remains powered up even when the function group or widget is placed in a low power state. This would simplify the codec design but would lead to un-necessary power dissipation on the amplifier, when the audio subsystem (including hardware loops) is completely inactive.

It is possible that more than one Pin Widget supports the EAPD function as indicated in bit 16 of the Pin Capabilities Parameter (Section 7.3.4.9); this would be true, for example, when external amps were supported for 4-channel output. In this case, each supporting Pin Widget must respond to this control; however, since there is only a single EAPD Pin, there is also only one logical value to set/get, and that value must be accessible, using this control, via any/all supporting Pin Widgets. In this case the level of the EAPD hardware signal / pin must be the higher of the duplicate EAPD bits. This will keep the amplifier on while any of the EAPD bits requires its amplifier to be on.

BTL controls the output configuration of a Pin Widget which has indicated support for balanced I/O (bit 6, Pin Capabilities Parameter). When this bit is 0, the output drivers are configured in normal, single-ended mode; when this bit is 1, they are configured in balanced mode. Note that in balanced mode, the Pin Widget has twice as many pins as it does in normal mode; i.e., a stereo Pin Widget in balanced mode has four signal pins (in addition to Vref pins). However, in both modes it must appear to software as a single Pin Widget. The additional pins must be reserved to this purpose; thus, in a configuration supporting BTL outputs the additional pins may not be enumerated as a separate Pin Widget.

Applies to:

- Any Audio Widget

• • •

7.3.3.29 Volume Knob

Volume Knob provides the controls for an optional external hardware volume control.

Command Options:

Table 11. Volume Knob Control

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F0Fh	0	Bit 7 is Direct Bits 6:0 is Volume
Set	70Fh	Bit 7 is Direct Bits 6:0 is Volume	0

Direct causes the Volume Control Widget to directly control the hardware volume of the slave amplifiers. If "Direct" is set to a 0, the volume control will not directly affect the volume of the slaves amplifiers; rather, the

software receives an unsolicited response, reads the volume control, and then programs the appropriate amplifiers correctly. If the unsolicited responses are enabled for the Volume Knob widget and the Direct bit is set to 0, then unsolicited responses will be generated while in D0 through D3 states. If the EPSS and PS-ClkStopOk bits are set, the codec will generate an unsolicited response in D3 state even when the HD Audio link clock has stopped.

Volume is specified in steps, as is amplifier gain. If two amplifiers slaved to the Volume Knob control have different "StepSize" parameters, they are both adjusted by the same number of steps, implying a differing total dB treatment. If the Volume Knob control has more steps than a slave amplifier is capable of supporting (as indicated in the Volume Knob Capabilities parameter), the amplifier remains at its limiting value.

Note, the Volume Knob should continue to operate in D3 state (e.g. to support a loop through which might be active). Software will have to re-read the value of the Volume Knob register after it exits a low power state, if the codec does not generate unsolicited responses.

Applies to:

- Volume Knob Widget

• • •

7.3.3.33 Function Reset

The **Function Reset** command causes the functional unit, and all widgets associated with the functional unit, to return to their power-on reset values. Note that some controls such as the Configuration Default controls should not be reset with this command. It is also possible that certain other controls, such as Caller-ID, should not be reset.

This command does not affect the Link interface logic, which must be reset with the link **RST#** signal. Therefore, a codec must not initiate a Status Change request on the link.

When a codec receives the Function reset verb, the expected behavior is that the codec will issue a response to the verb to acknowledge receipt, and then reset the affected Function Group controls. The codec must be ready to respond to the verbs on the Link frame after the frame on which it returns its response to the Reset command.

Command Options:

Table108. Function Reset

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Execute	7FFh	0	0

For codecs that report Extended Power State Support (EPSS) set to one (1), either at the Function Group level or for any widget, the Reset functionality changes and a new reset type is required. When EPSS is set, and a Function Group Reset is received, settings that can be changed by host software are NOT initialized i.e. settings are persisted across the reset. In order to allow host software to guarantee that a full initialization has occurred, a new reset functionality is defined and support for this new reset is required. This new reset is created by sending two Function Group resets, potentially separated by an undefined number of idle frames, but no other valid commands. This Function Group "Double" reset shall do a full initialization and reset most settings to their power on defaults.. A few exceptions apply, such as:

- Sub-System ID
- Configuration Defaults

Note, when a Function Reset is received, it shall be decoded and executed as a single Function Reset. If another valid command is subsequently received (possibly separated by idle frames from the last Function Reset), then:

- If the new command is a second Function Reset, it will cause a full reset of the Function Group. Any memory of the two received Function Resets shall be erased at that point.
- If the new command is not a Function Reset, it will be executed normally. Any memory of the last single Function Reset will be erased at that point.

If a single Function Reset is received (followed by zero or more idle frames) and a link reset occurs, the link reset shall erase any memory of the last Function Reset.

Applies to:

(a) Audio Function Group
(b) Modem Function Group
(c) Other Function Group

• • •

7.3.4.6 Audio Widget Capabilities

The Audio Capabilities control returns a set of bit fields describing the audio capabilities of the widget.
Parameter ID: 09h
Response Format:

31:24	23:20	19:16	15:13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	Type	Delay	Chan count ext	CP caps	L-R Swap	Power Cntrl	Digital	Conn List	Unsol Cap-able	Proc Widget	Stripe	Format Override	Amp Param Over-ride	Out Amp Present	In Amp Present	Chan count LSB (stereo)

Figure 73. Audio Widget Capabilities Response Format

Table 118. Widget Type

Value	Type
0h	Audio Output
1h	Audio Input
2h	Audio Mixer
3h	Audio Selector
4h	Pin Complex; includes analog, digital and HDMI variants
5h	Power Widget
6h	Volume Knob Widget[5]
7h	Beep Generator Widget[6]
8h-Eh	*Reserved*

[5] In the case of the Volume Knob Widget, none of the parameter bits [9:0] or [19:11] are used and may be omitted or set to 0. However, software assumes the capability of unsolicited responses and a connection list, as these are required by this widget type.
[6] In the case of the Beep Generator Widget, the only meaningful parameter bits are 2 ("Out Amp Present"), 3 ("Amp Param Override") and 10 ("Power Cntrl"). None of the other parameter bits are used and may be omitted or set to 0.

Fh	Vendor defined audio widget

Any vendor defined widget that is enumerated hierarchically within an Audio Function Group must be identified as a vendor defined type (Fh) using this parameter.

Delay indicates the number of sample delays through the widget. This may be 0 if the delay value in the Audio Function Parameters is supplied to represent the entire path.

Chan count ext and Chan count LSB together these 4 bits specify the number of channels that the widget supports. The value contained in the 4 bit field is split with the 3 most significant bits contained in bits 15:13 and the least significant bit in bit 0. These bits combined form the channel count supported minus (-) 1. So if two channels (stereo) are supported then the value would be – bits 15:13=000, bit 0=1. For 8 channels the value would be – bits 15:13=011, bit 0=1.

CP Caps indicates that the widget supports "Content Protection". No indication of the type of protection is implied by this, but does require that the Copy Protection Control verb be supported. This capability is only meaningful for pin widgets.

L-R Swap indicates the capability of swapping the left and right channels through the Audio Widget. If the Audio Widget is both input and output capable (e.g., Pin Widget), then swapping must be supported for both input and output paths. Default (0) is no swap capability.

PowerCntrl indicates that the Power State control is supported on this widget. This allows finer grained power management than just at the Function Group level for widgets which support it. The power states supported is reported by the Supported Power States parameter (see 7.3.4.12 Supported Power States). In cases where this parameter is not supported the widget supports the same power states as the function group.

When the Widget reporting that it supports "Power Cntrl" by setting bit 10 and if the EPSS is also set in the Supported Power States response for the Audio Function group or for this Widget, the following additional capabilities are required:

1) The output associated with this Pin Widget does not generate spurious or anomalous sound output (aka pops and clicks) during any power state changes. The codec should not count on any amplifiers being muted or attenuated in order to achieve pop/click suppression. This is required if this output is analog such as for headphone, speaker jacks or other analog audio outputs. If this output is associated with the EAPD (External Amplifier Power Down) then power state transitions are assumed to activate the EAPD functionality, even if the software has not programmed this state. The definition of "Spurious" or "Anomalous" sounds is that the output does not incur a voltage change of more than -65dBFS relative to the voltage prior to and post any power state change.
2) Jack Presence state change or on/off hook or ring detection reporting, if enabled, to operate as specified regardless of the power state of the Pin Widget and Codec.
3) Jack presence state change or on/off hook or ring detection reporting, if enabled, must operate even if the link clock is not running (Controller is in low power state) if the CLKSTOP bit is also set in the Supported Power States response for this widget. Also it is required that the codec be capable of system wake before sending of unsolicited responses.
4) Any looping functionality (excluding input monitoring during recording or other functionality which is visible to software), provided that it is available in D0, must also be available in D1, D2 and D3. For example, audio render from side-show device during S3.

Digital indicates that a widget supports a digital stream. If the bit is a 1, it is a digital widget. For an Input or Output converter, for instance, this means the widget is translating between the High Definition Audio Link and a digital format such as S/P-DIF or I2S rather than analog data.

ConnList indicates whether a connection list is present on the widget. If the bit is a 1, the Connection List Length parameter and the Connection List Entry controls should be queried to discover the input connections. This bit must be a 1 for Input Converters, Sum Widgets, and Selector Widgets. The bit may be a 0 for Output Converters if the only connection for the widget is to the High Definition Audio Link.

If **Unsol Capable** is a 1, the audio widget supports unsolicited responses. The Unsolicited Response command can be used to configure and enable Unsolicited Response generation. When this parameter is associated with a Pin Widget, then

setting this bit requires that the Pin Widget generate an unsolicited response (when enabled) whenever the "Presence Detect" bit (see Section 7.3.3.15) changes state.

If **ProcWidget** is a 1, the "Processing Controls" parameter should be queried for more information about the widget's processing controls.

The **Stripe** bit defines whether the Audio Output Converter Widget supports striping, as defined in (Section TO DO). If Stripe is a 1, the Audio Output Converter Widget must support the Stripe Control verb. Stripe is only defined for Audio Output Converter Widgets; for all other widget types, this bit must be 0.

If **Format Override** is a 1, the widget contains format information, and the "Supported Formats" and "Supported PCM Bits, Rates" should be queried for the widget's format capabilities. If this bit is a 0, then the Audio Function node must contain default amplifier parameters, and that node's format related parameters should be queried to determine the format parameters. This bit is not applicable to, and is always 0 for, Pin Complex Widgets.

If **Amp Param Override** is a 1, the widget contains its own amplifier parameters. If this bit is a 0, then the Audio Function node must contain default amplifier parameters, and they should be used to define all amplifier parameters (both input and output) in this widget.

If **(In|Out) AmpPresent** is a 1, the widget contains an input or output amplifier, as indicated. The Amp Param Override bit should be examined to determine whether the widget contains default amplifier parameters or has amplifier parameters that need to be explicitly queried. The "In Amp Present" bit is only relevant for Sum Widgets, Input Converters, and Pin Complexes. The "Out Amp Present" bit is only relevant for Selector Widgets, Sum Widgets, Output Converter Widgets, and Pin Complex Widgets.

The **Stereo** bit determines if the widget is a stereo or mono widget. If the "Stereo" bit is a 1, the widget is a stereo widget.

Applies to:
- Input Converter Widget
- Output Converter Widget
- Selector Widget
- Mixer Widget
- Pin Widget

• • •

7.3.4.12 Supported Power States

Returns a bit field describing the power states supported by the functional unit and widgets. Support for this parameter is required for the Function Group and for a Power Widget if implemented. Although this parameter is optional for any other node, if a node implements a Power State Control, then it is recommended that the node also support the Supported Power States parameter. If this is not implemented (returns 0's) or just returns 0 as response to reading this parameter for a node that supports a Power State Control (See 7.3.3.10) then the supported power states for that node will be the same as reported for the Function Group.

Parameter ID: 0Fh
Response Format:

31	30	29	28-5	4	3	2	1	0
Extended Power States Supported (EPSS)	CLKSTOP	S3D3coldSup	Reserved	D3coldSup	D3Sup	D2Sup	D1Sup	D0Sup

Figure 80. Supported Power States Response Format

D0Sup indicates that the Widget or Function Group supports D0 operation. This is required for any widget that supports the Supported Power State Verb.

D1Sup indicates that the Widget or Function Group supports D1 operation. This is an optional power state. If supported then the maximum exit time back to fully functional is 1 millisecond.

D2Sup indicates that the Widget or Function Group supports D2 operation. This is an optional power state. If supported then the maximum exit time back to fully functional is 2 milliseconds.

D3Sup indicates that the Widget or Function Group supports D3 operation (also called D3hot). This is required for any widget that supports the Supported Power State Verb. If supported and Extended Power States Supported is also reported (set to 1) then the maximum exit time back to fully functional is 10 milliseconds. This is measured from the response to the Set Power State verb that caused the transition from D3 back to fully operational D0 state.

D3coldSup indicates that the Function Group supports D3cold operation. This state is only supported at the Function Group level. This is an optional power state. If supported then the maximum exit time back to fully functional is 200ms.

After all codecs on the HD Audio link have been placed in D3 (D3hot) or D3cold state, the bus driver can optionally also reset the HD Audio link and stop the link clock (BCLK). That will enable the HD Audio Controller to turn off upstream clocking resources, effectively bringing itself into a low power state.

S3D3coldSup: this bit is intended to report the state the codec should be placed in, when the platform goes to suspend (S3). This bit is meaningful only when the D3coldSup bit indicates that D3cold state is supported, otherwise this bit is reserved. If this bit is set to '1', then software should place the codec in D3cold state, when the platform is entering S3 state, otherwise it will be placed in D3 (i.e. D3hot) state. This bit is defined only for the Function Group and it is vendor-specific for other nodes.

CLKSTOP bit is defined only at the Function Group only (not at the widget level) and indicates that the Function Group and all widgets under it support D3 operation even when there is no BitCLK present on the Link. This is an optional power state, but is strongly recommended for any codec that will be used in low power environments. If supported then the maximum exit time back to fully functional is 10 milliseconds from the time that the clock begins operation and a codec address cycle has been completed. This capability extends the required functionality for D3 support while the link is operational to include:

1) Reporting of presence detect or on/off hook state changes or ring detection, if enabled and supported by the pin widget, even if the Link Clock is not running (controller low power state) or is currently in Reset.
2) Presence or on/off hook state changes or ring detection occurring during Link Reset must be deferred until after the reset sequence has completed. Any Unsolicited Responses, if enabled and supported, must not be lost because the Link Clock stops or if Link Resets are generated before the Unsolicited Response for the state change has been returned to the host.
3) Reporting of ClkStopOk when stopping of the clock would be permitted. The CLKSTOP is a static capability with ClkStopOk a dynamic reporting. The Setting the capability CLKSTOP to one (1) and not allowing the clock to stop by not reporting ClkStopOk is not permissible. Unless there is a condition or dependency that the host

software cannot be made aware of, that would prohibit stopping the clock, the ClkStopOk shall be reported as set (1). It is expected that host software will poll the ClkStopOk before stopping the clock if the CLKSTOP is reported at one (1).

The bus clock should never stop, if CLKSTOP is reported as '0'. However, if the bus clock does stop (while the Function Group is in any power state, D0 through D3), then a full reset shall be performed.

EPSS indicates that the Widget or Function Group supports additional capabilities allowing better low power operation. The following are the additional capabilities required when EPSS is set. There are two basic approaches for supporting additional low power capabilities.

First is to report EPSS support at the Function group level. This enables low power operation for all Widgets and thus the following are then required for "**applicable Widgets**", which are converters, mixers and any pin widgets that are capable of reporting presence detection, on/off hook or ring detection and have analog input or outputs (e.g. headphone, line in, line out, microphone input and line input)..

1) "Applicable" widgets in the Function Group must enable the Codec to meet the capabilities described below. These widgets may, but are not required to, report PowerCntrl and EPSS set to 1 (if they don't, they are still implied to have PowerCntrl or EPSS set to 1, since their Function Group has PowerCntrl and EPSS set to 1). These widgets are also required to support the Power State verbs, which can be used to get/set the widget power states, but are not required to report the PS-SettingsReset, PS-ClockStopOk and PS-Error bits in their response to a Get Power State verb.
2) Requires that Codec does not generate spurious or anomalous sound output on any analog outputs such as headphones and speaker jacks during any power state changes. The codec should not count on any amplifiers being muted or attenuated in order to achieve pop/click suppression. The definition of "Spurious" or "Anomalous" sounds is that the output does not incur a voltage change of more than -65dBFS relative to the voltage prior to and post any power state change.
3) Requires Jack Presence or on/off hook state change or ring detection reporting of any Pin Widget capable of reporting of these state changes to operate regardless of the Widget and Function Group power state. Reporting of these state changes when the link clock is not operational is also required if the Function Group also reports CLKSTOP capability (set to 1) in its Supported Power States response.
4) Requires system wake and reporting of presence, even if the Link clock is not running (Controller low power state) if CLKSTOP support is also reported (set to 1) by the Supported Power States for the Function Group.
5) Specifies time required to exit D3 state back to fully on D0 state must not exceed 10 milliseconds as measured from the when the response to the verb that caused a transition from D3 back to fully operational D0 is generated
6) Follows the rules for settings persistence outlined in Table T2 for all widgets in the codec

Second approach is to report EPSS support at the widget level for just the Pin Widgets and Converter Widgets that will be capable of fully operating in low power states. The following when then apply:

1) Requires granular power management and reporting of PowerCntrl on the widgets that report EPSS set.
2) Require that outputs from Pin Widgets reporting with EPSS capability (set to 1), do not generate any spurious or anomalous sounds during any supported power state changes. The definition of "Spurious" or "Anomalous" sounds is that the output does not incur a voltage change of more than -65dBFS relative to the voltage prior to and post any power state change.
3) Requires Jack Presence or on/off hook state change or ring detection reporting, if the Pin Widget is capable of reporting of these state changes, to operate regardless of the Widget and Function Group power state. Reporting of these state change when the link clock is not operational is also required if the Function Group also reports CLKSTOP capability (set to 1) in its Supported Power States response (note, the Function Group may report CLKSTOP capability, even if it reports its EPSS bit as '0').
4) Specifies time required to exit D3 state back to fully on D0 state for the widgets reporting EPSS capability (set to 1) does not exceed 10 milliseconds as measured from the when the response to the verb that caused a transition from D3 back to fully operational D0 is generated.
5) Requires system wake and reporting of presence, on/off hook or ring detection, even if the Link clock is not running (Controller low power state) if CLKSTOP support is also reported (set to 1) by the Supported Power

States for the Function Group CLKSTOP in its Supported Power States response.

6) Supported Power States command (Verb) is required for all widgets that report PowerCntrl bit set to 1 in their Audio Widget Capabilities response. Widgets that would report EPSS of 1, but not PowerCntrl of 1 is not permitted.
7) Follows the rules for settings persistence outlined in Table T2, for the widget reporting EPSS of one (1).

Note that a codec is considered EPSS compliant regardless of whether it support EPPS at the Function Group or at the widget level, as long as it supports one of these two approaches, as described above.

In either case when EPSS is reported there are some additional requirements:

1) Functionality where there are dependencies between nodes, these dependencies must not cause unexpected results when one node of the dependency is placed into D3 state. For example if there is logic to allow audio to be routed directly from inputs to outputs during low power states, this must not be affected when the output (pin complex) or the input (pin complex) or both are placed into D3. A further complication arises as once all the nodes in the codec are in D3 state the controller may also be placed into D3 and the clock maybe stopped. In this case, any audio that is not specifically being controlled by the host must continue to operate. If this is not possible as there is a dependency on the clock being operational during this state, then the function group must report ClkStopOK cleared (0), thus prohibiting the clock from being stopped. This should only be done when absolutely required and should transition back to the state where the clock may be stopped as soon as possible. It is recommended that the codec reporting the capability to operate without a clock in D3, should always allow the clock to stop and provide its own clock when necessary

Applies to:

(a) Audio Function
(b) Modem Function
(c) Other Function Groups (optional)
(d) Power Widget
(e) Pin Complex Widget
(f) Input Converter
(g) Output Converter
(h) Mixer
(i) Other Widgets (optional)

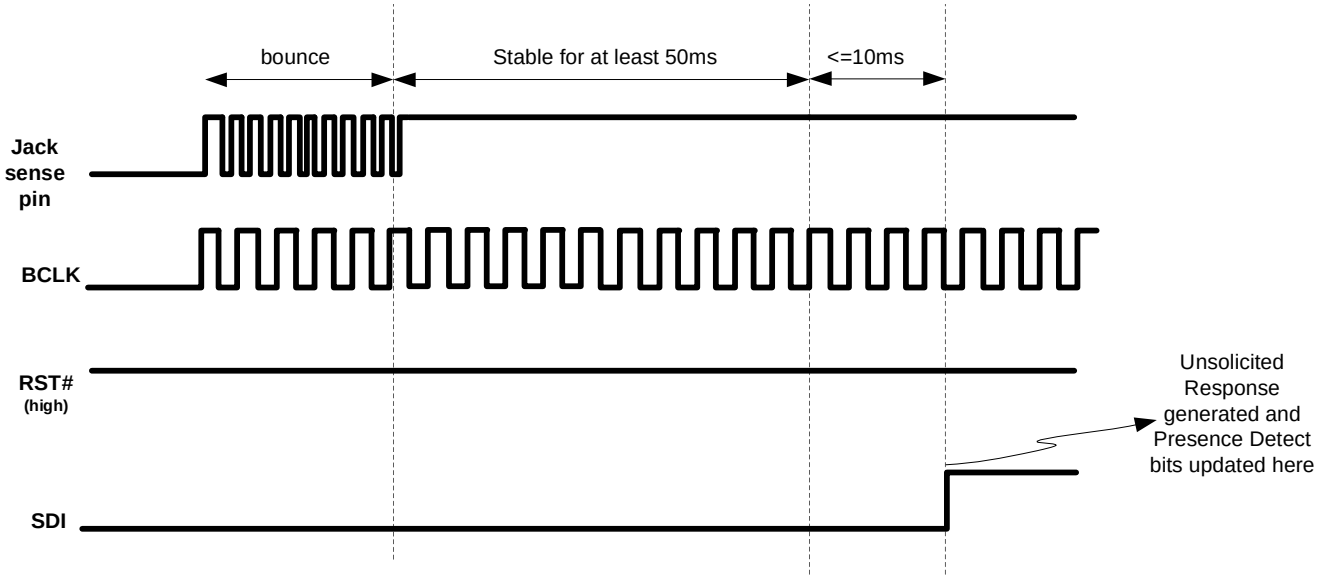
7.4.2 Audio Jack Detection Circuits

[following text added at the end of existing paragraph 7.4.2]

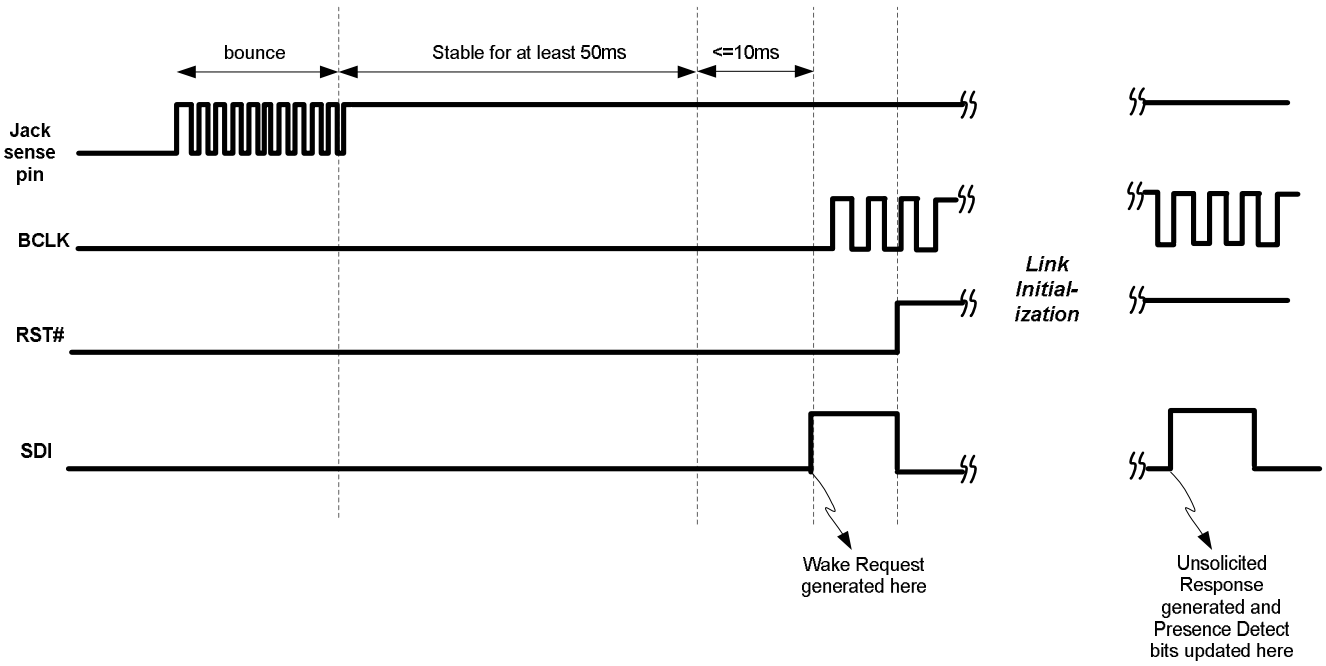
When detecting the insertion or removal of a jack, where the impedance of a shared sense line is being used, the codec shall measure the impedance of the jack's presence detect precision resistors continuously to determine when to report a change of state. Reporting of state change and change in the presence detect state bits shall not occur until any impedance (does not preclude other measurement techniques) change has initially stabilized for at least 50 Milliseconds. From the point at which the impedance has stabilized the codec shall report an Unsolicited Response, if enabled and the High Definition Audio Link clock is running, within 10 Milliseconds. If this clock is not running, then the request to wake the Link shall occur within 10 Milliseconds. Thus any presence detection logic used to detect which resistors are switched in for the purposes of Presence Detection, must operate more quickly than 10 Milliseconds. Once the unplug or plug event has been signaled to the host through the unsolicited response, another event or change of the presence detection bits shall not be generated unless the opposite jack state has been sensed (detected) continuously for at least 50 Milliseconds. The state of the Presence Detect bits for all the jacks associated with a shared sense line shall not change until the point where an Unsolicited Response could be generated, if disabled,

or is generated when enabled. Thus the state of the Presence Detection bits should be “de-bounced” with hysteresis of at least 50 Milliseconds, but longer times are permissible as long as the initial state change and reporting time is met. When the codec has returned to D0 from any lower power state, the state of the presence detection bits must be correct. If the codec power has been removed and the state of the presence detection bits has been reset, the codec shall report this by setting the PS-SettingsReset bit for the affected Pin Widget(s).
The timing specifications described above are demonstrated in the following diagrams:

Link clock is running



Link clock is NOT running



Intel® High Definition Audio Specification Document Change Notification