

Intel® High Definition Audio Specification

Document Change Notification

Date: June 8, 2012
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Change Identification: **DCN No: HDA033-A**
Change Revision: 1.0
Document Revision: Intel® High Definition Audio 1.0a

This document discloses changes to the Intel® High Definition Audio Specification and all information contained herein is provided under the terms of the "AZALIA" SPECIFICATION DEVELOPMENT AGREEMENT" also known as Intel® High Definition Audio Specification Developer Agreement, and all the terms of such agreement, including the confidentiality provisions, shall apply to this disclosure.

Title: RUN Bit Clear Time Clarification

Brief description of the functional changes:

This DCN relaxes the time-out period requirement for RUN bit clear.

Definition Text Formatting:

xxx Original text in existing specification or DCN released earlier.
yyy New text inserted by this new DCN.
zzz Deleted text introduced by this new DCN.

New Definitions:

4.5.4 Stopping Streams

To stop a stream, the software writes a 0 to the RUN bit in the Stream Descriptor. The RUN bit will not immediately transition to a 0. Rather, the DMA engine will continue receiving or transmitting data normally for the rest of the current frame but will stop receiving or transmitting data at the beginning of the next frame. When the DMA transfer has stopped and the hardware has idled, the RUN bit will then be read as 0. The run bit ~~should~~ typically transition from a 1 to a 0 within 40 μ s, however, it may take longer in some systems with heavy workload. If time-out is to be implemented in software for waiting the RUN bit to be cleared, it is recommended to be a minimum of 10 ms.