Intel® 875P Chipset Customer Reference Board Schematics

For use with the Intel® 875P Chipset Platform Design Guide

July 2003

Document Number: 252812-002

Revision History

Rev. No.	Description	Rev. Date
-001	Initial Release.	April 2003
-002	Change VR for compliance with Prescott FMB	July 2003

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PAGE #	COMPONENT/FUNCTION
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NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

POWER SYMBOLS USED:

VCC3
VCC
+12V
-12V

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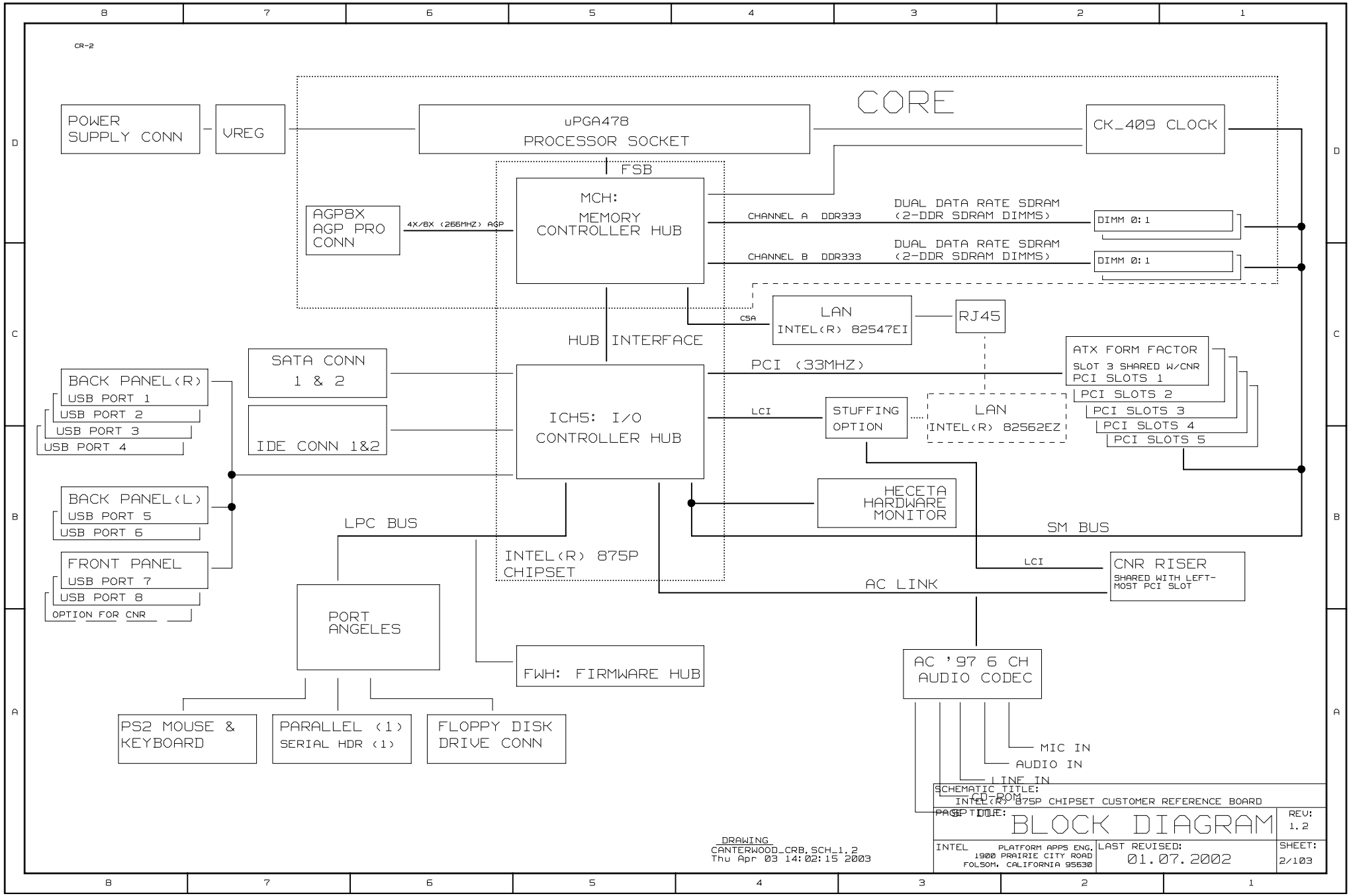
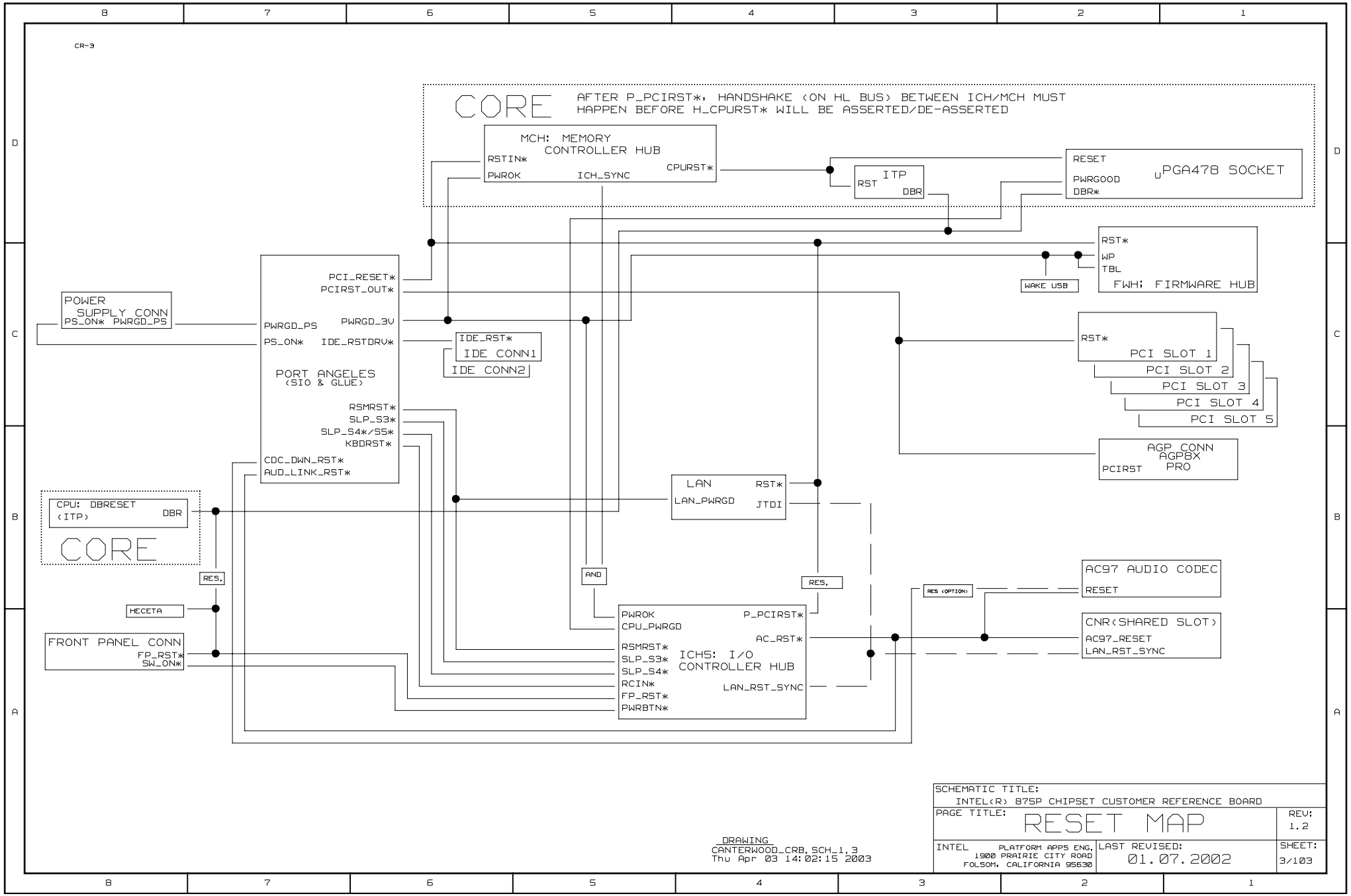
Thu Apr 03 14:02:15 2003

INTEL(R) 875P
CUSTOMER REFERENCE BOARD

2-CHANNEL DDR, AGP8X, 4 LAYER, ATX

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: TITLE PAGE		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 1/103


CR-2
CORE
POWER SUPPLY CONN
VREG
uPGA478 PROCESSOR SOCKET
CK_409 CLOCK
FSB
MCH: MEMORY CONTROLLER HUB
AGP8X AGP PRO CONN
4X/8X (266MHZ) AGP
CHANNEL A DDR333
DUAL DATA RATE SDRAM (2-DDR SDRAM DIMMS)
DIMM 0:1
CHANNEL B DDR333
DUAL DATA RATE SDRAM (2-DDR SDRAM DIMMS)
DIMM 0:1
CSA
LAN INTEL(R) 82547EI
RJ45
HUB INTERFACE
SATA CONN 1 & 2
IDE CONN 1&2
ICH5: I/O CONTROLLER HUB
PCI (33MHZ)
ATX FORM FACTOR
SLOT 3 SHARED W/CNR
PCI SLOTS 1
PCI SLOTS 2
PCI SLOTS 3
PCI SLOTS 4
PCI SLOTS 5
LCI
STUFFING OPTION
LAN INTEL(R) 82562EZ
BACK PANEL(R)
USB PORT 1
USB PORT 2
USB PORT 3
USB PORT 4
BACK PANEL(L)
USB PORT 5
USB PORT 6
FRONT PANEL
USB PORT 7
USB PORT 8
OPTION FOR CNR
HECETA HARDWARE MONITOR
LPC BUS
SM BUS
INTEL(R) 875P CHIPSET
LCI
CNR RISER
SHARED WITH LEFT-MOST PCI SLOT
AC LINK
PORT ANGELES
FWH: FIRMWARE HUB
AC '97 6 CH AUDIO CODEC
MIC IN
AUDIO IN
LINE IN
CD-ROM
PS2 MOUSE & KEYBOARD
PARALLEL (1)
SERIAL HDR (1)
FLOPPY DISK DRIVE CONN
DRAWING
CANTERWOOD_CRB.SCH_1,2
Thu Apr 03 14:02:15 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
BLOCK DIAGRAM
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
2/103


CR-3
CORE
AFTER P_PCIRST*, HANDSHAKE (ON HL BUS) BETWEEN ICH/MCH MUST HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED
MCH: MEMORY CONTROLLER HUB
RSTIN*
PWROK
ICH_SYNC
CPURST*
ITP
RST
DBR
RESET
PWRGOOD
DBR*
uPGA478 SOCKET
RST*
WP
TBL
FWH; FIRMWARE HUB
WAKE USB
POWER SUPPLY CONN
PS_ON* PWRGD_PS
PCI_RESET*
PCIRST_OUT*
PWRGD_PS
PWRGD_3V
PS_ON*
IDE_RSTDRV*
IDE_RST*
IDE CONN1
IDE CONN2
PORT ANGELES
(SIO & GLUE)
RSMRST*
SLP_S3*
SLP_S4*/S5*
KBDRST*
CDC_DWN_RST*
AUD_LINK_RST*
RST*
PCI SLOT 1
PCI SLOT 2
PCI SLOT 3
PCI SLOT 4
PCI SLOT 5
AGP CONN
AGP8X PRO
PCIRST
LAN
LAN_PWRGD
RST*
JTDI
CPU: DBRESET (ITP)
DBR
CORE
RES.
AND
RES.
RES (OPTION)
HECETA
FRONT PANEL CONN
FP_RST*
SW_ON*
PWROK
CPU_PWRGD
RSMRST*
SLP_S3*
SLP_S4*
RCIN*
FP_RST*
PWRBTN*
P_PCIRST*
AC_RST*
ICH5: I/O CONTROLLER HUB
LAN_RST_SYNC
AC97 AUDIO CODEC
RESET
CNR (SHARED SLOT)
AC97_RESET
LAN_RST_SYNC
DRAWING
CANTERWOOD_CRB.SCH_1.3
Thu Apr 03 14:02:15 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
RESET MAP
REV:
1.2
INTEL
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LAST REVISED:
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SHEET:
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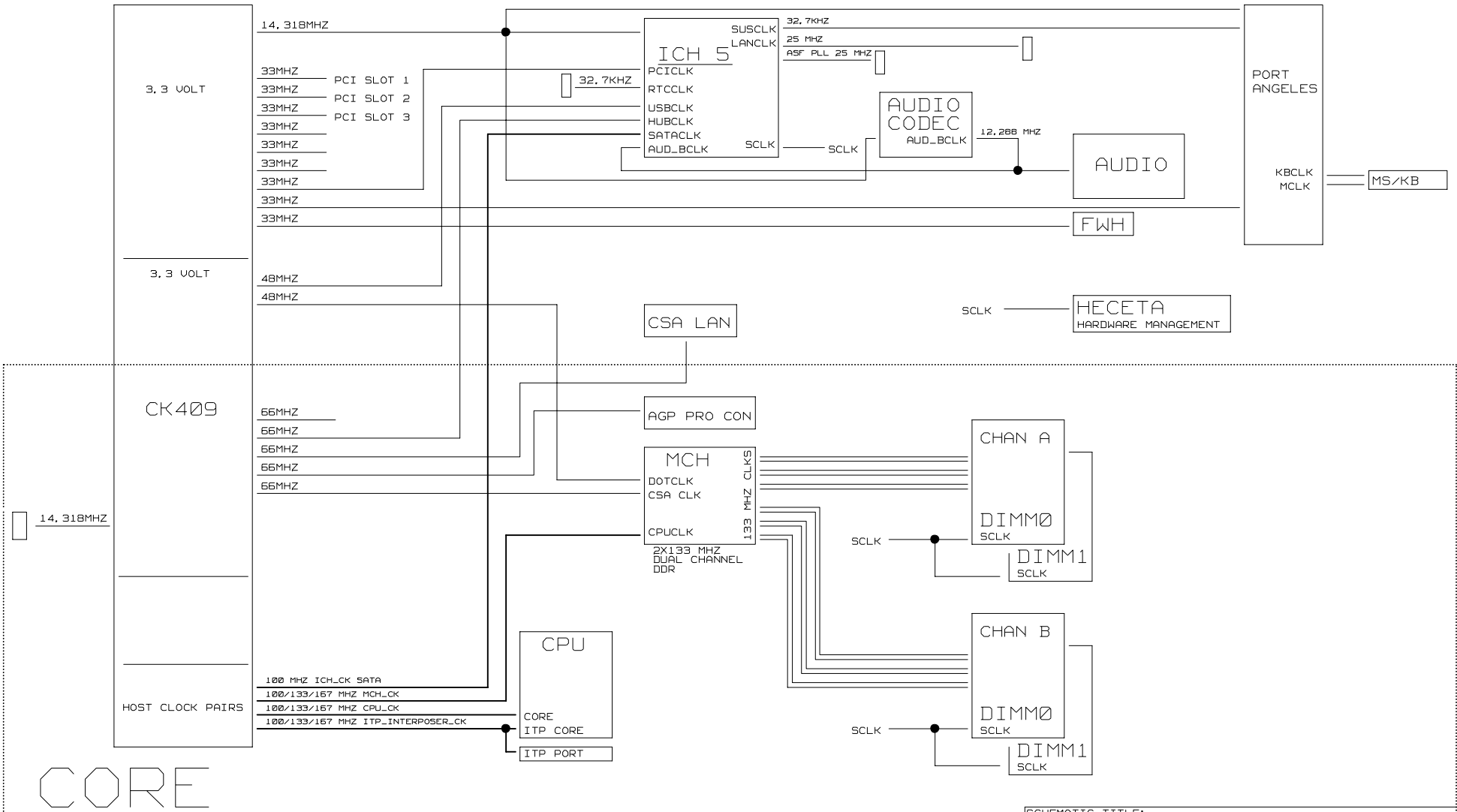
CR-4



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SCHEMATIC TITLE: INTEL® 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CLOCK DISTRIBUTION		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 4/103

CR-5

	PIN NAME	WELL	USAGE	DURING RESET	S3/S5	NOTES
ICH 5	GPI[0]	MAIN	P_REQA*			
	GPI[1]	MAIN	P_REQ5*			
	GPI[2]	MAIN	P_INTE*			
	GPI[3]	MAIN	P_INTF*			
	GPI[4]	MAIN	P_INTG*			
	GPI[5]	MAIN	P_INTH*			
	GPI[6]	MAIN	AGPBUSY*			
	GPI[7]	MAIN	BOARD SKU 0			
	GPI[8]	RESUME	CSA_PME*			
	GPI[9]	RESUME	OC[4]*			
	GPI[10]	RESUME	OC[5]*			
	GPI[11]	RESUME	SMBALERT*			
	GPI[12]	RESUME	LPC_SIO_SMI*			
	GPI[13]	RESUME	LPC_SIO_PME*			
	GPI[14]	RESUME	OC[6]*			
	GPI[15]	RESUME	OC[7]*			
	GPO[16]	MAIN	GNT[A]*			
	GPO[17]	MAIN	GNT[5]*			
	GPO[18]	MAIN	GPO18_LED			
	GPIO[24]	RESUME	CLKRUN*			
	GPIO[25]	RESUME	GPIO_LAN_DISABLE			
	GPIO[27]	RESUME	GPIO_AUD_EN (OUTPUT)			
	GPIO[28]	RESUME	CODEC_DOWN_EN*			
	GPIO[32]	MAIN	BOARD SKU 1			
	GPIO[33]	MAIN	BOARD SKU 2			
	GPIO[34]	MAIN	BOARD SKU 3			
	GPI[40]	MAIN	REQ[4]*			
	GPI[41]	MAIN	LDRQ[1]*			
	GPO[48]	MAIN	GNT[4]*			
	GPO[49]	CPU	CPUPWRGD			
FWH	GPI4	MAIN	NORM	INPUT	DEFINED	CONFIG JUMPER
	GPI3	MAIN	MFG_MODE*	INPUT	DEFINED	MANUF MODE
	GPI2	MAIN	NOT USED	INPUT	DEFINED	HI/LOW BIOS CONFIG (FEATURE IS DEFAULT LOW)
	GPI1	MAIN	DMA66_DETECT_SEC	INPUT	DEFINED	HI/LOW BIOS CONFIG FOR IDE SEC (FEATURE IS DEFAULT LOW)
	GPI0	MAIN	DMA66_DETECT_PRI	INPUT	DEFINED	HI/LOW BIOS CONFIG FOR IDE PRI (FEATURE IS DEFAULT LOW)
PORT ANGELES	GPO0	RESUME	FAN1_CTRL			
	GPO1	RESUME	FAN2_CTRL			
	GPI6	RESUME	FAN1_TACH			
	GPI7	RESUME	FAN2_TACH			
	GPI08	RESUME	5V_DDCSDA			
	GPIO9	RESUME	5V_DDCSCL			
	GPIO10	RESUME	3V_DDCSDA			
	GPI011	RESUME	3V_DDCSCL			
	GPI12	RESUME	CDC_DWN_ENAB*			
	IO_PME*	RESUME	IO_PME*			
	GRN_LED	RESUME	GRN_LED			
	YLW_LED	RESUME	YLW_LED			

IRQ ROUTING TABLE

	AGP	SLOT1	SLOT2	SLOT3			
P_INTA*	IRQA			IRQD			
P_INTB*	IRQB			IRQA			
P_INTC*				IRQB			
P_INTD*				IRQC			
P_INTE*		IRQD	IRQC				
P_INTF*		IRQA	IRQB				
P_INTG*		IRQB	IRQA				
P_INTH*		IRQC	IRQD				
REQ/GNT		0	1	2			
IDSEL		16	17	18			

MULTI-PLEXED GPIO PINS ON PORT ANGELES USED FOR SPECIFIC FUNCTIONS (NOT AS GPIO) ARE NOT IDENTIFIED HERE
UN-USED GPIO PINS ON PORT ANGELES ARE NOT IDENTIFIED HERE
TOTAL OF (37) POSSIBLE GPIO PINS ON PORT ANGELES.

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SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: GPIO, IRQ, IDSEL MAPS

REV: 1.2

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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LAST REVISED: 01.07.2002

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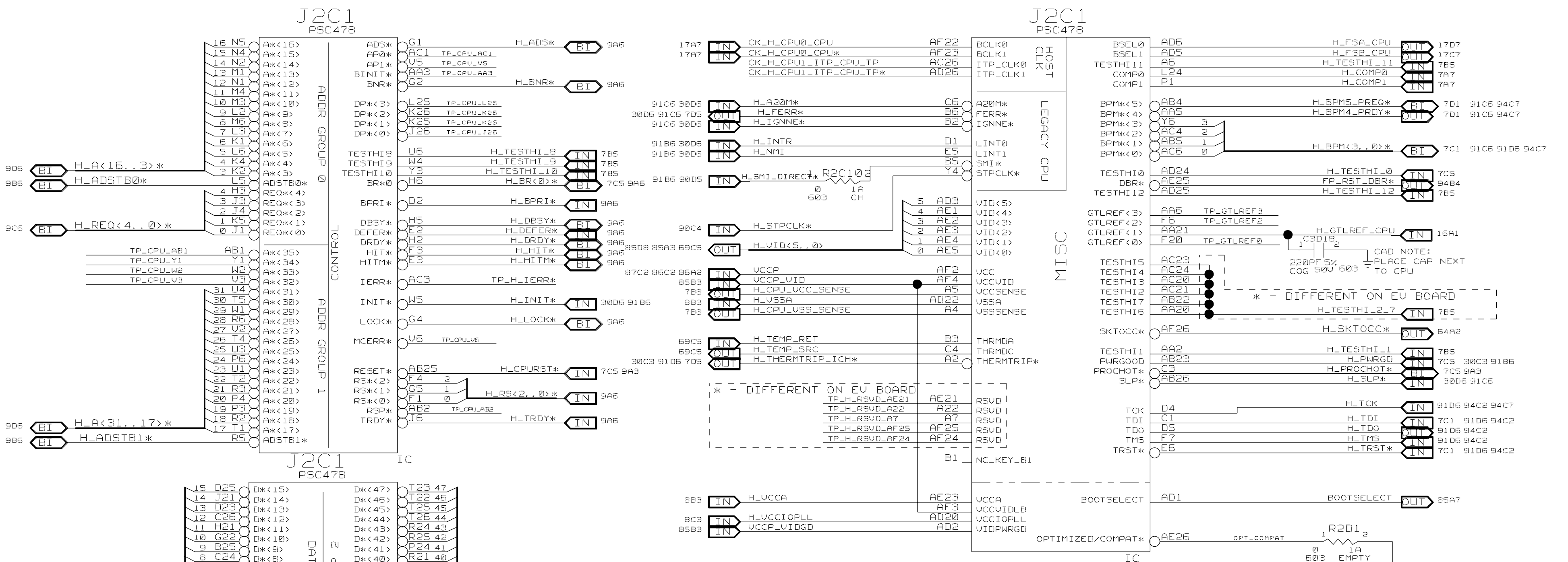

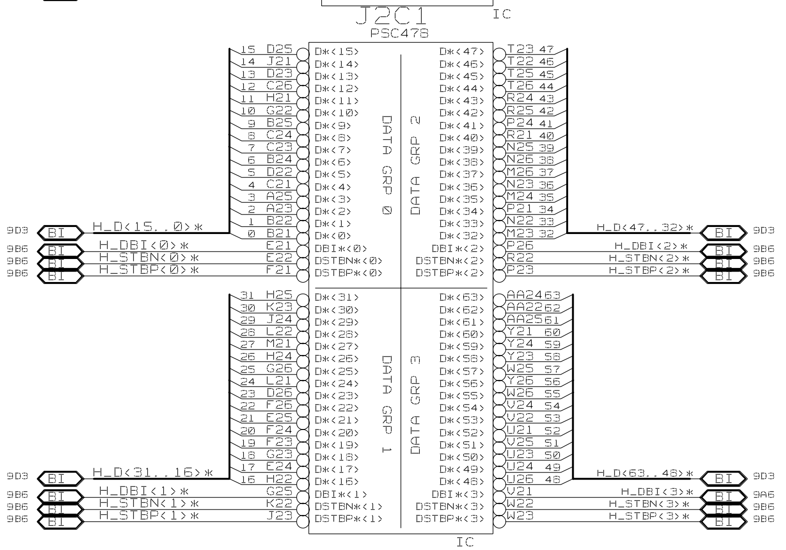

VCCP=AD11, AD9, AD7, AD19, AE18, AE16, AE14, AE12, AE10, AE8, AE6, AE20
VCCP=AB15, AB13, AB11, AB9, AB7, AB19, AC18, AC16, AC14, AC12, AC10, AC8, AD17, AD15, AD13
VCCP=E14, E12, E10, E8, E20, F17, F15, F13, F11, F9, F19, AA18, AA16, AA14, AA12, AA10, AA8, AB17
VCCP=B13, B11, B9, B7, B19, C18, C16, C14, C12, C10, C8, C20, D17, D15, D13, D11, D9, D7, D19, E18, E16
VCCP=AF17, AF15, AF13, AF11, AF9, AF7, AF5, AF21, AF19, A18, A16, A14, A12, A10, A8, A20, B17, B15

GND=W24, Y2, Y5, Y22, Y25, AA1, AA4, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA23, AA26
GND=N6, N3, N24, N21, P5, P2, P25, P22, R26, R4, R1, R23, T6, T3, T24, T21, U5, U2, U25, U22, V26
GND=G21, H26, H4, H1, H23, J5, J2, J25, J22, K6, K3, K24, K21, L26, L4, L1, L23, M5, M2, M25, M22
GND=E11, E9, E26, E7, E4, E1, E23, E19, F18, F16, F14, F12, F10, F8, F5, F2, F25, F22, G6, G3, G24
GND=C5, C2, C25, C22, C19, D18, D16, D14, D12, D10, D8, D6, D3, D24, D21, D20, E17, E15, E13
GND=A3, A24, A21, A19, B18, B16, B14, B12, B10, B26, B8, B4, B23, B20, C17, C15, C13, C11, C9, C7
GND=AF18, AF16, AF14, AF12, AF10, AF8, AF6, AF1, AF20, A17, A15, A13, A11, A9, A26
GND=AE7, AE24, AE22, AE19
GND=AD14, AD12, AD10, AD8, AD4, AD23, AD21, AE17, AE15, AE13, AE11, AE9
GND=AB20, AC17, AC15, AC13, AC11, AC9, AC7, AC5, AC2, AC25, AC22, AC19, AD18, AD16
GND=AB18, AB16, AB14, AB12, AB10, AB8, AB6, AB3, AB24, AB21
GND=V4, V1, V23, W6, W3, W21, AA26

CAD NOTE:

H_D AND H_A (AND ASSOCIATED SIGNALS)
MUST BE LENGTH MATCHED TO THE STROBE (STB OR STBP/STBN)
SIGNAL(S) WITHIN THE SAME GROUP TO +/-25 MILS,
AND STBP/STBN PAIRS MUST BE MATCHED TO +/-10 MILS OF EACH OTHER.

DESIGN NOTE:

AF3 TIED TO VCCVID FOR PRESCOTT SUPPORT
AE26 IS GND ON PENTIUM 4 PROCESSOR BUT WILL BE DETECT ON PRESCOTT

TESTHI PIN NAME MAPPING	
TESTHI[0]	BYPASSEN
TESTHI[1]	ODT
TESTHI[5:2]	MCLK[3:0]
TESTHI[7:6]	MCLKIO[1:0]
TESTHI[10:8]	BR#[3:1]
TESTHI[11]	GHI#
TESTHI[12]	DPSLP#

DRAWING
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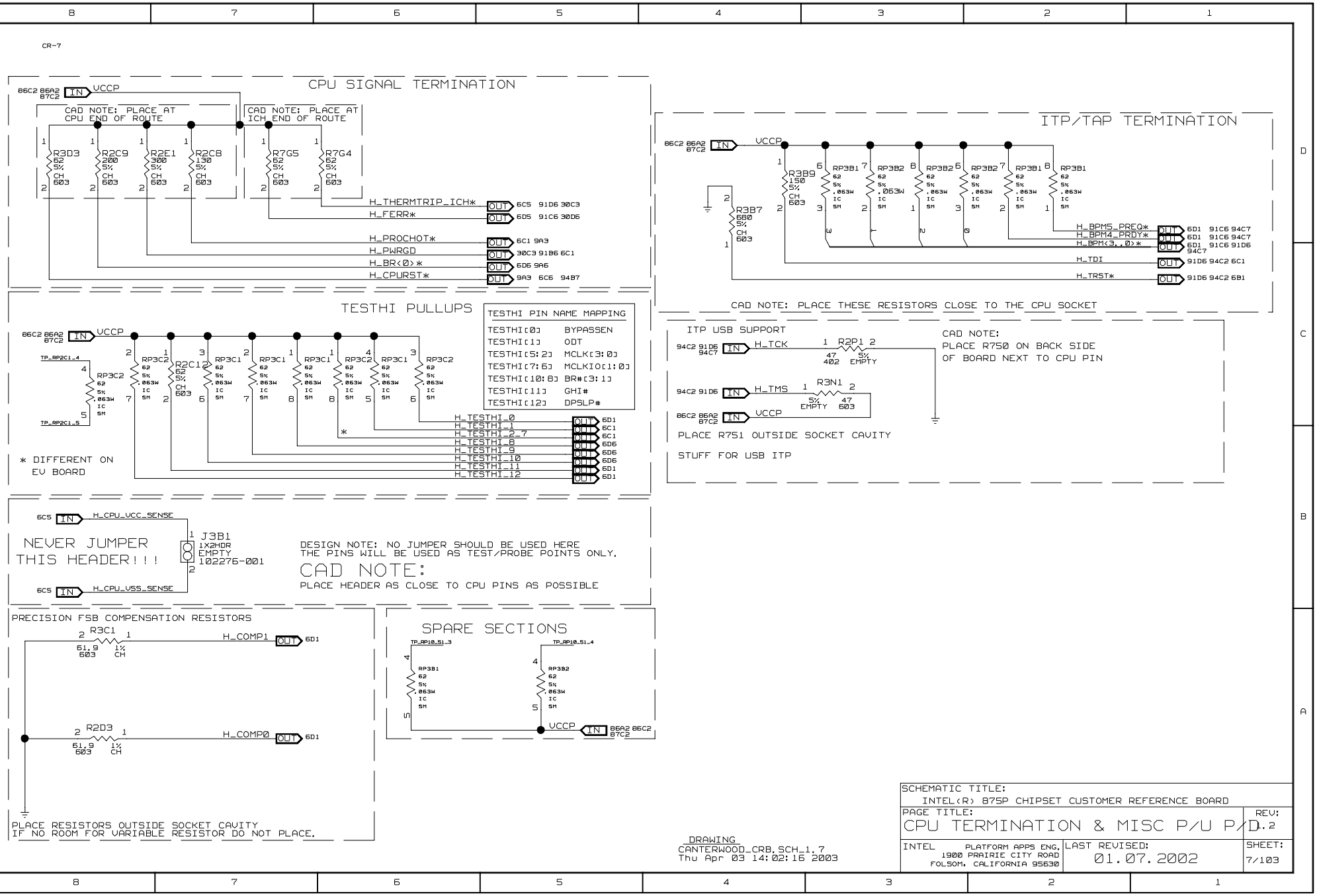
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU CONNECTOR uPGA478 (PSC/NWD)		REV: 1.2
INTEL — PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 6/103


CR-7
CPU SIGNAL TERMINATION
VCCP
CAD NOTE: PLACE AT CPU END OF ROUTE
CAD NOTE: PLACE AT ICH END OF ROUTE
R3D3 62 5% CH 603
R2C9 200 5% CH 603
R2E1 300 5% CH 603
R2C8 130 5% CH 603
R7G5 62 5% CH 603
R7G4 62 5% CH 603
H_THERMTRIP_ICH*
H_FERR*
H_PROCHOT*
H_PWRGD
H_BR<0>*
H_CPURST*
ITP/TAP TERMINATION
R3B9 150 5% CH 603
R3B7 680 5% CH 603
RP3B1 62 5% .063W IC 5M
RP3B2 62 5% .063W IC 5M
H_BPM5_PREQ*
H_BPM4_PRDY*
H_BPM<3,0>*
H_TDI
H_TRST*
CAD NOTE: PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET
TESTHI PULLUPS
TESTHI PIN NAME MAPPING
TESTHI[0] BYPASSEN
TESTHI[1] ODT
TESTHI[5:2] MCLK[3:0]
TESTHI[7:6] MCLKIO[1:0]
TESTHI[10:8] BR#[3:1]
TESTHI[11] GHI#
TESTHI[12] DPSLP#
RP3C1 62 5% .063W IC 5M
RP3C2 62 5% .063W IC 5M
R2C1 62 5% CH 603
TP_RP2C1_4
TP_RP2C1_5
H_TESTHI_0
H_TESTHI_1
H_TESTHI_2_7
H_TESTHI_8
H_TESTHI_9
H_TESTHI_10
H_TESTHI_11
H_TESTHI_12
* DIFFERENT ON EV BOARD
ITP USB SUPPORT
H_TCK
R2P1 47 402 5% EMPTY
H_TMS
R3N1 5% EMPTY 47 603
PLACE R751 OUTSIDE SOCKET CAVITY
STUFF FOR USB ITP
CAD NOTE:
PLACE R750 ON BACK SIDE OF BOARD NEXT TO CPU PIN
H_CPU_VCC_SENSE
H_CPU_VSS_SENSE
NEVER JUMPER THIS HEADER!!!
J3B1 1X2HDR EMPTY 102276-001
DESIGN NOTE: NO JUMPER SHOULD BE USED HERE THE PINS WILL BE USED AS TEST/PROBE POINTS ONLY.
CAD NOTE:
PLACE HEADER AS CLOSE TO CPU PINS AS POSSIBLE
PRECISION FSB COMPENSATION RESISTORS
R3C1 61.9 603 1% CH
R2D3 61.9 603 1% CH
H_COMP1
H_COMP0
PLACE RESISTORS OUTSIDE SOCKET CAVITY IF NO ROOM FOR VARIABLE RESISTOR DO NOT PLACE.
SPARE SECTIONS
TP_RP1B_5I_3
TP_RP1B_5I_4
DRAWING
CANTERWOOD_CRB.SCH_1,7
Thu Apr 03 14:02:16 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
CPU TERMINATION & MISC P/U P/D
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
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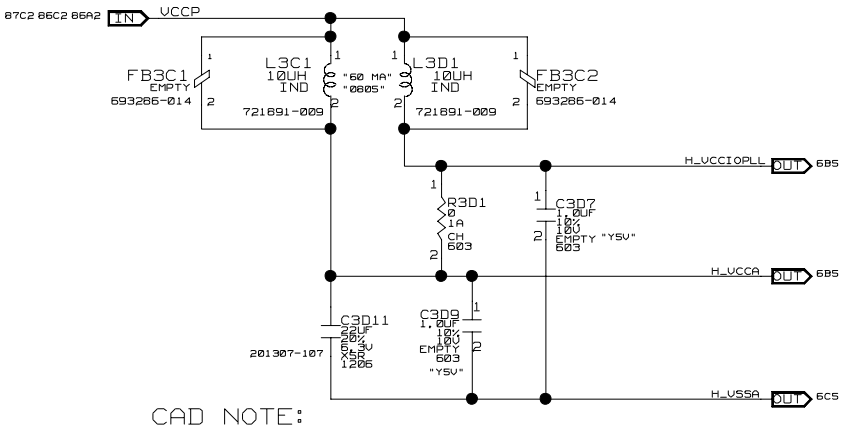
7/103

CR-8

PLL SUPPLY FILTER



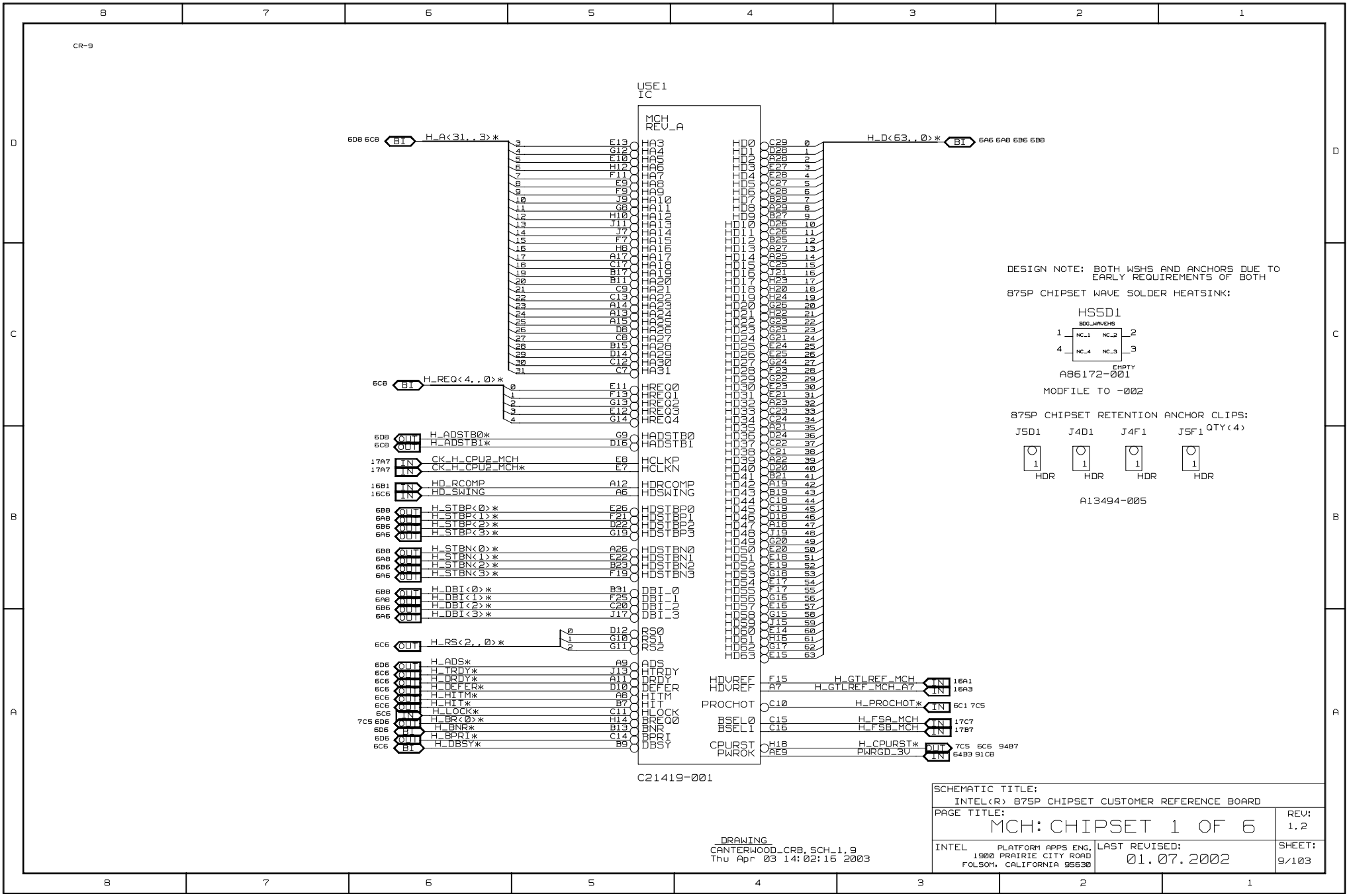
CAD NOTE:

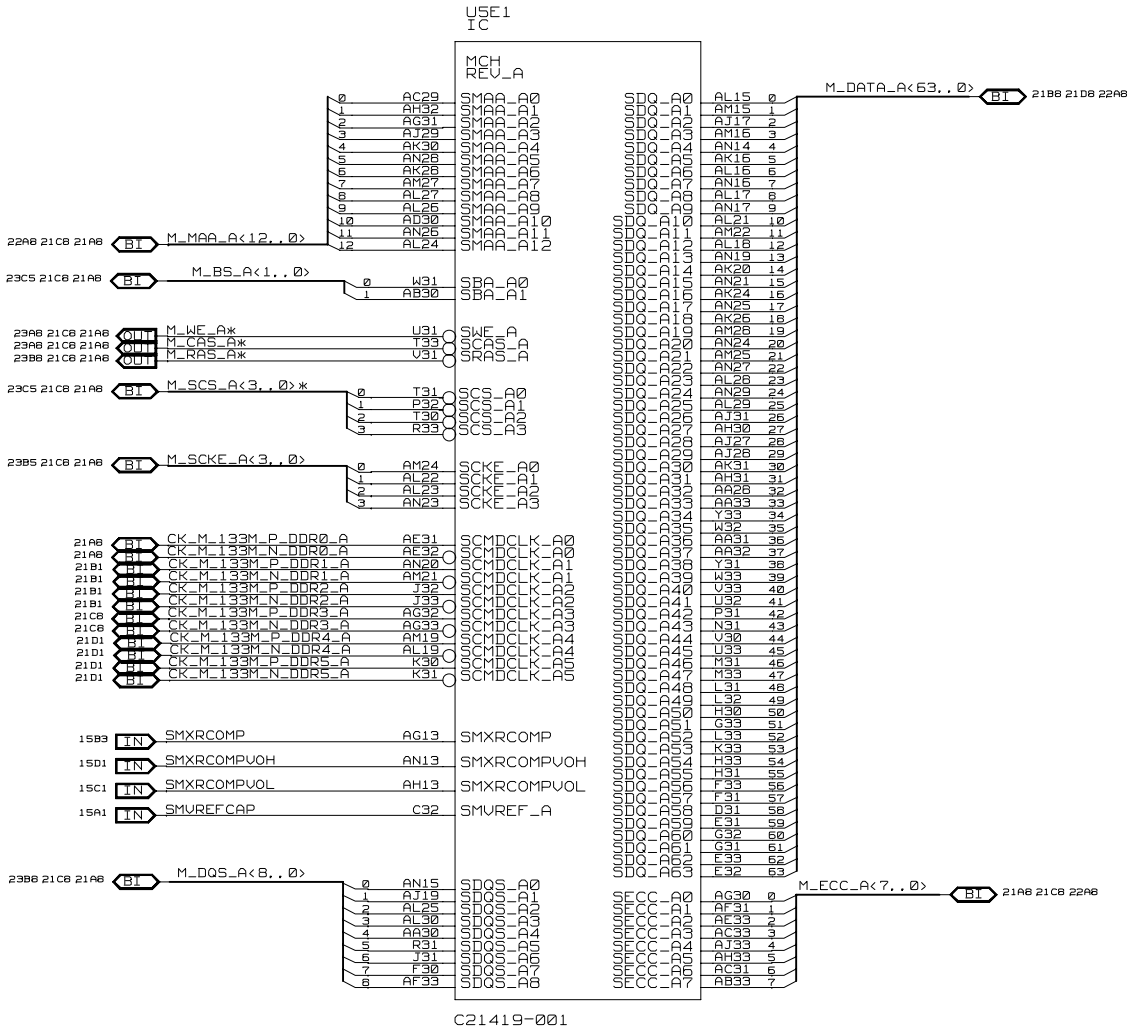
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

DRAWING
CANTERWOOD_CRB.SCH_1.8
Thu Apr 03 14:02:16 2003

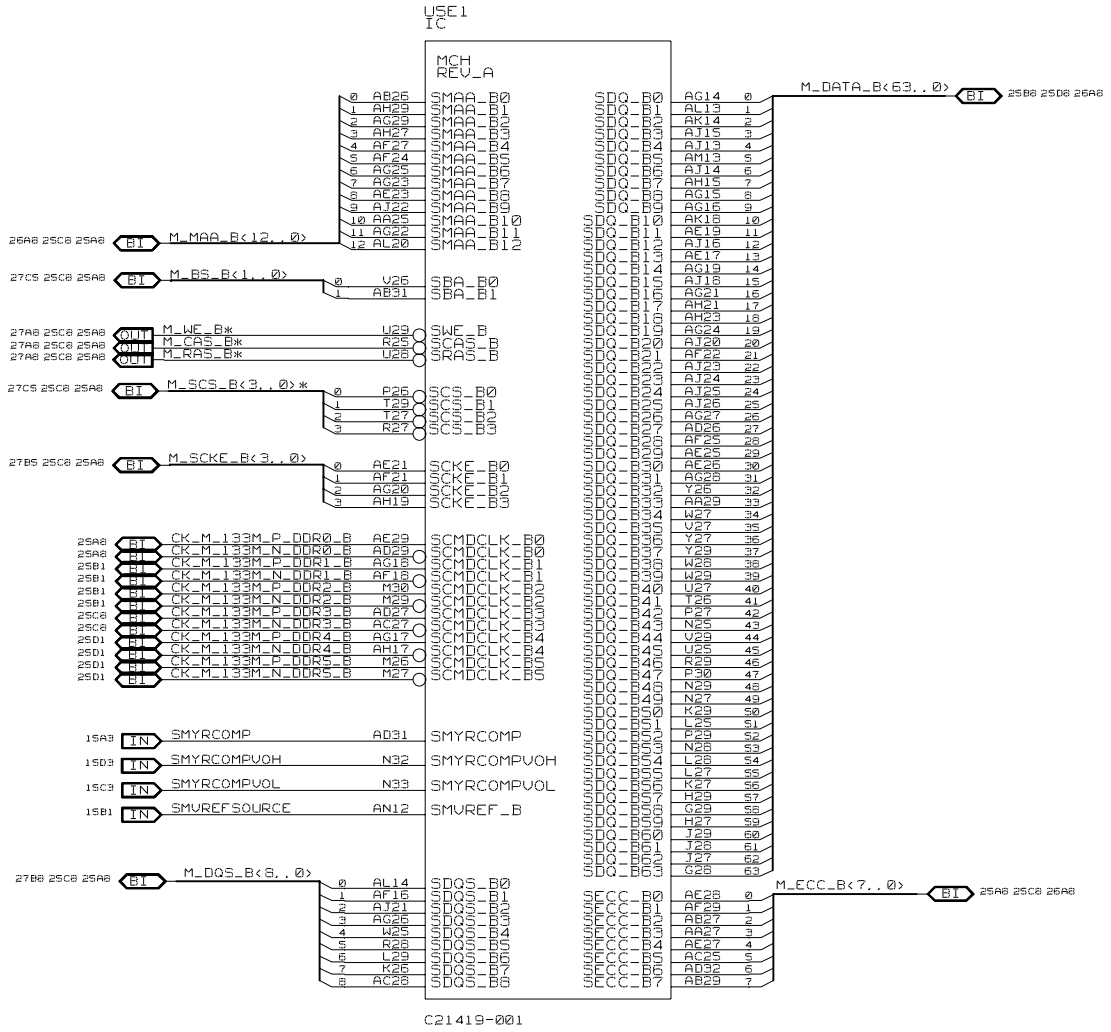
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU-VCCP FILTERED ANALOG SUPPLY		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 8/103


CR-9
U5E1
IC
MCH
REV_A
H_A<31..3>*
H_REQ<4..0>*
H_ADSTB0*
H_ADSTB1*
CK_H_CPU2_MCH
CK_H_CPU2_MCH*
HD_RCOMP
HD_SWING
H_STBP<0>*
H_STBP<1>*
H_STBP<2>*
H_STBP<3>*
H_STBN<0>*
H_STBN<1>*
H_STBN<2>*
H_STBN<3>*
H_DBI<0>*
H_DBI<1>*
H_DBI<2>*
H_DBI<3>*
H_RS<2..0>*
H_ADS*
H_TRDY*
H_DRDY*
H_DEFER*
H_HITM*
H_HIT*
H_LOCK*
H_BR<0>*
H_BNR*
H_BPRI*
H_DBSY*
H_D<63..0>*
H_GTLREF_MCH
H_GTLREF_MCH_A7
H_PROCHOT*
H_FSA_MCH
H_FSB_MCH
H_CPURST*
PWRGD_3V
C21419-001
DESIGN NOTE: BOTH WSHS AND ANCHORS DUE TO EARLY REQUIREMENTS OF BOTH
875P CHIPSET WAVE SOLDER HEATSINK:
HS5D1
BDG_WAVEHS
NC_1
NC_2
NC_3
NC_4
EMPTY
A86172-001
MODFILE TO -002
875P CHIPSET RETENTION ANCHOR CLIPS:
J5D1
J4D1
J4F1
J5F1
QTY<4>
HDR
A13494-005
DRAWING
CANTERWOOD_CRB.SCH_1,9
Thu Apr 03 14:02:16 2003
SCHEMATIC TITLE:
INTEL<R> 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH: CHIPSET 1 OF 6
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
9/103



DRAWING
CANTERWOOD_CRB.SCH_1.10
Thu Apr 03 14:02:16 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: MCH: CHIPSET 2 OF 6		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 10/103



SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
MCH: CHIPSET 3 OF 6

REV: 1.2

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED:
01.07.2002

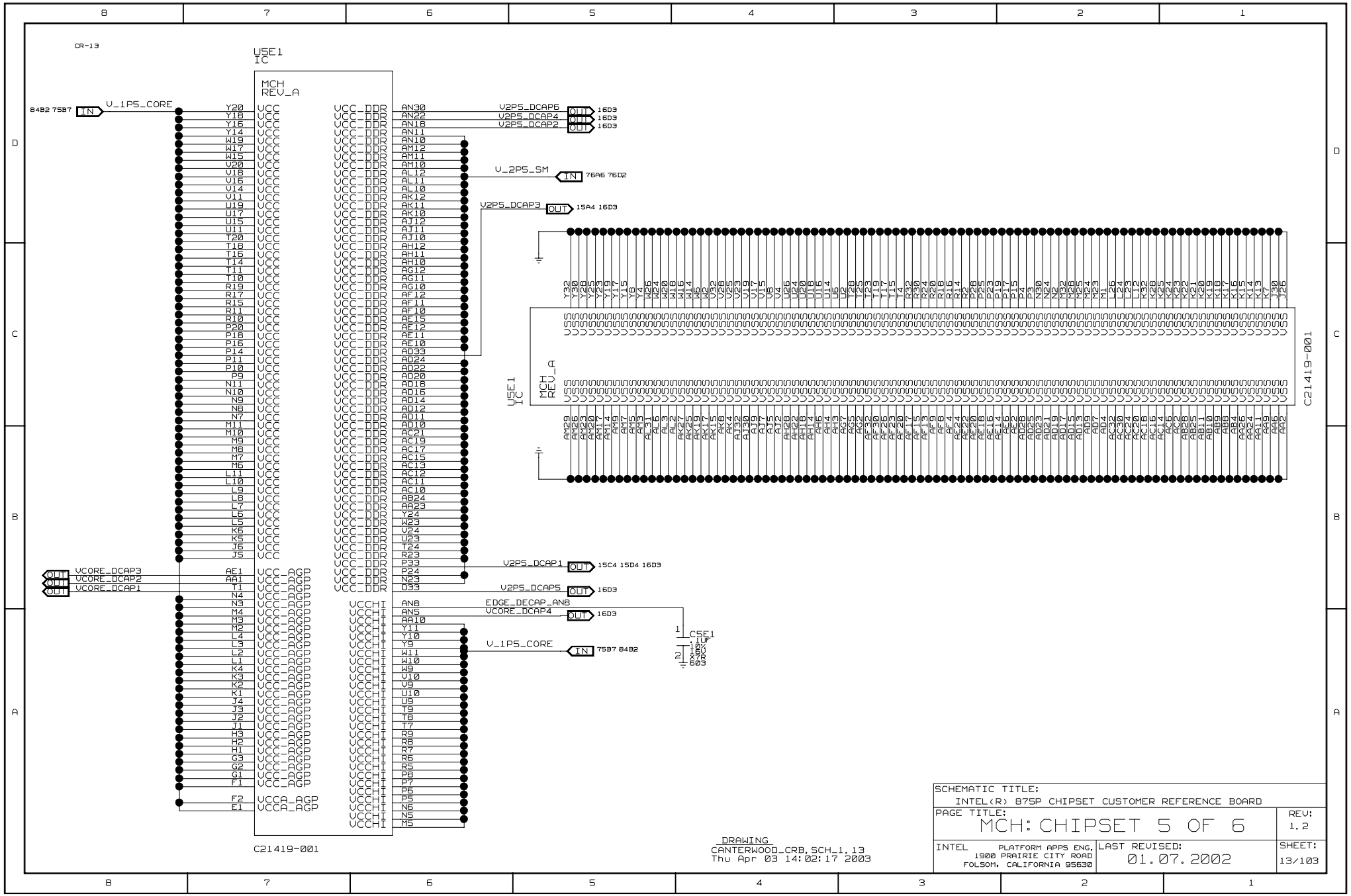
SHEET:
11/103

DRAWING
CANTERWOOD_CRB.SCH_1.11
Thu Apr 03 14:02:17 2003

CR-12

DRAWING
CANTERWOOD_CRB.SCH_1,12
Thu Apr 03 14:02:17 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: MCH: CHIPSET 4 OF 6		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 12/103

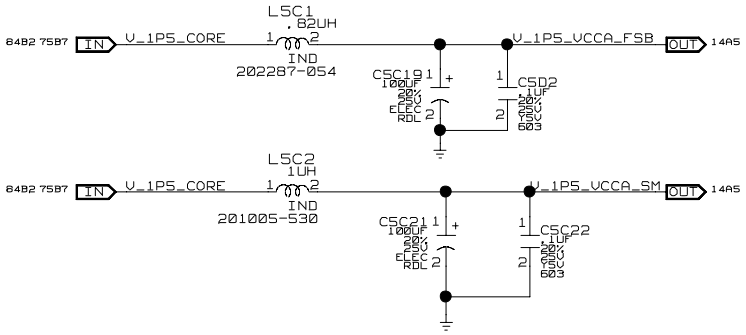

CR-13
U5E1
IC
MCH
REV_A
V_1P5_CORE
V_2P5_SM
V2P5_DCAP3
V2P5_DCAP6
V2P5_DCAP4
V2P5_DCAP2
V2P5_DCAP1
V2P5_DCAP5
VCORE_DCAP3
VCORE_DCAP2
VCORE_DCAP1
EDGE_DECAP_AN8
VCORE_DCAP4
C5E1
1UF
C21419-001
DRAWING
CANTERWOOD_CRB.SCH_1,13
Thu Apr 03 14:02:17 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH: CHIPSET 5 OF 6
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
13/103

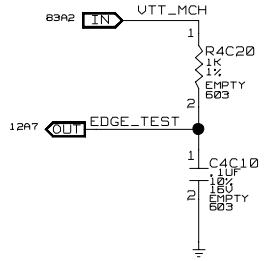

CR-14
U5E1
IC
MCH
REV_A
83A2
IN
VTT_MCH
16C3
16C3
16D3
16D3
OUT
VTT_DCAP4
VTT_DCAP1
VTT_DCAP2
VTT_DCAP3
CAD NOTE:
ROUTE TO VIA
VCC3
VCC3_3
V_1P5_VCCA_FSB
15D6
V_1P5_VCCA_SM
15C6
C5F1
C4E1
1UF
10V
16V
X7R
603
C21419-001
DRAWING
CANTERWOOD_CRB.SCH,1,14
Thu Apr 03 14:02:17 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH: CHIPSET 6 OF 6
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
14/103

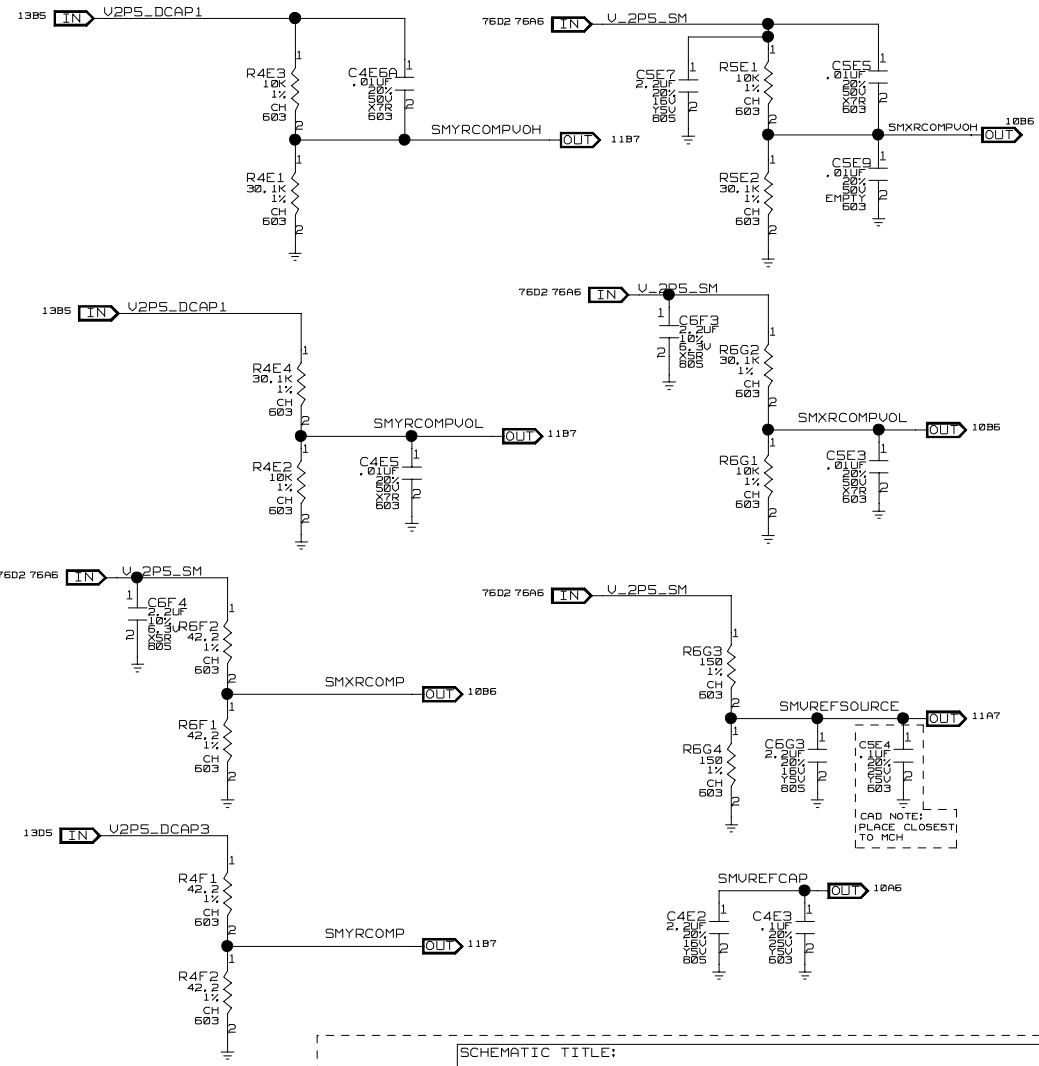
CR-15

ANALOG FILTERS

DCL_CORE_GMCH

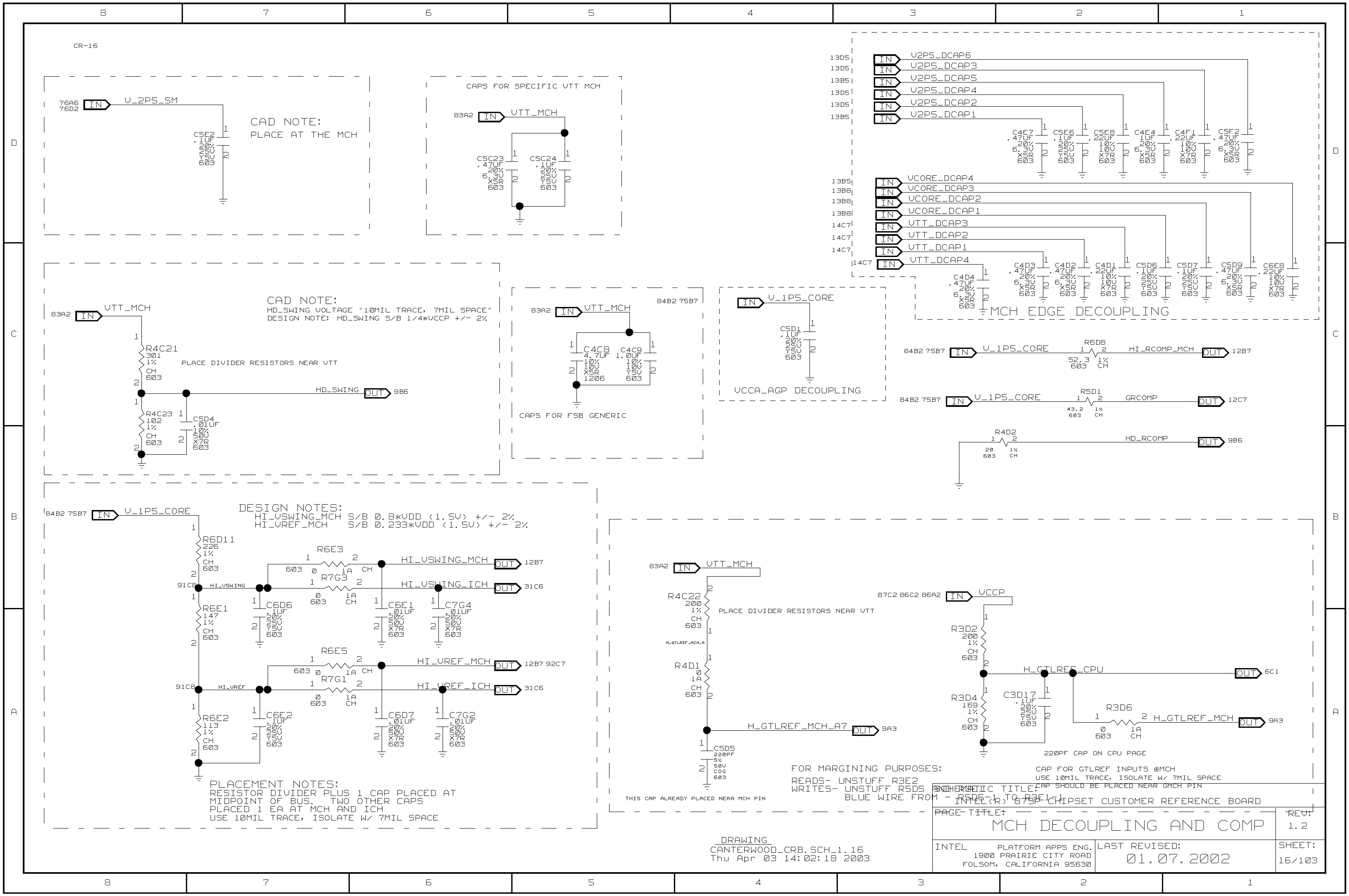


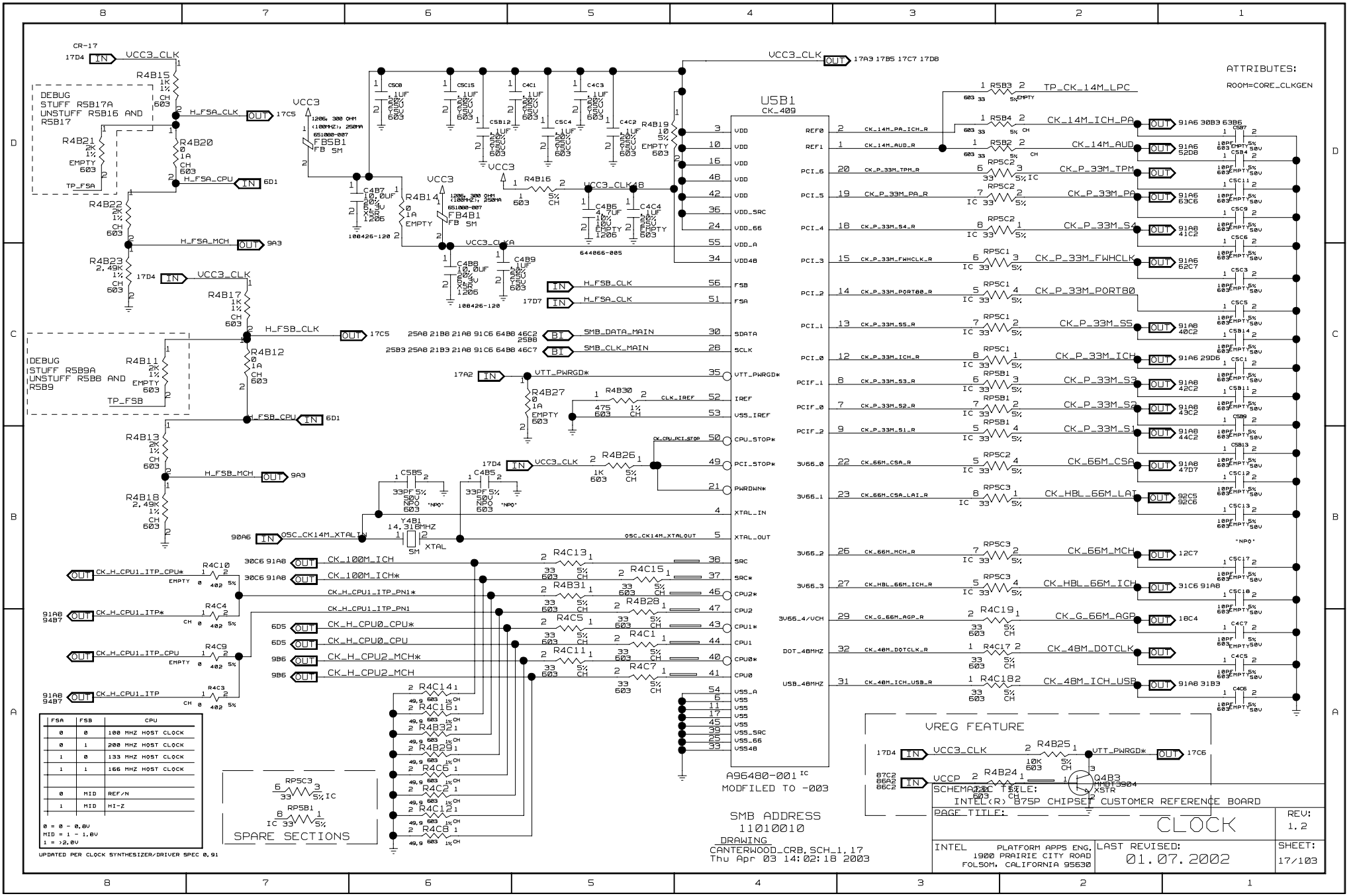




DRAWING
CANTERWOOD_CRB.SCH_1.15
Thu Apr 03 14:02:17 2003

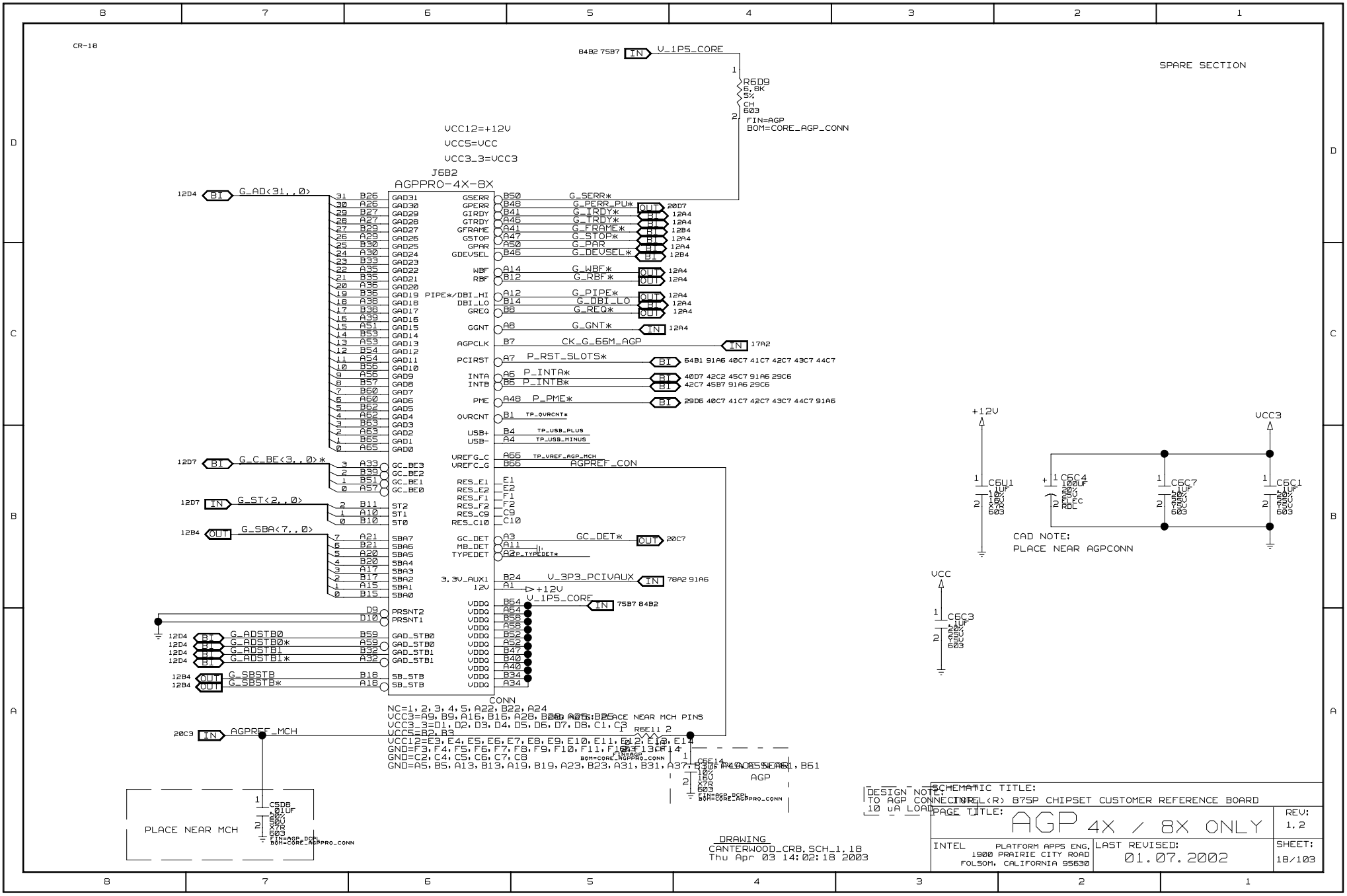
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: MCH; ANALOG FILTERS		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 15/103


CR-16
CAD NOTE:
PLACE AT THE MCH
V_2P5_SM
CAPS FOR SPECIFIC VTT MCH
VTT_MCH
C5E2 .1UF 20% 25V Y5V 603
C5C23 .47UF 20% 6.3V X5R 603
C5C24 .1UF 20% 25V Y5V 603
V2P5_DCAP6
V2P5_DCAP3
V2P5_DCAP5
V2P5_DCAP4
V2P5_DCAP2
V2P5_DCAP1
VCORE_DCAP4
VCORE_DCAP3
VCORE_DCAP2
VCORE_DCAP1
VTT_DCAP3
VTT_DCAP2
VTT_DCAP1
VTT_DCAP4
MCH EDGE DECOUPLING
CAD NOTE:
HD_SWING VOLTAGE "10MIL TRACE, 7MIL SPACE"
DESIGN NOTE: HD_SWING S/B 1/4*VCCP +/- 2%
PLACE DIVIDER RESISTORS NEAR VTT
R4C21 301 1% CH 603
R4C23 102 1% CH 603
C5D4 .01UF 10% 50V X7R 603
HD_SWING
CAPS FOR FSB GENERIC
C4C8 4.7UF 10% 10V X5R 1206
C4C9 1.0UF 10% 10V Y5V 603
V_1P5_CORE
C5D1 .1UF 20% 25V Y5V 603
VCCA_AGP DECOUPLING
R6D8 52.3 1% 603 CH
HI_RCOMP_MCH
R5D1 43.2 1% 603 CH
GRCOMP
R4D2 20 1% 603 CH
HD_RCOMP
DESIGN NOTES:
HI_VSWING_MCH S/B 0.8*VDD (1.5V) +/- 2%
HI_VREF_MCH S/B 0.233*VDD (1.5V) +/- 2%
R6D11 226 1% CH 603
R6E3 0 1A CH 603
R7G3 0 1A CH 603
HI_VSWING_MCH
HI_VSWING_ICH
R6E1 147 1% CH 603
C6D6 .1UF 20% 25V Y5V 603
C6E1 .01UF 20% 50V X7R 603
C7G4 .01UF 20% 50V X7R 603
R6E5 0 1A CH 603
R7G1 0 1A CH 603
HI_VREF_MCH
HI_VREF_ICH
R6E2 113 1% CH 603
C6E2 .1UF 20% 25V Y5V 603
C6D7 .01UF 20% 50V X7R 603
C7G2 .01UF 20% 50V X7R 603
PLACEMENT NOTES:
RESISTOR DIVIDER PLUS 1 CAP PLACED AT
MIDPOINT OF BUS. TWO OTHER CAPS
PLACED 1 EA AT MCH AND ICH
USE 10MIL TRACE, ISOLATE W/ 7MIL SPACE
R4C22 200 1% CH 603
R4D1 0 1A CH 603
H_GTLREF_MCH_A7
C5D5 220PF 5% 50V COG 603
THIS CAP ALREADY PLACED NEAR MCH PIN
VCCP
R3D2 200 1% CH 603
R3D4 169 1% CH 603
C3D17 .1UF 20% 25V Y5V 603
R3D6 0 1A CH 603
H_GTLREF_CPU
H_GTLREF_MCH
220PF CAP ON CPU PAGE
CAP FOR GTLREF INPUTS @MCH
USE 10MIL TRACE, ISOLATE W/ 7MIL SPACE
CAP SHOULD BE PLACED NEAR GMCH PIN
FOR MARGINING PURPOSES:
READS- UNSTUFF R3E2
WRITES- UNSTUFF R5D5 AND R3E1
BLUE WIRE FROM - R5D5-1 TO R3E1-1
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH DECOUPLING AND COMP
REV: 1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: 01.07.2002
SHEET: 16/103
DRAWING
CANTERWOOD_CRB.SCH_1.16
Thu Apr 03 14:02:18 2003



FSA	FSB	CPU
0	0	100 MHZ HOST CLOCK
0	1	200 MHZ HOST CLOCK
1	0	133 MHZ HOST CLOCK
1	1	166 MHZ HOST CLOCK
0	MID	REF/N
1	MID	HI-Z

0 = 0 - 0.8V
MID = 1 - 1.8V
1 = >2.0V


CR-18
SPARE SECTION
V_1P5_CORE
R5D9
6.8K
5%
CM
603
FIN=AGP
BOM=CORE_AGP_CONN
VCC12=+12V
VCC5=VCC
VCC3_3=VCC3
J6B2
AGPPRO-4X-8X
G_AD<31,,0>
G_SERR*
G_PERR_PU*
G_IRDY*
G_TRDY*
G_FRAME*
G_STOP*
G_PAR
G_DEVSEL*
G_WBF*
G_RBF*
G_PIPE*
G_DBI_LO
G_REQ*
G_GNT*
CK_G_66M_AGP
P_RST_SLOTS*
P_INTA*
P_INTB*
P_PME*
TP_OVRCNT*
TP_USB_PLUS
TP_USB_MINUS
TP_VREF_AGP_MCH
AGPREF_CON
G_C_BE<3,,0>*
G_ST<2,,0>
G_SBA<7,,0>
GC_DET*
V_3P3_PCIVAUX
+12V
V_1P5_CORE
G_ADSTB0
G_ADSTB0*
G_ADSTB1
G_ADSTB1*
G_SBSTB
G_SBSTB*
CONN
NC=1, 2, 3, 4, 5, A22, B22, A24
VCC3=A9, B9, A16, B16, A28, B28, A35, B35
VCC3_3=D1, D2, D3, D4, D5, D6, D7, D8, C1, C3
VCC5=B2, B3
VCC12=E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14
GND=F3, F4, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14
GND=A5, B5, A13, B13, A19, B19, A23, B23, A31, B31, A37, B37, A41, B41, A55, B55, A61, B61
AGPREF_MCH
PLACE NEAR MCH
PLACE NEAR MCH PINS
AGP
CAD NOTE:
PLACE NEAR AGPCONN
VCC
DESIGN NOTE:
TO AGP CONNECTOR
10 uA LOAD
DRAWING
CANTERWOOD_CRB.SCH_1, 18
Thu Apr 03 14:02:18 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
AGP 4X / 8X ONLY
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
18/103

CR-19

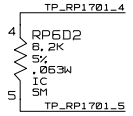
BLANK PAGE

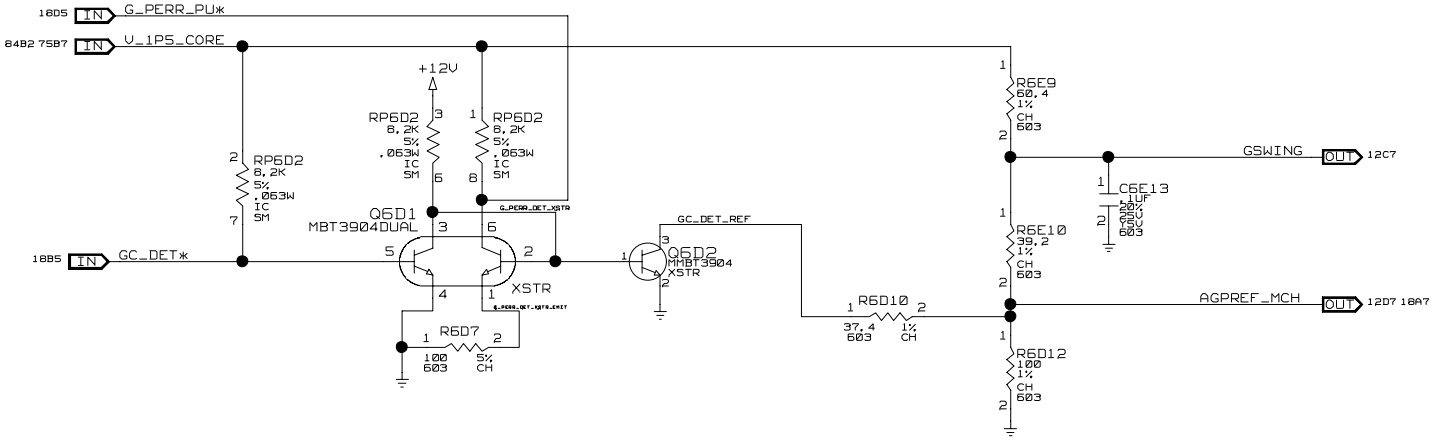
DRAWING
CANTERWOOD_CRB.SCH_1.19
Thu Apr 03 14:02:18 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE:		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 19/103

CR-20

SPARE





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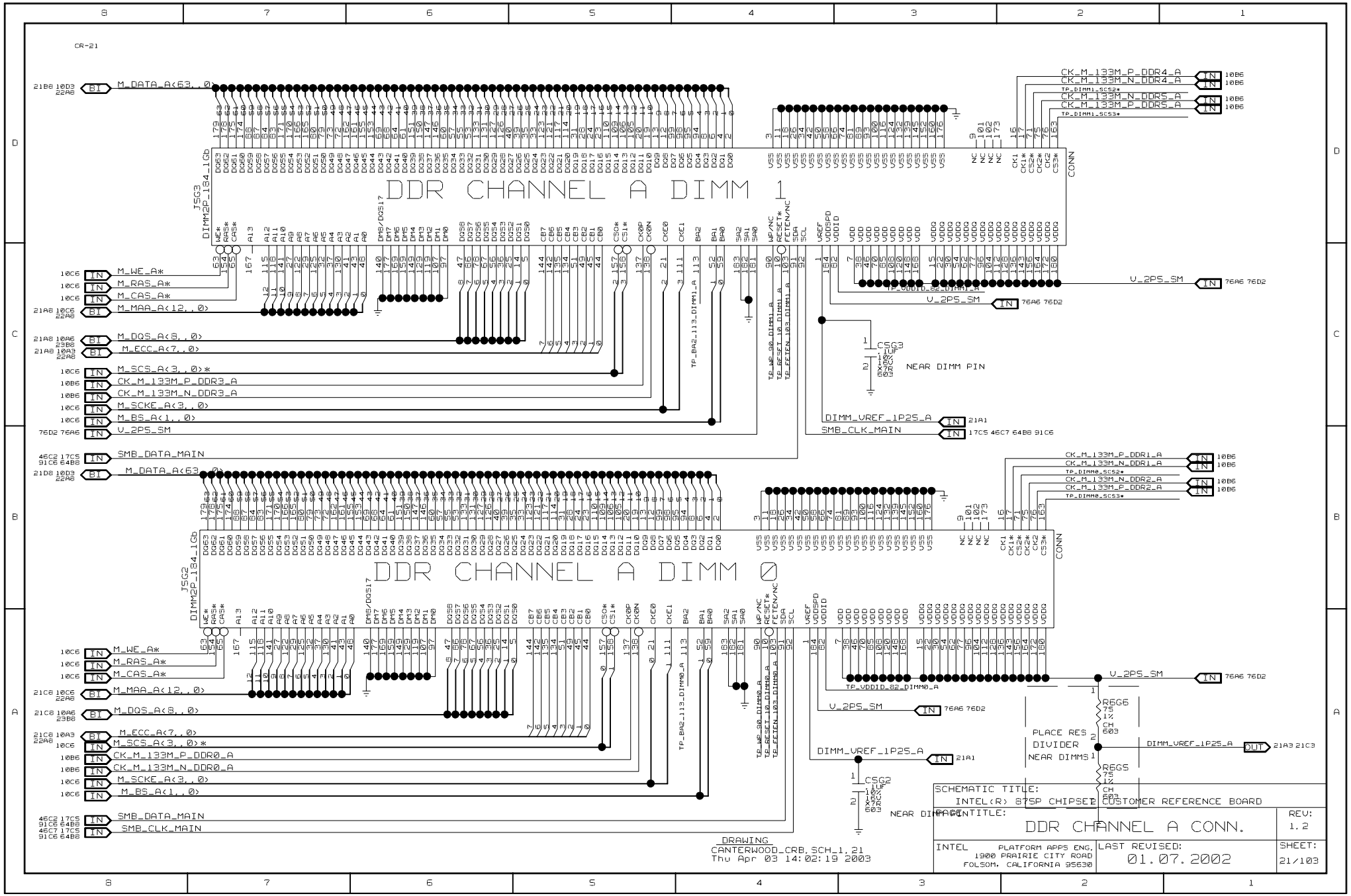
Thu Apr 03 14:02:18 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AGP SWING AND VREF		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 20/103


DDR CHANNEL A DIMM 1
DDR CHANNEL A DIMM 0
DDR CHANNEL A CONN.
M_DATA_A<63,,0>
M_WE_A*
M_RAS_A*
M_CAS_A*
M_MAA_A<12,,0>
M_DQS_A<8,,0>
M_ECC_A<7,,0>
M_SCS_A<3,,0>*
CK_M_133M_P_DDR3_A
CK_M_133M_N_DDR3_A
M_SCKE_A<3,,0>
M_BS_A<1,,0>
V_2PS_SM
SMB_DATA_MAIN
SMB_CLK_MAIN
DIMM_VREF_1P25S_A
NEAR DIMM PIN
PLACE RES DIVIDER NEAR DIMMS
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET
CUSTOMER REFERENCE BOARD
PAGE TITLE:
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
REV:
1.2
SHEET:
21/103
DRAWING
CANTERWOOD_CRB.SCH_1,21
Thu Apr 03 14:02:19 2003

CR-22

DDR CHANNEL A

DDR RESISTOR TERMINATION

SPARE SECTIONS

76A6 IN V_1P25_MEMVTT

SPARE RPACKS

TP_RP20D2_1 — RP3G2 — 4 47 5 — 5% .063W SM IC

TP_RP2105_2 — RP5G4 — 3 56 6 — 5% .063W SM IC

TP_RP2105_3 — RP5G2 — 1 56 8 — 5% .063W SM IC

TP_RP2105_5 — RP3G4 — 2 56 7 — 5% .063W SM IC

TP_RP4G1_2 — RP4G3 — 2 47 7 — 5% .063W SM IC

TP_RP2G6_4 — RP2G6 — 4 56 5 — 5% .063W SM IC

76A6 IN V_1P25_MEMVTT

RPG3G1 — 0 4 5 — 5% .063W SM IC

RPG3G1 — 1 2 7 — 5% .063W SM IC

RPG3G2 — 2 4 5 — 5% .063W SM IC

RPG3G2 — 3 2 7 — 5% .063W SM IC

RP3G1 — 4 1 8 — 5% .063W SM IC

RPG3G1 — 5 3 6 — 5% .063W SM IC

RPG3G2 — 6 3 6 — 5% .063W SM IC

RPG3G2 — 7 1 8 — 5% .063W SM IC

RP2G7 — 63 3 6 — 5% .063W SM IC

RP2G7 — 62 4 5 — 5% .063W SM IC

RP2G5 — 61 1 8 — 5% .063W SM IC

RP2G5 — 60 2 7 — 5% .063W SM IC

RP2G7 — 59 2 7 — 5% .063W SM IC

RP2G7 — 58 1 8 — 5% .063W SM IC

RP2G6 — 57 2 7 — 5% .063W SM IC

RP2G6 — 56 3 6 — 5% .063W SM IC

RP2G4 — 55 1 8 — 5% .063W SM IC

RP2G4 — 54 2 7 — 5% .063W SM IC

RP2G4 — 53 4 5 — 5% .063W SM IC

RP2G3 — 52 1 8 — 5% .063W SM IC

RP2G5 — 51 3 6 — 5% .063W SM IC

RP2G5 — 50 4 5 — 5% .063W SM IC

RP2G3 — 49 2 7 — 5% .063W SM IC

RP2G3 — 48 3 6 — 5% .063W SM IC

RP2G3 — 47 4 5 — 5% .063W SM IC

RP2G2 — 46 1 8 — 5% .063W SM IC

R2G1 2 — 45 1 2 — 56 603 5% CH

RP3G5 — 44 2 7 — 5% .063W SM IC

RP2G2 — 43 2 7 — 5% .063W SM IC

RP2G2 — 42 3 6 — 5% .063W SM IC

R2G2 2 — 41 1 2 — 56 603 5% CH

RP3G5 — 40 1 8 — 5% .063W SM IC

RP3G5 — 39 4 5 — 5% .063W SM IC

RP3G4 — 38 1 8 — 5% .063W SM IC

RP3G3 — 37 1 8 — 5% .063W SM IC

RP3G3 — 36 3 6 — 5% .063W SM IC

RP3G5 — 35 3 6 — 5% .063W SM IC

RP3G4 — 34 3 6 — 5% .063W SM IC

RP3G3 — 33 2 7 — 5% .063W SM IC

RP3G3 — 32 4 5 — 5% .063W SM IC

RP3G1 — 31 2 7 — 5% .063W SM IC

RP4G5 — 30 1 8 — 5% .063W SM IC

RP4G5 — 29 3 6 — 5% .063W SM IC

RP4G5 — 28 4 5 — 5% .063W SM IC

RP3G1 — 27 3 6 — 5% .063W SM IC

RP3G1 — 26 4 5 — 5% .063W SM IC

RP4G4 — 25 1 8 — 5% .063W SM IC

RP4G4 — 24 2 7 — 5% .063W SM IC

RP4G4 — 23 4 5 — 5% .063W SM IC

R4G8 2 — 22 1 2 — 56 603 5% CH

RP4G2 — 21 2 7 — 5% .063W SM IC

R4G3 2 — 20 1 2 — 56 603 5% CH

RP4G4 — 19 3 6 — 5% .063W SM IC

R4G7 2 — 18 1 2 — 56 603 5% CH

RP4G2 — 17 3 6 — 5% .063W SM IC

RP4G2 — 16 4 5 — 5% .063W SM IC

RP5G3 — 15 3 6 — 5% .063W SM IC

RP5G3 — 14 4 5 — 5% .063W SM IC

RP5G2 — 13 2 7 — 5% .063W SM IC

RP5G2 — 12 4 5 — 5% .063W SM IC

RP5G3 — 11 1 8 — 5% .063W SM IC

RP5G3 — 10 2 7 — 5% .063W SM IC

RP5G1 — 9 4 5 — 5% .063W SM IC

RP5G1 — 8 1 8 — 5% .063W SM IC

RP5G1 — 7 3 6 — 5% .063W SM IC

RP5G4 — 6 1 8 — 5% .063W SM IC

RP5G5 — 5 2 7 — 5% .063W SM IC

RP5G5 — 4 3 6 — 5% .063W SM IC

RP5G1 — 3 2 7 — 5% .063W SM IC

RP5G4 — 2 2 7 — 5% .063W SM IC

RP5G5 — 1 1 8 — 5% .063W SM IC

RP5G5 — 0 4 5 — 5% .063W SM IC

R4G4 — 12 1 2 — 47 603 5% CH

R4G5 — 11 1 2 — 47 603 5% CH

RP3G2 — 10 2 7 — 47 SM 5% .063W IC

R4G6 — 9 1 2 — 47 603 5% CH

RP4G3 — 8 3 5 — 47 SM 5% .063W IC

RP4G3 — 7 4 5 — 47 SM 5% .063W IC

R4G9 — 6 1 2 — 47 603 5% CH

RP4G3 — 5 1 8 — 47 SM 5% .063W IC

R4G1 2 — 4 1 2 — 47 603 5% CH

R4G2 2 — 3 1 2 — 47 603 5% CH

R3G1 2 — 2 1 2 — 47 603 5% CH

R3G2 2 — 1 1 2 — 47 603 5% CH

RP3G2 — 0 3 6 — 47 SM 5% .063W IC

21CB 10A3 21A8 BI M_ECC_A<7..0>

21DB 10D3 21B8 BI M_DATA_A<63..0>

21CB 10C5 21A8 BI M_MAA_A<12..0>

DRAWING
CANTERWOOD_CRB.SCH_1.22
Thu Apr 03 14:02:41 2003

SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: DDR CHAN A TERM

REV: 1.2

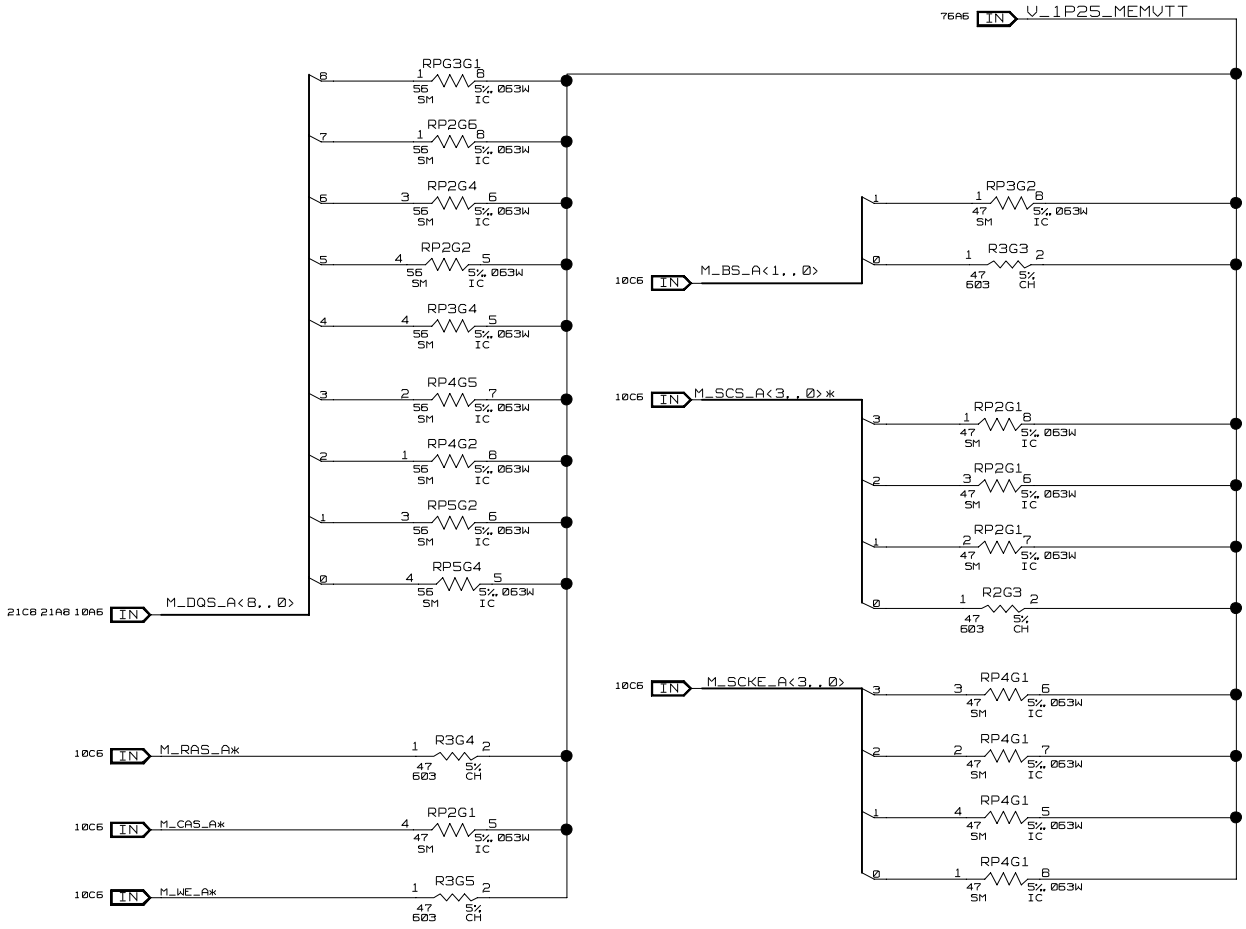
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: 01.07.2002

SHEET: 22/103

CR-23

DDR CHANNEL A

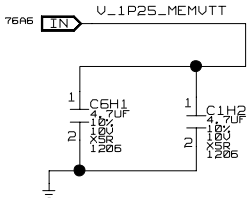


DRAWING
CANTERWOOD_CRB.SCH_1.23
Thu Apr 03 14:02:41 2003

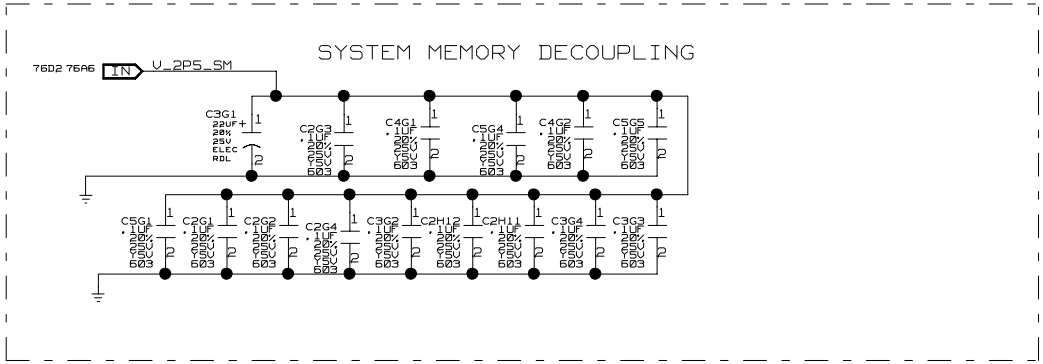
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: DDR CHAN A TERM		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 23/103

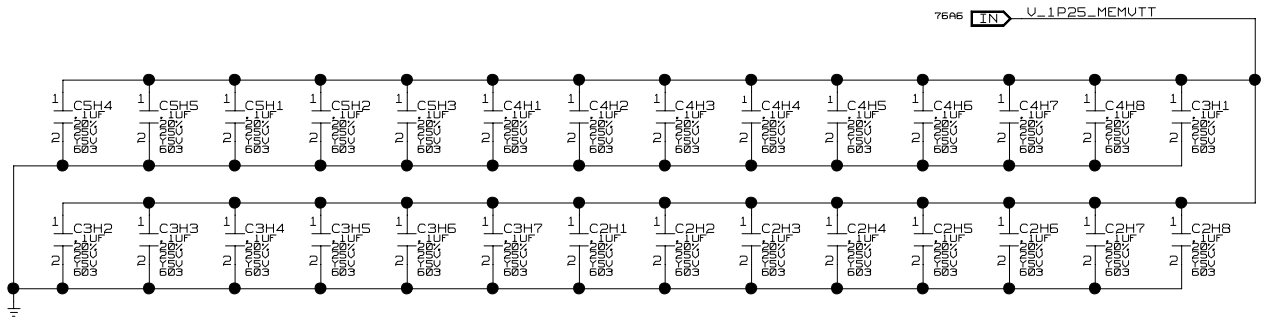
CR-24

DDR CHANNEL A



PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND

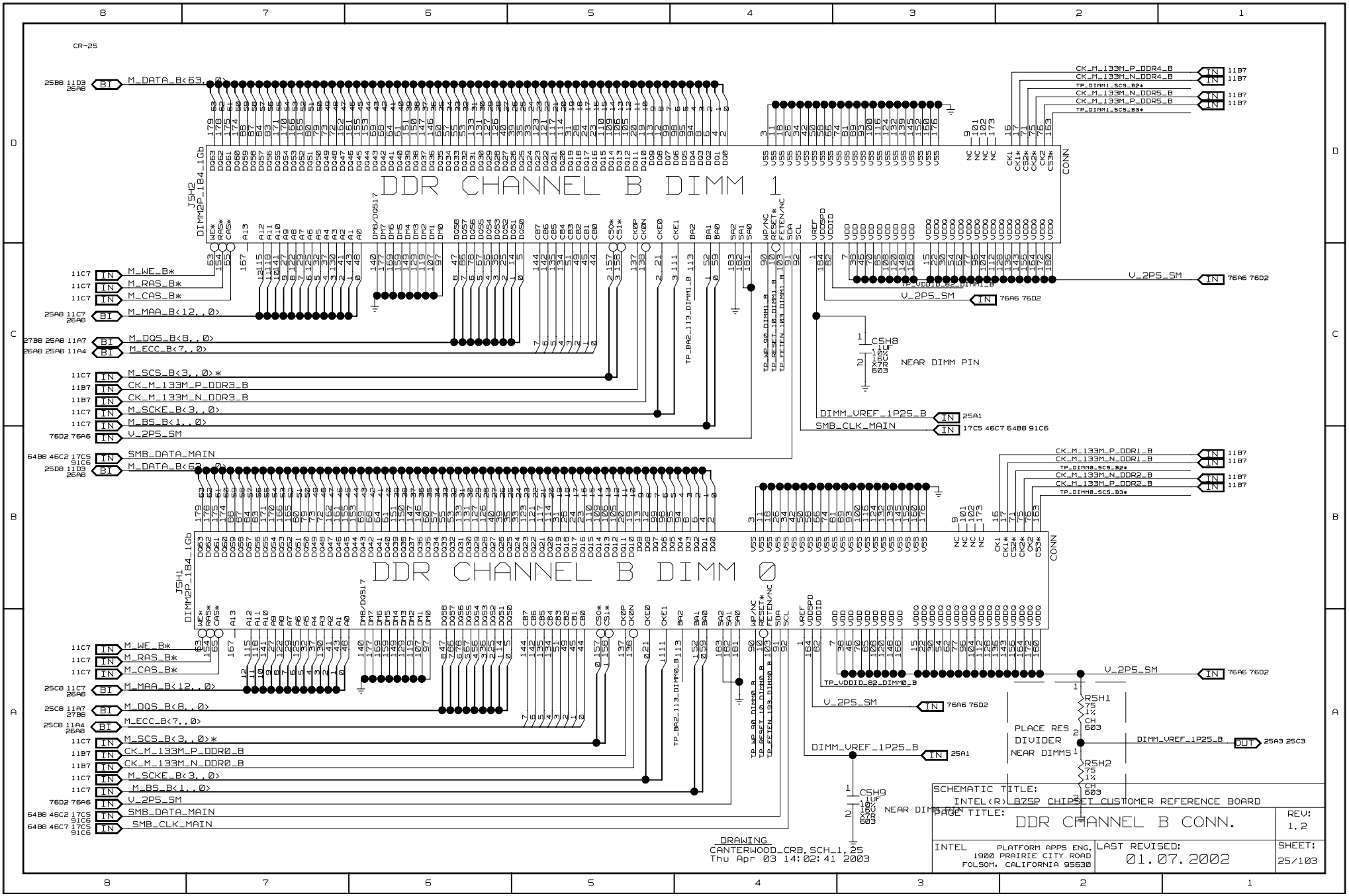




DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

DRAWING
CANTERWOOD_CRB.SCH,1,24
Thu Apr 03 14:02:41 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: DDR CHAN A VTERM DECOUPLING		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 24/103

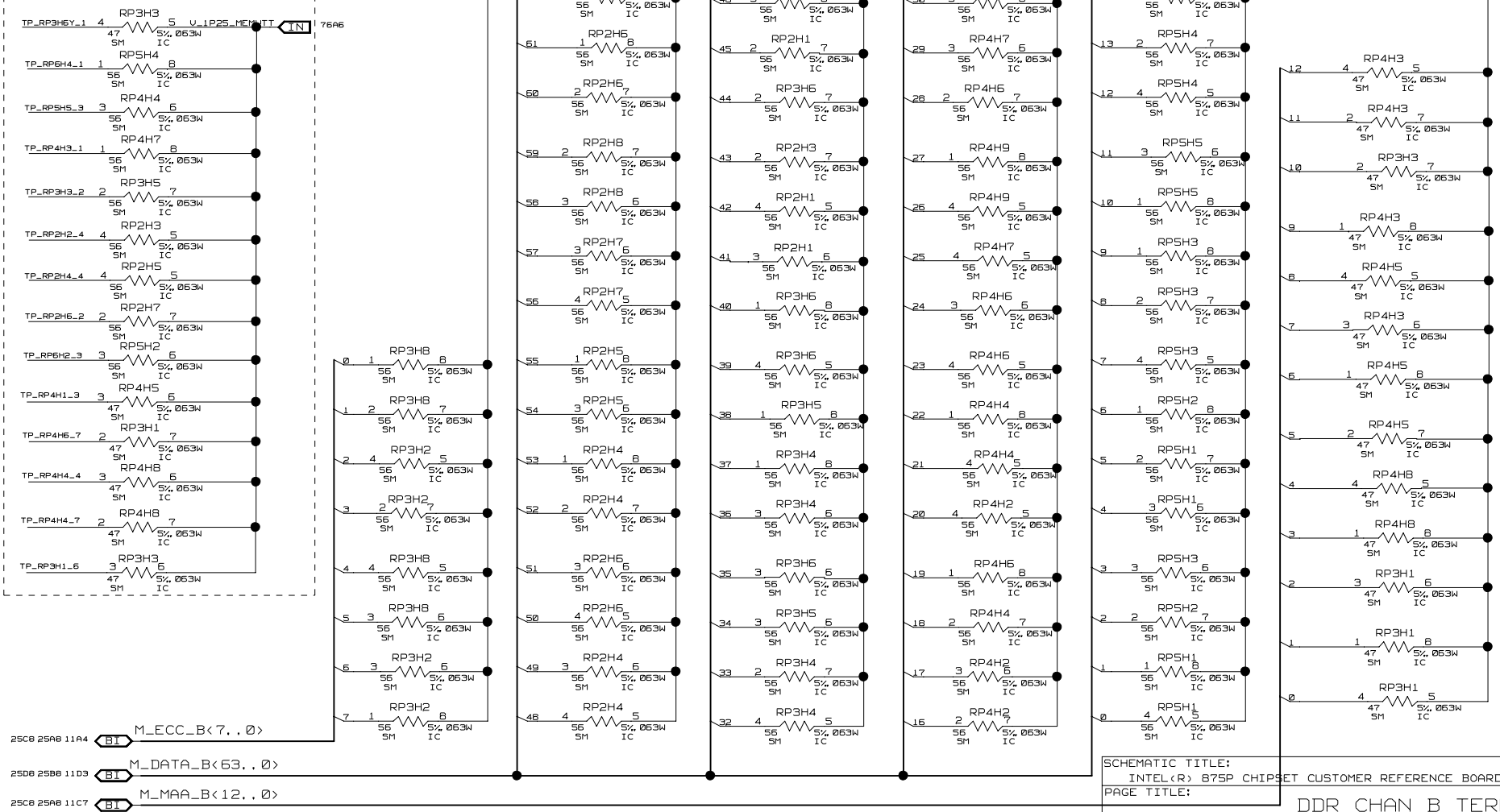

DDR CHANNEL B DIMM 1
DDR CHANNEL B DIMM 0
M_DATA_B<63..0>
M_WE_B*
M_RAS_B*
M_CAS_B*
M_MAA_B<12..0>
M_DQS_B<8..0>
M_ECC_B<7..0>
M_SCS_B<3..0>*
CK_M_133M_P_DDR3_B
CK_M_133M_N_DDR3_B
M_SCKE_B<3..0>
M_BS_B<1..0>
V_2P5_SM
SMB_DATA_MAIN
SMB_CLK_MAIN
DIMM_VREF_1P25_B
CK_M_133M_P_DDR4_B
CK_M_133M_N_DDR4_B
CK_M_133M_N_DDR5_B
CK_M_133M_P_DDR5_B
CK_M_133M_P_DDR1_B
CK_M_133M_N_DDR1_B
CK_M_133M_N_DDR2_B
CK_M_133M_P_DDR2_B
C5H8
C5H9
R5H1
R5H2
NEAR DIMM PIN
PLACE RES DIVIDER NEAR DIMMS
DRAWING
CANTERWOOD_CRB.SCH_1.25
Thu Apr 03 14:02:41 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
DDR CHANNEL B CONN.
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
25/103

CR-26

DDR CHANNEL B

DDR RESISTOR TERMINATION

SPARE SECTIONS

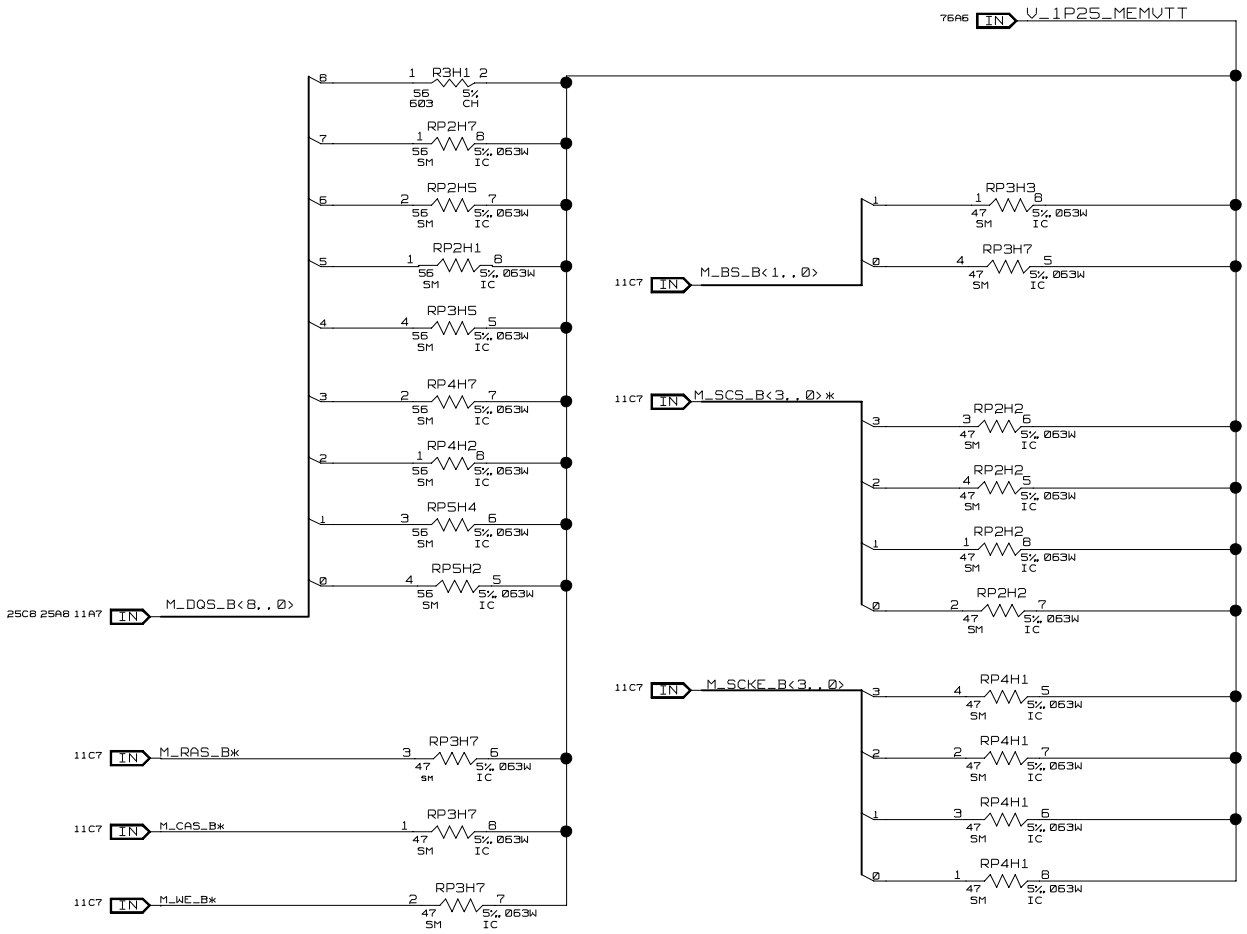


DRAWING
CANTERWOOD_CRB.SCH_1.26
Thu Apr 03 14:02:42 2003

SCHEMATIC TITLE: INTEL<R> 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: DDR CHAN B TERM		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 26/103

CR-27

DDR CHANNEL B

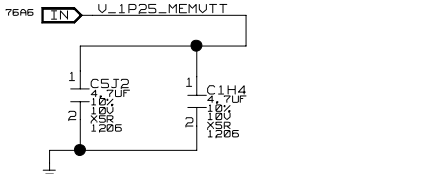


DRAWING
CANTERWOOD_CRB.SCH_1,27
Thu Apr 03 14:02:42 2003

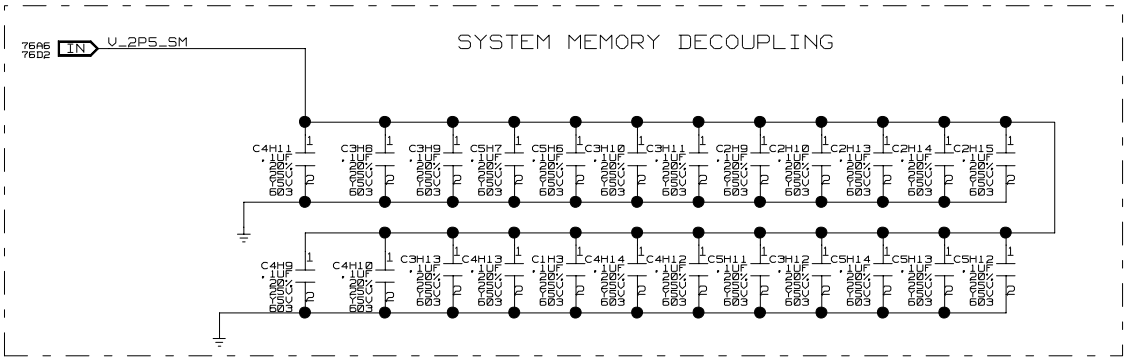
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: DDR CHAN B TERM		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 27/103

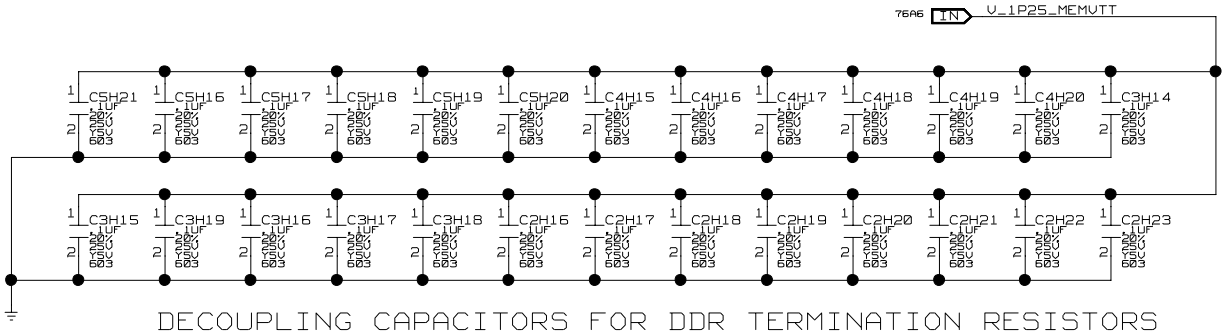
CR-28

DDR CHANNEL B



PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND

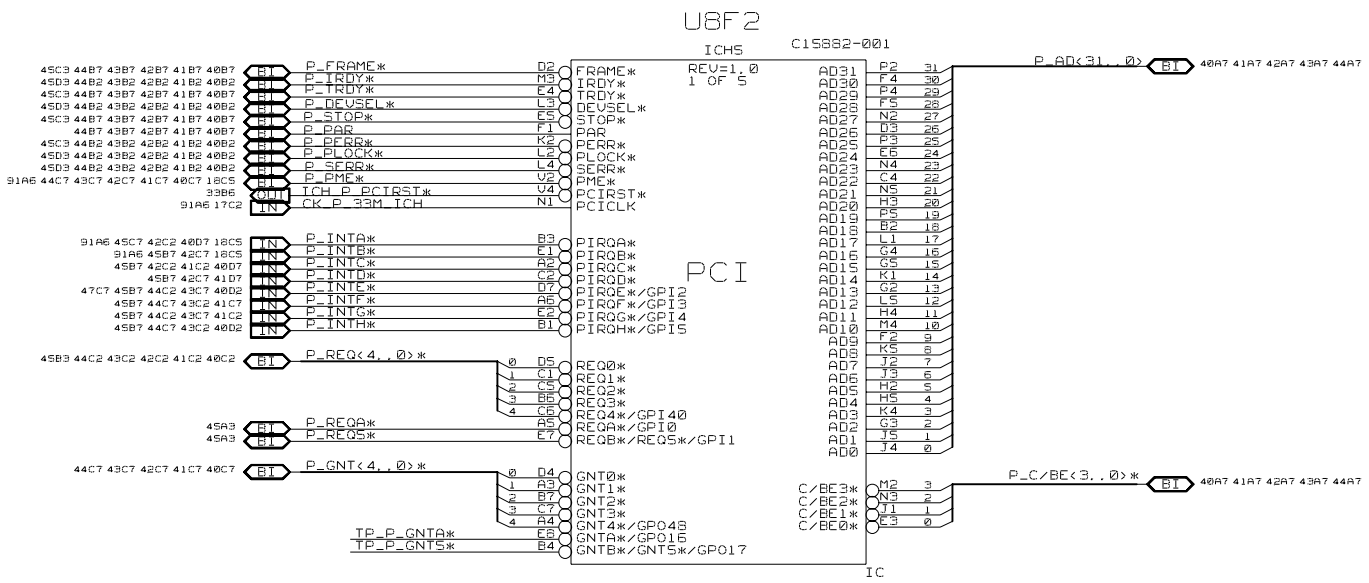


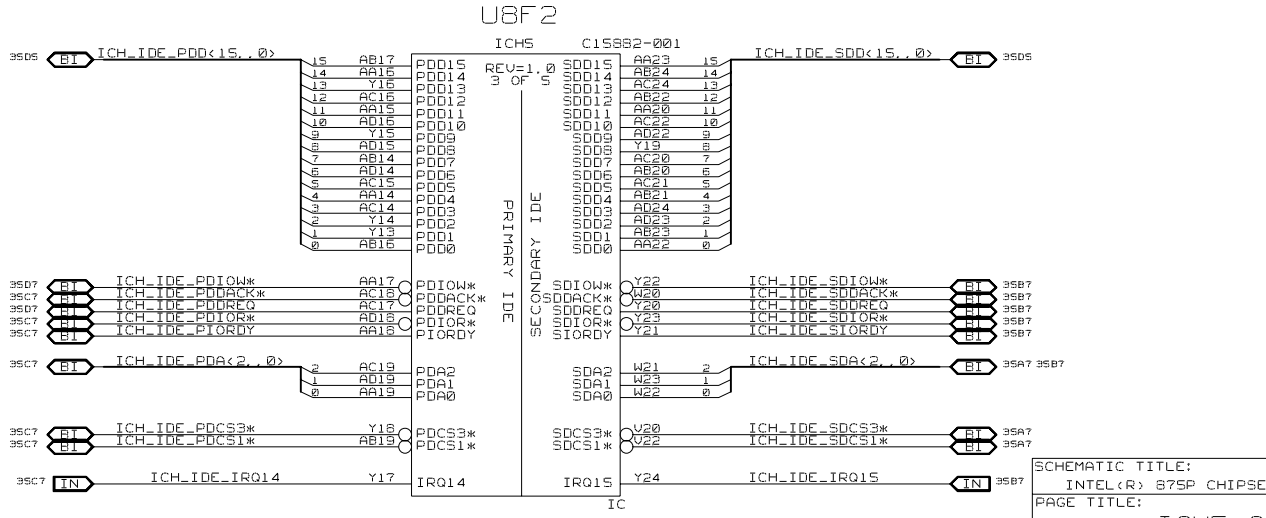


DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

DRAWING
CANTERWOOD_CRB.SCH_1.28
Thu Apr 03 14:02:42 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: DDR CHAN B VTERM DECOUPLING		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 28/103





DRAWING
CANTERWOOD_CRB.SCH_1.29
Thu Apr 03 14:02:42 2003

SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
ICH5: CHIPSET 1 OF 4

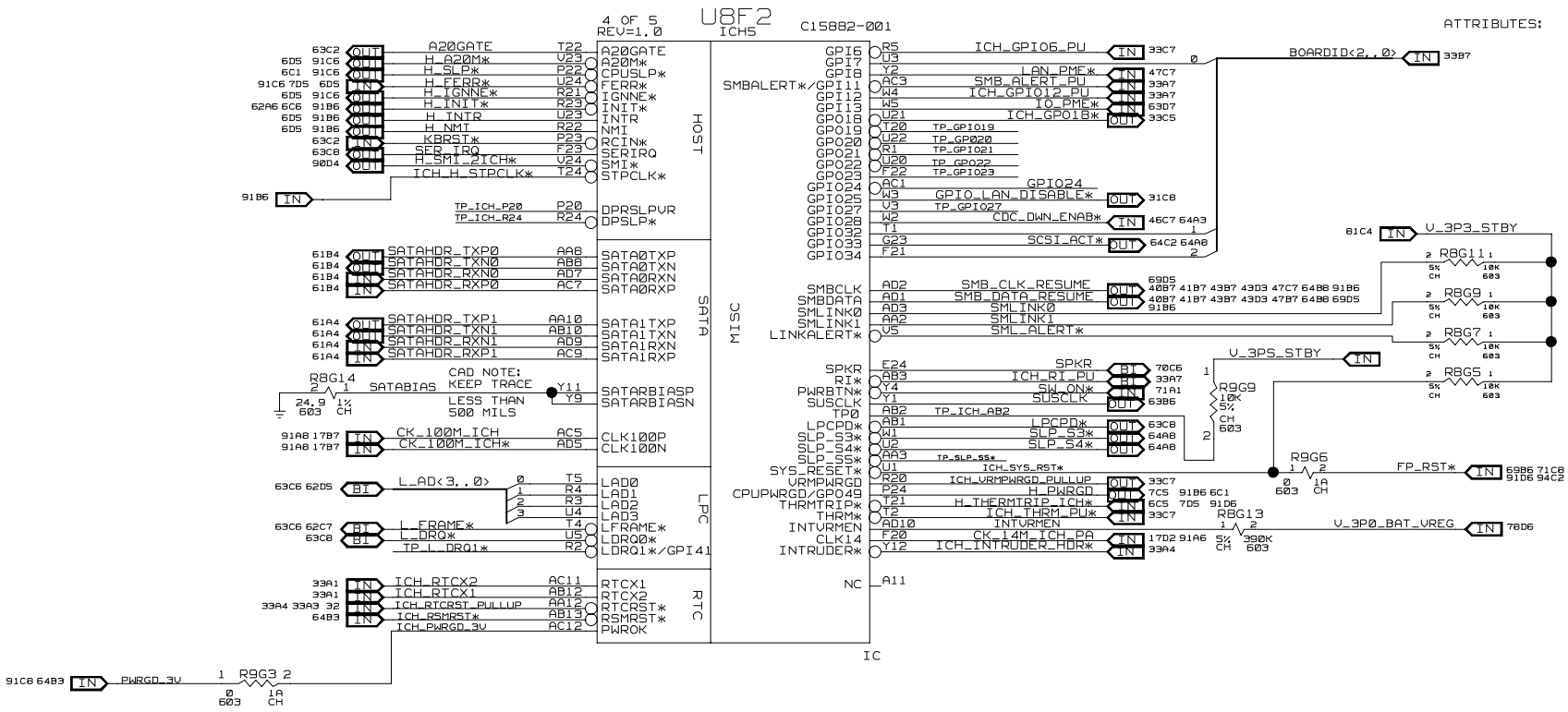
REV: 1.2

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED:
01.07.2002

SHEET:
29/103

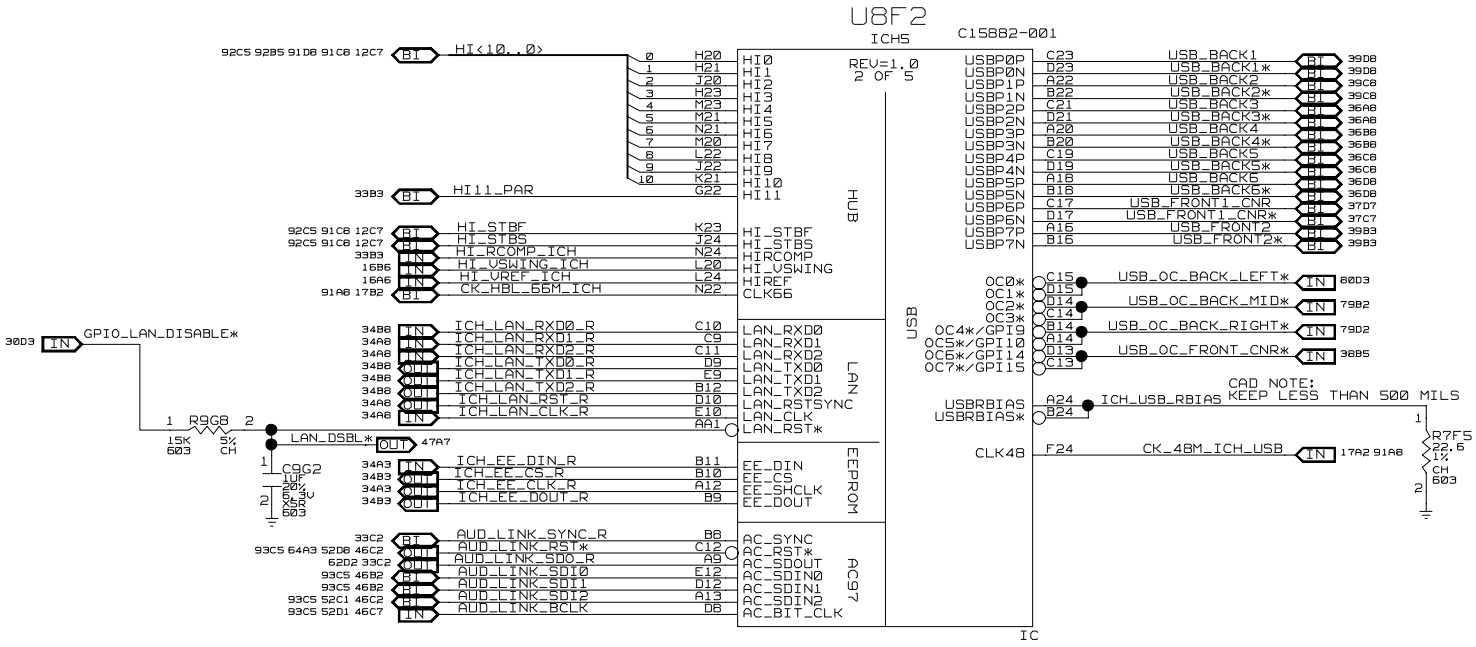
[PAGE_TITLE=ICH5_PCI_IDE]



DRAWING
CANTERWOOD_CRB.SCH_1.30
Thu Apr 03 14:02:42 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: ICH5: CHIPSET 2 OF 4		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 30/103

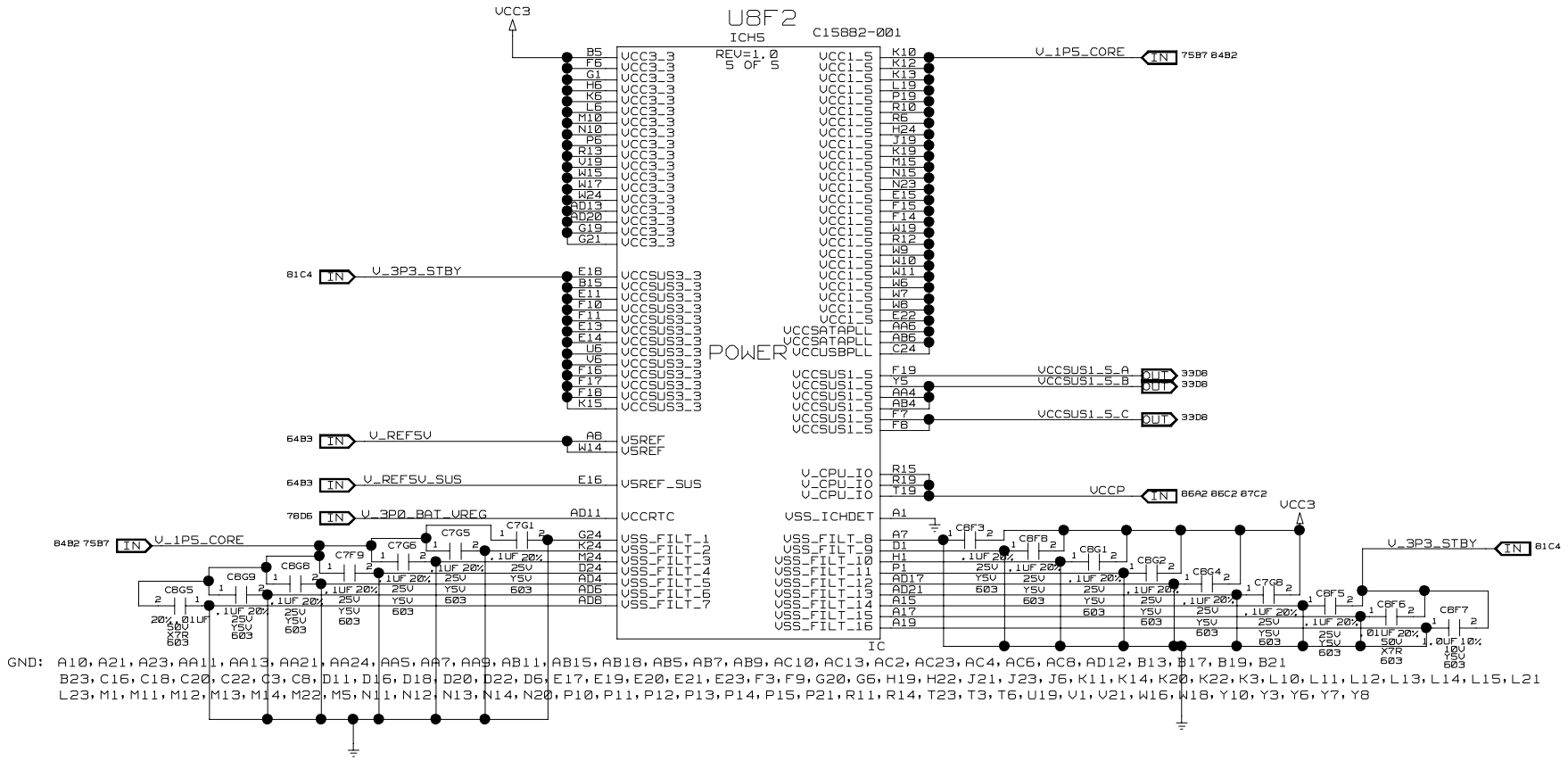
[PAGE_TITLE=ICH5_HOST_SATA_LPC_RTC_MISC]



[PAGE_TITLE=ICH5_USB_HUB_LAN_AC97]

DRAWING
CANTERWOOD_CRB.SCH,1,31
Thu Apr 03 14:02:43 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: ICH5: CHIPSET 3 OF 4		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 31/103

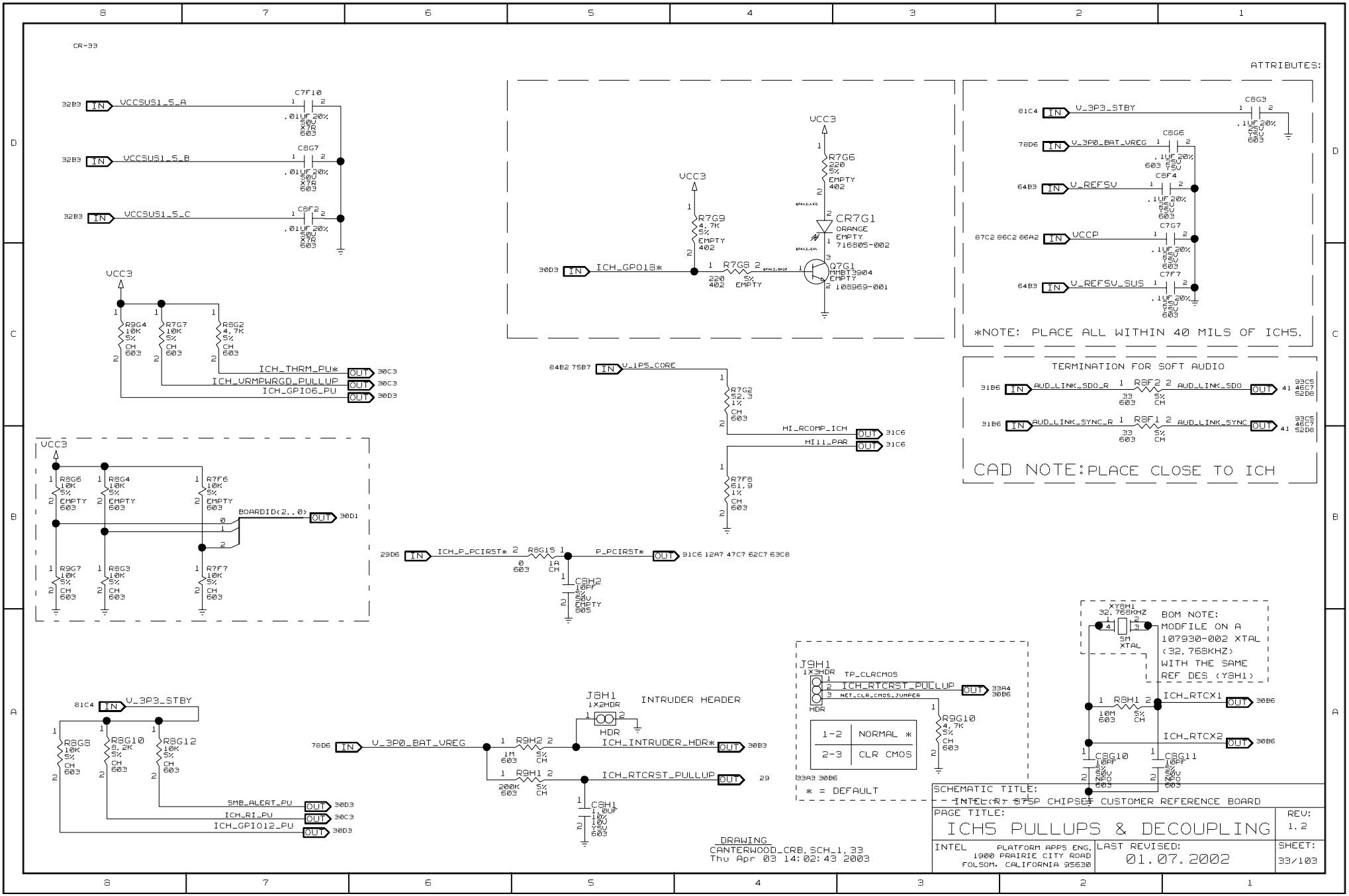


CR-32

[PAGE_TITLE=ICH5_PWR_GND]

DRAWING
CANTERWOOD_CRB.SCH_1.32
Thu Apr 03 14:02:43 2003

SCHEMATIC TITLE:	INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	ICH5: CHIPSET 4 OF 4
REV:	1.2
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	01.07.2002
SHEET:	32/103


CR-33
ATTRIBUTES:
VCCSUS1_5_A
VCCSUS1_5_B
VCCSUS1_5_C
C7F10
C8G7
C8F2
.01UF 20% X5R 0402 16V
VCC3
R8G4 10K 5% CH 603
R7G7 10K 5% CH 603
R8G2 4.7K 5% CH 603
ICH_THRM_PU*
ICH_VRMPWRGD_PULLUP
ICH_GPIO6_PU
R7G9 4.7K 5% EMPTY 402
R7G8 2 220 402 5% EMPTY
ICH_GPO18*
R7G6 220 5% EMPTY 402
CR7G1 ORANGE EMPTY 716805-002
Q7G1 MMBT3904 EMPTY 1085969-001
V_3P3_STBY
V_3P0_BAT_VREG
V_REFSV
VCCP
V_REFSV_SUS
C8G3
C8G6
C8F4
C7G7
C7F7
.1UF 20% Y5V 0603 16V
*NOTE: PLACE ALL WITHIN 40 MILS OF ICH5.
V_1PS_CORE
R7G2 52.3 1% CH 603
HI_RCOMP_ICH
HI11_PAR
R7F8 61.9 1% CH 603
TERMINATION FOR SOFT AUDIO
AUD_LINK_SDO_R
AUD_LINK_SDO
AUD_LINK_SYNC_R
AUD_LINK_SYNC
R8F2 33 603 5% CH
R8F1 33 603 5% CH
CAD NOTE: PLACE CLOSE TO ICH
R8G6 10K 5% EMPTY 603
R8G4 10K 5% EMPTY 603
R7F6 10K 5% EMPTY 603
BOARDID<2..0>
R8G7 10K 5% CH 603
R8G3 10K 5% CH 603
R7F7 10K 5% CH 603
ICH_P_PCIRST*
R8G15 0 603 1A CH
P_PCIRST*
C8H2 10PF 50V CERAMIC EMPTY 005
R8G8 10K 5% CH 603
R8G10 2.2K 5% CH 603
R8G12 10K 5% CH 603
SMB_ALERT_PU
ICH_RI_PU
ICH_GPIO12_PU
J8H1 1X2HDR HDR
INTRUDER HEADER
R9H2 1M 603 5% CH
R9H1 200K 603 5% CH
ICH_INTRUDER_HDR*
ICH_RTCRST_PULLUP
C8H1 1.0UF 10V 10% X5R 0603
J9H1 1X3HDR HDR
TP_CLRCMOS
ICH_RTCRST_PULLUP
NET_CLR_CMOS_JUMPER
1-2 NORMAL *
2-3 CLR CMOS
* = DEFAULT
R9G10 4.7K 5% CH 603
XY8H1 32.768KHZ SM XTAL
BOM NOTE:
MODFILE ON A
107930-002 XTAL
(32.768KHZ)
WITH THE SAME
REF DES (Y8H1)
R8H1 10M 603 5% CH
ICH_RTCX1
ICH_RTCX2
C8G10 10PF 50V CERAMIC 0603
C8G11 10PF 50V CERAMIC 0603
SCHEMATIC TITLE:
INTEL® 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
ICH5 PULLUPS & DECOUPLING
REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED: 01.07.2002
SHEET: 33/103
DRAWING
CANTERWOOD_CRB.SCH_1.33
Thu Apr 03 14:02:43 2003

CR-34

PROPERTIES FOR STUFFING OPTIONS: BOM= CNR_LINK_LAN
CNR STUFFING OPTION FOR LAN-UP SOLUTION

TO CNR

RP8F5 3 6 33 SM 5% .063W IC — ICH_LAN_TXD0_CNR — OUT 46D2
RP8F5 1 8 33 SM 5% .063W IC — ICH_LAN_TXD1_CNR — OUT 46D7
RP8F6 2 7 33 SM 5% .063W IC — ICH_LAN_TXD2_CNR — OUT 46D2
RP8F6 4 5 33 SM 5% .063W IC — ICH_LAN_RXD0_CNR — IN 46C7
RP8F5 2 7 33 SM 5% .063W IC — ICH_LAN_RXD1_CNR — IN 46C2
RP8F6 3 6 33 SM 5% .063W IC — ICH_LAN_RXD2_CNR — IN 46C7
RP8F6 1 8 33 SM 5% .063W IC — ICH_LAN_RST_CNR — OUT 46D7
RP8F5 4 5 33 SM 5% .063W IC — ICH_LAN_CLK_CNR — IN 46D2

TO CNR

RP8F2 2 7 0 SM 5% .063W IC — ICH_EE_CS_CNR — OUT 46C2
RP8F2 1 8 0 SM 5% .063W IC — ICH_EE_DOUT_CNR — OUT 46C2
RP8F2 3 6 0 SM 5% .063W IC — ICH_EE_DIN_CNR — IN 46C7
RP8F2 4 5 0 SM 5% .063W IC — ICH_EE_CLK_CNR — OUT 46C7

0-OHMS ARE PROVIDED TO MINIMIZE STUBS ON LAN INTERFACE

PROPERTIES FOR STUFFING OPTIONS: BOM= LAN_LINK_CNR

FROM ICH5

31C6 IN ICH_LAN_TXD0_R — RP8F3 2 7 33 SM EMPTY 5% .063W — ICH_LAN_TXD0_KIN — OUT 47C3
31C6 IN ICH_LAN_TXD1_R — RP8F3 4 5 33 SM EMPTY 5% .063W — ICH_LAN_TXD1_KIN — OUT 47C3
31C6 IN ICH_LAN_TXD2_R — RP8F4 3 6 33 SM EMPTY 5% .063W — ICH_LAN_TXD2_KIN — OUT 47C3
31C6 OUT ICH_LAN_RXD0_R — RP8F4 1 8 33 SM EMPTY 5% .063W — ICH_LAN_RXD0_KIN — IN 47A7
31C6 OUT ICH_LAN_RXD1_R — RP8F3 3 6 33 SM EMPTY 5% .063W — ICH_LAN_RXD1_KIN — IN 47A7
31C6 OUT ICH_LAN_RXD2_R — RP8F4 2 7 33 SM EMPTY 5% .063W — ICH_LAN_RXD2_KIN — IN 47A7
31B6 IN ICH_LAN_RST_R — RP8F4 4 5 33 SM EMPTY 5% .063W — ICH_LAN_RST_KIN — OUT 47C3
31B6 OUT ICH_LAN_CLK_R — RP8F3 1 8 33 SM EMPTY 5% .063W — ICH_LAN_CLK_KIN — IN 47A7

TO LAN (KINNERETH-R)

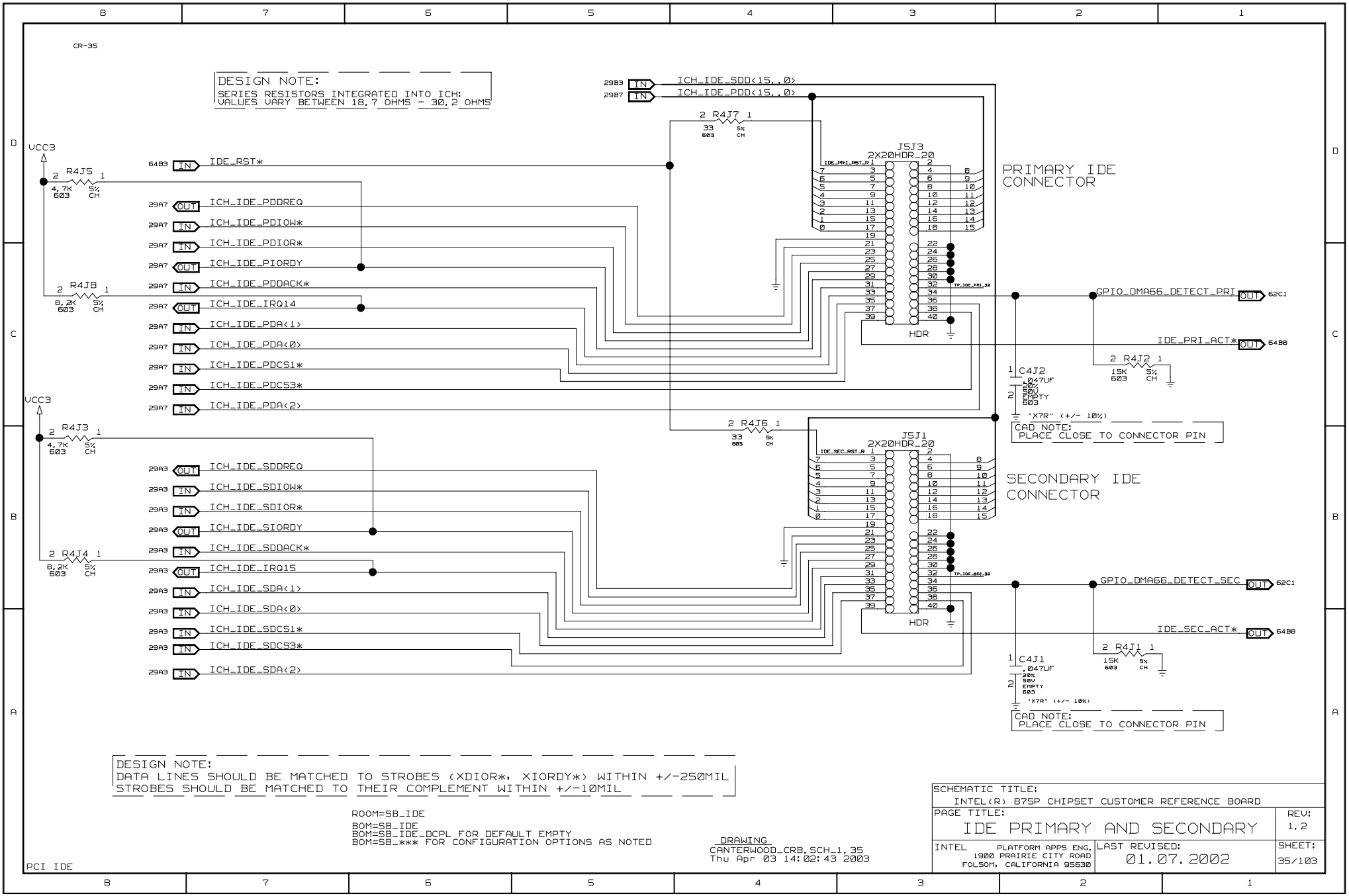
FROM ICH5

31B6 IN ICH_EE_CS_R — RP8F1 3 6 0 SM EMPTY 5% .063W — LAN_EECS — OUT 49B8
31B6 IN ICH_EE_DOUT_R — RP8F1 4 5 0 SM EMPTY 5% .063W — LAN_EEDO — OUT 49B8
31B6 OUT ICH_EE_DIN_R — RP8F1 2 7 0 SM EMPTY 5% .063W — LAN_EEDI — IN 49B8
31B6 IN ICH_EE_CLK_R — RP8F1 1 8 0 SM EMPTY 5% .063W — LAN_EESK — OUT 49B8

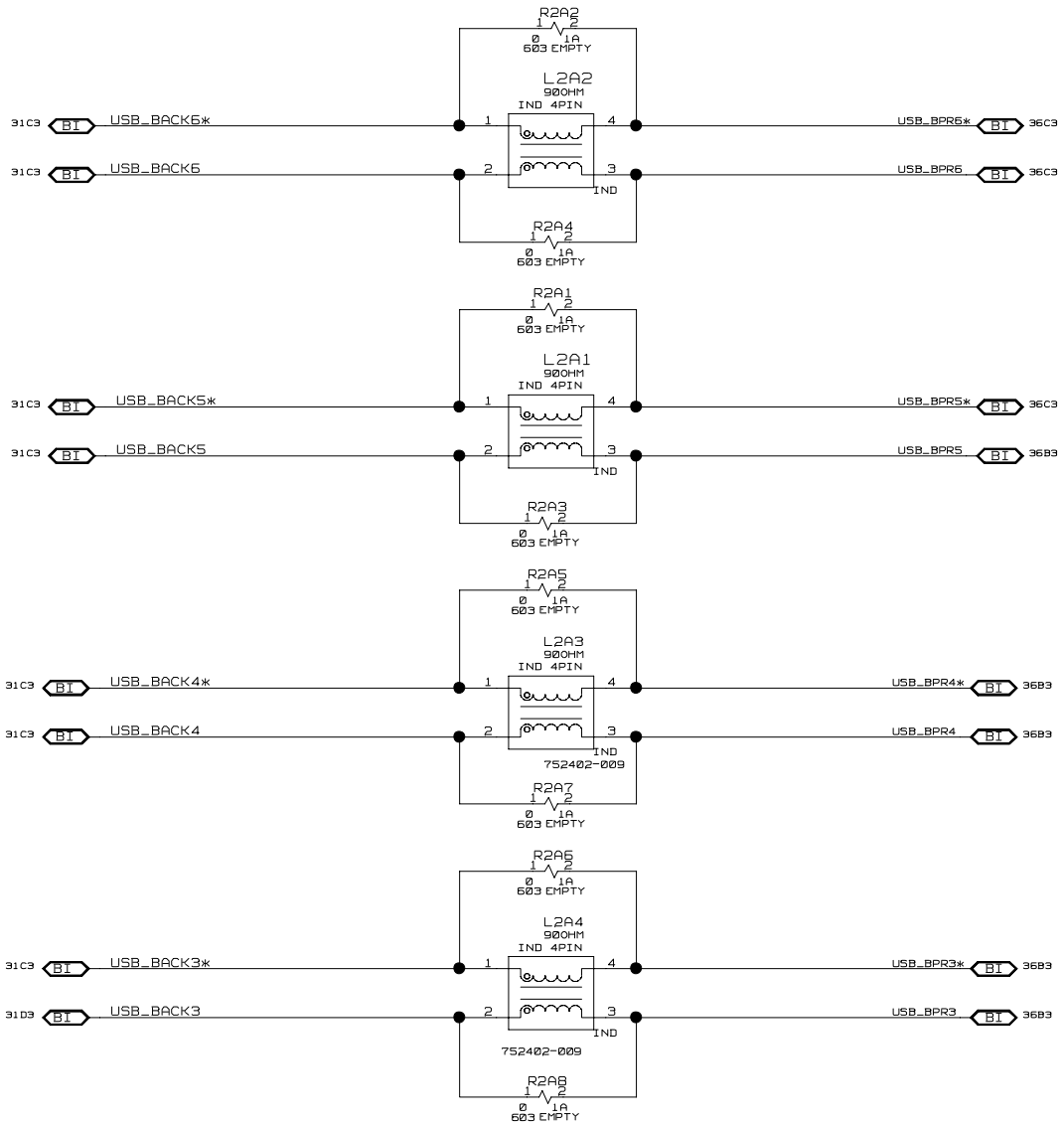
TO LAN EEPROMS

DRAWING
CANTERWOOD_CRB.SCH_1.34
Thu Apr 03 14:02:43 2003

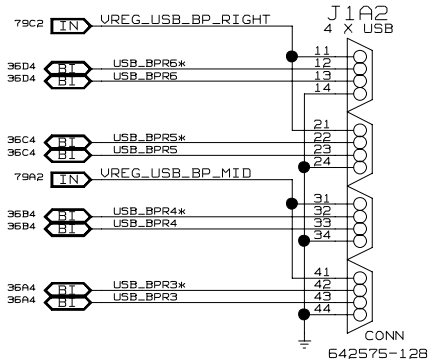
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: LAN-ON-CNR STUFFING OPTION PAGE		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 34/103


CR-35
DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS
ICH_IDE_SDD<15..0>
ICH_IDE_PDD<15..0>
PRIMARY IDE CONNECTOR
SECONDARY IDE CONNECTOR
IDE_RST*
ICH_IDE_PDDREQ
ICH_IDE_PDIOW*
ICH_IDE_PDIOR*
ICH_IDE_PIORDY
ICH_IDE_PDDACK*
ICH_IDE_IRQ14
ICH_IDE_PDA<1>
ICH_IDE_PDA<0>
ICH_IDE_PDCS1*
ICH_IDE_PDCS3*
ICH_IDE_PDA<2>
ICH_IDE_SDDREQ
ICH_IDE_SDIOW*
ICH_IDE_SDIOR*
ICH_IDE_SIORDY
ICH_IDE_SDDACK*
ICH_IDE_IRQ15
ICH_IDE_SDA<1>
ICH_IDE_SDA<0>
ICH_IDE_SDCS1*
ICH_IDE_SDCS3*
ICH_IDE_SDA<2>
GPIO_DMA66_DETECT_PRI
IDE_PRI_ACT*
GPIO_DMA66_DETECT_SEC
IDE_SEC_ACT*
CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN
DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL
ROOM=SB_IDE
BOM=SB_IDE
BOM=SB_IDE_DCPL FOR DEFAULT EMPTY
BOM=SB_*** FOR CONFIGURATION OPTIONS AS NOTED
DRAWING
CANTERWOOD_CRB.SCH_1.35
Thu Apr 03 14:02:43 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
IDE PRIMARY AND SECONDARY
REV:
1.2
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
35/103
PCI IDE

CR-36



QUAD STACK USB



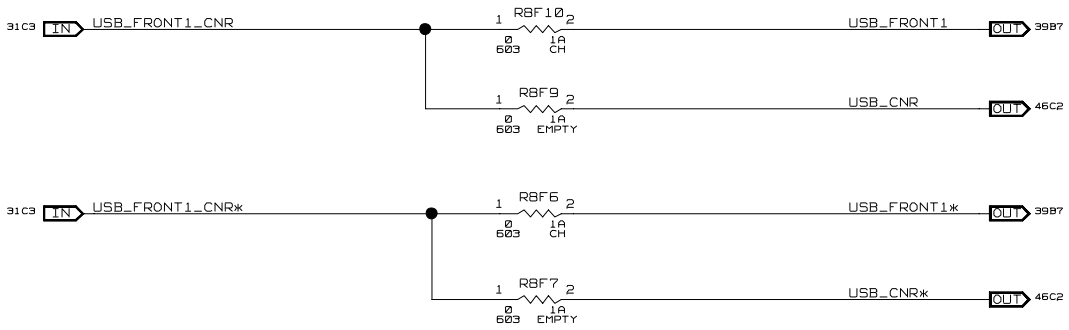
DRAWING
CANTERWOOD_CRB.SCH_1,36
Thu Apr 03 14:02:44 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: BACKPANEL_USB_RIGHT AND MID		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 36/103

CR-37

USB SWITCH

USB OPTION FOR FRONT PANEL OR CNR



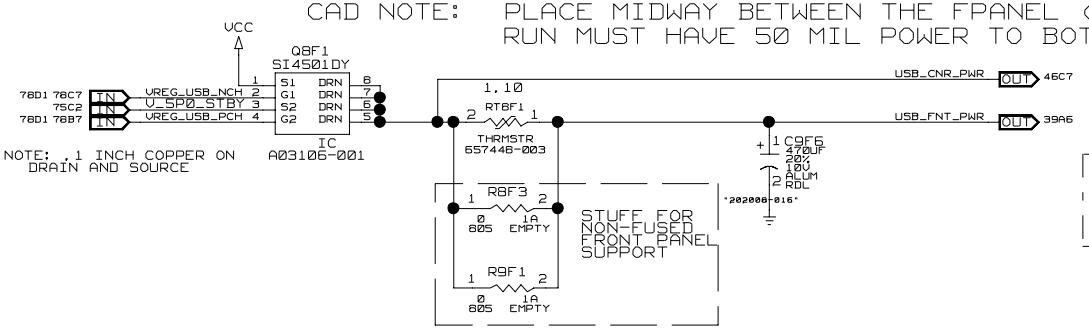
DRAWING
CANTERWOOD_CRB.SCH_1.37
Thu Apr 03 14:02:44 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: USB OPTION FOR FP		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 37/103

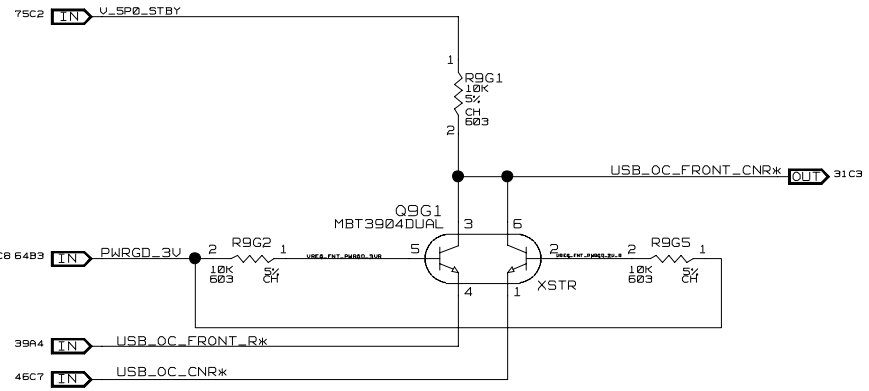
CR-38

CAD NOTE;
TRACE ROUTING IS 7.5 MIL, 7 MIL SPACING

CAD NOTE: PLACE MIDWAY BETWEEN THE FPANEL (2X5) & INTERNAL HEADERS
RUN MUST HAVE 50 MIL POWER TO BOTH LOCATIONS.



NOTE:
RPD ASSUMES FPANEL CARD HAS THERM & PROVIDES OC#

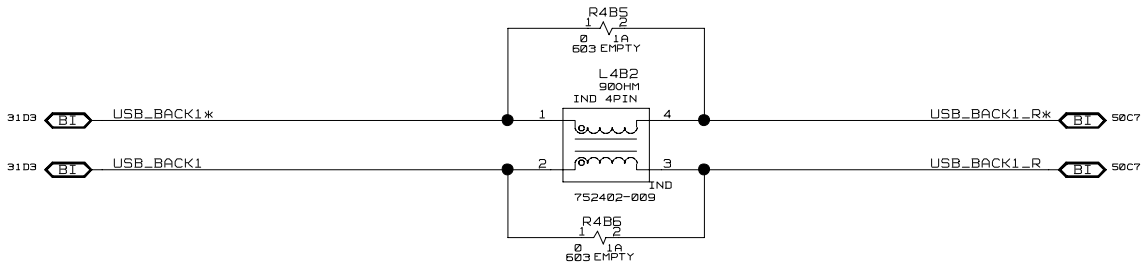


DRAWING
CANTERWOOD_CRB.SCH_1,38
Thu Apr 03 14:02:44 2003

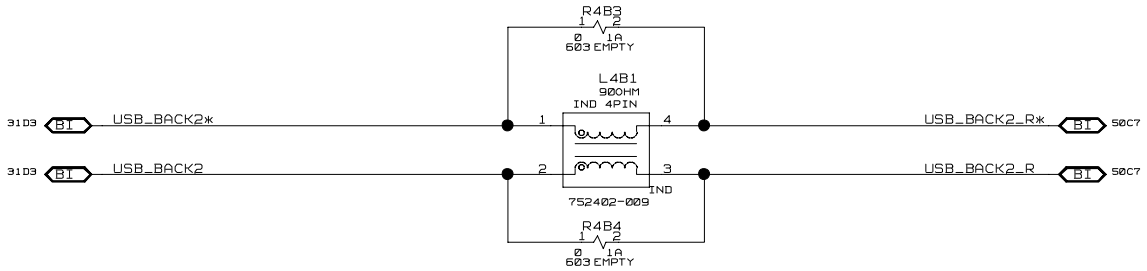
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: USB FNT PANEL POWER CNR VREG / OVER CURRENT		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 38/103

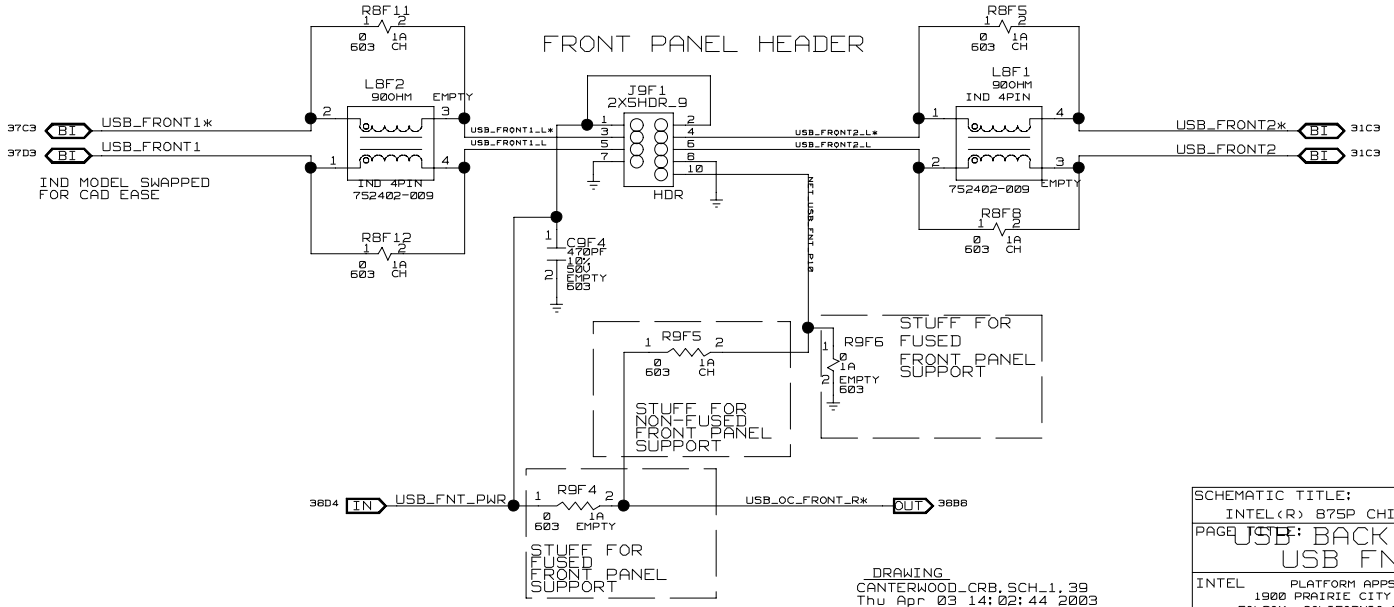
CR-39

CONNECTOR STUFFING OPTIONS:
RJ45/2 USB - A11509-001 (DEFAULT)
DOUBLE STACK USB - 642575-124



LAN/USB CONNECTOR (BACK PANEL LEFT)
CONNECTOR IS ON PAGE 49
WITH THE REST OF THE CONNECTOR





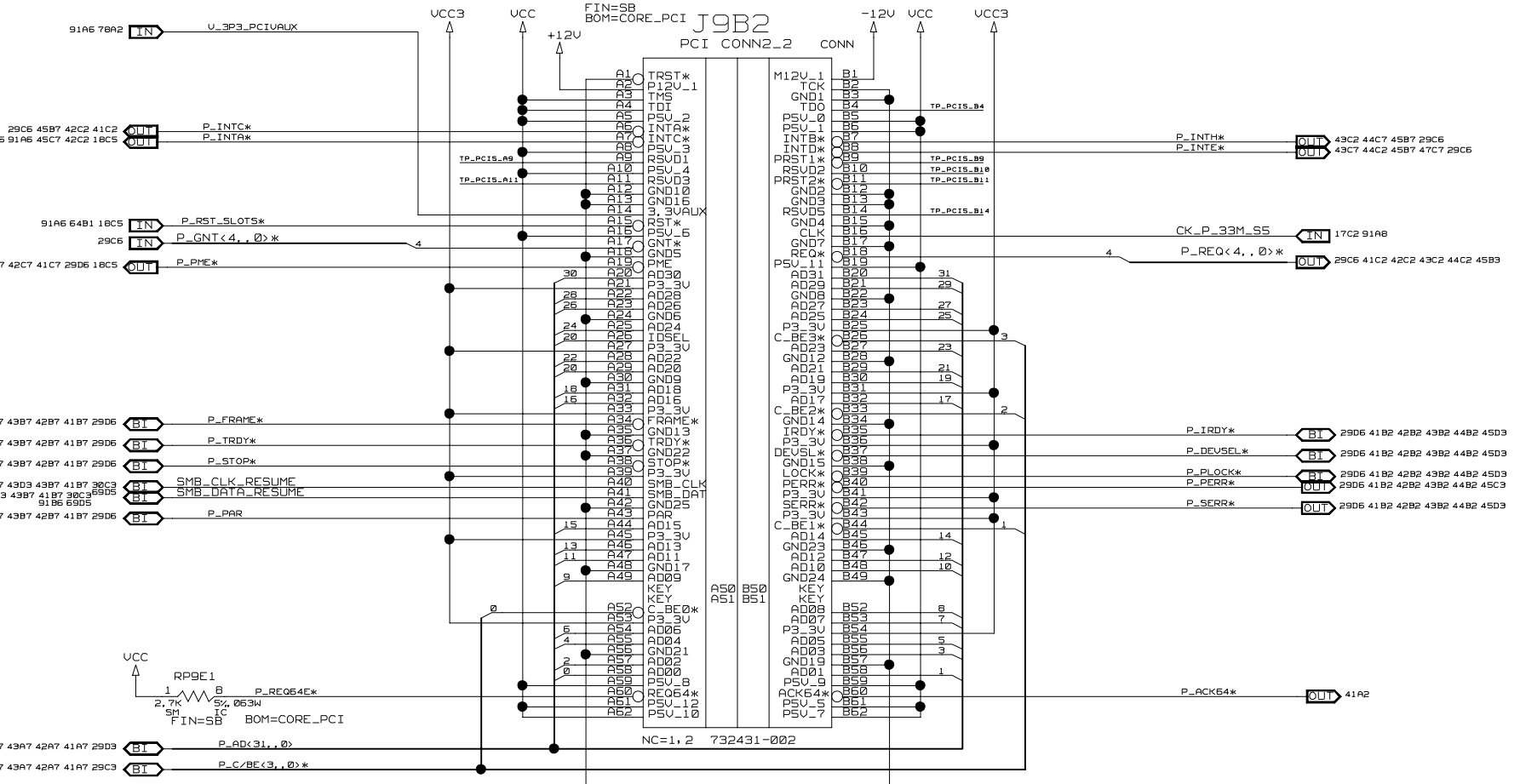
DRAWING
CANTERWOOD_CRB.SCH_1.39
Thu Apr 03 14:02:44 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: USB BACK PANEL LEFT CONN. USB FNT PANEL HEADER		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 39/103

CR-40

PCI SLOT 5
FURTHEST PCI SLOT FROM CPU

ATTRIBUTES:
BOM=CORE_PCI
ROOM=ICH_PCISLOT



SPARES

RP9E1
TP_2700_RP3 — 3 — 2.7K — 6 — TP_2700_RP6
5% .063W SM IC FIN=SB BOM=CORE_PCI

RP9E1
TP_2700_RP4 — 4 — 2.7K — 5 — TP_2700_RP5
5% .063W SM IC FIN=SB BOM=CORE_PCI

DESIGN NOTE:

PCI SLOT5 = PCI DEVICE FUNCTION 20H
= PCI DEVICE NUMBER 4H
= IDSEL VALUE AD20

[PAGE_TITLE=PCI_SLOT_5]

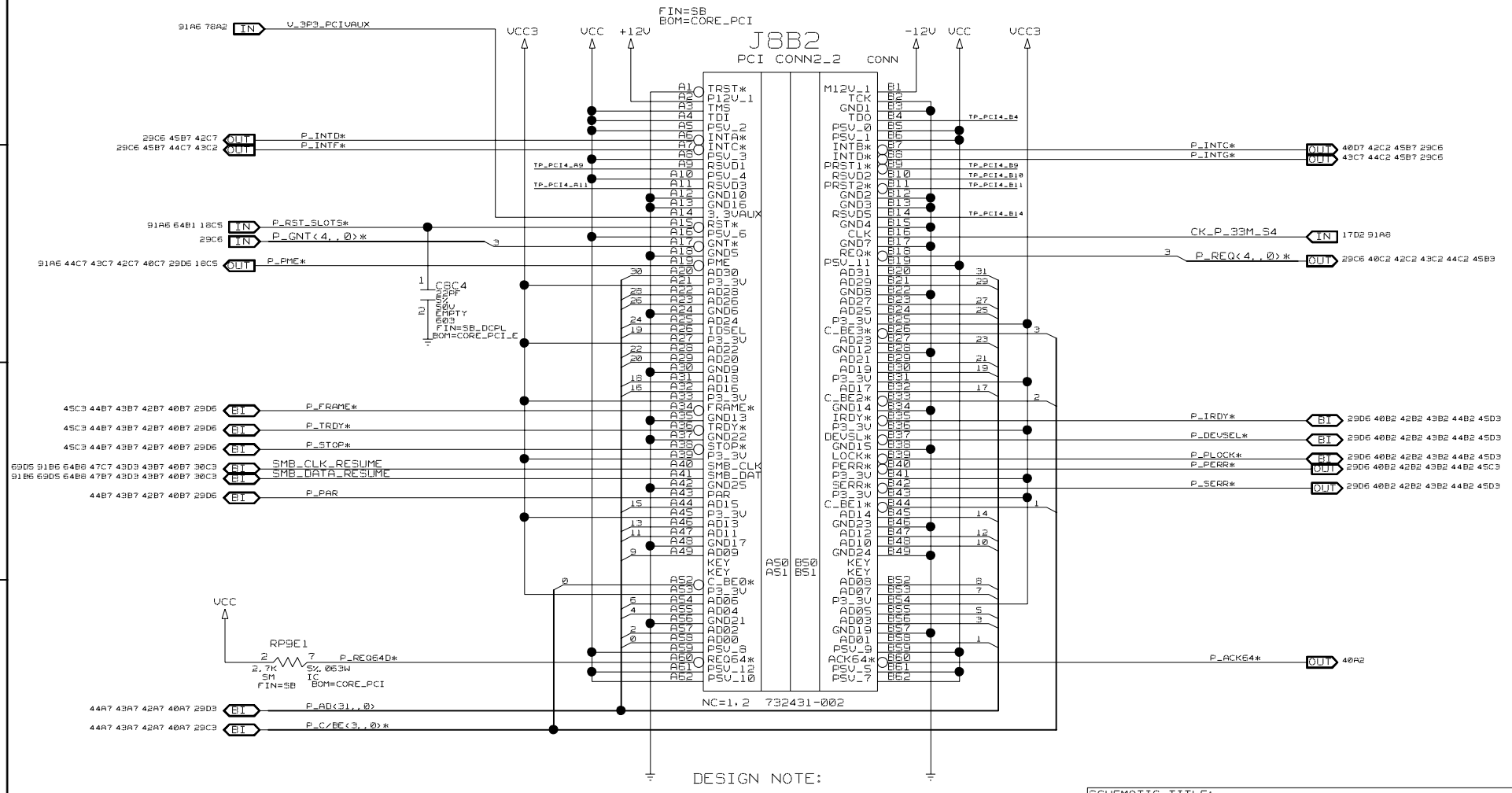
DRAWING
CANTERWOOD_CRB.SCH_1,40
Thu Apr 03 14:02:44 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 5		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 40/103

CR-41

PCI SLOT 4

ATTRIBUTES:
BOM=CORE_PCI
ROOM=ICH_PCISLOT



DESIGN NOTE:

PCI SLOT4 = PCI DEVICE FUNCTION 18H
= PCI DEVICE NUMBER 3H
= IDSEL VALUE AD19

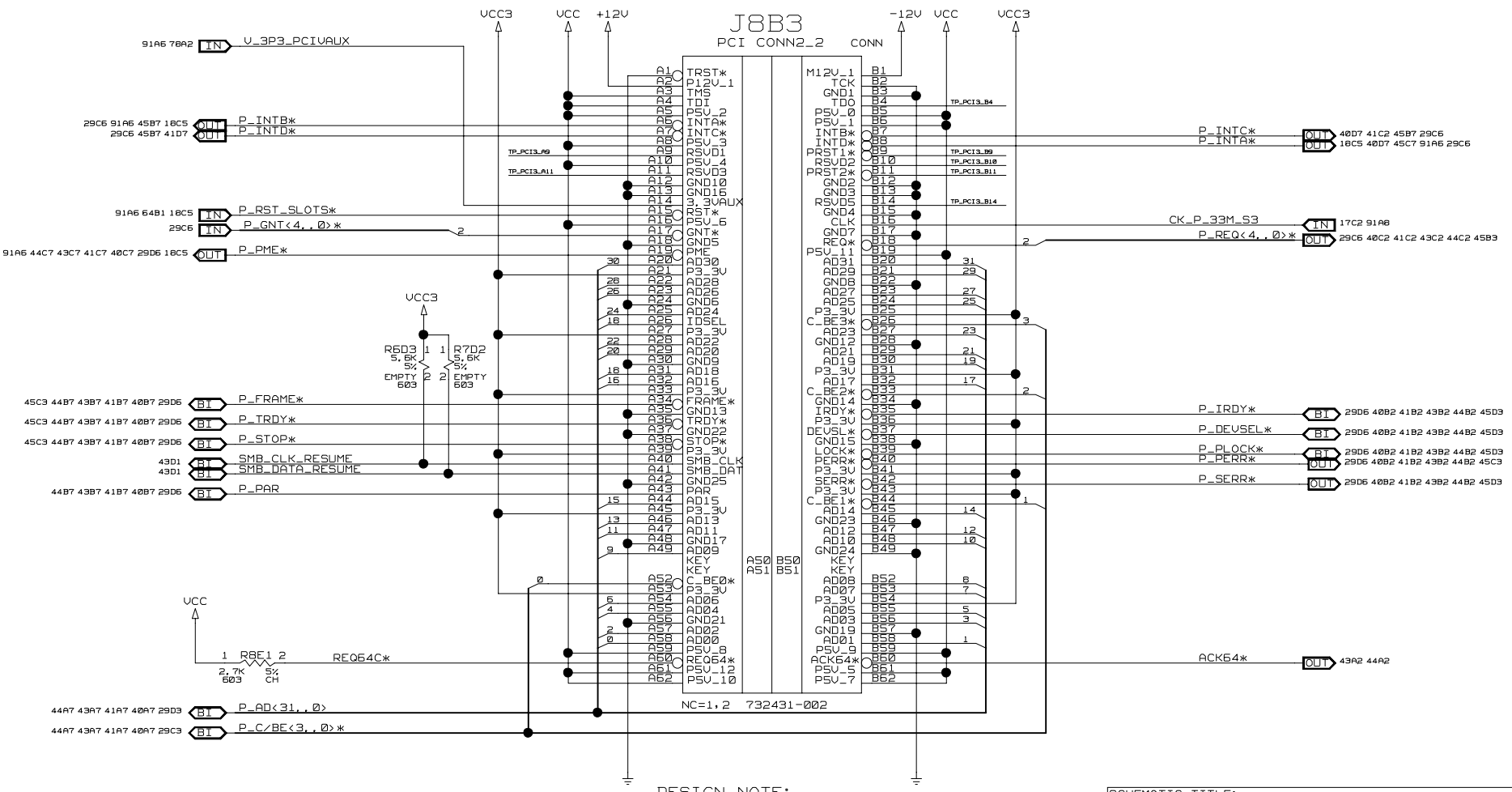
[PAGE_TITLE=PCI_SLOT_4]

DRAWING
CANTERWOOD_CRB.SCH_1.41
Thu Apr 03 14:02:44 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 4		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 41/103

CR-42

PCI SLOT 3



DESIGN NOTE:

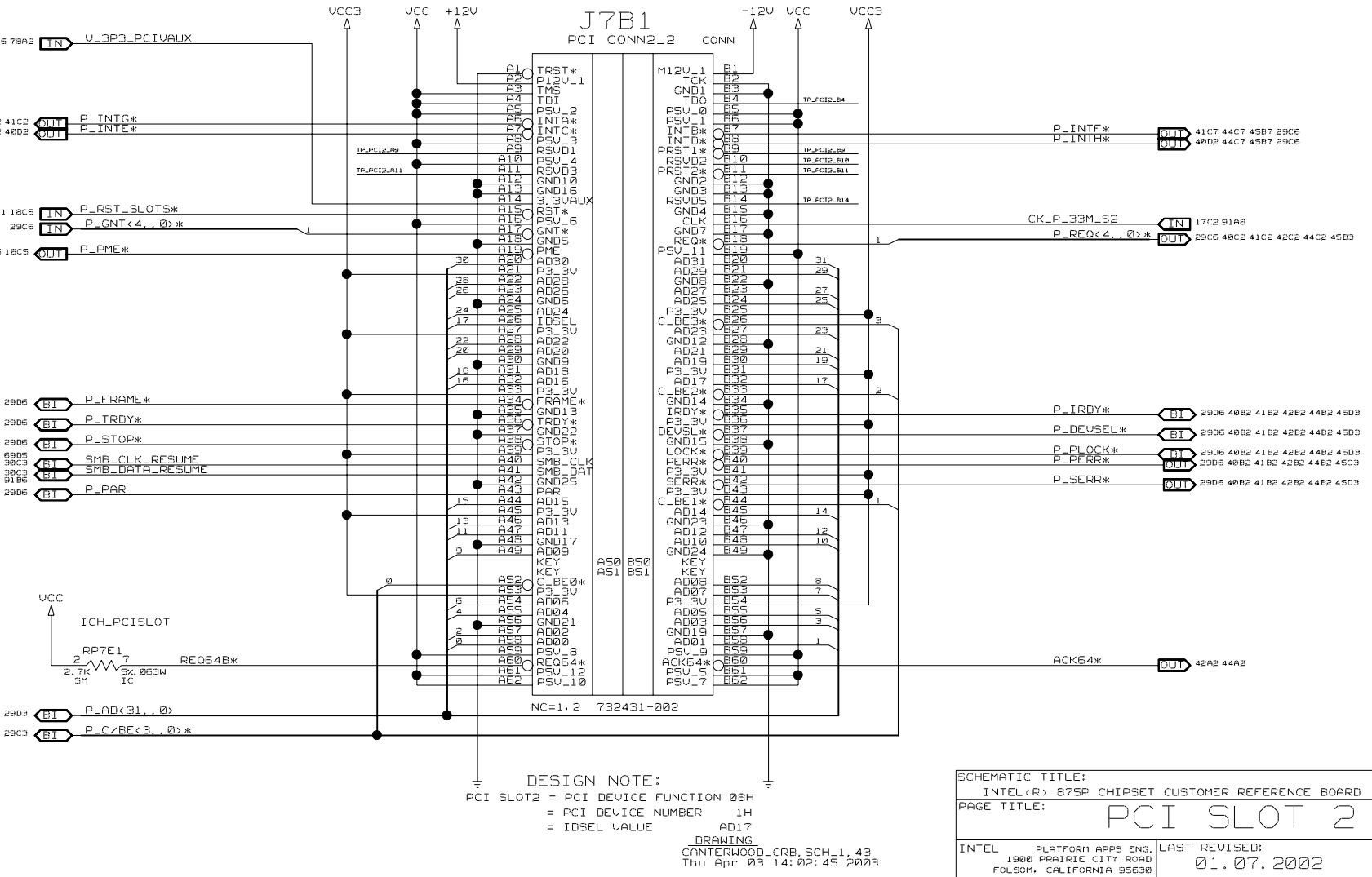
PCI SLOT3 = PCI DEVICE FUNCTION 10H
= PCI DEVICE NUMBER 2H
= IDSEL VALUE AD18

DRAWING
CANTERWOOD_CRB.SCH_1,42
Thu Apr 03 14:02:45 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 3		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 42/103

CR-43

PCI SLOT 2

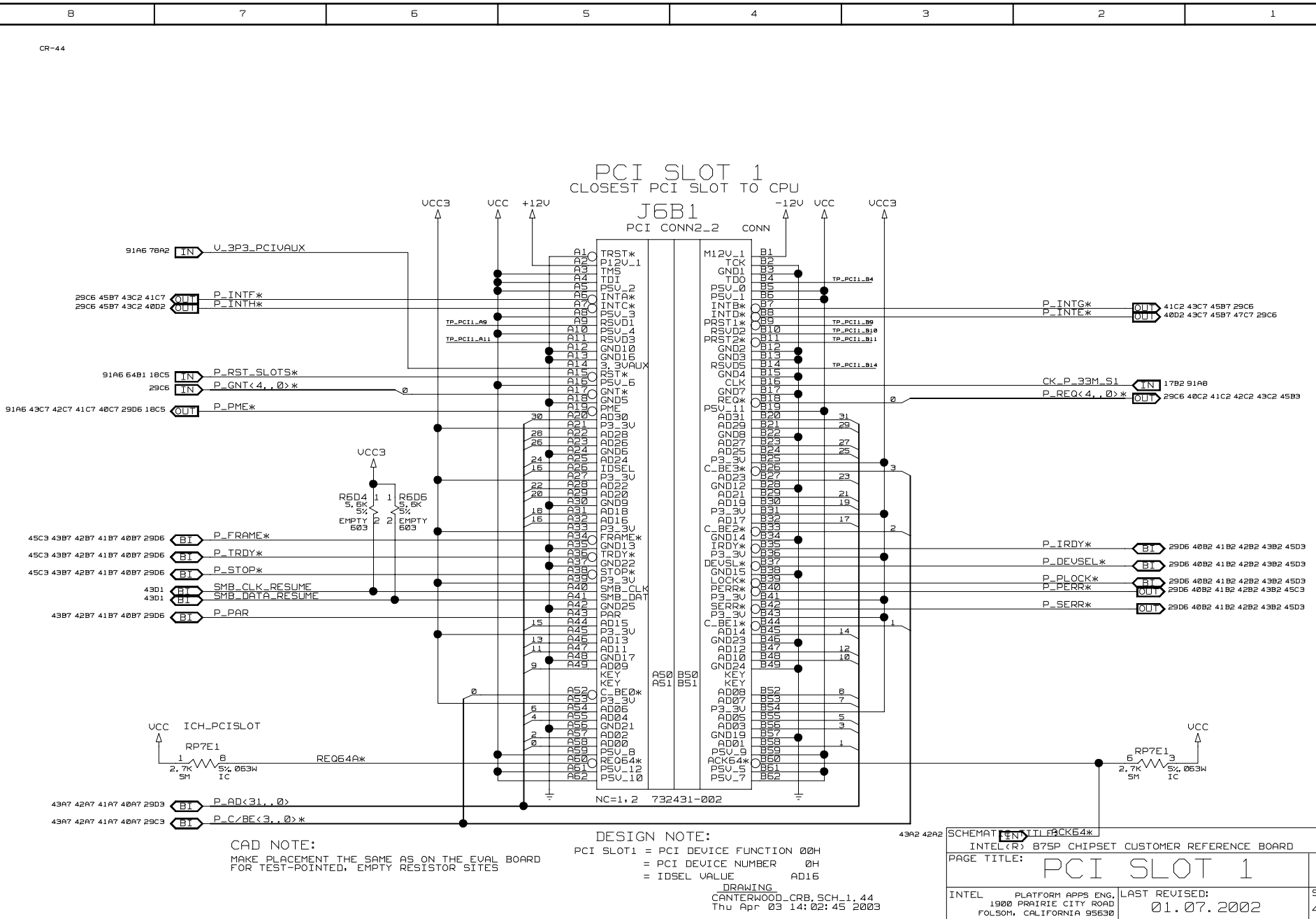


DESIGN NOTE:

PCI SLOT2 = PCI DEVICE FUNCTION 0BH
= PCI DEVICE NUMBER 1H
= IDSEL VALUE AD17

DRAWING
CANTERWOOD_CRB.SCH_1,43
Thu Apr 03 14:02:45 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 2		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 43/103


CR-44
PCI SLOT 1
CLOSEST PCI SLOT TO CPU
J6B1
PCI CONN2_2 CONN
VCC3
VCC
+12V
-12V
V_3P3_PCIVAUX
P_INTF*
P_INTH*
P_RST_SLOTS*
P_GNT<4,,0>*
P_PME*
P_FRAME*
P_TRDY*
P_STOP*
SMB_CLK_RESUME
SMB_DATA_RESUME
P_PAR
P_AD<31,,0>
P_C/BE<3,,0>*
REQ64A*
ICH_PCISLOT
RP7E1
R6D4
R6D5
5.6K
EMPTY
603
P_INTG*
P_INTE*
CK_P_33M_S1
P_REQ<4,,0>*
P_IRDY*
P_DEVSEL*
P_PLOCK*
P_PERR*
P_SERR*
ACK64*
TRST*
TCK
TMS
TDI
TDO
INTA*
INTB*
INTC*
INTD*
RSVD1
RSVD2
RSVD3
RST*
GNT*
PME
CLK
REQ*
IDSEL
FRAME*
IRDY*
DEVSEL*
STOP*
LOCK*
PERR*
SERR*
REQ64*
AD30
AD28
AD26
AD24
AD22
AD20
AD18
AD16
AD15
AD13
AD11
AD09
AD06
AD04
AD02
AD00
AD31
AD29
AD27
AD25
AD23
AD21
AD19
AD17
AD14
AD12
AD10
AD08
AD07
AD05
AD03
AD01
C_BE0*
C_BE1*
C_BE2*
C_BE3*
KEY
NC=1,2 732431-002
DESIGN NOTE:
PCI SLOT1 = PCI DEVICE FUNCTION 00H
= PCI DEVICE NUMBER 0H
= IDSEL VALUE AD16
CAD NOTE:
MAKE PLACEMENT THE SAME AS ON THE EVAL BOARD
FOR TEST-POINTED, EMPTY RESISTOR SITES
DRAWING
CANTERWOOD_CRB.SCH_1,44
Thu Apr 03 14:02:45 2003
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE: PCI SLOT 1
REV: 1.2
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED: 01.07.2002
SHEET: 44/103

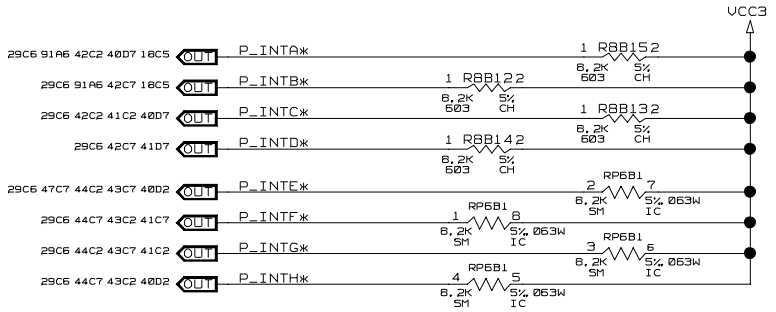
CR-45

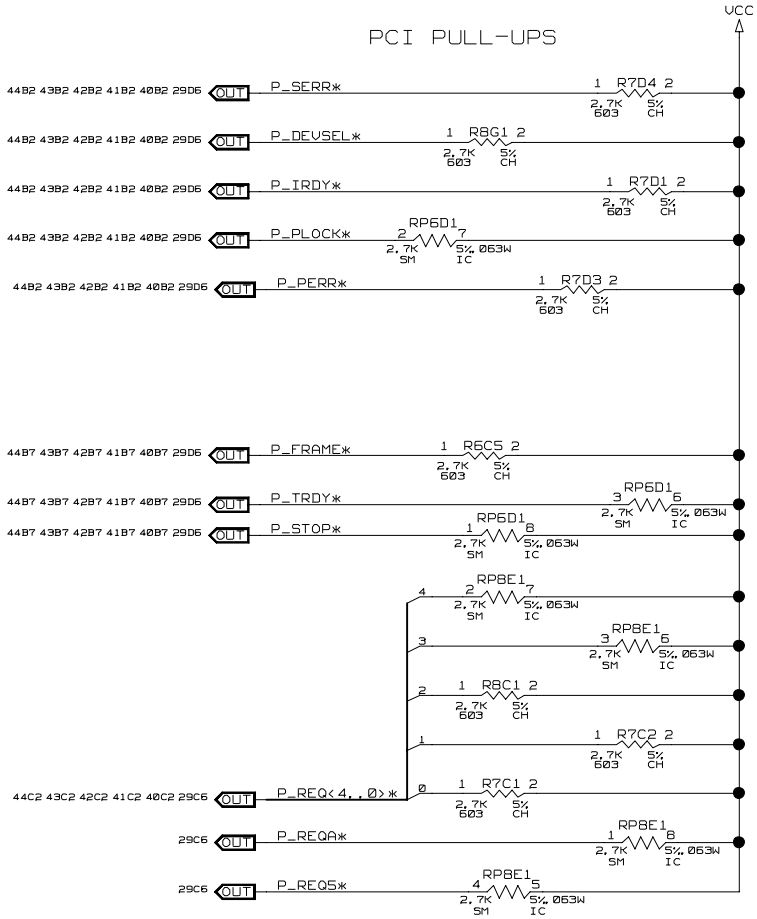
SPARE SECTIONS SB_TERMINATION

TP_RP6D2_4 — RP6D1 4 — 2.7K SM — 5% .063W IC — 5 — TP_RP6D2_5

ICH_PCISLOT

TP_RP8E4_5 — RP7E1 4 — 2.7K SM — 5% .063W IC — 5 — TP_RP8E4_5





DRAWING
CANTERWOOD_CRB.SCH_1.45
Thu Apr 03 14:02:45 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI TERMINATION		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 45/103

CR-46

SMB ADDRESS: 110
WRITE AC
READ AD

CNR SLOT DECOUPLING

VCC
C9C1 10.0UF 20% 6.3V EMPTY 1206
VCC3
C9C3 .1UF 20% 25V EMPTY 603
+12V
C9B7 .1UF 20% 25V EMPTY 603

J9B1
CNR60

	TP_CNR_B1	B1	RESERVED	RESERVED	A1	TP_CNR_A1	
	TP_CNR_B2	B2	RESERVED	RESERVED	A2	TP_CNR_A2	
	TP_CNR_B3	B3	RESERVED	GND	A3		
		B4	GND	RESERVED	A4	TP_CNR_A4	
	TP_CNR_B5	B5	RESERVED	RESERVED	A5	TP_CNR_A5	
	TP_CNR_B6	B6	RESERVED	GND	A6		
		B7	GND	LAN_TXD2	A7		
34C4 IN	ICH_LAN_TXD1_CNR	B8	LAN_TXD1	LAN_TXD0	A8	ICH_LAN_TXD2_CNR	IN 34C4
34C4 IN	ICH_LAN_RST_CNR	B9	LAN_RSTSYNC	GND	A9	ICH_LAN_TXD0_CNR	IN 34C4
		B10	GND	LAN_CLK	A10	ICH_LAN_CLK_CNR	OUT 34B4
34C4 OUT	ICH_LAN_RXD2_CNR	B11	LAN_RXD2	LAN_RXD1	A11	ICH_LAN_RXD1_CNR	OUT 34C4
34C4 OUT	ICH_LAN_RXD0_CNR	B12	LAN_RXD0	RESERVED	A12	TP_CNR_A12	
		B13	GND	USB+	A13	USB_CNR	BI 37C3
	TP_CNR_B14	B14	RESERVED	GND	A14		
38D4 IN	USB_CNR_PWR	B15	+5VDUAL	USB-	A15	USB_CNR*	BI 37C3
38A8 OUT	USB_OC_CNR*	B16	USB_OC	+12V	A16	+12V	
		B17	GND	GND	A17		
-12V		B18	-12V	+3.3VDUAL	A18	V_3P3_PCIVAUX	IN 78A2 91A6
VCC3		B19	+3.3VD	+5VD	A19	VCC	
		B20	GND	GND	A20		
34C1 OUT	ICH_EE_DIN_CNR	B21	EEDO	EEDI	A21	ICH_EE_DOUT_CNR	IN 34C1
34C1 IN	ICH_EE_CLK_CNR	B22	EECK	EECS	A22	ICH_EE_CS_CNR	IN 34C1
		B23	GND	SMB_A1	A23		
		B24	SMB_A0	SMB_A2	A24		
25B3 25A8 21B3 21A8 91C6 64B8 17C5	BI SMB_CLK_MAIN	B25	SMB_SCL	SMB_SDA	A25	SMB_DATA_MAIN	BI 17C5 64B8 91C6 21A8 21B8 25A8 25B8
30D3 64A3	OUT CDC_DWN_ENAB*	B26	CDC_DWN_ENAB	AC97_RESET	A26	AUD_LINK_RST*	IN 31B6
		B27	GND	AC97_SDATA_IN2	A27	CNR_SDI2_A27	
33C1 IN	AUD_LINK_SYNC	B28	AC97_SYNC	AC97_SDATA_IN1	A28	CNR_SDI1_A28	
33C1 IN	AUD_LINK_SDO	B29	AC97_SDATA_OUT	AC97_SDATA_IN0	A29	CNR_SDI0_A29	
31B6 93C5 52D1	BI AUD_LINK_BCLK	B30	AC97_BITCLK	GND	A30		

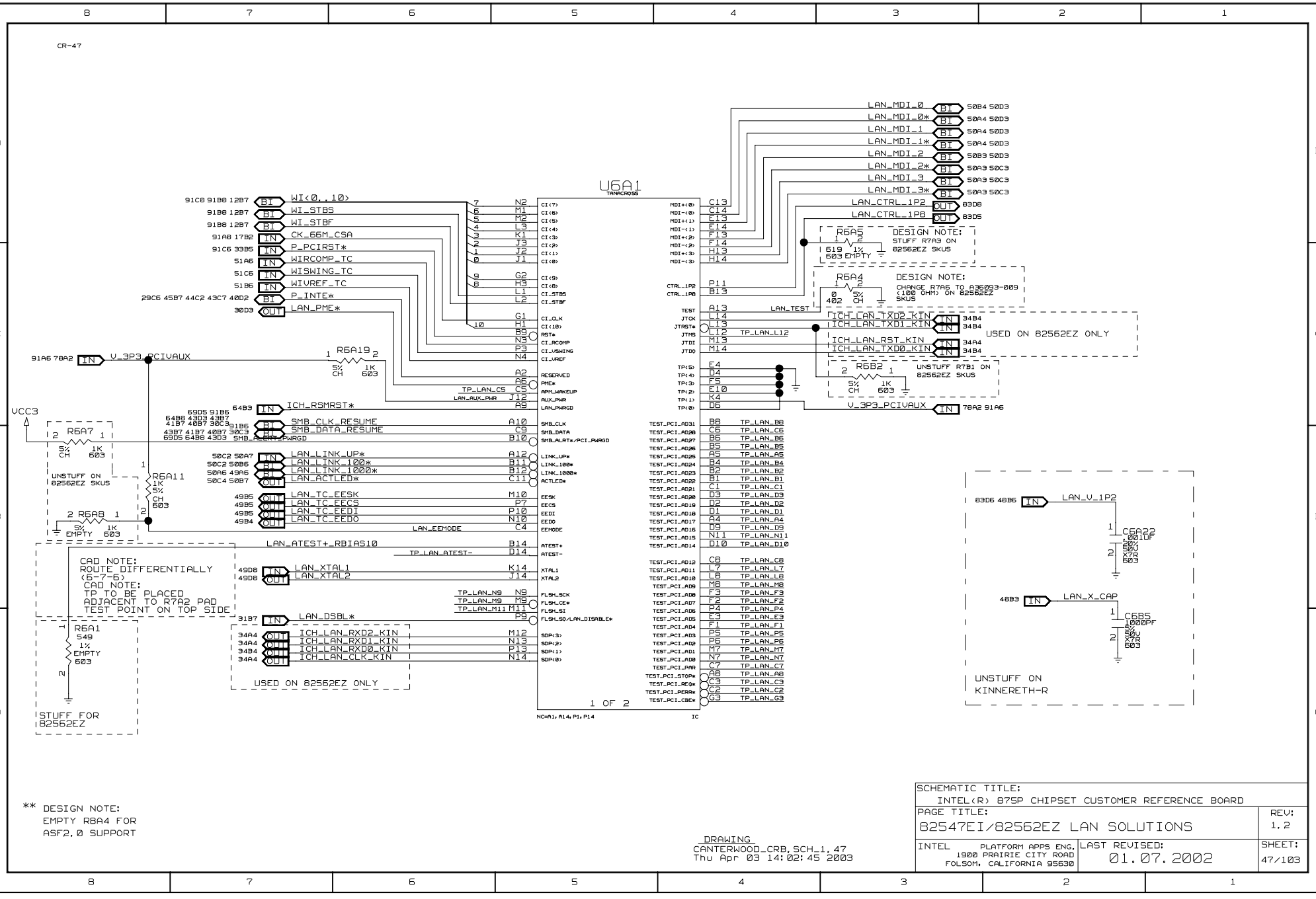
750073-002
CONN

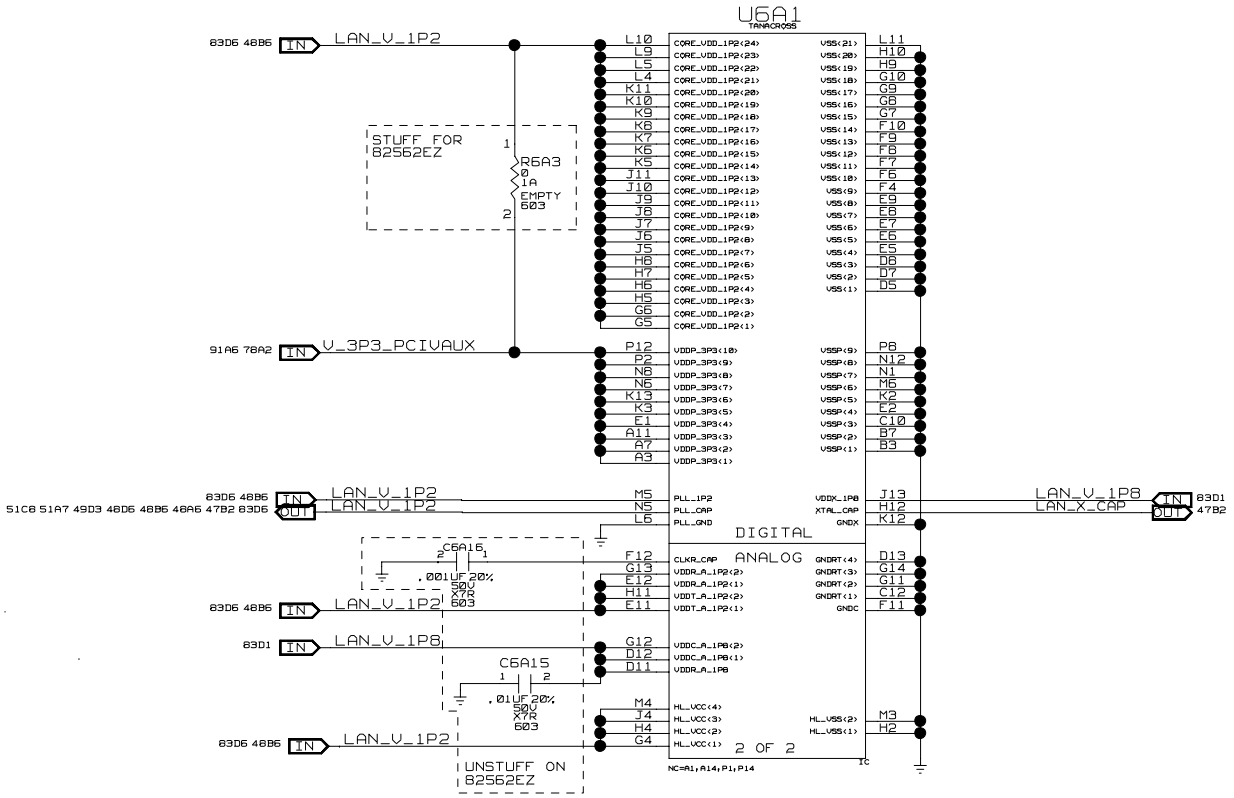
R9C3 0 603 1A CH — AUD_LINK_SDI2 OUT 31B6 52C1 93C5
R9C2 0 603 1A CH — AUD_LINK_SDI1 OUT 31B6 93C5
R9C1 0 603 1A CH — AUD_LINK_SDI0 OUT 31B6 93C5
R9C4 10K 5% CH 603

VCC
R9B4 10K 5% EMPTY 603
R9B6 10K 5% CH 603
R9B5 10K 5% CH 603
CNR_SMB_A1
CNR_SMB_A2
CNR_SMB_A0
R9B1 10K 5% CH 603
R9B3 10K 5% EMPTY 603
R9B2 10K 5% EMPTY 603

DRAWING
CANTERWOOD_CRB.SCH_1.46
Thu Apr 03 14:02:45 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CNR CONNECTOR		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 46/103


CR-47
U6A1
TANACROSS
1 OF 2
WI<0..10>
WI_STBS
WI_STBF
CK_66M_CSA
P_PCIRST#
WIRCOMP_TC
WISWING_TC
WIVREF_TC
P_INTE#
LAN_PME#
V_3P3_PCIVAUX
R6A19
ICH_RSMRST#
SMB_CLK_RESUME
SMB_DATA_RESUME
R6A7
R6A11
R6A8
LAN_LINK_UP#
LAN_LINK_100#
LAN_LINK_1000#
LAN_ACTLED#
LAN_TC_EESK
LAN_TC_EECS
LAN_TC_EEDI
LAN_TC_EEDO
LAN_EEMODE
LAN_ATEST+_RBIAS10
TP_LAN_ATEST-
LAN_XTAL1
LAN_XTAL2
LAN_DSBL#
R6A1
STUFF FOR 82562EZ
CAD NOTE: ROUTE DIFFERENTIALLY (6-7-6)
CAD NOTE: TP TO BE PLACED ADJACENT TO R7A2 PAD TEST POINT ON TOP SIDE
ICH_LAN_RXD2_KIN
ICH_LAN_RXD1_KIN
ICH_LAN_RXD0_KIN
ICH_LAN_CLK_KIN
USED ON 82562EZ ONLY
LAN_MDI_0
LAN_MDI_0*
LAN_MDI_1
LAN_MDI_1*
LAN_MDI_2
LAN_MDI_2*
LAN_MDI_3
LAN_MDI_3*
LAN_CTRL_1P2
LAN_CTRL_1P8
R6A5
DESIGN NOTE: STUFF R7A3 ON 82562EZ SKUS
R6A4
DESIGN NOTE: CHANGE R7A6 TO A36093-009 (100 OHM) ON 82562EZ SKUS
LAN_TEST
ICH_LAN_TXD2_KIN
ICH_LAN_TXD1_KIN
ICH_LAN_RST_KIN
ICH_LAN_TXD0_KIN
USED ON 82562EZ ONLY
R6B2
UNSTUFF R7B1 ON 82562EZ SKUS
V_3P3_PCIVAUX
LAN_V_1P2
C6A22
LAN_X_CAP
C6B5
UNSTUFF ON KINNERETH-R
** DESIGN NOTE: EMPTY R8A4 FOR ASF2.0 SUPPORT
DRAWING
CANTERWOOD_CRB.SCH_1.47
Thu Apr 03 14:02:45 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
82547EI/82562EZ LAN SOLUTIONS
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
47/103



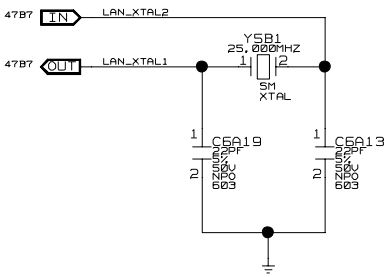
DRAWING
CANTERWOOD_CRB.SCH_1,48
Thu Apr 03 14:02:46 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: 82547EI/82562EZ POWER CONNECTIONS		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 48/103

CR-49

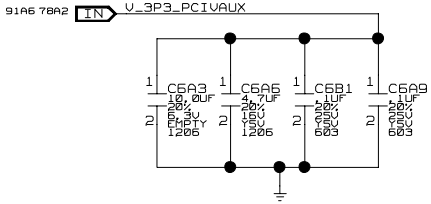
LAN CRYSTAL

CAD NOTE:
MINIMIZE XTAL TRACES
DO NOT PLACE OR ROUTE NEAR PLANE SPLIT



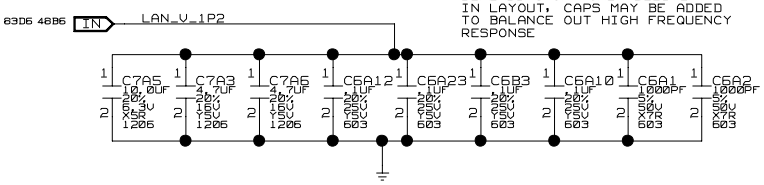
LAN DECOUPLING

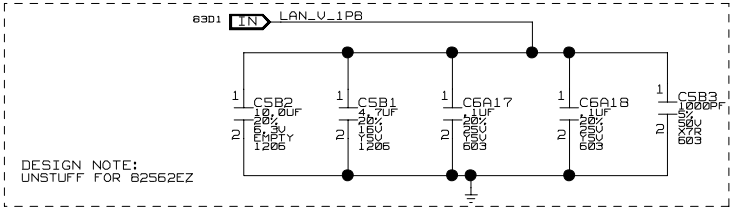
DESIGN NOTE:
DECOUPLING CAPS SHARE BETWEEN 82547EI & 82562EZ VOLTAGE NETS



DESIGN NOTE:

DEPENDING ON POWER DELIVERY IN LAYOUT, CAPS MAY BE ADDED TO BALANCE OUT HIGH FREQUENCY RESPONSE





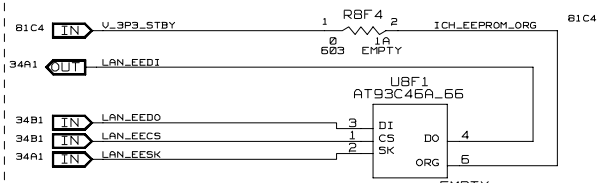
DESIGN NOTE:
UNSTUFF FOR 82562EZ

82562EZ EEPROM

STUFF THIS EEPROM ONLY WITH 82562EZ, SKUS. PLACE NEAR ICH. SEE LINK SHOWN BELOW FOR CORRECT P/N IMPLEMENTATION

HTTP://DPSD.INTEL.COM/LMM/LAN/DOCS/EEPROM.DOC

DESIGN NOTE:
IN ABSENCE OF CNR, THIS RESISTOR MAY BE REMOVED



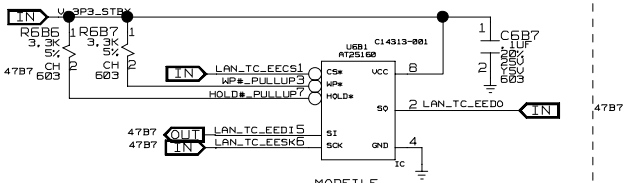
PRE-PROG = 729345-006
ATE-PROG = XXXXXX-XXX

82547EI EEPROM

CAD NOTE:
PLACE EEPROM NEAR LAN CONTROLLER.

DESIGN NOTE:

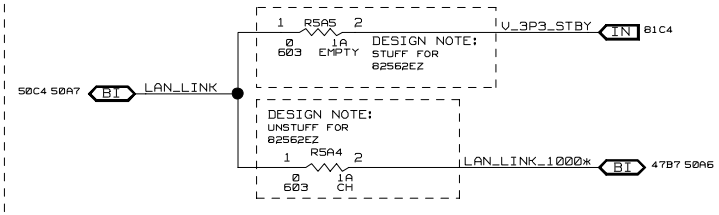
SEE URL FILE LINKED BELOW FOR CORRECT P/N
HTTP://DPSD.INTEL.COM/LMM/LAN/EEPROM/EEPROM_SELECTION_GUIDE.XLS



PRE-PROG = XXXXXX-XXX
ATE-PROG = XXXXXX-XXX

MODFILE
TO C14759-003
FOR PRE-PROGRAMMED PART

STUFFING OPTIONS FOR LED ENABLING

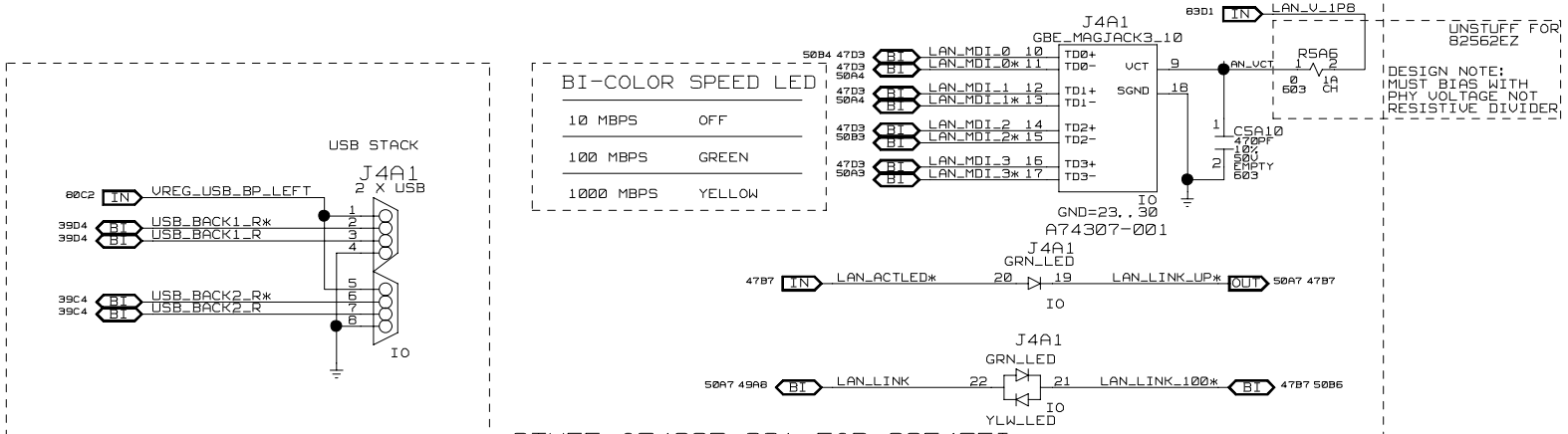


DRAWING
CANTERWOOD_CRB.SCH_1.49
Thu Apr 03 14:02:46 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: 82547EI/82562EZ MISC CIRCUITS		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 49/103

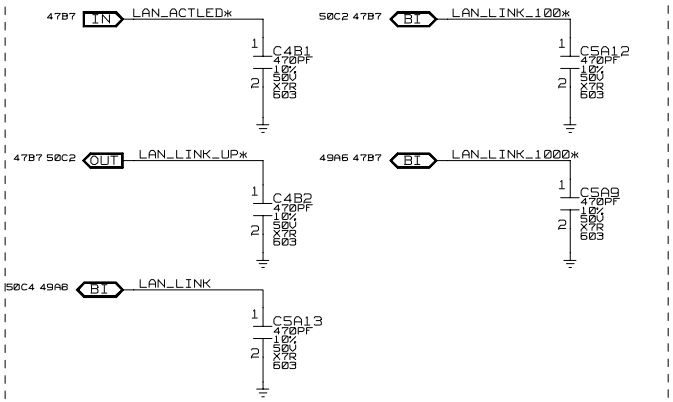
CR-50

LAN CONNECTOR



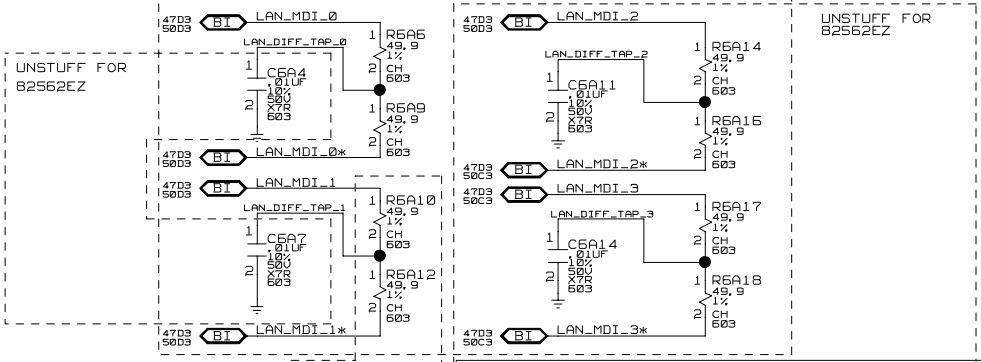
LED DECOUPLING

CAD NOTE:
LED CAPS SHOULD BE PLACED NEXT TO CONNECTOR



DIFFERENTIAL PAIR TERMINATONS

CAD NOTE:
PLACE NEXT TO CONTROLLER



DESIGN NOTE:
FOR 82562EZ, STUFF 60.4 OHM 0603 1% 202286-616 FOR BOTH SITES

DRAWING
CANTERWOOD_CRB.SCH,1,50
Thu Apr 03 14:02:46 2003

SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: LAN MAGJACK AND DIFF PAIR TERM

REV: 1.2

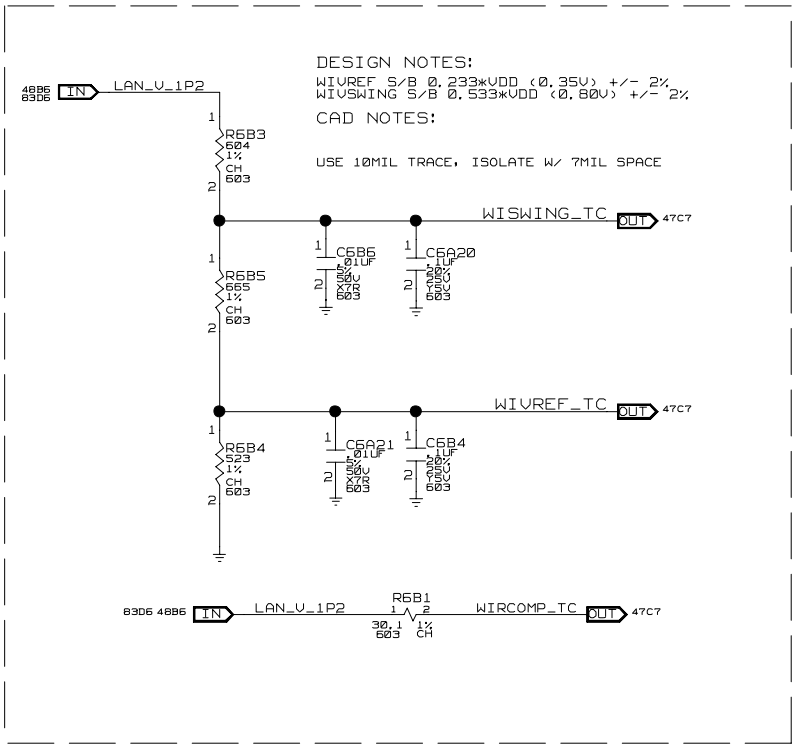
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630

LAST REVISED: 01.07.2002

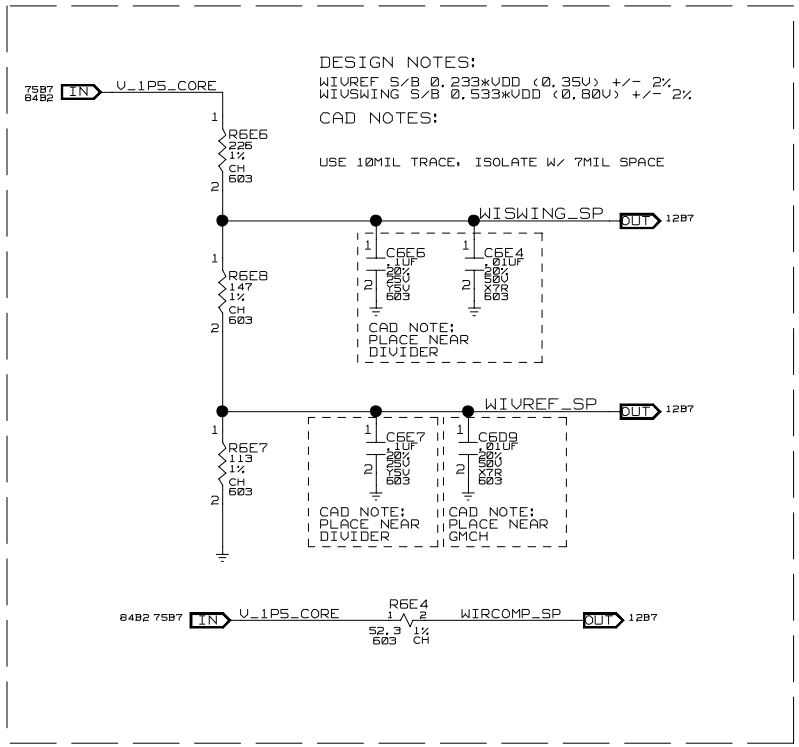
SHEET: 50/103

CR-51

LAN
CSA INTERFACE REFERENCE

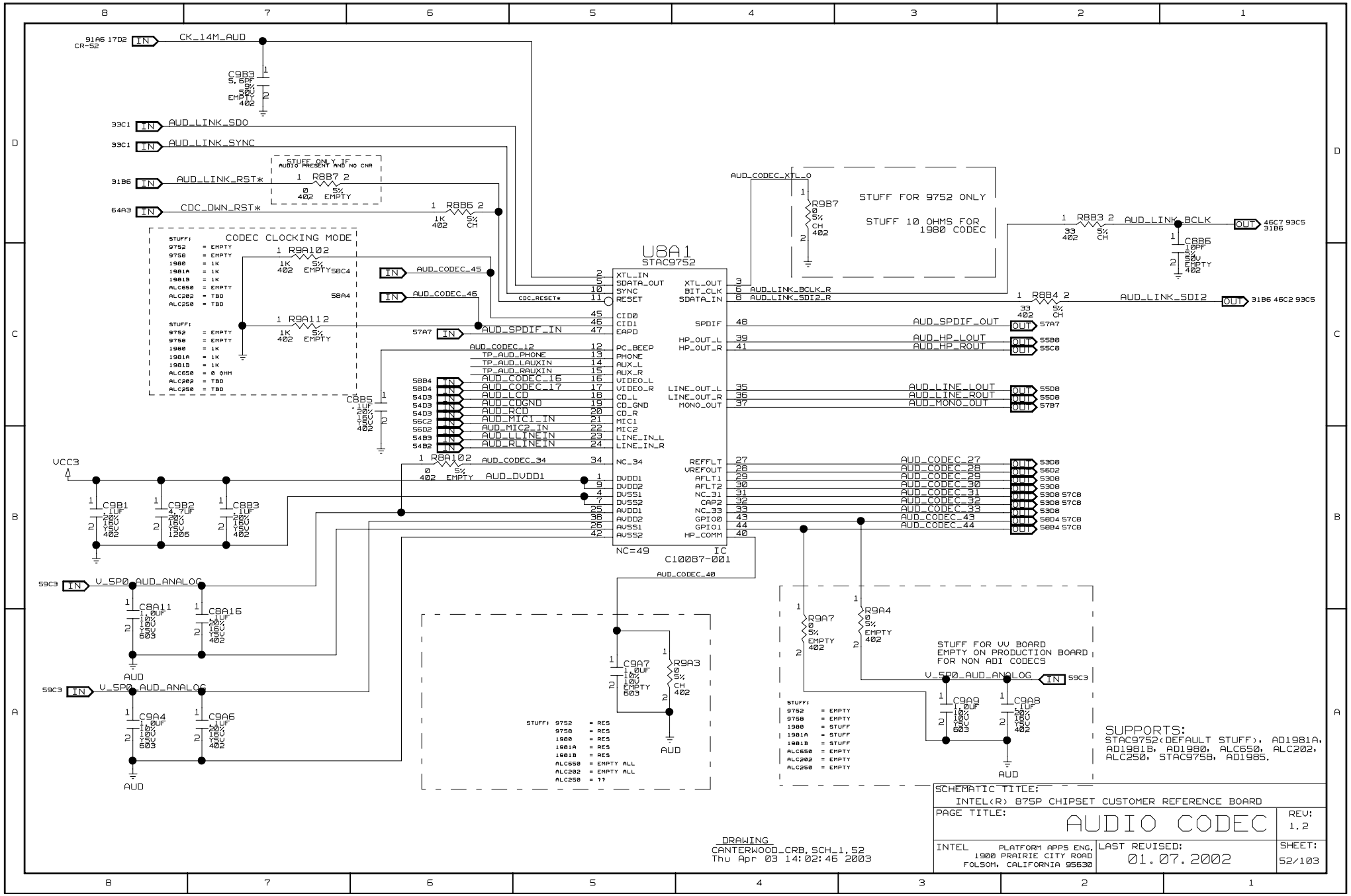


MCH
CSA INTERFACE REFERENCE



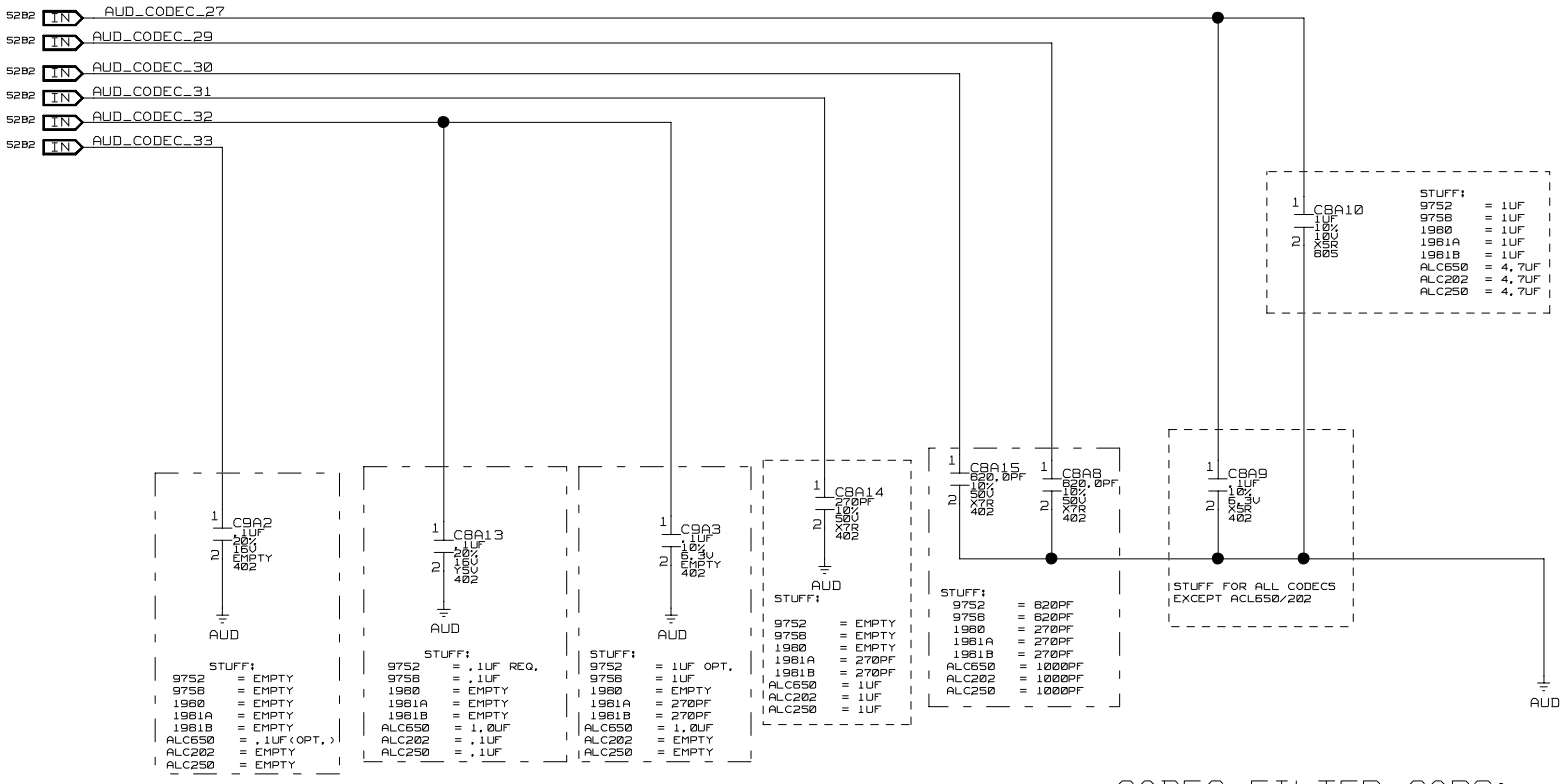
DRAWING
CANTERWOOD_CRB.SCH_1,51
Thu Apr 03 14:02:46 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CSA INTERFACE REFERENCE		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 51/103


CK_14M_AUD
AUD_LINK_SDO
AUD_LINK_SYNC
AUD_LINK_RST*
CDC_DWN_RST*
CODEC CLOCKING MODE
U8A1
STAC9752
XTL_IN
SDATA_OUT
SYNC
RESET
CID0
CID1
EAPD
PC_BEEP
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
NC_34
DVDD1
DVDD2
DVSS1
DVSS2
AVDD1
AVDD2
AVSS1
AVSS2
XTL_OUT
BIT_CLK
SDATA_IN
SPDIF
HP_OUT_L
HP_OUT_R
LINE_OUT_L
LINE_OUT_R
MONO_OUT
REFFLT
VREFOUT
AFLT1
AFLT2
NC_31
CAP2
NC_33
GPIO0
GPIO1
HP_COMM
NC=49
IC
C10087-001
AUD_CODEC_XTL_O
STUFF FOR 9752 ONLY
STUFF 10 OHMS FOR 1980 CODEC
AUD_LINK_BCLK
AUD_LINK_SDI2
AUD_SPDIF_OUT
AUD_HP_LOUT
AUD_HP_ROUT
AUD_LINE_LOUT
AUD_LINE_ROUT
AUD_MONO_OUT
AUD_SPDIF_IN
AUD_DVDD1
V_5P0_AUD_ANALOG
AUD
STUFF FOR VV BOARD
EMPTY ON PRODUCTION BOARD
FOR NON ADI CODECS
SUPPORTS:
STAC9752(DEFAULT STUFF), AD1981A, AD1981B, AD1980, ALC650, ALC202, ALC250, STAC9758, AD1985.
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
AUDIO CODEC
REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED: 01.07.2002
SHEET: 52/103
DRAWING
CANTERWOOD_CRB.SCH_1,52
Thu Apr 03 14:02:46 2003

CR-53

KEEP CAPS AS CLOSE AS POSSIBLE TO AC97 CODEC.



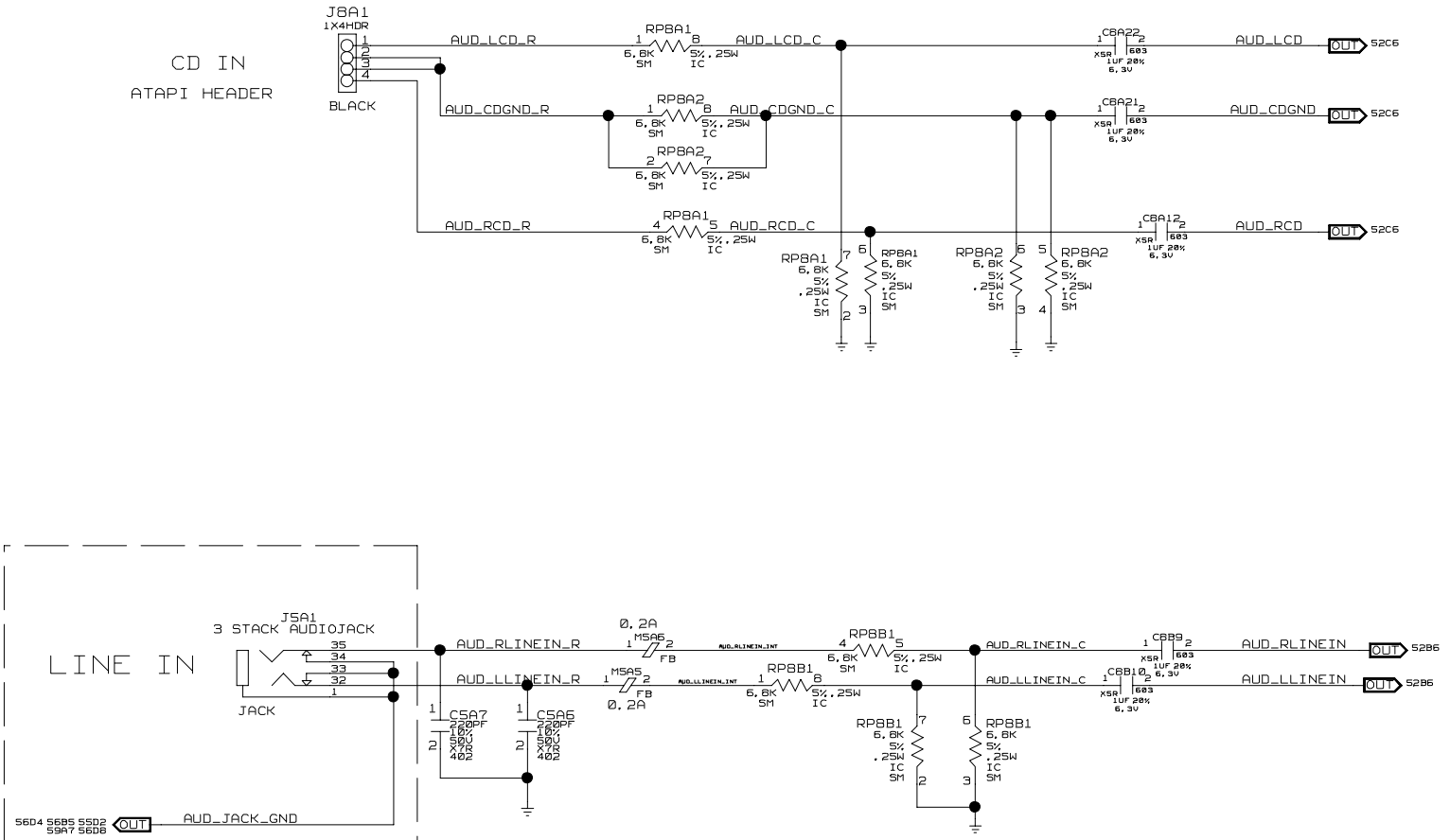
CODEC FILTER CAPS:
9752, 9758, 1980, 1981A, 1981B,
ALC650, ALC202, ALC250

DEFAULT STUFFING STAC 9752

DRAWING
CANTERWOOD_CRB.SCH_1.53
Thu Apr 03 14:02:46 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CODEC FILTER CAPS		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 53/103

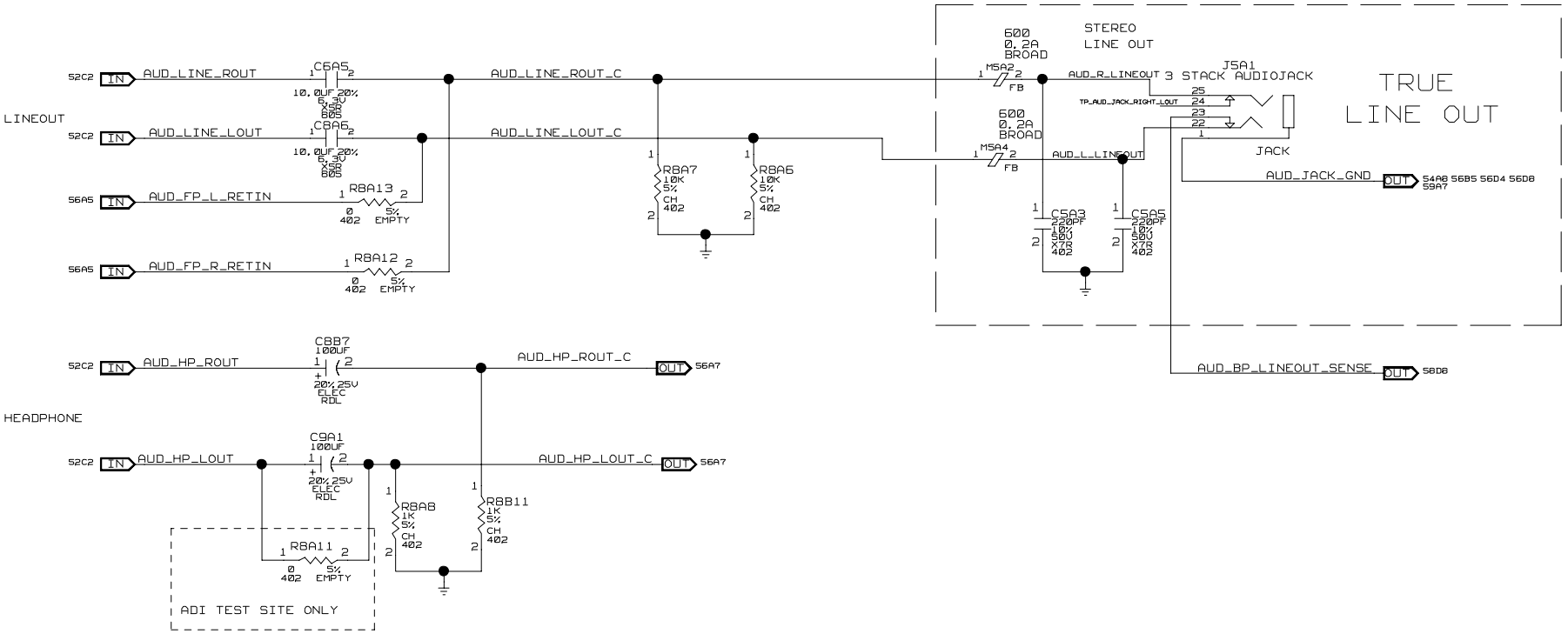
CR-54



DRAWING
CANTERWOOD_CRB.SCH_1.54
Thu Apr 03 14:02:47 2003

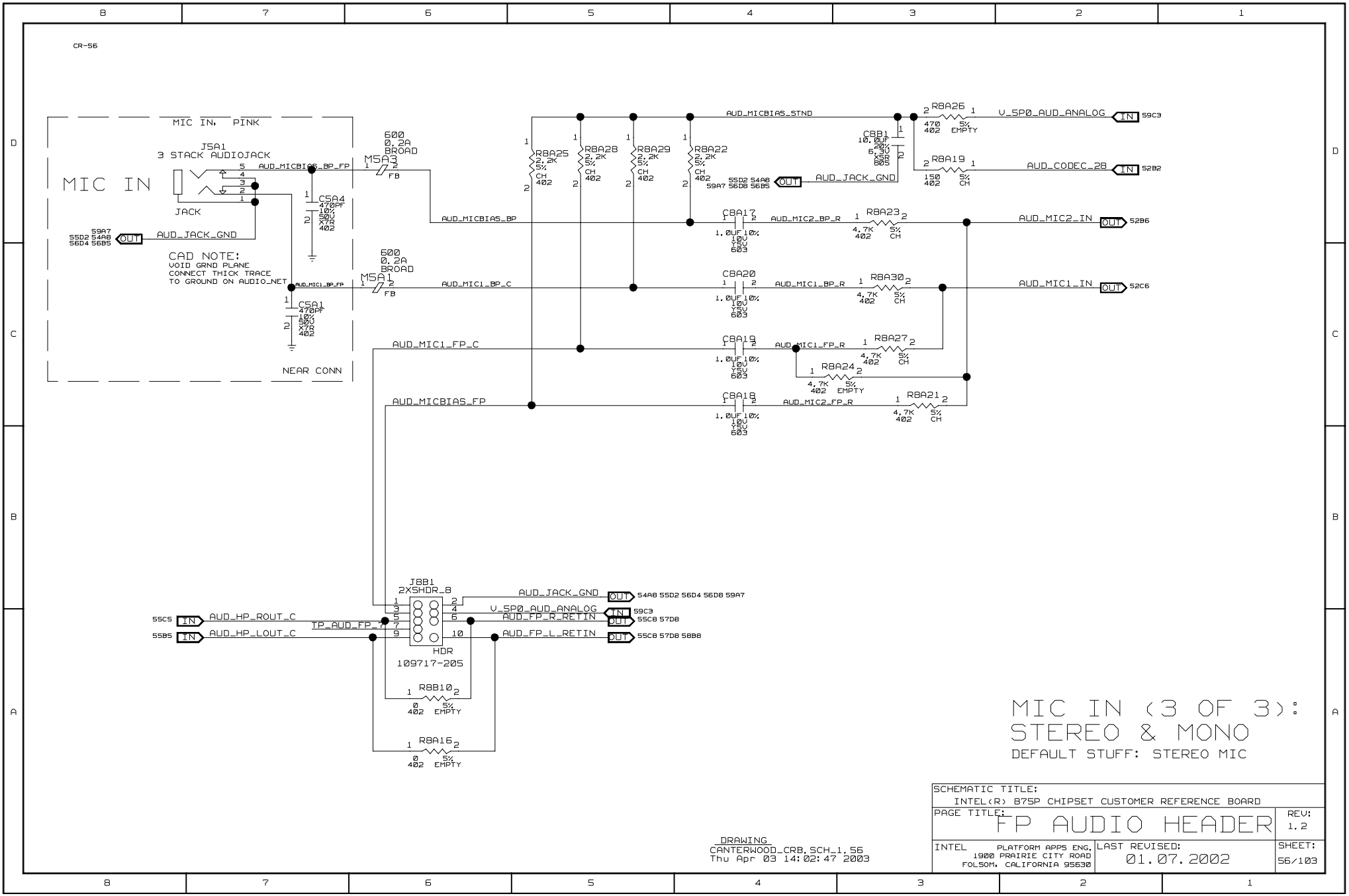
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CD IN ATAPI HEADER LINE IN CONN. (1 OF 3)		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 54/103

CR-55

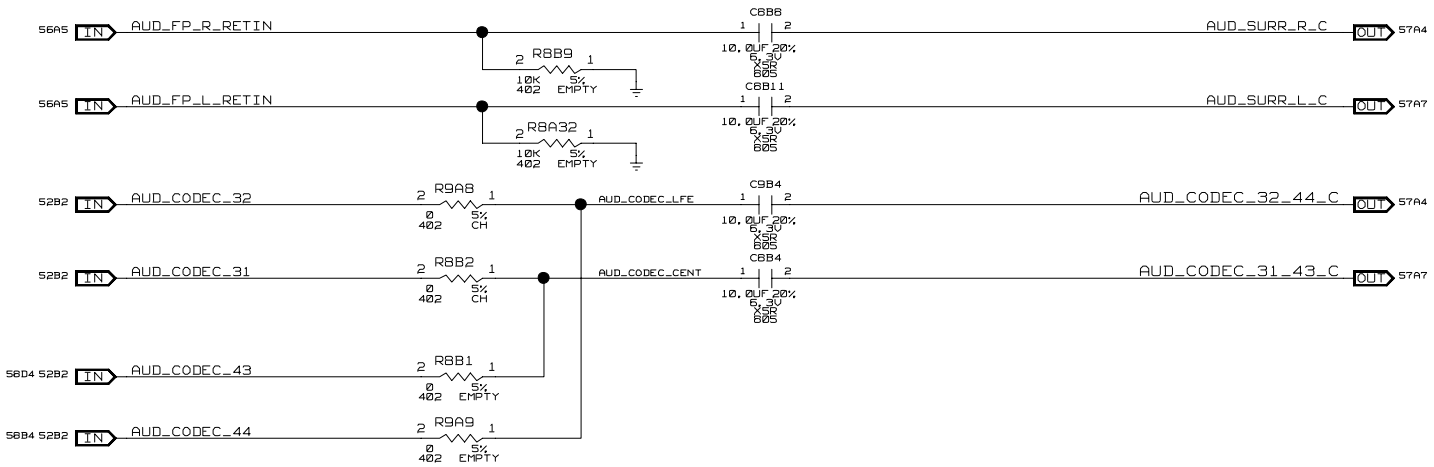


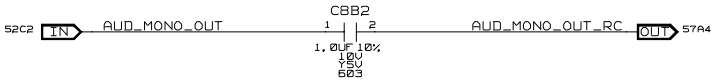
DRAWING
CANTERWOOD_CRB.SCH_1.55
Thu Apr 03 14:02:47 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: LINE OUT CONN. (2 OF 3)		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 55/103

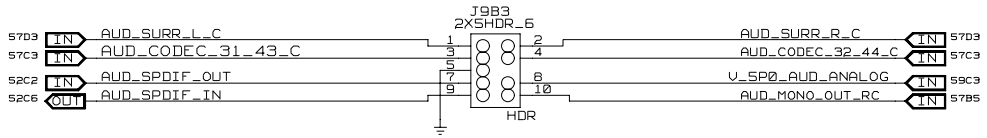

CR-56
MIC IN, PINK
MIC IN
J5A1
3 STACK AUDIOJACK
JACK
AUD_MICBIAS_BP_FP
AUD_JACK_GND
59A7 55D2 54A8 56D4 56B5
OUT
C5A4
470PF
16V
X7R
402
C5A1
470PF
50V
X7R
402
CAD NOTE:
VOID GRND PLANE
CONNECT THICK TRACE
TO GROUND ON AUDIO_NET
NEAR CONN
AUD_MIC1_BP_FP
600
0.2A
BROAD
M5A3
FB
M5A1
AUD_MICBIAS_BP
AUD_MIC1_BP_C
AUD_MICBIAS_STND
R8A25
2.2K
5%
CH
402
R8A28
R8A29
R8A22
C8B1
10.0UF
20%
6.3V
TANT
B2
R8A26
470
402
5%
EMPTY
V_5P0_AUD_ANALOG
IN
59C3
R8A19
150
402
5%
CH
AUD_CODEC_2B
52B2
C8A17
1.0UF
10%
10V
Y5V
603
AUD_MIC2_BP_R
R8A23
4.7K
AUD_MIC2_IN
52B6
C8A20
AUD_MIC1_BP_R
R8A30
AUD_MIC1_IN
52C6
AUD_MIC1_FP_C
C8A19
AUD_MIC1_FP_R
R8A27
R8A24
AUD_MICBIAS_FP
C8A18
AUD_MIC2_FP_R
R8A21
J8B1
2X5HDR_8
HDR
109717-205
55C5
AUD_HP_ROUT_C
55B5
AUD_HP_LOUT_C
TP_AUD_FP_7
AUD_JACK_GND
54A8 55D2 56D4 56D8 59A7
V_5P0_AUD_ANALOG
59C3
AUD_FP_R_RETIN
55C8 57D8
AUD_FP_L_RETIN
55C8 57D8 58B8
R8B10
0
R8A16
MIC IN (3 OF 3): STEREO & MONO
DEFAULT STUFF: STEREO MIC
DRAWING
CANTERWOOD_CRB.SCH_1.56
Thu Apr 03 14:02:47 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
FP AUDIO HEADER
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
56/103

CR-57





6 CHANNEL AUDIO HEADER

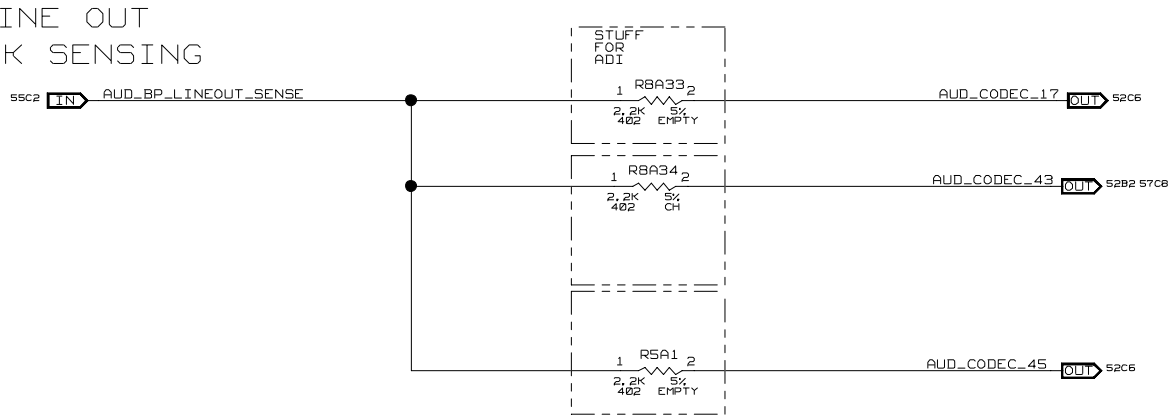


DRAWING
CANTERWOOD_CRB.SCH_1.57
Thu Apr 03 14:02:47 2003

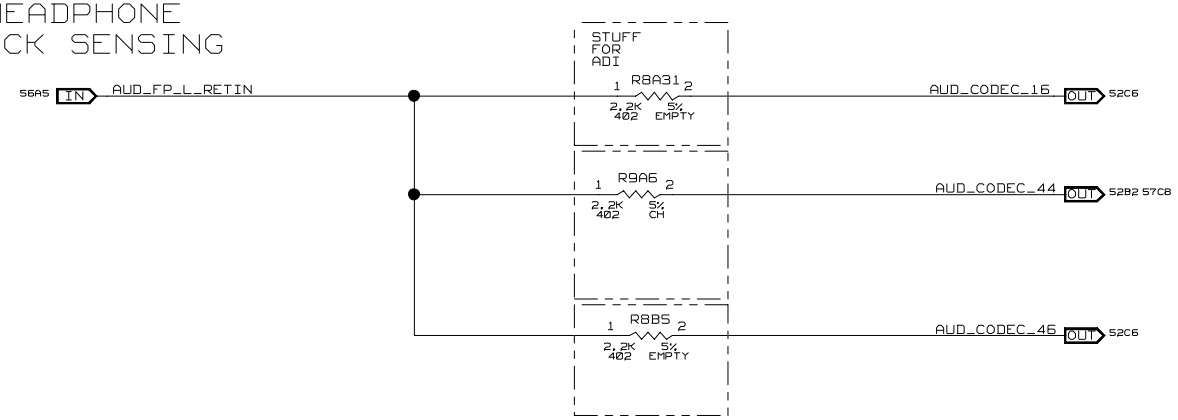
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CENTER/LFE OUTPUTS 6 CHAN AUDIO HEADER		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 57/103

CR-58

LINE OUT JACK SENSING



HEADPHONE JACK SENSING



DRAWING
CANTERWOOD_CRB.SCH_1.58
Thu Apr 03 14:02:47 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO JACK SENSING		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 58/103

CR-59

SPECIAL OPTION

PLACE IN TOP LEFT CORNER OF BOARD

75C2 IN V_5P0_STBY 1 R9A2 2 0 603 1A EMPTY

VCC

1 R9A5 2 0 603 1A EMPTY

1 R8A1 2 0OHM 5M EMPTY

1 R8A2 2 0OHM 5M EMPTY

AUD

REGULATOR THERMAL TAB SHOULD BE SOLDERED TO A COPPER PAD THAT IS LARGE ENOUGH TO ALLOW 5 TO 10 GROUND VIAS AROUND THE COMPONENT FOR COOLING

+12V

U9A1 78M05C

IN OUT GND IC

CLOSE TO REGULATOR

C9A5 10UF 20% 16V Y5V 805

AUD

C8A1 .1UF 20% 16V Y5V 402

AUD

C8A3 1.0UF 10% 16V Y5V 603

AUD

C8A5 22.0U 20% 6.3V X5R 1210 644066-008

AUD

V_5P0_AUD_ANALOG OUT 52A2 52A8 52B8 56B5 56D2 57A4

NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO CAPS AND THEN THROUGH SEVERAL VIAS TO V_5P0_AUD_ANALOG

56D8 56D4 56B5 55D2 54A8 IN AUD_JACK_GND

PLACE NEAR TRIPLE -STACK AUDIO CONNECTOR

C5A2 1.0UF 10% 16V EMPTY 603

GND AT MOUNTING HOLE

R9A1 0 5% CH 402

PLACE NEXT TO CODEC

AUD

DRAWING
CANTERWOOD_CRB.SCH_1.59
Thu Apr 03 14:02:48 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AUDIO VREG		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 59/103

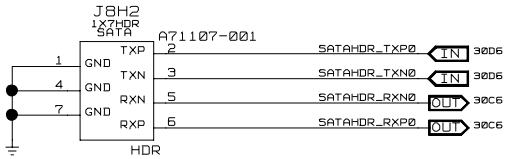
CR-60

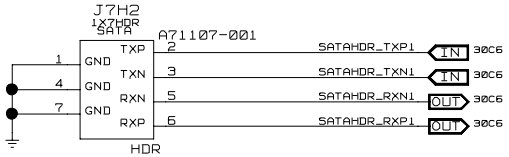
BLANK PAGE

DRAWING
CANTERWOOD_CRB.SCH_1.60
Thu Apr 03 14:02:48 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE:		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 60/103

CR-61





DRAWING
CANTERWOOD_CRB.SCH_1.61
Thu Apr 03 14:02:48 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: SATA CONNECTORS		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 61/103

CR-62

ROM IS COOL

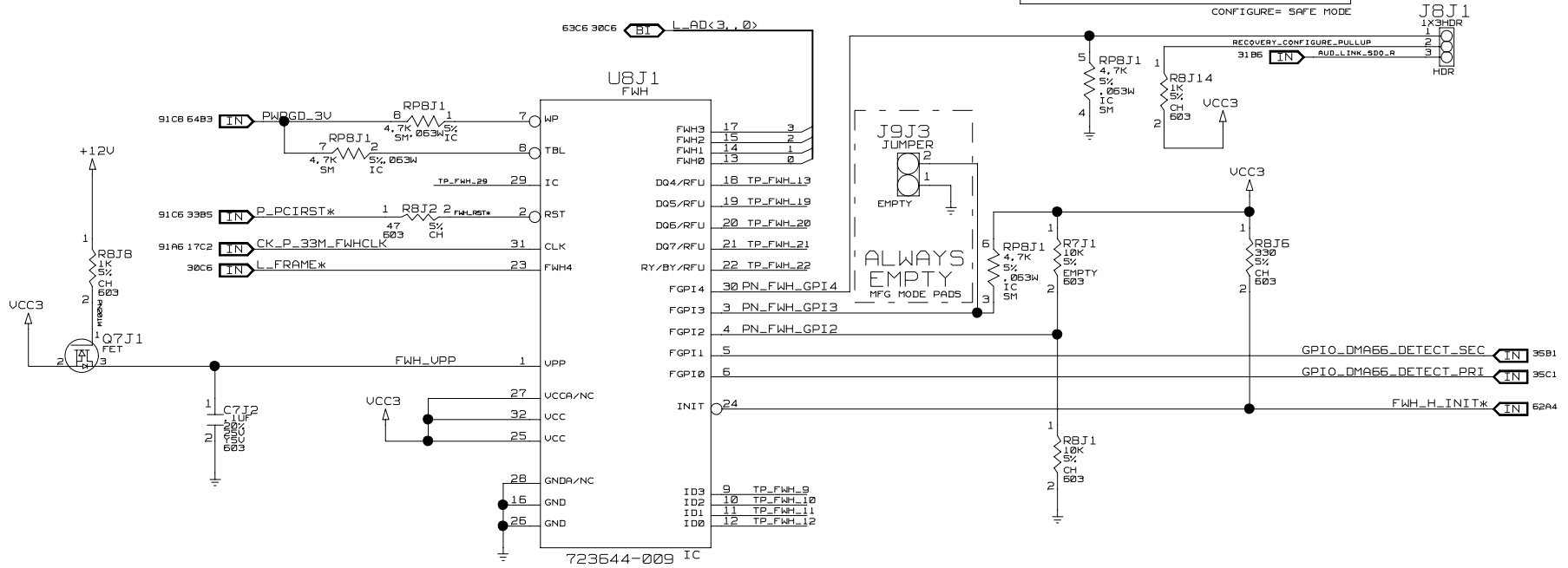
LAST_USED:

R215W
C203W
RP203W
TP_FWH_22
U201W
Q201W
J202W

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

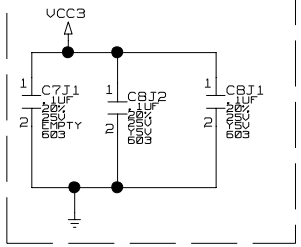
CONFIGURE= SAFE MODE

ATTRIBUTES:
ROOM=FWH
BOM=FWH_OPT

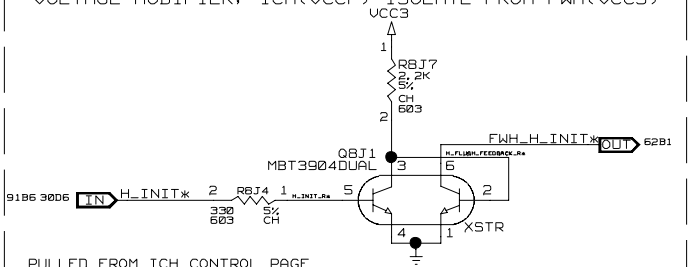


MODFILED ON SOCKET XU8J1= 700000-884

FIRMWARE HUB DECOUPLING



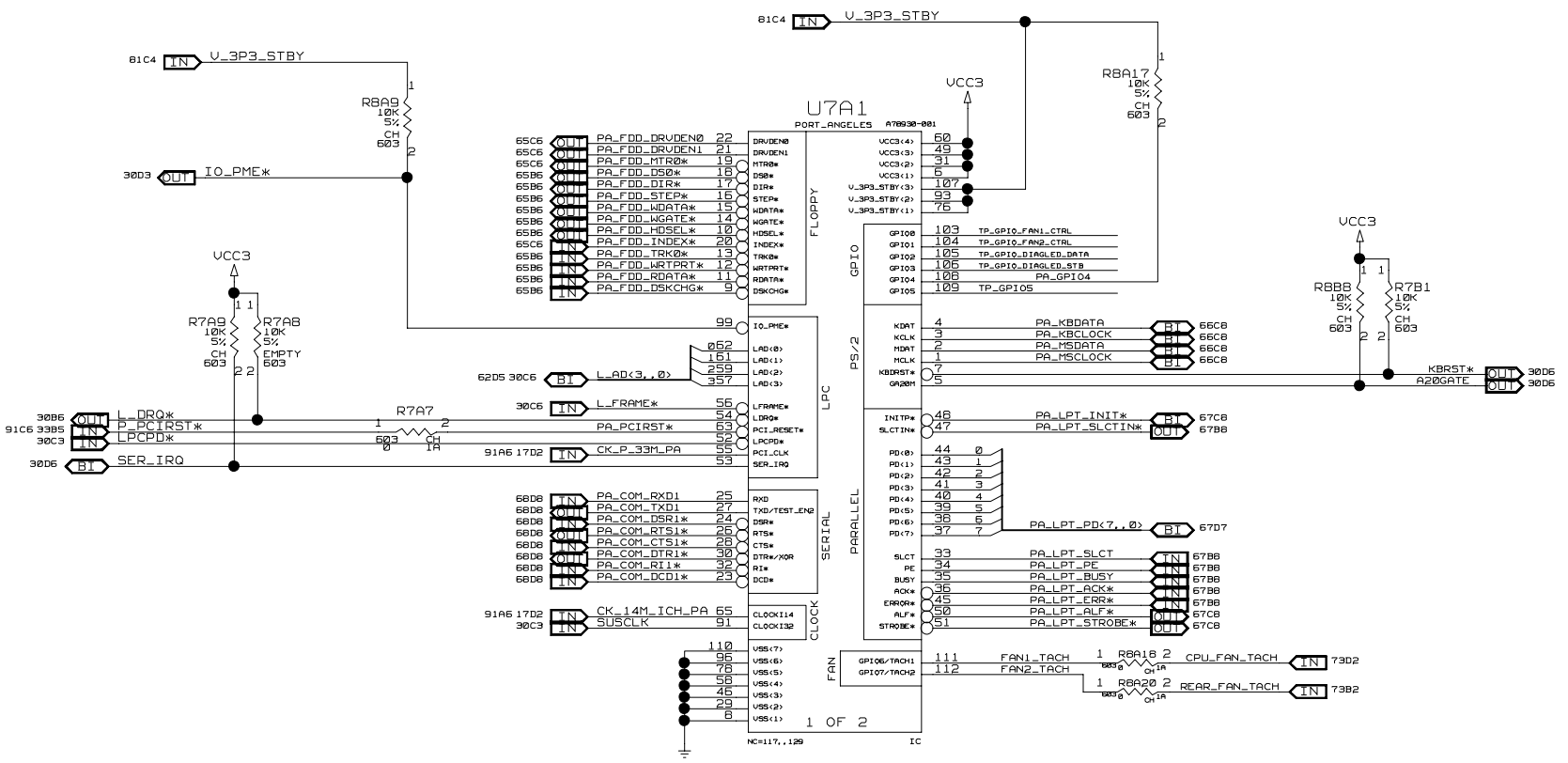
VOLTAGE MODIFIER; ICH(VCCP) ISOLATE FROM FWH(VCC3)



PULLED FROM ICH CONTROL PAGE

DRAWING
CANTERWOOD_CRB.SCH_1.62
Thu Apr 03 14:02:48 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: FIRMWARE HUB		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 62/103


CR-63
U7A1
PORT_ANGELES A70930-001
81C4 IN V_3P3_STBY
VCC3
R8A9 10K 5% CH 603
R8A17 10K 5% CH 603
30D3 OUT IO_PME#
IO_PME#
R7A9 10K 5% CH 603
R7A8 10K 5% EMPTY 603
R8B8 10K 5% CH 603
R7B1 10K 5% CH 603
KBRST# OUT 30D6
A20GATE OUT 30D6
30B6 OUT L_DRQ#
91C6 33B5 IN L_PCIRST#
30C3 IN LPCPD#
30D6 BI SER_IRQ
R7A7 603 0 CH 1A
62D5 30C6 BI L_AD<3,,0>
30C6 IN L_FRAME#
91A6 17D2 IN CK_P_33M_PA
PA_PCIRST#
FLOPPY
GPIO
LPC
PS/2
PARALLEL
SERIAL
CLOCK
FAN
PA_FDD_DRVDEN0
PA_FDD_DRVDEN1
PA_FDD_MTR0#
PA_FDD_DS0#
PA_FDD_DIR#
PA_FDD_STEP#
PA_FDD_WDATA#
PA_FDD_WGATE#
PA_FDD_HDSEL#
PA_FDD_INDEX#
PA_FDD_TRK0#
PA_FDD_WRTPRT#
PA_FDD_RDATA#
PA_FDD_DSKCHG#
TP_GPIO_FAN1_CTRL
TP_GPIO_FAN2_CTRL
TP_GPIO_DIAGLED_DATA
TP_GPIO_DIAGLED_STB
PA_GPIO4
TP_GPIO5
PA_KBDATA
PA_KBCLOCK
PA_MSDATA
PA_MSCLOCK
PA_LPT_INIT#
PA_LPT_SLCTIN#
PA_LPT_PD<7,,0>
PA_LPT_SLCT
PA_LPT_PE
PA_LPT_BUSY
PA_LPT_ACK#
PA_LPT_ERR#
PA_LPT_ALF#
PA_LPT_STROBE#
PA_COM_RXD1
PA_COM_TXD1
PA_COM_DSR1#
PA_COM_RTS1#
PA_COM_CTS1#
PA_COM_DTR1#
PA_COM_RI1#
PA_COM_DCD1#
CK_14M_ICH_PA
SUSCLK
FAN1_TACH
FAN2_TACH
R8A18 CPU_FAN_TACH
R8A20 REAR_FAN_TACH
1 OF 2
C7B2 .1UF 16V CER 603
C7B1 .1UF 16V CER 603
C7A7 .1UF 16V CER 603
C7A4 .1UF 16V CER 603
C8A7 .1UF 16V CER 603
PLACE NEAR DEVICE PINS 6, 31, 49, 60, 75, 93, 107
DRAWING
CANTERWOOD_CRB.SCH_1.63
Thu Apr 03 14:02:48 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
PORT ANGELES (1 OF 2)
REV:
1.2
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
63/103

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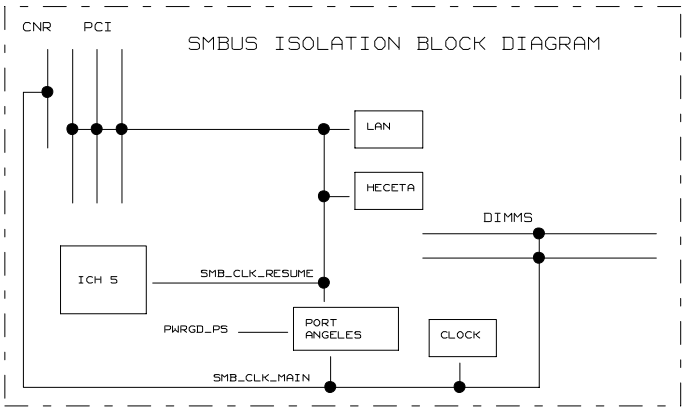
SMBUS ISOLATION BLOCK DIAGRAM

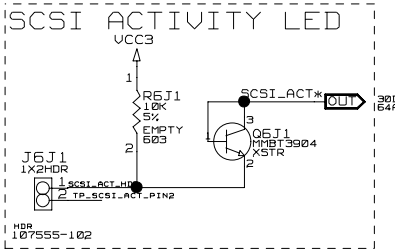


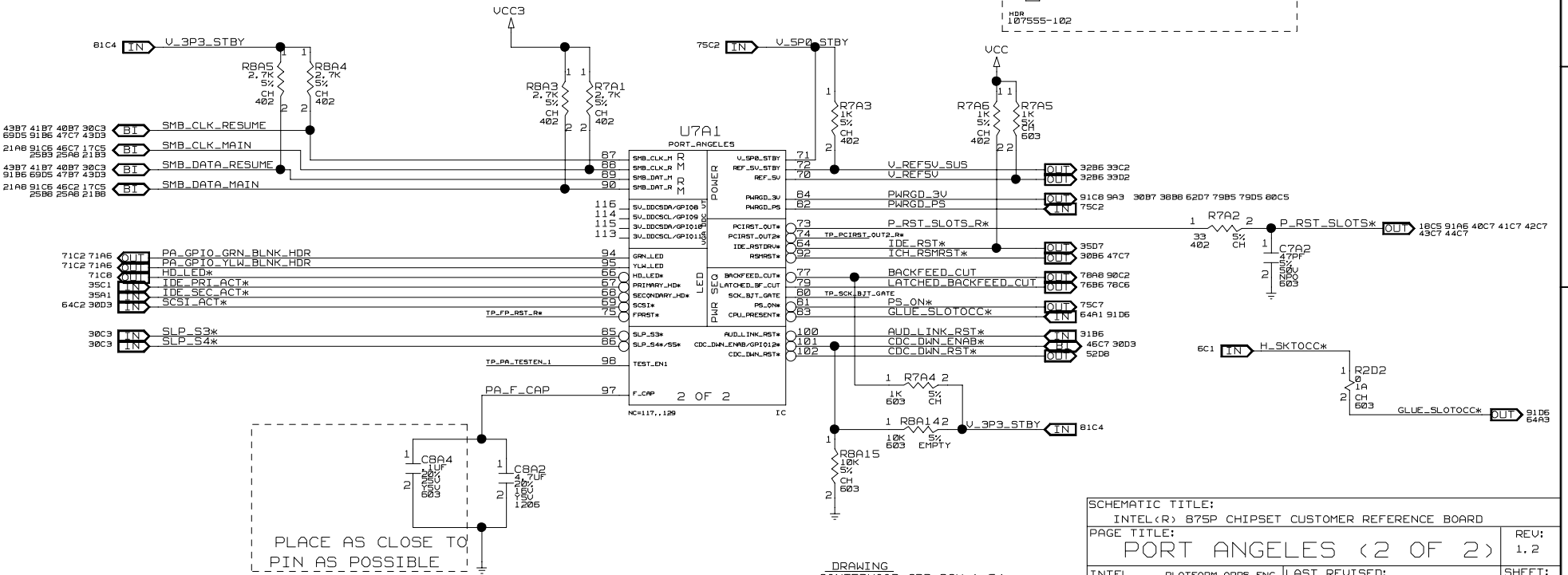
PORT_ANGELES 2 OF 2 INPUTS

NOTE: DEFAULT TYPE IS LISTED FIRST.
SEE PORT_ANGELES SPEC FOR TYPE DESCRIPTION

PIN	FUNCTION	TYPE
1	TEST_EN	3IPD
2	AUD_LINK_RST*	5I
3	CDC_DWN_ENAB/GPIO12*	5I/O12
70	PRIMARY_HD*	3ISPU_400
71	SECONDARY_HD*	3ISPU_400
72	SCSI*	3ISPU_400
75	FPRST*	3ISPU_400
80	PWRGD_PS	3ISPU_400
81	CPU_PRESENT*	3ISPU_400
83	SLP_S3*	3IS_400
84	SLP_S5*	3IS_400
87	SMB_CLK_M	3IOD6
88	SMB_CLK_R	3IOD6
89	SMB_DAT_M	3IOD6
90	SMB_DAT_R	3IOD6
124	5V_DDCSDA/GPIO8	5IOD6/3IO8
125	5V_DDCSCL/GPIO9	5IOD6/3IO8
126	3V_DDCSDA/GPIO10	3IOD6/3IO8
127	3V_DDCSCL/GPIO11	3IOD6/3IO8

SCSI ACTIVITY LED

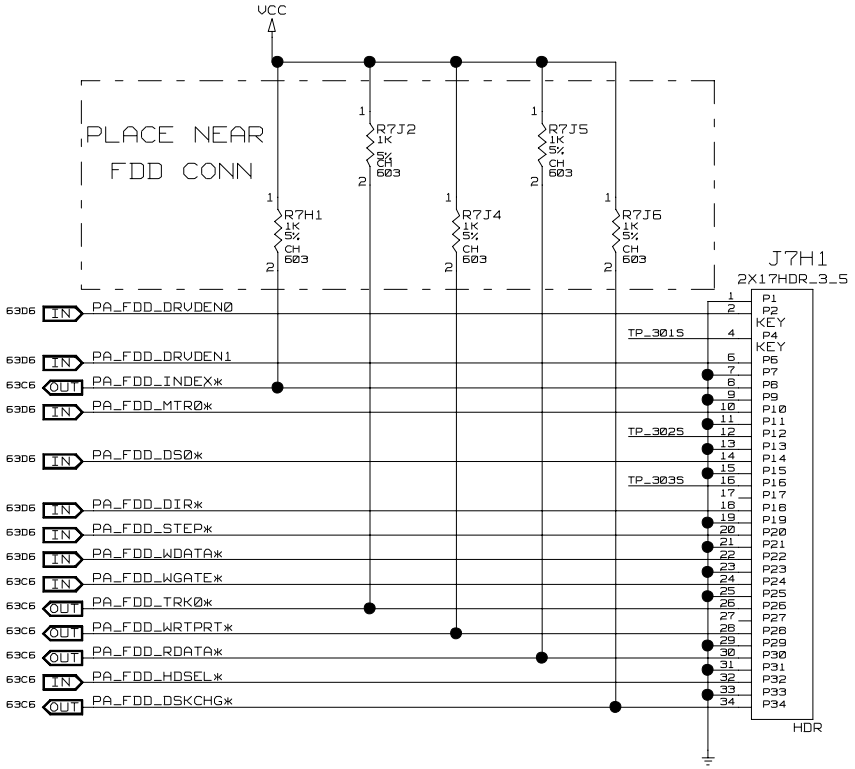




DRAWING
CANTERWOOD_CRB.SCH_1.64
Thu Apr 03 14:02:49 2003

SCHEMATIC TITLE:	INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	PORT ANGELES (2 OF 2)
REV:	1.2
INTEL	PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED:	01.07.2002
SHEET:	64/103

CR-65

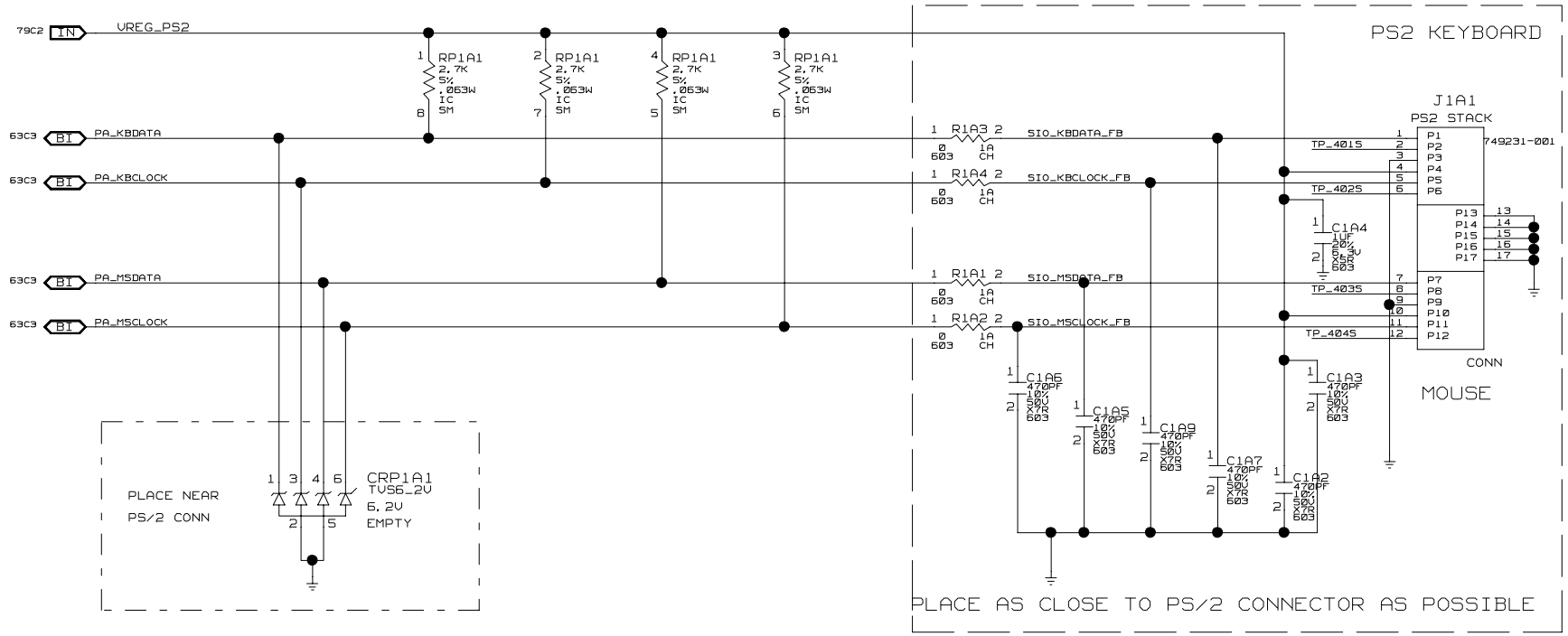


DRAWING
CANTERWOOD_CRB.SCH_1.65
Thu Apr 03 14:02:49 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: FDD CONN		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 65/103

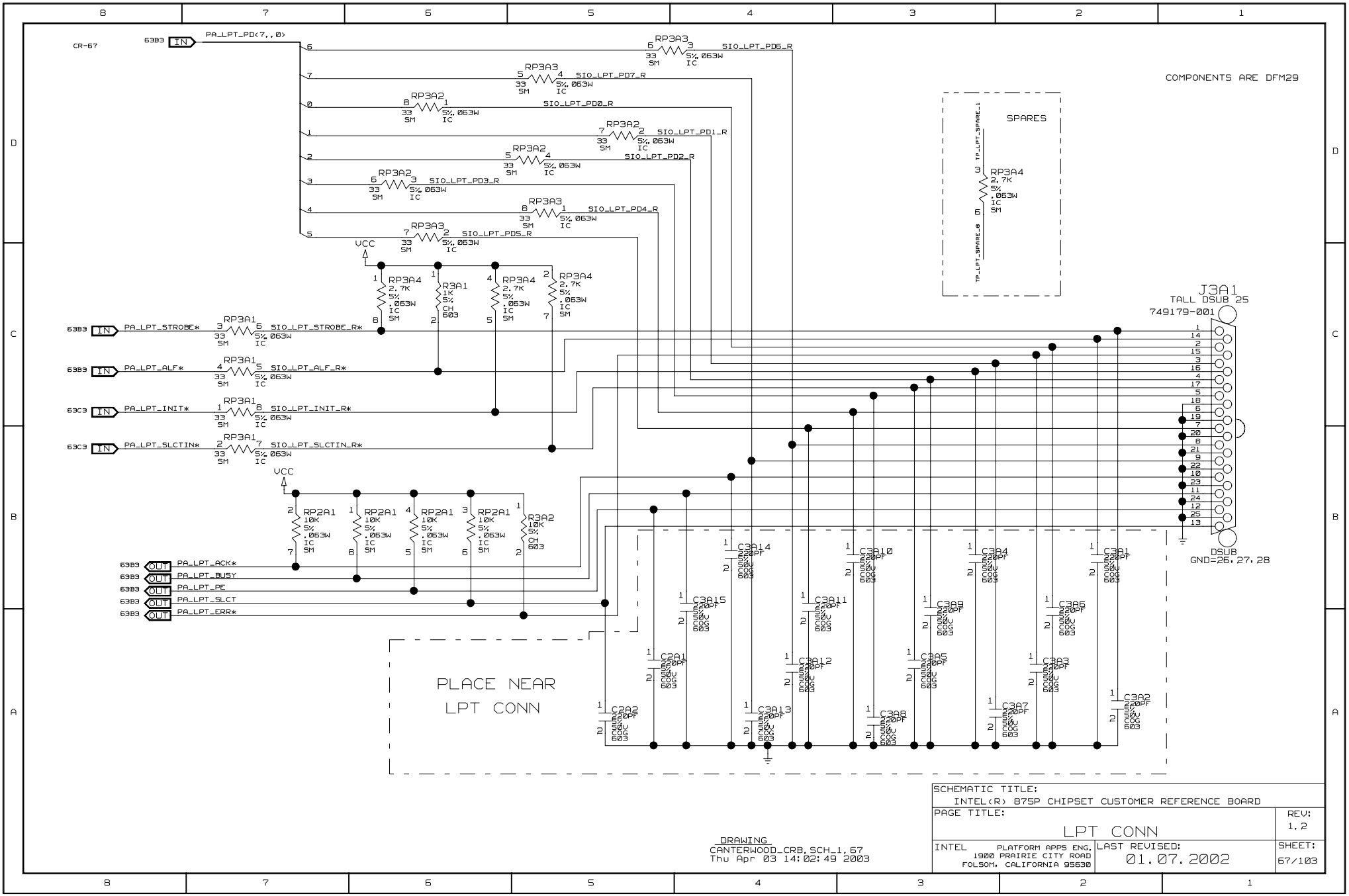
CR-66

COMPONENTS ARE DFM29



DRAWING
CANTERWOOD_CRB.SCH_1.66
Thu Apr 03 14:02:49 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: ATX DOUBLE-STACKED		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 66/103



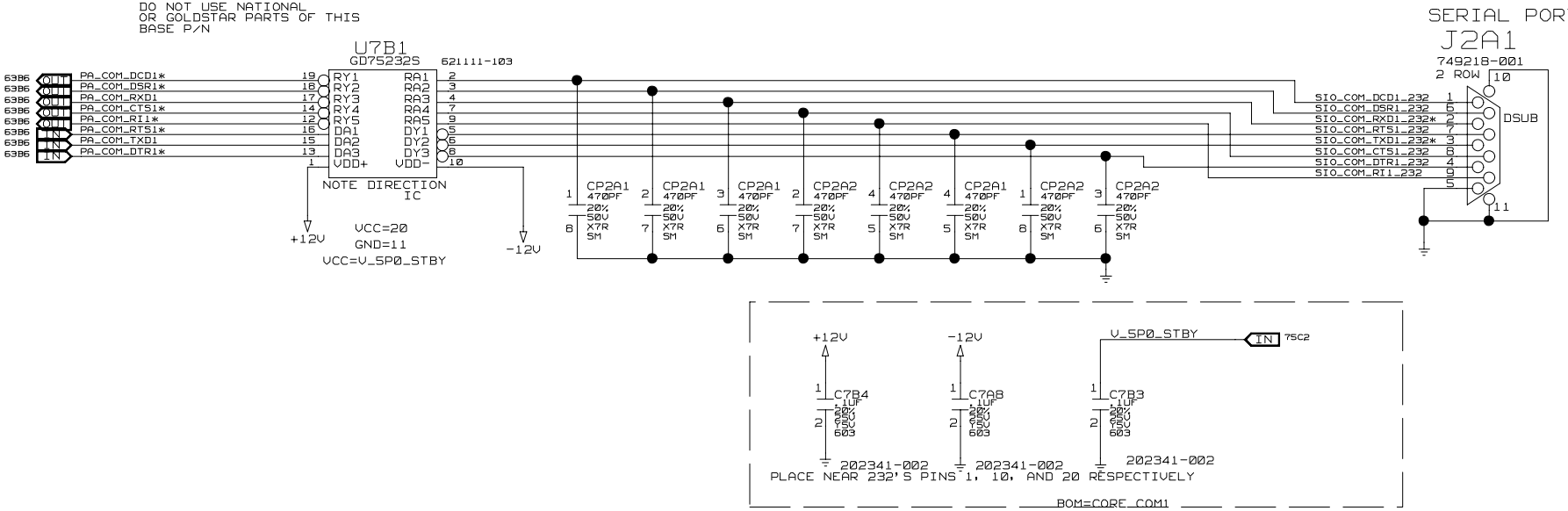
DRAWING
CANTERWOOD_CRB.SCH_1.67
Thu Apr 03 14:02:49 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: LPT CONN		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 67/103

CR-68

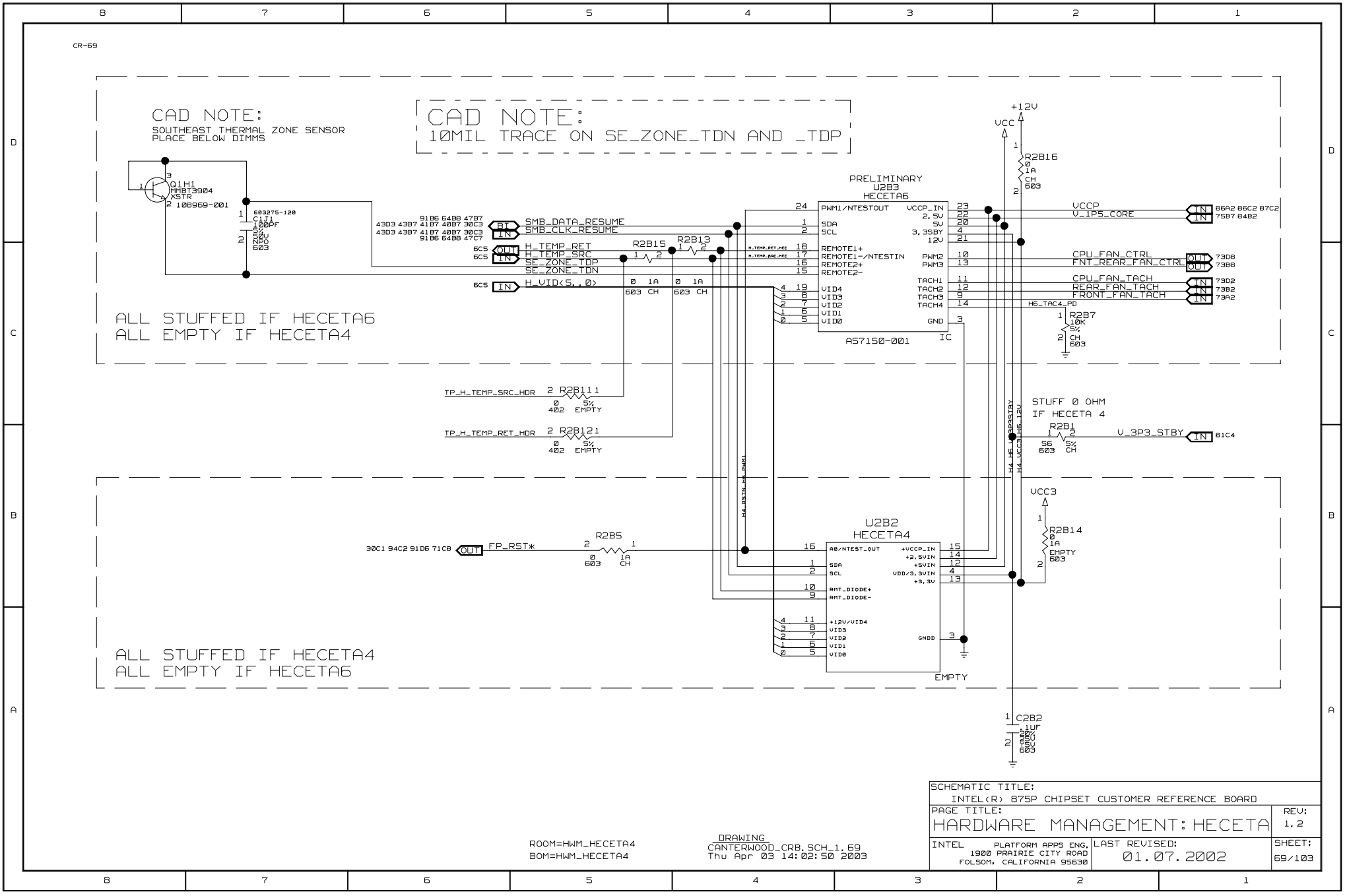
COMPONENTS ARE DFM31

DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N

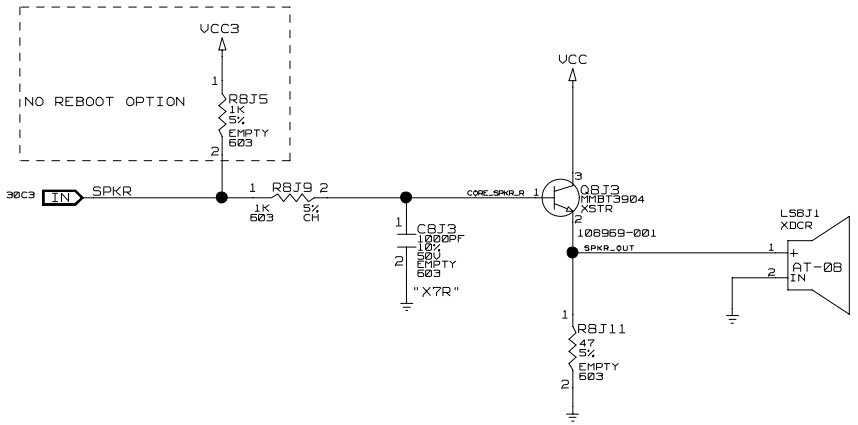


DRAWING
CANTERWOOD_CRB.SCH_1,68
Thu Apr 03 14:02:49 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: SERIAL PORT A		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 68/103


CR-69
CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS
CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP
Q1H1
MMBT3904
XSTR
108969-001
603275-120
C1J1
100PF
50V
NPO
603
SMB_DATA_RESUME
SMB_CLK_RESUME
H_TEMP_RET
H_TEMP_SRC
SE_ZONE_TDP
SE_ZONE_TDN
H_VID<5..0>
R2B15
R2B13
PRELIMINARY
U2B3
HECETA6
PWM1/NTESTOUT
SDA
SCL
REMOTE1+
REMOTE1-/NTESTIN
REMOTE2+
REMOTE2-
VID4
VID3
VID2
VID1
VID0
VCCP_IN
2.5V
5V
3.3SBY
12V
PWM2
PWM3
TACH1
TACH2
TACH3
TACH4
GND
A57150-001
IC
+12V
VCC
R2B16
VCCP
V_1P5_CORE
CPU_FAN_CTRL
FNT_REAR_FAN_CTRL
CPU_FAN_TACH
REAR_FAN_TACH
FRONT_FAN_TACH
H6_TAC4_PD
R2B7
10K
5%
CH
603
ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4
TP_H_TEMP_SRC_HDR
TP_H_TEMP_RET_HDR
R2B111
R2B121
0
5%
402
EMPTY
STUFF 0 OHM
IF HECETA 4
R2B1
56
V_3P3_STBY
VCC3
R2B14
EMPTY
U2B2
HECETA4
FP_RST#
R2B5
A0/NTEST_OUT
+VCCP_IN
+2.5VIN
+5VIN
VDD/3.3VIN
+3.3V
AMT_DIODE+
AMT_DIODE-
+12V/VID4
GNDD
EMPTY
ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6
C2B2
.1UF
10V
X7R
603
ROOM=HWM_HECETA4
BOM=HWM_HECETA4
DRAWING
CANTERWOOD_CRB.SCH,1,69
Thu Apr 03 14:02:50 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
HARDWARE MANAGEMENT: HECETA
REV:
1.2
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
01.07.2002
SHEET:
69/103

CR-70



DRAWING
CANTERWOOD_CRB.SCH_1.70
Thu Apr 03 14:02:50 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: SPEAKER		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 70/103

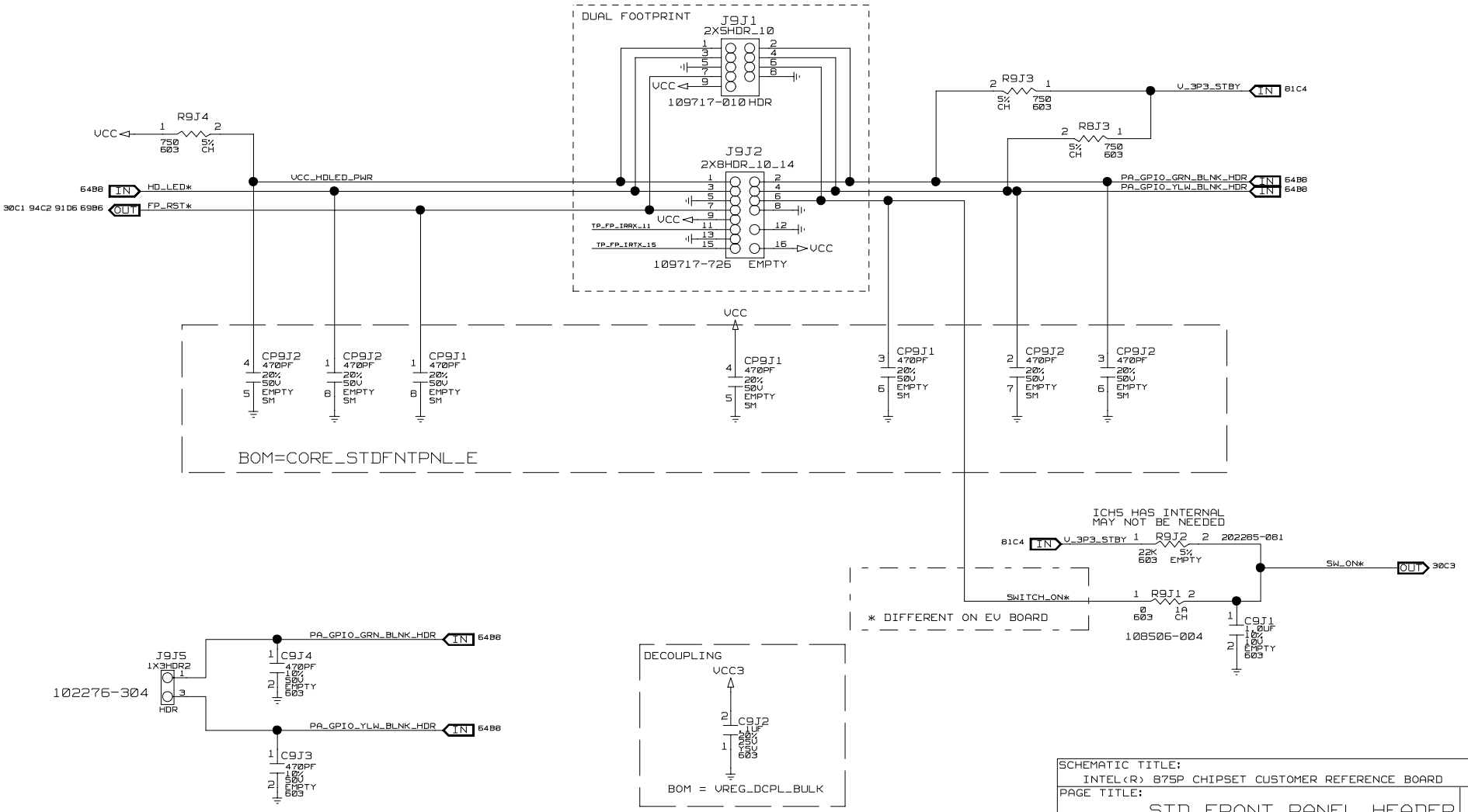
CR-71

LAST_USED:

R1105S
C1104S
J1101S

ATTRIBUTES:

BOM=SIO_STDFNTPNL
ROOM=SIO_STDFNTPNL



[PAGE_TITLE=STD_FRONT_PANEL]

DRAWING
CANTERWOOD_CRB.SCH,1,71
Thu Apr 18 14:02:50 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: STD FRONT PANEL HEADER		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 71/103

CR-72

PB MOUNTING HOLES

J1G1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J9J4
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J5G1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J5J2
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J9G1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J1B1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J5A2
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J9A1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

J1J1
MTG_HOLE
NC9 — 9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

LABELS

LB5F1
LABEL
1
A19177-001
1375X250_TARGET MAKE ISN ON BOM

LB6F1
SILK
1
INTELtm
EMPTY
'INTEL' LOGO SILKSCREEN
2.0 X 0.250
MAKE EMPTY ON BOM

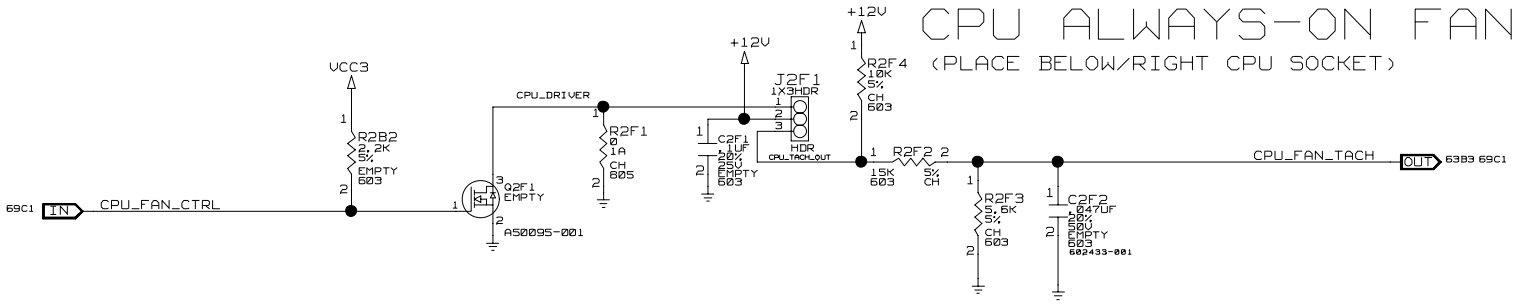
DRAWING
CANTERWOOD_CRB.SCH_1.72
Thu Apr 03 14:02:50 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: LABELS & HOLES		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 72/103

CR-73

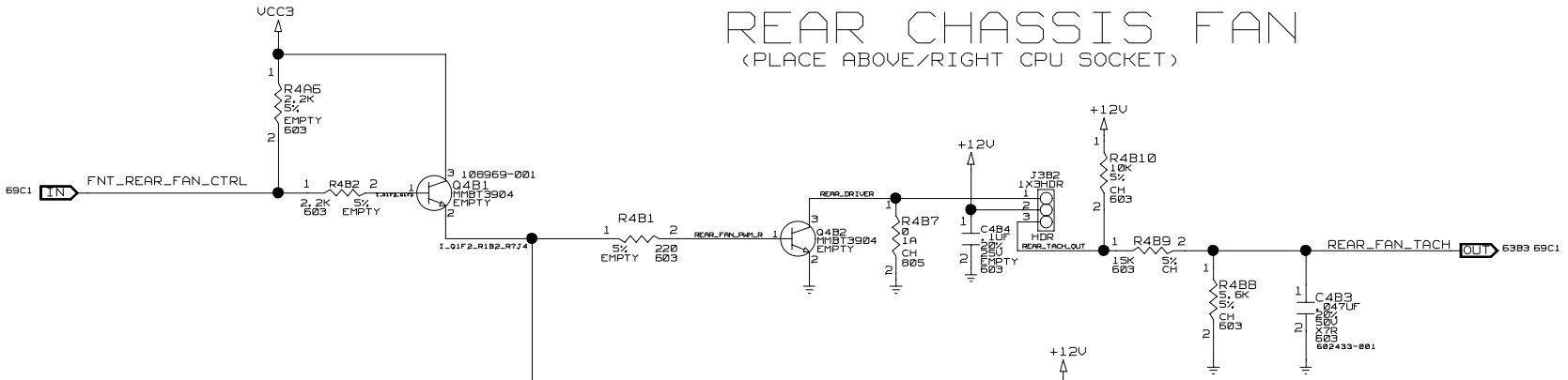
CPU ALWAYS-ON FAN

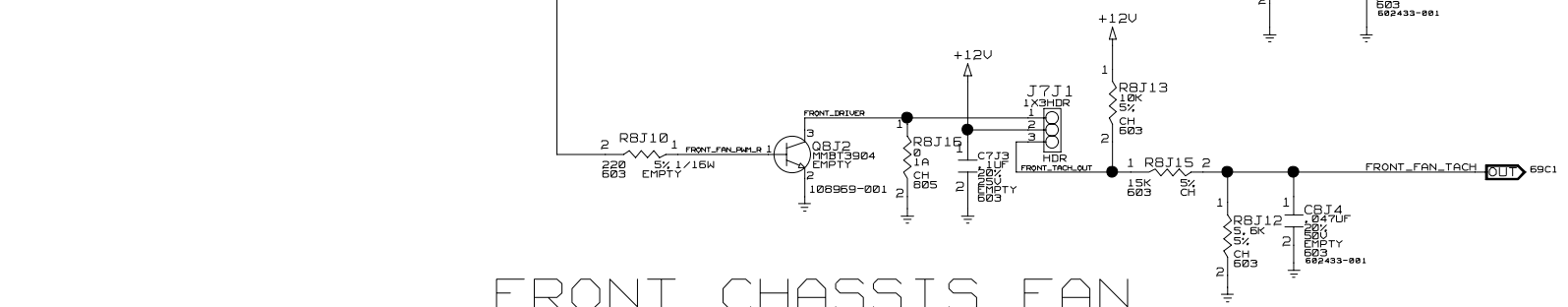
(PLACE BELOW/RIGHT CPU SOCKET)



REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)





FRONT CHASSIS FAN

(PLACE LOWER LEFT CORNER OF PLATFORM)

DRAWING
CANTERWOOD_CRB.SCH_1.73
Thu Apr 03 14:02:50 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: FAN CONTROL		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 73/103

CR-74

MCH
GMCH_VTT (1.2 OR 1.45V)
1.5 CORE
2.5 SM (S0 & S3)
3.3 (VCC3)

ICH 5
3.3 (VCC3)
1.5 CORE
3.3 STBY
5.0 STBY
1.35 (VCCP)

CK-409
3.3 (VCC3)

HEC6
3.3 STBY (VCC3 STBY)
5.0 (VCC)
12
1.35 (VCCP)
1.5 (CORE)

HEC4
3.3 STBY (VCC3 STBY)
5.0 (VCC)
3.3 (VCC3)
1.35 (VCCP)
1.5 (CORE)

PORT ANGELES
3.3 (VCC3)
5.0 (VCC)
3.3 STBY (VCC3 STBY)
5.0 STBY (VCC STBY)

82547EI/82562EZ
1.2 LAN
1.8 LAN
3.3 PCIVAUX
3.3 STBY (VCC3 STBY)

FWH
3.3 (VCC3)

DIMMS
2.5 SM (S0 & S3)
1.25 (MEM_VTT)

VREG_12V_FILTERED (+12V FILTERED FROM 12V POWER-SUPPLY)
VCCP (FOR CPU 1.29 - 1.45V)
V_1P25_MEMVTT (1.25V DERIVED FROM V_2.5)
V_2P5_SM (2.5V DERIVED FROM VCC)
VREG_USB_BP_LEFT (5.0 FROM VCC OR 5.0-STANDBY)
VREG_USB_BP_RIGHT (5.0 FROM VCC OR 5.0-STANDBY)
VREG_PS2 (5.0 FROM VCCC OR 5.0-STANDBY)
USB_FNT_PWR (5.0 FROM VCC OR 5.0-STANDBY)
USB_CNR_PWR (5.0 FROM VCC OR 5.0-STANDBY)
V_3P3_PCI_VAUX (3.3V OR 3.3-STANDBY SOURCE)
V_3P3_STBY (3.3V DERIVED FROM 5.0-STANDBY)
V_5P0_STBY (5.0V STANDBY FROM POWER-SUPPLY)
V_BAT_VREG_R_CR (3.0V FROM THE BATTERY)
V_3P0_BAT_VREG (~3.0V FROM THE BATTERY THROUGH A DIODE)
+12V (PLUS 12V FROM POWER-SUPPLY)
-12V (MINUS 12V FROM POWER-SUPPLY)
VCC3 (3.3V FROM POWER-SUPPLY)
VCC (5.0V FROM POWER-SUPPLY)
LAN_V_1P2 (1.2V DERIVED FROM 3.3PCIVAUX)
LAN_V_1P8 (1.8V DERIVED FROM 3.3PCIVAUX)

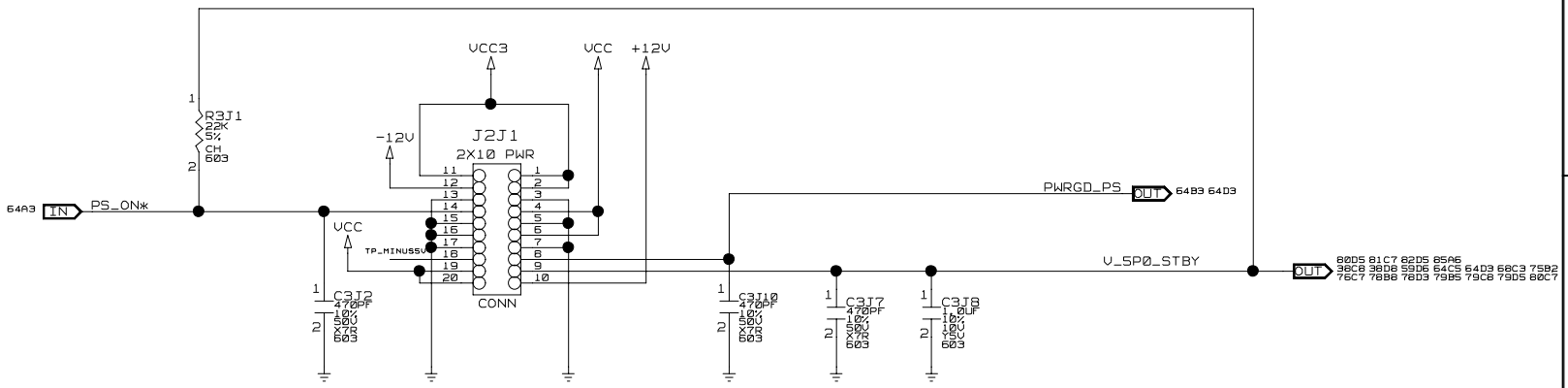
V_1P5_CORE (NOT CONNECTED)
V_1P25_MEMVTT_B (NOT CONNECTED)
V_1P3_NOMINAL (NOT CONNECTED)
V_1P5_AGP (DERVIVED FROM 1.5V CORE) (NOT CONNECTED)
V_12VREG (NOT CONNECTED)
V_AGP_VDDQ (DERVIVED FROM 1.5V CORE) (NOT CONNECTED)

DRAWING
CANTERWOOD_CRB.SCH_1.74
Thu Apr 03 14:02:50 2003

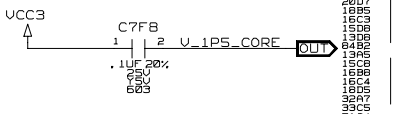
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: VREG: VOLTAGE DISTRIBUTION		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 74/103

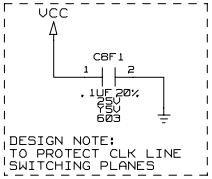
CR-75

ROOM=VREG_PWR_CONN
BOM=VREG_PWR_CONN
UNLESS OTHERWISE SPECIFIED

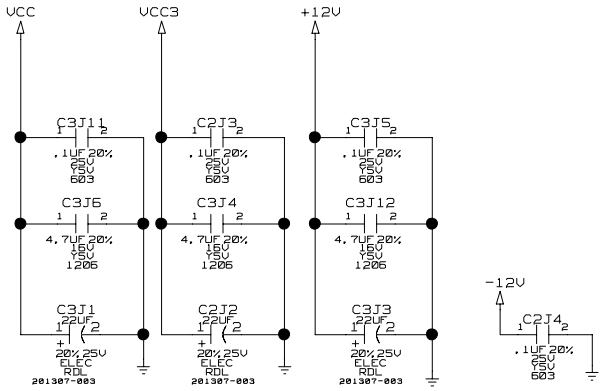


STITCHING CAPS

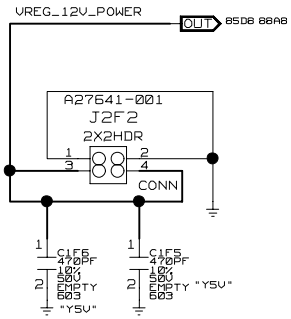


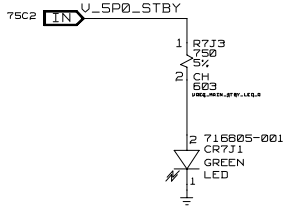


69D1
91A4
92C3
20D7
18B5
16C3
15D8
13D8
84B2
13A5
15C8
16B8
16C4
18D5
32A7
33C5
51C4
84A5
84A8
84B2
92B7



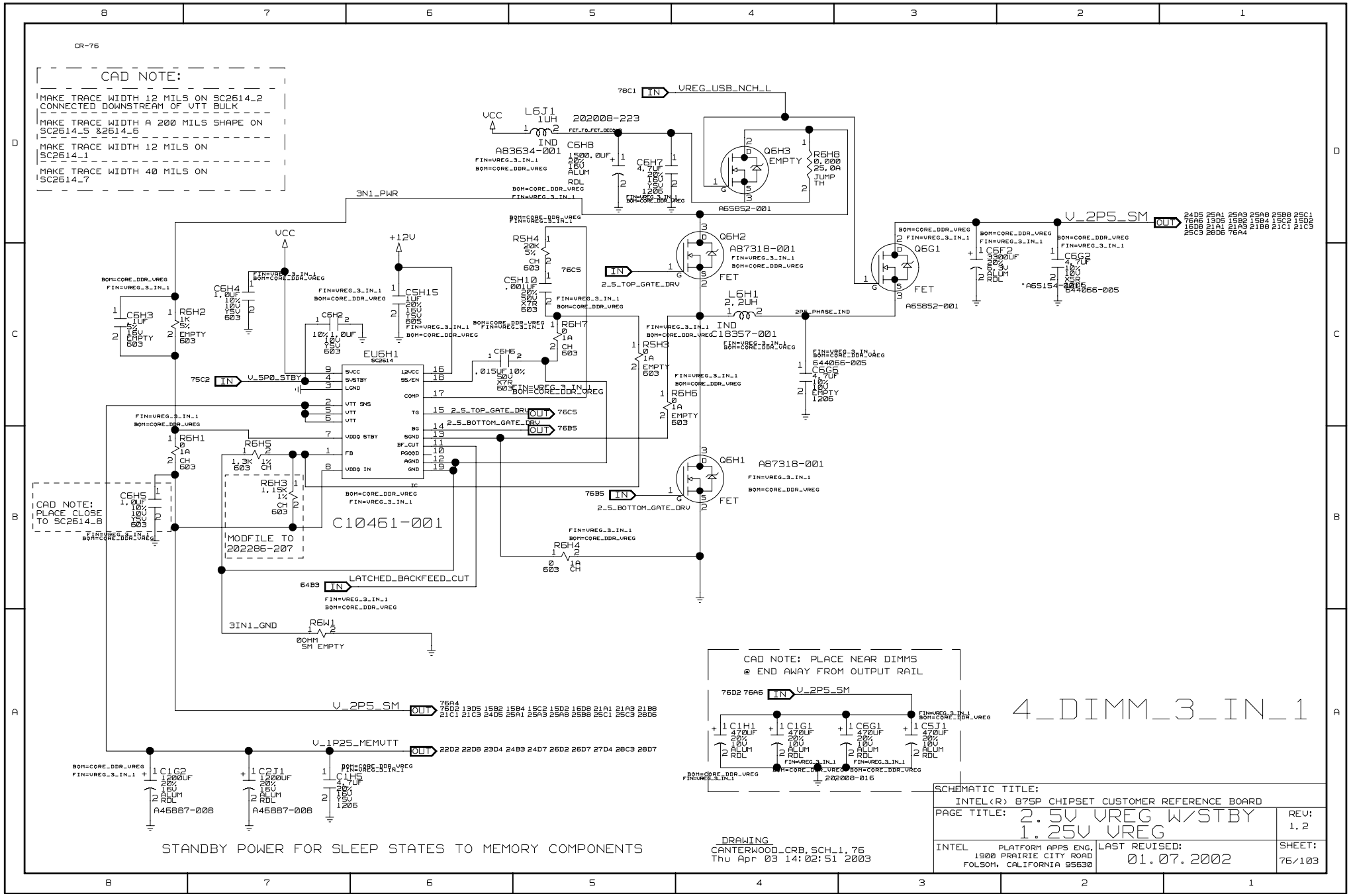
POWER CONNECTOR DECOUPLING





DRAWING
CANTERWOOD_CRB.SCH_1.75
Thu Apr 03 14:02:50 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: STANDARD POWER CONNECTOR		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 75/103


CR-76
CAD NOTE:
MAKE TRACE WIDTH 12 MILS ON SC2614_2 CONNECTED DOWNSTREAM OF VTT BULK
MAKE TRACE WIDTH A 200 MILS SHAPE ON SC2614_5 &2614_6
MAKE TRACE WIDTH 12 MILS ON SC2614_1
MAKE TRACE WIDTH 40 MILS ON SC2614_7
VREG_USB_NCH_L
VCC
L6J1 1UH
202008-223
IND A83634-001
C6H8 1500.0UF 20% 16V ALUM RDL
C6H7 4.7UF 20% 16V Y5V 1206
Q6H3 EMPTY
R6H8 0.000 25.0A JUMP TH
A65852-001
3N1_PWR
Q6H2 A8731B-001 FET
2_5_TOP_GATE_DRV
Q6G1 FET
A65852-001
C6F2 330UF 20% 2.5V ALUM RDL
C6G2 4.7UF 10% 10V X5R 1206
"A65154-0205 644066-005
V_2P5_SM
24D5 25A1 25A3 25A8 25B8 25C1 76A5 13D5 15B2 15B4 15C2 15D2 16D8 21A1 21A3 21B8 21C1 21C3 25C3 28D6 76A4
R5H4 20K 5% CH 603
76C5
C5H10 .001UF 10% 50V X7R 603
C5H15 1UF 20% 10V Y5V 805
+12V
C6H4 1.0UF 10% 10V Y5V 603
C6H2 1.0UF 10% 10V Y5V 603
C6H3 .1UF 5% 16V EMPTY 603
R6H2 1K 5% EMPTY 603
L6H1 2.2UH
IND C18357-001
2P5_PHASE_IND
R5H3 0 1A EMPTY 603
R6H6 0 1A EMPTY 603
R6H7 0 1A CH 603
C6H6 .015UF 10% 50V X7R 603
C6G5 4.7UF 10% 10V EMPTY 1206
644056-005
75C2 V_5P0_STBY
EU6H1 SC2614
SVCC
SVSTBY
LGND
VTT SNS
VTT
VTT
VDDQ STBY
FB
VDDQ IN
12VCC
SS/EN
COMP
TG
BG
SGND
BF_CUT
PGOOD
AGND
GND
TC
2_5_TOP_GATE_DRV OUT 76C5
2_5_BOTTOM_GATE_DRV OUT 76B5
R6H1 0 1A CH 603
R6H5 1.3K 1% CH 603
R6H3 1.15K 1% CH 603
C6H5 1.0UF 10% 10V Y5V 603
CAD NOTE: PLACE CLOSE TO SC2614_8
MODFILE TO 202286-207
C10461-001
Q6H1 A8731B-001 FET
76B5 IN 2_5_BOTTOM_GATE_DRV
R6H4 0 1A CH 603
64B3 IN LATCHED_BACKFEED_CUT
3IN1_GND
R6W1 0OHM SM EMPTY
V_2P5_SM OUT 76A4 76D2 13D5 15B2 15B4 15C2 15D2 16D8 21A1 21A3 21B8 21C1 21C3 24D5 25A1 25A3 25A8 25B8 25C1 25C3 28D6
V_1P25_MEMVTT OUT 22D2 22D8 23D4 24B3 24D7 26D2 26D7 27D4 28C3 28D7
C1G2 1200UF 20% 16V ALUM RDL A45887-008
C2J1 1200UF 20% 16V ALUM RDL A45887-008
C1H5 4.7UF 20% 16V Y5V 1206
CAD NOTE: PLACE NEAR DIMMS @ END AWAY FROM OUTPUT RAIL
76D2 76A6 IN V_2P5_SM
C1H1 470UF 20% 10V ALUM RDL
C1G1 470UF 20% 10V ALUM RDL
C5G1 470UF 20% 10V ALUM RDL
C5J1 470UF 20% 10V ALUM RDL
202008-016
4_DIMM_3_IN_1
STANDBY POWER FOR SLEEP STATES TO MEMORY COMPONENTS
DRAWING
CANTERWOOD_CRB.SCH_1.76
Thu Apr 03 14:02:51 2003
SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE: 2.5V VREG W/STBY
1.25V VREG
REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED: 01.07.2002
SHEET: 76/103

[FULL_ID=1272-79-22132][PAGE_INFO_ID=22132] [OWNED_BY=DE] [MODULE_ID=1130-63-15252xDOMOR_ID=1200-71-17898]

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[PAGE_TITLE=BLANK]

DRAWING
CANTERWOOD_CRB.SCH_1.77
Thu Apr 03 14:02:51 2003

SCHEMATIC TITLE:	INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002
	SHEET: 77/103

[DONOR_REV=0.11/page79]
[DONOR_PROJ=NPAVP_GL_A--1200]
[PROJ_REV=0.01/page79]
[PROJ_NAME=NGAVP_A--1272]
[MODULE=NONE]
[LAST_MAKEPROJ: 10/23/2001 10:47:46 AM]

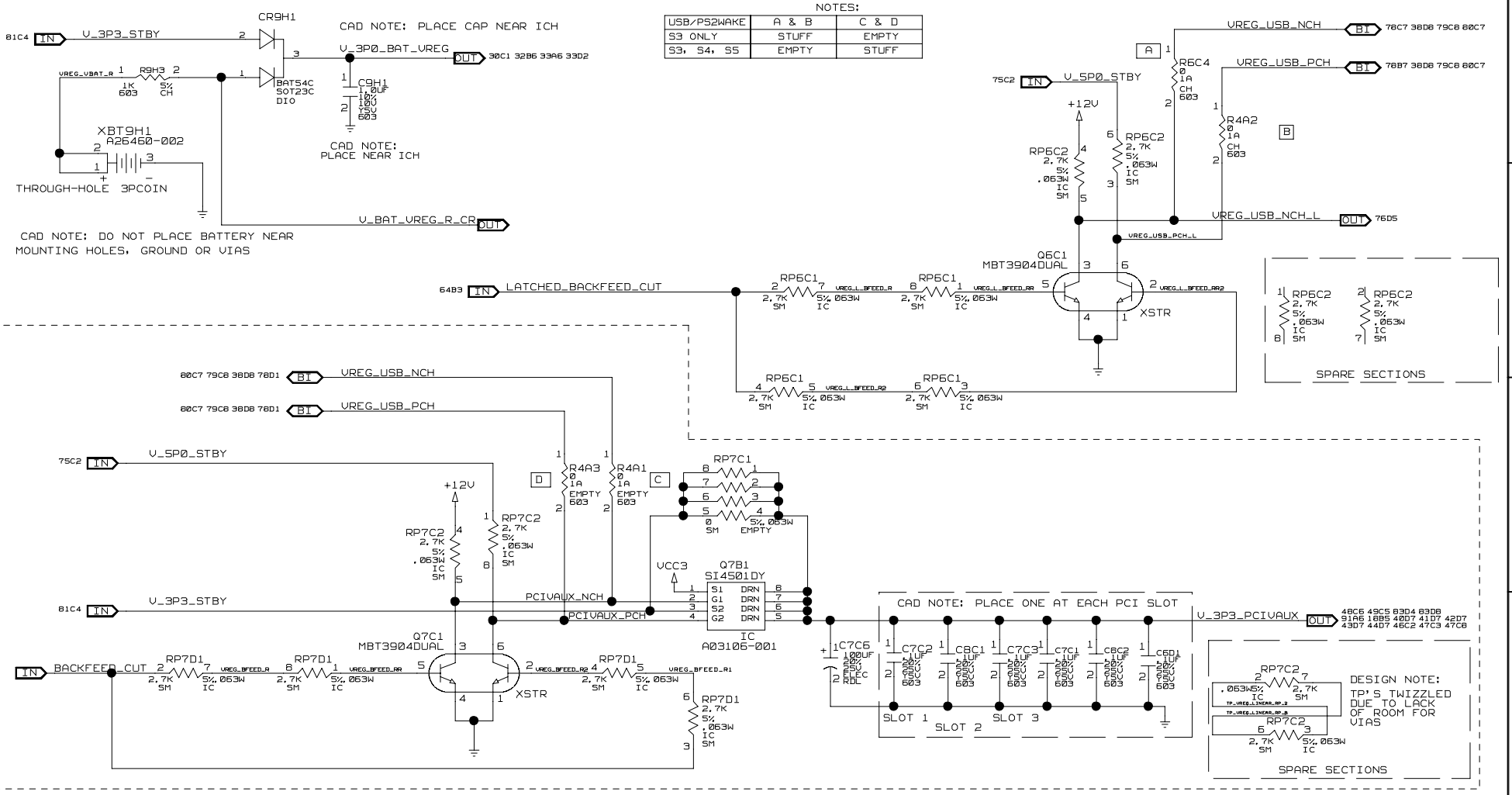
CR-78

BATTERY

BOM=VREG
ROOM = VREG UNLESS SPECIFIED

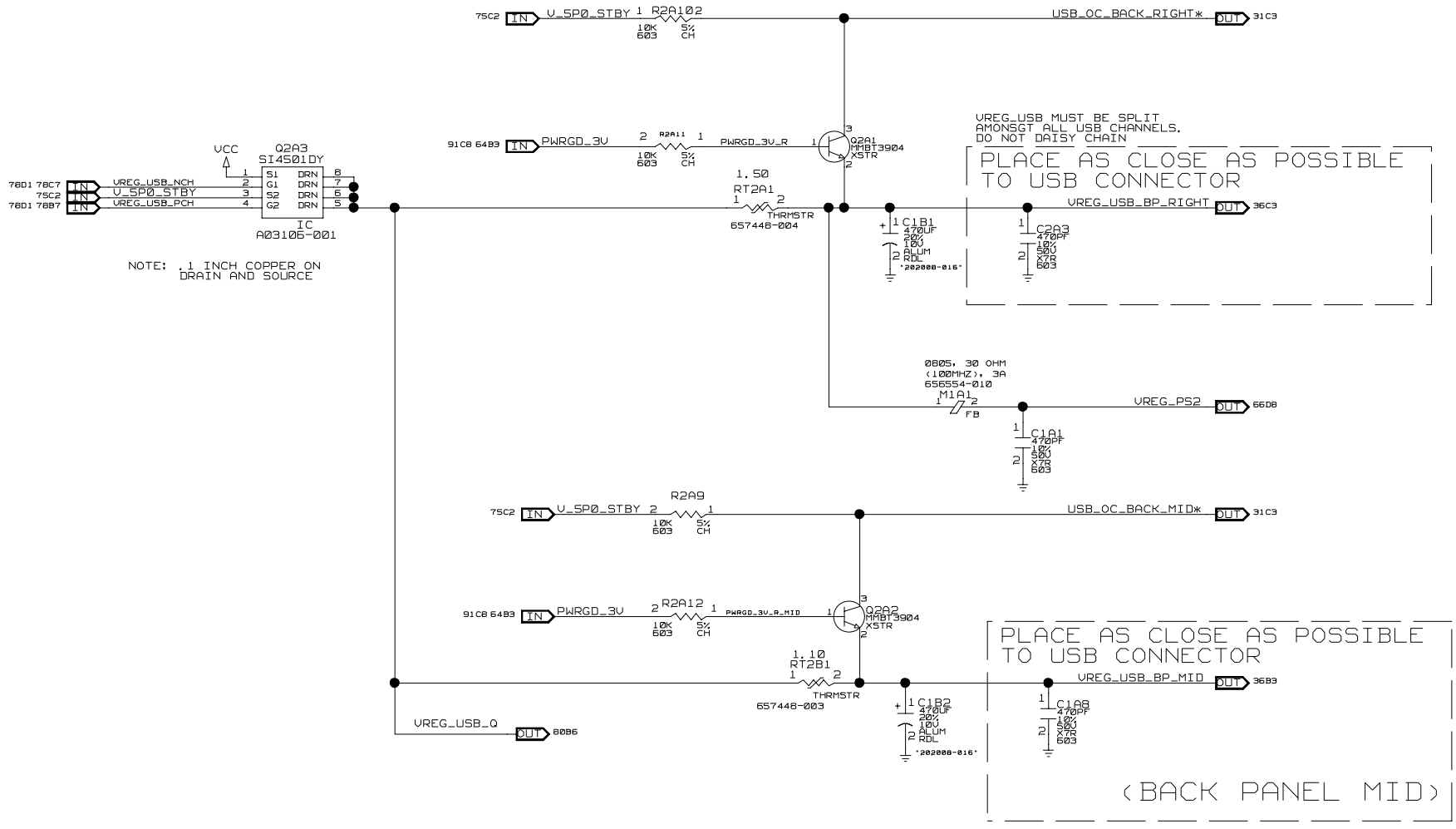
NOTES:

USB/PS2WAKE	A & B	C & D
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF



DRAWING
CANTERWOOD_CRB.SCH_1.78
Thu Apr 03 14:02:51 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI VAUX		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 78/103

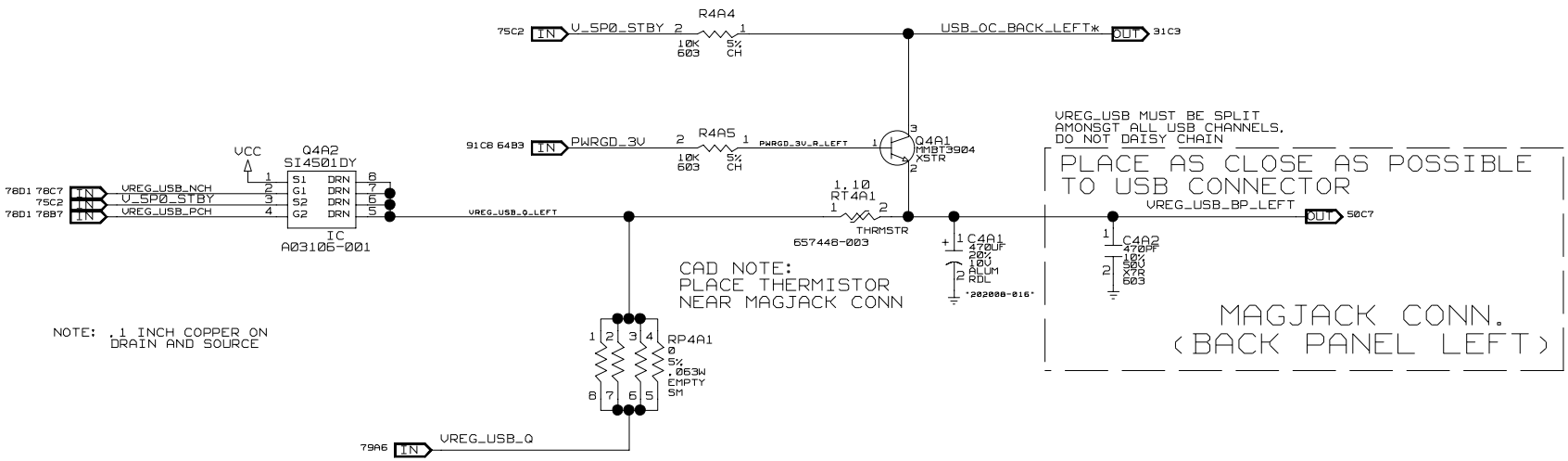


DRAWING
CANTERWOOD_CRB.SCH_1.79
Thu Apr 03 14:02:51 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: WAKE ON PS2 & USB (BACK PANEL RIGHT) WAKE ON USB (BACK PANEL LEFT)		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 79/103

CR-80

BOM=USB
ROOM= USB_BP_LEFT
UNLESS OTHERWISE SPECIFIED

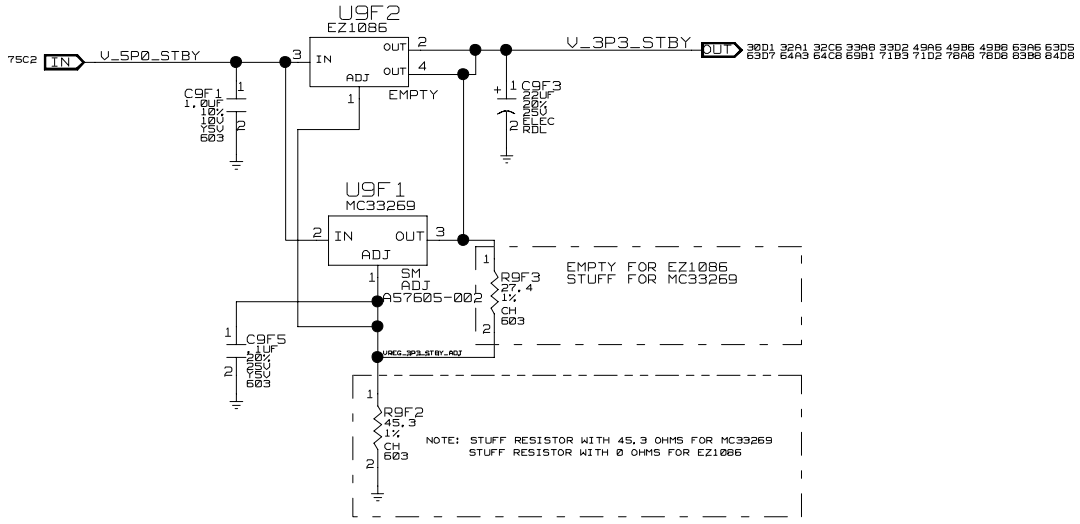


DRAWING
CANTERWOOD_CRB.SCH_1.80
Thu Apr 03 14:02:51 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: MAGJACK CONN. WAKE ON USB (BACK PANEL LEFT)		REV: 1.3
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 80/103

CR-81

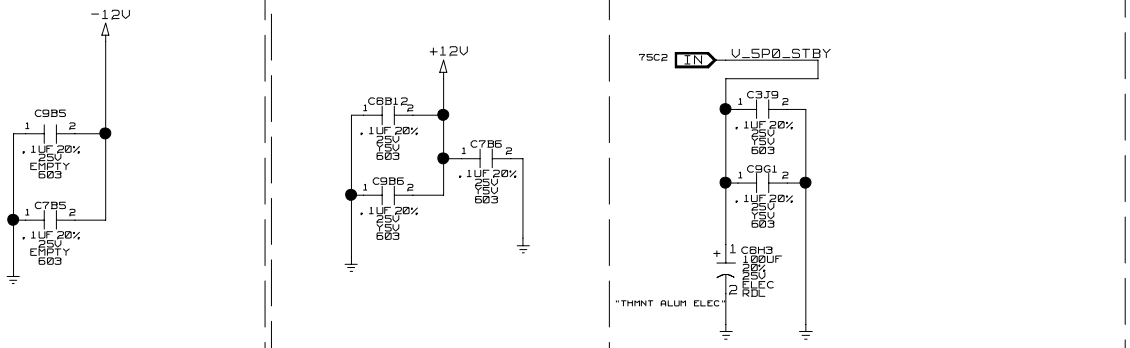
BOM = VREG
ROOM = VREG
UNLESS OTHERWISE SPECIFIED

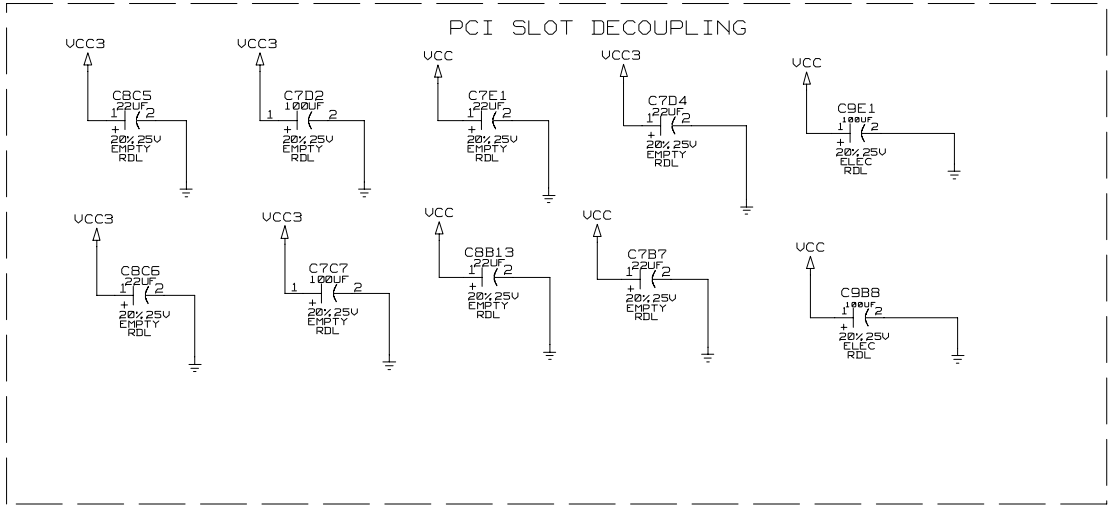


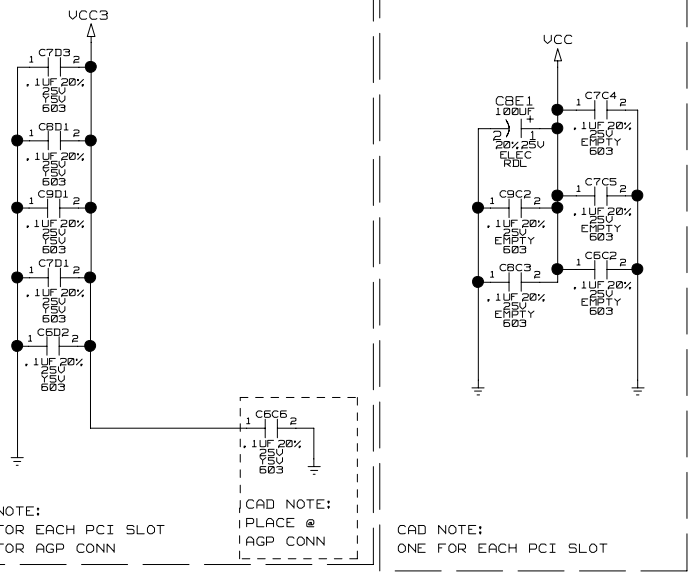
DRAWING
CANTERWOOD_CRB.SCH_1.81
Thu Apr 03 14:02:52 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: 3.3V STANDBY		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 81/103

CR-82







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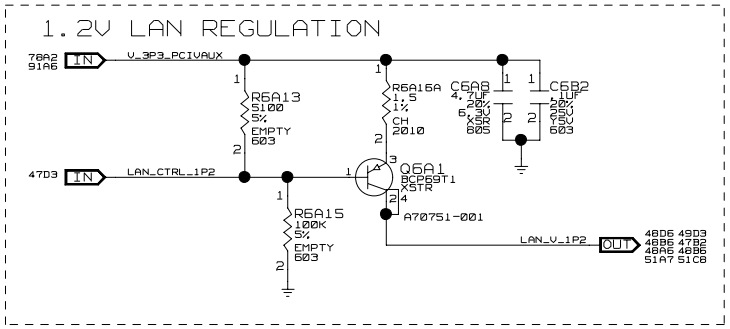
CANTERWOOD_CRB.SCH_1.82
ROOM=DCPL_BULKThu Apr 03 14:02:52 2003
BOM=VREG_DCPL_BULK

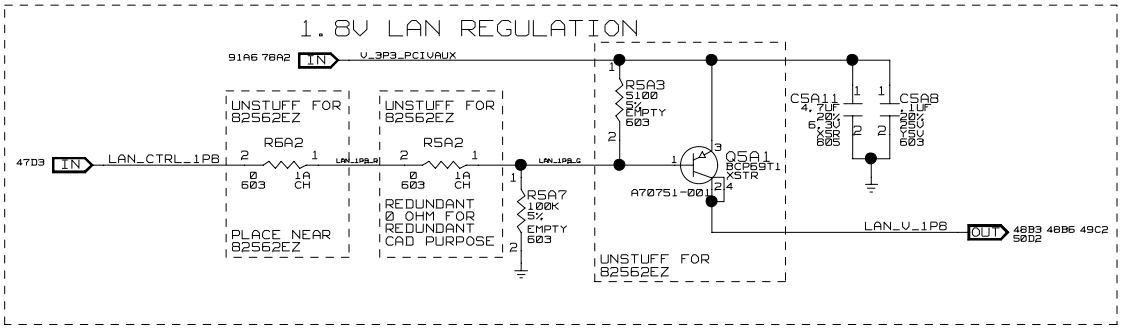
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: VREG_DCPL_BULK		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 82/103

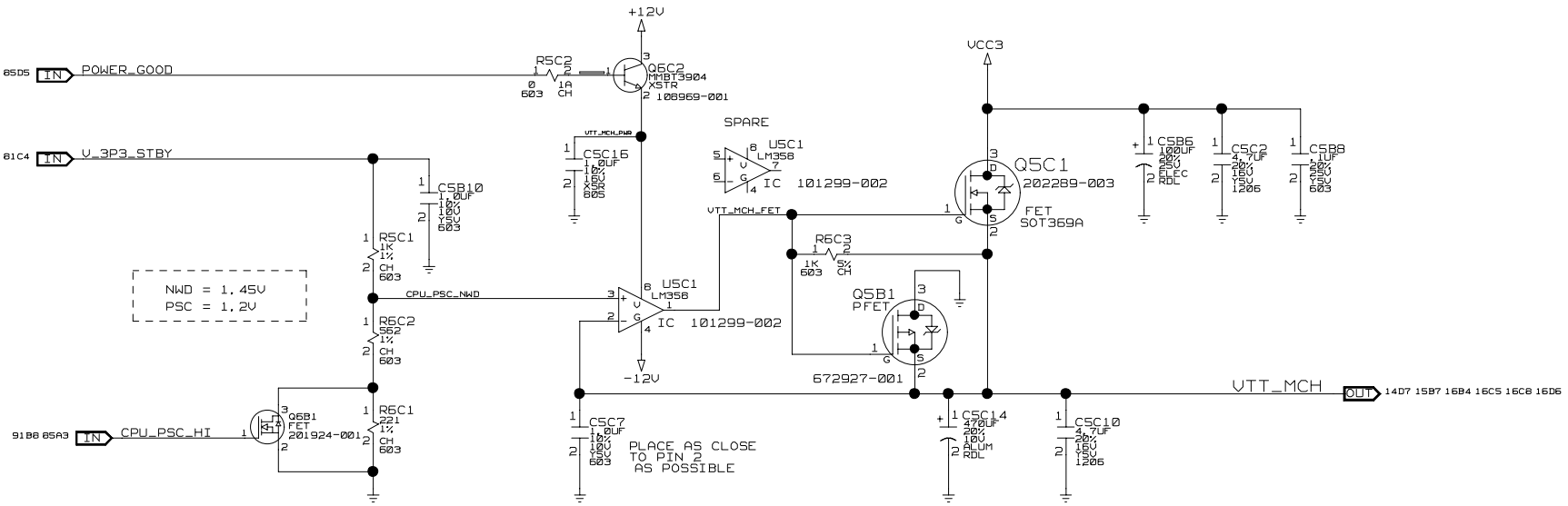
CR-83

1.2V LAN REGULATION



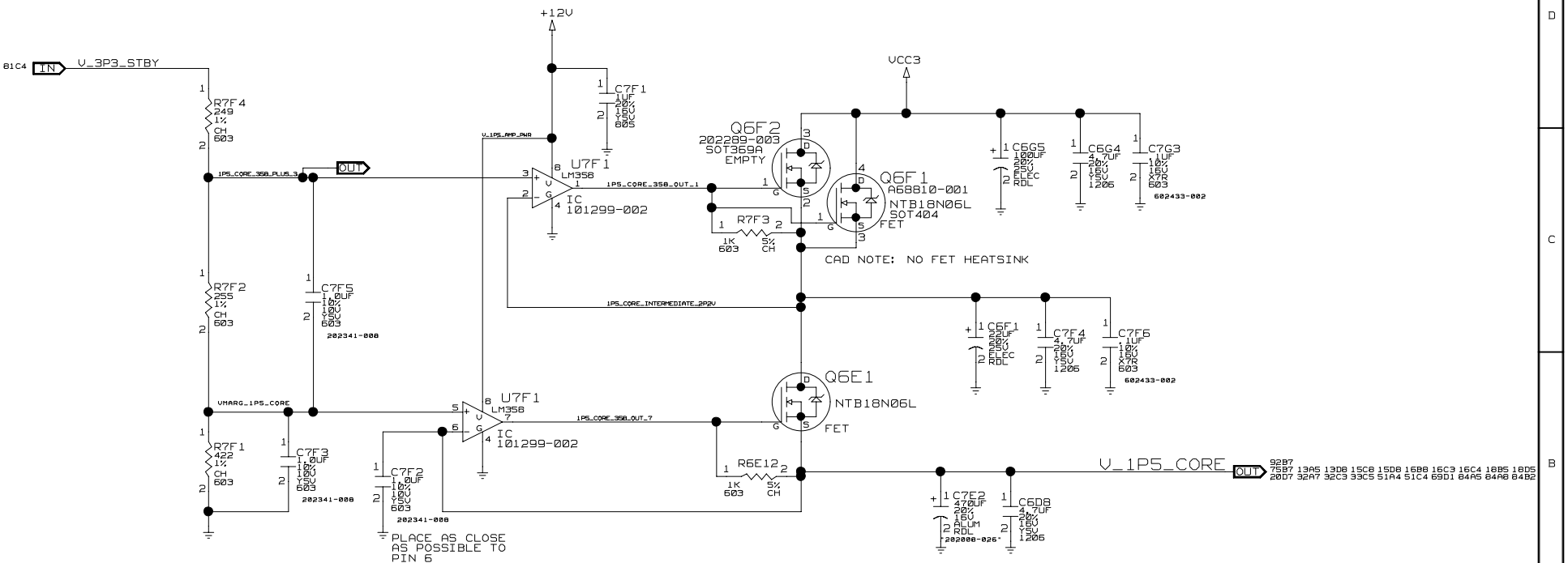
1.8V LAN REGULATION





DRAWING
CANTERWOOD_CRB.SCH_1.83
Thu Apr 03 14:02:52 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: LAN VREG MCH VTT		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 83/103



[PAGE_TITLE=1.5VOLT]

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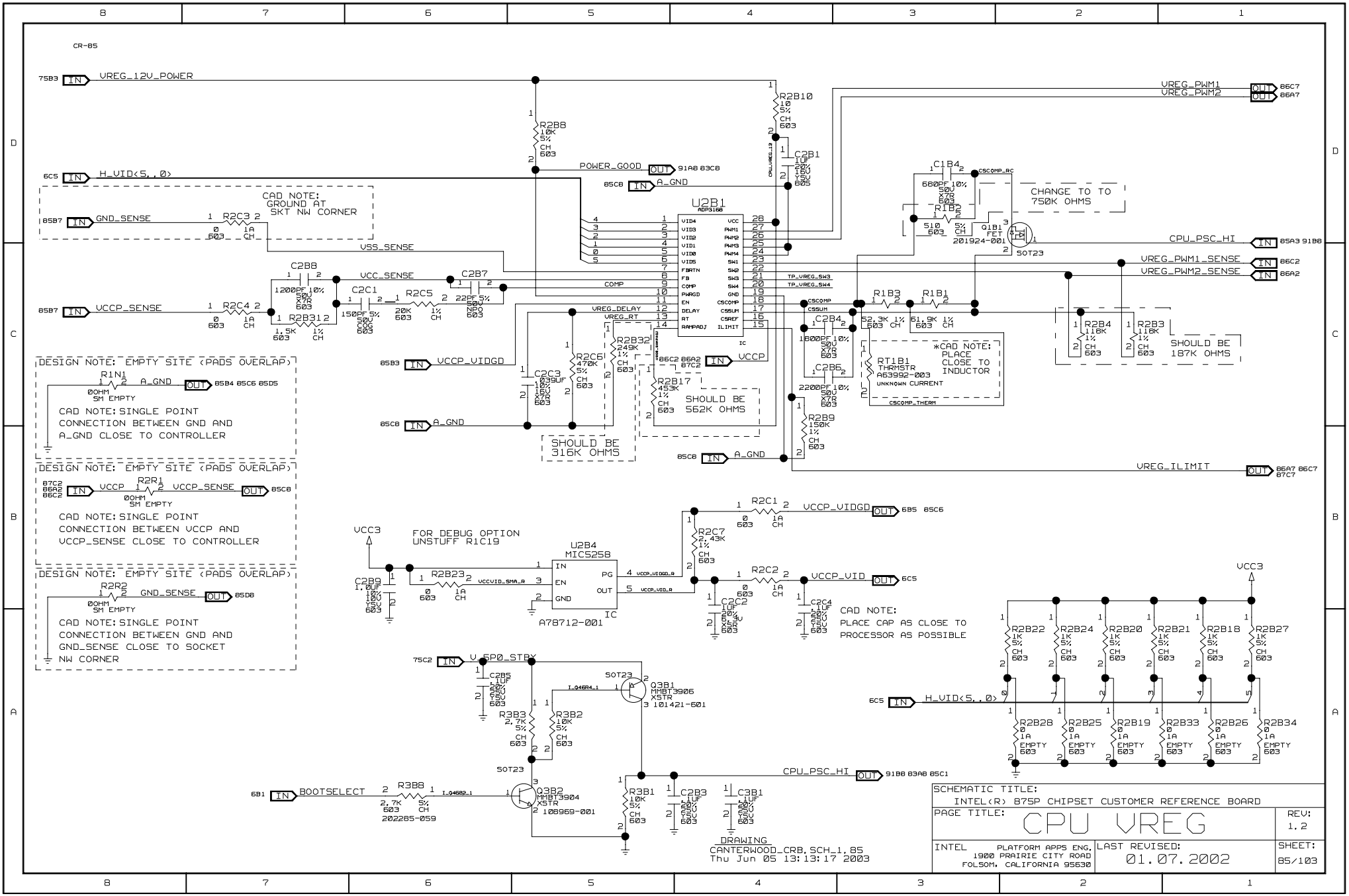
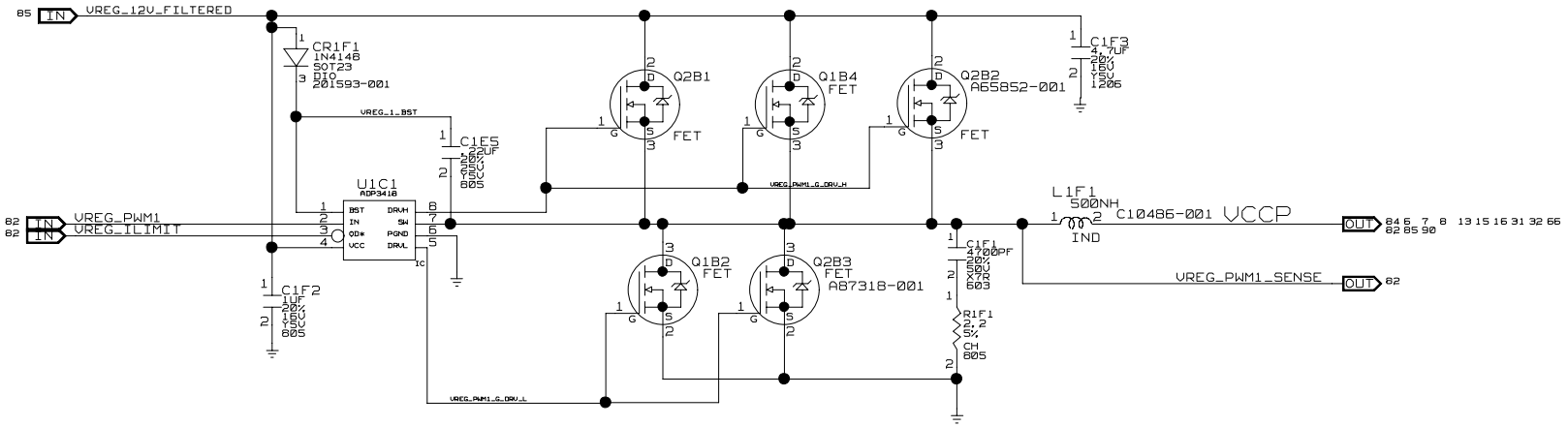
CANTERWOOD_CRB.SCH_1.84
Thu Apr 03 14:02:52 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: 1.5V CORE		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 84/103


CR-85
VREG_12V_POWER
H_VID<5,,0>
GND_SENSE
VSS_SENSE
VCC_SENSE
VCCP_SENSE
POWER_GOOD
A_GND
VREG_PWM1
VREG_PWM2
CPU_PSC_HI
VREG_PWM1_SENSE
VREG_PWM2_SENSE
VREG_ILIMIT
VCCP_VIDGD
VCCP
VCCP_VID
VCC3
V_5P0_STBY
BOOTSELECT
CAD NOTE: GROUND AT SKT NW CORNER
CHANGE TO TO 750K OHMS
SHOULD BE 187K OHMS
SHOULD BE 562K OHMS
SHOULD BE 316K OHMS
*CAD NOTE: PLACE CLOSE TO INDUCTOR
DESIGN NOTE: EMPTY SITE (PADS OVERLAP)
CAD NOTE: SINGLE POINT CONNECTION BETWEEN GND AND A_GND CLOSE TO CONTROLLER
CAD NOTE: SINGLE POINT CONNECTION BETWEEN VCCP AND VCCP_SENSE CLOSE TO CONTROLLER
CAD NOTE: SINGLE POINT CONNECTION BETWEEN GND AND GND_SENSE CLOSE TO SOCKET NW CORNER
FOR DEBUG OPTION UNSTUFF R1C19
CAD NOTE: PLACE CAP AS CLOSE TO PROCESSOR AS POSSIBLE
U2B1 ADP3168
U2B4 MIC5258 A78712-001
Q3B1 MMBT3906 XSTR 101421-601
Q3B2 MMBT3904 XSTR 100969-001
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE: CPU VREG
REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630
LAST REVISED: 01.07.2002
SHEET: 85/103
DRAWING CANTERWOOD_CRB.SCH_1.85 Thu Jun 05 13:13:17 2003

CR-86



DRAWING
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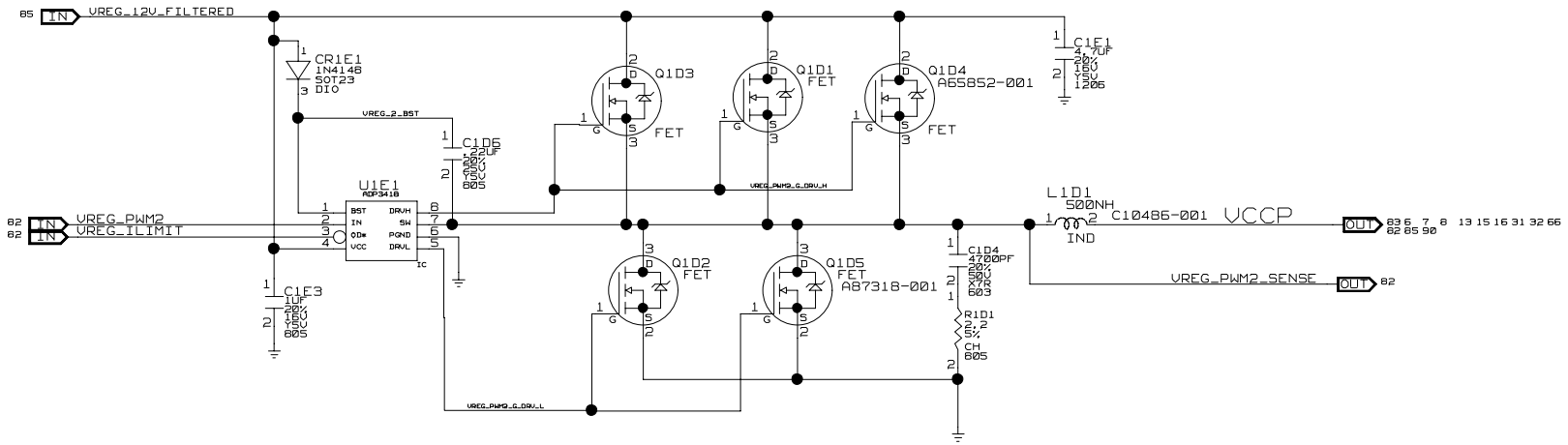
Thu Apr 03 14:02:53 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU VREG		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 86/103

CR-87



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Thu Apr 03 14:02:53 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU VREG		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 87/103

CR-88

CAD NOTE: PLACE AS MANY 1206 CAPACITORS AS POSSIBLE WITHIN CPU CAVITY

87C2 86C2 86A2 IN VCCP

644066-024

C3C1 C3C2 C3C3 C3C4 C3D1 C3D6 C3D8 C3D10 C3D12 — WESTERN DECOUPLING

C2C6 C2C7 C2C8 C2C9 C2C10 C2C11 C2C12 C2D6 C2D3 C2D4 — EASTERN DECOUPLING

C3D2 C3D3 C3D4 C3D5 C2D1 C2D2 C3D13 C3D14 C3D15 C3D16 C2D11 C2D12 — SOCKET DECOUPLING

C2D5 C2D8 C2D9 C2D10 C2D13 C2D14 C2D15 C2D7 C2C5 — EASTERN DECOUPLING

C1E2 C1D5 C1C3 C1D2 C1B8 C1C4 C1B9 C1D1 C1C5 C1E4

628955-024

PLACE NORTH OF SOCKET

PLACEMENT NOTE FOR 1206:
PLACE 19 EAST OF SOCKET (STUFF 6)
PLACE 12 INSIDE CPU SOCKET (STUFF ALL)
PLACE 9 WEST OF SOCKET (STUFF ALL)

MODFILED TO -027 UNTIL SPEC AND MODEL AVAILABLE

7SB3 IN VREG_12V_POWER

L1F2 1UH IND A83634-001

C1C2 C1B3 C1D3 C1F4 1200UF 20% 16V ALUM RDL

A46887-012

VREG_12V_FILTERED OUT 86B7 86D7 87D7

DRAWING
CANTERWOOD_CRB.SCH_1,88
Thu Apr 03 14:02:53 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU VREG DECOUPLING		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 88/103

CR-89

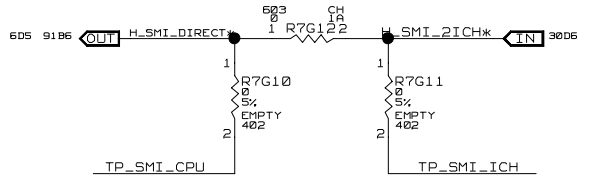
DEBUG PAGES

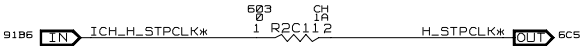
DRAWING
CANTERWOOD_CRB.SCH_1.89
Thu Apr 03 14:02:53 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE:		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 89/103

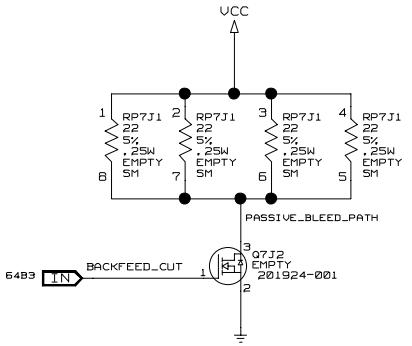
CR-90

DEBUG/EV FEATURE: SMI/STPCLK INJECTION HEADERS





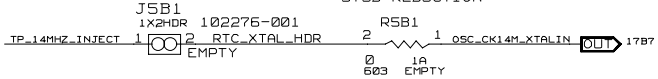
PASSIVE BLEED CIRCUIT



14 MHZ CLOCK INJECTION

CAD NOTE:
PLACE ALL PARTS
NEAR CLK GEN XTAL

STUB REDUCTION



DEBUG:

VID JUMPER RESISTORS

SMI/STPCLK INJECTION HDRS

PASSIVE BLEED CIRCUIT

DRAWING
CANTERWOOD_CRB.SCH_1.90
Thu Apr 03 14:02:53 2003

SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: 14MHZ CLOCK INJECTION		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 90/103

CR-91

DEBUG/EV FEATURE: TRACK SPLITTER

92C5 31D6 12C7 — BI — HI<0> — EMPTY — T55V10
92C5 31D6 12C7 — BI — HI<1> — EMPTY — T55V9
92C5 31D6 12C7 — BI — HI<2> — EMPTY — T55V17
92C5 31D6 12C7 — BI — HI<3> — EMPTY — T55V16
92C5 31D6 12C7 — BI — HI<4> — EMPTY — T55V35
92B5 31D6 12C7 — BI — HI<5> — EMPTY — T55V37
92B5 31D6 12C7 — BI — HI<6> — EMPTY — T55V36
92B5 31D6 12C7 — BI — HI<7> — EMPTY — T55V38
92C5 31D6 12C7 — BI — HI<8> — EMPTY — T55V14
92C5 31D6 12C7 — BI — HI<9> — EMPTY — T55V11
92C5 31D6 12C7 — BI — HI<10> — EMPTY — T55V15
38B8 30B7 9A3 64B3 80C5 75D5 79B5 62D7 — BI — PWRGD_3V — EMPTY — T55V7
92C5 31C6 12C7 — BI — HI_STBF — EMPTY — T55V13
92C5 31C6 12C7 — BI — HI_STBS — EMPTY — T55V12

16A7 — BI — HI_VREF
16B7 — BI — HI_VSWING — EMPTY — T55V28 (25B8 25A8 21B8 21A8)
EMPTY — T55V21 (25B3 25A8 21B3 21A8)

47D7 12B7 — BI — WI<0> — EMPTY — T55V27
47D7 12B7 — BI — WI<1> — EMPTY — T55V24
47D7 12B7 — BI — WI<2> — EMPTY — T55V29
47D7 12B7 — BI — WI<3> — EMPTY — T55V33
47D7 12B7 — BI — WI<4> — EMPTY — T55V34
47D7 12B7 — BI — WI<5> — EMPTY — T55V32
47D7 12B7 — BI — WI<6> — EMPTY — T55V28
47D7 12B7 — BI — WI<7> — EMPTY — T55V30
47D7 12B7 — BI — WI<8> — EMPTY — T55V25
47D7 12B7 — BI — WI<9> — EMPTY — T55V23
47D7 12B7 — BI — WI<10> — EMPTY — T55V31
47D7 12B7 — BI — WI_STBF — EMPTY — T55V26 (64B8 47B7 43D3 43B7)
47D7 12B7 — BI — WI_STBS — EMPTY — T55V22 (64B8 47C7 43D3 43B7 69D5)

85C1 83A8 85A3 — BI — CPU_PSC_HI
30C6 17B7 — BI — CK_100M_ICH — EMPTY — T55V40
30C6 17B7 — BI — CK_100M_ICH* — EMPTY — T55V18
94B7 17A8 — BI — CK_H_CPU1_ITP — EMPTY — T55V19
94B7 17B8 — BI — CK_H_CPU1_ITP* — EMPTY — TSXX5V18
31B3 17A2 — BI — CK_48M_ICH_USB — EMPTY — TSXX5V19
31C6 17B2 — BI — CK_HBL_66M_ICH — EMPTY — TSXX5V2
41C2 17D2 — BI — CK_P_33M_S4 — EMPTY — TSXX5V1
47D7 17B2 — BI — CK_66M_CSA — EMPTY — TSXX5V9
44C2 17B2 — BI — CK_P_33M_S1 — EMPTY — TSXX5V29 (44C7 43C7 42C7 41C7)
43C2 17C2 — BI — CK_P_33M_S2 — EMPTY — TSXX5V30 (44C7 43C7 42C7 41C7)
42C2 17C2 — BI — CK_P_33M_S3 — EMPTY — TSXX5V31 (44D7 43D7 42D7 41D7 47C3 46C2 47C6)
40C2 17C2 — BI — CK_P_33M_S5 — EMPTY — TSXX5V32 (48C5 48C6 83D8 83D4)
83C8 85D5 — BI — POWER_GOOD — EMPTY — TSXX5V33
EMPTY — TSXX5V34

30C3 7D5 6C5 — BI — H_THERMTRIP_ICH* — EMPTY — TSXX5V35
6B1 94C2 7C1 — BI — H_TRST* — EMPTY — TSXX5V17
7C4 6C1 94C2 — BI — H_TMS — EMPTY — TSXX5V27
6C1 94C2 7C1 — BI — H_TDI — EMPTY — TSXX5V39
94C2 6C1 — BI — H_TDO — EMPTY — TSXX5V40
6C1 94C7 94C2 94B7 7C4 — BI — H_TCK — EMPTY — TSXX5V41
64A3 64A1 — BI — GLUE_SLOTOCC* — EMPTY — TSXX5V10
94C2 71C8 69B6 30C1 — BI — FP_RST* — EMPTY — TSXX5V20
94C7 7C1 6D1 — BI — H_BPM<3>* — EMPTY — TSXX5V14
94C7 7C1 6D1 — BI — H_BPM<2>* — EMPTY — TSXX5V12
94C7 7C1 6D1 — BI — H_BPM<1>* — EMPTY — TSXX5V11
94C7 7C1 6D1 — BI — H_BPM<0>* — EMPTY — TSXX5V13
94C7 7D1 6D1 — BI — H_BPM4_PRDY* — EMPTY — TSXX5V15
94C7 7D1 6D1 — BI — H_BPM5_PREQ* — EMPTY — TSXX5V16
63C8 62C7 47C7 12A7 33B5 — BI — P_PCIRST* — EMPTY — TSXX5V38
64B8 46C2 17C5 25B8 25A8 21B8 21A8 — BI — SMB_DATA_MAIN — EMPTY — TSXX5V6
64B8 46C7 17C5 25B3 25A8 21B3 21A8 — BI — SMB_CLK_MAIN — EMPTY — TSXX5V32
6D5 30D6 — BI — H_A20M* — EMPTY — T55V3
6C1 30D6 — BI — H_SLP* — EMPTY — T55V39
30D6 7D5 6D5 — BI — H_FERR* — EMPTY — T55V1
6D5 30D6 — BI — H_IGNNE* — EMPTY — T55V2
62A6 6C6 30D6 — BI — H_INIT* — EMPTY — T55V6
6D5 30D6 — BI — H_INTR — EMPTY — T55V4
6D5 30D6 — BI — H_NMI — EMPTY — T55V5
6C1 30C3 7C5 — BI — H_PWRGD — EMPTY — T55V8

6D5 90D5 — BI — H_SMI_DIRECT* — EMPTY — TSXX5V36
90C5 30D6 — BI — ICH_H_STPCLK* — EMPTY — TSXX5V42
41B7 40B7 30C3 69D5 — BI — SMB_DATA_RESUME — EMPTY — TSXX5V37
41B7 40B7 30C3 64B8 47B7 43D3 43B7 — BI — SMB_CLK_RESUME — EMPTY — TSXX5V38

63B6 30B3 17D2 — BI — CK_14M_ICH_PA — EMPTY — TSXX5V21
52D8 17D2 — BI — CK_14M_AUD — EMPTY — TSXX5V26
42C2 40D7 18C5 29C6 45C7 — BI — P_INTA* — EMPTY — TSXX5V4
45B7 42C7 18C5 29C8 — BI — P_INTB* — EMPTY — TSXX5V7
40C7 29D6 16C5 44C7 43C7 42C7 41C7 — BI — P_PME* — EMPTY — TSXX5V3
40C7 64B1 18C5 44C7 43C7 42C7 41C7 — BI — P_RST_SLOTS* — EMPTY — TSXX5V5
40D7 18B5 78A2 — BI — V_3P3_PCIVAUX — EMPTY — TSXX5V8
62C7 17C2 — BI — CK_P_33M_ICH — EMPTY — TSXX5V23
29D6 17C2 — BI — CK_P_33M_FWHCLK — EMPTY — TSXX5V31
63C6 17D2 — BI — CK_P_33M_PA — EMPTY — TSXX5V24

DRAWING
CANTERWOOD_CRB.SCH_1.91
Thu Apr 03 14:02:53 2003

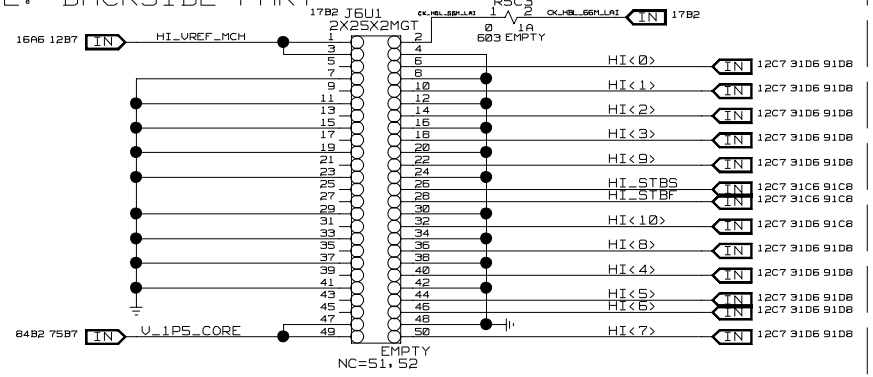
SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: TRACK SPLITTERS		REV: 1.2
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 91/103

CR-92

DEBUG FEATURE: HUBLINK LAI HEADER

NOTE: BACKSIDE PART 700000-450

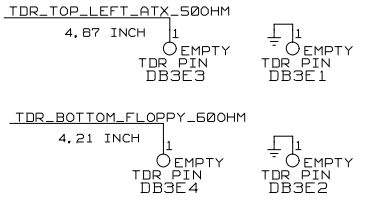
PLACE AT MIDPOINT OF HUBLINK ROUTING



SOLDER MASK PADS: 5, 9, 13, 17, 21, 25, 27, 31, 35, 39, 43, 45

PINS ARE NOT ASSIGNED TP SIGNAL NAMES (PREVENTS TRACE CONNECTION)

DEBUG FEATURE: TDR COUPONS



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CANTERWOOD_CRB.SCH_1,92
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SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: DEBUG: TDR COUPONS		REV: 1.2
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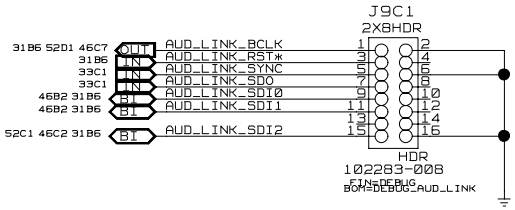

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SCHEMATIC TITLE: INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE:		REV: 1.2
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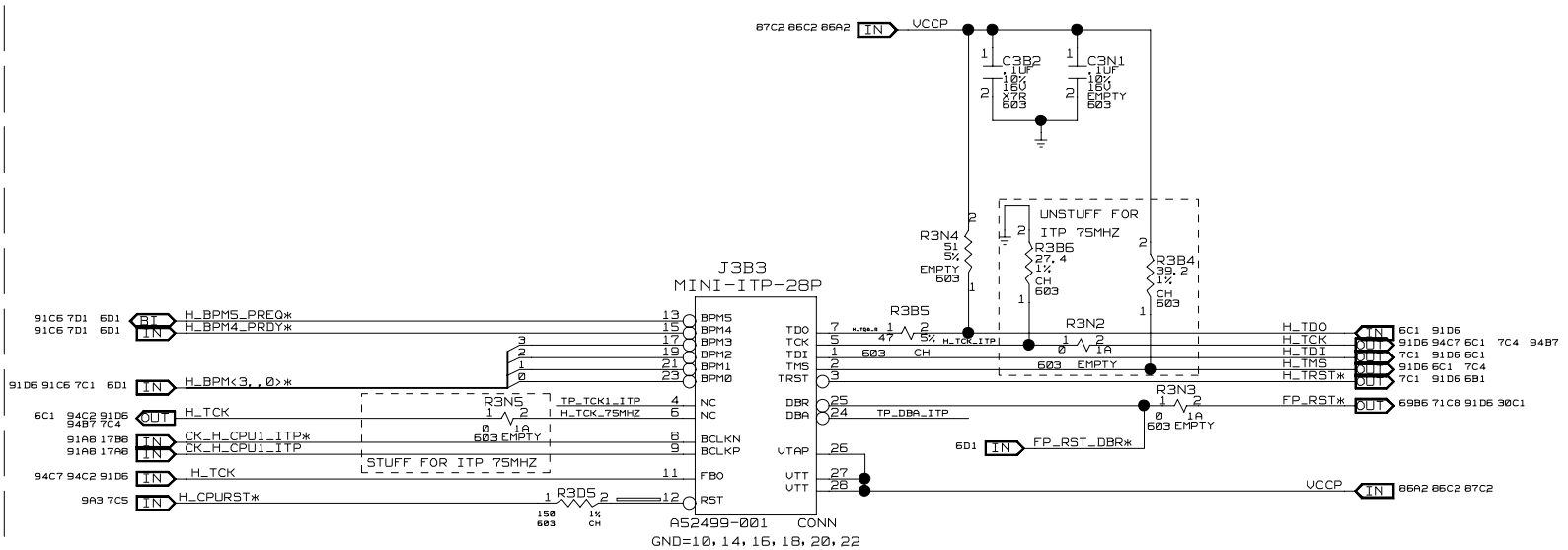
ITP/DPFLEX CONNECTOR



DESIGN NOTE:

INCLUDES STUFFING OPTIONS FOR 75MHZ ITP.

CAD NOTE:

ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN.
FB0 TAPS INTO THE H_TCK SIGNAL (CLOSE TO THE TCK PIN OF THE CONNECTOR).
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS.

XTG LAYOUT GUIDELINES:

T1 : MAXIMUM 1NS (ITP TO CPU PINS)

T2 : MAXIMUM 200PS (CPU PINS (TCK & TMS) TO PULL UP/DOWN)

T3 : MAXIMUM 200PS (ITP PINS (TCK & TMS) TO PULL UP/DOWN)

T4 : MAXIMUM 200PS (STUB LENGTH ON ITP PINS(TCK & TMS))

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PAGE TITLE: ITP/DPFLEX CONNECTOR		REV: 1.2
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*** Signal Cross-Reference ***
--- for the entire design --

```
1PS_CORE_3S8_OUT_1 84
1PS_CORE_3S8_OUT_7 84
1PS_CORE_3S8_PLUS_3 84
1PS_CORE_INTERMEDIATE_2P2V 84
2PS_PHASE_IND   76
2_5_BOTTOM_GATE_DRV 76
2_5_TOP_GATE_DRV 76
3IN1_GND        76
A20GATE         30 63
ACK64*          42 43 44
AGPREF_CON      18
AGPREF_MCH      12 18 20
AUD_BP_LINEOUT_SENSE 55 58
AUD_CDGND       52 54
AUD_CDGND_C     54
AUD_CDGND_R     54
AUD_CODEC_12    52
AUD_CODEC_16    52 58
AUD_CODEC_17    52 58
AUD_CODEC_27    52 53
AUD_CODEC_28    52 56
AUD_CODEC_29    52 53
AUD_CODEC_30    52 53
AUD_CODEC_31    52 53 57
AUD_CODEC_31_43_C 57
AUD_CODEC_32    52 53 57
AUD_CODEC_32_44_C 57
AUD_CODEC_33    52 53
AUD_CODEC_34    52
AUD_CODEC_40    52
AUD_CODEC_43    52 57 58
AUD_CODEC_44    52 57 58
AUD_CODEC_45    52 58
AUD_CODEC_46    52 58
AUD_CODEC_CENT  57
AUD_CODEC_LFE   57
AUD_CODEC_XTL_O 52
AUD_DVDD1       52
AUD_FP_L_RETIN  55 56 57 58
AUD_FP_R_RETIN  55 56 57
AUD_HP_LOUT     52 55
AUD_HP_LOUT_C   55 56
AUD_HP_ROUT     52 55
AUD_HP_ROUT_C   55 56
AUD_JACK_GND    54 55 56 59
AUD_LCD         52 54
AUD_LCD_C       54
AUD_LCD_R       54
AUD_LINE_LOUT   52 55
AUD_LINE_LOUT_C 55
AUD_LINE_ROUT   52 55
AUD_LINE_ROUT_C 55
AUD_LINK_BCLK   31 46 52 92
AUD_LINK_BCLK_R 52
AUD_LINK_RST*   31 46 52 64 92
AUD_LINK_SDI0   31 46 92
AUD_LINK_SDI1   31 46 92
AUD_LINK_SDI2   31 46 52 92
AUD_LINK_SDI2_R 52
AUD_LINK_SDO    33 46 52 92
AUD_LINK_SDO_R  31 33 62
AUD_LINK_SYNC   33 46 52 92
AUD_LINK_SYNC_R 31 33
AUD_LLINEIN     52 54
AUD_LLINEIN_C   54
AUD_LLINEIN_INT 54
AUD_LLINEIN_R   54
AUD_L_LINEOUT   55
AUD_MIC1_BP_C   56
AUD_MIC1_BP_FP  56
AUD_MIC1_BP_R   56
AUD_MIC1_FP_C   56
AUD_MIC1_FP_R   56
AUD_MIC1_IN     52 56
AUD_MIC2_BP_R   56
AUD_MIC2_FP_R   56
AUD_MIC2_IN     52 56
AUD_MICBIAS_BP  56
AUD_MICBIAS_BP_FP 56
AUD_MICBIAS_FP  56
AUD_MICBIAS_STND 56
AUD_MONO_OUT    52 57
AUD_MONO_OUT_RC 57
AUD_RCD         52 54
AUD_RCD_C       54
AUD_RCD_R       54
AUD_RLINEIN     52 54
AUD_RLINEIN_C   54
AUD_RLINEIN_INT 54
AUD_RLINEIN_R   54
AUD_R_LINEOUT   55
AUD_SPDIF_IN    52 57
AUD_SPDIF_OUT   52 57
AUD_SURR_L_C    57
AUD_SURR_R_C    57
A_GND           85
BACKFEED_CUT    64 78 90
BOARDID<2,,0>   30 33
BOOTSELECT      6 85
CDC_DWN_ENAB*   30 46 64
CDC_DWN_RST*    52 64
CDC_RESET*      52
CK_14M_AUD      17 52
CK_14M_AUD_R    17
CK_14M_ICH_PA   17 30 63
CK_14M_PA_ICH_R 17
CK_48M_DOTCLK   17
CK_48M_DOTCLK_R 17
CK_48M_ICH_USB  17 31
CK_48M_ICH_USB_R 17
CK_66M_CSA      17 47
CK_66M_CSA_LAI_R 17
CK_66M_CSA_R    17
CK_66M_MCH      12 17
CK_66M_MCH_R    17
CK_100M_ICH     17 30
CK_100M_ICH*    17 30
CK_100M_ICH_R   17
CK_100M_ICH_R*  17
CK_CPU_PCI_STOP 17
CK_G_66M_AGP    17 18
CK_G_66M_AGP_R  17
CK_HBL_66M_ICH  17 31
CK_HBL_66M_ICH_R 17
CK_HBL_66M_LAI  17 91
CK_H_CPU0_CPU   6 17
CK_H_CPU0_CPU*  6 17
CK_H_CPU0_CPU_R 17
CK_H_CPU0_CPU_R* 17
CK_H_CPU1_ITP   17 93
CK_H_CPU1_ITP*  17 93
CK_H_CPU1_ITP_CPU 17
CK_H_CPU1_ITP_CPU* 17
CK_H_CPU1_ITP_CPU_TP 6
CK_H_CPU1_ITP_CPU_TP* 6
CK_H_CPU1_ITP_PN1 17
CK_H_CPU1_ITP_PN1* 17
CK_H_CPU1_ITP_R 17
CK_H_CPU1_ITP_R* 17
CK_H_CPU2_MCH   9 17
CK_H_CPU2_MCH*  9 17
CK_H_CPU2_MCH_R 17
CK_H_CPU2_MCH_R* 17
CK_M_133M_N_DDR0_A 10 21
CK_M_133M_N_DDR0_B 11 25
CK_M_133M_N_DDR1_A 10 21
CK_M_133M_N_DDR1_B 11 25
CK_M_133M_N_DDR2_A 10 21
CK_M_133M_N_DDR2_B 11 25
CK_M_133M_N_DDR3_A 10 21
CK_M_133M_N_DDR3_B 11 25
CK_M_133M_N_DDR4_A 10 21
CK_M_133M_N_DDR4_B 11 25
CK_M_133M_N_DDR5_A 10 21
CK_M_133M_N_DDR5_B 11 25
CK_M_133M_P_DDR0_A 10 21
CK_M_133M_P_DDR0_B 11 25
CK_M_133M_P_DDR1_A 10 21
CK_M_133M_P_DDR1_B 11 25
CK_M_133M_P_DDR2_A 10 21
CK_M_133M_P_DDR2_B 11 25
CK_M_133M_P_DDR3_A 10 21
CK_M_133M_P_DDR3_B 11 25
CK_M_133M_P_DDR4_A 10 21
CK_M_133M_P_DDR4_B 11 25
CK_M_133M_P_DDR5_A 10 21
CK_M_133M_P_DDR5_B 11 25
CK_P_33M_FWHCLK 17 62
CK_P_33M_FWHCLK_R 17
CK_P_33M_ICH    17 29
CK_P_33M_ICH_R  17
CK_P_33M_PA     17 63
CK_P_33M_PA_R   17
CK_P_33M_PORT80 17
CK_P_33M_PORT80_R 17
CK_P_33M_S1     17 44
CK_P_33M_S1_R   17
CK_P_33M_S2     17 43
CK_P_33M_S2_R   17
CK_P_33M_S3     17 42
CK_P_33M_S3_R   17
CK_P_33M_S4     17 41
CK_P_33M_S4_R   17
CK_P_33M_S5     17 40
CK_P_33M_S5_R   17
CK_P_33M_TPM    17
CK_P_33M_TPM_R  17
CLK_IREF        17
CNR_SDI0_A29    46
CNR_SDI1_A28    46
CNR_SDI2_A27    46
CNR_SMB_A0      46
CNR_SMB_A1      46
CNR_SMB_A2      46
COMP            85
CORE_SPKR_R     70
CPU_DRIVER      73
CPU_FAN_CTRL    69 73
CPU_FAN_TACH    63 69 73
CPU_NWD_HI      85
CPU_PSC_HI      83 85
CPU_PSC_NWD     83
CPU_TACH_OUT    73
CPU_VREG_12     85
CSCOMP          85
CSCOMP_RC       85
CSCOMP_THERM    85
CSSUM           85
DIMM_VREF_1P25_A 21
DIMM_VREF_1P25_B 25
EDGE_TEST       12 15
FAN1_TACH       63
FAN2_TACH       63
FET_TO_FET_DECOUP 76
FNT_REAR_FAN_CTRL 69 73
FP_RST*         30 69 71 93
FP_RST_DBR*     6 93
FRONT_DRIVER    73
FRONT_FAN_PWM_R 73
FRONT_FAN_TACH  69 73
FRONT_TACH_OUT  73
FWH_H_INIT*     62
FWH_RST*        62
FWH_VPP         62
GC_DET*         18 20
GC_DET_REF      20
GLUE_SLOTOCC*   64
GND_SENSE       85
GPIO24          30
GPIO_DMA66_DETECT_PRI 35 62
GPIO_DMA66_DETECT_SEC 35 62
GPIO_LAN_DISABLE* 30
GPO18_BASE      33
GPO18_COL       33
GPO18_LED       33
GRCOMP          12 16
GSWING          12 20
G_AD<31,,0>     12 18
G_ADSTB0        12 18
G_ADSTB0*       12 18
G_ADSTB1        12 18
G_ADSTB1*       12 18
G_C_BE*<3,,0>   12 18
G_DBI_LO        12 18
G_DEVSEL*       12 18
G_FRAME*        12 18
G_GNT*          12 18
G_IRDY*         12 18
G_PAR           12 18
G_PERR_DET_XSTR 20
G_PERR_DET_XSTR_EMIT 20
G_PERR_PU*      18 20
G_PIPE*         12 18
G_RBF*          12 18
G_REQ*          12 18
G_SBA<7,,0>     12 18
G_SBSTB         12 18
G_SBSTB*        12 18
G_SERR*         18
G_ST<2,,0>      12 18
G_STOP*         12 18
G_TRDY*         12 18
G_WBF*          12 18
H4_H6_V_3P3STBY 69
H4_RSTN_H6_PWM1 69
H4_VCC3_H6_12V  69
H6_TAC4_PD      69
HD_LED*         64 71
HD_RCOMP        9 16
HD_SWING        9 16
HI11_PAR        31 33
HI<10,,0>       12 31 91
HI_RCOMP_ICH    31 33
HI_RCOMP_MCH    12 16
HI_STBF         12 31 91
HI_STBS         12 31 91
HI_VREF         16
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SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:

REV: 1.2

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HI_VREF_ICH	16 31
HI_VREF_MCH	12 16 91
HI_VSWING	16
HI_VSWING_ICH	16 31
HI_VSWING_MCH	12 16
HOLD#_PULLUP	49
H_A#<31,,3>	6 9
H_A20M#	6 30
H_ADS#	6 9
H_ADSTB0#	6 9
H_ADSTB1#	6 9
H_BNR#	6 9
H_BPM#<3,,0>	6 7 93
H_BPM4_PRDY#	6 7 93
H_BPM5_PREQ#	6 7 93
H_BPRI#	6 9
H_BR#<0,,0>	6 7 9
H_COMP0	6 7
H_COMP1	6 7
H_CPURST#	6 7 9 93
H_CPURST_ITP_R#	93
H_CPU_VCC_SENSE	6 7 85
H_CPU_VSS_SENSE	6 7 85
H_D#<63,,0>	6 9
H_DBI#<3,,0>	6 9
H_DBSY#	6 9
H_DEFER#	6 9
H_DRDY#	6 9
H_FERR#	6 7 30
H_FLUSH_FEEDBACK_R#	62
H_FSA_CLK	17
H_FSA_CPU	6 17
H_FSA_MCH	9 17
H_FSB_CLK	17
H_FSB_CPU	6 17
H_FSB_MCH	9 17
H_GTLREF	16
H_GTLREF_CPU	6 9 16
H_GTLREF_MCH	9 16
H_GTLREF_MCH_R	16
H_HIT#	6 9
H_HITM#	6 9
H_IGNNE#	6 30
H_INIT#	6 30 62
H_INIT_R#	62
H_INTR	6 30
H_LOCK#	6 9
H_NMI	6 30
H_PROCHOT#	6 7 9
H_PWRGD	6 7 30
H_REQ#<4,,0>	6 9
H_RS#<2,,0>	6 9
H_SKTOCC#	6 64
H_SLP#	6 30
H_SMI_2ICH#	30 90
H_SMI_DIRECT#	6 90
H_STBN#<3,,0>	6 9
H_STBP#<3,,0>	6 9
H_STPCLK#	6 90
H_TCK	6 7 93
H_TCK_75MHZ	93
H_TCK_ITP	93
H_TDI	6 7 93
H_TDO	6 93
H_TDO_R	93
H_TEMP_RET	6 69
H_TEMP_RET_HEC	69
H_TEMP_SRC	6 69
H_TEMP_SRC_HEC	69
H_TESTHI_0	6 7

H_TESTHI_1	6 7
H_TESTHI_2_7	6 7
H_TESTHI_8	6 7
H_TESTHI_9	6 7
H_TESTHI_10	6 7
H_TESTHI_11	6 7
H_TESTHI_12	6 7
H_THERMTRIP_ICH#	6 7 30
H_TMS	6 7 93
H_TRDY#	6 9
H_TRST#	6 7 93
H_VCCA	6 8
H_VCCIOPLL	6 8
H_VID<5,,0>	6 69 85
H_VSSA	6 8
ICH_EEPROM_ORG	49
ICH_EE_CLK_CNR	34 46
ICH_EE_CLK_R	31 34
ICH_EE_CS_CNR	34 46
ICH_EE_CS_R	31 34
ICH_EE_DIN_CNR	34 46
ICH_EE_DIN_R	31 34
ICH_EE_DOUT_CNR	34 46
ICH_EE_DOUT_R	31 34
ICH_GPIO6_PU	30 33
ICH_GPIO12_PU	30 33
ICH_GPO18#	30 33
ICH_H_STPCLK#	30 90
ICH_IDE_IRQ14	29 35
ICH_IDE_IRQ15	29 35
ICH_IDE_PDA<2,,0>	29 35
ICH_IDE_PDCS1#	29 35
ICH_IDE_PDCS3#	29 35
ICH_IDE_PDD<15,,0>	29 35
ICH_IDE_PDDACK#	29 35
ICH_IDE_PDDREQ	29 35
ICH_IDE_PDIOR#	29 35
ICH_IDE_PDIOW#	29 35
ICH_IDE_PIORDY	29 35
ICH_IDE_SDA<2,,0>	29 35
ICH_IDE_SDCS1#	29 35
ICH_IDE_SDCS3#	29 35
ICH_IDE_SDD<15,,0>	29 35
ICH_IDE_SDDACK#	29 35
ICH_IDE_SDDREQ	29 35
ICH_IDE_SDIOR#	29 35
ICH_IDE_SDIOW#	29 35
ICH_IDE_SIORDY	29 35
ICH_INTRUDER_HDR#	30 33
ICH_LAN_CLK_CNR	34 46
ICH_LAN_CLK_KIN	34 47
ICH_LAN_CLK_R	31 34
ICH_LAN_RST_CNR	34 46
ICH_LAN_RST_KIN	34 47
ICH_LAN_RST_R	31 34
ICH_LAN_RXD0_CNR	34 46
ICH_LAN_RXD0_KIN	34 47
ICH_LAN_RXD0_R	31 34
ICH_LAN_RXD1_CNR	34 46
ICH_LAN_RXD1_KIN	34 47
ICH_LAN_RXD1_R	31 34
ICH_LAN_RXD2_CNR	34 46
ICH_LAN_RXD2_KIN	34 47
ICH_LAN_RXD2_R	31 34
ICH_LAN_TXD0_CNR	34 46
ICH_LAN_TXD0_KIN	34 47
ICH_LAN_TXD0_R	31 34
ICH_LAN_TXD1_CNR	34 46
ICH_LAN_TXD1_KIN	34 47
ICH_LAN_TXD1_R	31 34

ICH_LAN_TXD2_CNR	34 46
ICH_LAN_TXD2_KIN	34 47
ICH_LAN_TXD2_R	31 34
ICH_P_PCIRST#	29 33
ICH_RI_PU	30 33
ICH_RSMRST#	30 47 64
ICH_RTCRST_PULLUP	30 33
ICH_RTCX1	30 33
ICH_RTCX2	30 33
ICH_SYS_RST#	30
ICH_THRM_PU#	30 33
ICH_USB_RBIAS	31
ICH_VRMPWRGD_PULLUP	30 33
IDE_PRI_ACT#	35 64
IDE_PRI_RST_R	35
IDE_RST#	35 64
IDE_SEC_ACT#	35 64
IDE_SEC_RST_R	35
INTVRMEN	30
IO_PME#	30 63
ISOL_TCK_KIN	30
ISOL_TEX_KIN	30
ISOL_TI_KIN	30 48
I_Q1F2_R1B2_R7J4	73
I_Q46R4_1	85
I_Q4602_1	85
I_R1F8_Q1F2	73
KBRST#	30 63
LAN_1P8_G	83
LAN_1P8_R	83
LAN_ACTLED#	47 50
LAN_ATEST+_RBIAS	10 47
LAN_AUX_PWR	47
LAN_CTRL_1P2	47 83
LAN_CTRL_1P8	47 83
LAN_DIFF_TAP_0	50
LAN_DIFF_TAP_1	50
LAN_DIFF_TAP_2	50
LAN_DIFF_TAP_3	50
LAN_DSBL#	30 47
LAN_EECS	34 49
LAN_EEDI	34 49
LAN_EEDO	34 49
LAN_EEMODE	47
LAN_EESK	34 49
LAN_LINK	49 50
LAN_LINK_100#	47 50
LAN_LINK_1000#	47 49 50
LAN_LINK_UP#	47 50
LAN_MDI_0	47 50
LAN_MDI_0#	47 50
LAN_MDI_1	47 50
LAN_MDI_1#	47 50
LAN_MDI_2	47 50
LAN_MDI_2#	47 50
LAN_MDI_3	47 50
LAN_MDI_3#	47 50
LAN_PME#	30 47
LAN_RST#	30 31
LAN_TC_EECS	47 49
LAN_TC_EEDI	47 49
LAN_TC_EEDO	47 49
LAN_TC_EESK	47 49
LAN_TEST	47
LAN_VCT	50
LAN_V_1P2	48 49 51 83
LAN_V_1P8	48 49 50 83
LAN_XTAL1	47 49
LAN_XTAL2	47 49
LAN_X_CAP	48

LATCHED_BACKFEED_CUT	64 76 78
LPCPD#	30 63
L_AD<3,,0>	30 62 63
L_DRQ#	30 63
L_FRAME#	30 62 63
M_B5_A<1,,0>	10 21 23
M_B5_B<1,,0>	11 25 27
M_CAS_A#	10 21 23
M_CAS_B#	11 25 27
M_DATA_A<63,,0>	10 21 22
M_DATA_B<63,,0>	11 25 26
M_DQS_A<8,,0>	10 21 23
M_DQS_B<8,,0>	11 25 27
M_ECC_A<7,,0>	10 21 22
M_ECC_B<7,,0>	11 25 26
M_MAA_A<12,,0>	10 21 22
M_MAA_B<12,,0>	11 25 26
M_RAS_A#	10 21 23
M_RAS_B#	11 25 27
M_SCKE_A<3,,0>	10 21 23
M_SCKE_B<3,,0>	11 25 27
M_SCS_A#<3,,0>	10 21 23
M_SCS_B#<3,,0>	11 25 27
M_WE_A#	10 21 23
M_WE_B#	11 25 27
NET_CLR_CMOS_JUMPER	33
NET_USB_FNT_P10	39
OPT_COMPAT	6
OSC_CK14M_XTALIN	17 90
OSC_CK14M_XTALOUT	17
PASSIVE_BLEED_PATH	90
PA_COM_CTS1#	63 68
PA_COM_DCD1#	63 68
PA_COM_DSR1#	63 68
PA_COM_DTR1#	63 68
PA_COM_RI1#	63 68
PA_COM_RTS1#	63 68
PA_COM_RXD1	63 68
PA_COM_TXD1	63 68
PA_FDD_DIR#	63 65
PA_FDD_DRVDEN0	63 65
PA_FDD_DRVDEN1	63 65
PA_FDD_DS0#	63 65
PA_FDD_DSKCHG#	63 65
PA_FDD_HDSEL#	63 65
PA_FDD_INDEX#	63 65
PA_FDD_MTR0#	63 65
PA_FDD_RDATA#	63 65
PA_FDD_STEP#	63 65
PA_FDD_TRK0#	63 65
PA_FDD_WDATA#	63 65
PA_FDD_WGATE#	63 65
PA_FDD_WRTPRT#	63 65
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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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*** Unit Cross-Reference ***
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C1H3	CAPN	24
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C1J1	CAPN	64
C1J2	CAPN	68
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C2C7	CAPN	88
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C2C10	CAPN	88
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C2C14	CAPN	88
C2C15	CAPN	88
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C2E11	CAPN	6
C2F1	CAPN	73
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C2G1	CAPN	24
C2G2	CAPN	24
C2G3	CAPN	24
C2G4	CAPN	24
C2H1	CAPN	24
C2H2	CAPN	24
C2H3	CAPN	24
C2H4	CAPN	24
C2H5	CAPN	24
C2H6	CAPN	24
C2H7	CAPN	24
C2H8	CAPN	24
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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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C9D2	CAP-P	82
C9E1	CAP-P	81
C9E2	CAPN	81
C9E3	CAPN	81
C9E4	CAPN	41
C9F1	capn	39

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1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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C9J6  CAPN      70
C301LB CAPN      48
C70VC2 CAPN      76
C70VCC CAPN      76
C73A1 CAPN      76
C113A CAPN      13
C301LC CAPN      48
C302LA CAPN      48
C445  CAPN      15
C447  CAPN      15
C7001J CAPN      76
C2101 CAPN      21
CP2A1 CPAK4C4C  68
CP2A2 CPAK4C4C  68
CP9J1 CPAK4C4C  71
CP9J2 CPAK4C4C  71
CR1B1 DIODE     86
CR3B1 DIODE     86
CR4B1 DIODE     87
CR6B1 LED       33
CR7J1 LED       75
CR9H1 DIOSOT23C 78
CRP1A1 TVS6_2V   66
DB2F1 TDR_PIN   91
DB2F2 TDR_PIN   91
DB2F3 TDR_PIN   91
DB3F1 TDR_PIN   91
EU7001J SC2614    76
FB4C1 FERRITE   8
FB4C2 FERRITE   8
FB5B1 FERRITE   17
FB6B1 FERRITE   17
HS901 BDG_WAVEHS 9
J1A1  PS2STACK  66
J1AC97 2X8HDR    92
J1B1  STD_MTG_HOLE 72
J1B2  1X3HDR    73
J1D1  MINI_ITP_28P 93
J1G1  STD_MTG_HOLE 72
J1J1  STD_MTG_HOLE 72
J2A1  DSUB9     68
J2A2  QUAD_USB  36
J2E1  PSC478    6
J2F1  1X3HDR    73
J3D1  ANCHOR_CLP_GHST 9
J3F1  ANCHOR_CLP_GHST 9
J3J1  2X10PWR   75
J4A2  DSUB25TALL 67
J4J1  2X17HDR3_5 65
J5A1  GBE_MAGJACK3_10 50
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J6G2  DIMM2P_184_1GB 21
J6H1  DIMM2P_184_1GB 25
J6H2  DIMM2P_184_1GB 25
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J6J2  2X20HDR20 35
J6U1  2X25X2MGT 91
J7A1  STD_MTG_HOLE 72
J7B1  CONPCI2_2 44
J7G1  STD_MTG_HOLE 72
J7J1  STD_MTG_HOLE 72
J7J2  1X3HDR    73
J7J3  1X2HDR    64
J8A2  1X4HDR    54
J8B1  2X5HDR8   56
J8B2  CONPCI2_2 43
J8H1  1X7HDR    61
J8H2  1X7HDR    61
J8J1  1X3HDR    62
J9B1  2X5HDR6   57
J9B2  CNR60_ICH4 46
J9B3  CONPCI2_2 42
J9F1  2X5HDR9   39
J9H1  1X3HDR    33
J9H2  1X2HDR    33
J9J3  2X8HDR10_14 71
J9J4  2X5HDR10  71
J9J5  MFG_MODE_JMPR 62
J9J6  1X3HDR2   71
J111  STD_MTG_HOLE 72
J112  STD_MTG_HOLE 72
J113  STD_MTG_HOLE 72
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J9850 CONPCI2_2 41
L1B1  INDUCTOR  86
L2A1  IND_4PIN  36
L2A2  IND_4PIN  36
L2A3  IND_4PIN  36
L2A4  IND_4PIN  36
L2B1  INDUCTOR  86
L4B1  INDUCTOR  87
L4B2  INDUCTOR  88
L4C1  INDUCTOR  8
L4C2  INDUCTOR  8
L5B1  IND_4PIN  39
L5B2  IND_4PIN  39
L5C3  INDUCTOR  15
L6C1  INDUCTOR  15
L7H1  INDUCTOR  76
L7H2  INDUCTOR  76
L9F1  IND_4PIN  39
L9F2  IND_4PIN  39
LB5F1 LABEL     72
LB6F1 LOGO      72
LSBJ1 SPKR      70
M1A1  FERRITE   79
M6A1  NFERRBD   56
M6A2  NFERRBD   55
M6A3  NFERRBD   56
M6A4  NFERRBD   55
M6A5  NFERRBD   54
M6A6  NFERRBD   54
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Q1F2  FET       73
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Q3B1  STD60NF3LL 86
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Q3B3  FET_VREG  86
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Q7E1  NTB18N06L 84
Q7E2  FET_VREG  84
Q7G1  FET_VREG  76
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Q8A1  BCP69T1   83
Q8C1  MBT3904DUAL 78
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Q8C3  MBT3904DUAL 78
Q8E1  NTB18N06L 84
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Q8J2  MBT3904DUAL 62
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Q9G1  MBT3904DUAL 38
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Q83A00UA NPN       30
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SCHEMATIC TITLE:
INTEL(R) 875P CHIPSET CUSTOMER REFERENCE BOARD

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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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U7E1  LM358     84
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INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: 01.07.2002	SHEET: 103/103