CR-1

INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

CONTENTS

PAGE #	COMPONENT / FUNCTION
1	TITLE / TABLE OF CONTENTS
2	VOLTAGE TABLE
3	DEVICE TABLE
4-9	SYSTEM, IRQ, RESET, CLOCK, AND VR
10-13	PROCESSOR P0/P1
14	PROCESSOR P0/P1 DECOUPLING
15	ITP
16-18	MCH
19	CKX_SKS CLOCK GENERATOR
20	MECC CONNECTOR
21	DRCG RAMBUS CLOCK GENERATORS
22	AGP CONNECTOR
23-24	ICH2
25-28	PCI33 SLOTS 0-2 AND TERMINATION
29	IDE
30	P64H
31-33	PCI64 SLOTS 0-1 AND TERMINATION
34	HECETA4
35	GLUECHIP3
36	FIRMWARE HUB
37	SUPER I/O
38-41	LEGACY I/O
42-43	USB AND WAKE ON USB
44-48	AUDIO 1881 AND SUPPORT CIRCUITRY, BATTERY
49	FRONT PANEL HEADER / SPEAKER
50	LAN / 82562EM
51	VREF CIRCUITS AGP, RSL, GTL+ AND HUB INTERFACE
52	POWER AND MICS. CONNECTORS
53	PROCESSOR VOLTAGE REGULATORS
54	VOLTAGE REGULATORS AGP, 1.8V, SB1.8V
55	FAN SPEED CONTROL AND CONNECTORS
56	IDROM, SMBUS CLOCK MUXING, VID CIRCUIT
57	FAN MUX, MOUNTING HOLES, PLD CIRCUIT, SB LED
58	SPARE COMPONENTS
59-67	COMPONENT AND SIGNAL CROSS REFERENCE

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: TITLE / TABLE OF CONTENTS		REV: 1.0
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DRAWING

CR-2

VOLTAGE TABLE

SYMBOL	NETNAME		PAGE
+12V :	+12V	:POWER SUPPLY OUTPUT	: P.52
+3.3V:	+3_3V	:POWER SUPPLY OUTPUT	: P.52
-12V :	-12V	:POWER SUPPLY OUTPUT	: P.52
N\A :	AGP_VDDQ	:VOLTAGE REGULATOR OUTPUT FROM +3.3V	: P.52
N\A :	GND	:SYSTEM DC GROUND	
N\A :	P12V_CPU	:POWER SUPPLY OUTPUT	: P.52
N\A :	COIL_P12V_CPU	:POWER SUPPLY OUTPUT	: P.53
+1.8V:	P1_8V	:VOLTAGE REGULATOR OUTPUT FROM +12V	: P.54
+5V :	P5V	:POWER SUPPLY OUTPUT	: P.52
N\A :	SB1_8V	:VOLTAGE REGULATOR OUTPUT FROM SB5V	: P.54
SB5V :	SB5V	:POWER SUPPLY OUTPUT	: P.52
N\A :	SB2.5V	:VOLTAGE REGULATOR OUTPUT FROM SB5V ON MEC	: P.20
SB3V :	STANDBY3V	:POWER SUPPLY OUTPUT	: P.52
N\A :	VCC_CORE	:VR OUTPUT FROM P12V_CPU	: P.53
N\A :	VCC3_CLK	:CK00 FILTERED POWER FROM +3.3V	: P19
N\A :	DRCGA_3_3V	:DRCGA FILTERED POWER FROM +3.3V	: P21
N\A :	DRCGB_3_3V	:DRCGB FILTERED POWER FROM +3.3V	: P21
N\A :	AGND	:FILTERED GND FOR SERIAL,PARALLEL,USB,KEYBRD,MOUSE	: P38
N\A :	AUD_GND	:FILTERED GND ISLAND FOR AUDIO	: P48
N\A :	AUD_VCC	:+5V VOLTAGE REGULATOR OUTPUT FROM +12V	: P47
N\A :	CHGND	:CHASSIS GND	: P50

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VOLTAGE TABLE

SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: VOLTAGE TABLE

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Thu May 17 14:04:38 2001

SHEET: 2

DEVICE TABLE

DEVICE	POWER	PINS
MCH U6D1 PAGES 16-18	+1.8V	A6 A9 AA12 AA13 AA14 AA15 AA18 AA19 AA20 AA21 AA27 AB8 AB9 AB10 AB11 AB16 AB17 AB22 AB23 AB24 AB25 AB30 AC8 AC9 AC10 AC11 AC16 AC17 AC22 AC23 AC24 AC25 AD8 AD9 AD10 AD11 AD16 AD17 AD22 AD23 AD24 AD25 AE8 AE9 AE10 AE11 AE16 AE17 AE22 AE23 AE24 AE25 AF22 B29 B31 C5 C8 C15 C19 C22 D11 D26 D27 E7 E10 E31 F15 F20 F21 F25 G7 G8 G9 G11 G29 G32 H5 H8 H9 H10 H11 H16 H17 H22 H23 H24 H25 H26 J8 J9 J10 J11 J16 J17 J22 J23 J24 J25 J27 J30 K5 K7 K8 K9 K10 K11 K16 K17 K22 K23 K24 K25 L8 L9 L10 L11 L16 L17 L22 L23 L24 L25 L27 L29 M12 M13 M14 M15 M18 M19 M20 M21 N12 N13 N14 N15 N18 N19 N20 N21 P12 P13 P14 P15 P18 P19 P20 P21 R12 R13 R14 R15 R18 R19 R20 R21 R27 R30 T8 T9 T10 T11 T16 T17 T22 T23 T24 T25 U8 U9 U10 U11 U16 U17 U22 U23 U24 U25 V12 V13 V14 V15 V18 V19 V20 V21 W12 W13 W14 W15 W18 W19 W20 W21 W30 Y12 Y13 Y14 Y15 Y18 Y19 Y20 Y21 Y27
	VCC_CORE	AB2 AB5 AB7 AD1 AD4 AD7 AF3 AF6 AF9 AF11 AG5 AG10 AG12 AG14 AH2 AH5 AJ9 AJ11 AK1 AK4 AK7 AL14 AM3 AM6 AM9 B3 D2 F1 F4 H3 K2 M1 M4 M7 P3 P6 T2 T5 T7 V1 V4 V7 Y3 Y6 Y7
	AGP_VDDQ	AG30 AJ32 AK27 AL19 AL25 AM23 AM29
	GND	A12 A13 A14 A16 A18 A19 A22 A23 A25 AA1 AA4 AA7 AA8 AA9 AA10 AA11 AA16 AA17 AA22 AA23 AA24 AA25 AA26 AA28 AA30 AB12 AB13 AB14 AB15 AB18 AB19 AB20 AB21 AB26 AB27 AB29 AB31 AB32 AC3 AC6 AC7 AC12 AC13 AC14 AC15 AC18 AC19 AC20 AC21 AC26 AC28 AC30 AC32 AD12 AD13 AD14 AD15 AD18 AD19 AD20 AD21 AD26 AD27 AD29 AD31 AD32 AE2 AE5 AE7 AE12 AE13 AE14 AE15 AE18 AE19 AE20 AE21 AE26 AE28 AE30 AE32 AF10 AF14 AF15 AF16 AF23 AF29 AF31 AG1 AG4 AG8 AG15 AG16 AG24 AH8 AH14 AH22 AH28 AH31 AJ3 AJ6 AJ13 AJ20 AJ26 AK10 AK18 AK24 AK30 AL5 AL8 AL12 AL22 AL28 AM20 AM26 B4 B7 B11 B13 B15 B17 B19 B22 B24 B26 C1 C3 C12 C14 C16 C18 C20 C21 C23 C25 C28 C30 D6 D9 D13 D15 D17 D19 D22 D24 D32 E3 E11 E12 E14 E15 E16 E18 E20 E21 E23 E25 E28 F11 F13 F17 F19 F22 F24 F30 G2 G5 G10 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 G25 G26 H7 H12 H13 H14 H15 H18 H19 H20 H21 H28 H31 J1 J4 J7 J12 J13 J14 J15 J18 J19 J20 J21 J26 K12 K13 K14 K15 K18 K19 K20 K21 K29 L3 L6 L7 L12 L13 L14 L15 L18 L19 L20 L21 L26 L28 L31 M8 M9 M10 M11 M16 M17 M22 M23 M24 M25 M26 M28 M30 M32 N2 N5 N8 N9 N10 N11 N16 N17 N22 N23 N24 N25 N26 N27 N29 N31 N32 P8 P9 P10 P11 P16 P17 P22 P23 P24 P25 P26 P28 P30 P32 R1 R4 R7 R8 R9 R10 R11 R16 R17 R22 R23 R24 R25 R26 R28 R29 P31 T12 T13 T14 T15 T18 T19 T20 T21 T26 T28 T30 T32 U3 U6 U7 U12 U13 U14 U15 U18 U19 U20 U21 U26 U27 U29 U31 V8 V9 V10 V11 V16 V17 V22 V23 V24 V25 V26 V28 V30 V32 W2 W5 W7 W8 W9 W10 W11 W16 W17 W22 W23 W24 W25 W26 W27 W29 W31 W32 Y8 Y9 Y10 Y11 Y16 Y17 Y22 Y23 Y24 Y25 Y26 Y28 Y30
PROCESSORS U7H1 U8E1 PAGES 10-13	+3.3V	AE28, AE29
	GND	A11, A21, A27, A29, A5, AA15, AA17, AA2, AA23, AA30, AB1, AB31, AC30, AD31AA9, AB11, AB21, AB27, AB5, AC13, AC19, AC2, AC25, AC7, AD15, AD17, AD23 AD3, AD9, AE11, AE2, AE21, AE27, B15, B17, B2, B23, B28, B9, B30, C1, C31, C13, C19, C25, C29, C7, D11, D30, D2, D21, D27, D28, D5, E1, E15, E17 E23, E29, E9, F13, F19, F2, F25, F28, F7, G1, G31, G25, G27, G29, G3, G5, G7, G9, H2, H24, H26, H28, H4, H6, H8, H30, J1, J31J23, J25, J27, J29 J3, J5, J7, J9, K2, K24, K26, K28, K4, K6, K8, K30, L1, L31, L23, L25, L27, L29, L3, L5, L7, L9, M2, M24, M26, M28, M4, M6, M8, M30, N30, N2, N24, N26 N28, N4, N6, N8, P23, P25, P27, P29, P3, P5, P7, P9, P1, P31, R30, R2, R24, R26, R28, R4, R6, R8, T23, T25, T27, T29, T3, T5, T7, T9, U2, U24 U26, U28, U4, U6, U8, V23, V25, V27, V29, V3, V5, V7, V9, V1, V31, W30, W2, W24, W26, W28, W4, Y13, Y19, Y25, Y5, Y7
	VCC_CORE	A30, AD30, AC31, AB30, AA31, AA1, A14, A18, A2, A24, A28, A8, AA12, AA20, AA26, AAV4, AA6, AB14, AB18, AB2, AB24, AB8, AC10, AC16, AC22, AC3, AC4, AD12, AD2 AD20, AD26, AD6, AE14, AE18, AE24, AE3, AE8, B4, B31, C30, D1, D31B12, B20, B26, B29, B6, C10, C16, C2, C22, C28, C4, D14, D18, D24, D29, D8, E12 E30, F1, F31, G30, H1, H31, E2, E20, E26, E28, E6, E31, F30, F10, F16, F22, F29, F4, G2, G24, G26, G28, G4, G6, G8, H23, H25, H27, H29, H3, H5, H7, H9, J2, J24, J26 J30, K1, K31, L30, M1, M31, J28, J4, J6, J8, K23, K25, K27, K29, K3, K5, K7, K9, L2, L24, L26, L28, L4, L6, L8, M23, M25, M27, M29, M3, M5, M7, M9, N23, N25 N1, N31, P30, R1, R31, T30, N27, N29, N3, N5, N7, N9, P2, P24, P26, P28, P4, P6, P8, R23, R25, R27, R29, R3, R5, R7, R9, T2, T24, T26, T28, T4, T6, T8, T1, T31, U30, U23 U1, U31, V30, W1, W31, Y30, U25, U27, U29, U3, U5, U7, U9, V2, V24, V26, V28, V4, V6, V8, W25, W27, W29, Y1, Y31, Y10, Y16, Y2, Y22
ICH2 U6B3 PAGES 23-24	+3.3V(vcc3_CLK)	E14, E15, E16, E17, E18, F18, G18, H18, J18, P18, R18, R5, T5, U5, V5, V6, V7, V8
	GND	A1, A10, A2, A21, A22, AA1, AA2, AA21, AA22, AB1, AB2, AB21, AB22, B1, B10, B2, B21, B22, B3, B9, C2, C3, C4 C9, D3, D5, D6, D7, D8, D9, E6, E7, E8, E9, J10, J11, J12, J13, J14, J9, K1, K10, K11, K12, K13, K14, K9, L10, L11 L12, L13, L14, L9, M10, M11, M12, M13, M14, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9
	+1.8V	D10, D2, E5, K19, L19, P5, V9
	SB1_8V	H5, J5, V14, V15, V16
	SB5V	V19
	VCC_CORE	D12, D13
P64H U3D1 PAGE 30	+3.3V	E11, E13, E5, E7, E9, F14, F4, H17, J13, J5, L13, M13, M5, N12, N6, P7
	+1.8V	N11, N7, N9, P10, P8
	GND	A1, A17, B12, B6, B9, C3, D16, E12, E14, F13, F16, F2, F5, G13, H10, H8, H9, J10, J8, J9, K10, K2, K8, K9, L5 M16, N13, P12, P2, P6, P9, R15, R16, T10, T13, T7, U1, U17
CKX_SKS U4F2 PAGE 19	+3.3V	4, 10, 16, 22, 27, 29, 36, 38, 43, 49, 56
	GND	1, 7, 13, 19, 24, 32, 33, 37, 40, 46, 53
DRCG'S U4E2 U4F1 PAGE 21	+3.3V	3, 9, 16, 22
	+1.8V	10
	+3.3V(vcc3_CLK)	1
	GND	4, 5, 8, 13, 17, 21
HECETA4 U7B2 PAGE 34	+3.3V	4, 13
	+5V	12
	SB2.5V	14
	VCC_CORE	15
	GND	3
74HCT4051 U3J2 PAGE 55	+5V	16
	GND	7
HCT4052 U4E2 PAGE 56	+5V	16
	GND	8
74F08 U9C1 PAGE 41-43	+5V	14
	GND	7
SIO LPC47B27X U7C1 PAGE 37	+3.3V	53, 65, 93
	+5V	44
	STANDBY3V	18
	GND	7, 31, 40, 60, 76
AD1881 U2A1 PAGE 44	+3.3V	1, 9
	AUD_VCC	25, 38
	GND	4, 7, 26, 42
GLUECHIP3 U1E1 PAGE 35	SB5V	2
	STANDBY3V	3
	GND	42 17
74HC682 U5H1 PAGE 56	+3.3V	20
	GND	10
82562EM U6B1 PAGE 50	STANDBY3V	1, 7, 25, 2, 9, 12, 14, 17, 19, 23, 36, 40
	GND	3, 6, 8, 13, 18, 20, 22, 24, 33, 38, 48
FWH U1F1 PAGE 36	+3.3V	25, 27, 32
	GND	16, 26, 28
QS3126 U1C1 PAGE49	+5V	16
	GND	8
74F07 U3J1 PAGE 49	SB5V	14
	GND	7
HIP6601 U2F1 PAGE 54	+12V	7
	GND	4
HIP6301 U2E1 PAGE 54	+5V	20
	GND	9
AT24C08 U6F1 PAGE 56	+3.3V	8
	GND	4
74LVC00 U5G1 PAGE 56	+3.3V	14
	GND	7
74LVC08 U5A1 PAGE 34	+3.3V	7
	GND	14

DEVICE TABLE

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SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE: DEVICE TABLE

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INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
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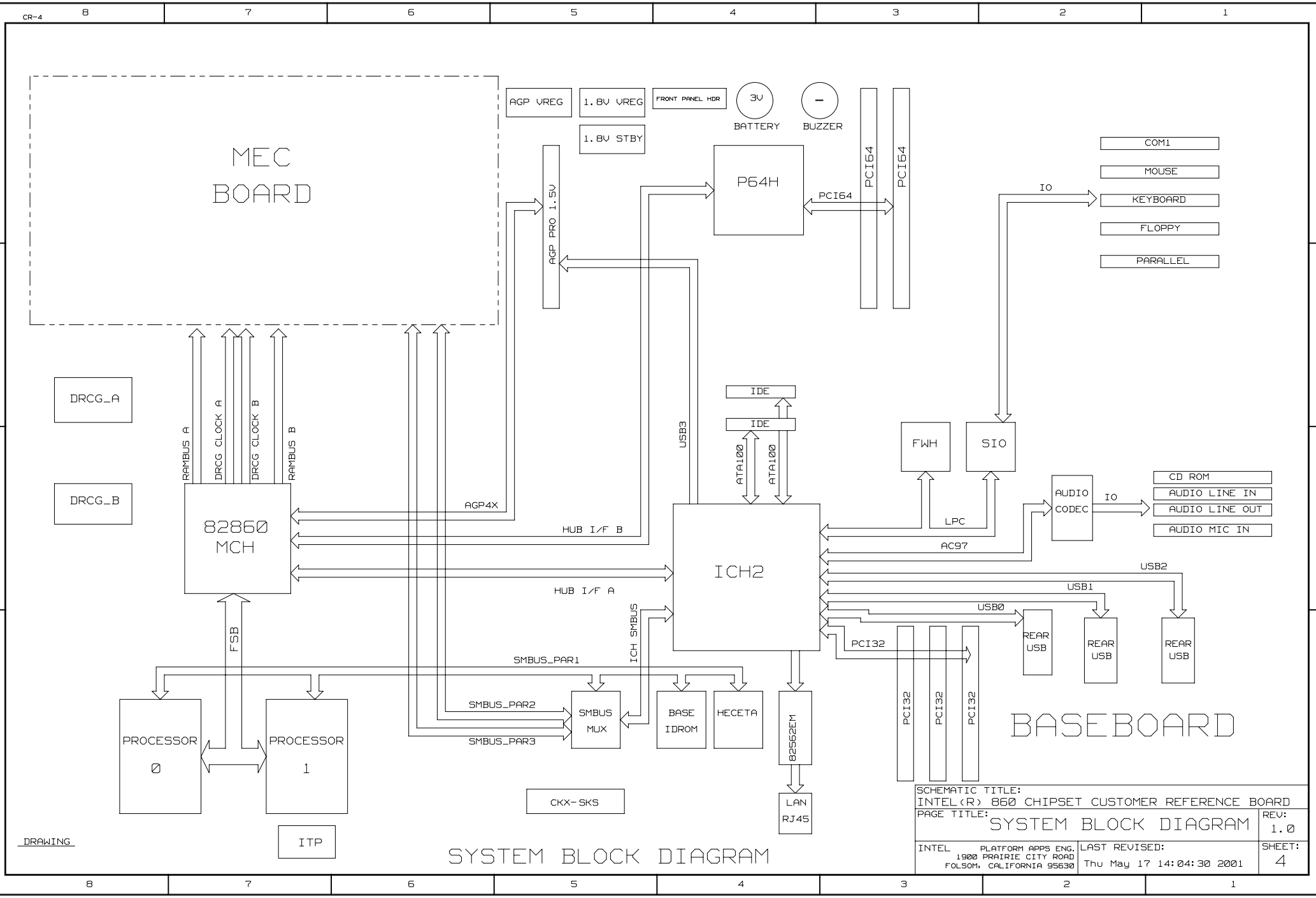
SHEET: 3


CR-4
MEC BOARD
AGP VREG
1.8V VREG
1.8V STBY
FRONT PANEL HDR
3V
BATTERY
BUZZER
P64H
PCI64
PCI64
PCI64
AGP PRO 1.5V
COM1
MOUSE
KEYBOARD
FLOPPY
PARALLEL
IO
DRCG_A
DRCG_B
RAMBUS A
DRCG CLOCK A
DRCG CLOCK B
RAMBUS B
82860 MCH
AGP4X
HUB I/F B
HUB I/F A
USB3
IDE
IDE
ATA100
ATA100
FWH
SIO
LPC
AUDIO CODEC
IO
CD ROM
AUDIO LINE IN
AUDIO LINE OUT
AUDIO MIC IN
AC97
ICH2
USB2
USB1
USB0
REAR USB
REAR USB
REAR USB
PCI32
PCI32
PCI32
PCI32
FSB
ICH SMBUS
SMBUS_PAR1
SMBUS_PAR2
SMBUS_PAR3
SMBUS MUX
BASE IDROM
HECETA
82562EM
LAN RJ45
PROCESSOR 0
PROCESSOR 1
ITP
CKX-SKS
BASEBOARD
DRAWING
SYSTEM BLOCK DIAGRAM
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
SYSTEM BLOCK DIAGRAM
REV:
1.0
INTEL PLATFORM APPS ENG.
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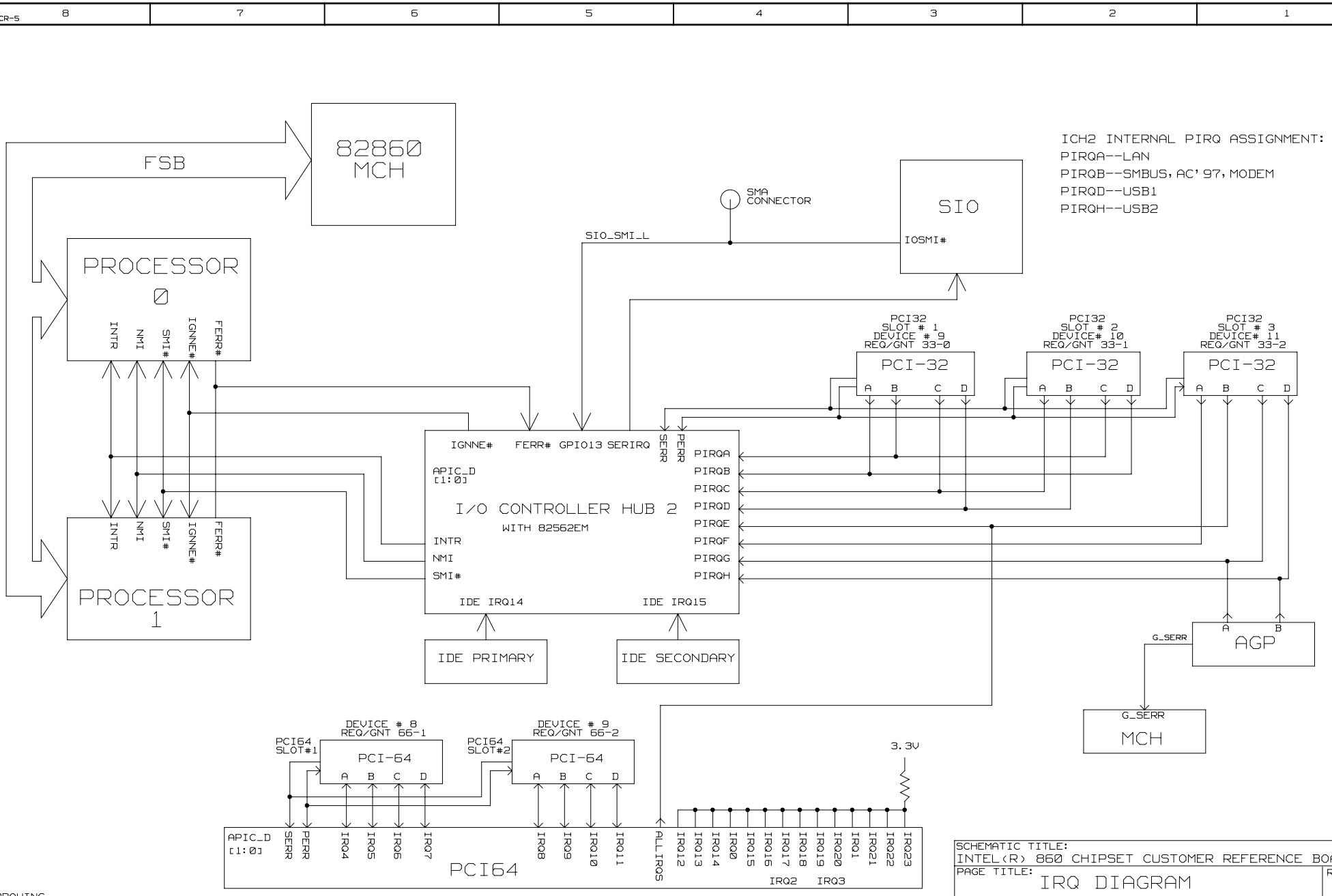
LAST REVISED:
Thu May 17 14:04:30 2001
SHEET:
4



IRQ DIAGRAM

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SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: IRQ DIAGRAM	REV: 1.0
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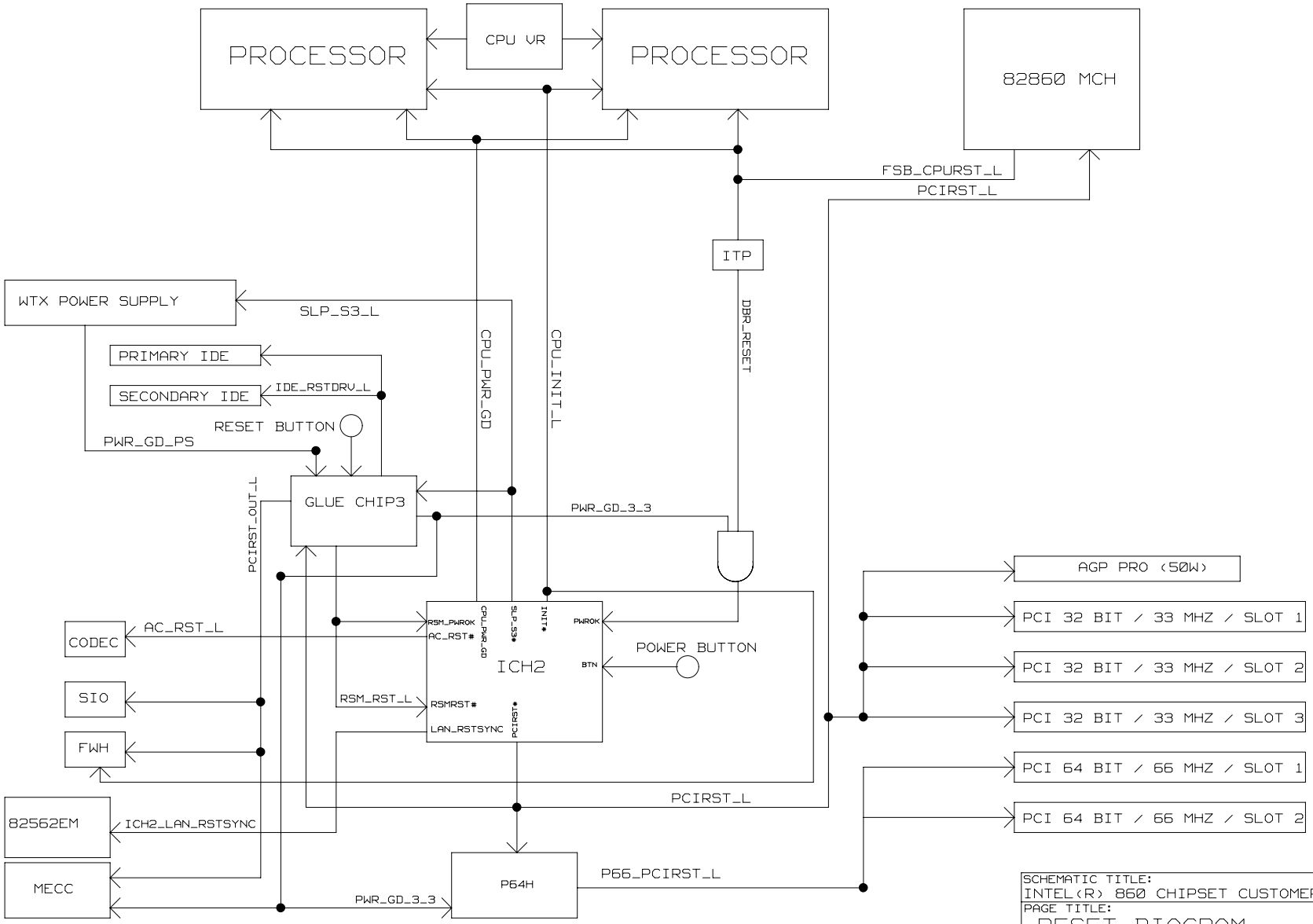
	SHEET: 5

CR-6



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RESET DIAGRAM

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: RESET DIAGRAM	REV: 1.0
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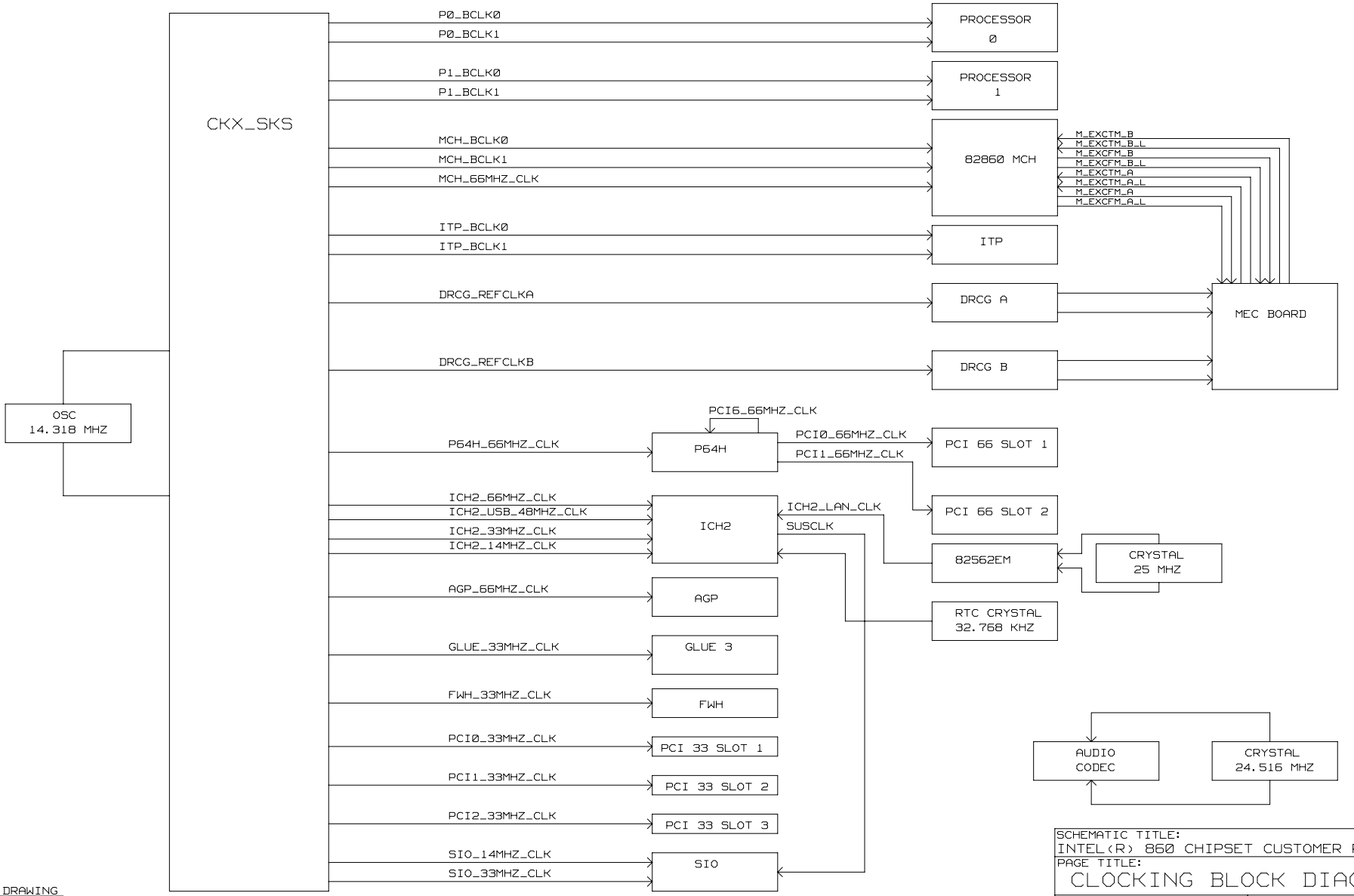
	SHEET: 6



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CLOCKING BLOCK DIAGRAM

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: CLOCKING BLOCK DIAGRAM	REV: 1.0
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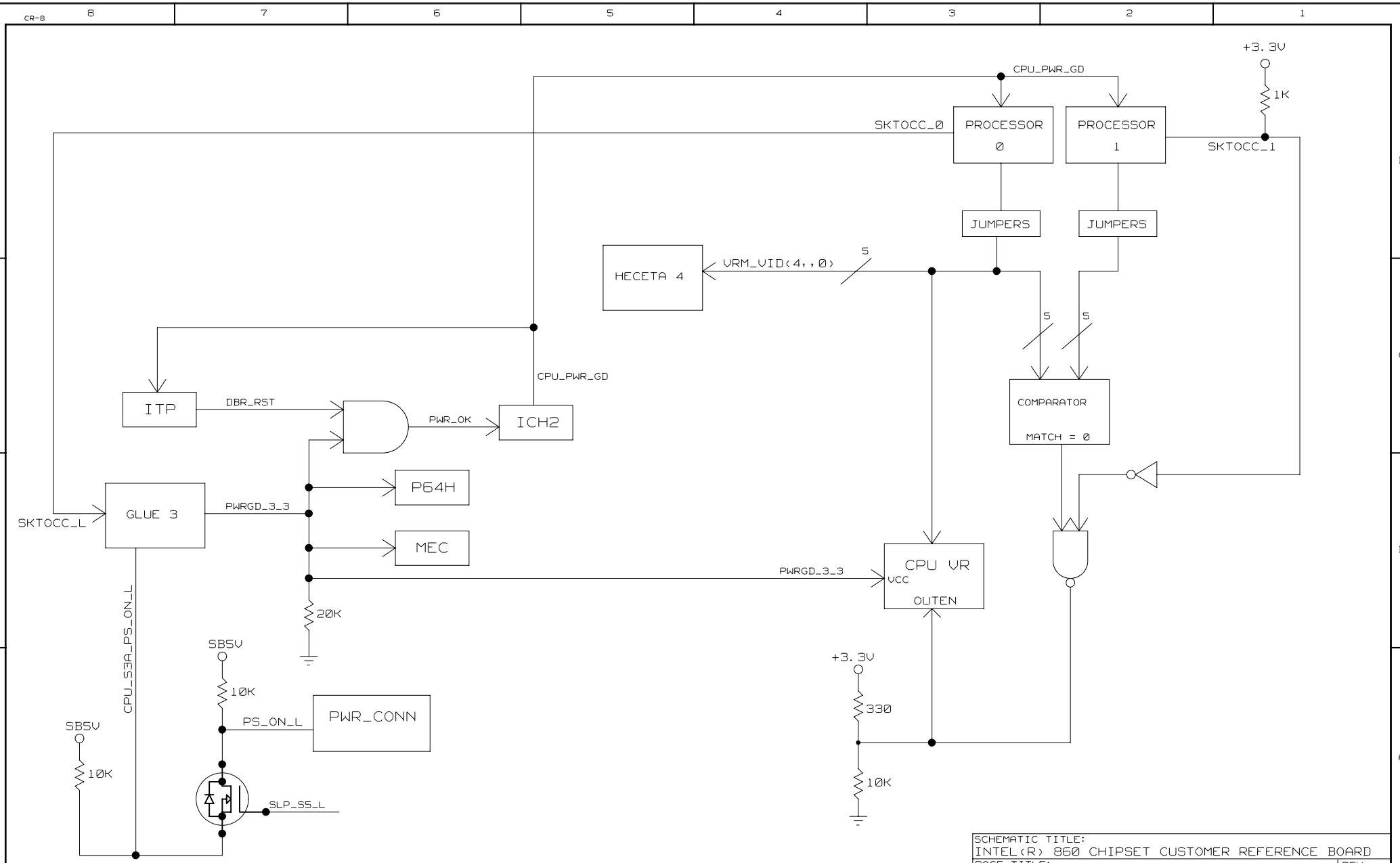
	SHEET: 7



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POWER GOOD AND CPU VR BLOCK DIAGRAM

SCHEMATIC TITLE:	INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	PWR GD AND CPU VR BLOCK DIAGRAM
REV:	1.0
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LAST REVISED:	Thu May 17 14:04:13 2001
SHEET:	8

CR-9

SMBUS PARTITION1

PARTITION SELECT = 10, 11

CPU0

THERMAL SENSOR: 30
IDROM SMB_ADDR: A0

CPU1

THERMAL SENSOR: 32
IDROM SMB_ADDR: A2

HECETA 4

SMB_ADDR: 5A

BASEBOARD IDROM

SMB_ADDR: A8-AE

ICH2

WITH 82562EM

ICH2 LAN
SMB_ADDR: C8

ICH_SMBUS

SMBUS_CTRL_0

SMBUS_CTRL_1

MUX

SMBUS_PAR1

SMBUS_PAR2

SMBUS PARTITION2

PARTITION SELECT = 00

RIMM* 1

SMB_ADDR: A0

RIMM* 2

SMB_ADDR: A2

RIMM* 3

SMB_ADDR: A4

RIMM* 4

SMB_ADDR: A6

RIMM* 5

SMB_ADDR: A8

RIMM* 6

SMB_ADDR: AA

RIMM* 7

SMB_ADDR: AC

RIMM* 8

SMB_ADDR: AE

S0	S1	SMBUS PARTITION
0	0	PAR2
0	1	PAR3
1	X	PAR1

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SMBUS ADDRESS PARTITION

SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

PAGE TITLE:
SMBUS ADDRESS PARTITION

REV: 1.0

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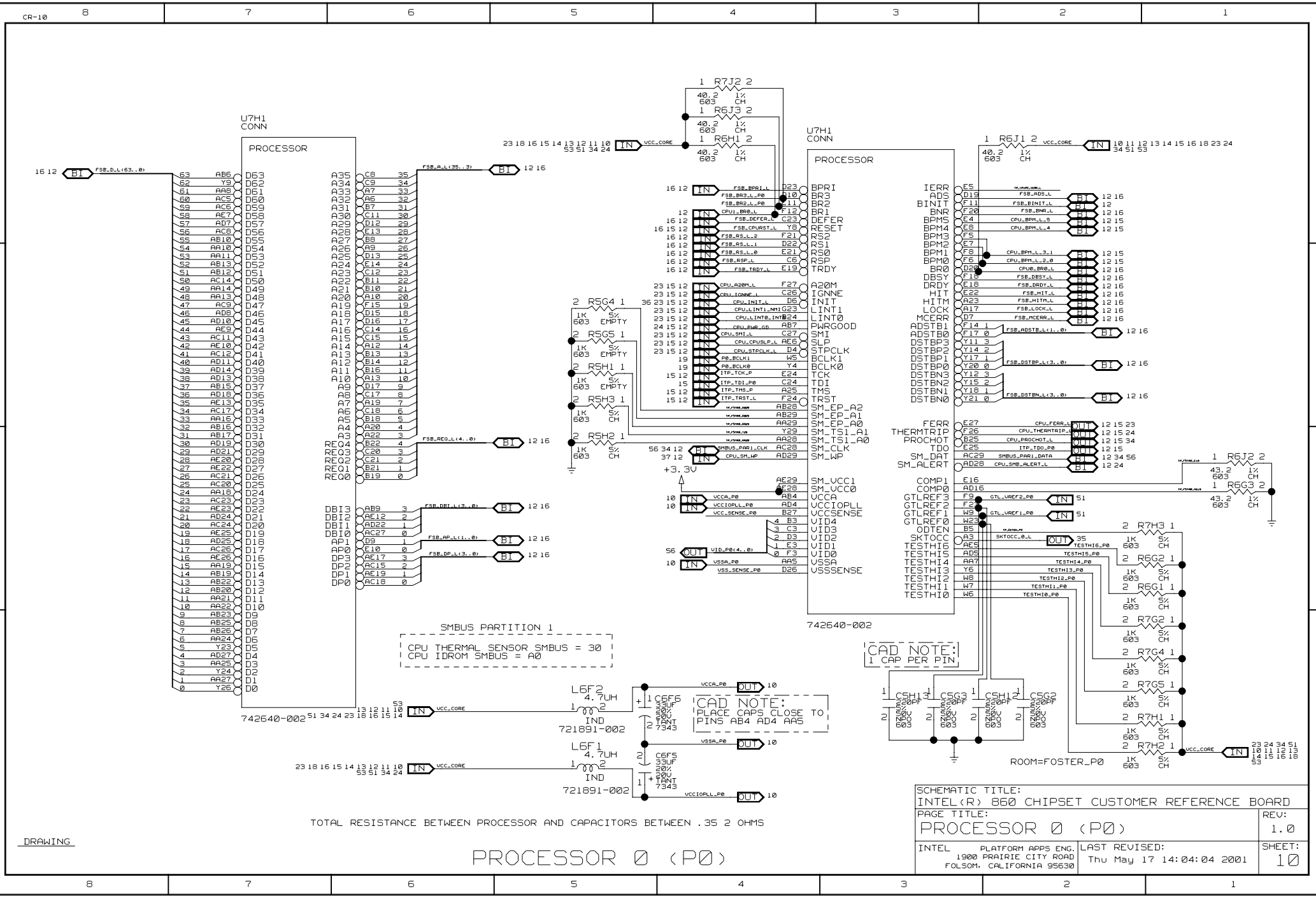
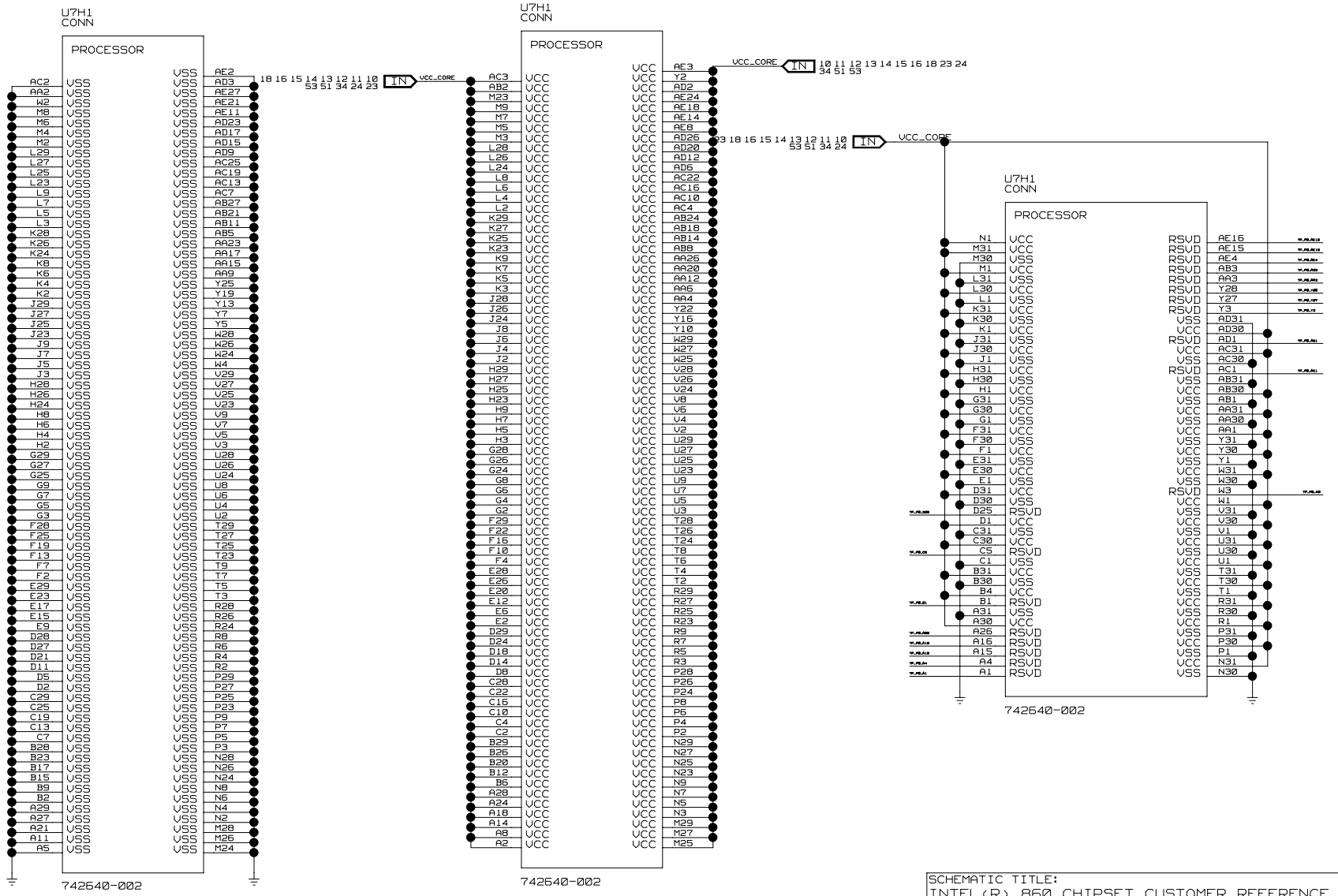
LAST REVISED:
Fri May 18 13:54:44 2001

SHEET: 9


U7H1
CONN
PROCESSOR
742640-002
SMBUS PARTITION 1
CPU THERMAL SENSOR SMBUS = 30
CPU IDROM SMBUS = A0
CAD NOTE:
PLACE CAPS CLOSE TO
PINS AB4 AD4 AA5
CAD NOTE:
1 CAP PER PIN
ROOM=FOSTER_P0
TOTAL RESISTANCE BETWEEN PROCESSOR AND CAPACITORS BETWEEN .35 2 OHMS
DRAWING
PROCESSOR 0 (P0)
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
PROCESSOR 0 (P0)
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:04:04 2001
SHEET:
10



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PROCESSOR 0 / POWER GROUND & RESERVED

SCHEMATIC TITLE:	INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	PROCESSOR 0
REV:	1.0
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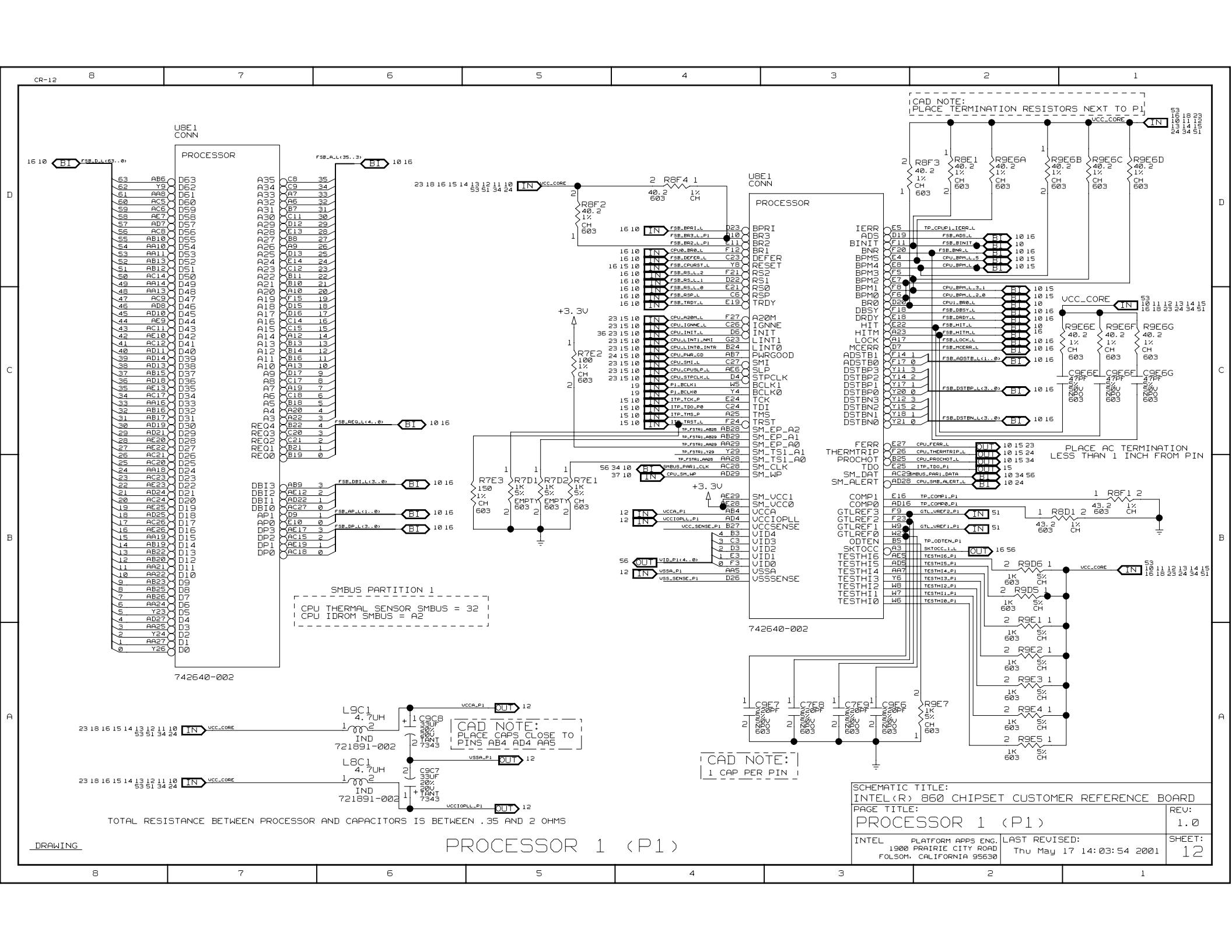
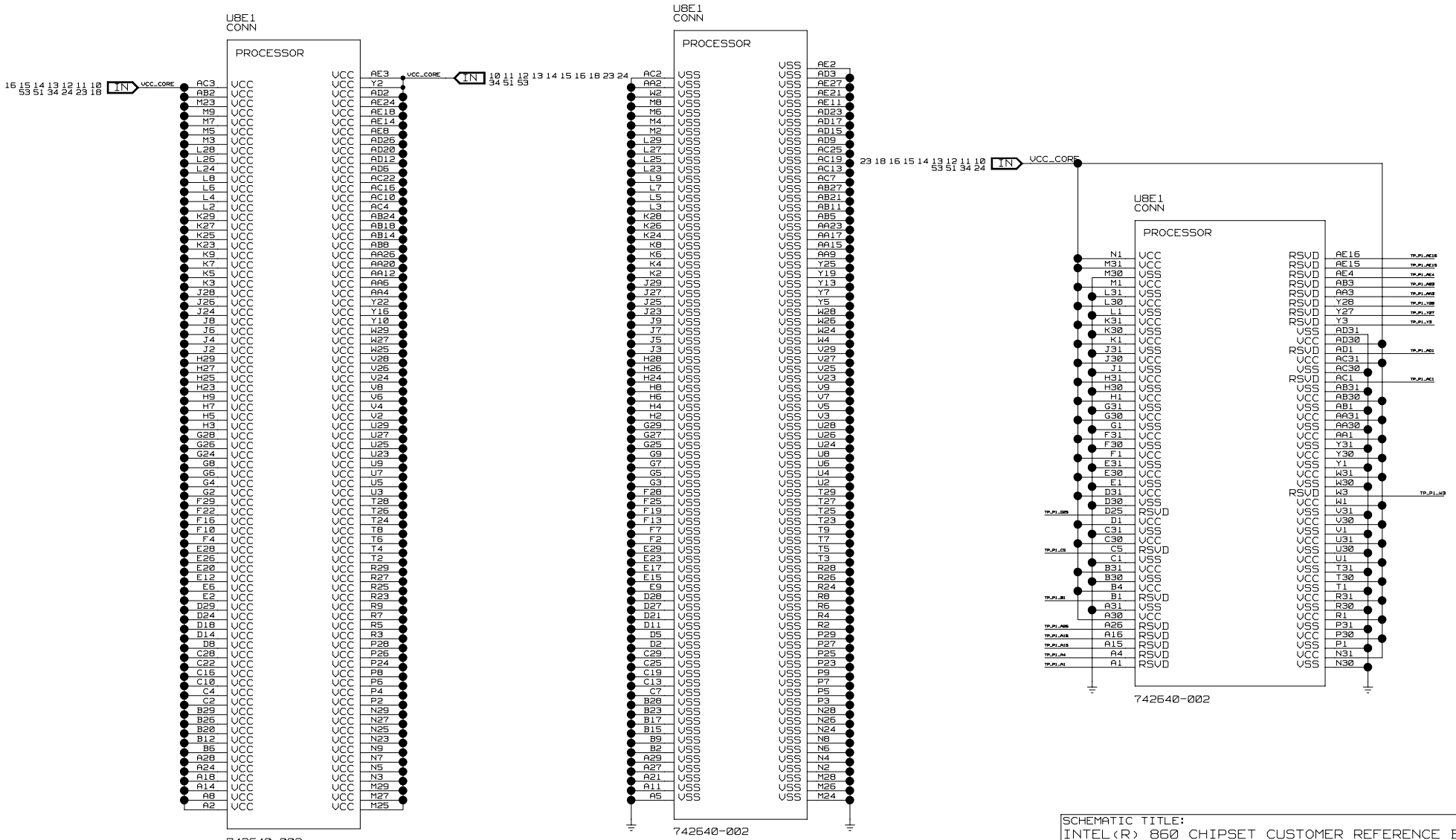
LAST REVISED:	Thu May 17 14:03:59 2001
SHEET:	11

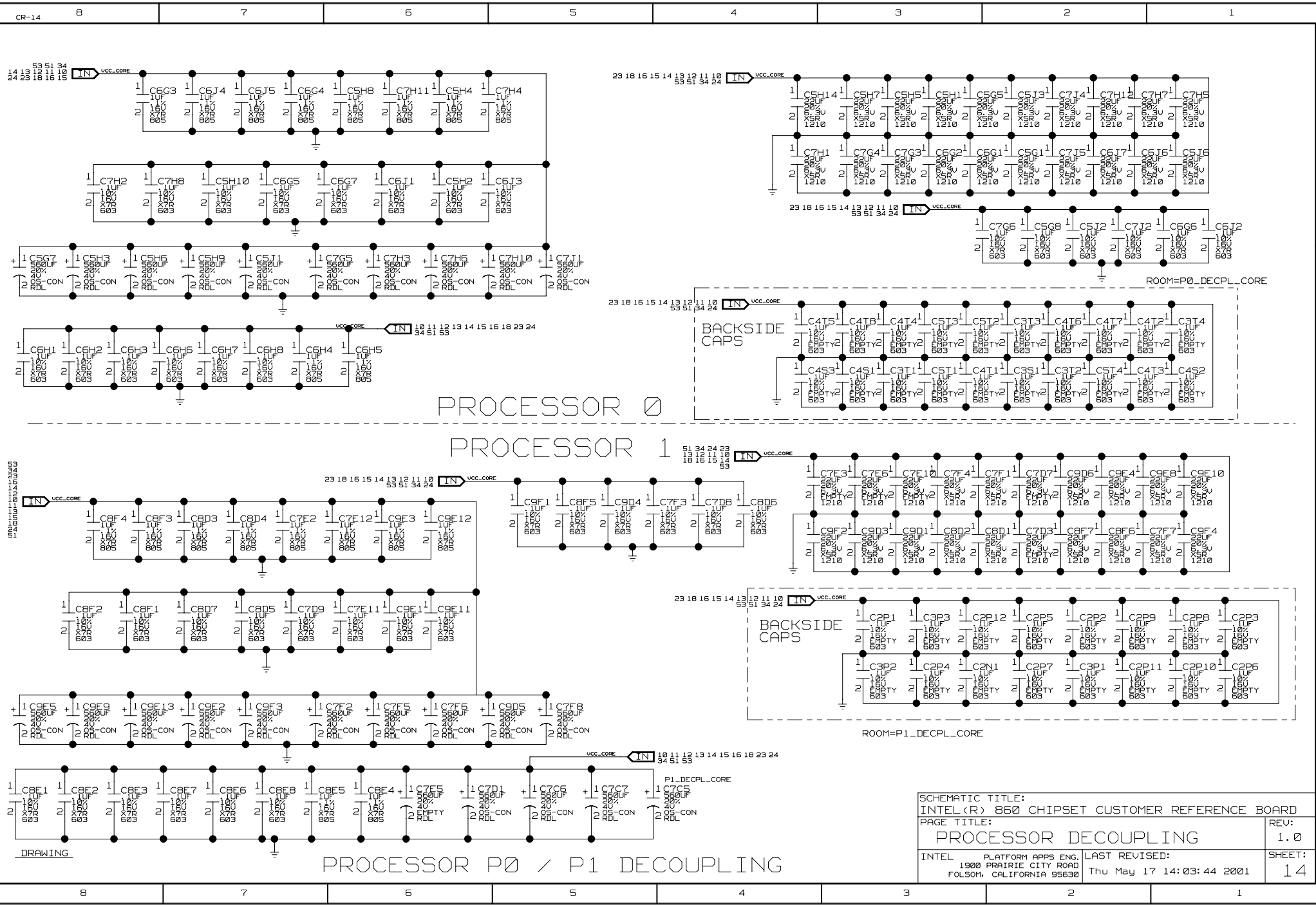

U8E1
CONN
PROCESSOR
742640-002
SMBUS PARTITION 1
CPU THERMAL SENSOR SMBUS = 32
CPU IDROM SMBUS = A2
CAD NOTE:
PLACE TERMINATION RESISTORS NEXT TO P1
PLACE AC TERMINATION
LESS THAN 1 INCH FROM PIN
CAD NOTE:
PLACE CAPS CLOSE TO
PINS AB4 AD4 AA5
CAD NOTE:
1 CAP PER PIN
TOTAL RESISTANCE BETWEEN PROCESSOR AND CAPACITORS IS BETWEEN .35 AND 2 OHMS
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
PROCESSOR 1 (P1)
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:54 2001
SHEET:
12
DRAWING
PROCESSOR 1 (P1)



DRAWING

PROCESSOR 1 / POWER GROUND & RESERVED

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PROCESSOR 1		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:49 2001	SHEET: 13



SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

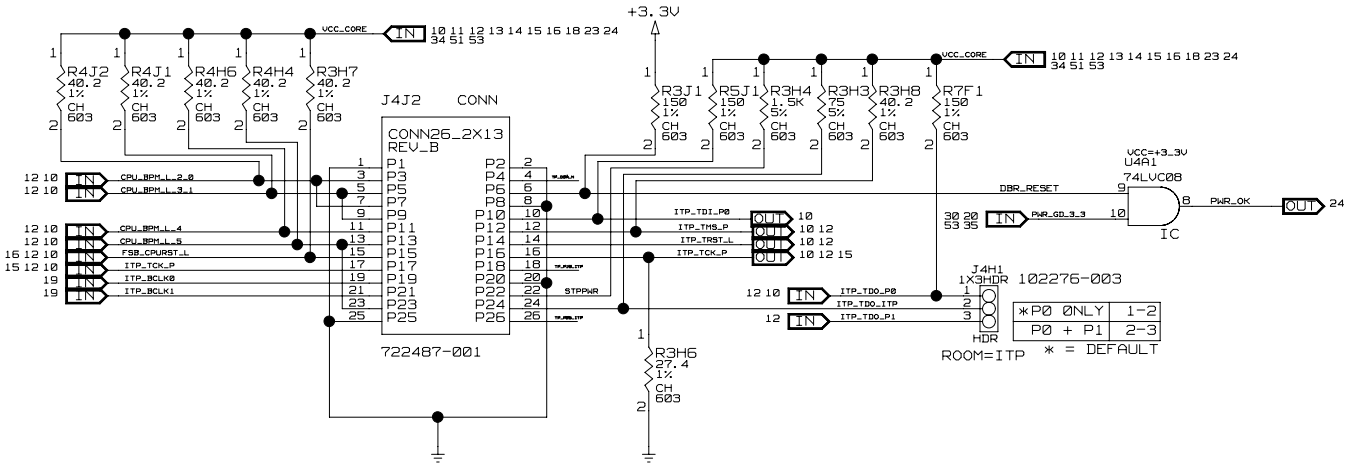
PAGE TITLE:
PROCESSOR DECOUPLING

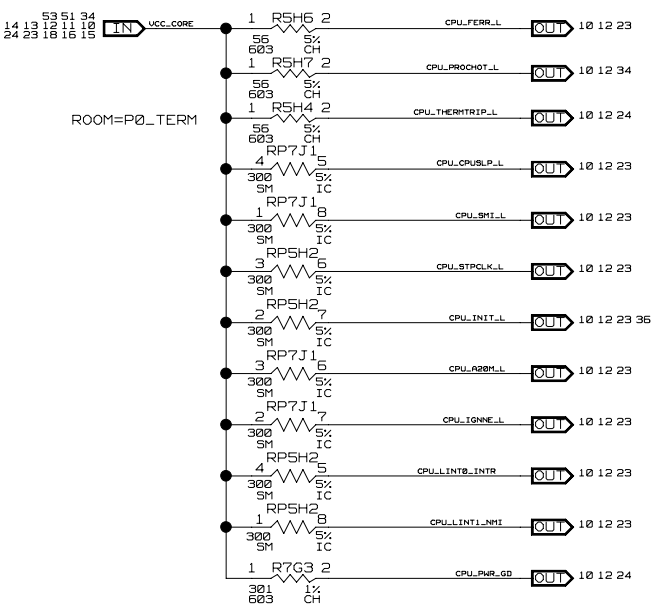
REV:
1.0

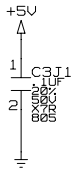
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

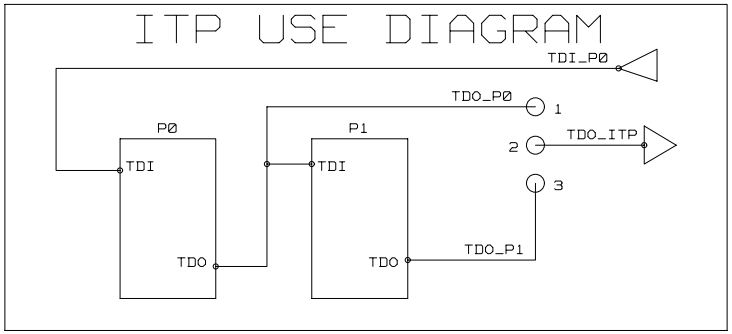
LAST REVISED:
Thu May 17 14:03:44 2001

SHEET:
14







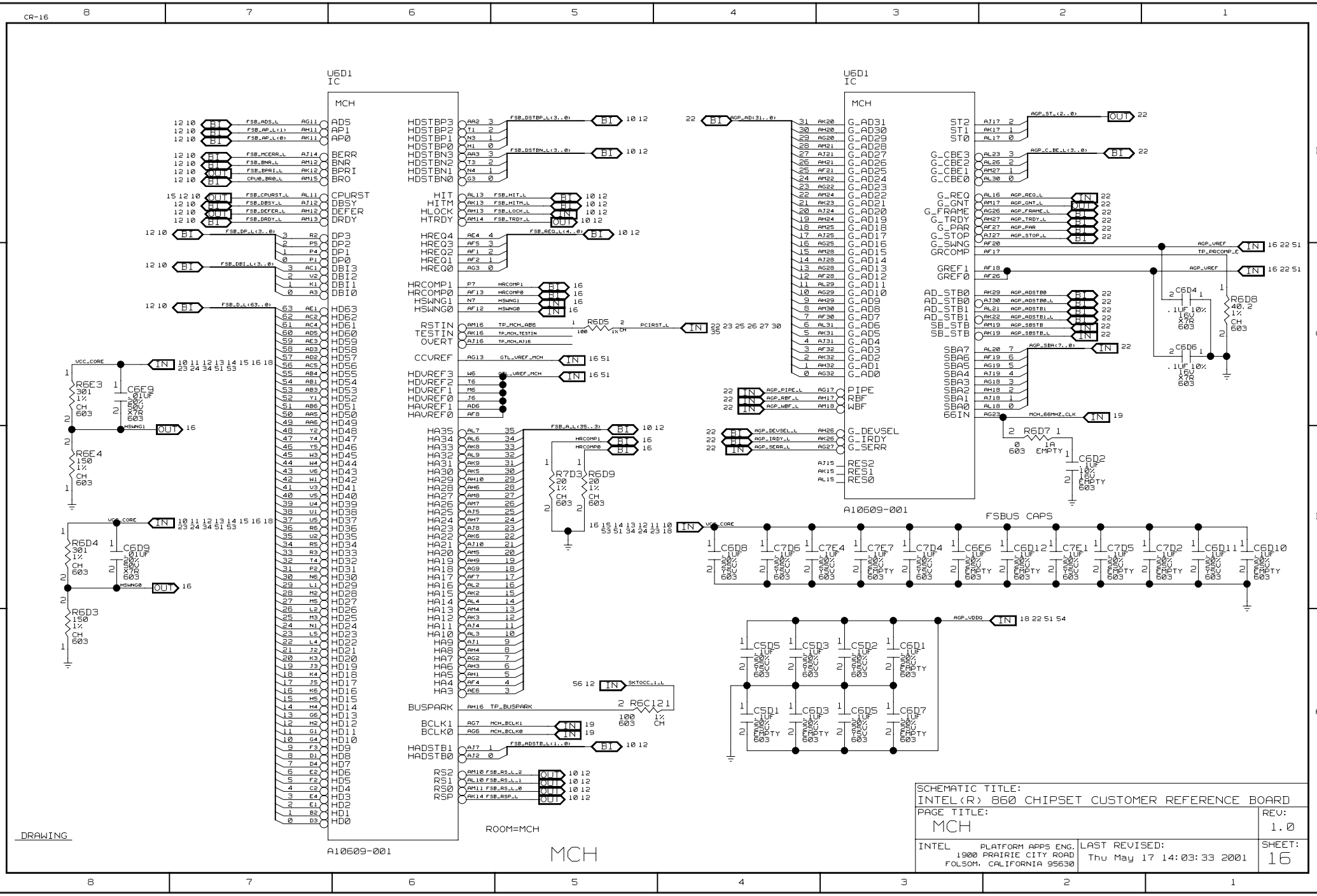


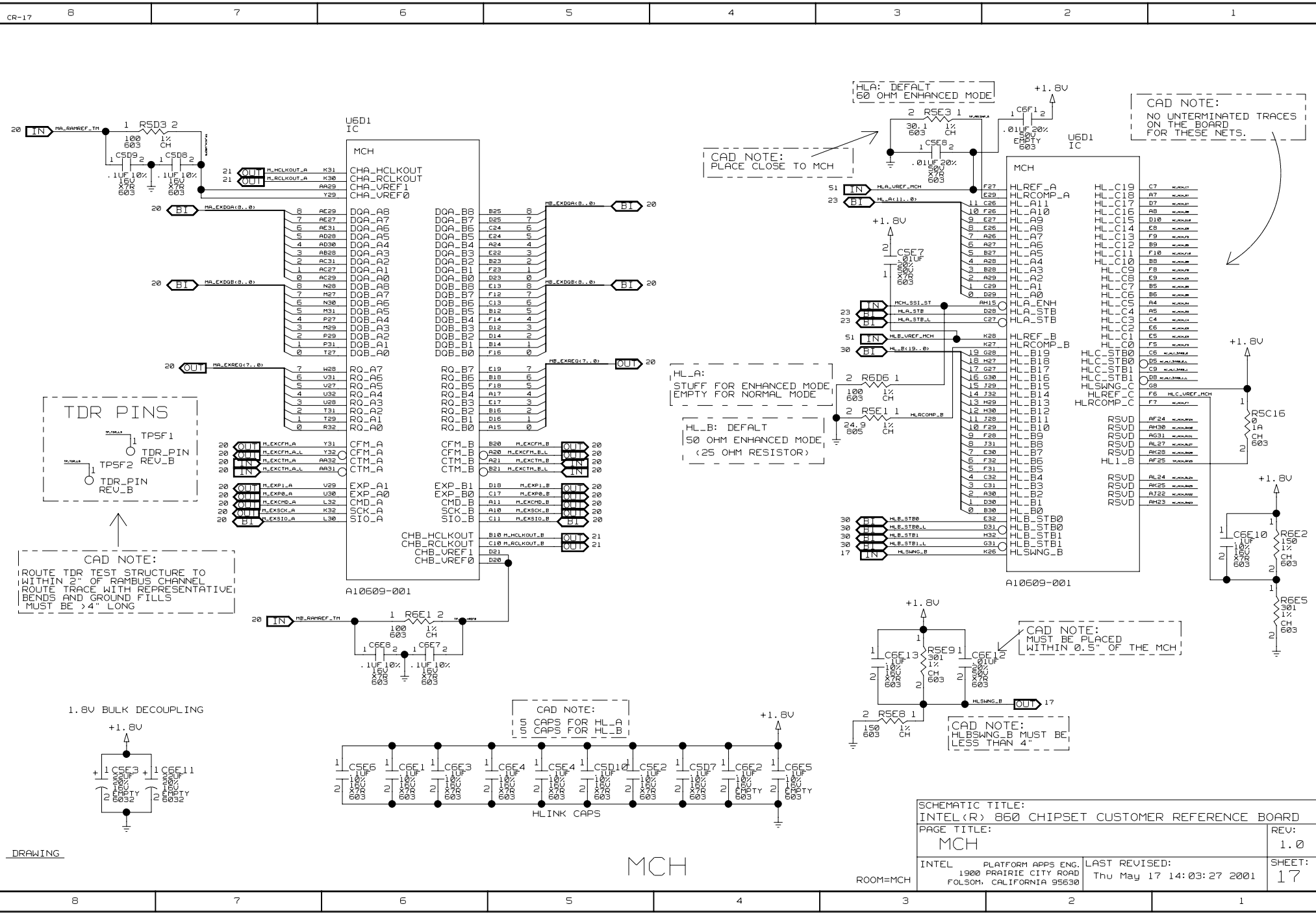
DRAWING

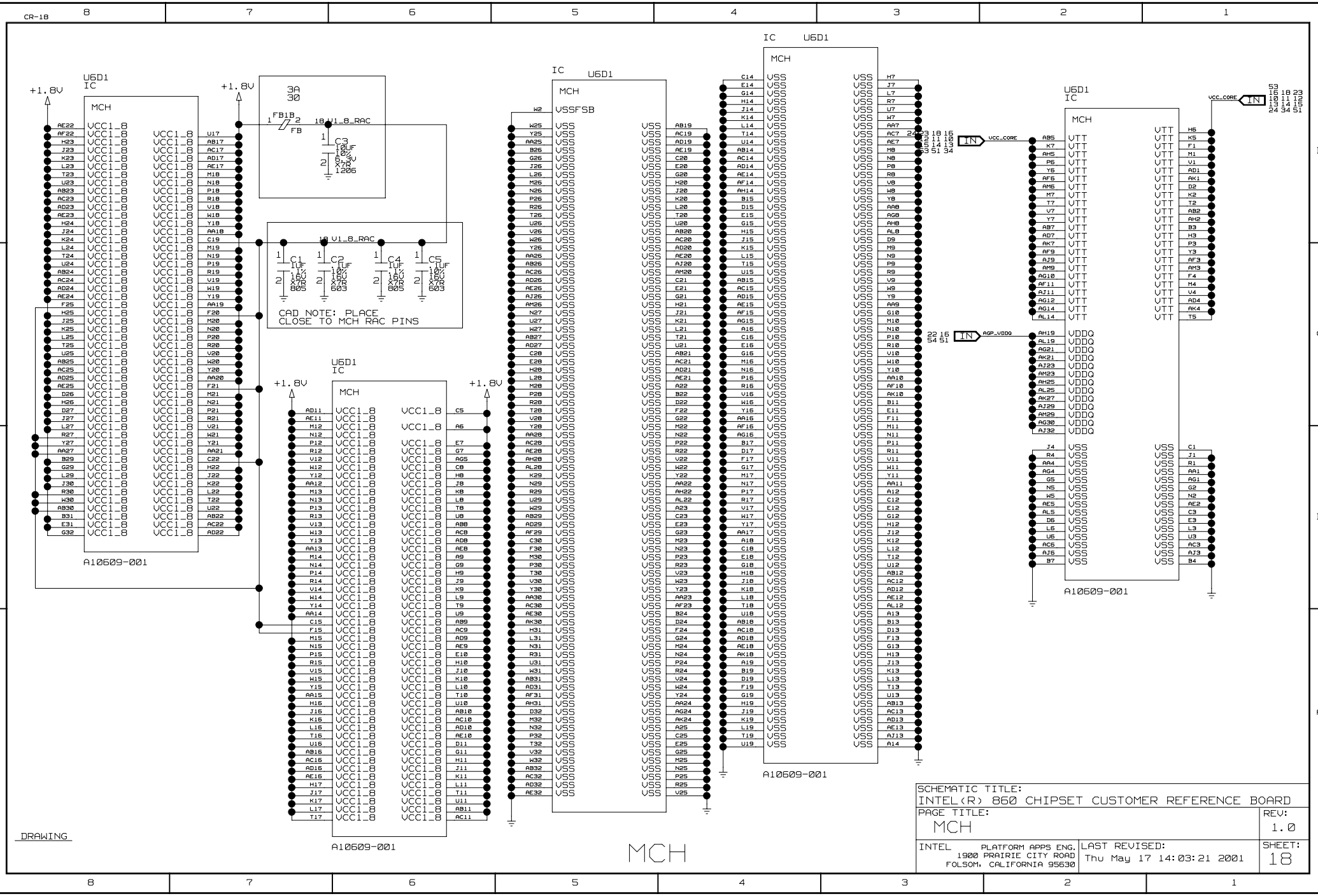
ITP

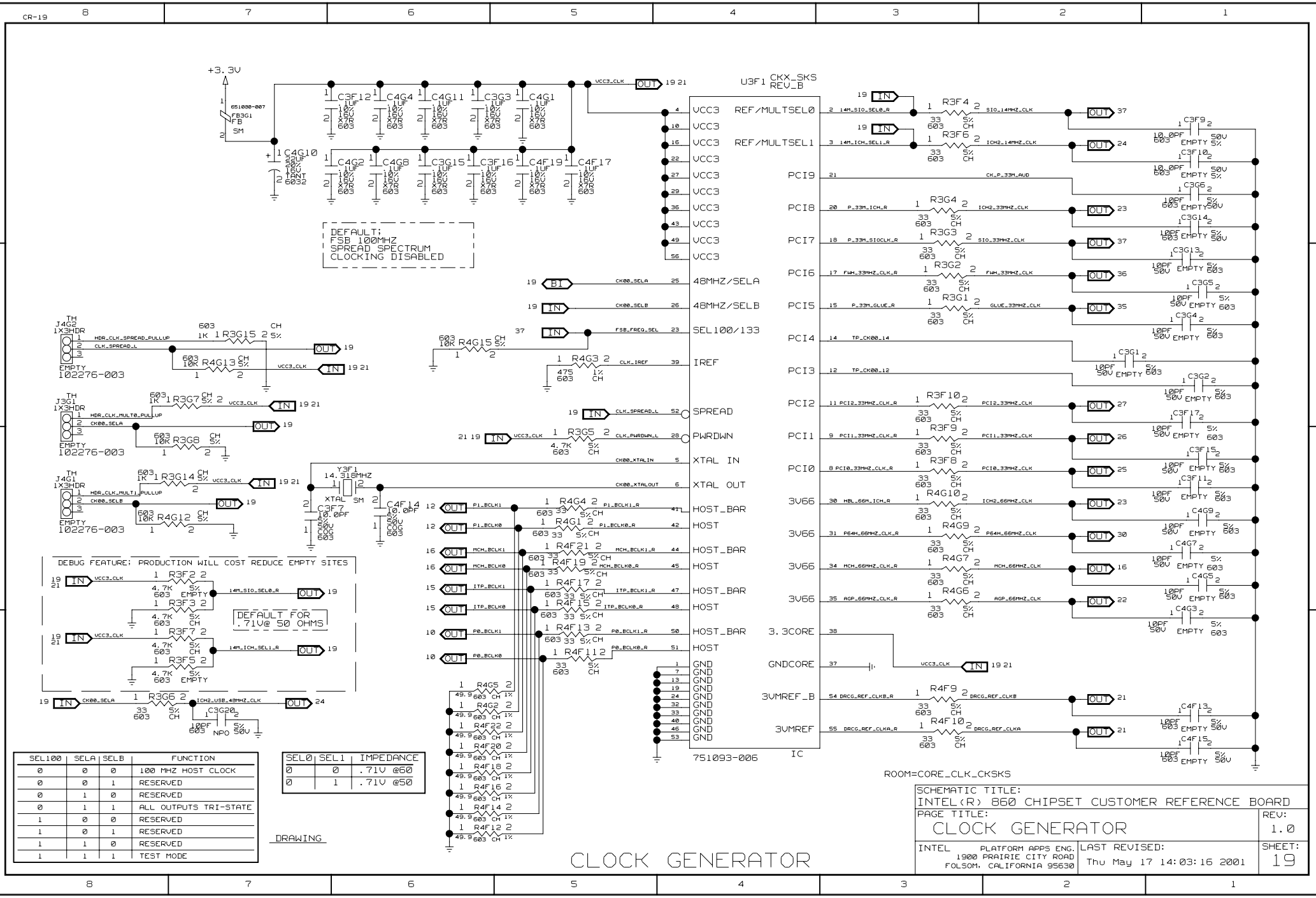
ROOM=ITP

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: ITP	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:39 2001
	SHEET: 15


U6D1
IC
MCH
A10609-001
ROOM=MCH
MCH
DRAWING
FSBUS CAPS
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:33 2001
SHEET:
16

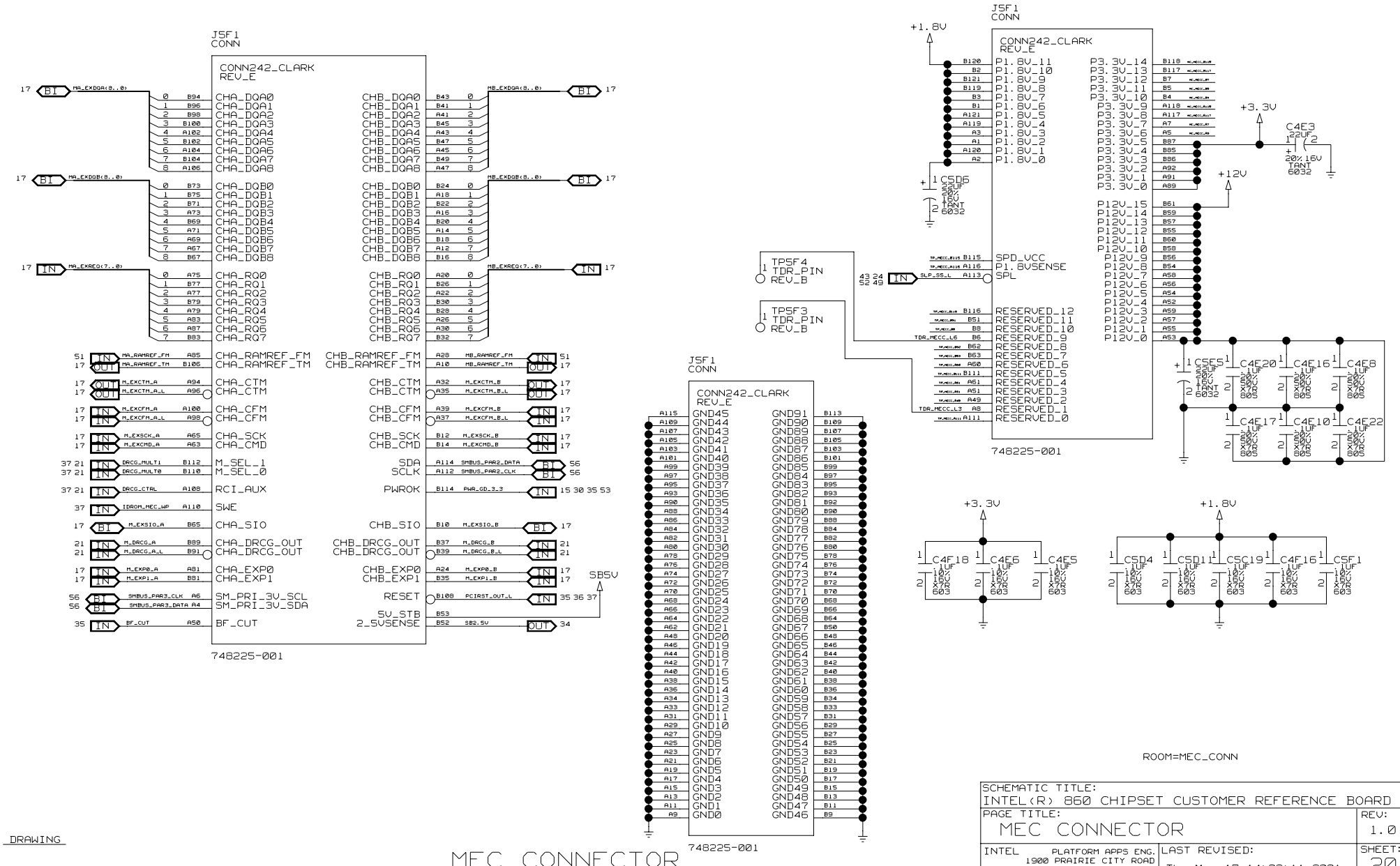

CR-17
U6D1
IC
MCH
A10609-001
TDR PINS
TPSF1
TDR_PIN
REV_B
TPSF2
TDR_PIN
REV_B
CAD NOTE:
ROUTE TDR TEST STRUCTURE TO WITHIN 2" OF RAMBUS CHANNEL
ROUTE TRACE WITH REPRESENTATIVE BENDS AND GROUND FILLS
MUST BE >4" LONG
HLA: DEFALT
60 OHM ENHANCED MODE
CAD NOTE:
PLACE CLOSE TO MCH
CAD NOTE:
NO UNTERMINATED TRACES
ON THE BOARD
FOR THESE NETS.
HL_A:
STUFF FOR ENHANCED MODE
EMPTY FOR NORMAL MODE
HL_B: DEFALT
50 OHM ENHANCED MODE
(25 OHM RESISTOR)
CAD NOTE:
MUST BE PLACED
WITHIN 0.5" OF THE MCH
CAD NOTE:
HLBSWNG_B MUST BE
LESS THAN 4"
CAD NOTE:
5 CAPS FOR HL_A
5 CAPS FOR HL_B
HLINK CAPS
1.8V BULK DECOUPLING
+1.8V
DRAWING
MCH
ROOM=MCH
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:27 2001
SHEET:
17


CR-1B
U6D1
IC
MCH
+1.8V
3A
30
FB1B
FB
1B_V1_8_RAC
C3
10UF
10%
6.3V
X7R
1206
C1
1UF
16V
X5R
805
C2
10UF
10%
6.3V
X5R
603
C4
1UF
16V
X5R
805
C5
10UF
10%
6.3V
X5R
603
CAD NOTE: PLACE
CLOSE TO MCH RAC PINS
A10609-001
VSSFSB
VSS
VCC1_8
VTT
VDDQ
VCC_CORE
AGP_VDDQ
IN
MCH
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
MCH
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:03:21 2001
SHEET:
18
DRAWING



SEL100	SELA	SELB	FUNCTION
0	0	0	100 MHZ HOST CLOCK
0	0	1	RESERVED
0	1	0	RESERVED
0	1	1	ALL OUTPUTS TRI-STATE
1	0	0	RESERVED
1	0	1	RESERVED
1	1	0	RESERVED
1	1	1	TEST MODE

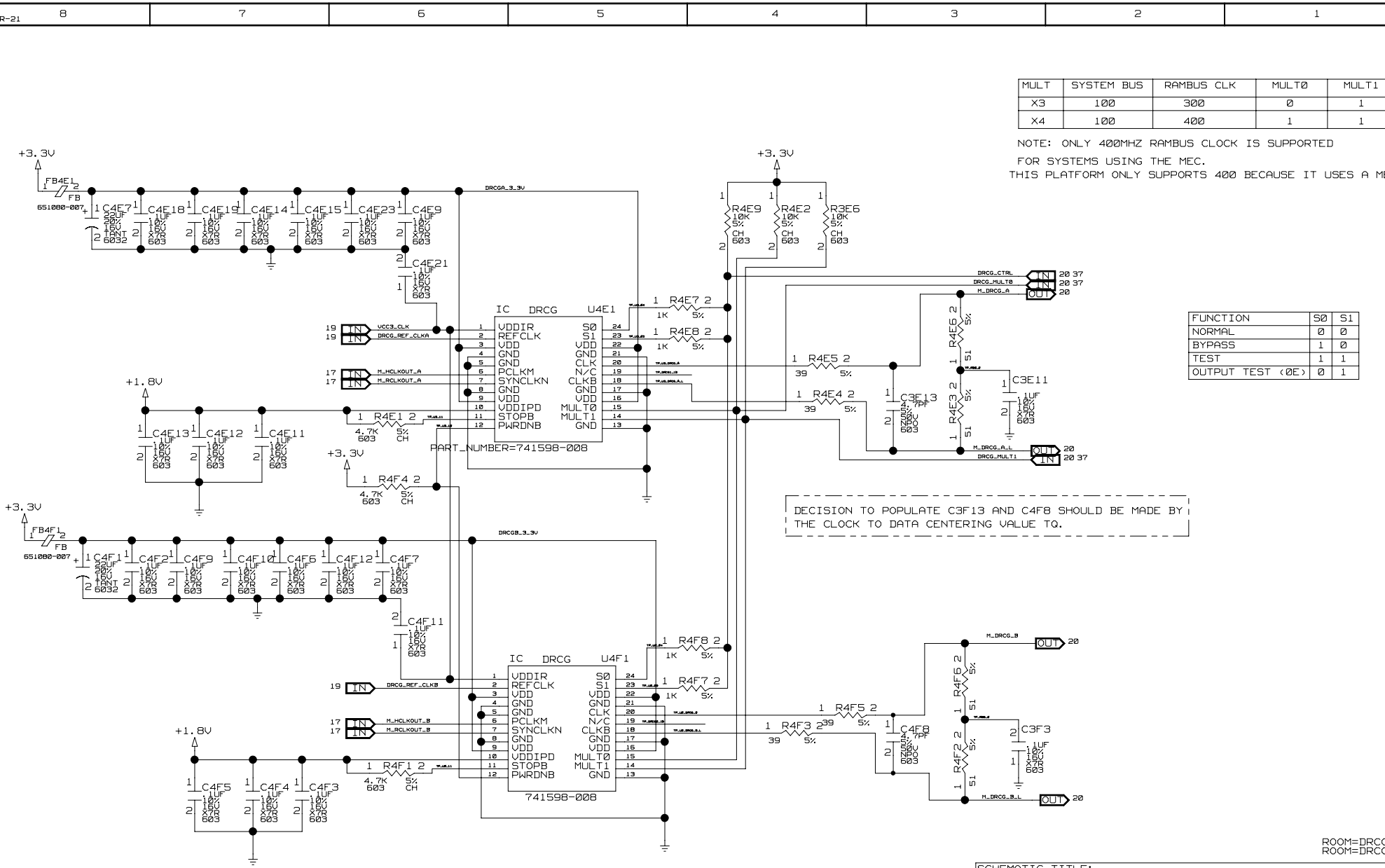
SEL0	SEL1	IMPEDANCE
0	0	.71V @60
0	1	.71V @50

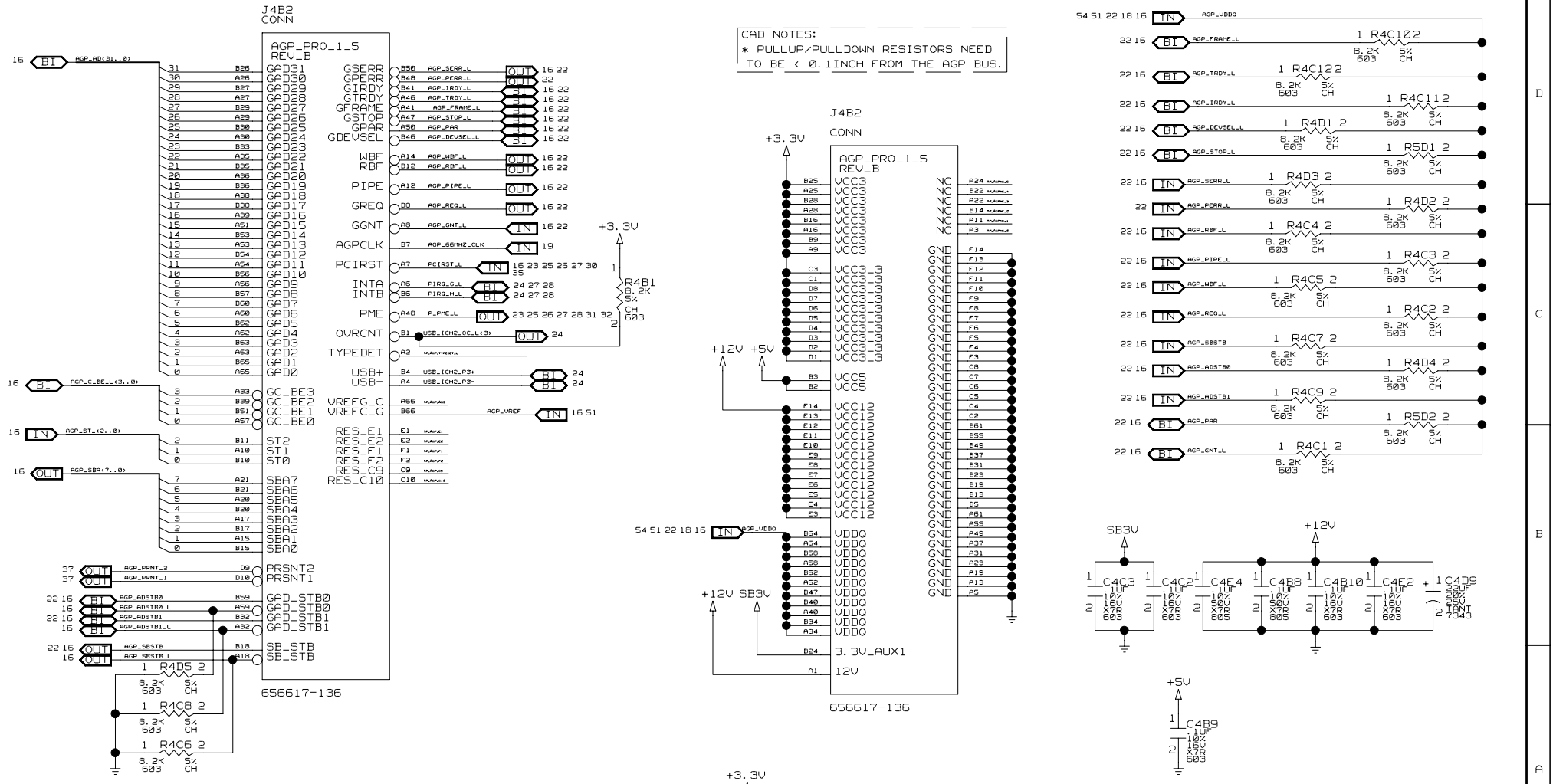


DRAWING

MEC CONNECTOR

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: MEC CONNECTOR	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:11 2001
	SHEET: 20

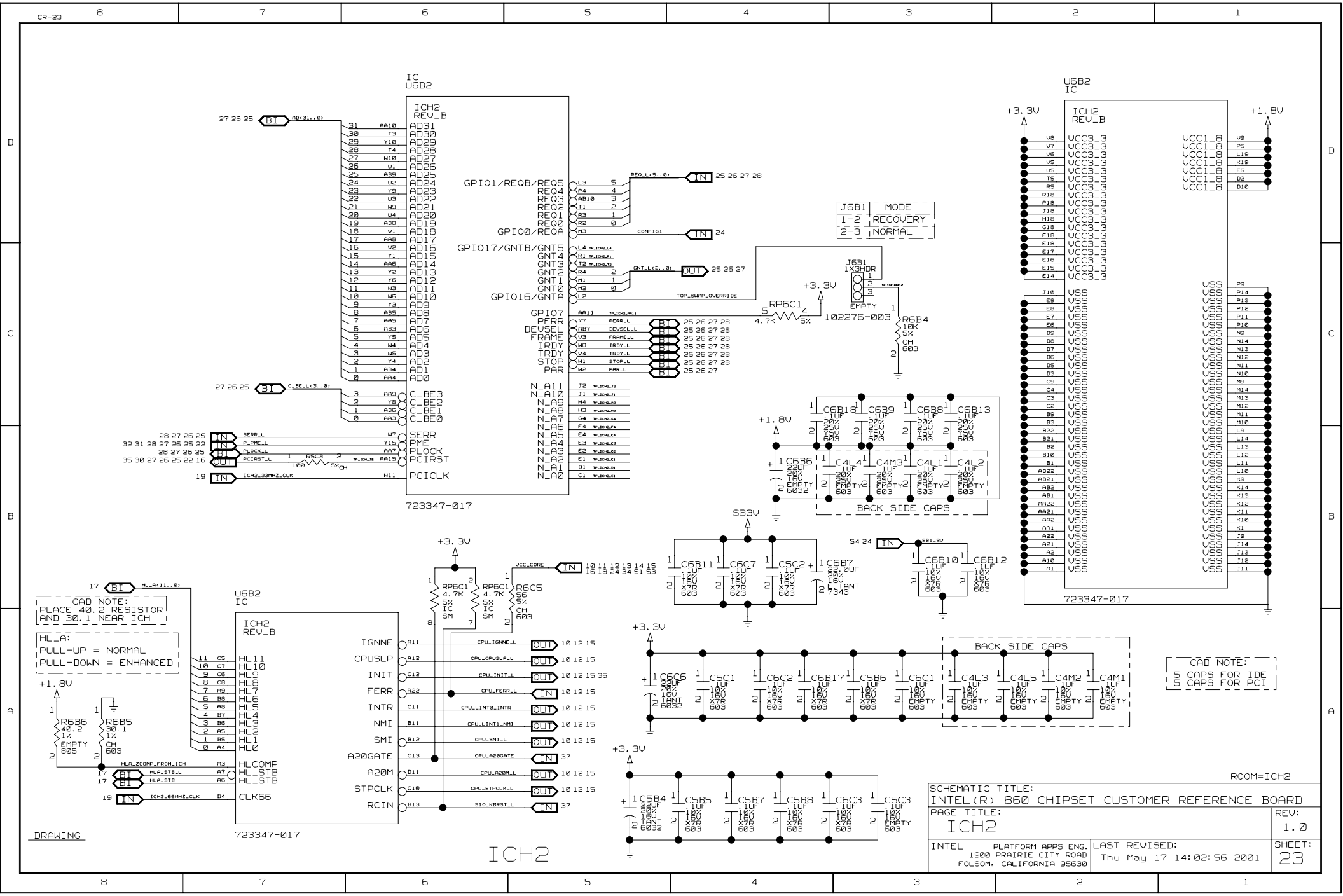

CR-21
8
7
6
5
4
3
2
1
D
C
B
A
MULT | SYSTEM BUS | RAMBUS CLK | MULT0 | MULT1
X3 | 100 | 300 | 0 | 1
X4 | 100 | 400 | 1 | 1
NOTE: ONLY 400MHZ RAMBUS CLOCK IS SUPPORTED
FOR SYSTEMS USING THE MEC.
THIS PLATFORM ONLY SUPPORTS 400 BECAUSE IT USES A MEC.
FUNCTION | S0 | S1
NORMAL | 0 | 0
BYPASS | 1 | 0
TEST | 1 | 1
OUTPUT TEST (0E) | 0 | 1
+3.3V
+1.8V
FB4E1
FB4F1
651000-007
IC DRCG U4E1
IC DRCG U4F1
VDDIR
REFCLK
VDD
GND
PCLKM
SYNCLKN
VDDIPD
STOPB
PWRDNB
S0
S1
N/C
CLKB
MULT0
MULT1
PART_NUMBER=741598-008
741598-008
DRCGA_3_3V
DRCGB_3_3V
VCC3_CLK
DRCG_REF_CLKA
DRCG_REF_CLKB
M_HCLKOUT_A
M_RCLKOUT_A
M_HCLKOUT_B
M_RCLKOUT_B
DRCG_CTRL
DRCG_MULT0
DRCG_MULT1
M_DRCG_A
M_DRCG_A_L
M_DRCG_B
M_DRCG_B_L
R4E9 10K 5% CH 603
R4E2 10K 5% CH 603
R3E6 10K 5% CH 603
R4E7 2 1K 5%
R4E8 2 1K 5%
R4E5 2 39 5%
R4E4 2 39 5%
R4E3 2 51 5%
R4E6 2 51 5%
R4E1 2 4.7K 603 5% CH
R4F8 2 1K 5%
R4F7 2 1K 5%
R4F5 2 39 5%
R4F3 2 39 5%
R4F6 2 51 5%
R4F2 2 51 5%
R4F4 2 4.7K 603 5% CH
R4F1 2 4.7K 603 5% CH
C4E7 22UF 20% 16V TANT 6032
C4E18 C4E19 C4E14 C4E15 C4E23 C4E9 C4E21 C4E13 C4E12 C4E11
C4F1 C4F2 C4F9 C4F10 C4F6 C4F12 C4F7 C4F11 C4F5 C4F4 C4F3
C3E11 C3F3
C4E8 C4F8 4.7PF 50V COG 603
DECISION TO POPULATE C3F13 AND C4F8 SHOULD BE MADE BY
THE CLOCK TO DATA CENTERING VALUE TQ.
ROOM=DRCG0
ROOM=DRCG1
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
DRCG* (RAMBUS CLOCK)
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Fri May 18 14:01:20 2001
SHEET:
21
DRAWING
DRCG* (RAMBUS CLOCK)

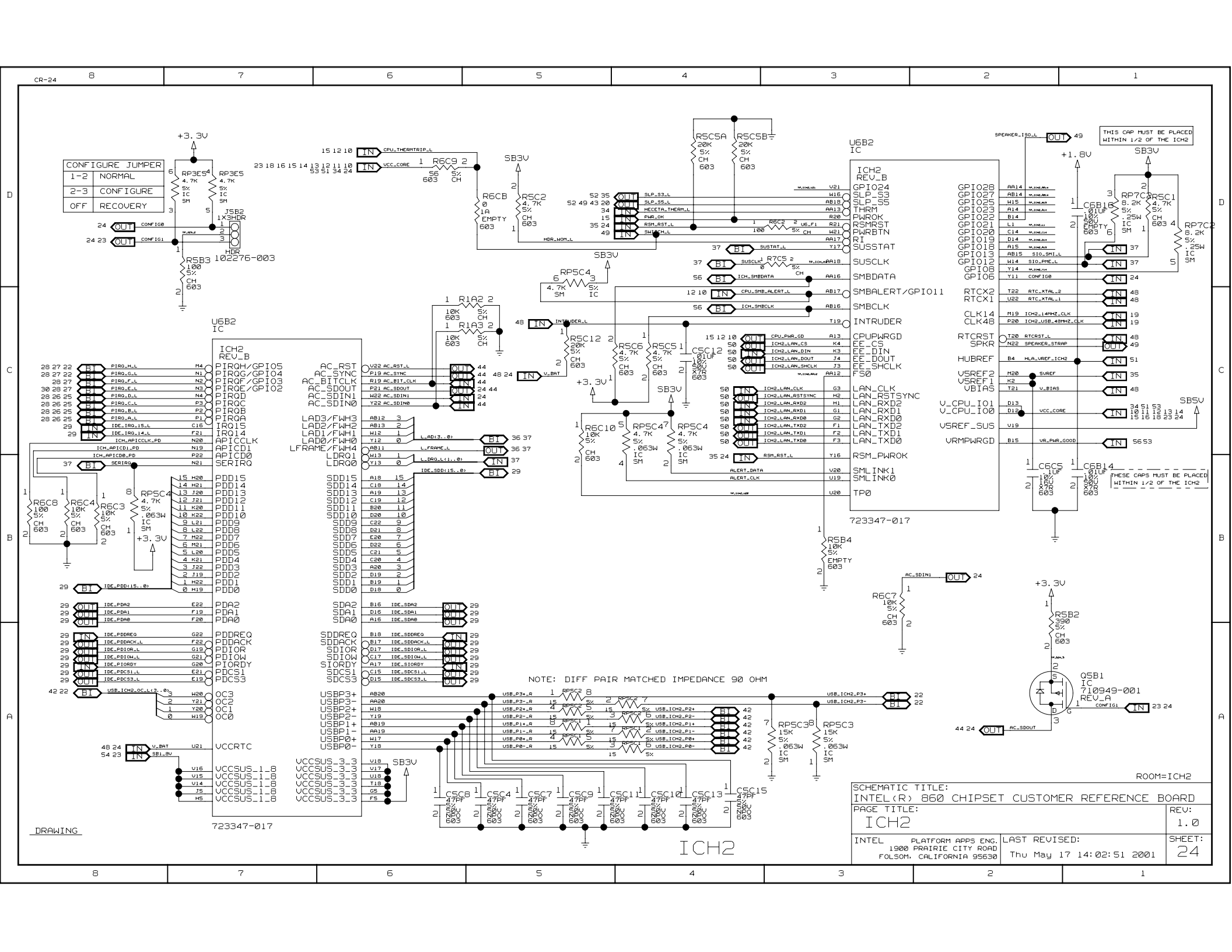


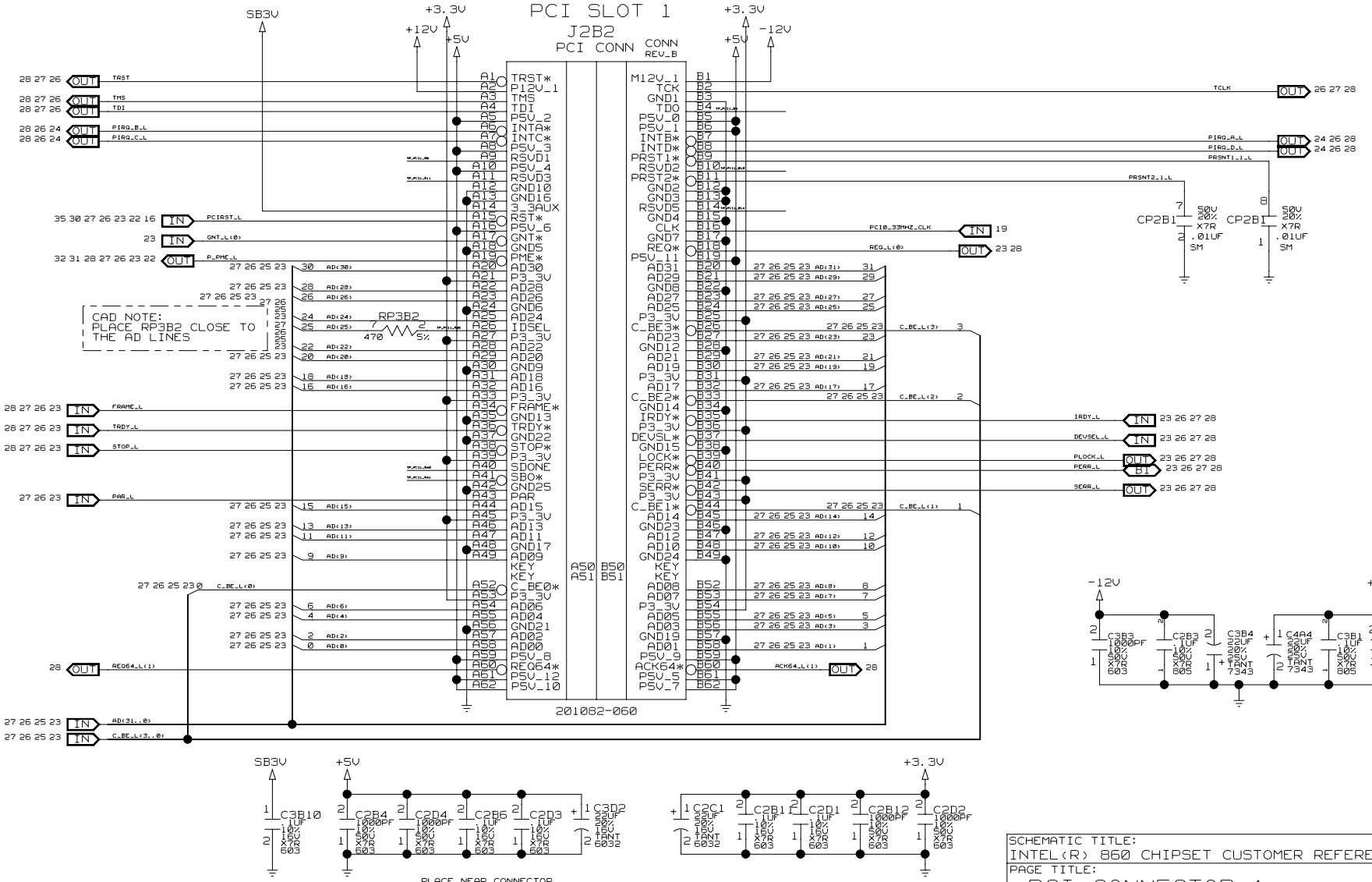
AGP CONNECTOR

ROOM=AGP

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AGP CONNECTOR	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:03:01 2001
	SHEET: 22


IC
U6B2
ICH2
REV_B
723347-017
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
C_BE3
C_BE2
C_BE1
C_BE0
SERR
PME
PLOCK
PCIRST
PCICLK
GPIO1/REQB/REQ5
REQ4
REQ3
REQ2
REQ1
REQ0
GPIO0/REQA
GPIO17/GNTB/GNT5
GNT4
GNT3
GNT2
GNT1
GNT0
GPIO16/GNTA
GPIO7
PERR
DEVSEL
FRAME
IRDY
TRDY
STOP
PAR
N_A11
N_A10
N_A9
N_A8
N_A7
N_A6
N_A5
N_A4
N_A3
N_A2
N_A1
N_A0
REQ_L(5..0)
CONFIG1
GNT_L(2..0)
TOP_SWAP_OVERRIDE
J6B1
MODE
1-2 RECOVERY
2-3 NORMAL
J6B1
1X3HDR
EMPTY
102276-003
RP6C1
4.7K
R6B4
10K
CH
603
+3.3V
+1.8V
SB3V
BACK SIDE CAPS
CAD NOTE:
PLACE 40.2 RESISTOR
AND 30.1 NEAR ICH
HL_A:
PULL-UP = NORMAL
PULL-DOWN = ENHANCED
R6B6
40.2
EMPTY
805
R6B5
30.1
CH
603
HL11
HL10
HL9
HL8
HL7
HL6
HL5
HL4
HL3
HL2
HL1
HL0
HLCOMP
HL_STB
HL_STB
CLK66
IGNNE
CPUSLP
INIT
FERR
INTR
NMI
SMI
A20GATE
A20M
STPCLK
RCIN
R6C5
56
CAD NOTE:
5 CAPS FOR IDE
5 CAPS FOR PCI
DRAWING
ICH2
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
ICH2
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:02:56 2001
SHEET:
23
ROOM=ICH2


CR-24
CONFIGURE JUMPER
1-2 NORMAL
2-3 CONFIGURE
OFF RECOVERY
J5B2 1X3HDR
HDR 102276-003
U6B2 IC
ICH2 REV_B
723347-017
THIS CAP MUST BE PLACED WITHIN 1/2 OF THE ICH2
THESE CAPS MUST BE PLACED WITHIN 1/2 OF THE ICH2
NOTE: DIFF PAIR MATCHED IMPEDANCE 90 OHM
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
ICH2
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:02:51 2001
SHEET:
24
ROOM=ICH2
DRAWING
ICH2

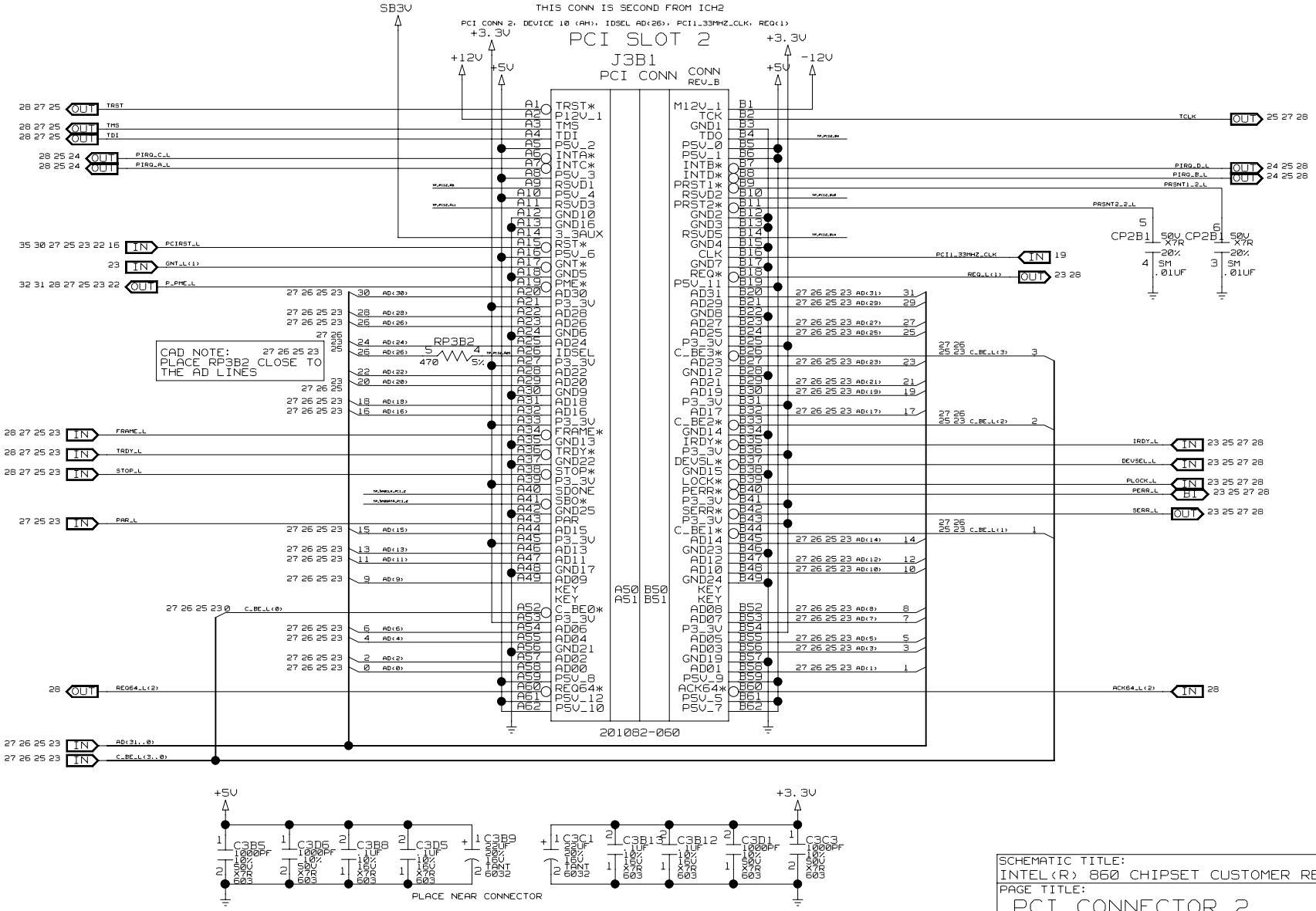


DRAWING

PCI CONNECTOR 1 AND DECOUPLING

ROOM=PCI1

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI CONNECTOR 1	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:46 2001
	SHEET: 25

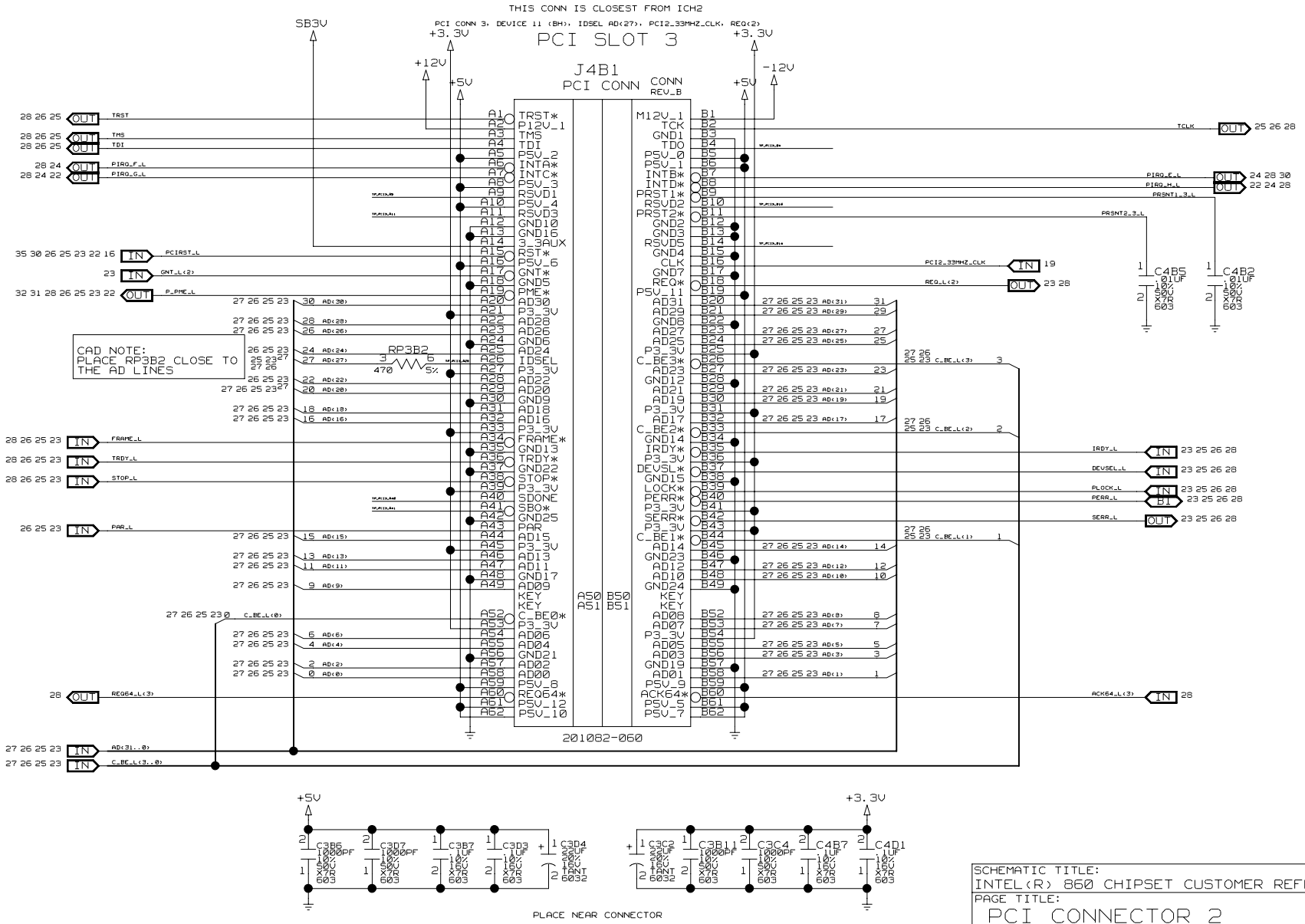


DRAWING

PCI CONNECTOR 2 AND DECOUPLING

ROOM=PCI2

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI CONNECTOR 2	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:41 2001
	SHEET: 26

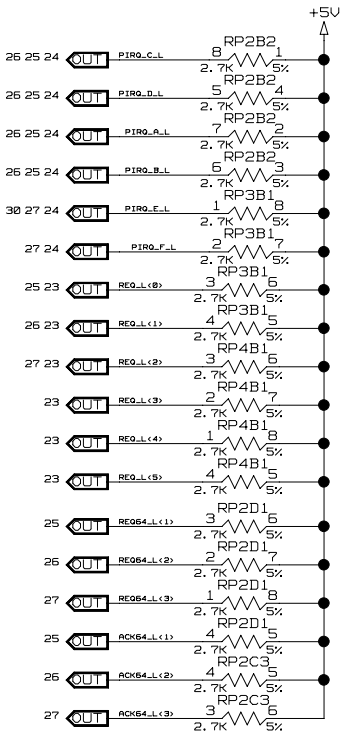


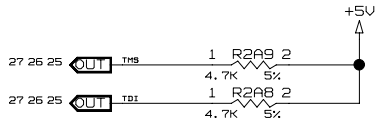
PCI CONNECTOR 3 AND DECOUPLING

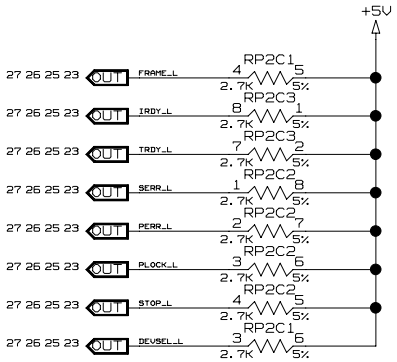
DRAWING

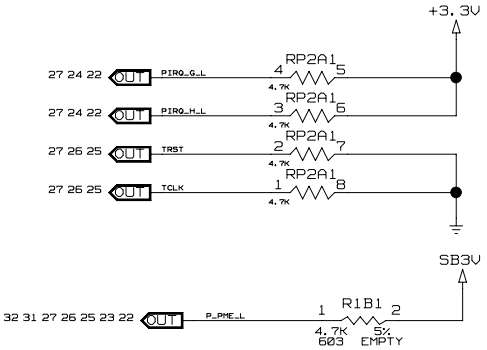
ROOM=PCI3

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI CONNECTOR 2	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:36 2001
	SHEET: 27









DRAWING

PCI33 TERMINATION

ROOM=PCI33_TERM

SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD

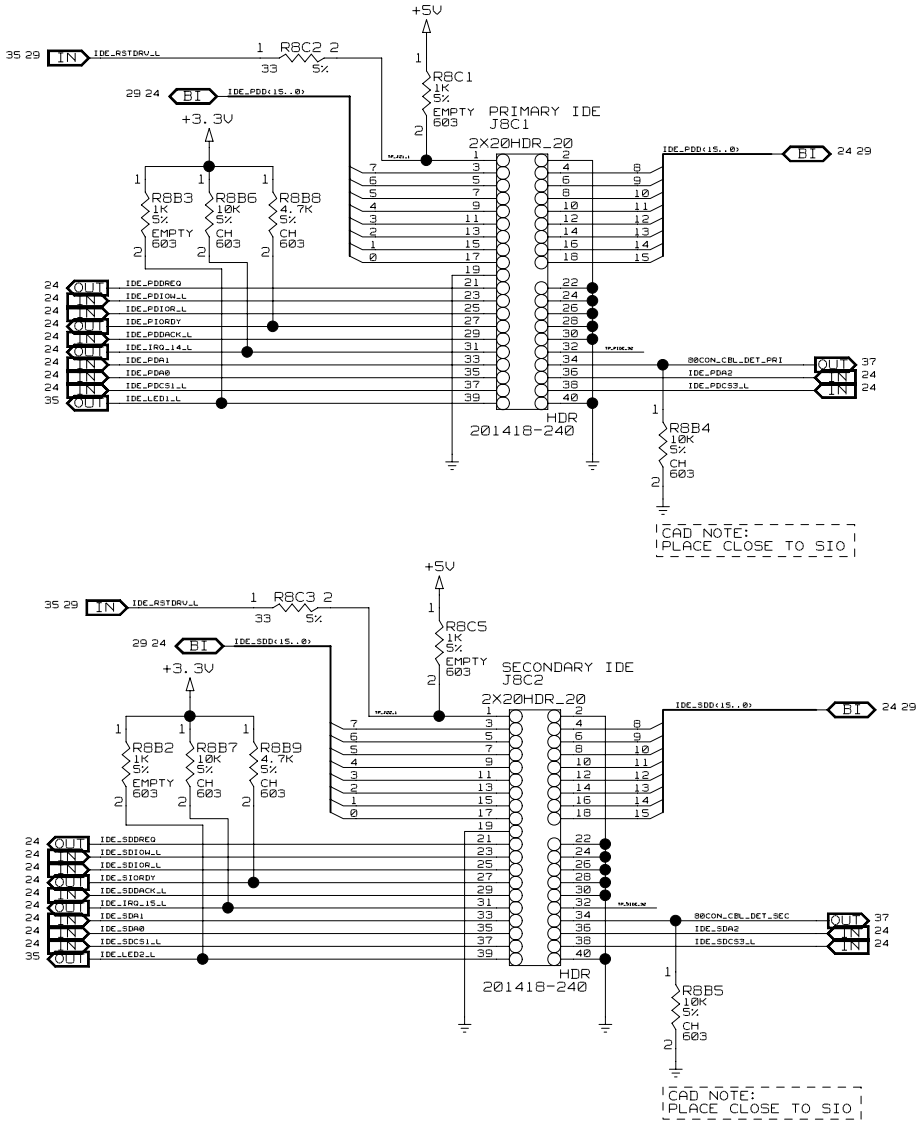
PAGE TITLE:
PCI33 TERMINATION

REV: 1.0

INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED:
Thu May 17 14:02:31 2001

SHEET: 28



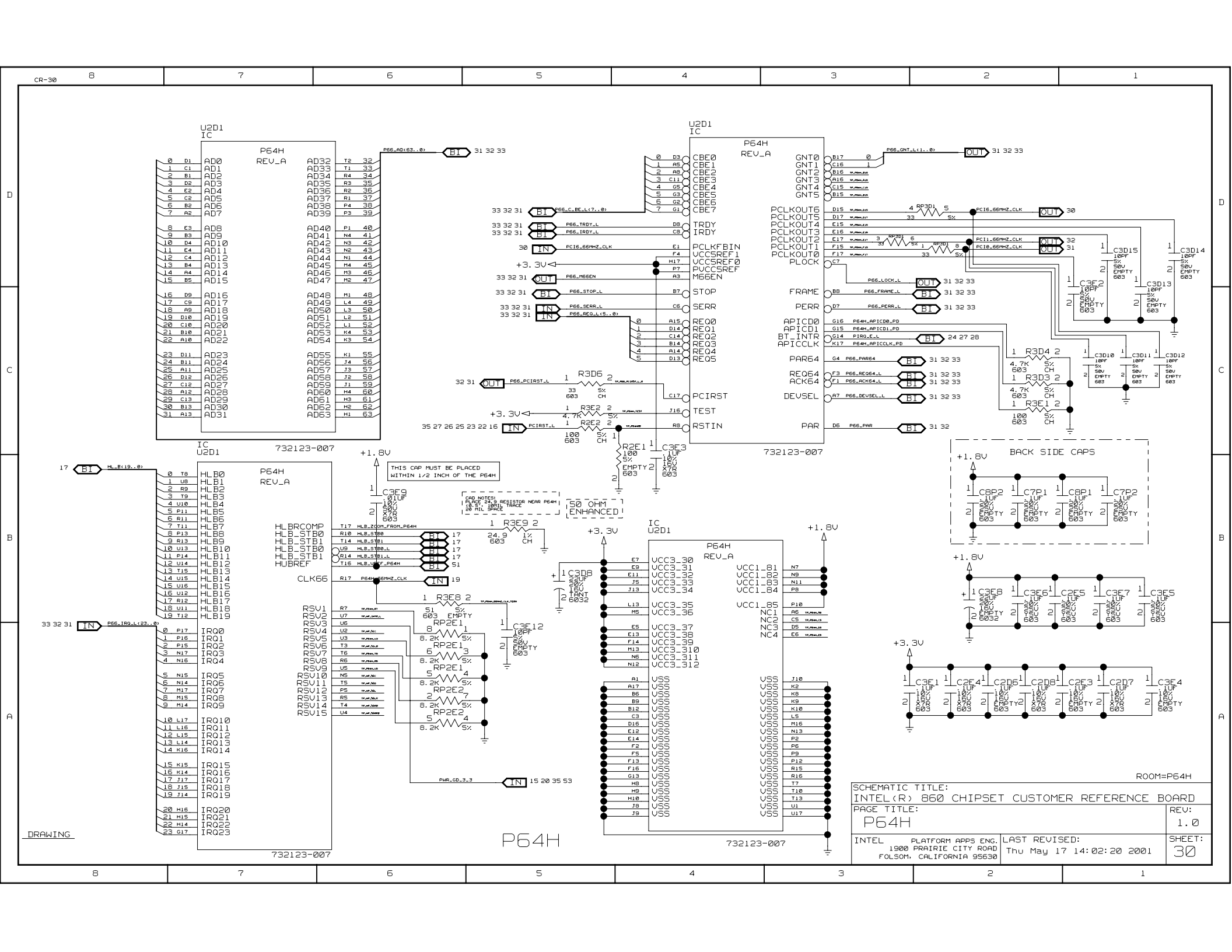
ROOM=IDEPRI

ROOM=IDESEC

DRAWING

IDE PRIMARY / SECONDARY

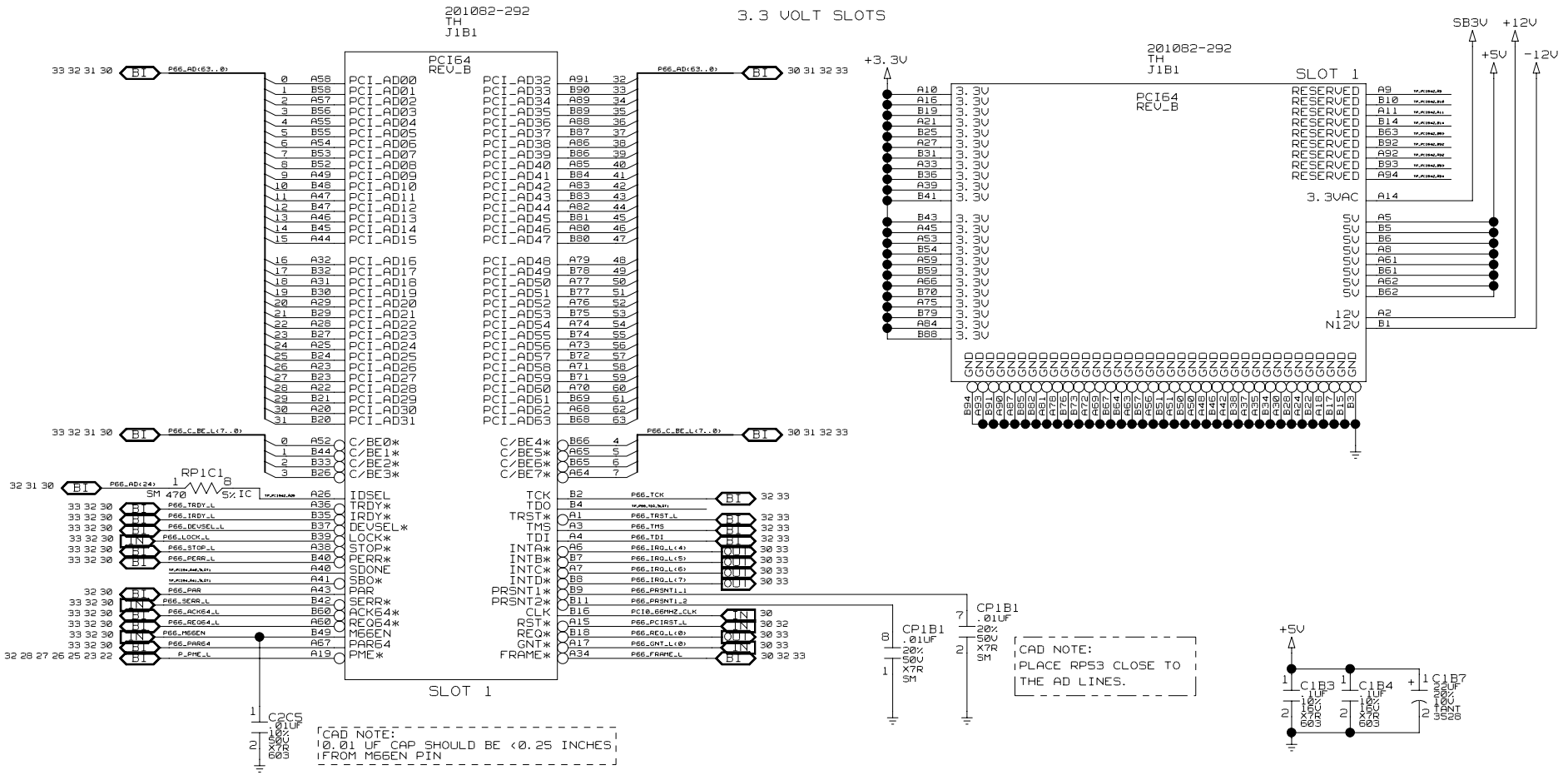
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: IDE PRIMARY / SECONDARY		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:26 2001	SHEET: 29

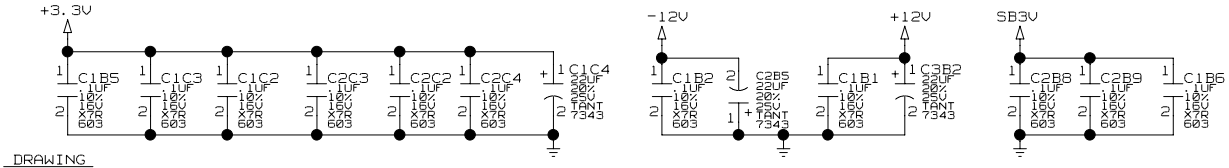

U2D1
IC
P64H
REV_A
732123-007
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
AD32
AD33
AD34
AD35
AD36
AD37
AD38
AD39
AD40
AD41
AD42
AD43
AD44
AD45
AD46
AD47
AD48
AD49
AD50
AD51
AD52
AD53
AD54
AD55
AD56
AD57
AD58
AD59
AD60
AD61
AD62
AD63
P66_AD<63..0>
CBE0
CBE1
CBE2
CBE3
CBE4
CBE5
CBE6
CBE7
P66_C_BE_L<7..0>
TRDY
IRDY
P66_TRDY_L
P66_IRDY_L
PCLKFBIN
VCC5REF1
VCC5REF0
PUCC5REF
M66EN
P66_M66EN
STOP
P66_STOP_L
SERR
P66_SERR_L
P66_REQ_L<5..0>
REQ0
REQ1
REQ2
REQ3
REQ4
REQ5
PCIRST
TEST
RSTIN
PCIRST_L
R3D6
R3E2
R2E2
R2E1
C3E3
GNT0
GNT1
GNT2
GNT3
GNT4
GNT5
P66_GNT_L<1..0>
PCLKOUT6
PCLKOUT5
PCLKOUT4
PCLKOUT3
PCLKOUT2
PCLKOUT1
PCLKOUT0
PLOCK
P66_LOCK_L
FRAME
P66_FRAME_L
PERR
P66_PERR_L
APICD0
APICD1
BT_INTR
APICCLK
P64H_APICD0_PD
P64H_APICD1_PD
P1RQ_E_L
P64H_APICCLK_PD
PAR64
P66_PAR64
REQ64
P66_REQ64_L
ACK64
P66_ACK64_L
DEVSEL
P66_DEVSEL_L
PAR
P66_PAR
RP3D1
R3D4
R3D3
R3E1
C3D15
C3D14
C3E2
C3D13
C3D10
C3D11
C3D12
PCI6_66MHZ_CLK
PCI1_66MHZ_CLK
BACK SIDE CAPS
C8P2
C7P1
C8P1
C7P2
HLB_B<19..0>
HLB0
HLB1
HLB2
HLB3
HLB4
HLB5
HLB6
HLB7
HLB8
HLB9
HLB10
HLB11
HLB12
HLB13
HLB14
HLB15
HLB16
HLB17
HLB18
HLB19
HLBRCOMP
HLB_STB0
HLB_STB1
HLB_STB0_L
HLB_STB1_L
HUBREF
CLK66
P64H_66MHZ_CLK
P66_IRQ_L<23..0>
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
IRQ16
IRQ17
IRQ18
IRQ19
IRQ20
IRQ21
IRQ22
IRQ23
RSV1
RSV2
RSV3
RSV4
RSV5
RSV6
RSV7
RSV8
RSV9
RSV10
RSV11
RSV12
RSV13
RSV14
RSV15
RP2E1
RP2E2
C3E12
R3E8
R3E9
C3E9
THIS CAP MUST BE PLACED
WITHIN 1/2 INCH OF THE P64H
CAD NOTES:
PLACE 24.9 RESISTOR NEAR P64H
(@ 5", 10MIL TRACE
20 MIL SPACE
50 OHM
ENHANCED
PWR_GD_3_3
C3D8
C3E1
C2E4
C2D6
C2D8
C2E3
C2D7
C3E4
C3E6
C2E5
C3E7
C3E5
C3E8
+1.8V
+3.3V
ROOM=P64H
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
P64H
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:02:20 2001
SHEET:
30
DRAWING
P64H

THIS CONN IS FIFTH FROM ICH2
PCI64 CONN 1, DEVICE 8 (8H), IDSEL P66_AD(24), PCI0_66MHZ_CLK, REQ(0)

PCI64 SLOT 1

3.3 VOLT SLOTS





DRAWING

PCI64 SLOT1

ROOM=PCI66_1

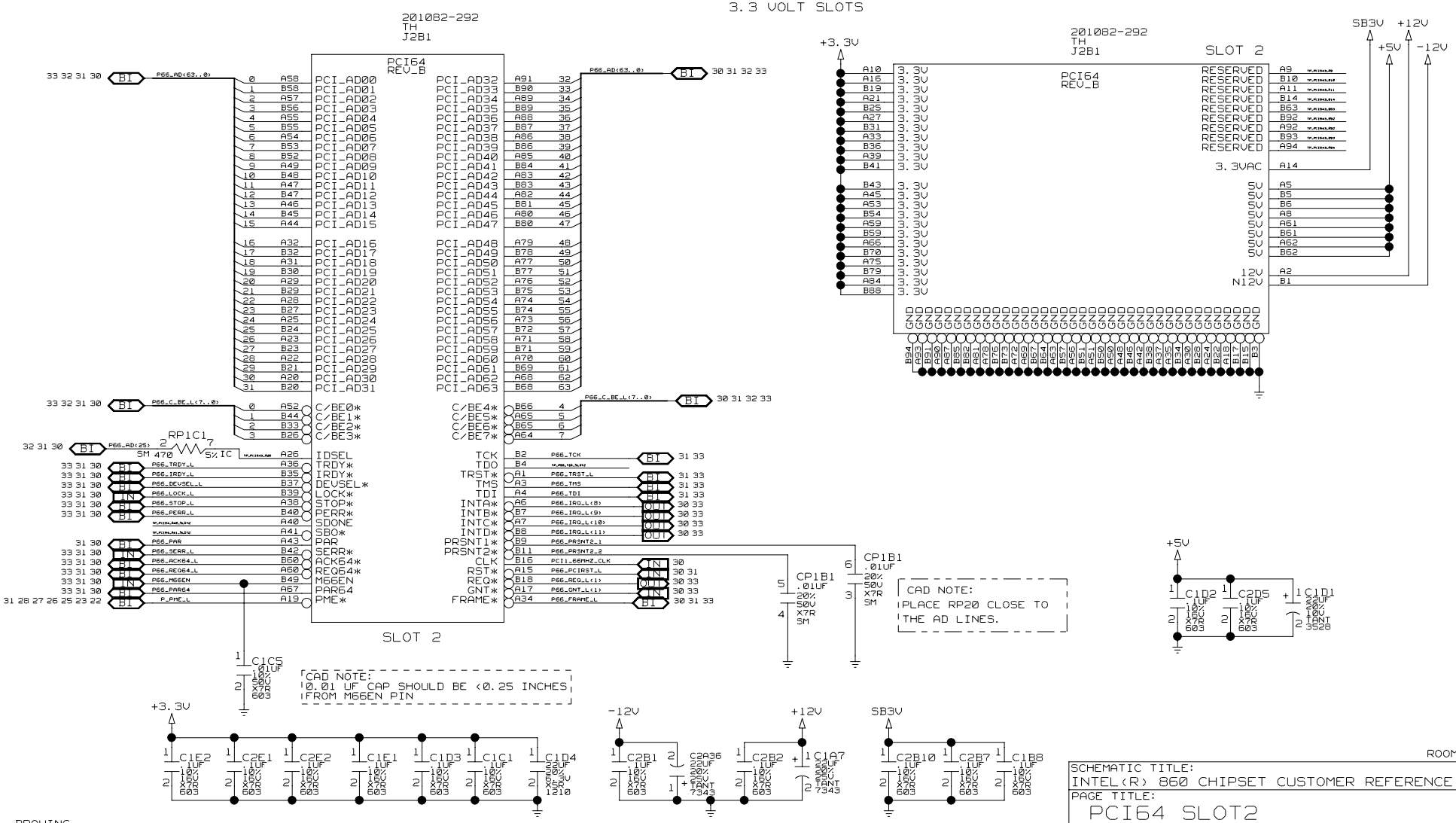
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI64 SLOT1	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:15 2001
	SHEET: 31

THIS CONN IS FOURTH FROM ICH2

PCI64 CONN21, DEVICE 9 (9H), IDSEL P66_AD(25), PCI1_66MHZ_CLK, REQ(1)

PCI64 SLOT 2

3.3 VOLT SLOTS

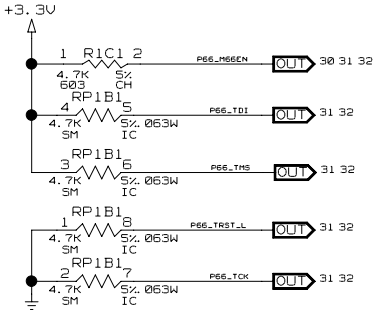


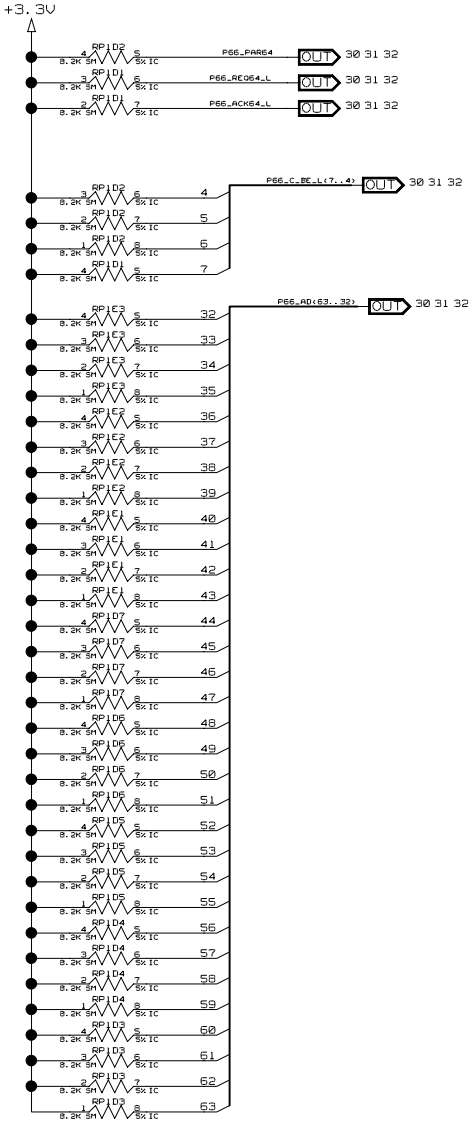
DRAWING

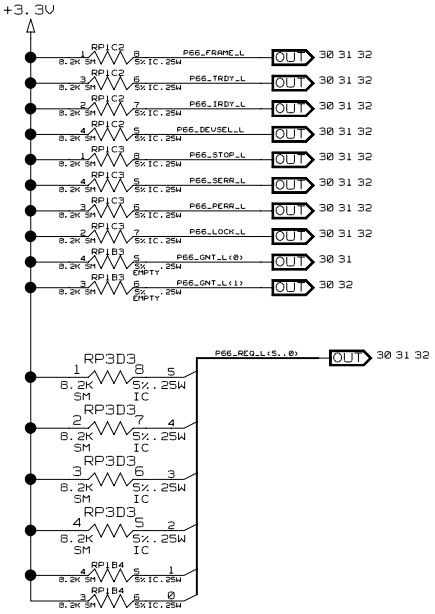
PCI64 SLOT2

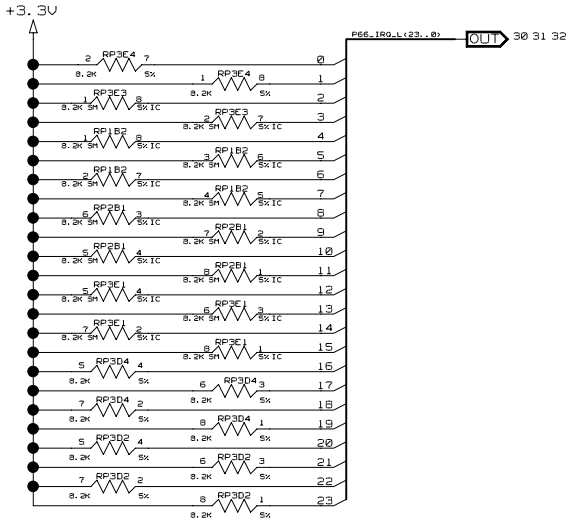
ROOM=PCI66_2

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI64 SLOT2		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:11 2001	SHEET: 32







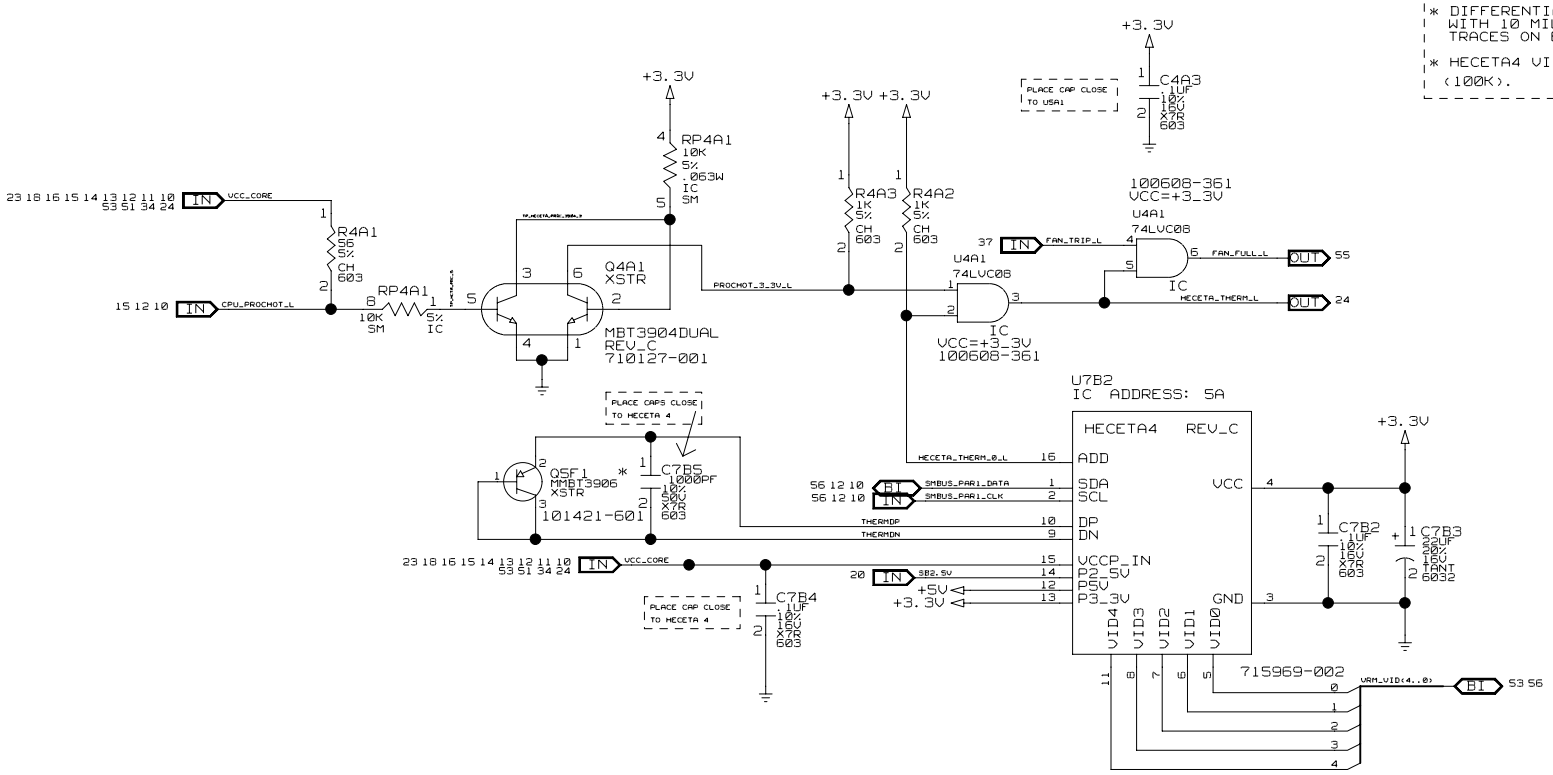


DRAWING

PCI66 TERMINATION

ROOM=PCI66_TERM

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI66 TERMINATION		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:06 2001	SHEET: 33

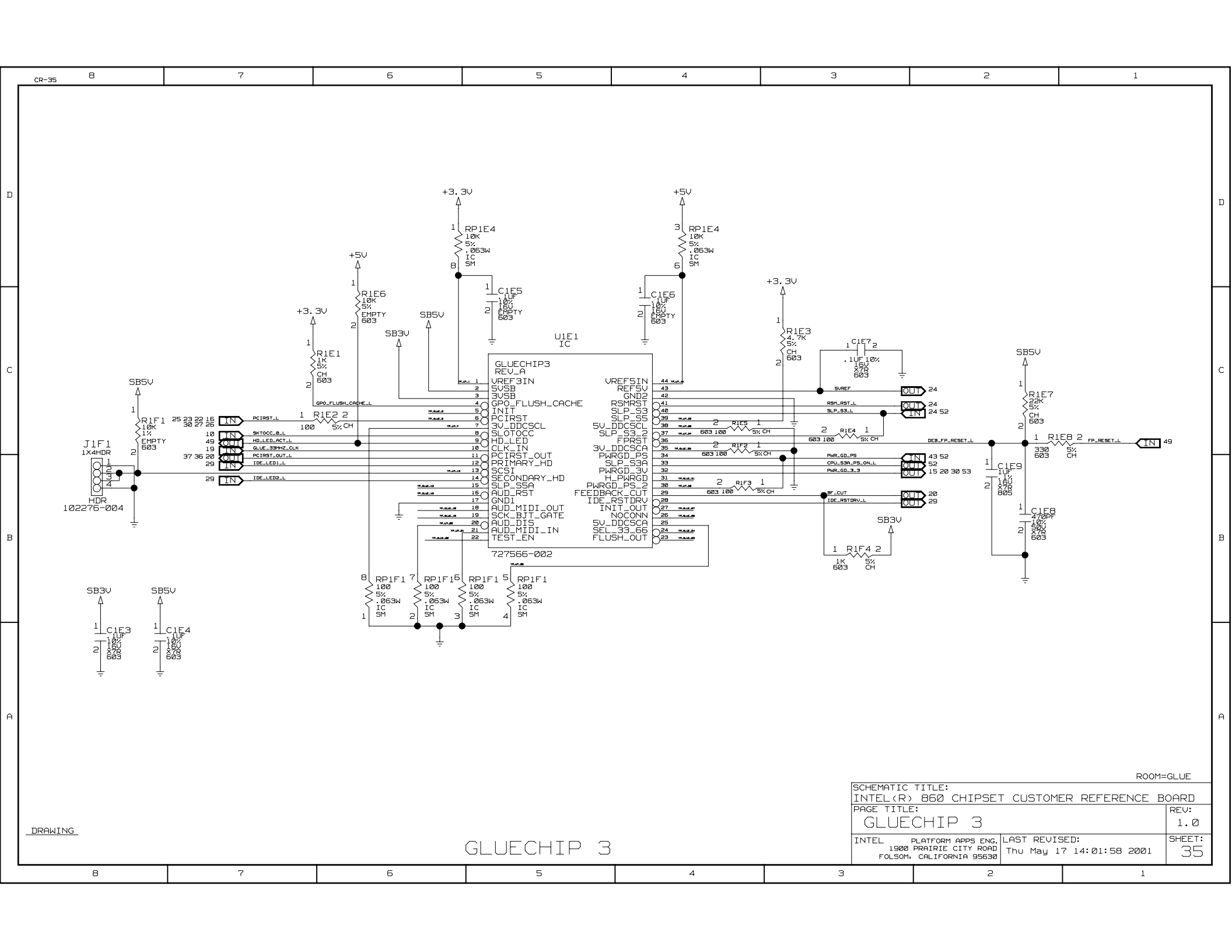


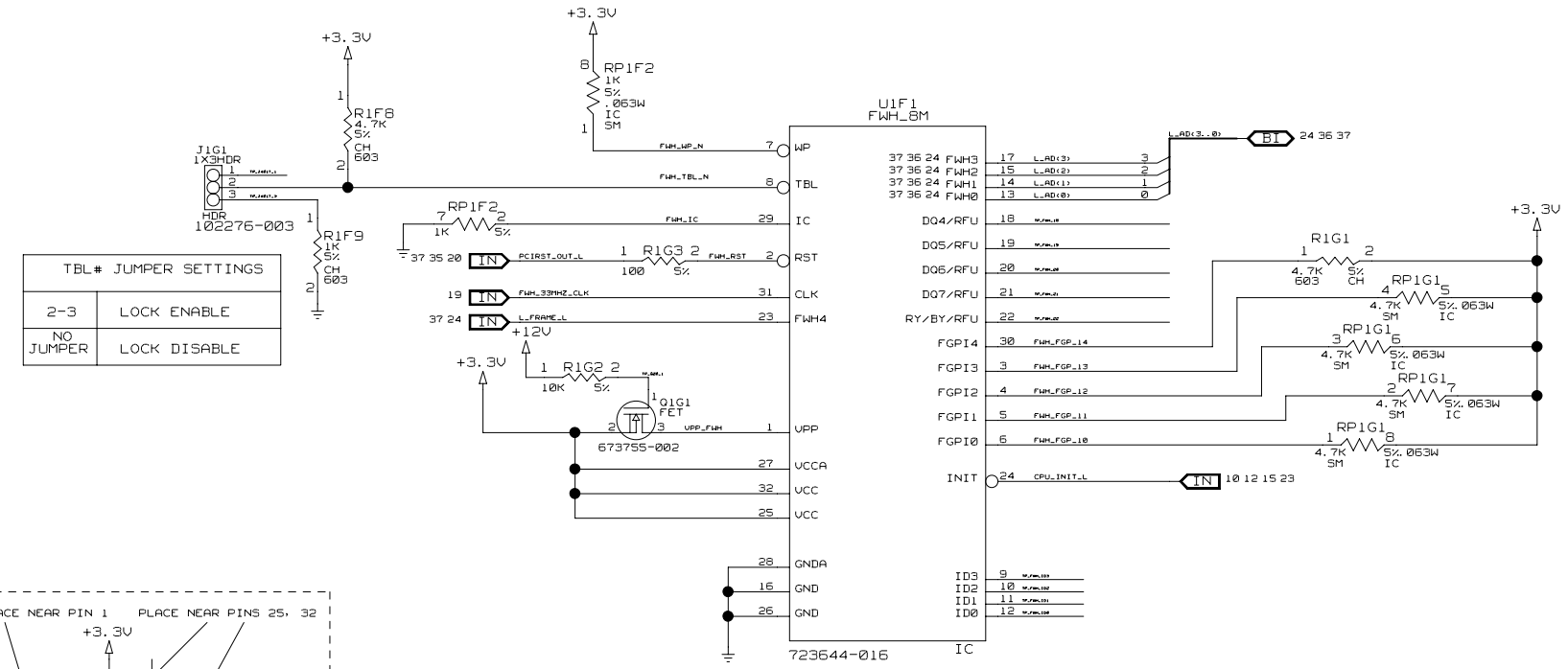
ROOM=HECETA

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: HECETA 4	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:02:02 2001
	SHEET: 34

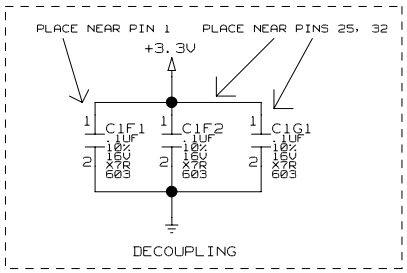
DRAWING

HECETA 4


CR-35
GLUECHIP3
REV_A
U1E1
IC
727566-002
VREF3IN
5VSB
3VSB
GPO_FLUSH_CACHE
INIT
PCIRST
3V_DDCSCL
SLOTOCC
HD_LED
CLK_IN
PCIRST_OUT
PRIMARY_HD
SCSI
SECONDARY_HD
SLP_S5A
AUD_RST
GND1
AUD_MIDI_OUT
SCK_BJT_GATE
AUD_DIS
AUD_MIDI_IN
TEST_EN
VREF5IN
REF5V
GND2
RSMRST
SLP_S3
SLP_S5
5V_DDCSCL
SLP_S3_2
FPRST
3V_DDCSCA
PWRGD_PS
SLP_S3A
PWRGD_3V
H_PWRGD
PWRGD_PS_2
FEEDBACK_CUT
IDE_RSTDRV
INIT_OUT
NOCONN
5V_DDCSCA
SEL_33_66
FLUSH_OUT
J1F1
1X4HDR
HDR
102276-004
+3.3V
+5V
SB5V
SB3V
DRAWING
GLUECHIP 3
ROOM=GLUE
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
GLUECHIP 3
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:01:58 2001
SHEET:
35



TBL# JUMPER SETTINGS	
2-3	LOCK ENABLE
NO JUMPER	LOCK DISABLE



NEED SPACE FOR SOCKET 201138-032

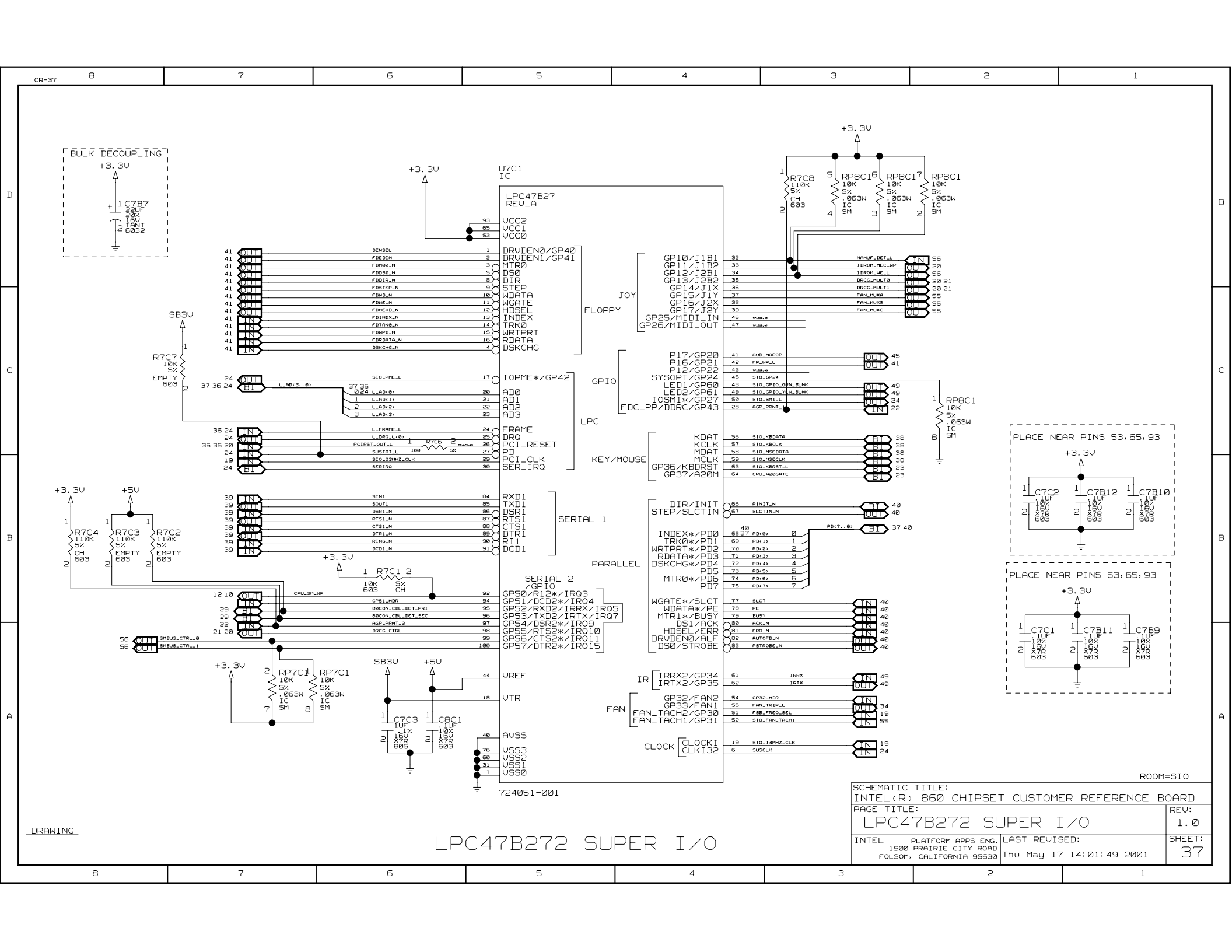
CAD/DESIGN NOTE: ALL PINS MUST HAVE TP'S TO SUPPORT FLASH PROGRAMMING

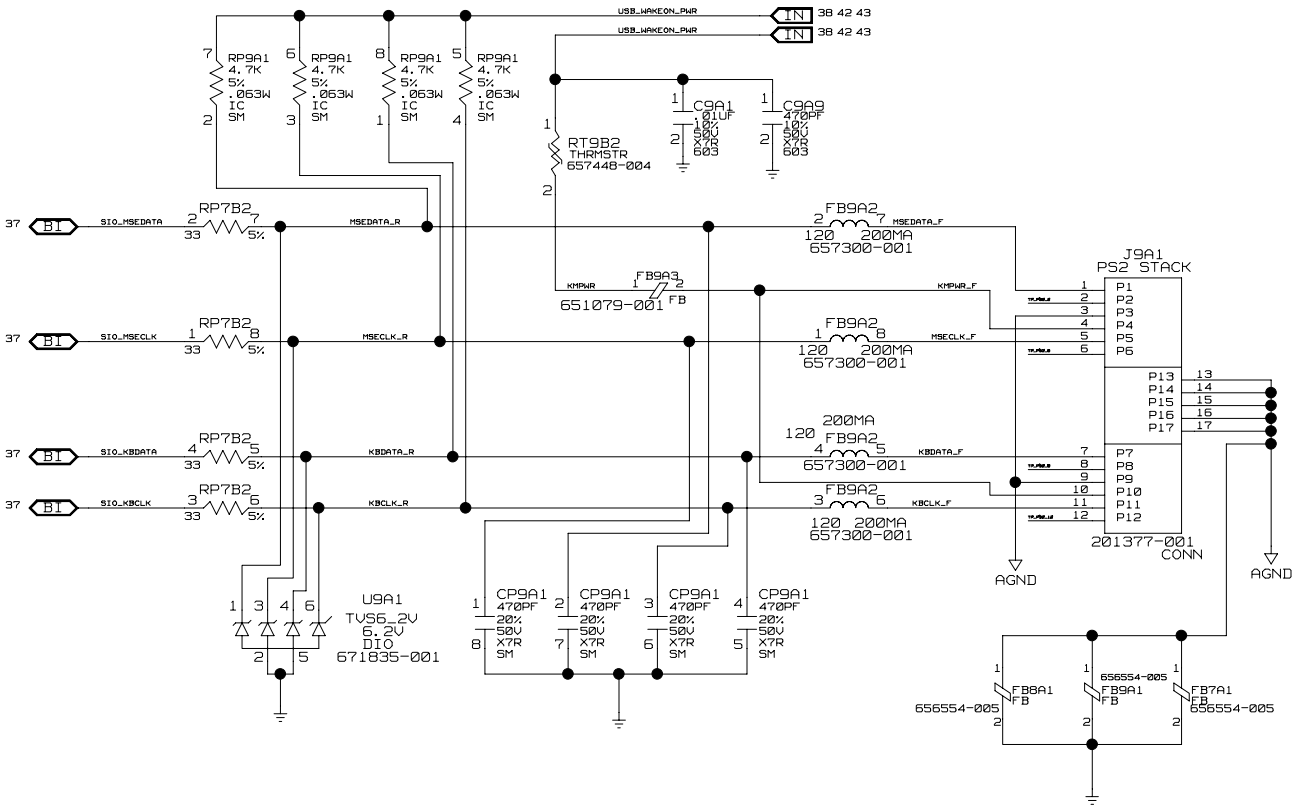
DRAWING

FIRMWARE HUB

ROOM=FWH

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: FIRMWARE HUB		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:53 2001	SHEET: 36


BULK DECOUPLING
+3.3V
C7B7
22UF
20%
16V
TANT
6032
U7C1
IC
LPC47B27
REV_A
VCC2
VCC1
VCC0
DRVDEN0/GP40
DRVDEN1/GP41
MTR0
DS0
DIR
STEP
WDATA
WGATE
HDSEL
INDEX
TRK0
WRTPRT
RDATA
DSKCHG
FLOPPY
IOPME*/GP42
AD0
AD1
AD2
AD3
LPC
FRAME
DRQ
PCI_RESET
PD
PCI_CLK
SER_IRQ
RXD1
TXD1
DSR1
RTS1
CTS1
DTR1
RI1
DCD1
SERIAL 1
SERIAL 2
/GPIO
GP50/R12*/IRQ3
GP51/DCD2*/IRQ4
GP52/RXD2/IRRX/IRQ5
GP53/TXD2/IRTX/IRQ7
GP54/DSR2*/IRQ9
GP55/RTS2*/IRQ10
GP56/CTS2*/IRQ11
GP57/DTR2*/IRQ15
VREF
VTR
AVSS
VSS3
VSS2
VSS1
VSS0
724051-001
GP10/J1B1
GP11/J1B2
GP12/J2B1
GP13/J2B2
GP14/J1X
GP15/J1Y
GP16/J2X
GP17/J2Y
GP25/MIDI_IN
GP26/MIDI_OUT
JOY
P17/GP20
P16/GP21
P12/GP22
SYSOPT/GP24
LED1/GP60
LED2/GP61
IOSMI*/GP27
FDC_PP/DDRC/GP43
GPIO
KDAT
KCLK
MDAT
MCLK
GP36/KBDRST
GP37/A20M
KEY/MOUSE
DIR/INIT
STEP/SLCTIN
INDEX*/PD0
TRK0*/PD1
WRTPRT*/PD2
RDATA*/PD3
DSKCHG*/PD4
PD5
MTR0*/PD6
PD7
WGATE*/SLCT
WDATA*/PE
MTR1*/BUSY
DS1/ACK
HDSEL/ERR
DRVDEN0/ALF
DS0/STROBE
PARALLEL
IRRX2/GP34
IRTX2/GP35
IR
GP32/FAN2
GP33/FAN1
FAN_TACH2/GP30
FAN_TACH1/GP31
FAN
CLOCKI
CLKI32
CLOCK
R7C8
110K
5%
CH
603
RP8C1
10K
5%
.063W
IC
SM
R7C7
10K
5%
EMPTY
603
SB3V
+5V
R7C4
110K
5%
CH
603
R7C3
110K
5%
EMPTY
603
R7C2
110K
5%
EMPTY
603
R7C1
10K
5%
CH
603
RP7C1
10K
5%
.063W
IC
SM
C7C3
1UF
10%
16V
X7R
805
C8C1
1UF
10%
16V
X7R
603
PLACE NEAR PINS 53,65,93
C7C2
C7B12
C7B10
C7C1
C7B11
C7B9
1UF
10%
16V
X7R
603
ROOM=SIO
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
LPC47B272 SUPER I/O
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:01:49 2001
SHEET:
37
DRAWING
LPC47B272 SUPER I/O

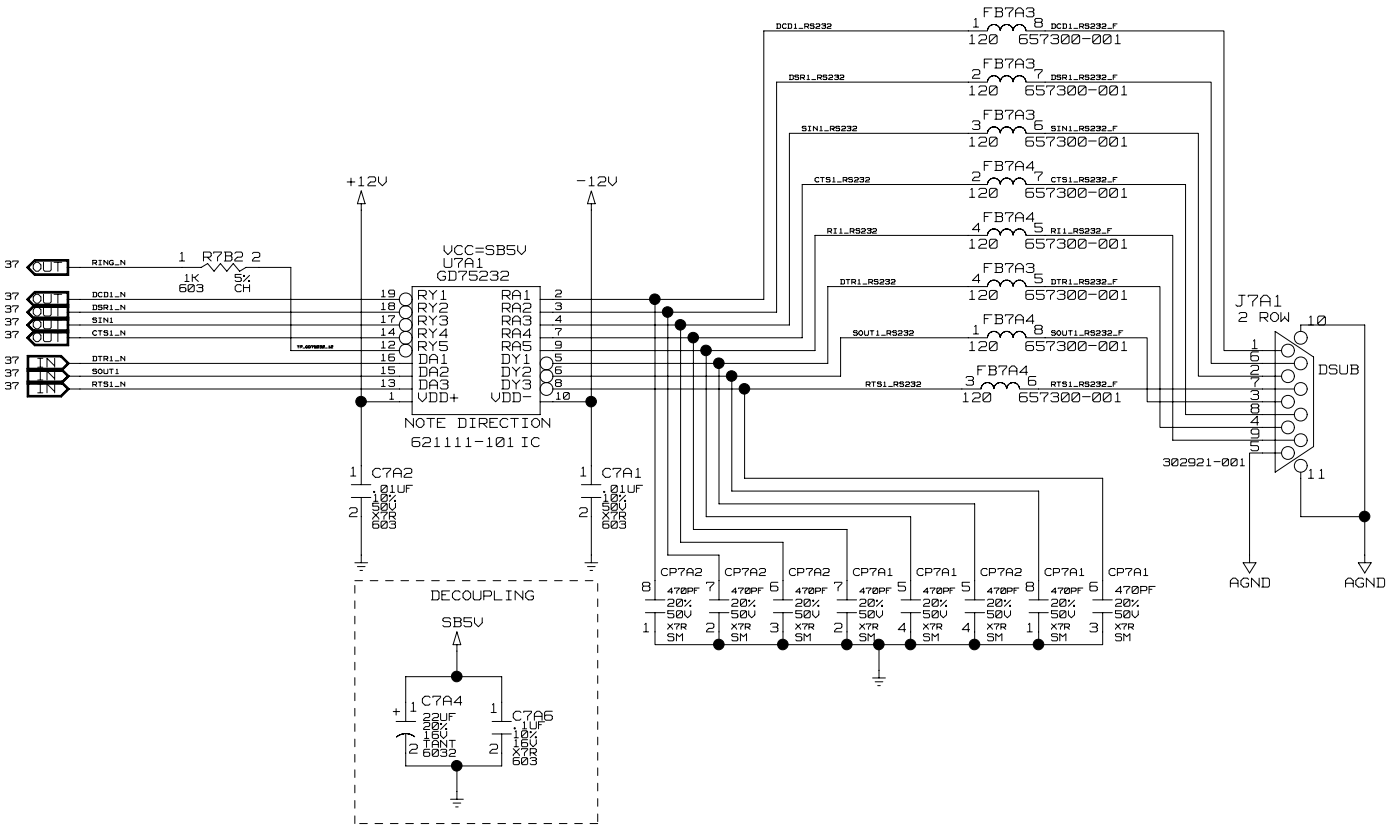


DRAWING

PS2 KEYBOARD AND MOUSE

ROOM=PS2_MOUSE

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PS2 KEYBOARD AND MOUSE	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:45 2001
	SHEET: 38

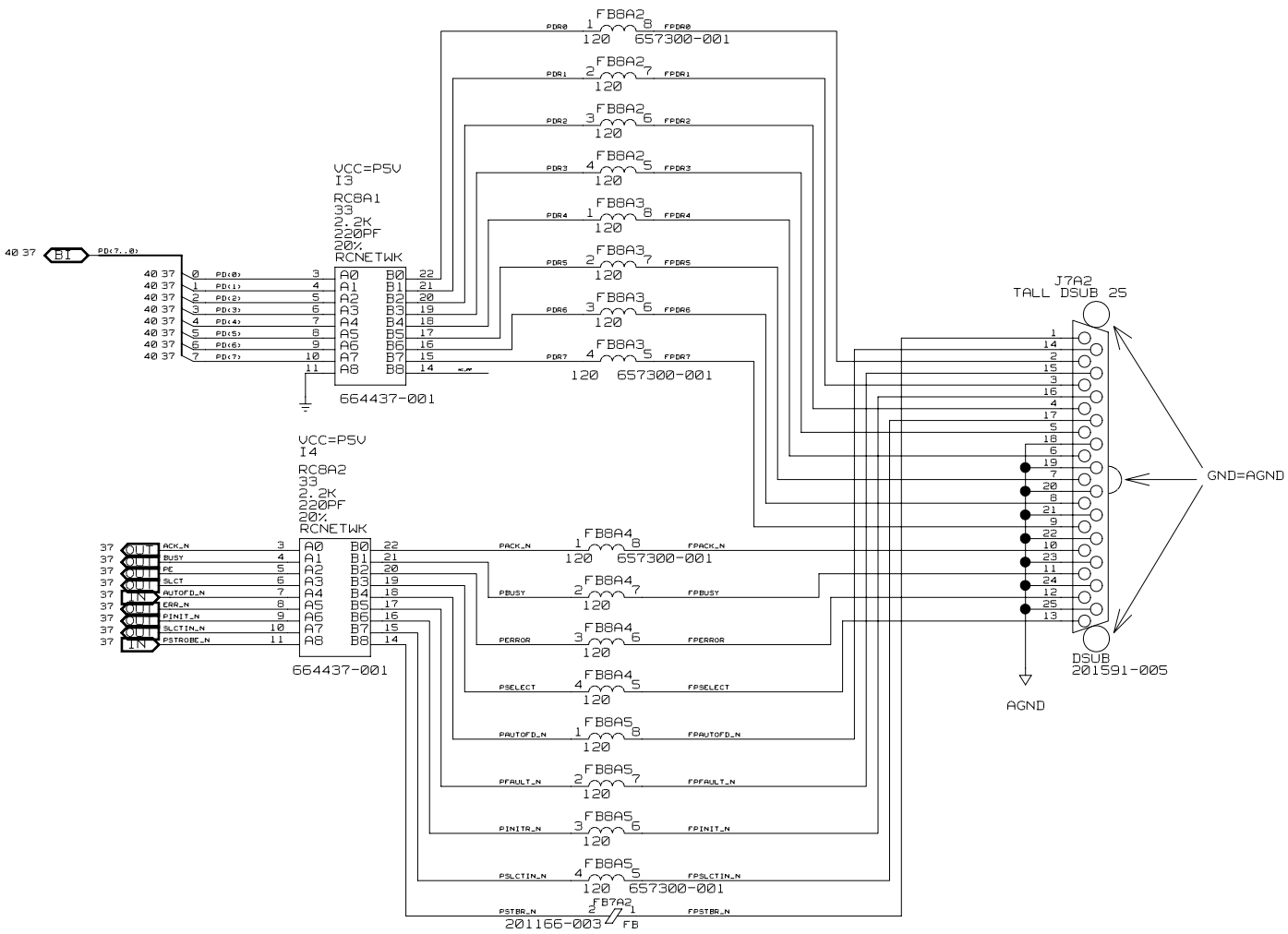


SERIAL PORT

DRAWING

ROOM=SERIAL

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: SERIAL PORT	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:41 2001
	SHEET: 39

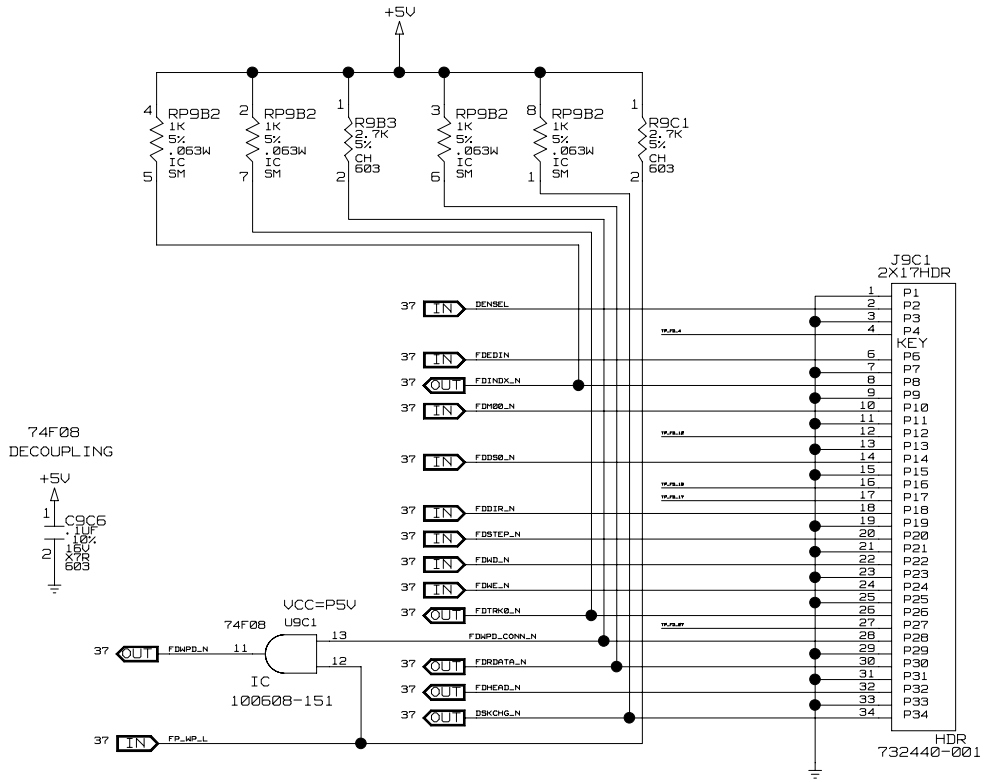


DRAWING

PARALLEL PORT

ROOM=PARALLEL

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: PARALLEL PORT	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:37 2001
	SHEET: 40

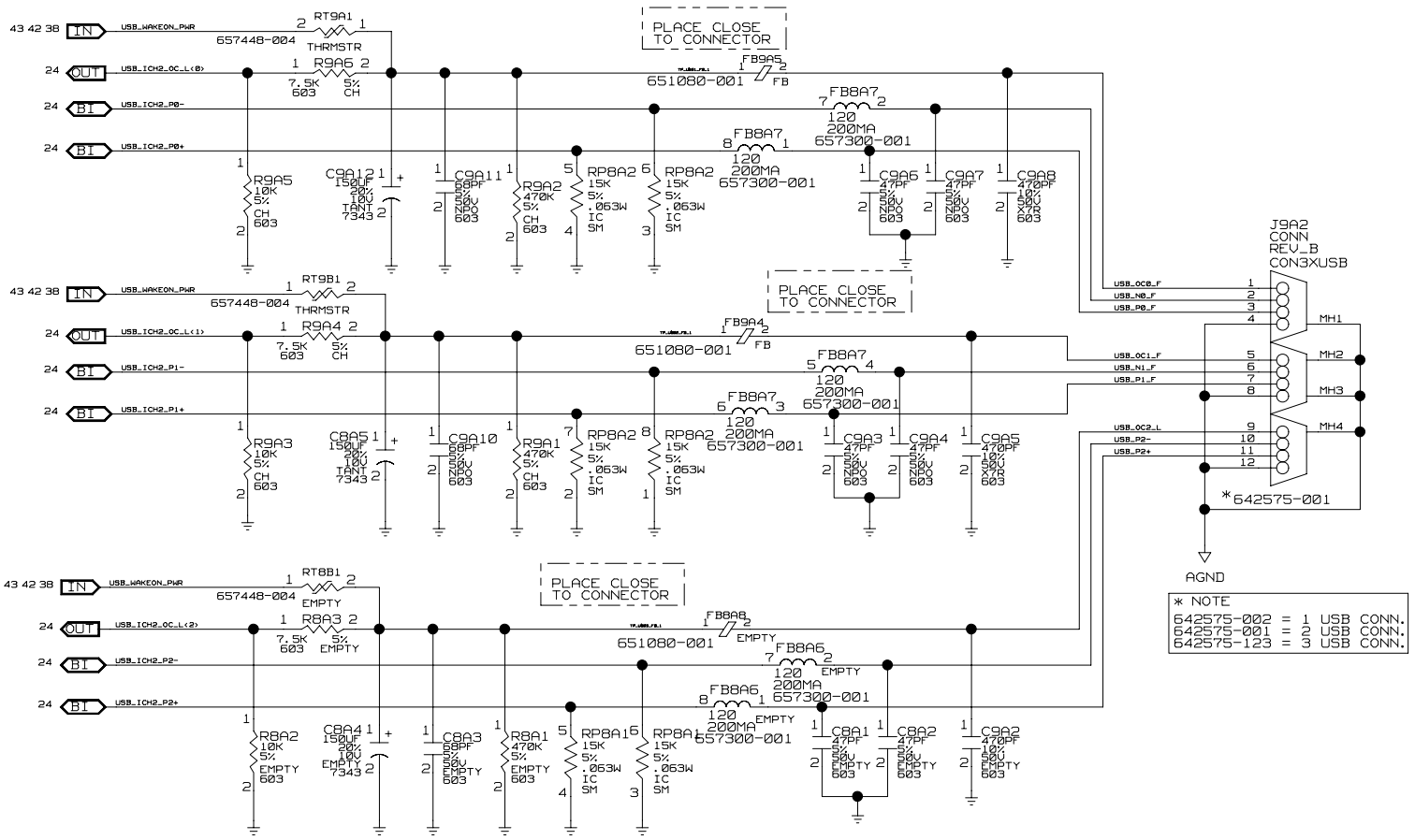


DRAWING

FLOPPY DRIVE PORT

ROOM=FLOPPY

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: FLOPPY DRIVE PORT	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:32 2001
	SHEET: 41



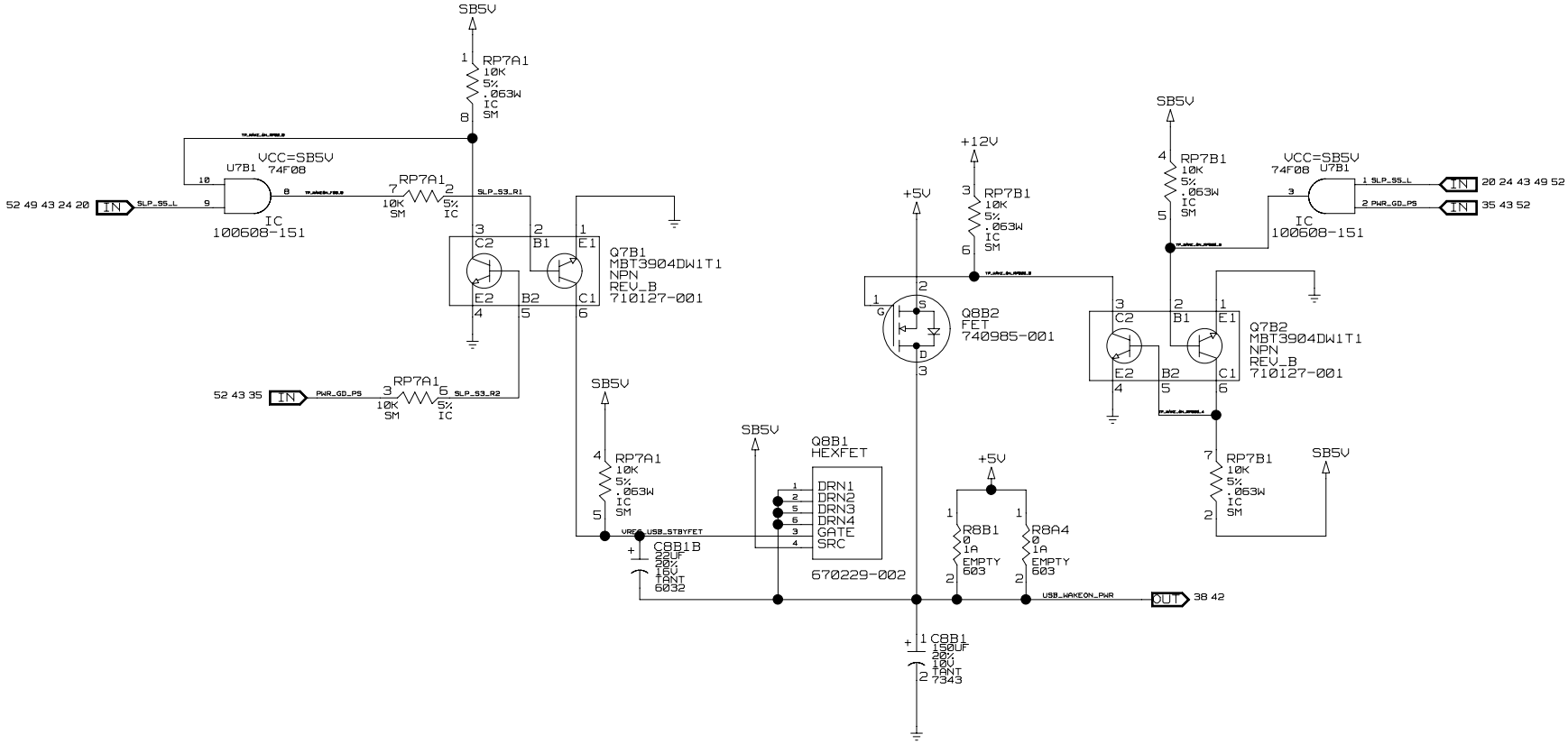
* NOTE
642575-002 = 1 USB CONN.
642575-001 = 2 USB CONN.
642575-123 = 3 USB CONN.

ROOM=USB

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: USB CONNECTORS	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:25 2001
	SHEET: 42

DRAWING

USB CONNECTORS

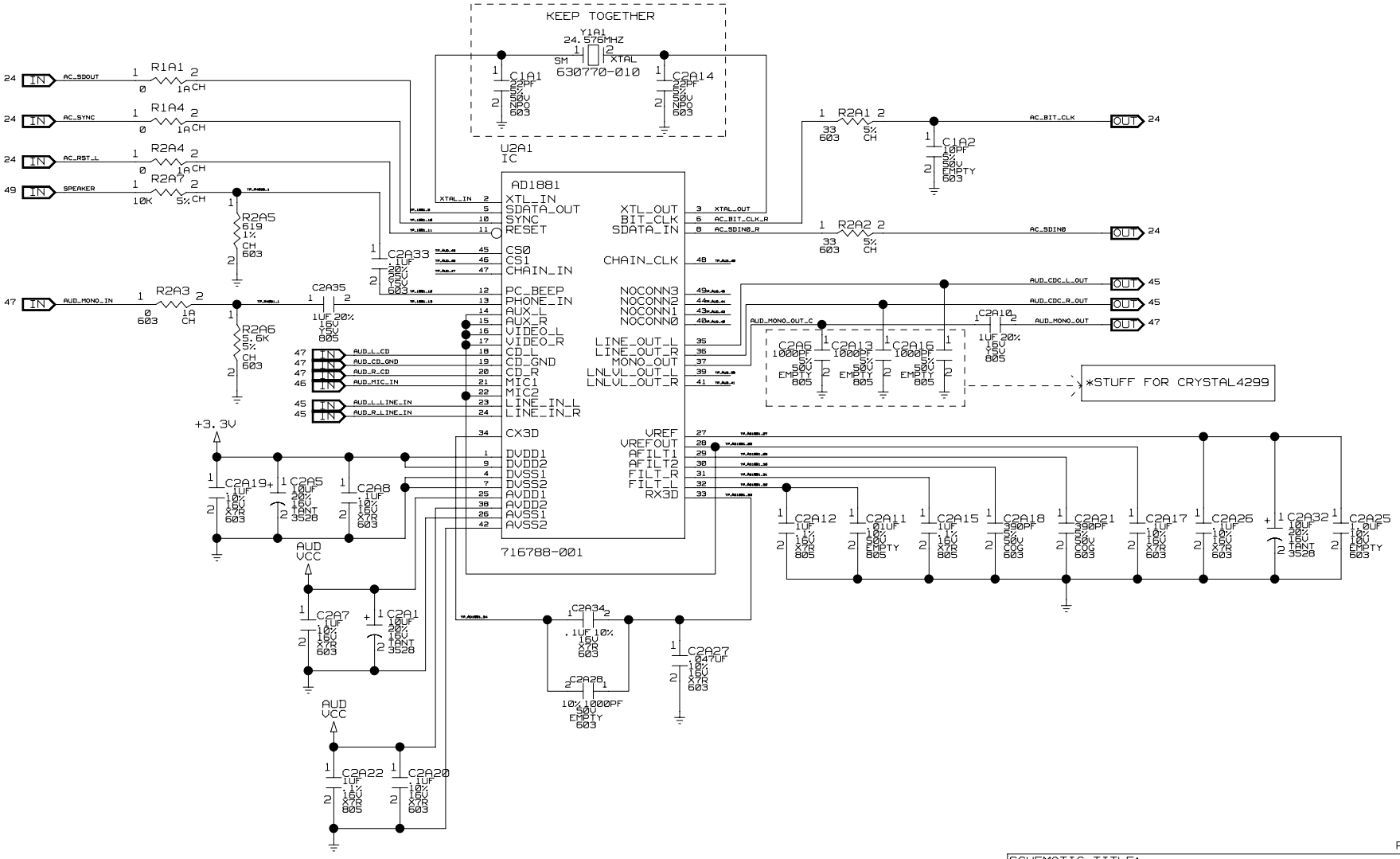


ROOM=USB_WAKE

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: WAKE ON USB	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:21 2001
	SHEET: 43

DRAWING

WAKE ON USB

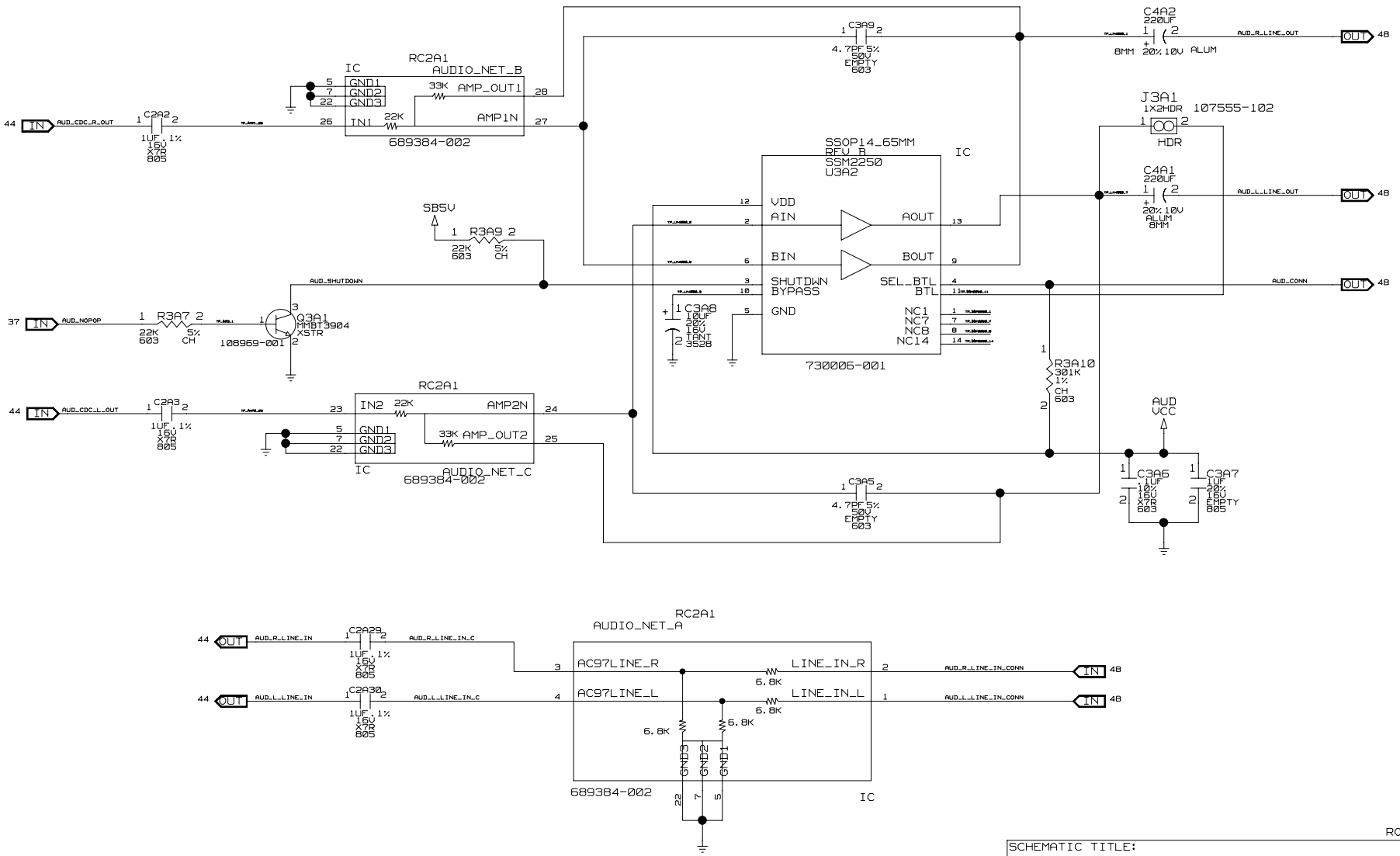


AD1881 AUDIO CODEC

DRAWING

ROOM=AUDIO

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AD1881 AUDIO CODEC	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:18 2001
	SHEET: 44

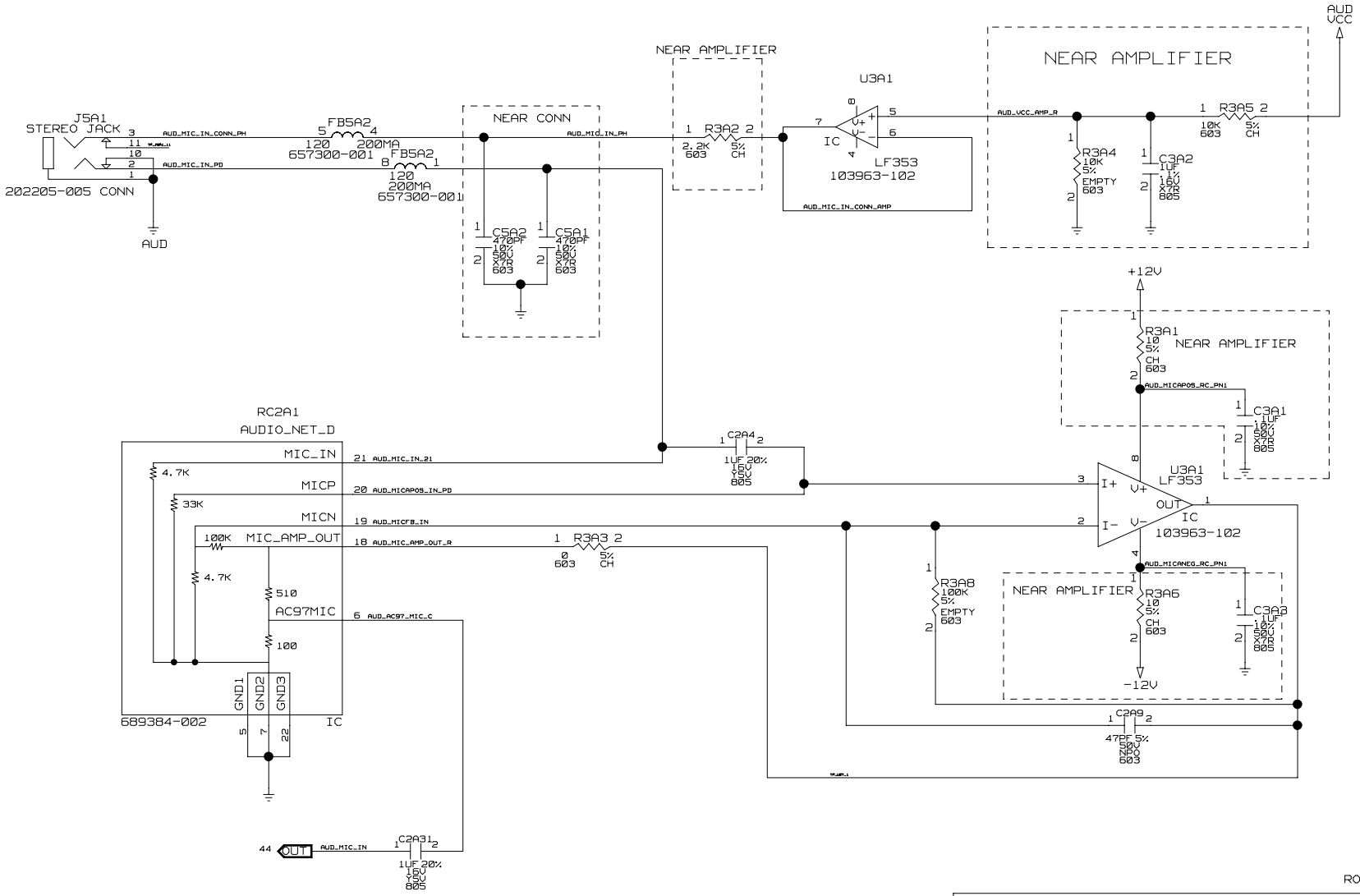


ROOM=AUDIO

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: LINE IN / OUT		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:12 2001	SHEET: 45

DRAWING

LINE IN / OUT

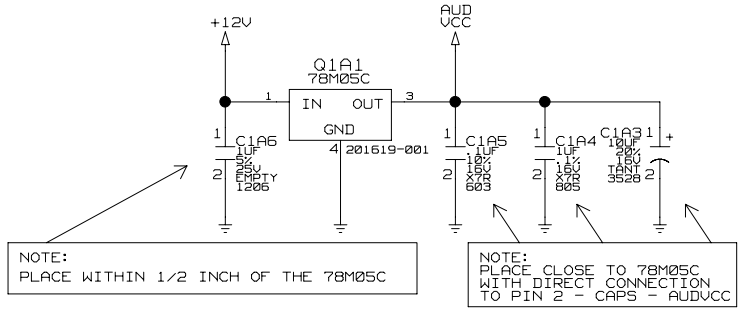


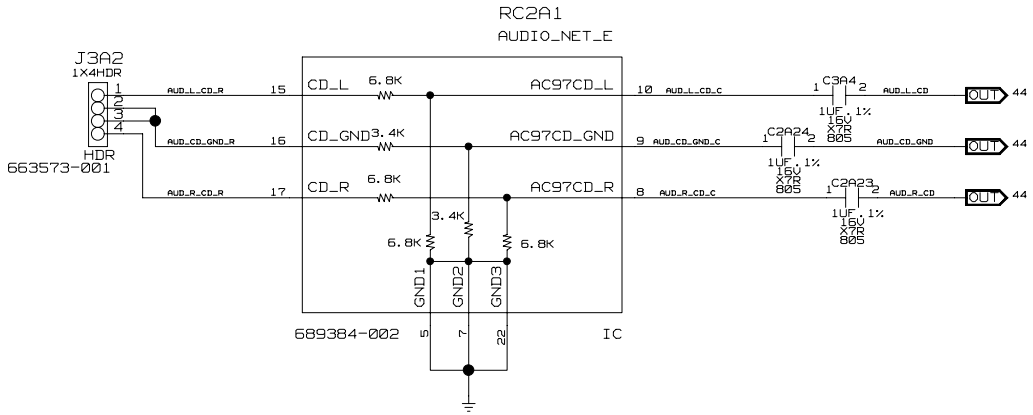
ROOM=AUDIO

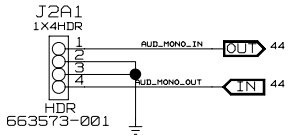
DRAWING

MICROPHONE IN

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: MICROPHONE IN	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:08 2001
	SHEET: 46





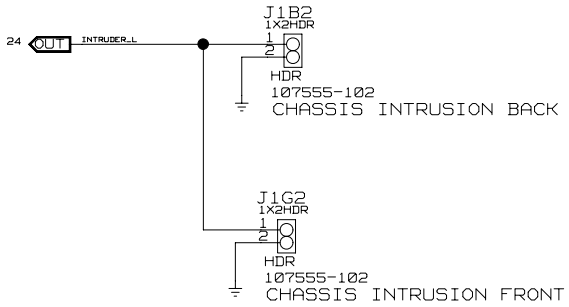


ROOM=AUDIO

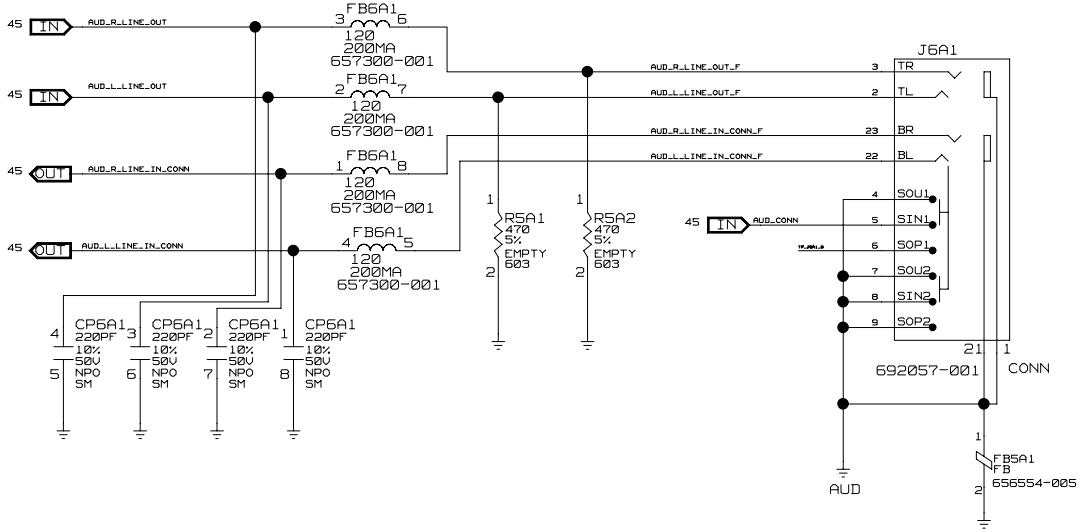
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: AUDIO NET & VREG	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:01:03 2001
	SHEET: 47

DRAWING

AUDIO NET & VREG

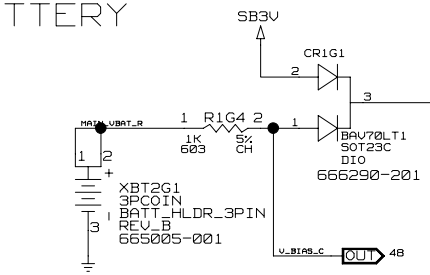


CHASSIS INTRUSION



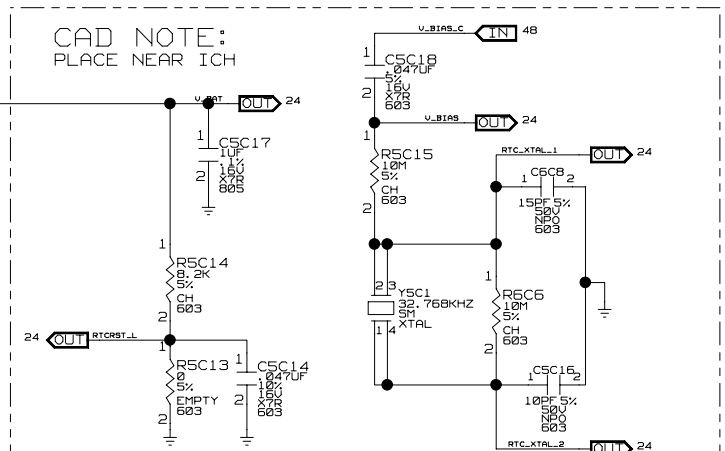
AUDIO CONNECTOR

BATTERY



CAD NOTE: DO NOT PLACE BATTERY NEAR MOUNTING HOLES, GROUND OR VIAS

ROOM=BATTERY



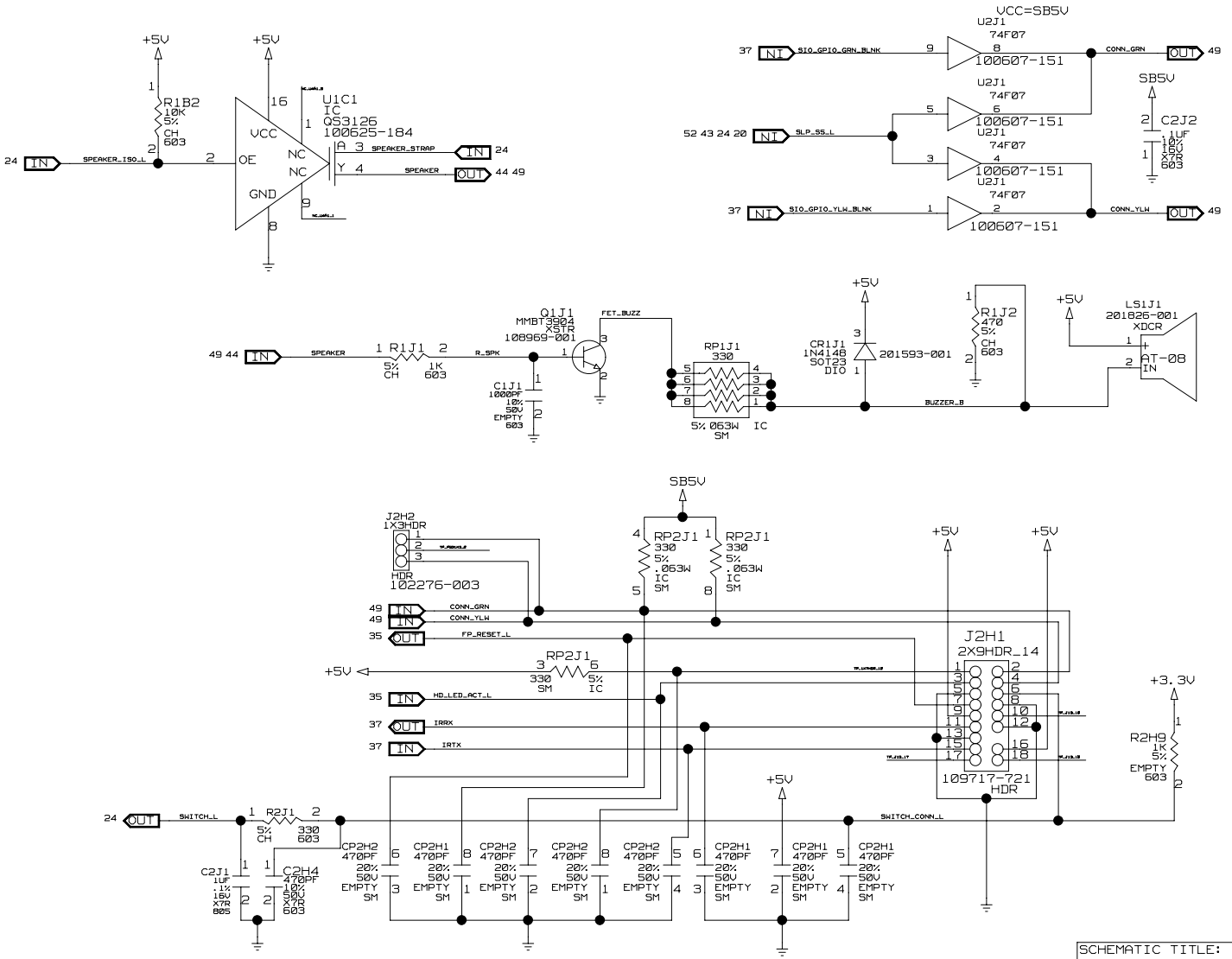
ROOM=STACKED AUDIO

ROOM=INTRUSION

DRAWING

CHASSIS INTRUSION, AUDIO AND BATTERY

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: CHASSIS INTRUSION & AUDIO	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:58 2001
	SHEET: 48



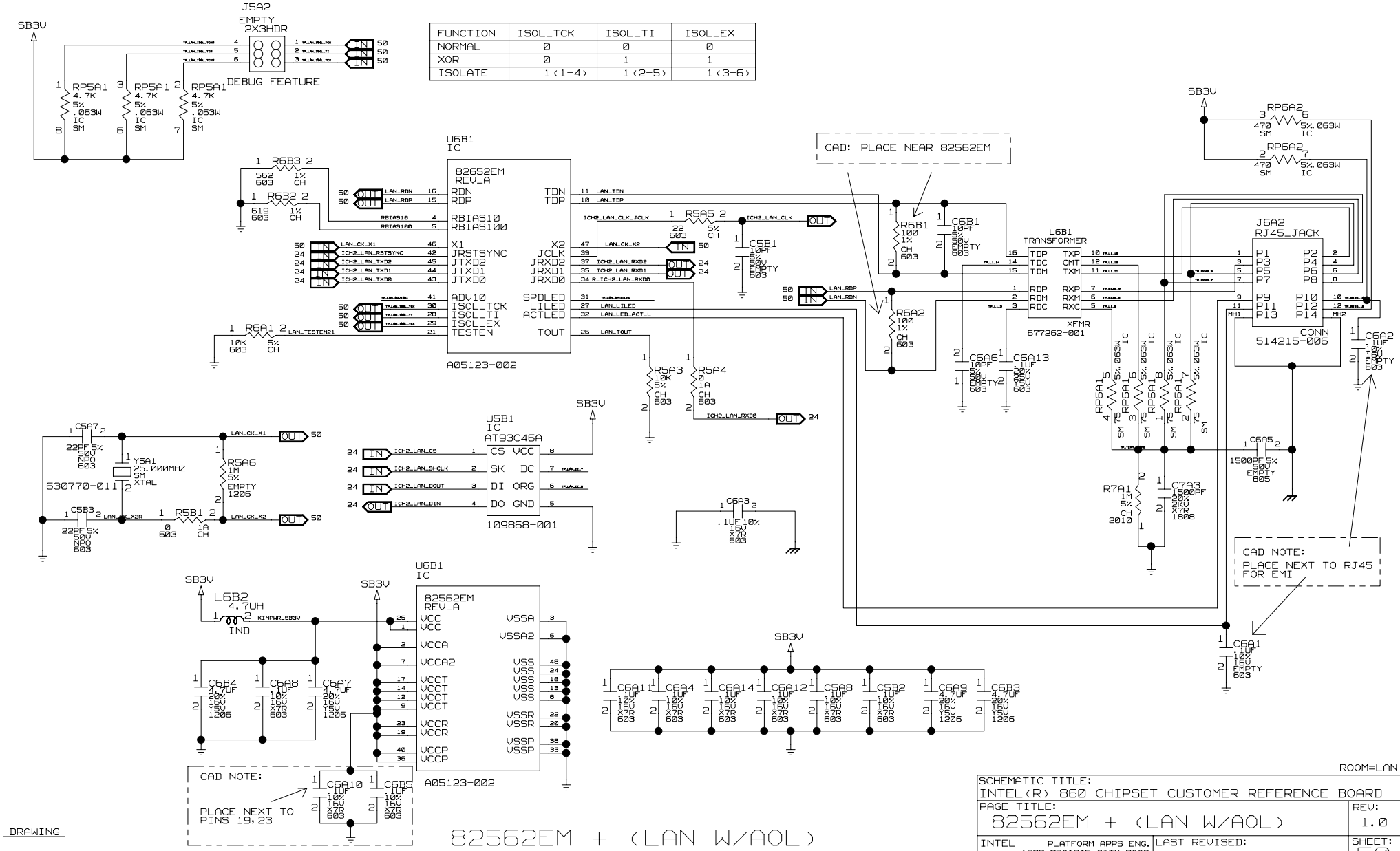
DRAWING

FRONT PANEL HEADERS / SPEAKER

ROOM=FRNT_PNL

ROOM=SPEAKER

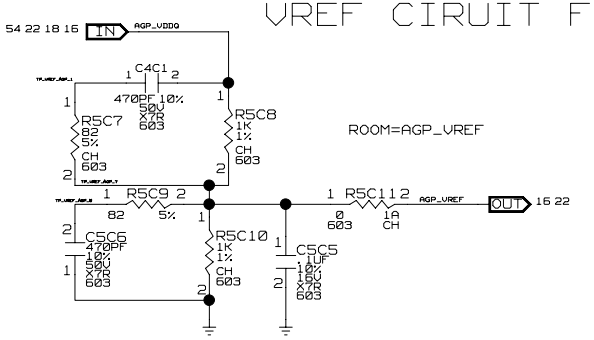
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: FRONT PANEL HEADERS	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:53 2001
	SHEET: 49



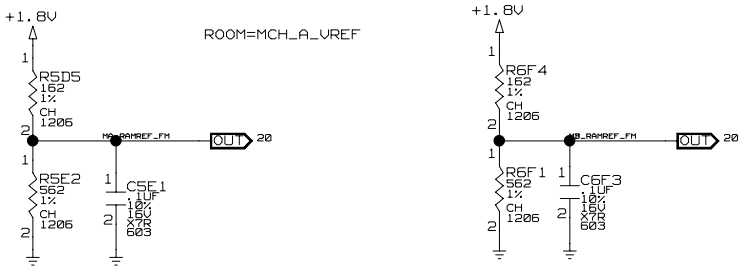
FUNCTION	ISOL_TCK	ISOL_TI	ISOL_EX
NORMAL	0	0	0
XOR	0	1	1
ISOLATE	1(1-4)	1(2-5)	1(3-6)

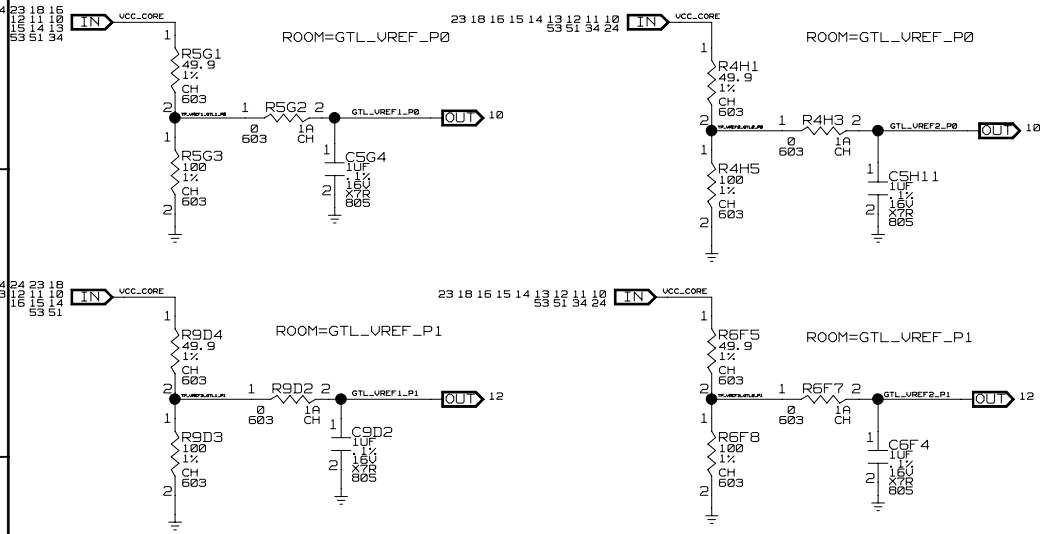
CR-51

VREF CIRUIT FOR AGP 4X



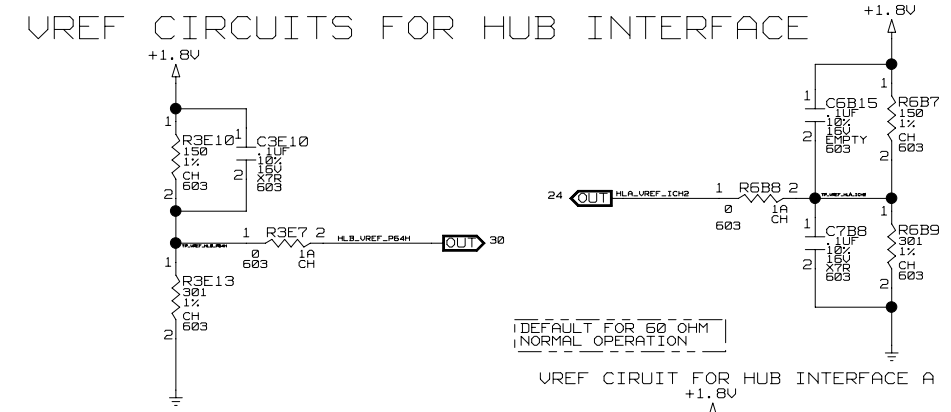
VREF CIRCUITS FOR RAMBUS





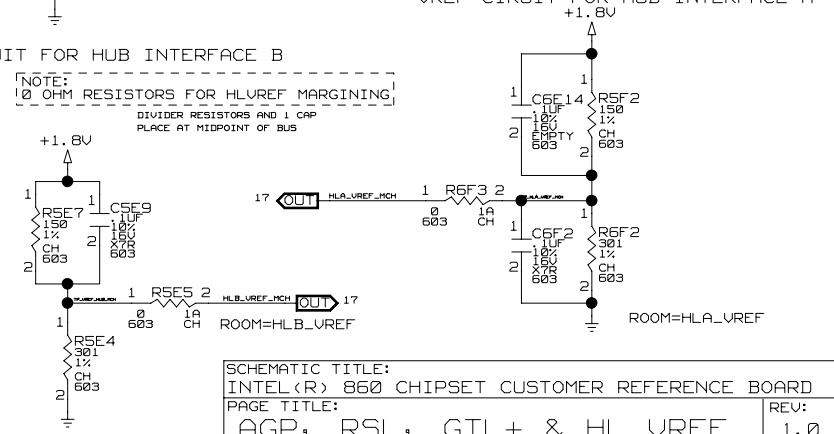
VREF CIRCUIT FOR GTL+

VREF CIRCUITS FOR HUB INTERFACE



VREF CIRUIT FOR HUB INTERFACE A

VREF CIRUIT FOR HUB INTERFACE B



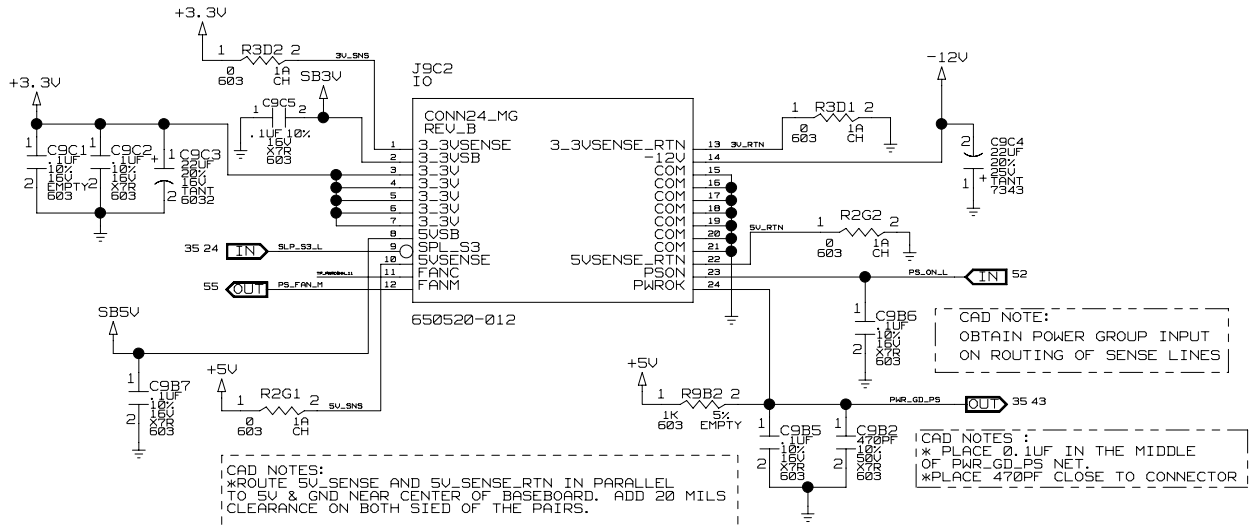
DRAWING

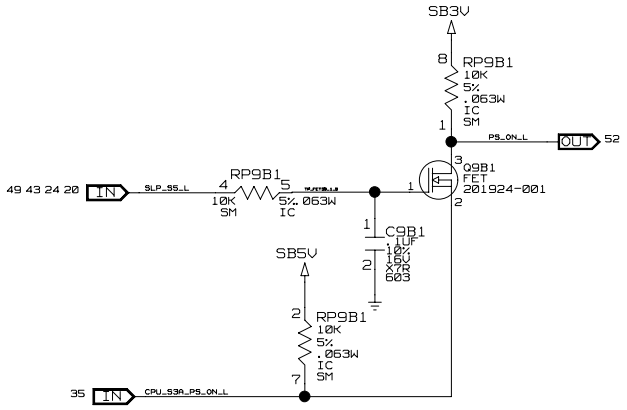
AGP, RSL, GTL+ & HUB LINK VREF CIRCUITS

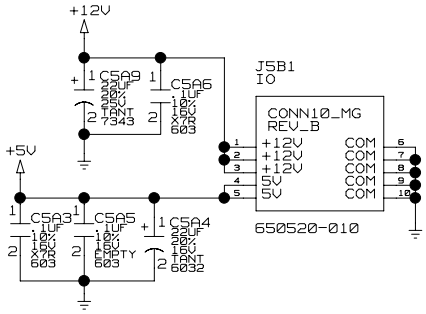
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: AGP, RSL, GTL+ & HL VREF		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:42 2001	SHEET: 51

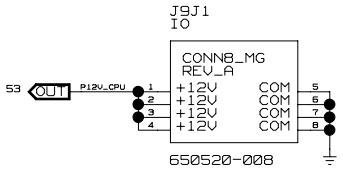
WTX PSU SIGNAL TABLE

PS_ON = 10K PULL UP TO 5VSB INTERNAL TO PSU
FAN_C = 10K PULL UP TO 5V INTERNAL TO PSU
SLEEP = 10 PULL UP TO 3.3V AUX INTERNAL TO PSU
PS_OK = 10K PULLUP TO 5V INTERNAL TO PSU









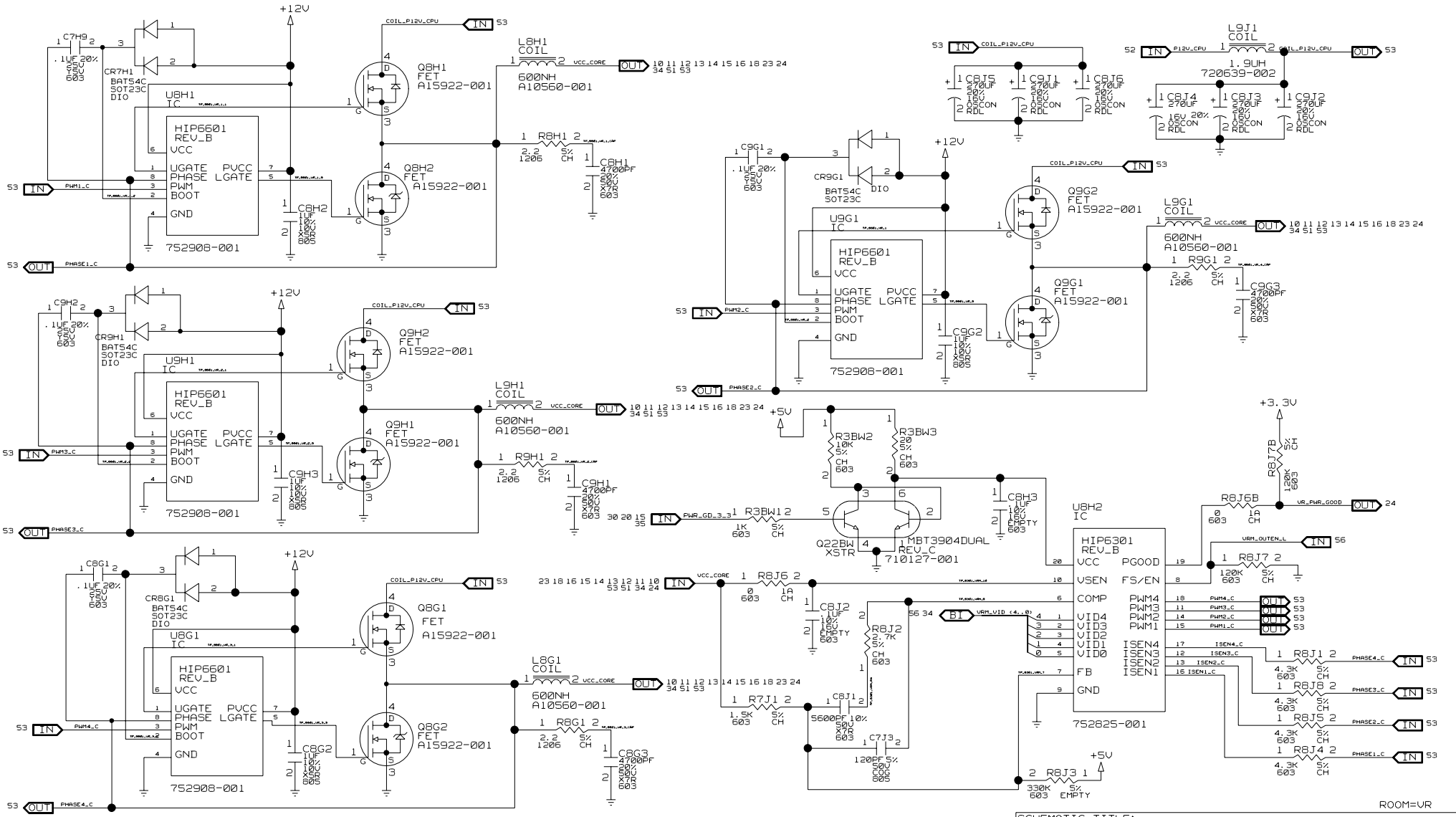
ROOM=POWER_HDR

ROOM=PWRCONN_BASE

DRAWING

POWER SUPPLY CONNECTORS

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: POWER SUPPLY CONNECTORS		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:37 2001	SHEET: 52



NOTE:
HEAT-SINK FOR VR IS IPN 701073-001
HEAT-SINK CLIP IS IPN XXXXXX-XXX

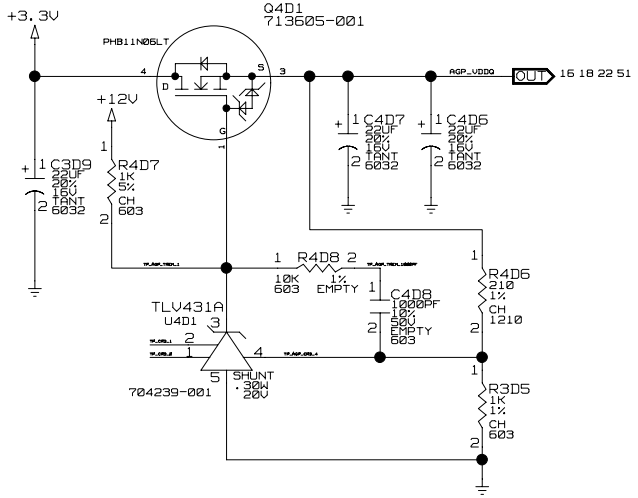
DRAWING

CPU VOLTAGE REGULATORS

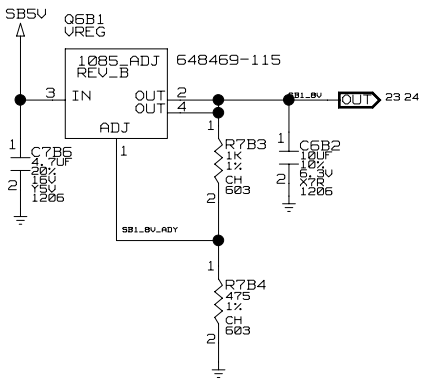
ROOM=VR

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: CPU VOLTAGE REGULATORS	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:31 2001
	SHEET: 53

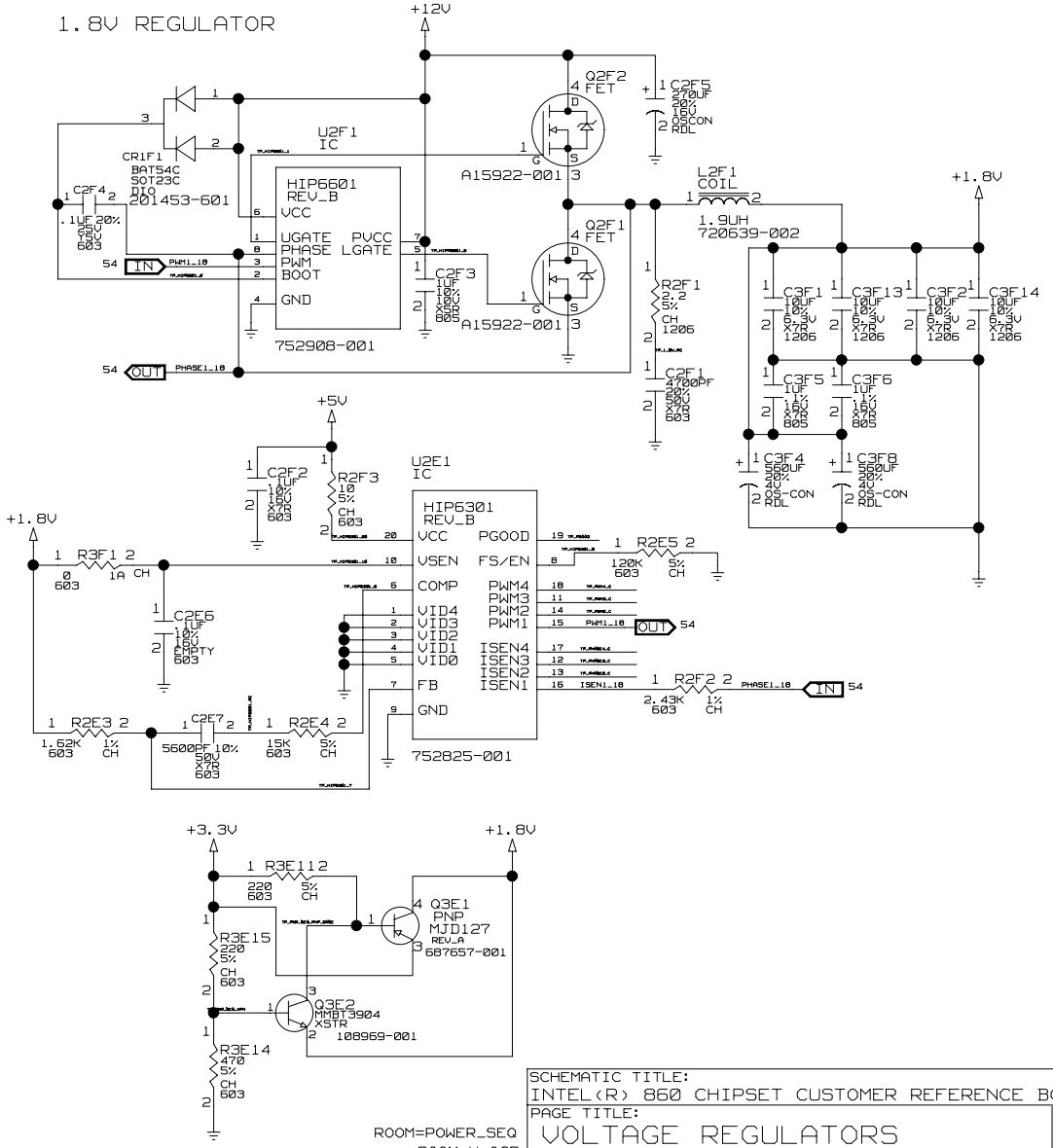
AGP PRO TERMINATION



STANDBY 1.8 V REGULATOR



1.8V REGULATOR



DRAWING

VOLTAGE REGULATORS

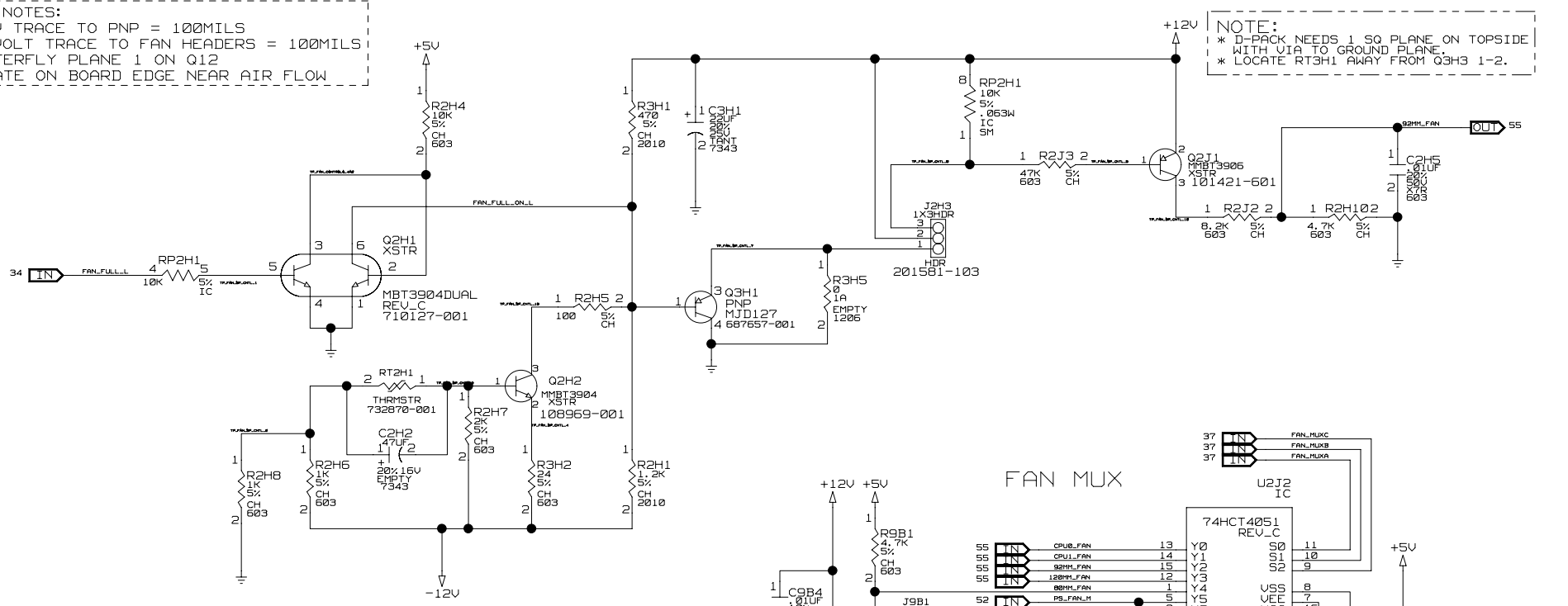
ROOM=POWER_SEQ
ROOM=V_AGP
ROOM=1_8VREG
ROOM=VREG_SB1.8V

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: VOLTAGE REGULATORS	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:25 2001
	SHEET: 54

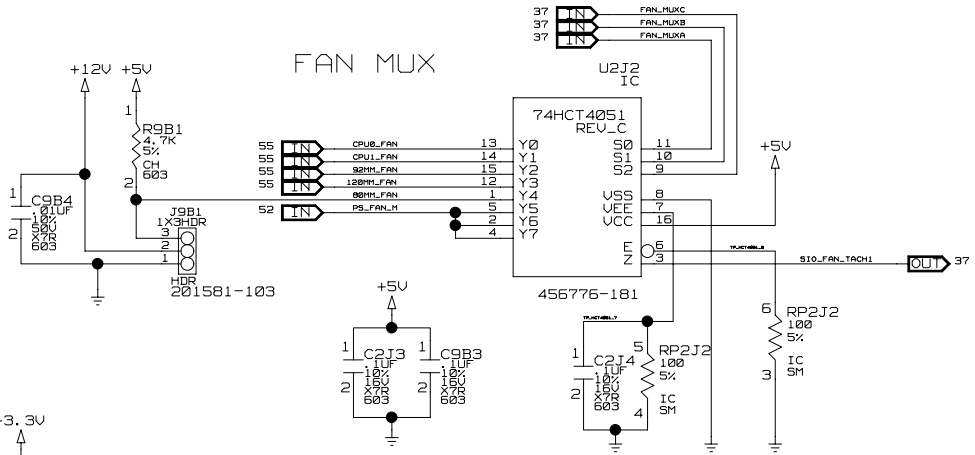
CR-55

CAD NOTES:
+12V TRACE TO PNP = 100MILS
12 VOLT TRACE TO FAN HEADERS = 100MILS
BUTTERFLY PLANE 1 ON Q12
LOCATE ON BOARD EDGE NEAR AIR FLOW

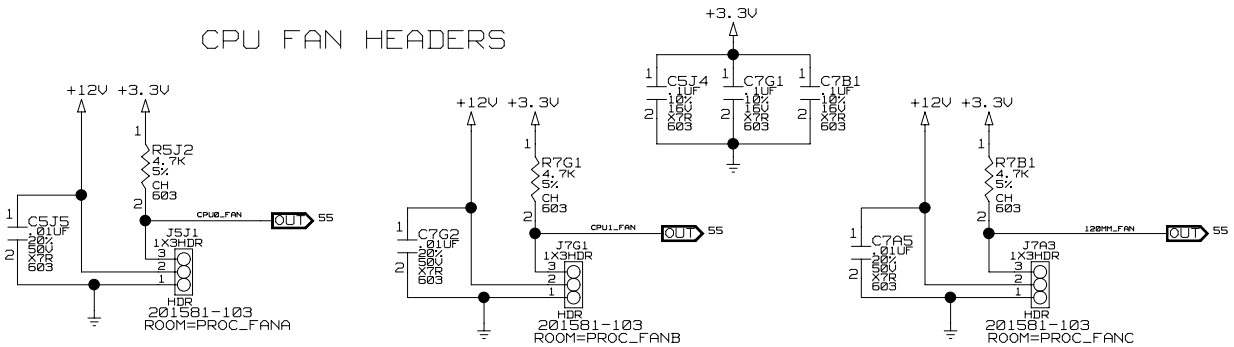
NOTE:
* D-PACK NEEDS 1 SQ PLANE ON TOPSIDE WITH VIA TO GROUND PLANE.
* LOCATE RT3H1 AWAY FROM Q3H3 1-2.



FAN MUX



CPU FAN HEADERS

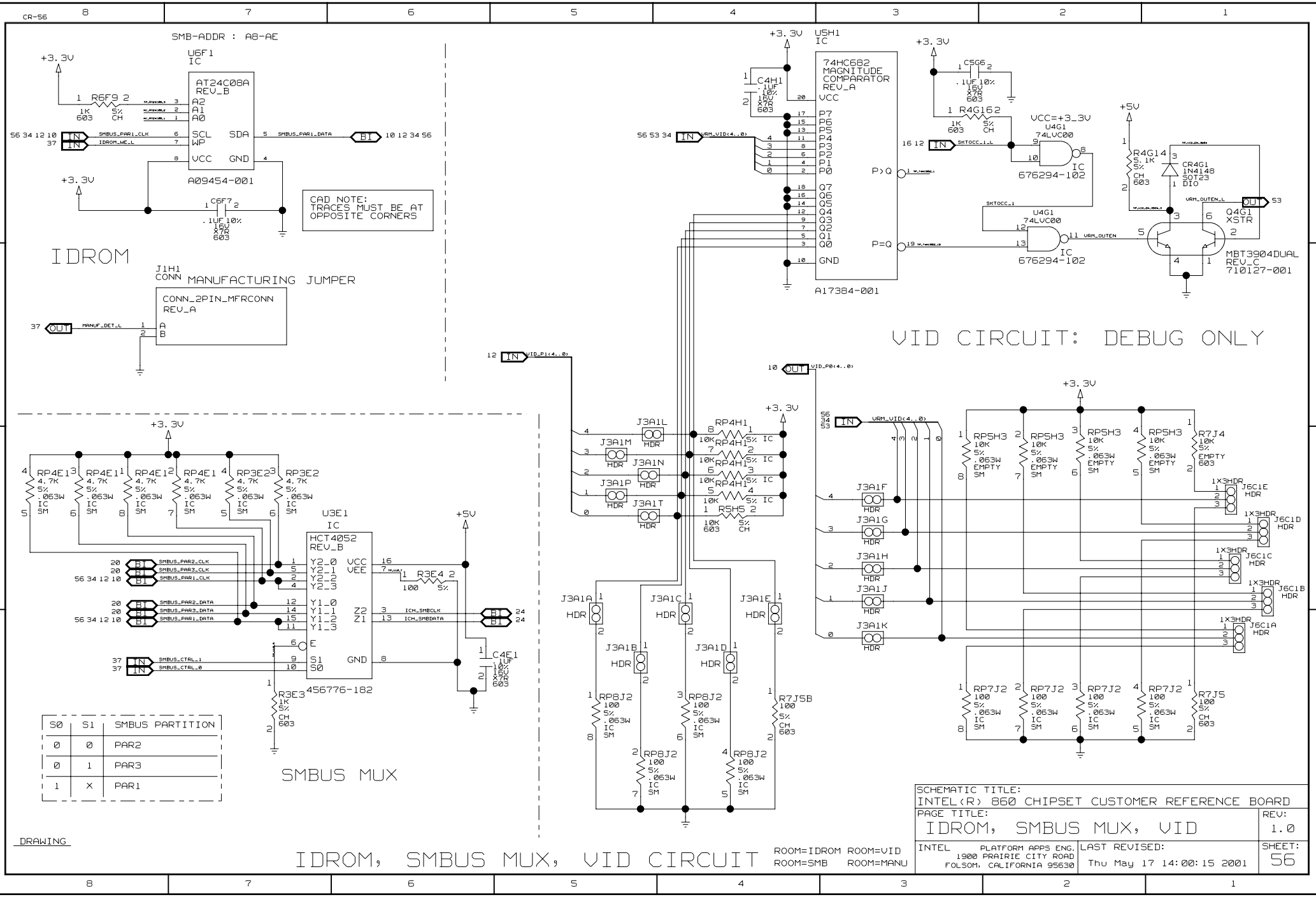


DRAWING

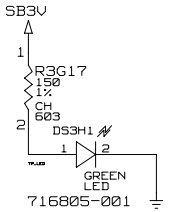
FAN CONTROL

ROOM=FAN_CONTROL

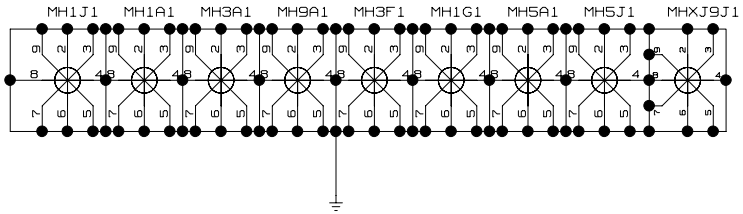
SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD	
PAGE TITLE: FAN CONTROL	REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:20 2001
	SHEET: 55


SMB-ADDR : A8-AE
U6F1
IC
AT24C08A
REV_B
A09454-001
IDROM
CAD NOTE:
TRACES MUST BE AT
OPPOSITE CORNERS
J1H1
CONN
MANUFACTURING JUMPER
CONN_2PIN_MFRCONN
REV_A
U5H1
IC
74HC682
MAGNITUDE
COMPARATOR
REV_A
A17384-001
VID CIRCUIT: DEBUG ONLY
MBT3904DUAL
REV_C
710127-001
SMBUS MUX
HCT4052
REV_B
456776-182
SMBUS_PAR1_CLK
SMBUS_PAR2_CLK
SMBUS_PAR3_CLK
SMBUS_PAR1_DATA
SMBUS_PAR2_DATA
SMBUS_PAR3_DATA
SMBUS_CTRL_1
SMBUS_CTRL_0
ICH_SMBCLK
ICH_SMBDATA
S0 S1 SMBUS PARTITION
0 0 PAR2
0 1 PAR3
1 X PAR1
IDROM, SMBUS MUX, VID CIRCUIT
ROOM=IDROM ROOM=VID
ROOM=SMB ROOM=MANU
DRAWING
SCHEMATIC TITLE:
INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:
IDROM, SMBUS MUX, VID
REV:
1.0
INTEL PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Thu May 17 14:00:15 2001
SHEET:
56

STANDBY LED



ROOM=LED

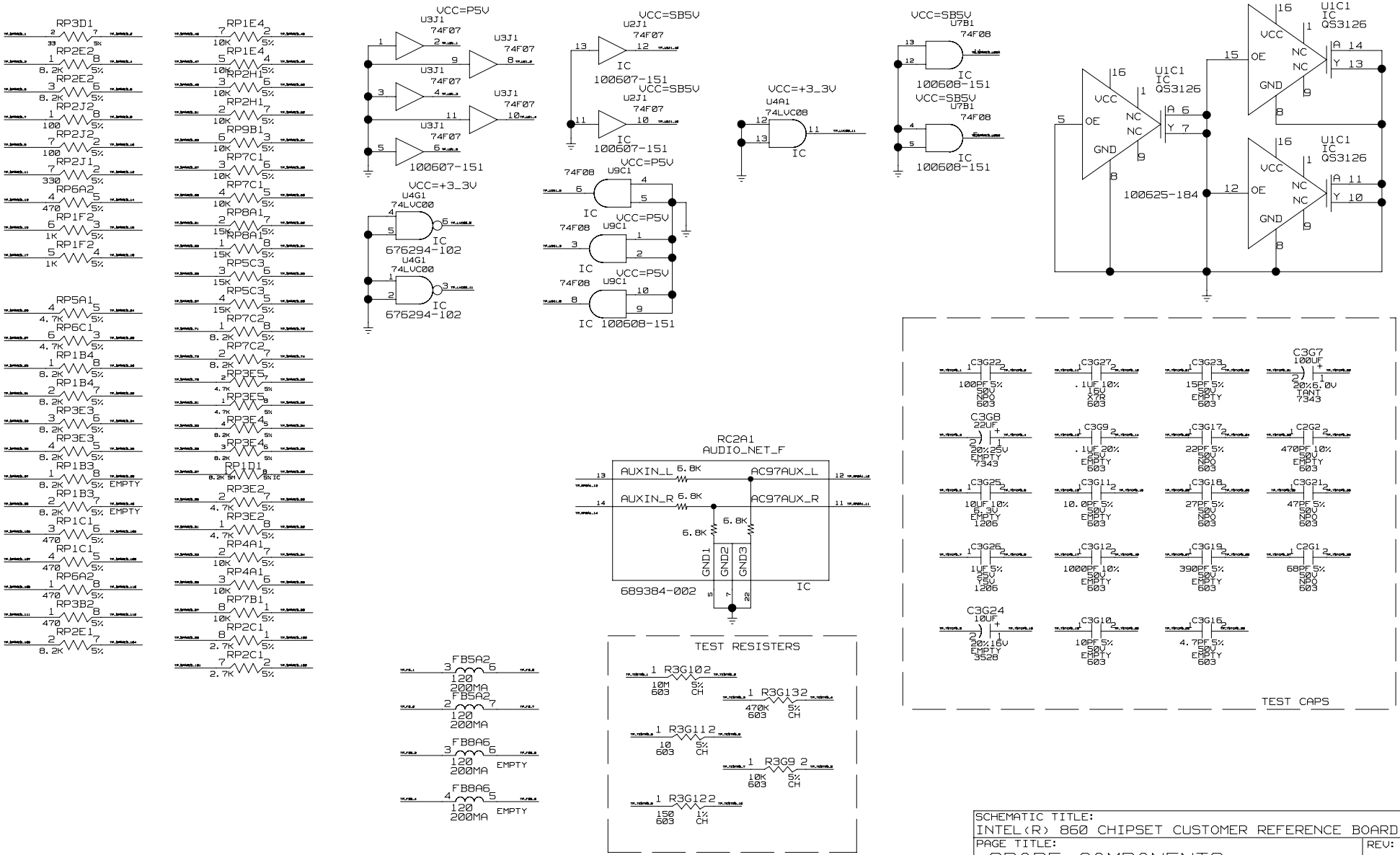


MOUNTING HOLES

DRAWING

VID JMPR'S MOUNTING HOLES, SB LED

SCHEMATIC TITLE: INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD		
PAGE TITLE: VID JMPR MNT HOLE, SB LED		REV: 1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 14:00:09 2001	SHEET: 57



DRAWING

SPARE COMPONENTS

SCHEMATIC TITLE:	INTEL(R) 860 CHIPSET CUSTOMER REFERENCE BOARD
PAGE TITLE:	SPARE COMPONENTS
REV:	1.0
INTEL PLATFORM APPS ENG. 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Thu May 17 13:59:59 2001
SHEET:	58