# Intel® 815 Chipset Family: 82815EP and 82815P Memory Controller Hub (MCH)

## Specification Update

*June 2001*

**Notice:** The Intel® 82815EP and 82815P MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290695-003

# Contents

# Revision History

| Rev. | Draft/Changes | Date |
|---|---|---|
| 001 | Initial Release | January 2001 |
| 002 | Added Intel® 82815P MCH product references.<br>Added Specification Clarifications:<br>2. The 82815EP Does Not Support Intel® Pentium® III Processors that use 0.13u Technology<br>3. The 82815EP Does Not Support Intel® Pentium® III Processors that use 0.13u Technology<br>Added Documentation Change:<br>1. 82815EP 544 BGA Ball-Out Package is Corrected | March 2001 |
| 003 | **Misc:**<br>Modified the Component Identification via Programming Interface table and the Component Marking Information table.<br>**Errata**:<br>Host Interface Buffer Noise; System Bus Snoop Logic, Asynchronous Screen Flip, System Memory Data Line Noise; System Memory Frequency Select, False Device 1 System Error Message added to indicate B0 stepping information.<br>**Specification Clarifications**:<br>Specification Clarification #4 modifies Clarification #2 to show that the B0 stepping of the 82815P/82815EP does support Intel® Pentium® III processors that use 0.13 µ technology.<br>Specification Clarification #5 is modified to include the 82815P MCH device as one of six 815 family chipsets.<br>Specification Clarification #6 modifies Clarification #3 to show that the B0 stepping of the 82815P/82815EP does support Intel® Pentium® III processors that use 0.13 µ technology. | June 2001 |

# Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

### Affected Documents/Related Documents

| Document Title | Document Number |
|---|---|
| *Intel® 815 Chipset Family: 82815EP and 82815P Memory Controller Hub (MCH)* Datasheet | 290693-002 |

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the Intel 82815EP and 82815P chipset behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Component Identification via Programming Interface

The Intel® 82815EP MCH may be identified by the following register contents:

| Stepping | Device | Vendor ID[1] | Device ID[2] | Revision Number[3] |
|---|---|---|---|---|
| A2 | 0 | 8086h | 1130h | 02h |
| | 1 | 8086h | 1131h | 02h |
| B0 | 0 | 8086h | 1130h | 04h |
| | 1 | 8086h | 1131h | 04h |

**NOTES:**
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space of Device 0, 1.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space of Device 0, 1.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space of Device 0, 1.

# Component Marking Information

The Intel 82815EP MCH can be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| A2 | SL552 | FW82815EP | Production 82815EP MCH |
| A2 | QB29 | FW82815 | Engineering Samples |
| B0 | SL5NR | FW82815EP | Production 82815EP MCH |
| B0 | QB80 | FW82815EP | Engineering Samples |
| B0 | QB81 | FW82815EP | Engineering Samples |

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel 82815EP and 82815P MCH stepping. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

| | |
|---|---|
| X: | Erratum, Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank Box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

### Status

| | |
|---|---|
| Doc: | Document change or update that will be implemented. |
| Fix: | This erratum is intended to be fixed in a future stepping of the component. |
| Fixed: | This erratum has been previously fixed. |
| No Fix | There are no plans to fix this erratum. |
| Eval | Plans to fix this erratum are under evaluation. |

### Other

| | |
|---|---|
| Shaded: | This item is either new or modified from the previous version of the document. |

| Number | SPECIFICATION CHANGES |
|---|---|
| | There are no specification changes in this Specification Update revision. |

| Number | Steppings | | Plans | ERRATA |
|---|---|---|---|---|
| | A2 | B0 | | |
| 1 | X | | Fix | Host Interface Buffer Noise |
| 2 | X | | No Fix | System Memory Data Line Noise Erratum |
| 3 | X | | No Fix | System Memory Frequency Select Erratum |
| 4 | X | | No Fix | False Device 1 System Error Message Erratum |
| 5 | X | X | No Fix | System Bus Snoop Logic |
| 6 | X | X | No Fix | Asynchronous Screen Flip |

| Number | Stepping | | SPECIFICATION CLARIFICATIONS |
|---|---|---|---|
| | A2 | B0 | |
| 1 | X | | Display Power Signals |
| 2 | X | | The 82815EP Does Not Support Intel® Pentium® III Processors that use 0.13 µ Technology |
| 3 | X | | The 82815EP Does Not Support Intel® Pentium® III Processors that use 0.13 µ Technology |
| 4 | | X | Support of Intel® Pentium® III Processors That Use 0.13 µ Technology |
| 5 | | X | Chipsets in the Intel® 815 Chipset Family |
| 6 | | X | Support of Intel® Pentium® III Processors That Use 0.13 µ Technology |

| Number | DOCUMENTATION CHANGES |
|---|---|
| 1 | 82815EP 544 BGA Ball-Out Package is Corrected |

# Specification Changes

There are no specification changes in this Specification Update revision.

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# Errata

## 1. Host Interface Buffer Noise

**Problem:** False assertions of H_ADS# signal observed on-die on the A-2 stepping of the Intel 815EP chipset (MCH).

**Implication:** System hangs or boot failures can occur with A-2 stepping of Intel 815EP chipset based platforms.

**Workaround:** Increase spacing between nearest neighbor system memory and GTL+ buffers. Reduce System Memory buffer strength settings for 100/133.

**Status:** The Root Cause of this errata was found to be cross coupling of system memory signals onto nearest neighbor GTL+ signals (specifically H_ADS#) on the board, package, & die. The A-2 stepping of the Intel 815EP chipset will include circuit changes to improve the noise immunity of GTL+ buffers.

## 2. System Memory Data Line Noise Erratum

**Problem:** When the Intel 82815EP A-2 step MCH has multiple system memory data lines transition from low to high, a glitch can appear on non-switching data lines.

**Implication:** The erratum is amplified by trace impedance and discontinuities on the motherboard and DIMM. When measured at the SDRAM pin, it can violate the published Vil specification of SDRAM components in the valid timing window. In this case, incorrect data could be clocked into the SDRAM causing data corruption.

**Workaround:** To minimize amplification of the glitch on the board:

- Follow published design specifications detailed in the Intel 82815EP Chipset Platform Design Guide, dated November 2000, NDA, para 5.2 and 5.4.
- Implement buffer strength and System Memory RCOMP settings documented in the Intel 82815 GMCH BIOS Specification Update, rev 0.76.

**Status:** There are no plans to fix this erratum in silicon.

## 3. System Memory Frequency Select Erratum

**Problem:** Register 50H (GMCHCFG) bit 2 of the Intel 82815EP A-2 step is set incorrectly when a 66 MHz Front Side Bus processor is plugged into the system.

**Implication:** When the Intel 82815EP MCH A-2 step sets this bit at reset with a 66 MHz Front Side Bus processor plugged into the system, this bit will be set incorrectly.

**Workaround:** BIOS must detect if a 66 MHz Front Side Bus processor is plugged into the system and set this bit to ‘0’ to indicate 100 MHz system memory.

**Status:** There are no plans to fix this erratum in silicon.

### 4. False Device 1 System Error Message Erratum

**Problem:** A false Signal System Error (SERR) is generated when Device 1 system error signaling is enabled. The false SERR results in the generation of a Non-Maskable Interrupt (NMI).

**Implication:** A false error is detected and the system may halt.

**Workaround:** Disable Device 1 SERR Message Enable by setting PCICMD1 - PCI-PCI Command Register (Device 1), address offset 04h-05h, bit [8] to "0". This is the existing BIOS default setting for this bit.

**Status:** There are no plans to fix this erratum in silicon.

### 5. System Bus Snoop Logic

**Problem:** Under specific sequence of bus cycles, data from the wrong address may be returned to the graphics controller. This can occur if the following three conditions align:

1. Back-to-back ADS# on the system bus
2. PHOLD (ISA Master) access on the hub interface
3. External graphics AGP snoop OR internal graphics cacheable BLTs/Store DWORD.

**Implication:** If the data from the wrong address is returned to the graphics controller, either graphics corruption or system hang can occur.

**Workaround:** None

**Status:** This Issue has only been observed in a System Validation Environment with a specific focus test. This issue has not been observed with any real applications tested. There are no plans to fix this erratum in silicon.

### 6. Asynchronous Screen Flip

**Problem:** When the Intel 815 chipset is configured for asynchronous screen flipping, under certain timing-dependent circumstances the display engine may temporarily read pixel data from a random memory location.

**Implication:** When changing display surfaces using the asynchronous screen flipping, subtle display corruption is seen in the form of short, somewhat random colored, horizontal lines along the left side of the screen.

**Workaround:** Driver version 4.1.1 does, and future versions will, disable asynchronous screen flipping for commonly used 3D resolutions.

**Status:** There are no plans to fix this erratum in silicon.

# Specification Clarifications

## 1. Display Power Signals

Reference the Intel 815EP Chipset Family: 82815EP Memory Controller Hub (MCH) Datasheet, dated November 2000, Document Reference Number 290693-001.

Page 28, para 2.5, Power Signals: The description for signal name VCCDA is changed as follows:

"Display Power Signal (Connect to an isolated 1.85V plane with VCCDACA1 and VCCDACA2.) Note that VCCDA, VCCDACA1, and VCCDACA2 provide display power for integrated graphics in an 815E platform. In an 815EP platform these power circuits provide bias to the core voltage and therefore must be retained in an 815EP platform."

## 2. The 82815EP Does Not Support Intel® Pentium® III Processors That Use 0.13 µ Technology

Reference the 82815EP MCH Features, Processor/Host Bus Support. Insert the following item in the list:

- Does not support Pentium III processors that use 0.13 µ technology.

## 3. The 82815EP Does Not Support Intel® Pentium® III Processors That Use 0.13 µ Technology

Reference Section 1.4, *Host Interface*. Add the following information to the first paragraph:

The 82815EP MCH will not support Pentium III processors that use 0.13 micron technology. These processors should not be placed in platforms using the 82815EP MCH. Future versions of the Intel® 815 chipset family will support Pentium III processors that use 0.13 micron technology.

## 4. Support of Intel® Pentium® III Processors That Use 0.13 µ Technology.

Reference the 82815EP/82815P MCH Features, Processor/Host Bus Support. Insert the following items in the list:

- The A2 Stepping does not support Pentium III processors that use 0.13 µ technology.
- The B0 Stepping does support Pentium III processors that use 0.13 µ technology

## 5. Chipsets in the Intel® 815 Chipset Family

Reference Section 1, *Overview*. Insert the following material to replace the paragraph beginning, "There are two chipsets…"

There are six chipsets in the Intel® 815 chipset family:

- Intel® 82815 chipset: This chipset contains the Intel 82815 and the Intel 82801AA (ICH).
- Intel® 82815E chipset: This chipset contains the Intel 82815E and the Intel 82801BA (ICH2).
- Intel® 82815P chipset. This chipset contains the Intel 82815P and the Intel 82801BA (ICH2). There is no internal graphics capability. This MCH uses an AGP port only.
- Intel® 82815EP chipset: This chipset contains the Intel 82815EP and theIntel 82801BA (ICH2). There is no internal graphics capability. This MCH uses an AGP port only.
- Intel® 82815G chipset: This chipset contains the Intel 82815G GMCH and Intel 82801AA (ICH). There is no AGP port capability and no display cache capability. This GMCH uses internal graphics only.
- Intel® 82815EG chipset. This chipset contains the Intel 82815EG GMCH and Intel 82801BA (ICH2). There is no AGP port capability and no display cache capability. This GMCH uses internal graphics only.

***Note:*** The only component difference between the Intel 82815 GMCH and the Intel 82815E GMCH is the I/O Controller Hub. The only component difference between the Intel 82815P MCH and the Intel 82815EP MCH is the I/O Controller Hub. The only component difference between the Intel 82815G GMCH and the Intel 82815EG GMCH is the I/O Controller Hub.

## 6. Support of Intel® Pentium® III Processors That Use 0.13 µ Technology

Reference Section 1.4, *Host Interface*. Add the following information to the first paragraph:

The Intel 82815P/82815EP MCH A2 stepping will not support Pentium III processors that use 0.13 µ technology. These processors should not be placed in platforms using the A2 stepping of the Intel 82815P/82815EP MCH. The B0 stepping of the Intel 82815P/82815EP MCH will support Pentium III processors that use 0.13 µ technology.

# Documentation Changes

## 1. 82815EP 544 BGA Ball-Out Package is Corrected

Reference Section 5.2, *Package Information*. Replace Figure 13 with the following correct 544 BGA ball-out package bottom view: