Intel® 860 Chipset: 82860 Memory Controller Hub (MCH)

Specification Update

May 2001

Notice: The Intel® 860 chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290715-001

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	May 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 860 Chipset: 82860 Memory Controller Hub (MCH) Datasheet	290713-001

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® 82860 MCH, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 82860 MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A3	8086h	2531h	04h

NOTES:

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The 82860 MCH may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
A3	QB78ES	SL5HB	KC82860	

Summary Table of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82860 MCH stepping. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
No Fix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.

Other

Shaded:	This item is either new or modified from the previous version of the document.

NO.	SPECIFICATION CHANGES
1	There are no specification changes in this specification update revision

NO.	A3	PLANS	ERRATA
1	X	NoFix	Suspend to RAM (S3) Entry
2	X	NoFix	Direct RDRAM NAP Mode
3	X	NoFix	Invalid Graphic Aperture Access
4	X	NoFix	VDDQ Leakage
5	X	NoFix	Sustained PCI Bandwidth
6	X	NoFix	RDRAM* Device Interface Initiate Initialization Operation (IIO) Bit
7	X	NoFix	Simultaneous Clear/Set on Hub Interface Parity Error
8	X	NoFix	System Hang when using MRH-R
9	X	NoFix	Split Lock Cycles
10	X	NoFix	Writes Passing Reads on an AGP Fence Command
11	X	NoFix	Lock Cycle Hang
12	X	NoFix	APIC Cluster Mode

NO.	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications in this specification update revision

NO.	DOCUMENTATION CHANGES
	There are no documentation changes in this specification update revision

Specification Changes

There are no specification changes in this specification update revision.

This page is intentionally left blank.

Errata

1. Suspend to RAM (S3) Entry

Problem: In the Intel 82860 MCH, a boundary condition between the “S3” (Suspend to RAM) state entry and a regularly scheduled refresh request causes the bank counter to miss an increment, leaving some banks in a non-precharged state. As a result these banks are not refreshed during the S3 state.

Implication: This erratum may cause data corruption and/or system hang upon resume from a power down state (S3/STR).

Workaround: System BIOS must ensure all banks are closed before executing the memory power down sequence. Reference the latest revision of the Intel 82860 BIOS Specification and Specification Update for details on implementing this workaround.

Status: Intel has no fix planned for this erratum.

2. Direct RDRAM NAP Mode

Problem: With NAP mode enabled, the MCH may hang causing an infinite number of random cycles to be issued to the memory interface.

Implication: NAP mode is not functional.

Workaround: None identified. The NAP feature should not be used.

Status: Intel has no fix planned for this erratum.

3. Invalid Graphic Aperture Access

Problem: Memory write accesses through the graphic aperture targeted above TOP memory or invalid memory location will cause the system to hang.

Implication: If an invalid graphic aperture access executed, the system will hang. Below are two scenarios that could cause an invalid graphic aperture translation:

- Write to aperture with entry marked as "invalid"
- Write to aperture with entry marked as "valid", but does not point to physical memory

Workaround: None.

Status: Intel has no fix planned for this erratum.

4. VDDQ Leakage

Problem: If the 1.5 V supply for the MCH's VDDQ voltage is turned off (set to 0) and the 1.8 V supply for the MCH is on (set to 1.8 V), an internal diode within the MCH will be forward biased. This will cause leakage into the VDDQ power plane, approximately 1 V.

Implication: During normal operations, this diode is not forward biased and has a leakage current of only 10 μA.

Workaround: Turn off and power on VCC1_8 and VDDQ at the same time. Follow the MCH power sequencing requirements documented in the platform design guide.

Status: Intel has no fix planned for this erratum.

5. Sustained PCI Bandwidth

Problem: During a memory read multiple operation, a PCI master will read more than one complete cache line from memory. In this situation, the MCH pre-fetches information from memory to provide optimal performance. However, the MCH cannot provide information to the PCI master fast enough. Therefore, the ICH2 terminates the read cycle early to free up the PCI bus for other PCI masters to claim.

Implication: The early termination limits the maximum bandwidth to ~90 MB/s.

Workaround: None

Status: Intel has no fix planned for this erratum.

6. RDRAM* Device Interface Initiate Initialization Operation (IIO) Bit

Problem: The Initiate Initialization Operation (IIO) bit in the RDRAM initialization control management (RICM) register may be cleared by the MCH too early.

Implication: If the MCH clears the bit too early and BIOS immediately issues a new initialization op code (IOP), the MCH may incorrectly control the RDRAM device CMD signal causing an invalid cycle to write to the memory subsystem, and the IIO bit may not be cleared. This results in a system hang during the memory initialization process.

Workaround: BIOS must allow at least 1 μs delay between executing initialization opcodes (IOP).

Status: Intel has no fix planned for this erratum.

7. Simultaneous Clear/Set on Hub Interface Parity Error

Problem: If a Hub Interface error occurs, the MCH will set an error status flag for the offending Hub Interface. When the status flag transitions from a 0 to a 1, the MCH will generate an SERR (if enabled) and the ICH2 will generate an NMI to the processor. If an NMI handler clears the status flag on exactly the same clock as the MCH is trying to set the flag for a second NMI, the status flag will remain set at a 1 and a second NMI will not be generated.

Implication: This erratum was discovered using Intel test cards and has not been seen with real world applications. It is thought that most OS's do not try to recover from an NMI.

Workaround: A specialized HAL can be written that clears the status flag and then checks to ensure that the status flag is indeed cleared before exiting the handler.

Status: Intel has no fix planned for this erratum.

8. System Hang when using MRH-R

Problem: System may hang when using MRH-R components where both stick channels of each MRH-R are populated.

Implication: System may hang

Workaround: Set bit 7 of register offset 09Fh in device 0.

Status: Intel has no fix planned for this erratum.

9. Split Lock Cycles

Problem: When two locked cycles to a write only PAM region are issued and are followed by 2 writes to the same region (these are redirected to RDRAM*) the MCH will lock up.

Implication: The system will hang

Workaround: BIOS should not issue locked cycles to write only PAM regions during boot time.

Status: Intel has no fix planned for this erratum.

10. Writes Passing Reads on an AGP Fence Command

Problem: When using the AGP Fence command the sequence of read … Fence … write may not keep the write from passing the read. Other fence sequences are unaffected.

Implication: Incorrect data may be read.

Workaround: AGP Graphics Card drivers should not use the Fence command.

Status: Intel has no fix planned for this erratum.

11. Lock Cycle Hang

Problem: The problem occurs when the processor issues two consecutive lock cycles directed toward the Intel P64H (or ICH2). During the first lock cycle the MCH must have at least 6 memory read transactions posted by the P64H (or ICH2) and an ICH2 DMA transaction in progress. This ICH2 DMA must be targeted toward main memory by the 8237 DMA controller in the ICH2, an LPC SIO device, or ISA device.

Implication: The above conditions will lead to system lockup. The conditions required for this erratum to occur appear to be unlikely in actual PC systems. In many hours of testing on a number of actual PC systems, Intel did not observe this erratum. However, customers should be aware of this erratum and determine its potential applicability to their system configuration.

Workaround: None identified.

Status: Intel has no fix planned for this erratum.

12. APIC Cluster Mode

Problem: APIC Cluster Mode does not work

Implication: An OS that tries to use cluster mode may not work

Workaround: None

Status: Intel has no fix planned for this erratum

Specification Clarifications

There are no specification clarifications in this specification update revision.

This page is intentionally left blank.

Documentation Changes

There are no documentation changes in this specification update revision