Intel® 815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH)

For Use with Universal Socket 370

Specification Update

December 14, 2001

Notice: The Intel® 82815P/82815EP MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290726-001

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Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	December 14, 2001

Preface

This Specification Update document is an update to the specifications contained in the *Intel® 815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH) For Use with Universal Socket 370 Datasheet, #290720-001*. The datasheet and other associated documents are listed in the following Affected Documents/Related Documents table. This document is a compilation of device specification changes, device errata, specification clarifications, and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document. This document will contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 815 Chipset Family: 82815P/82815EP Memory Controller Hub (MCH) For Use with Universal Socket 370 Datasheet (Public, Sep 2001)	290720-001

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel 82815G/EG behavior to deviate from published specifications. Hardware and software that are designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® 82815P/82815EP MCH may be identified by the following register contents:

Stepping	Device	Vendor ID[1]	Device ID[2]	Revision Number[3]
B0	0	8086h	1130h	04h
	1	8086h	1131h	04h

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space of Device 0, 1.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space of Device 0, 1.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space of Device 0, 1.

Component Marking Information

The Intel 82815P/82815EP MCH can be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B0	QB81	FW82815P	Engineering Sample
B0	SL5NR	FW82815P	Production 82815P/82815EP MCH

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel® 82815P/82815EP GMCH stepping. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
No Fix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.

Other

Shaded:	This item is either new or modified from the previous version of the document.

Number	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision

Number	Steppings	Plans	ERRATA
	BO		
1	X	No Fix	Host Interface Buffer Noise
2	X	No Fix	System Bus Snoop Logic
3	X	No Fix	Asynchronous Screen Flip
4	X	No Fix	System Memory Data Line Noise
5	X	No Fix	System Memory Frequency Select
6	X	No Fix	False Device 1 System Error Message

Number	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications in this Specification Update revision

Number	DOCUMENTATION CHANGES
	There are no documentation changes in this Specification Update revision

Specification Changes

There are no specification changes in this Specification Update revision.

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Errata

1. Host Interface Buffer Noise

Problem: False assertions of H_ADS# signal are observed on-die of the Intel 815 chipset (GMCH).

Implication: System hangs or boot failures can occur with Intel 815 chipset-based platforms.

Workaround: Increase spacing between nearest neighbor system memory and GTL+ buffers. Reduce System Memory buffer strength settings for 100/133 MHz.

Status: The root cause of this erratum was found to be cross coupling of system memory signals onto nearest neighbor GTL+ signals (specifically H_ADS#) on the board, package, and die. Future steppings of the Intel 815 chipset may include circuit changes to improve the noise immunity of GTL+ buffers. There are no plans to fix this erratum in silicon.

2. System Bus Snoop Logic

Problem: Under specific sequence of bus cycles, data from the wrong address may be returned to the graphics controller. This can occur if the following three conditions align:

1. Back-to-back ADS# on the system bus
2. PHOLD (ISA Master) access on the hub interface
3. External graphics AGP snoop OR internal graphics cacheable BLTs/Store DWORD.

Implication: If the data from the wrong address is returned to the graphics controller, either graphics corruption or system hang can occur.

Workaround: None

Status: This Issue has only been observed in a System Validation Environment with a specific focus test. This issue has not been observed with any real applications tested. There are no plans to fix this erratum in silicon.

3. Asynchronous Screen Flip Erratum

Problem: When the Intel 815 chipset is configured for asynchronous screen flipping, under certain timing-dependent circumstances the display engine may temporarily read pixel data from a random memory location.

Implication: When changing display surfaces using the asynchronous screen flipping, subtle display corruption is seen in the form of short, somewhat random colored, horizontal lines along the left side of the screen.

Workaround: Driver version 4.1.1 does, and future versions will, disable asynchronous screen flipping for commonly used 3D resolutions.

Status: There are no plans to fix this erratum in silicon.

4. System Memory Data Line Noise Erratum

Problem: When the Intel 82815 GMCH has multiple system memory data lines transition from low to high, a glitch can appear on non-switching data lines.

Implication: The erratum is amplified by trace impedance and discontinuities on the motherboard and DIMM. When measured at the SDRAM pin, it can violate the published Vil specification of SDRAM components in the valid timing window. In this case, incorrect data could be clocked into the SDRAM causing data corruption.

Workaround: To minimize amplification of the glitch on the board:

- Follow published design specifications detailed in *the Intel® 82815 Chipset Platform Design Guides*.
- Implement buffer strength and System Memory RCOMP settings documented in the latest version of the *Intel® 82815 GMCH BIOS Specification Update*.

Status: There are no plans to fix this erratum in silicon.

5. System Memory Frequency Select

Problem: Register 50H (GMCHCFG) bit 2 of the Intel 82815 is set incorrectly when a 66 MHz Front Side Bus processor is plugged into the system.

Implication: When the Intel 82815 GMCH sets this bit at reset with a 66 MHz Front Side Bus processor plugged into the system, this bit will be set incorrectly.

Workaround: BIOS must detect if a 66 MHz front side bus processor is plugged into the system and set this bit to '0' to indicate 100 MHz system memory.

Status: There are no plans to fix this erratum in silicon.

6. False Device 1 System Error Message

Problem: A false Signal System Error (SERR) is generated when Device 1 system error signaling is enabled. The false SERR results in the generation of a Non-Maskable Interrupt (NMI).

Implication: A false error is detected and the system may halt.

Workaround: Disable Device 1 SERR Message Enable by setting PCICMD1 - PCI-PCI Command Register (Device 1), address offset 04h-05h, bit [8] to "0". This is the existing BIOS default setting for this bit.

Status: There are no plans to fix this erratum in silicon.

Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

There are no documentation changes in this Specification Update revision.