intel®

82380AB (MISA) Docking PCIset

Specification Update

March 1999

Order Number: 297657-001

Contents

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Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	March 1999

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Preface

This document is an update to the specifications contained in the Intel® 380FB PCIset: 82380AB Mobile PCI-To-ISA Bridge (MISA) Datasheet, order number (290563). It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the 82380FB PCIset Datasheet.

Errata are design defects or errors. Errata may cause the 82380AB PCIsets, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Marking Information

The 82380FB PCIset may be identified by the following component markings:

Component	Stepping	S-Spec	Top Marking	Notes
MISA 82380AB	A-0	S U095	SB823080AB U095	Production

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed 82380AB (MISA) Docking PCIset steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

82380AB MISA

Device	NO.	A0	Plans	SPECIFICATION CHANGES
				There are currently no known Specification Changes.

Device	NO.	A0	Plans	ERRATA
MISA	1	x	NoFix	DSPWRG must be synchronized
MISA	2	x	NoFIx	MISA REFRESH# does not met ISA specification pull-up @ 300 ohms

Device	NO	A0	Plans	DOCUMENTATION CHANGES
MISA	1	x	Doc	8-bit I/O Recovery Time
MISA	2	x	Doc	Pin Correction

Specification Changes

There are currently no known Specification Changes.
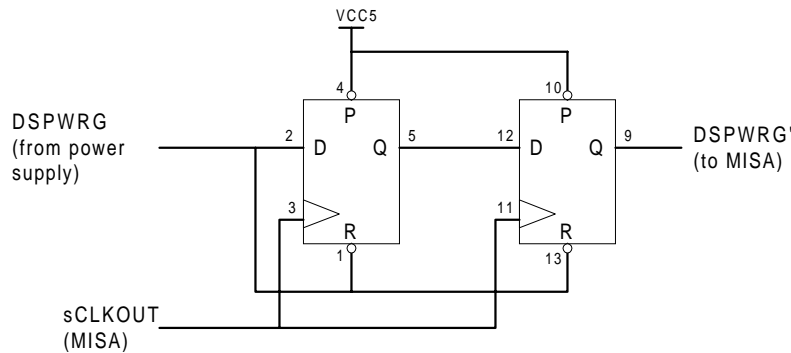
Errata

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1.   **DSPWRG must be synchronized.**

Problem: DSPWRG does not reset the device as expected if the PCICLK is not running when DSPWRG is asserted.

Implication: The MISA device will not function correctly.

Workaround: The following circuit will delay DSPWRG until PCICLK is running at MISA.

Status: This will not be fixed in a future stepping.

2.   **REFRESH# pull-up does not meet ISA specification @ 300 ohms**

Problem: ISA specification requires REFRESH# IOL capable of driving with 300 ohms pull-up, but the MISA does not meet this requirement.

Implication: With a 300ohm pull-up MISA may not meet VOL specification and ISA devices may not properly sample this signal asserted. Intel has received no complaints of system falling for this cause, additionally Intel believes there is no reliability risk for those systems with 300ohm pull-up's all ready in the field.

Workaround: The IOL specification will change from 2mA to 6mA and a 1K ohm external pull-up will be recommended for REFRESH#. This new IOL specification and resistor pull-up still will not meet the ISA specification.

Status: This will not be fixed in on MISA.

Documentation Changes

1.   **8-Bit I/O Recovery Time**

Bit	Bit Functions	Descriptions
5:3	8-bit I/O Recovery Times	This 3-bit field defines the recovery times for 8-bit I/O cycles. Programmable delays between back-to-back 8-bit PCI cycles to an ISA I/O slave is shown in terms of additional ISA clock recovery cycles (SYSCLK). The selected delay programmed into this field is enabled or disabled through bit 6 of this register. **Bits 5 4 3** **SYSCLK** 0 0 1 1 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 1 1 1 7 **0 0 0** **8**

2.   **Pin Correction**

On page 16, of the MISA datasheet (Order Number 290563-001) Figure 2, 82380AB MISA Pinout, Pin# 114 should read Vss and Pin#113 should read Vcc. On page 18, Table 2, MISA Alphabetical Pin assignement, some pins are mislabeled. See the table below for correct pin assignment shaded in gray:

Table 2. MISA Alphabetical Pin Assignment

NAME	PIN	TYPE
SMEMW#	26	O
STOP#	96	s/t/s
SYSCLK	9	O
TC	63	O
TESTIN#	64	I
TRDY#	94	s/t/s
ZEROWS#	16	I
Vcc	1	
Vcc	21	

vcc	39	
Vcc	59	
Vcc	69	
Vcc	75	
Vcc	81	
Vcc	91	
Vcc	97	
Vcc	103	
Vcc	113	
Vcc	119	
Vcc	125	
Vcc	139	
Vcc	149	
Vcc	159	
Vss	2	
Vss	10	
Vss	22	
Vss	40	
Vss	60	
Vss	70	
Vss	76	
Vss	82	
Vss	92	
Vss	98	
Vss	104	
Vss	114	
Vss	120	
Vss	**126**	
Vss	140	
Vss	150	
Vss	160	

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